原程序：

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 2019/10/28 11:49:18

// Design Name:

// Module Name: Translator

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module Translator(

input [2:0] G,

input [2:0] A,

output [7:0] Y

);

wire temp=(!G[2])&(!G[1])&G[0];

assign Y[0]=!(temp&!A[2]&!A[1]&!A[0]);

assign Y[1]=!(temp&!A[2]&!A[1]&A[0]);

assign Y[2]=!(temp&!A[2]&A[1]&!A[0]);

assign Y[3]=!(temp&!A[2]&A[1]&A[0]);

assign Y[4]=!(temp&A[2]&!A[1]&!A[0]);

assign Y[5]=!(temp&A[2]&!A[1]&A[0]);

assign Y[6]=!(temp&A[2]&A[1]&!A[0]);

assign Y[7]=!(temp&A[2]&A[1]&A[0]);

endmodule

仿真：

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 2019/10/28 11:50:15

// Design Name:

// Module Name: sim4

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module sim4(

output [7:0] Y

);

reg[2:0] G,A;

initial

begin

G=3'b001;

A=3'b000;

end

always #10

begin

A=A+1;

end

trans sim(G,A,Y);

endmodule

约束：

set\_property IOSTANDARD LVCMOS33 [get\_ports {A[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {A[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {A[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {G[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {G[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {G[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {Y[7]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {Y[6]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {Y[5]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {Y[4]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {Y[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {Y[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {Y[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {Y[0]}]

set\_property PACKAGE\_PIN P2 [get\_ports {A[2]}]

set\_property PACKAGE\_PIN R2 [get\_ports {A[1]}]

set\_property PACKAGE\_PIN M4 [get\_ports {A[0]}]

set\_property PACKAGE\_PIN P5 [get\_ports {G[2]}]

set\_property PACKAGE\_PIN P4 [get\_ports {G[1]}]

set\_property PACKAGE\_PIN P3 [get\_ports {G[0]}]

set\_property PACKAGE\_PIN F6 [get\_ports {Y[7]}]

set\_property PACKAGE\_PIN G4 [get\_ports {Y[6]}]

set\_property PACKAGE\_PIN G3 [get\_ports {Y[5]}]

set\_property PACKAGE\_PIN J4 [get\_ports {Y[4]}]

set\_property PACKAGE\_PIN H4 [get\_ports {Y[3]}]

set\_property PACKAGE\_PIN J3 [get\_ports {Y[2]}]

set\_property PACKAGE\_PIN J2 [get\_ports {Y[1]}]

set\_property PACKAGE\_PIN K2 [get\_ports {Y[0]}]









