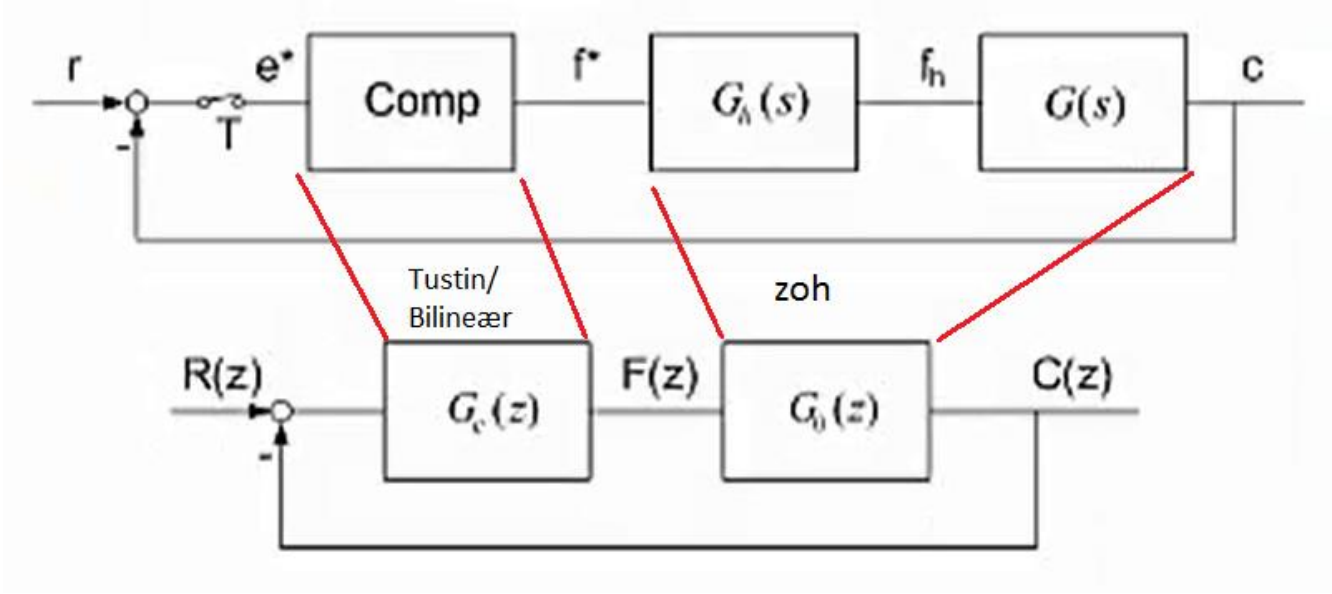
## Design process

Design forgår i S-domæne med bodeplots!

Controller dimensioneres i S-domæne, statiske og dynamiske krav ☺

Z-transformation udføres => differensligning => implementering på uProcessor.

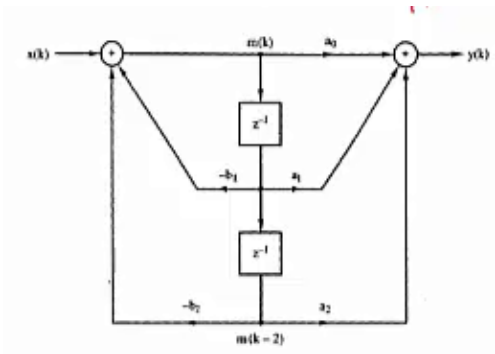


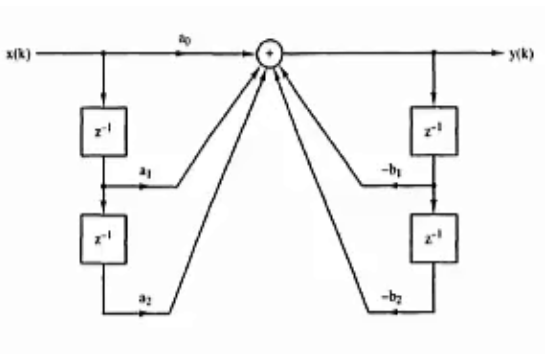

Td opstår pga. sampling, $T_d = \frac{T_s}{2}$

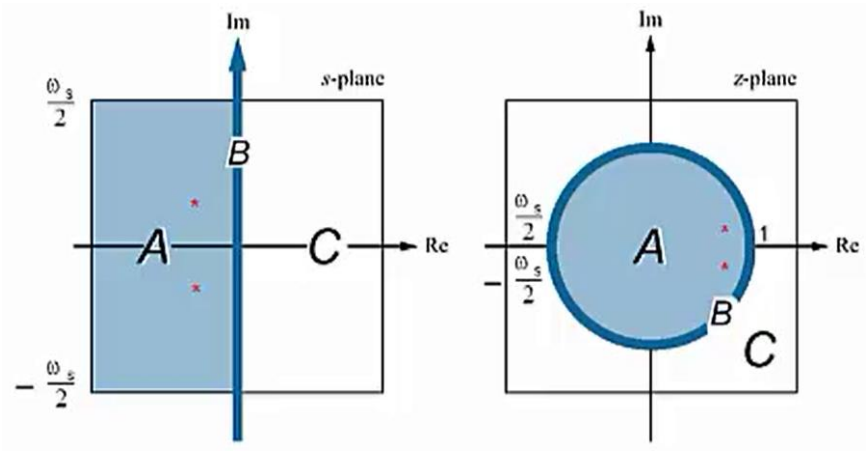
$\phi_{fs} = \omega * \frac{T_s}{2} * \frac{rad}{s}$

Ved høj samplingsfrekvens kan $T_{proc}$ udgøre en væsentlig andel,

Fingerregel : $T_{proc} < 0.15 * T_d$



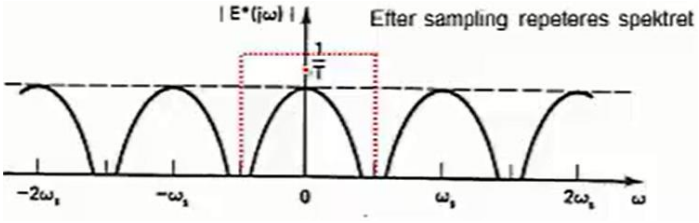





Ved høj fs går s mod $1\angle 0\ deg$, fare for afrunding

$$z = e^{sT},\ s = \alpha + j\omega \Rightarrow z = e^{\alpha T - j\omega T} = e^{\alpha T} e^{j\omega T}$$

Spejling forekommer, derfor ønskes ideelt lavpas filter for at undgå forvrængning af A/D konvertering.




Ikke ideelt lavpas => sinc => spektral forvridning. ☹

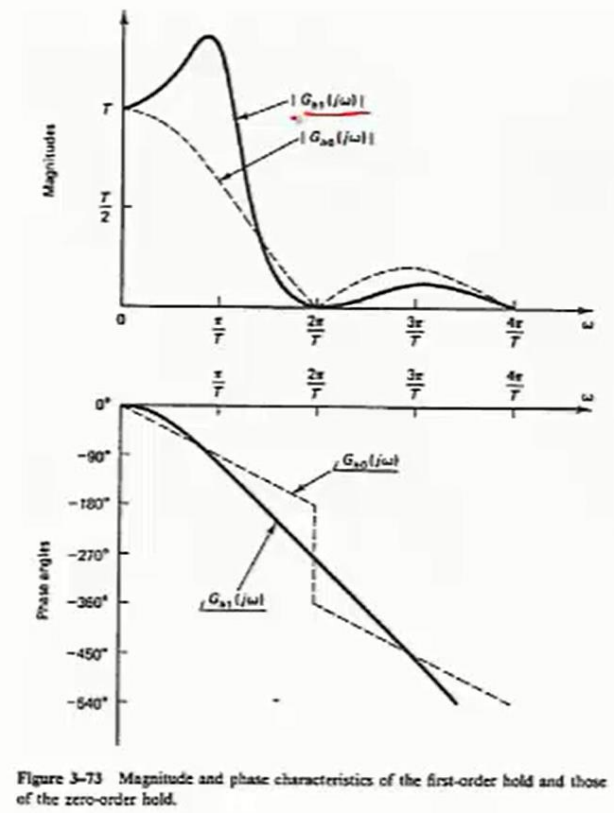



Figure 3–73 Magnitude and phase characteristics of the first-order hold and those of the zero-order hold.