VE 320 Fall 2021

Introduction to Semiconductor Devices

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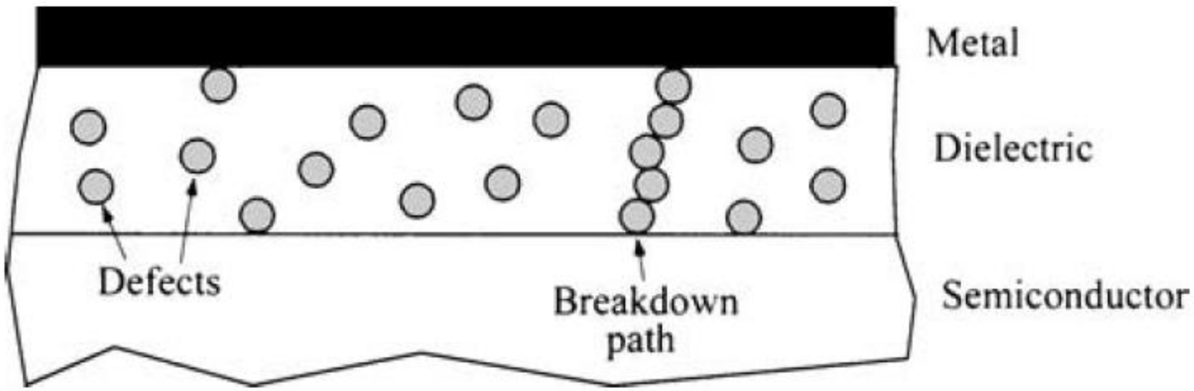
Lecture 15

MOSFET
(Chapter 11)

MOSFET: Breakdown

Breakdown mechanisms:

- Oxide breakdown: electric field in the oxide is large enough, oxide becomes conductive
  - Breakdown field ~ 6×10^6 V/cm: for a 50 nm thick oxide layer, need 30V gate voltage to cause the breakdown
  - Not reversible, catastrophic failure, defect generation due to energetic carriers
  - Time to breakdown t_{BD}



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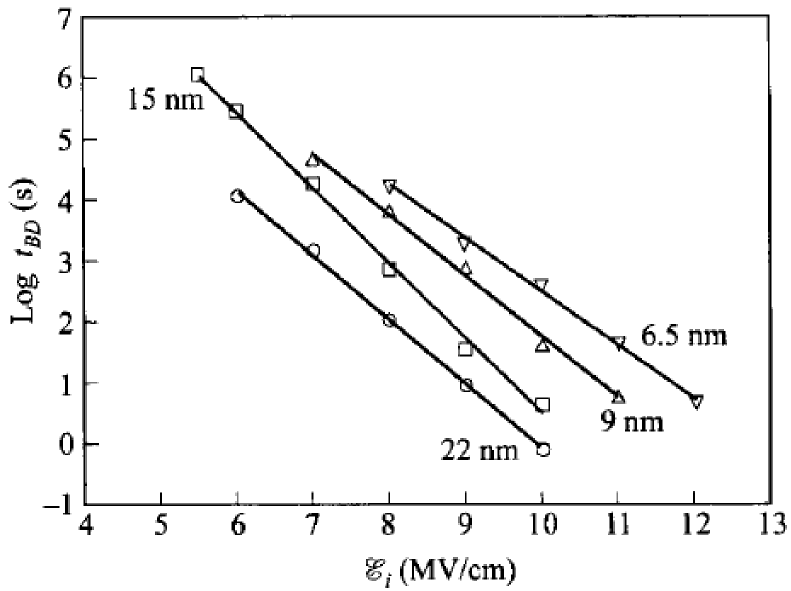

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- Avalanche breakdown: impact ionization in the space charge region near the drain terminal
  - Reverse-biased pn junction
  - If a p-type substrate doping is $N_a = 3 \times 10^{16}$ cm^{-3}, the pn junction breakdown voltage would be approximately 25 V for a planar junction
  - Actually… The electric field in the depletion region tends to be concentrated at the curvature, which lowers the breakdown voltage

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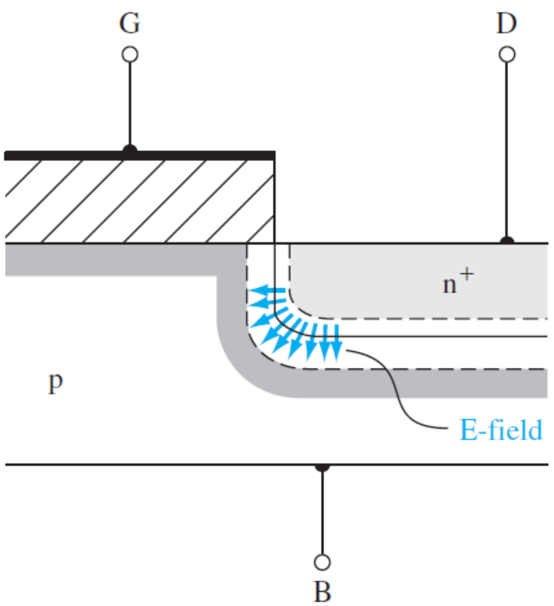
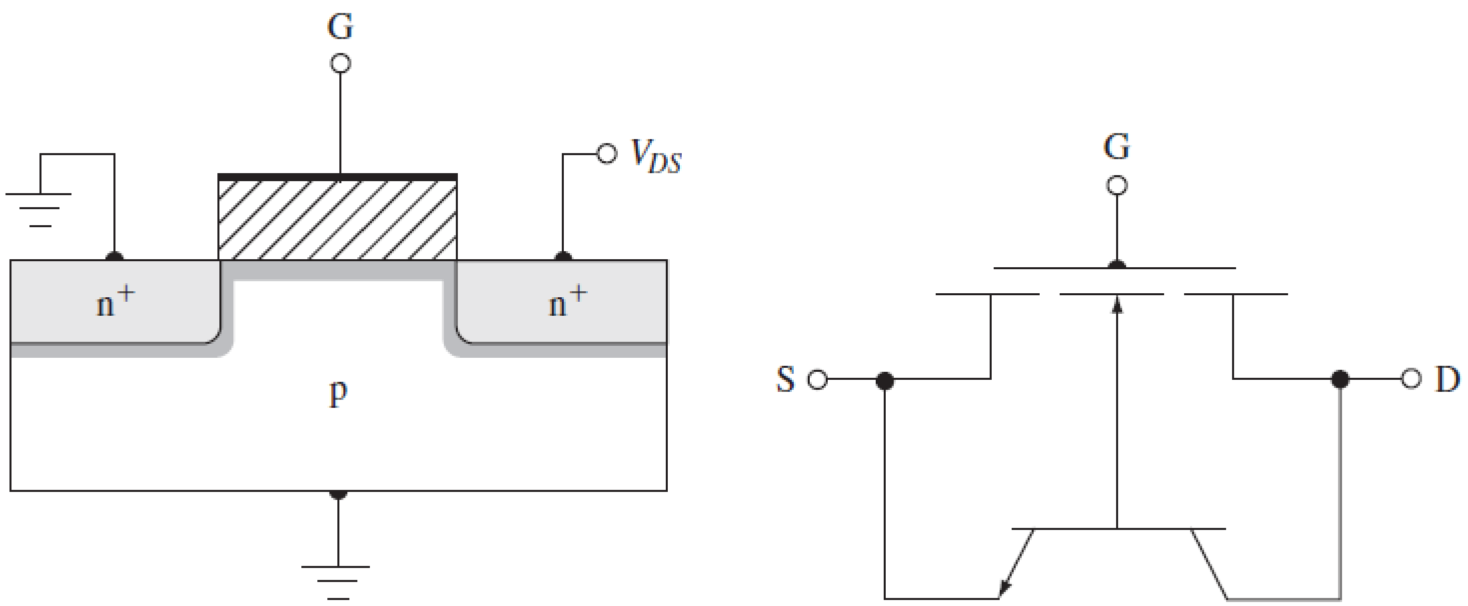


MOSFET: Breakdown

Breakdown mechanisms:

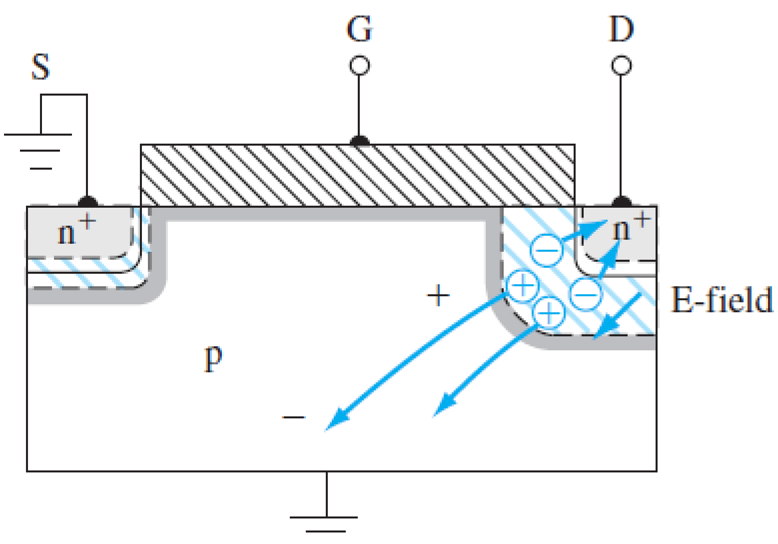
- Near avalanche and snapback breakdown
  - Second order effects
  - S-body-D form a parasitic BJT

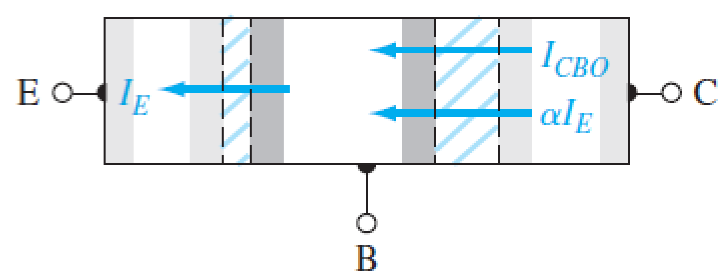


MOSFET: Breakdown

Breakdown mechanisms:

- Near avalanche and snapback breakdown
  - Second order effects
  - S-body-D form a parasitic BJT
  - The electrons generated by the avalanche process flow into the drain and contribute to the drain current
  - The avalanche-generated holes generally flow through the substrate to the body terminal
  - Voltage drop due to body resistance

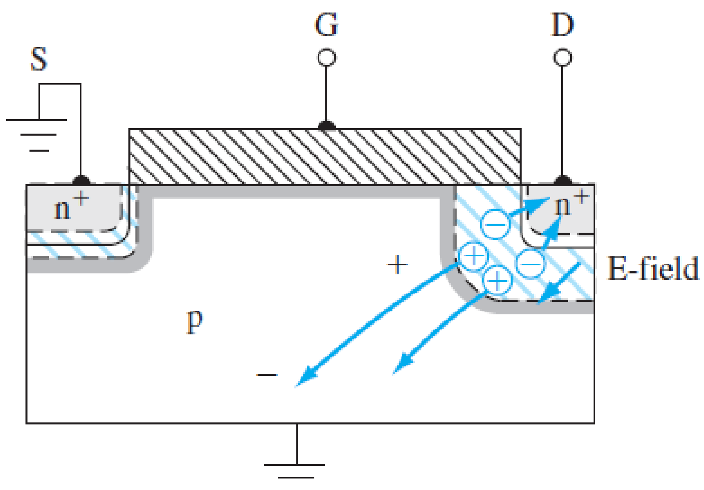


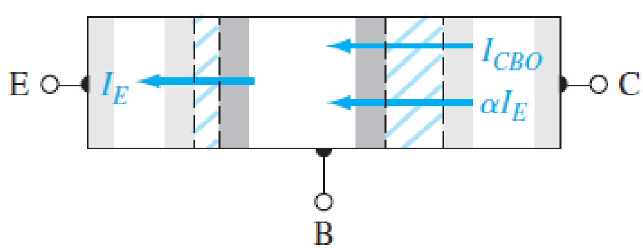


MOSFET: Breakdown

Breakdown mechanisms:

- Near avalanche and snapback breakdown
  - Source-to-substrate pn junction into forward bias near the source terminal
  - A large number of electrons can be injected from the source contact into the substrate under forward bias
  - A fraction of the injected electrons diffuses across the parasitic base region into the reverse-biased drain space charge region where they also add to the drain current
  - The rate of avalanche breakdown increases as the number of carriers in the drain space charge region increases

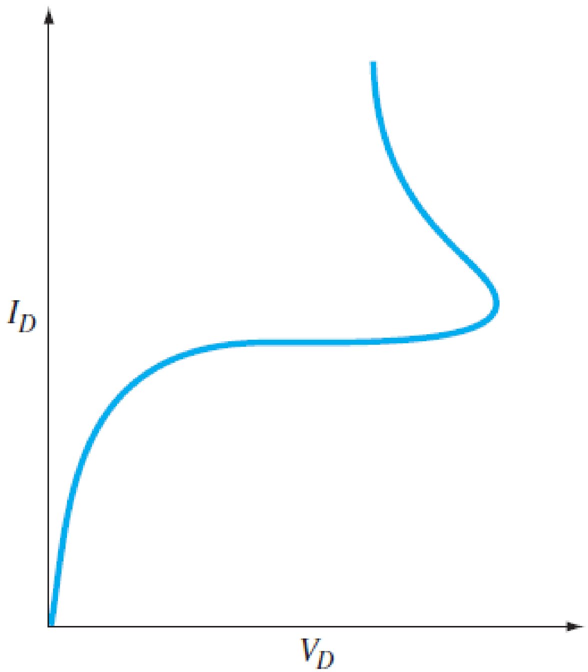




MOSFET: Breakdown

Breakdown mechanisms:

- Near avalanche and snapback breakdown
  - Positive feedback: Avalanche breakdown near the drain terminal produces the substrate current → forward-biased source-substrate pn junction voltage → injects carriers that can diffuse back to the drain and increase the avalanche process.
  - The positive feedback produces an unstable system
  - Snap back, negative resistance!
  - The potential of the base of the bipolar transistor near the emitter (source) is almost floating, since this voltage is determined primarily by the avalanche-generated substrate current rather than an externally applied voltage



MOSFET: Breakdown

Breakdown mechanisms:

- Near avalanche and snapback breakdown

Open-base bipolar transistor $I_C = \alpha I_E + I_{CB0}$

I_{CB0} is the base-collector leakage current

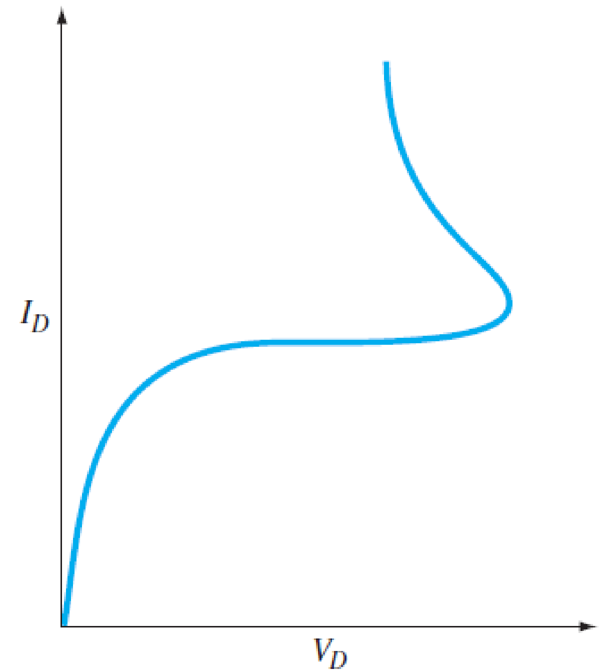
For an open base, $I_C = I_E$

$$I_C = \alpha I_C + I_{CB0}$$

At breakdown, $I_C = M(\alpha I_C + I_{CB0})$

$$I_C = \frac{M I_{CB0}}{1 - \alpha M}$$

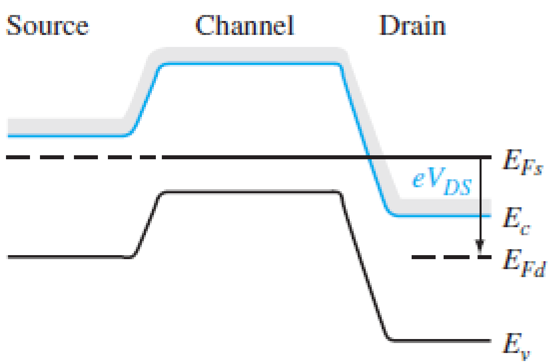
Breakdown condition: $\alpha M \rightarrow 1$

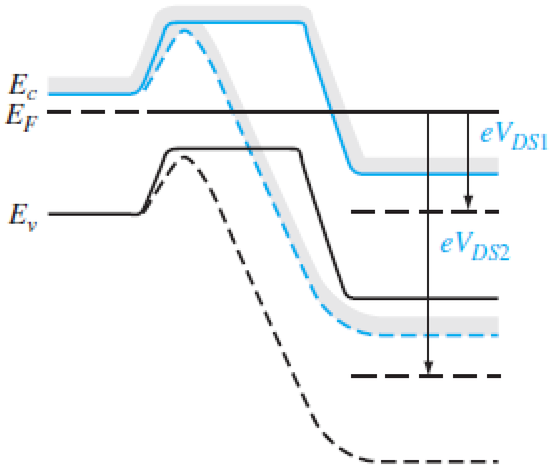


MOSFET: Breakdown

Breakdown mechanisms:

- Near punch-through effects
  - Punch-through is the condition at which the drain-to-substrate space charge region extends completely across the channel region to the source-to-substrate space charge region.
  - The barrier between the source and drain is completely eliminated and a very large drain current would exist
  - The drain current will begin to increase rapidly before the actual punch-through condition is reached: near punch-through condition, also known as Drain-Induced Barrier Lowering (DIBL).





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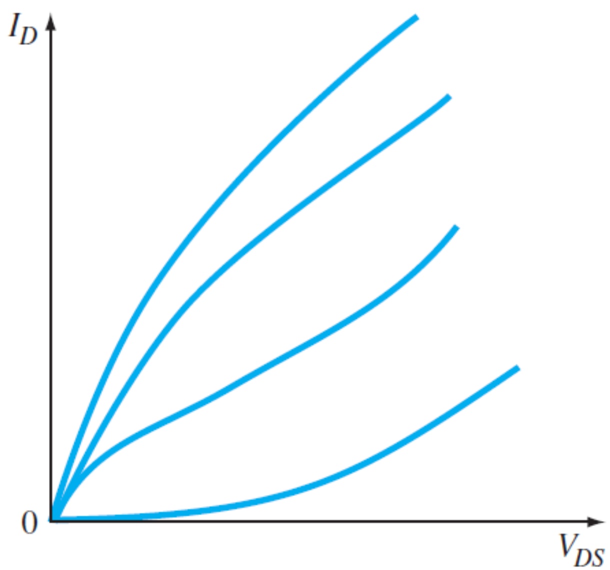
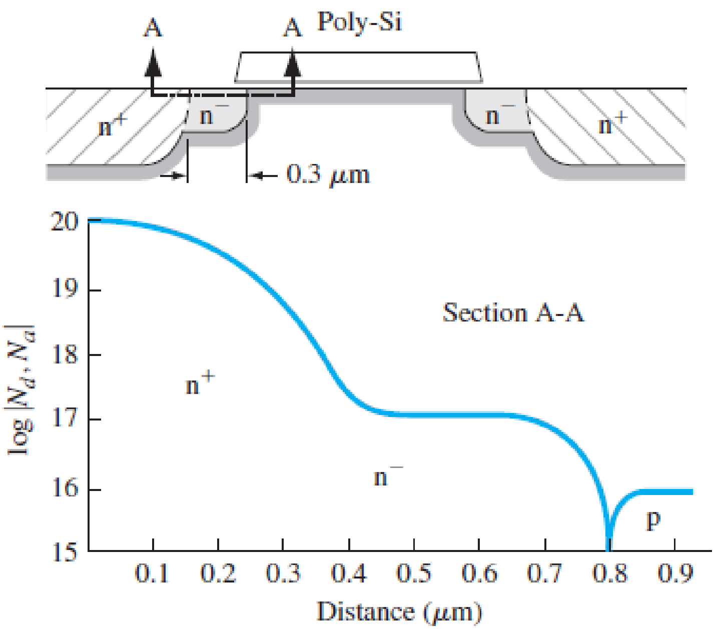
  - Short channel MOSFETs



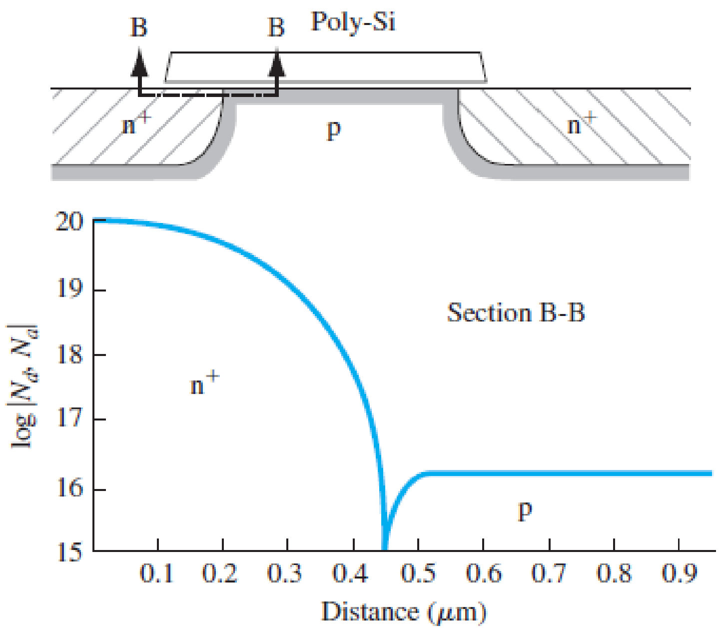
MOSFET: Lightly doped drain transistor

- Voltage does not scale together with the channel length, so electric field increases
- Near avalanche breakdown and near punch-through effects become more serious
- How to reduce the breakdown effect?
- Alter the doping profile at the drain: Lightly Doped Drain (LDD) design
- The peak electric field at the drain junction is a function of the semiconductor doping as well as the curvature of the n+ drain region

LDD



Conventional



MOSFET: Lightly doped drain (LDD) transistor

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- Alter the doping profile at the drain: Lightly Doped Drain (LDD) design
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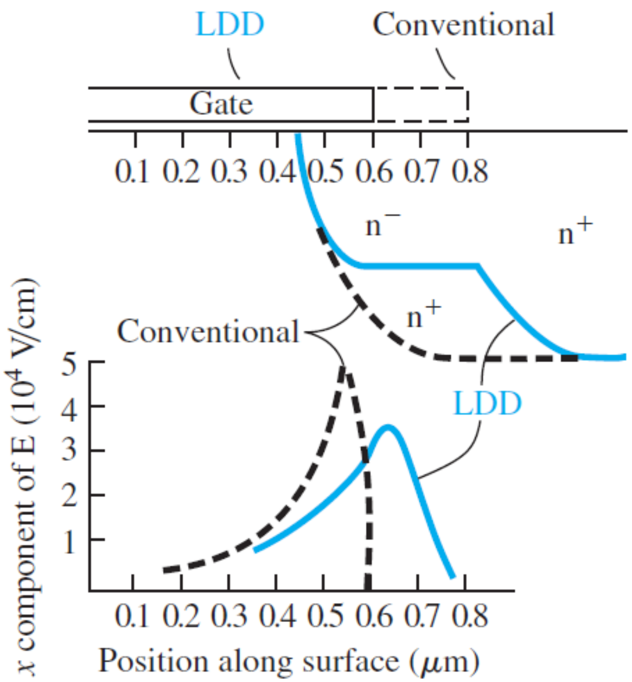
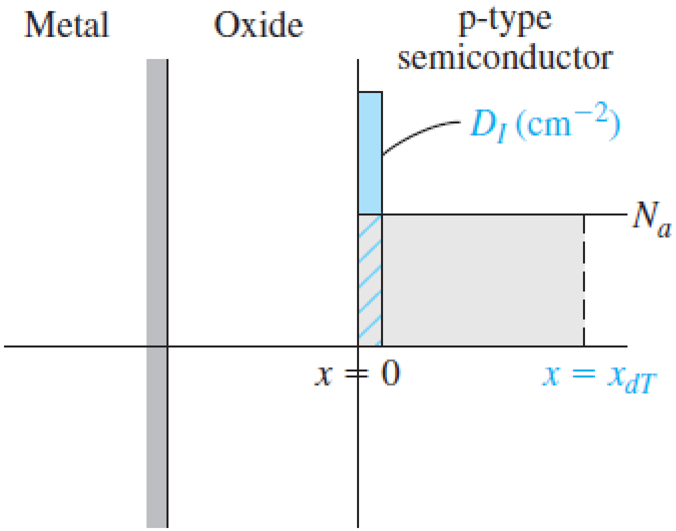
Disadvantages:

- Fabrication complexity
- Drain resistance



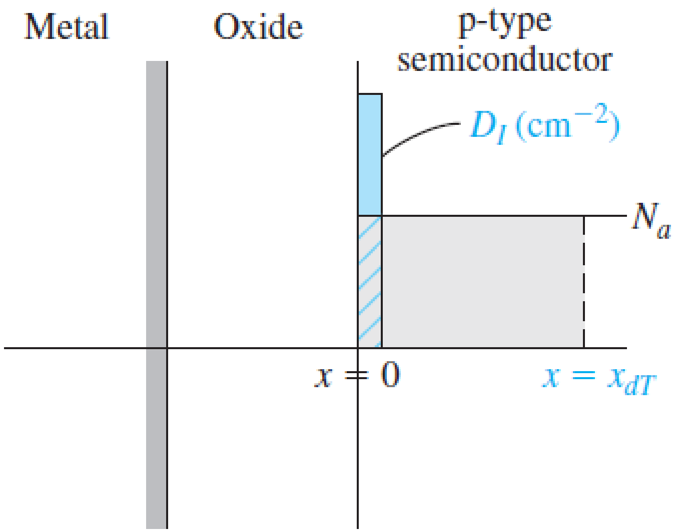
MOSFET: Threshold adjustment by ion implantation

- Threshold voltage: fixed oxide charge, metal–semiconductor work function difference, oxide thickness, and semiconductor doping
- Ion implantation can be used to change and adjust the substrate doping near the oxide–semiconductor surface to provide the desired threshold voltage
- An implant of acceptor ions into either a p- or n-type substrate will shift the threshold voltage to more positive values, while an implant of donor ions will shift the threshold voltage to more negative values.



MOSFET: Threshold adjustment by ion implantation

- Ion implantation can be carried out to change a depletion-mode device to enhancement-mode or an enhancement-mode device to depletion-mode.
- First type: Assume that D_I acceptor atoms per cm^2 are implanted into a p-type substrate directly adjacent to the oxide–semiconductor interface
- The shift in threshold voltage is $$\Delta V_T = +\frac{eD_I}{C_{ox}}$$
- If donor atoms were implanted into the p-type substrate, the space charge density would be reduced: threshold voltage would shift in the negative voltage direction.

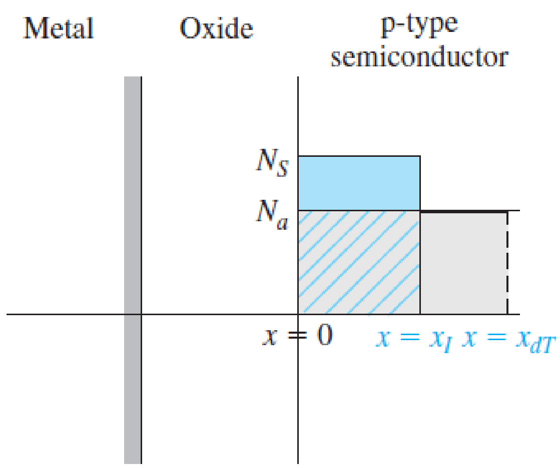


MOSFET: Threshold adjustment by ion implantation

- Second type: Step junction
- If the induced space charge width is greater than x_I at the threshold inversion point, then a new expression for x_{dT} must be derived
- Maximum induced space charge width

$$x_{dT} = \sqrt{\frac{2\epsilon_s}{eN_a}\left[2\phi_{fp} - \frac{ex_I^2}{2\epsilon_s}(N_s - N_a)\right]^{1/2}}$$

- Threshold voltage $V_T = V_{T0} + \frac{eD_I}{C_{ox}}$



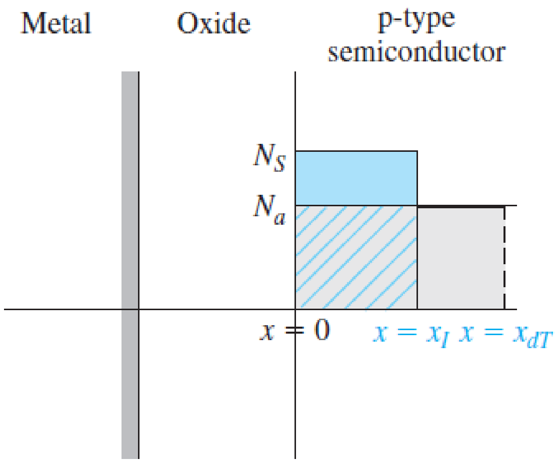
MOSFET: Threshold adjustment by ion implantation

- Second type: Step junction
- Threshold voltage

$$V_T = V_{T0} + \frac{eD_I}{C_{ox}}$$

$$D_I = (N_s - N_a)x_I$$

$$V_{T0} = V_{FB0} + 2\phi_{fp0} + \frac{eN_a x_{dT0}}{C_{ox}}$$

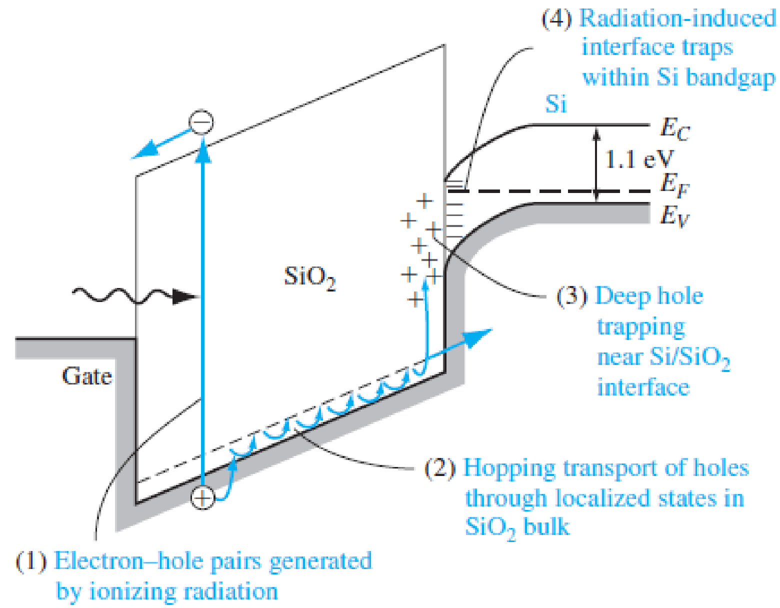


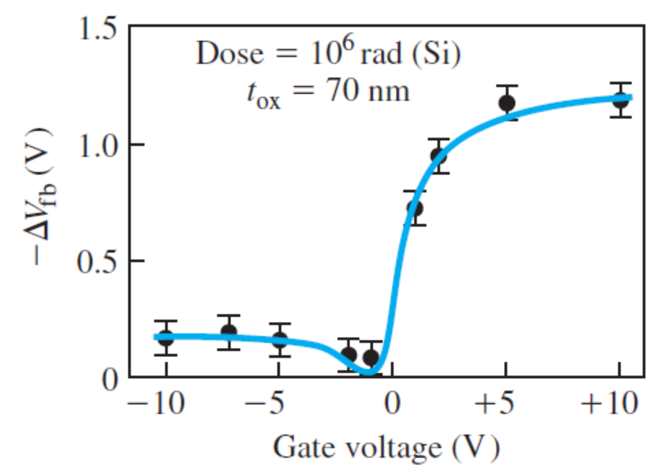
MOSFET: Threshold adjustment by ion implantation

- The actual implant dose versus distance is neither a delta function nor a step function
- It tends to be a Gaussian-type distribution
- The threshold shift due to a nonuniform ion implant density may be defined as the shift in curves of N_{inv} versus V_G
- This shift corresponds to an experimental shift of drain current versus V_G when the transistor is biased in the linear mode.
- The determination of the threshold voltage becomes more complicated

MOSFET: Radiation and hot electron

- Fixed trapped oxide charge and interface state charge
- Can also be generated after fabrication, by ionizing radiation and impact ionization in the drain region of a MOSFET operating near avalanche breakdown
- Ionizing radiation: high energy photon, cosmic ray
- Communication satellites

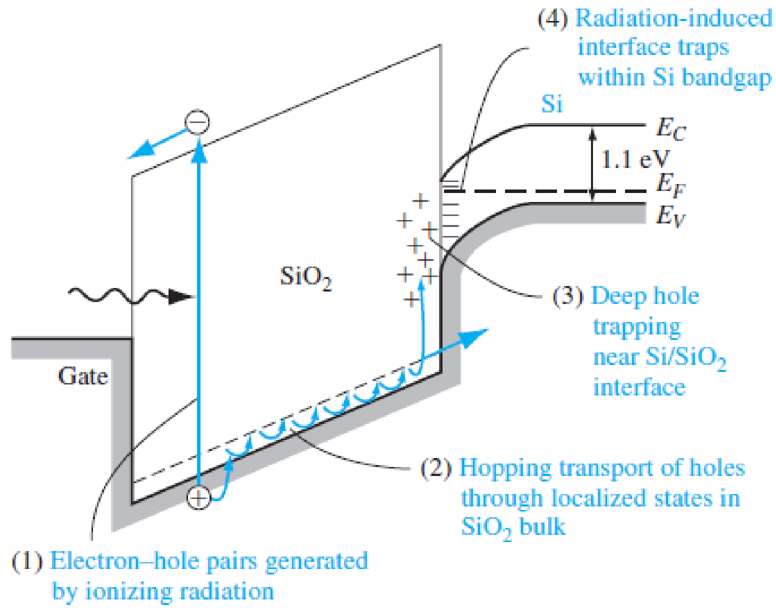


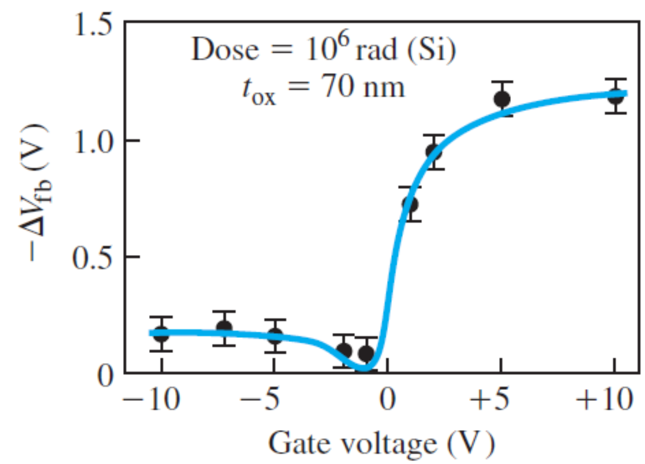


MOSFET: Radiation and hot electron

Oxide charge from radiation

- Gamma-rays or x-rays incident on semiconductor or oxide materials can interact with valence band electrons
- Generates electron–hole pairs
- Oxide bandgap is large (9eV for SiO_2): need high energy photons
- The force on the radiation-induced electron is toward the gate and the force on the radiation-induced hole is toward the semiconductor
- Generated electrons in the oxide are fairly mobile with a mobility value on the order of 20 cm^2/V-s.
- Electron: 10^7 cm/s at high field, and transit time is ~ps
- Electrons dissipate through the gate

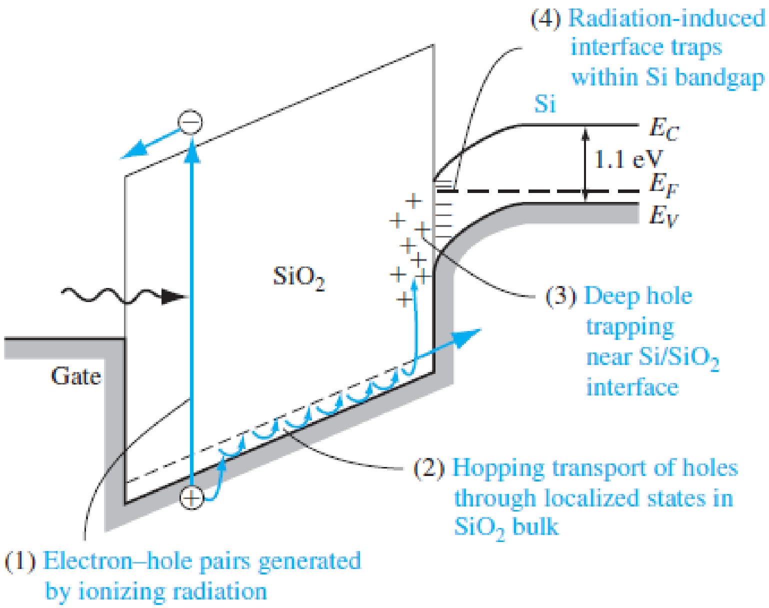


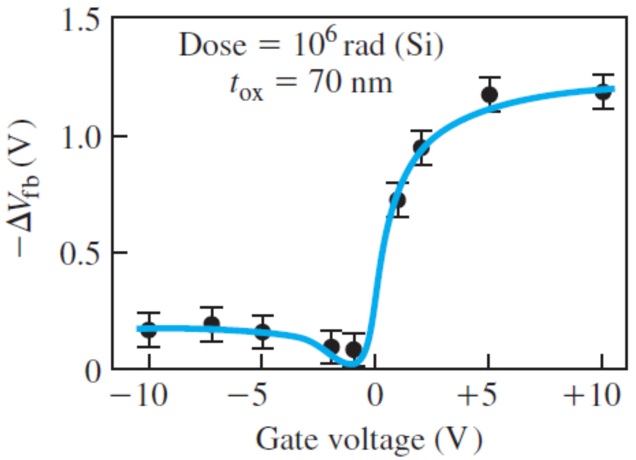


MOSFET: Radiation and hot electron

Oxide charge

- Holes: stochastic hopping transport process through the oxide
- The effective hole mobility in silicon dioxide is typically in the range of 10^{-4} to 10^{-11} $cm^2/V\text{-}s$
- Holes are relatively immobile
- When holes reach the silicon–silicon dioxide (Si–SiO_2) interface, a fraction are captured in trapping sites while the remainder flow into the silicon
- A net positive radiation-induced charge is then trapped in the oxide
- This trapped charge can last from hours to years.
- Positive oxide charge causes a negative shift in threshold voltage

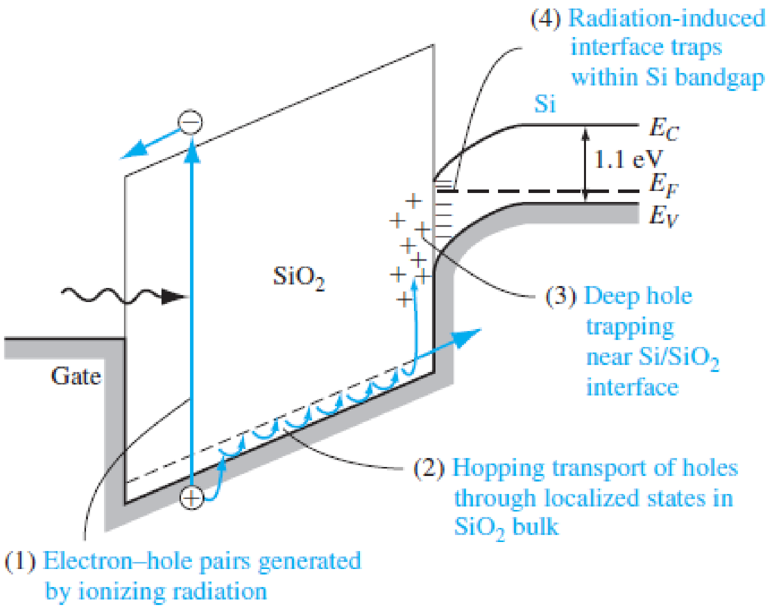


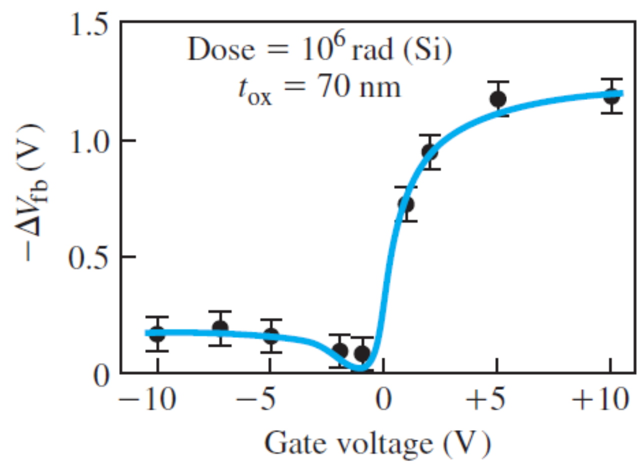


MOSFET: Radiation and hot electron

Oxide charge

- Hole trap densities are in the range of 10^{12} to 10^{13} cm^{-2}
- The hole trap is usually associated with a trivalent silicon defect that has an oxygen vacancy in the SiO_2 structure
- A function of gate voltage applied during irradiation
- Small values of gate voltage: some radiation-generated holes and electrons recombine in the oxide
- For negative applied gate voltages, the radiation-induced holes move toward the gate terminal. There can be positive charge trapping in the oxide near the gate, but the effect of this trapped charge on the threshold voltage is small

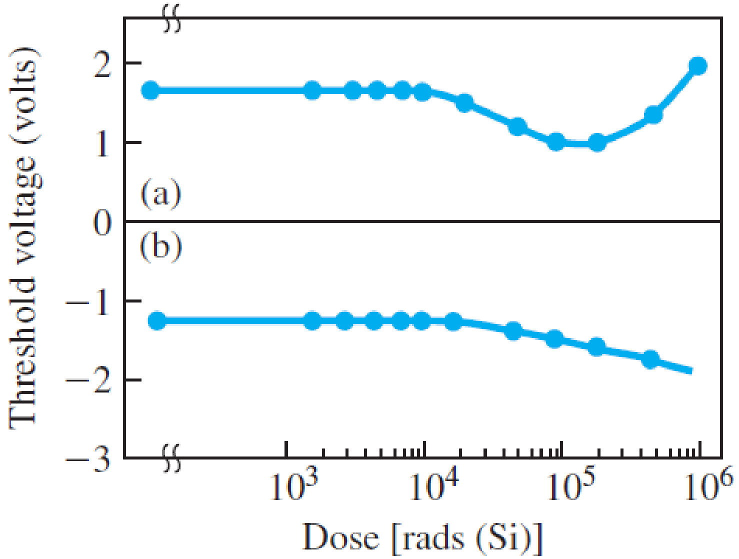


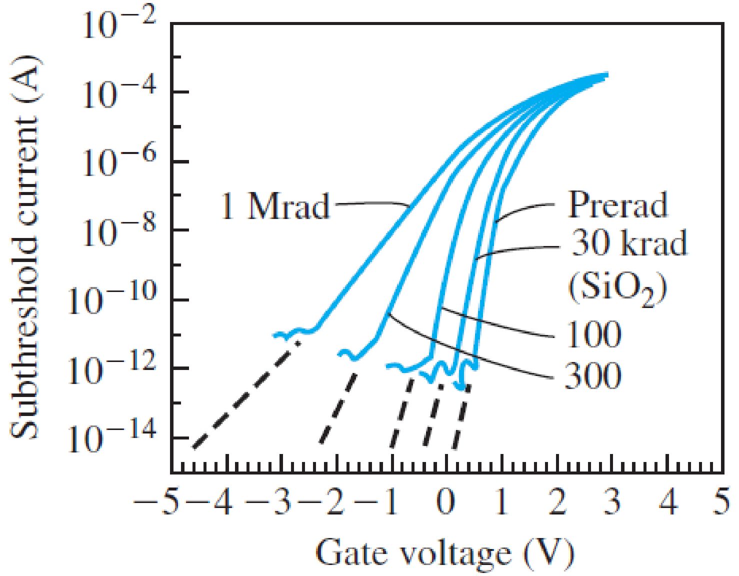


MOSFET: Radiation and hot electron

Interface states from radiation

- The net charge in the interface states of an n-channel MOS device at the threshold inversion point is negative: causes a shift in threshold voltage in the positive voltage direction
- Coulomb interaction with the inversion charge carrier, which means that the inversion carrier mobility is a function of the interface state density through surface-scattering effects

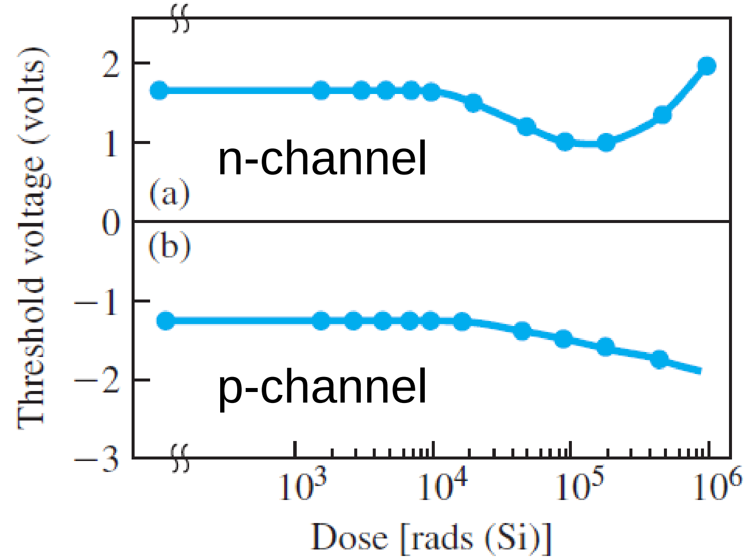


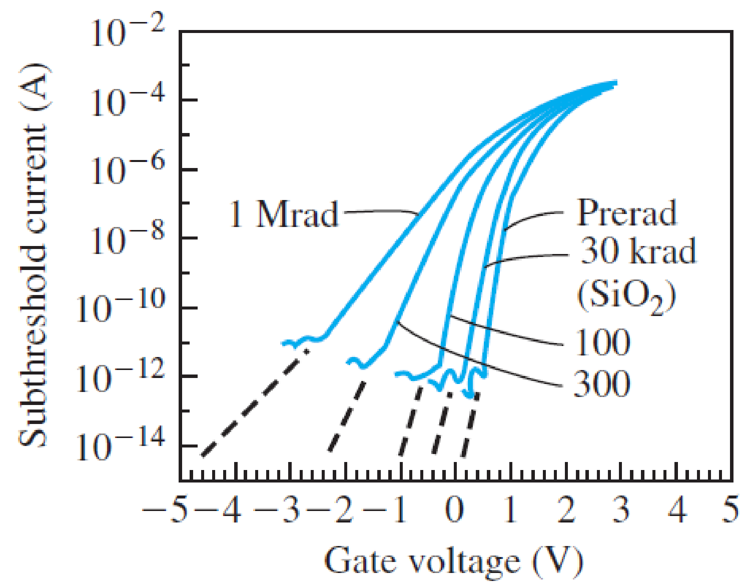


MOSFET: Radiation and hot electron

Interface states from radiation

- Ionizing radiation, additional interface states are generated at the Si–SiO_2 interface
- The radiation-induced interface states tend to be donor states in the lower half of the bandgap and acceptor states in the upper half.
- We initially see the negative threshold voltage shift in both devices due to the radiation-induced positive oxide charge.
- Then threshold shift at the higher dose levels is attributable to the creation of radiation-induced interface states that tend to compensate the radiation-induced positive oxide charge.
- Slope of the ln I_D versus V_{GS} curves in the subthreshold region is a function of the density of interface states.

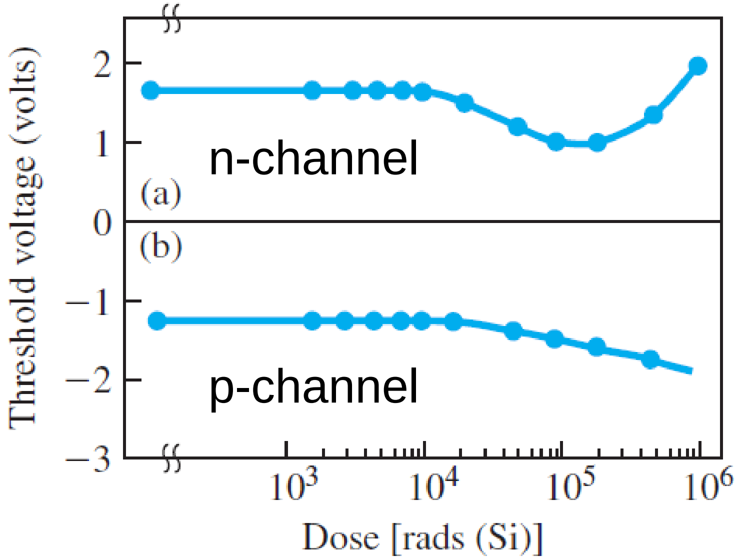


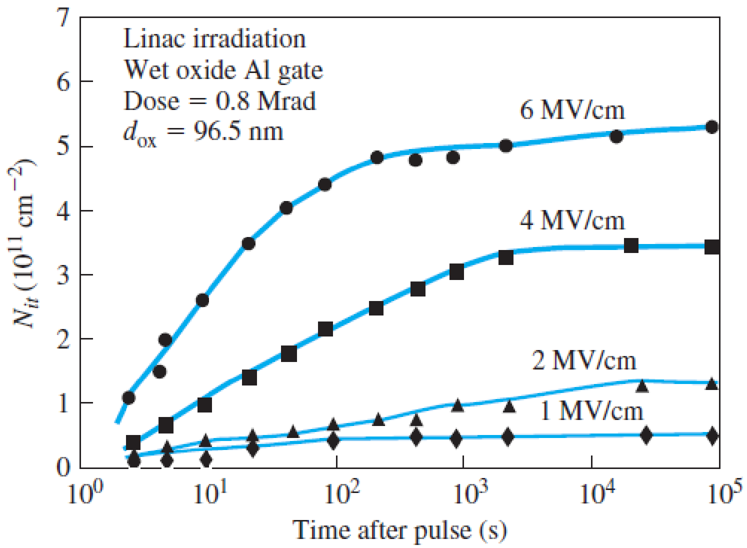


MOSFET: Radiation and hot electron

Interface states from radiation

- The final interface state density is reached between 100 to 10,000 seconds after a pulse of ionizing radiation.
- Radiation-induced interface states can cause shifts in threshold voltage, affecting circuit performance
- A reduction in mobility can affect the speed and output drive capability of a circuit

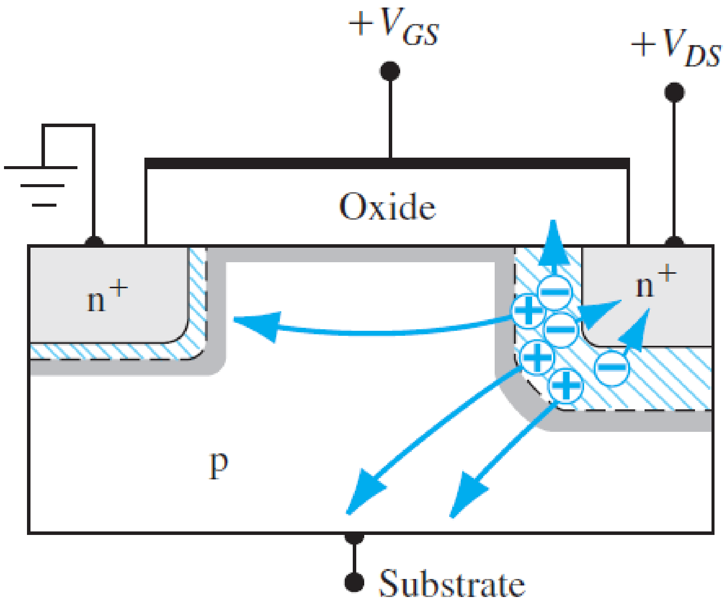




MOSFET: Radiation and hot electron

Hot electron

- Large field: impact ionization in the drain space charge region
- The generated electrons tend to be swept to the drain and generated holes swept into the substrate in an n-channel MOSFET
- Some of the electrons generated in the space charge region are attracted to the oxide due to the electric field induced by a positive gate voltage
- "Hot" electrons?
- High energy electrons
- Have energies far greater than the thermal-equilibrium value
- If the electrons have energies on the order of 1.5 eV, they may be able to tunnel into the oxide
- May be able to overcome the silicon oxide potential barrier and produce a gate current (fA, 10^{-15}A or pA, 10^{-12}A)



MOSFET: Radiation and hot electron

Hot electron

- Electrons traveling through the oxide may be trapped, producing a net negative charge density in the oxide
- Local positive shift in the threshold voltage

- The energetic electrons, as they cross the Si–SiO_2 interface, can generate additional interface states.
- Breaking up of silicon-hydrogen bonds
- Continuous processes, device degrades over a period of time.
- Limit the useful life of the device
- LDD structure can reduce the hot electron effect by reducing the maximum electric field