VE 320 Fall 2021

Introduction to Semiconductor Devices

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Lecture 16

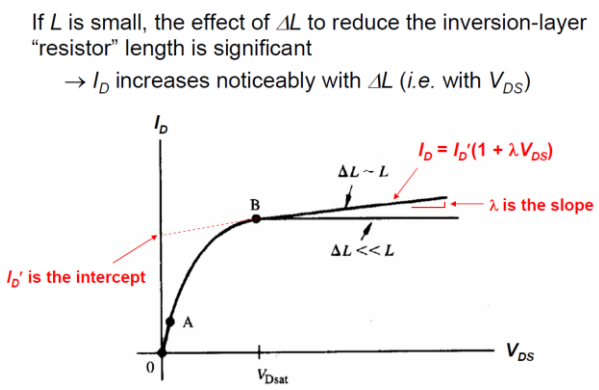
Modern MOSFET (Optional)

(Ref: Chenming Hu, “Modern Semiconductor Devices for Integrated Circuits”)

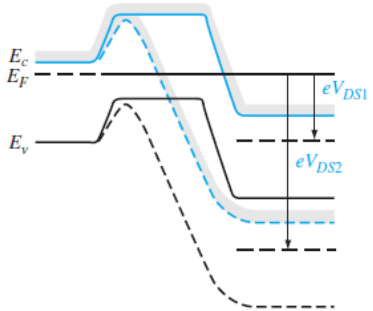
MOSFET: short channel effects summary

Short channel, if velocity saturation is not considered

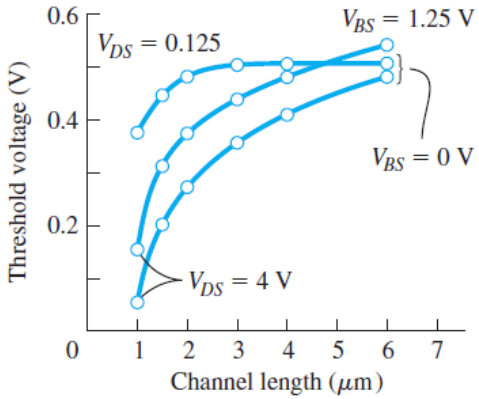
- Short channel: I_D not saturate

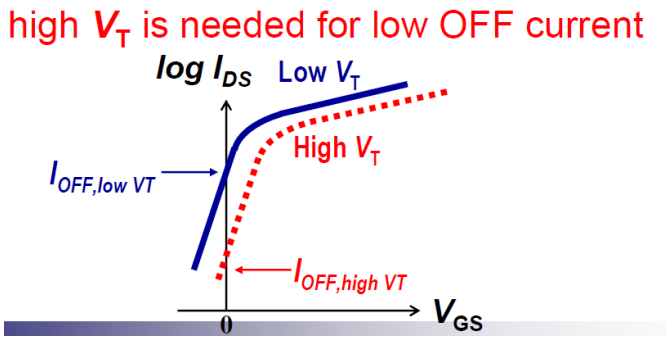


- Easier to have breakdown and DIBL



- V_T roll-off: short channel MOSFETs have more leakage

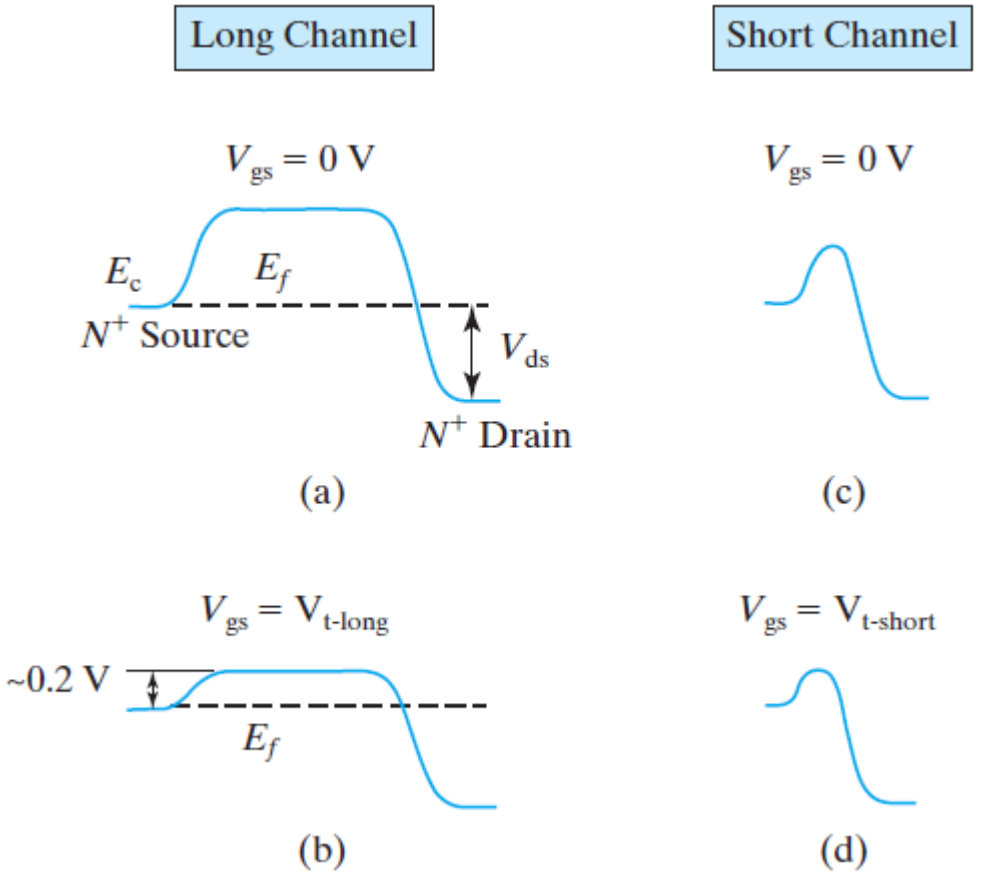




MOSFET: short channel effects summary

V_{GS} and V_{DS} "compete" for controlling the channel

- Short channel: DIBL



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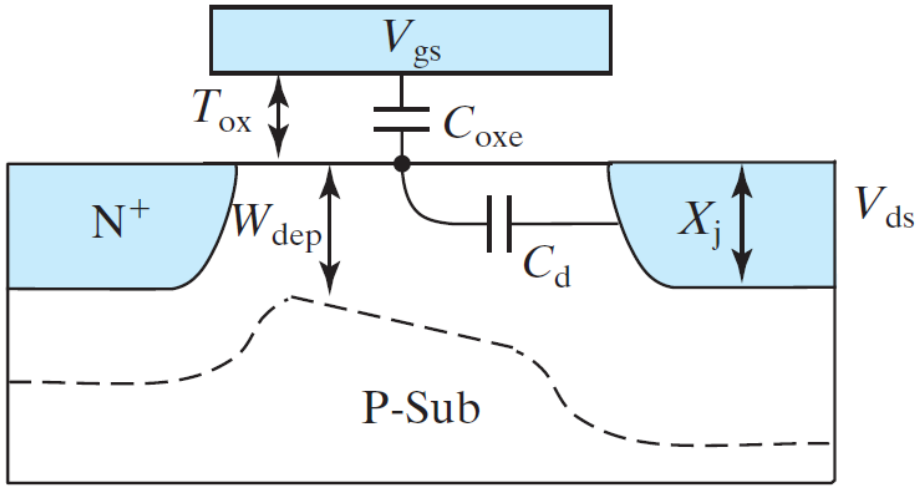

$$V_t = V_{t\text{-long}} - V_{ds} \cdot \frac{C_d}{C_{oxe}}$$

$$V_t = V_{t\text{-long}} - (V_{ds} + 0.4\,\text{V}) \cdot e^{-L/l_d}$$

$$l_d \propto \sqrt[3]{T_{oxe} W_{dep} X_j}$$

MOSFET: short channel effects summary

V_{GS} and V_{DS} "compete" for controlling the channel

- We want to maximize the gate-to-channel capacitance and minimize the drain-to-channel capacitance.
- Maximize the gate-to-channel capacitance: small T_{ox}
- Minimize the drain-to-channel capacitance: reduce W_{dep} and X_j (drain junction depth)

But… It is hard to make these dimensions smaller and smaller

- Gate can only have a good control at the surface of Si, even when T_{ox} is small
- The drain could still have more control than the gate along other leakage current paths that are some distance below the Si surface

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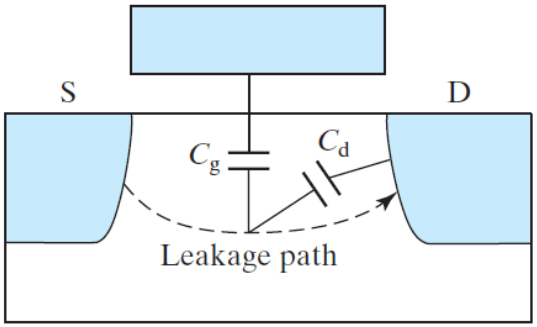
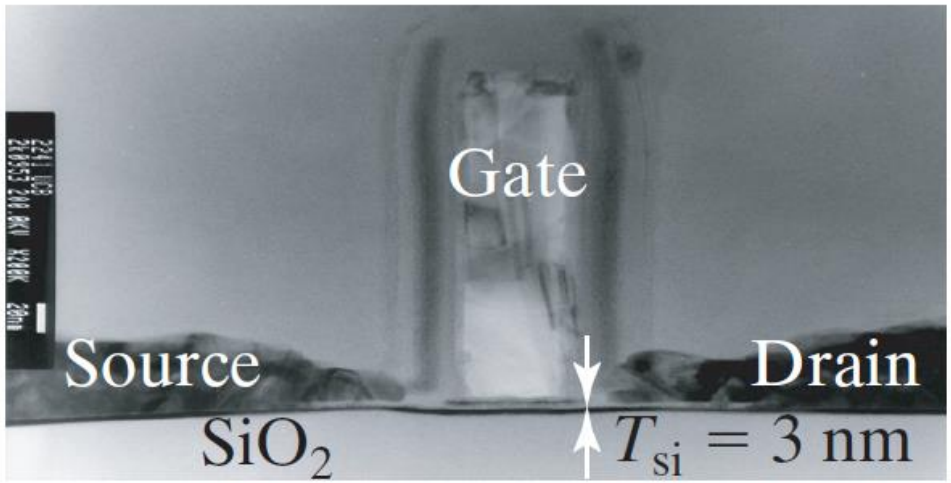


- The gate is far away and the gate control is weak
- The drain voltage can pull the potential barrier down and allow leakage current to flow along this submerged path
- How to solve the problem?

Solution 1: Ultra-Thin-Body (UTB) MOSFET and SOI

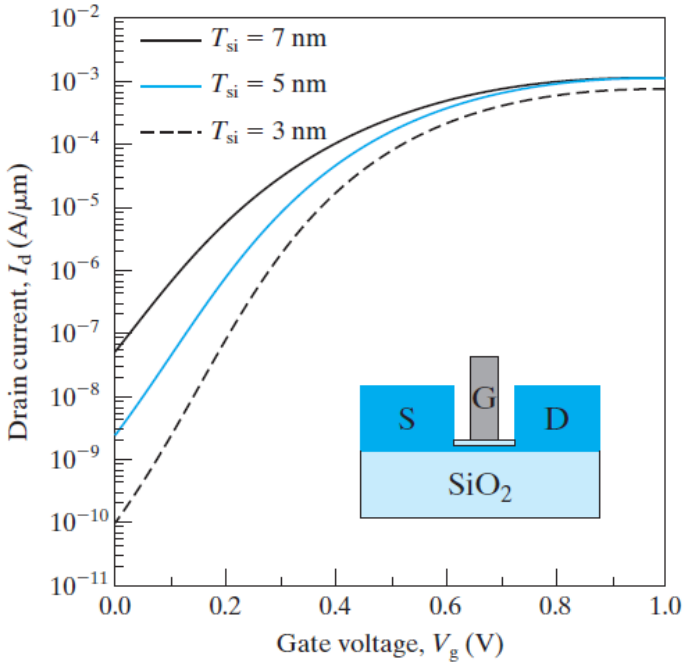
- SOI: silicon on insulator (SiO_2)
- Si film is very thin < 10 nm, no leakage path is very far from the gate
- Therefore, the gate can effectively suppress the leakage.



- L_g can be scaled roughly in proportion to T_{Si}
- Si thickness T_{Si} should be thinner than about one half of the gate length in order to reap the benefit of the UTB MOSFET concept to sustain scaling

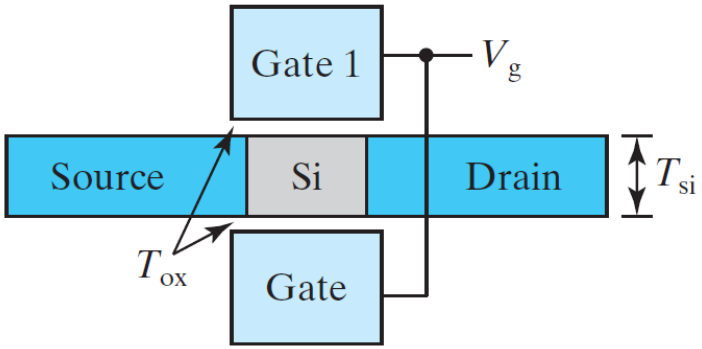
Solution 1: Ultra-Thin-Body (UTB) MOSFET and SOI

- SOI: silicon on insulator (SiO_2)
- Because small l_d can be obtained without heavy channel doping, carrier mobility is improved
- One challenge posed by UTB MOSFETs is the large source/drain resistance due to their thinness. The solution is to thicken the source and drain with epitaxial deposition.



Solution 2: FinFET (Multigate MOSFET)

- Provide gate control from more than one side of the channel

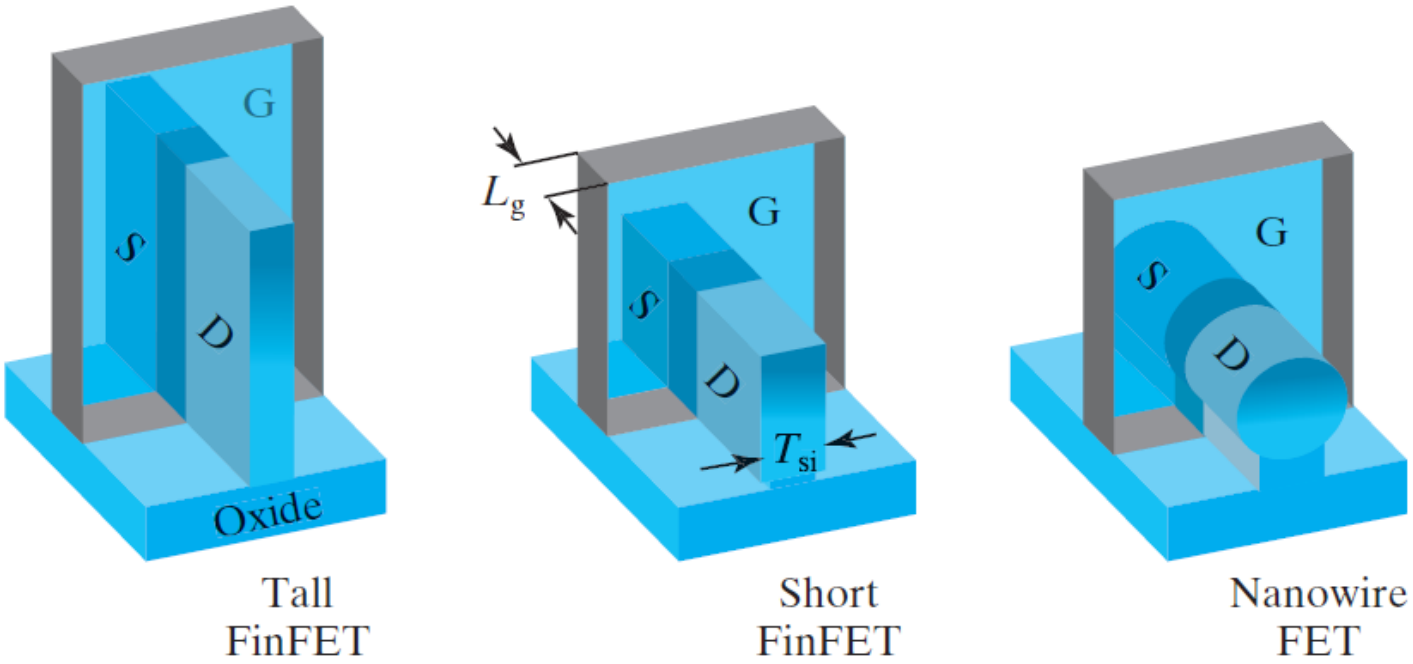


Double-gate MOSFET

- The Si film is very thin so that no leakage path is far from the gates
- Therefore, the gate(s) can suppress leakage current more effectively than the conventional MOSFET
- How to fabricate multigate MOSFET?

Solution 2: FinFET (Multigate MOSFET)

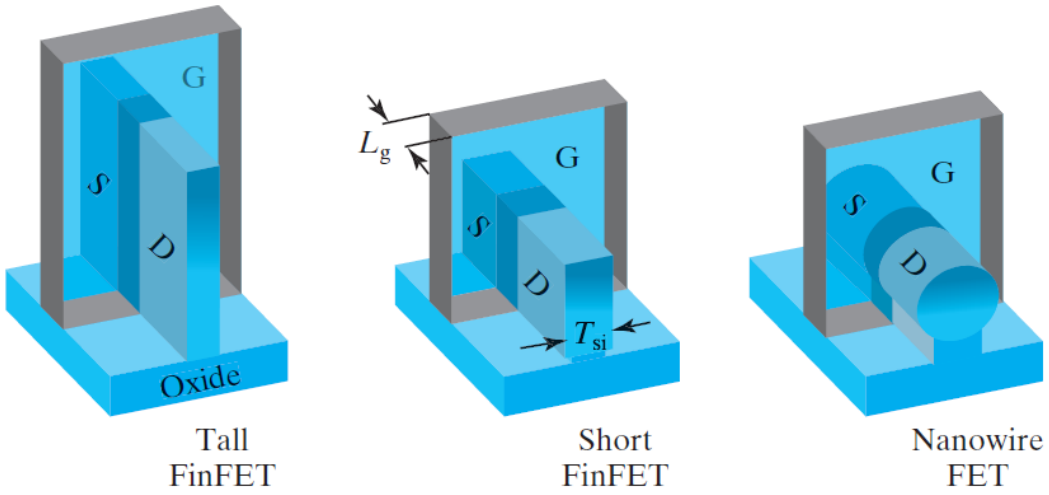
- Provide gate control from more than one side of the channel
- FinFET: like back fin of a fish



Tall FinFET | Short FinFET | Nanowire FET

Solution 2: FinFET (Multigate MOSFET)

- FinFET

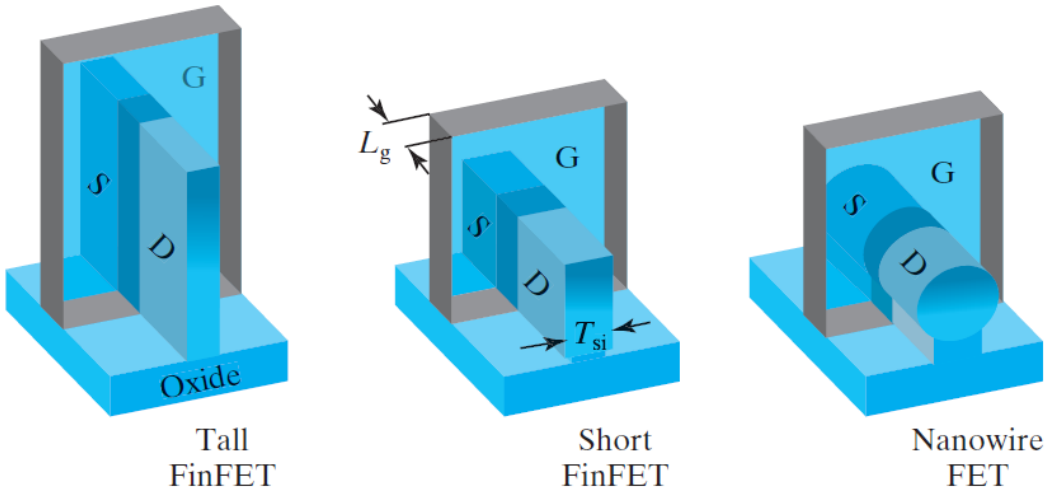


Tall FinFET | Short FinFET | Nanowire FET

- The process starts with an SOI wafer or a bulk Si wafer. A thin fin of Si is created by lithography and etching.
- Gate oxide is grown over the exposed surfaces of the fin.
- Poly-Si gate material is deposited over the fin and the gate is patterned by lithography and etching.
- Finally, source/drain implantation is performed.

Solution 2: FinFET (Multigate MOSFET)

- FinFET

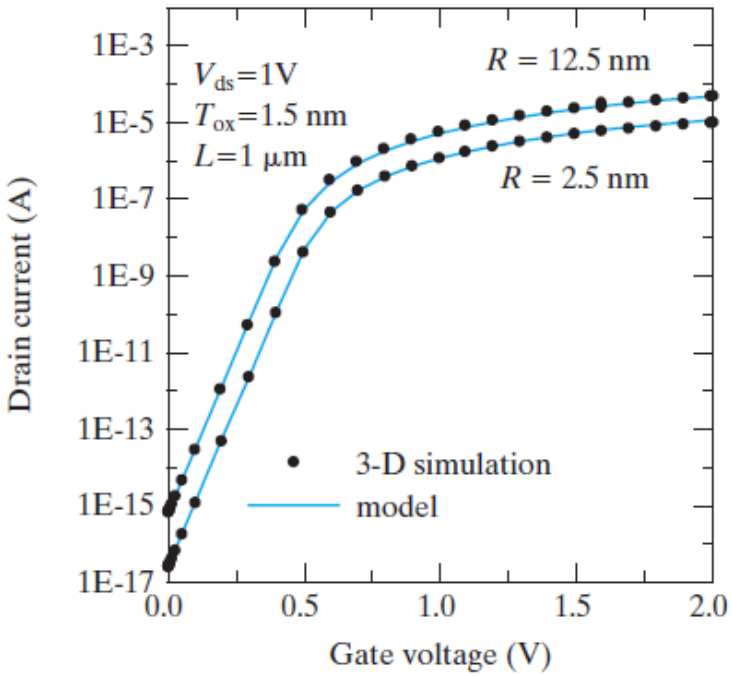


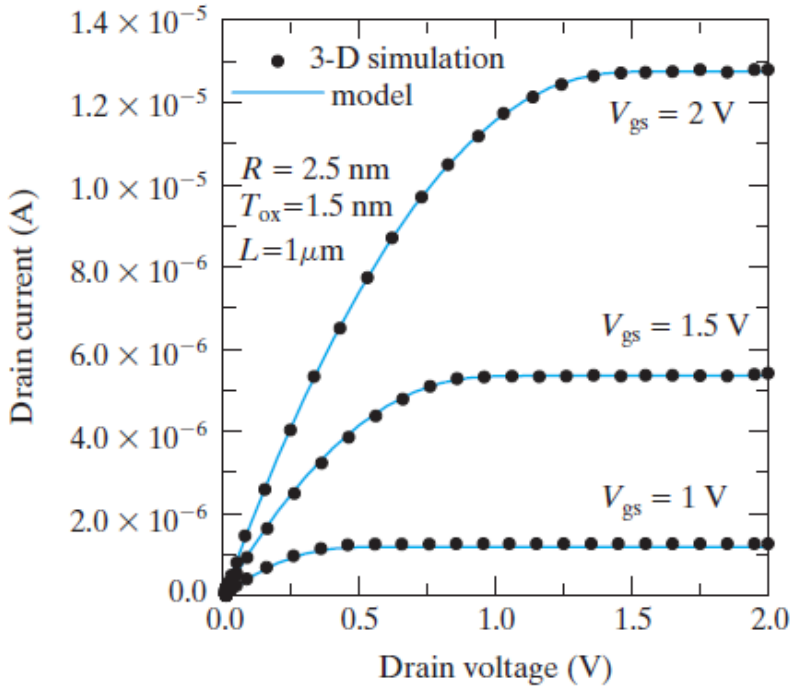
Tall FinFET | Short FinFET | Nanowire FET

- A tall FinFET has the advantage of providing a large W and therefore large Ion while occupying a small footprint.
- A short FinFET has the advantage of less challenging etching. In this case, the top surface of the fin contributes significantly to the suppression of V_t roll-off and to leakage control. This structure is also known as a triple-gate MOSFET.
- The third variation gives the gate even more control over the Si wire by surrounding it.

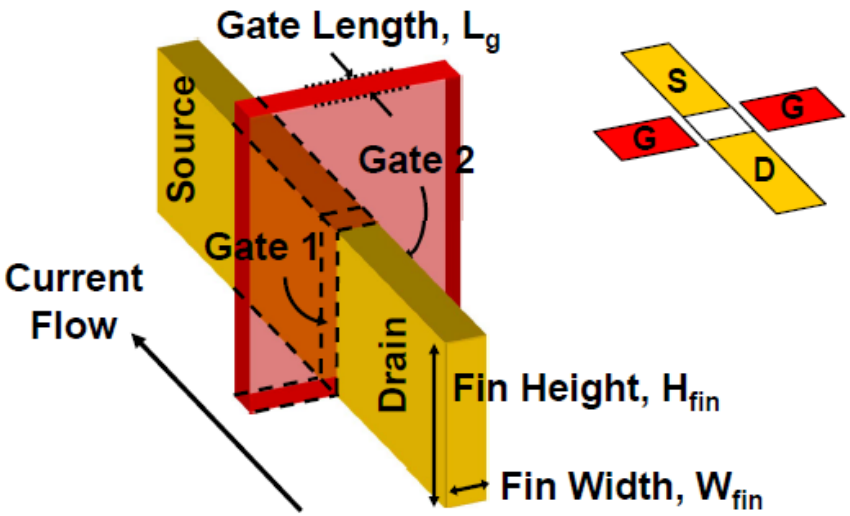
Solution 2: FinFET (Multigate MOSFET)

- FinFET with L_g as small as 3 nm have been experimentally demonstrated
- Scale beyond the limit of conventional planar transistor



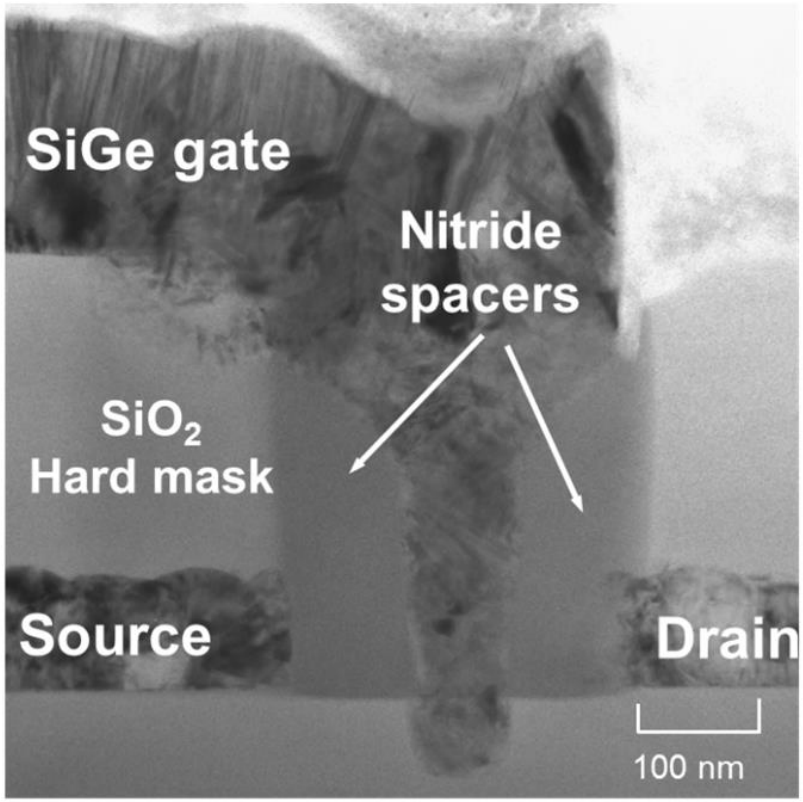


Solution 2: FinFET (Multigate MOSFET)

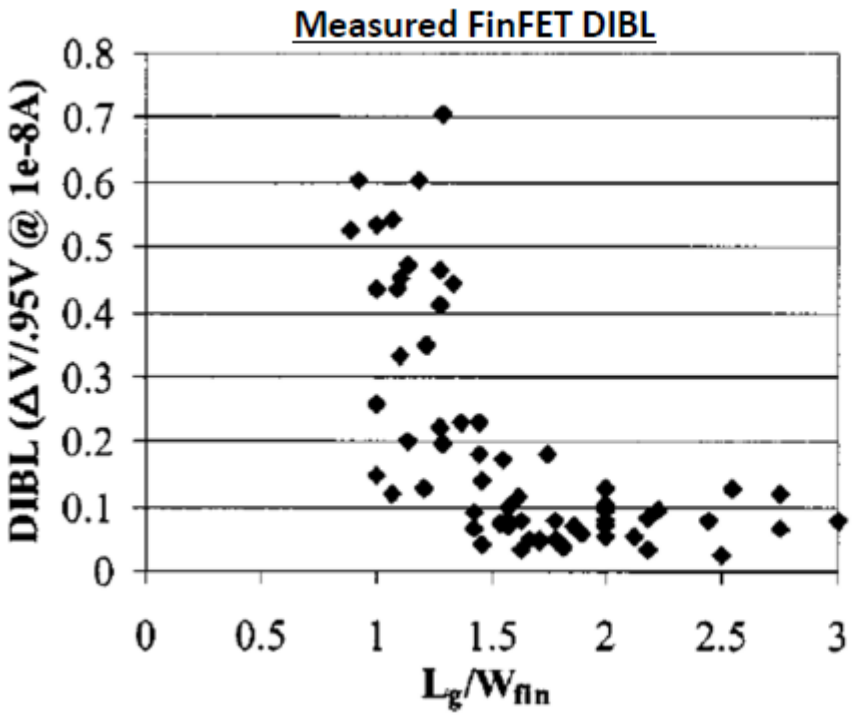


1998: First N-channel FinFETs

1999: First P-channel FinFETs



Solution 2: FinFET (Multigate MOSFET)

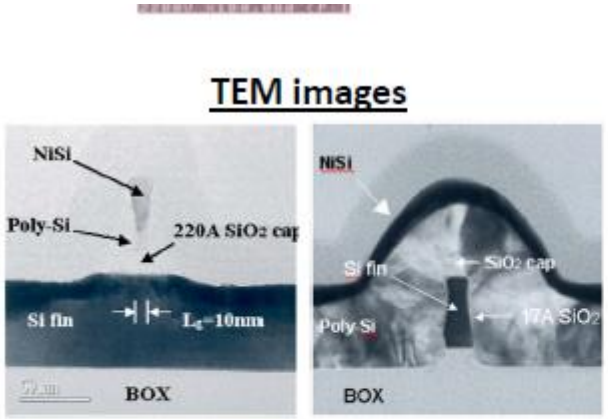


- To adequately suppress DIBL, $L_g/W_{fin} > 1.5$

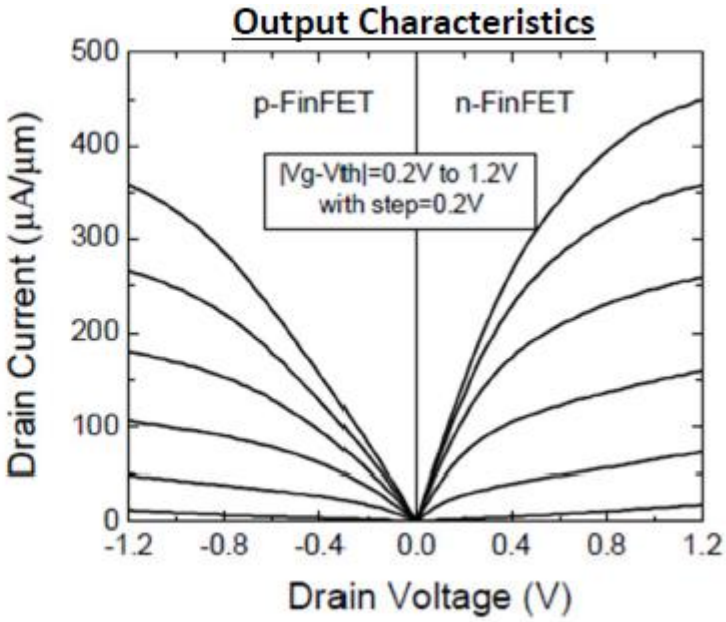
→ Challenge for lithography!

Solution 2: FinFET (Multigate MOSFET)

2002: 10 nm FinFETs

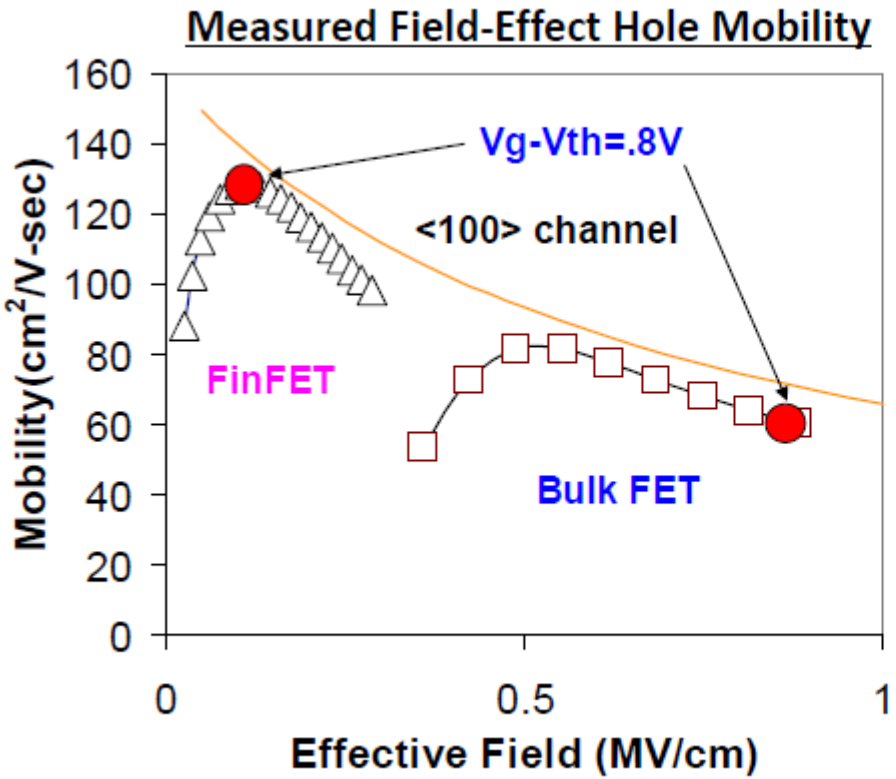


- These devices were fabricated at AMD, using optical lithography.



Solution 2: FinFET (Multigate MOSFET)

Mobility



- **DG FET has higher hole mobility due to lower transverse electric field**
- **For the same gate overdrive, hole mobility in DG-FinFET is 2× that in a control bulk FET**

Solution 2: FinFET (Multigate MOSFET)

Bulk FinFET

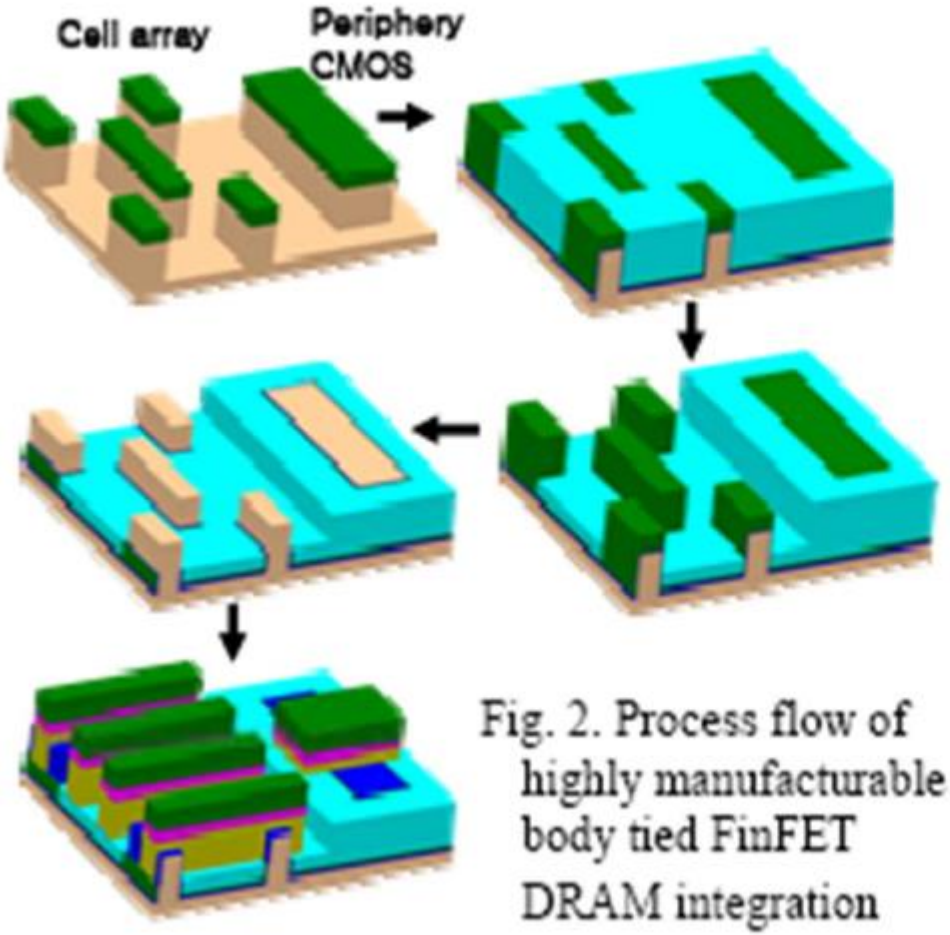


Fig. 2. Process flow of highly manufacturable body tied FinFET DRAM integration

- FinFETs can be made on bulk-Si wafers
  - ✓ lower cost
  - ✓ improved thermal conduction

  with super-steep retrograde well (SSRW) or "punch-through stopper" at the base of the fins
- 90 nm L_g FinFETs demonstrated
  - W_{fin} = 80 nm
  - H_{fin} = 100 nm

  DIBL = 25 mV

Solution 2: FinFET (Multigate MOSFET)

Bulk FinFET vs. SOI FinFET

Item	Comment	Bulk FINFET (compared to SOI FinFET)
Density	Well Contact	-
Parasitic Cap	Impact of PTS	-
Performance/ Variability	Performance tradeoff to overcome variability	- -
Leakage & HVT capability	Impact of PTS implant in bulk FIN	-
Non FIN structure compatibility (passives, etc)		+
s/d stressor	eSiGe, eSiC	++
Gate stressor, liner stressor		**Similar**
Channel stressor	SiGe pFET; SSOI Si nFET, III-V nFET	+/-
SRAM Vt Variation		- -