XXXXX XXXX

(86) 186-0000-000 • xxxxxxxxx@sjtu.edu.cn

EDUCATION

Shanghai Jiao Tong University (SJTU)

University of Michigan - Shanghai Jiao Tong University Joint Institute (UM-SJTU JI)

B.S.E. in Electrical and Computer Engineering — Sept 2014 – Aug 2018 (expected)

Overall GPA: 3.65/4.00 Rank: 11/96 Junior Year GPA: 3.83/4.00

PUBLICATIONS

[1] XXX, XXX, XXX, and XXX, **2016**, *High-availability Deployment for Large Enterprises,* **IEEE** International Conference on Progress in Informatics and Computing (PIC), pp. 503-507.

[2] XXX, XXX, XXX, and XXX,, **2016**, *Mass Data Storage Platform for Smart Grid*, **IEEE** International Conference on Progress in Informatics and Computing (PIC), pp. 530-535.

RESEARCH EXPERIENCE

Optical Imaging Laboratory, UM-SJTU JI

Research Assistant — May 2017 – Aug 2017

- Built the 2nd-generation (G2) optical-resolution photo-acoustic microscopy system for biomedical imaging
- Modified the GRIN Lens Probe system with hydrophone, ring shape transducer and FP sensor
- Tested the system using ink and conducted vivo experiment using mice as samples

Visual Media and Data Management Laboratory, SJTU

Research Assistant — Sept 2016 – Mar 2017

- Researched the reliability and high-availability of information system of China Southern Power Grid
- Modeled the information system using Markov Chain Algorithm
- Evaluated the reliability and assessed the static availability

INTERNSHIP EXPERIENCE

Intel Asia-Pacific Research & Development Ltd, Shanghai

Signal Integrity Engineer — Dec 2016 – Jun 2017

- Built the high-speed signal (25Gbps) testing system with Altera Arria10 GT Board, TI re-timer and TI re-driver
- Accomplished pre-emphasis and equalization with Quartus II and TI Sigcon to optimize the signal at the receiver

SELECTED COURSE PROJECTS

16-bit Adder & 8-bit multiplier Modeling

Course: *Digital Integrated Circuits,* **Teaching Assistant** — Sept 2017 – Present

- Instruct over 70 students to optimize logic gates using static CMOS, transmission gate
- Guide students to model SPG look-ahead adders in Cadence in lab experiments and grade coursework

Simulation and Implementation of 32-bit MIPS CPU

Course: *Introduction to Computer Organization,* **Team Leader** — Sept 2016 – Dec 2016

- Modeled both single-cycle and 5-stage pipelined MIPS Architecture CPU in Verilog HDL to process data
- Synthesized the design with Xilinx and implemented the pipelined CPU on FPGA board free of error

Computer Aided Chem Lab Assistant

Course: *Introduction to Engineering,* **Team Member** — May 2015 – Aug 2015

- Designed and manufactured a modeling equipment for automatically doing liquid experiments in Chem Lab
- Won the "**Top Overall Award**" in JI Design Expo among 18 teams

AWARDS

- Honorable Mention in Mathematical Contest in Modeling — Feb 2016
- National Encouragement Scholarship **(2 in UM-SJTU JI)** — Sept 2017
- Yu Liming Scholarship of UM-SJTU JI **(14 in UM-SJTU JI)** — Nov 2016, Oct 2015, Nov 2014
- Outstanding Student Scholarship (Grade 3) of SJTU **(Top 15%)** — Dec 2016, Dec 2015
- Dean's List of UM-SJTU JI (Semester GPA > 3.5) — Oct 2016, Feb 2016, Sept 2015

COMPUTER SKILLS

- **Programming:** C/C++, MATLAB, Verilog, MIPS Assembly
- **Software:** Cadence, Xilinx, Quartus II, Mathematica

LANGUAGE PROFICIENCY

- TOFEL iBT: 102 (R26+L27+S22+W27) GRE: V157+Q168, AW 4.0

EXTRA- CURRICULAR ACTIVITIES

- UM-SJTU JI Honor Council Member — Sept 2016 – Present
- Vice-captain of Youth Volunteer Service Team in UM-SJTU JI — Sept 2015 – Aug 2016
- Vice-captain of Career Department in UM-SJTU JI Student Union — Sept 2015 – Aug 2016
- Volunteer teacher in Yousuo Elementary School, Yunnan, China — Dec 2015 – Jan 2016