VE 320 Fall 2021

Introduction to Semiconductor Devices

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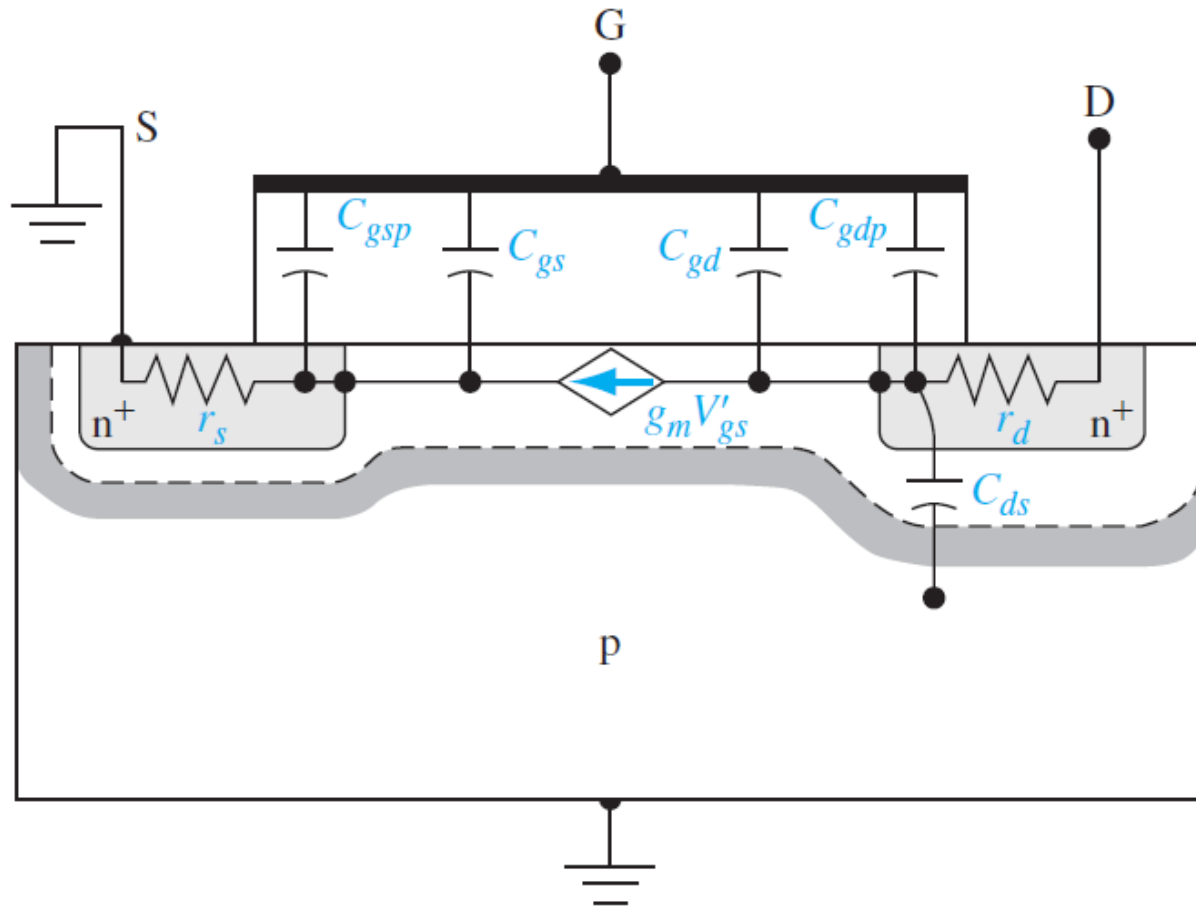
Lecture 13
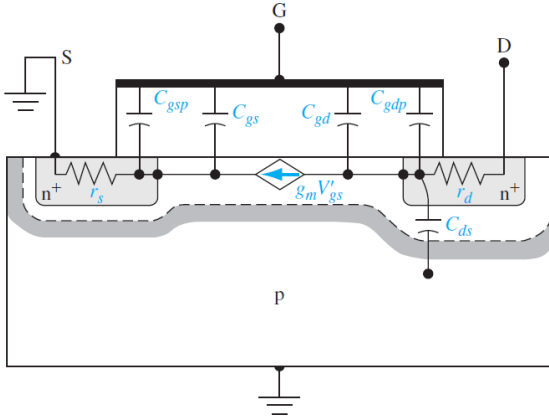
MOSFET
(Chapter 10 & 11)

MOSFET: Frequency limitation & cutoff frequency

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MOSFET: Frequency limitation & cutoff frequency

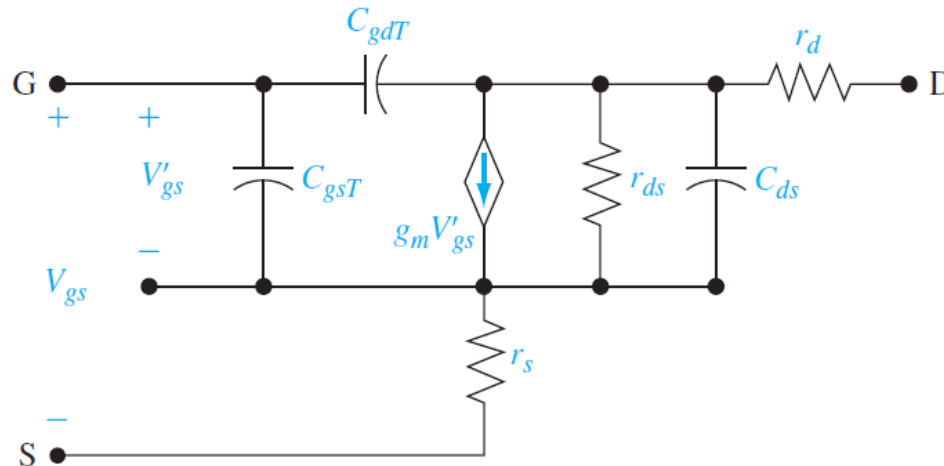Frequency limitation & cutoff frequency

C_{gs}, C_{gd}: interaction between the gate and the channel charge near the source and drain terminals

C_{gsp}, C_{gdp}: parasitic capacitance, due to overlap of the gate area and source/ drain area – Need to minimize this in real devices to get higher frequency/ speed
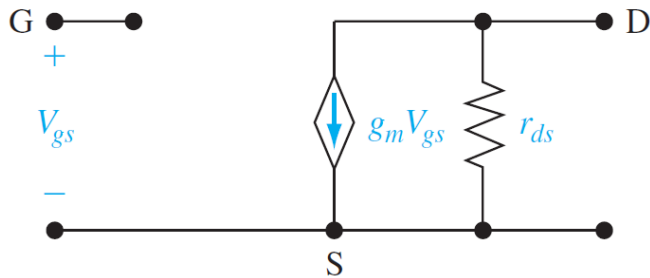
$g_m V_{gs}'$: current source, controlled by the gate voltage
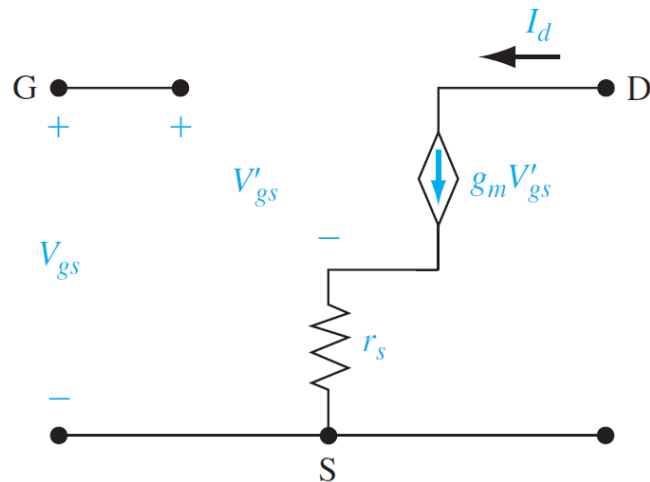
Small-signal equivalent circuit:

MOSFET: Frequency limitation & cutoff frequency

Simplified small-signal equivalent circuit at low frequency:

Common source NMOSFET
Ignored series resistances

Common source NMOSFET
Include source resistance r_s

$$I_d = g_m V'_{gs}$$

$$V_{gs} = V'_{gs} + (g_m V'_{gs})r_s = (1 + g_m r_s)V'_{gs}$$

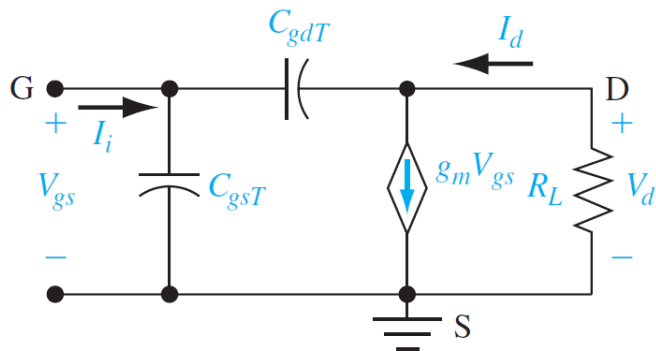$$I_d = \left(\frac{g_m}{1 + g_m r_s}\right)V_{gs} = g'_m V_{gs}$$

MOSFET: Frequency limitation & cutoff frequency

What is limiting the frequency of MOSFETs?

Carrier travel velocity? 10^7 cm/s, need 10 ps to travel 1 μm →100GHz!
Not the limiting factor

Capacitance charging!

Input:
$$I_i = j\omega C_{gsT}V_{gs} + j\omega C_{gdT}(V_{gs} - V_d)$$

Output:
$$\frac{V_d}{R_L} + g_mV_{gs} + j\omega C_{gdT}(V_d - V_{gs}) = 0$$

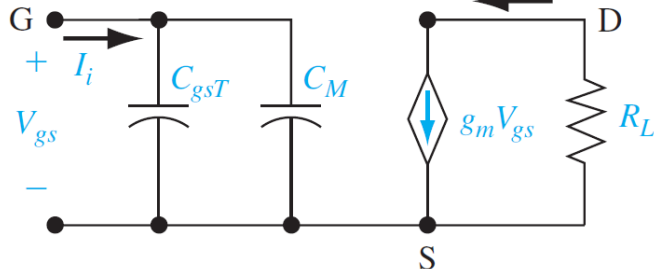$$I_i = j\omega\left[C_{gsT} + C_{gdT}\left(\frac{1 + g_mR_L}{1 + j\omega\ R_LC_{gdT}}\right)\right]V_{gs}$$

$$\omega R_L C_{gdT} \ll 1$$

$$I_i = j\omega[C_{gsT} + C_{gdT}(1 + g_mR_L)]V_{gs}$$

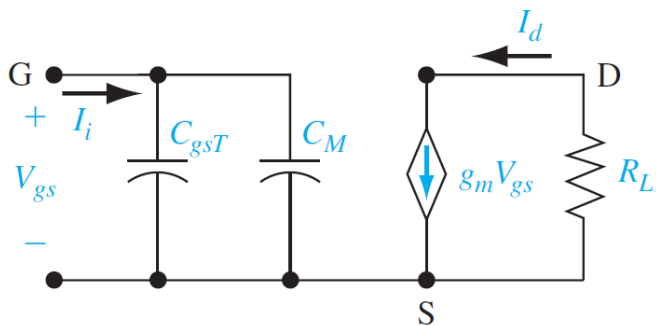$$C_M = C_{gdT}(1 + g_mR_L) \quad \text{Miller capacitance}$$

Drain overlap parasitic capacitance: important
Multiplied by gain g_m

MOSFET: Frequency limitation & cutoff frequency

Cutoff frequency f_T: the frequency at which the magnitude of the current gain of the device is unity, $I_i = I_d$

$$I_i = j\omega(C_{gsT} + C_M)V_{gs}$$

$$I_d = g_m V_{gs}$$

Current gain

$$\left|\frac{I_d}{I_i}\right| = \frac{g_m}{2\pi f(C_{gsT} + C_M)}$$

$$f_T = \frac{g_m}{2\pi(C_{gsT} + C_M)} = \frac{g_m}{2\pi C_G}$$

Ideal MOSFET in saturation: no parasitic, C_{gd} small in saturation, C_{gd} is $C_{ox}WL$
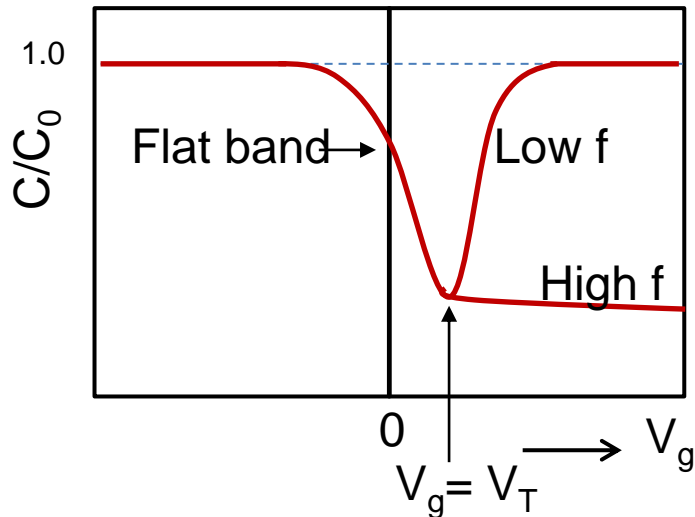
$$g_{ms} = \frac{W\mu_n C_{ox}}{L}(V_{GS} - V_T)$$

High mobility → High speed

$$f_T = \frac{g_m}{2\pi C_G} = \frac{\dfrac{W\mu_n C_{ox}}{L}(V_{GS} - V_T)}{2\pi(C_{ox}WL)} = \frac{\mu_n(V_{GS} - V_T)}{2\pi L^2}$$
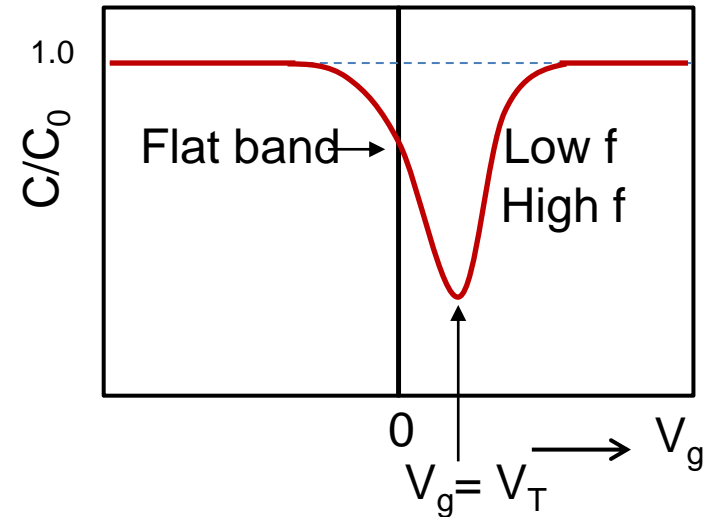
CV difference between MOS Capacitor and MOSFET

CV of MOS capacitor

Flat band →   Low f

High f

C/C_0
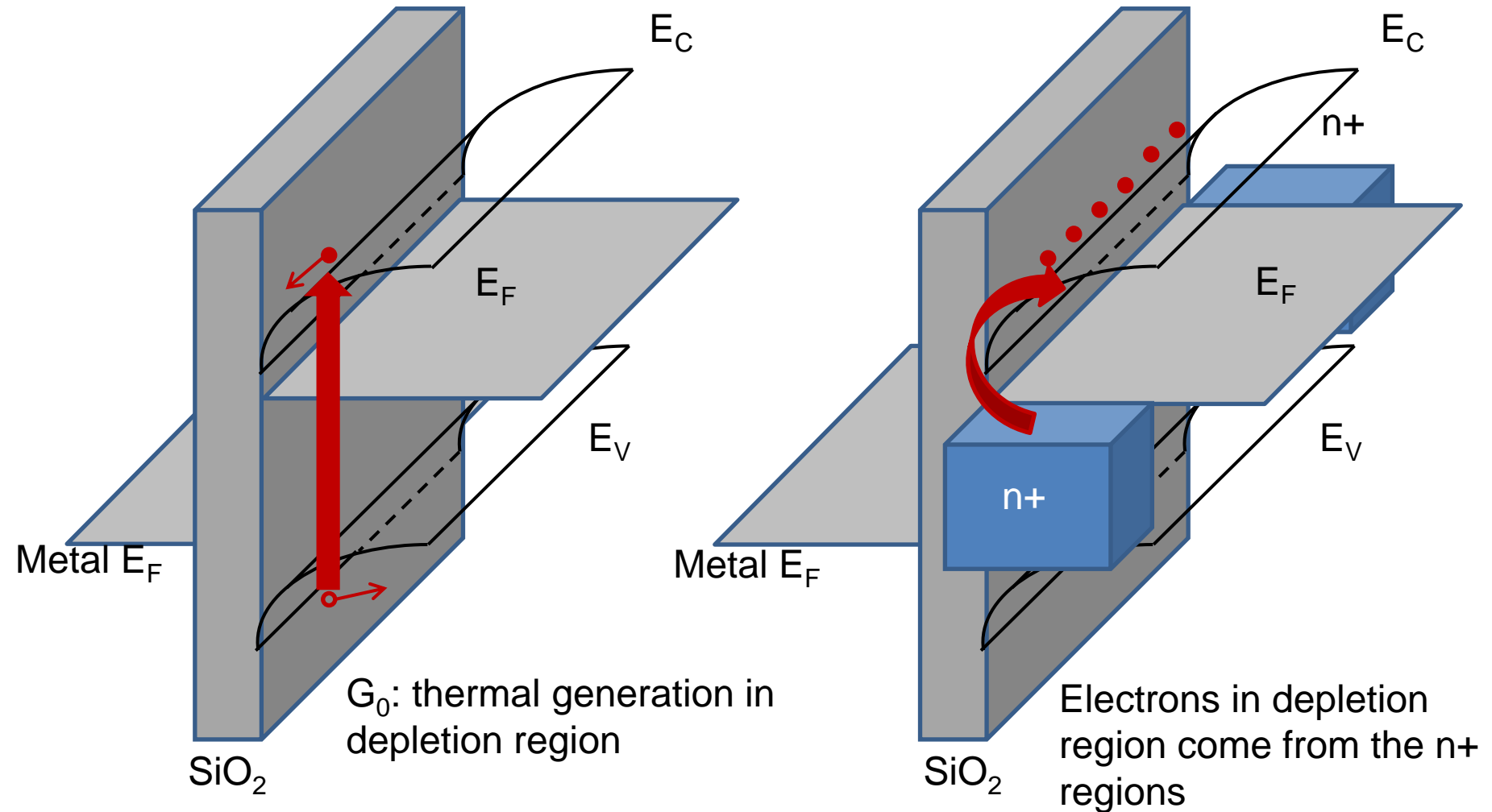
1.0

0   V_g

$V_g = V_T$

Inversion electrons come from electron generation from valance band which is slow. At high frequency, electron generation will be frozen out. Without inversion electrons, the capacitance will remain low.

CV of MOSFET

Flat band →   Low f
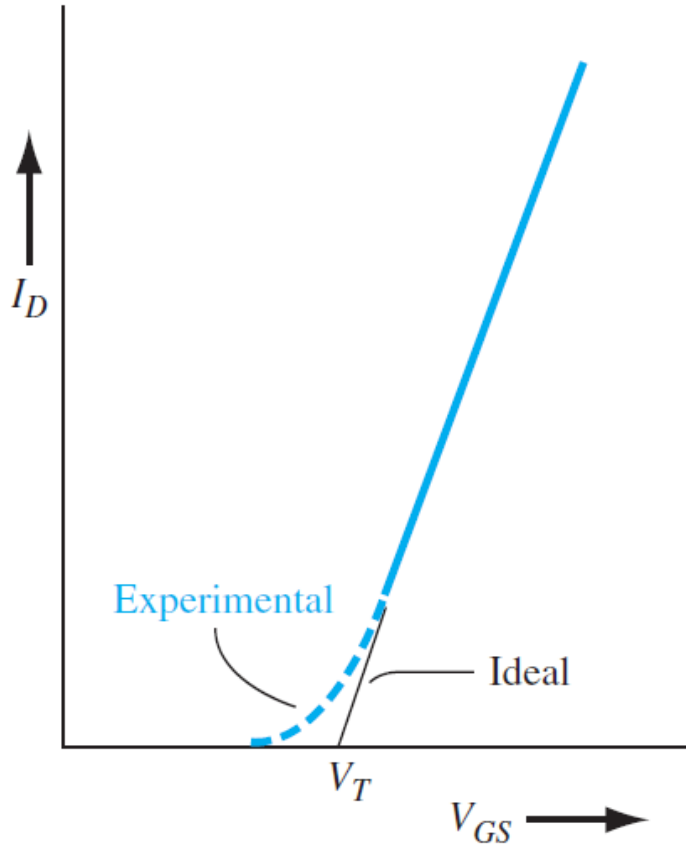High f

C/C_0

1.0

0   V_g

$V_g = V_T$

Electrons in the channel come from source and drain electrons. At high frequency, these electrons can move fast enough to respond to the gate electrode frequency.

Band structure of MOS Capacitor and MOSFET

E_C

E_F

E_V

Metal E_F

G_0: thermal generation in depletion region

SiO_2

E_C

n+

E_F

E_V

Metal E_F

n+

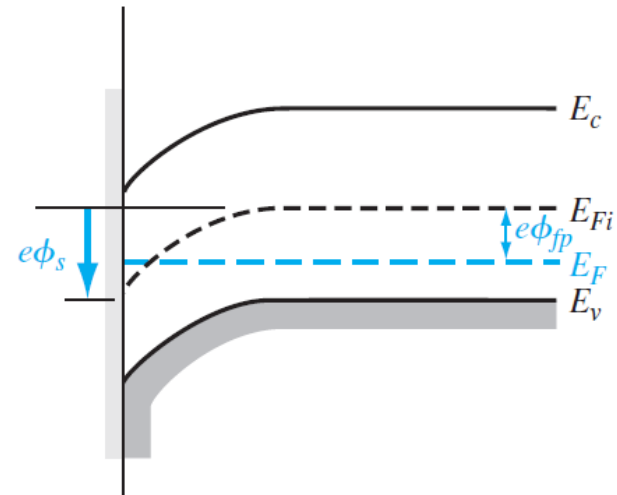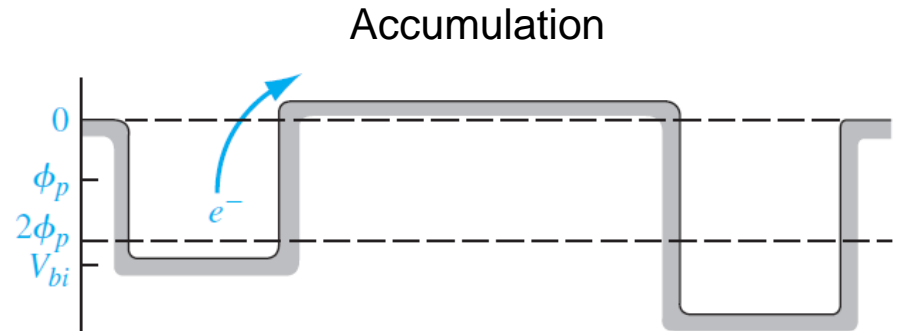Electrons in depletion region come from the n+ regions

SiO_2

MOSFET: Nonideal effects

Subthreshold leakage: drain current when $V_{GS} \leq V_T$

$$\phi_{fp} < \phi_s < 2\phi_{fp}$$

Weak inversion
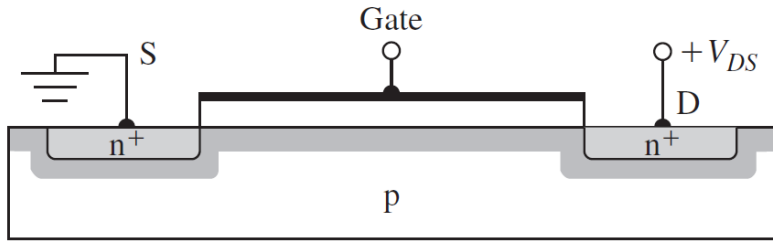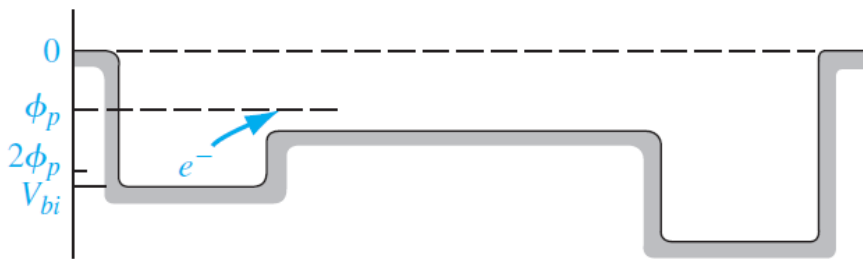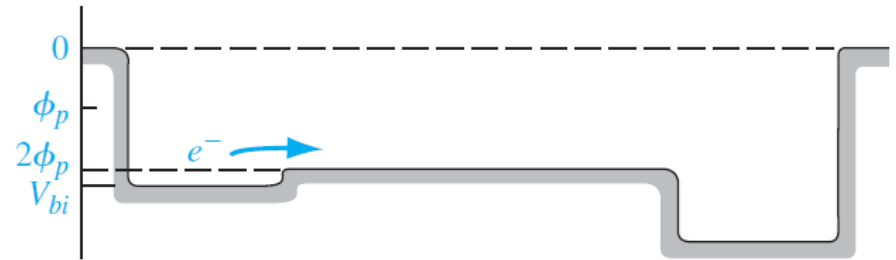
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MOSFET: Nonideal effects

Subthreshold leakage: drain current when $V_{GS} \leq V_T$

Accumulation

Weak inversion

Strong inversion

MOSFET: sub-threshold leakage current

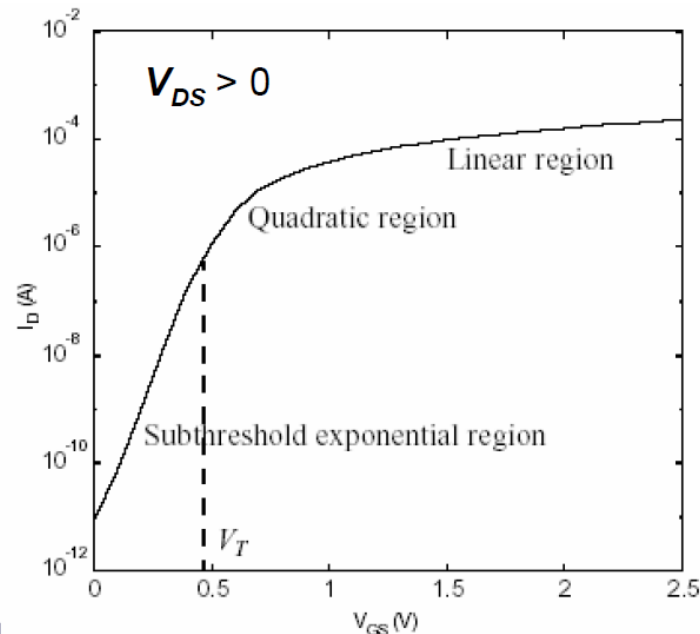## Subthreshold Conduction (Leakage Current)

- The transition from the ON state to the OFF state is gradual. This can be seen more clearly when I_D is plotted on a logarithmic scale:

- In the subthreshold ($V_{GS} < V_T$) region,

Large V_{DS}:

$$I_D \propto \exp\left(\frac{qV_{GS}}{nkT}\right)$$

This is essentially the channel-source pn junction current.
(Some electrons diffuse from the source into the channel, if this pn junction is forward biased.)
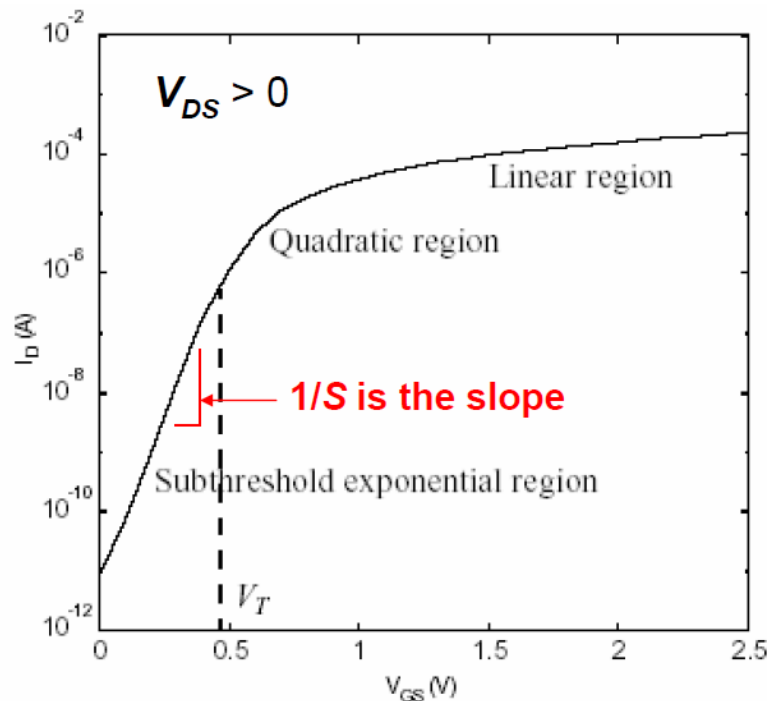

$$I_D(\text{sub}) \propto \left[\exp\left(\frac{eV_{GS}}{kT}\right)\right] \cdot \left[1 - \exp\left(\frac{-eV_{DS}}{kT}\right)\right]$$

Small V_{DS}

MOSFET: sub-threshold leakage current

Slope Factor (or Subthreshold Swing) S

- **S** is defined to be the inverse slope of the log (I_D) vs. V_{GS} characteristic in the subthreshold region:

$$S \equiv n\left(\frac{kT}{q}\right)\ln(10)$$

Ideally, n=1

Units: Volts per decade

Note that **S** $\geq$ 60 mV/dec at room temperature:

$$\left(\frac{kT}{q}\right)\ln(10) = 60\,\text{mV}$$

"Boltzmann limit"

In reality, usually larger than 60mV/dec due to semiconductor doping and interface state

MOSFET: sub-threshold leakage current

- Subthreshold leakage: lead to power dissipation in the "off" state

MOSFET: sub-threshold leakage current

- Subthreshold leakage: lead to power dissipation in the "off" state (Want to turn off at 0V)
- Want large subthreshold slope, or small subthreshold swing S
- Dynamic power dissipation $P_{dyn} \propto V_{DD}^2$
- Want to decrease V_{DD}
- Need to reduce V_T to remain large enough I_{ON}
- Lower V_T: larger off-state power dissipation P_{OFF}
- Small S: can decrease V_{DD} and V_T together, ideally $S=0$
- Limited by the MOSFET operating mechanism in the subthreshold region
- How to minimize the subthreshold leakage/ decrease the subthreshold swing?

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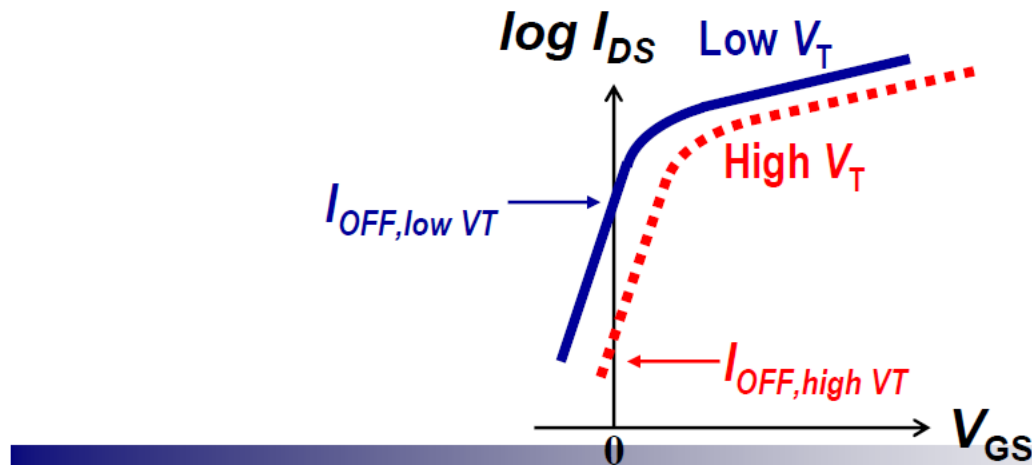# MOSFET: sub-threshold leakage current

V_T Design Trade-Off

(Important consideration for digital-circuit applications)
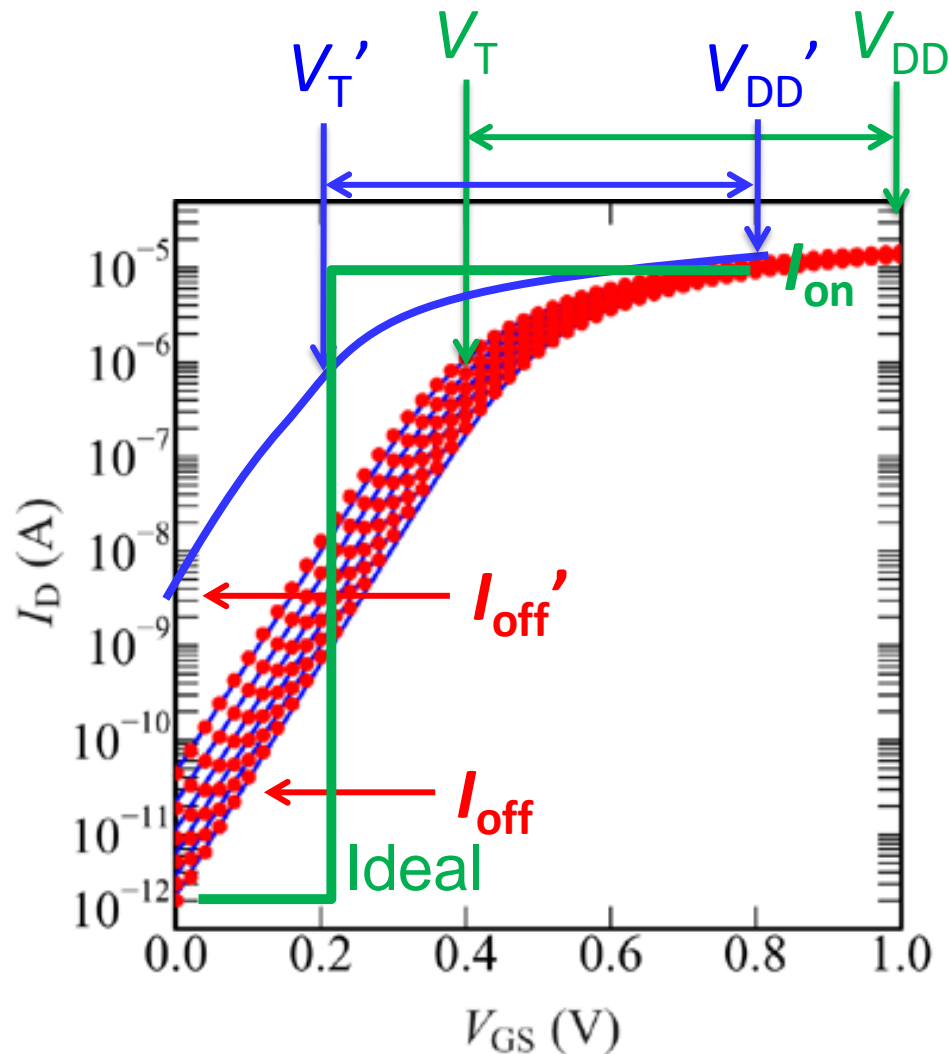
- Low V_T is desirable for high ON current

$$I_{DSAT} \propto (V_{DD} - V_T)^{\eta} \qquad 1 < \eta < 2$$

where V_{DD} is the power-supply voltage

…but high V_T is needed for low OFF current

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MOSFET: sub-threshold leakage current

Need Steep Subthreshold Slope Switches!

MOSFET: sub-threshold leakage current

- **New device technology to reduce subthreshold swing *S***
  - Microelectromechanical systems (MEMS) and nanoelectromechanical systems (NEMS) switch
  - Tunneling transistor
  - Negative capacitance transistor
  - Spin, photon

  …

  Still in active research

MOSFET: sub-threshold leakage current

Microelectromechanical systems (MEMS) and nanoelectromechanical systems (NEMS) switch
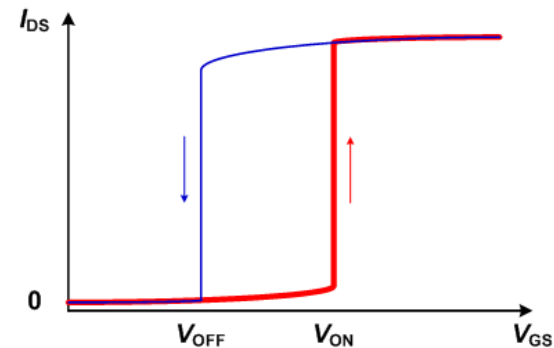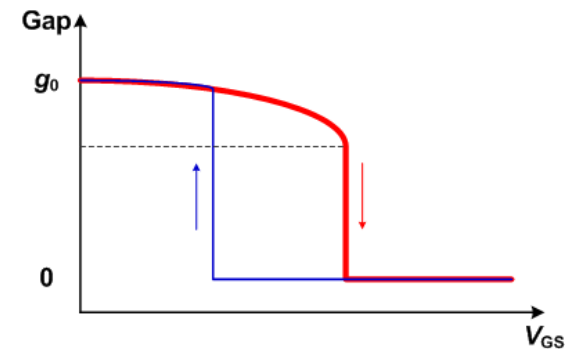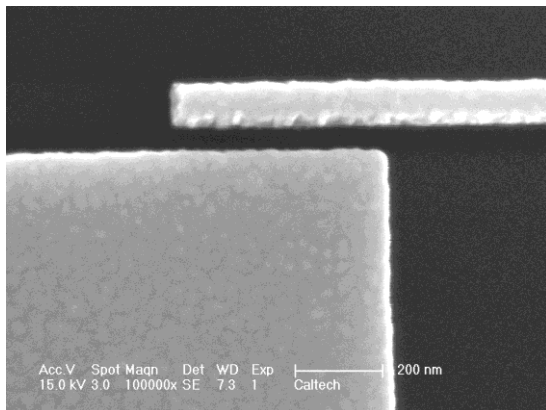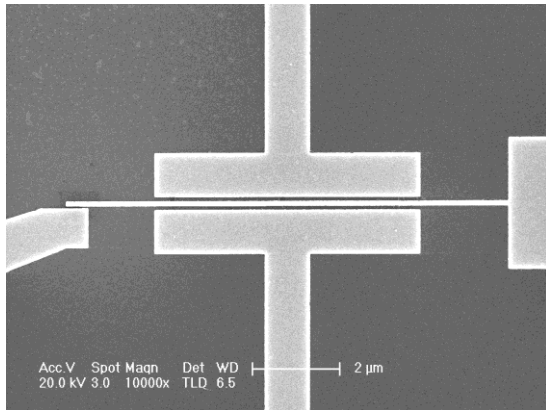
Suspended Gate ('SG') FET
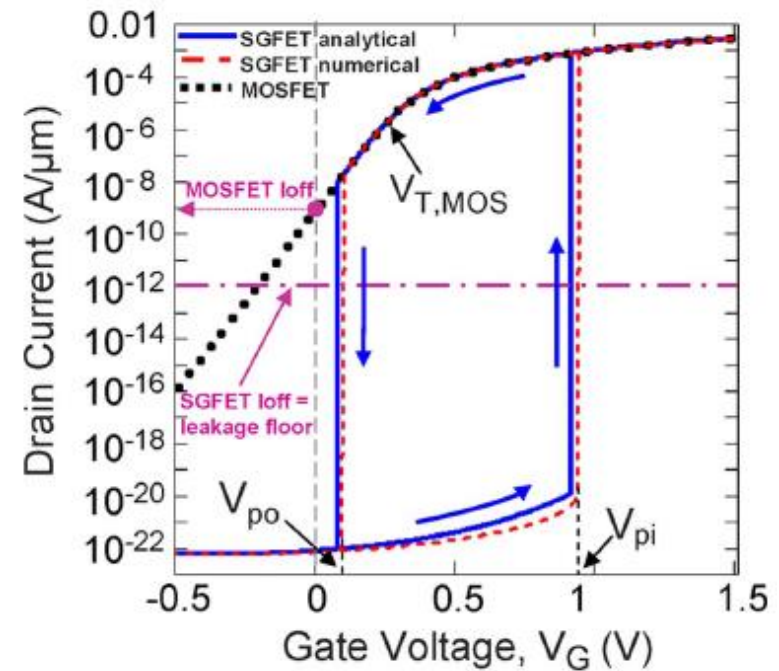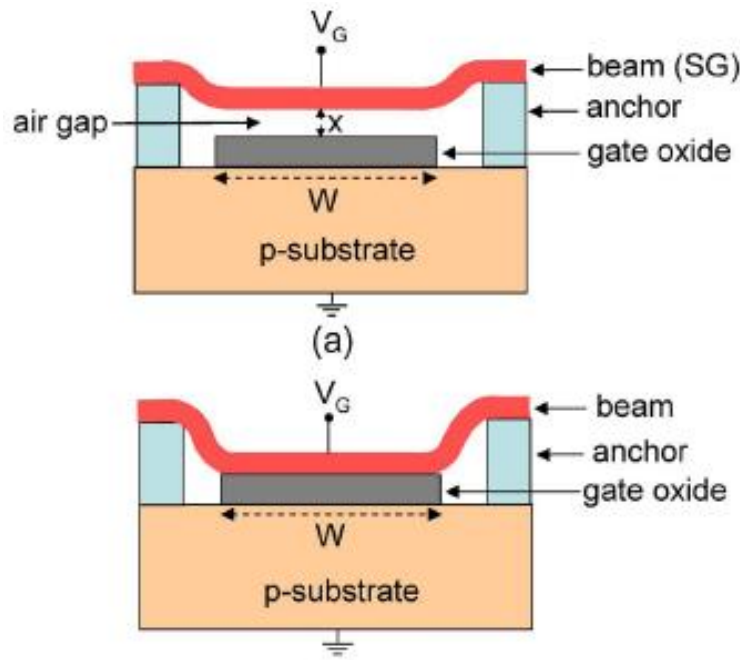
MOSFET: sub-threshold leakage current

Microelectromechanical systems (MEMS) and nanoelectromechanical systems (NEMS) switch

Suspended Gate ('SG') FET
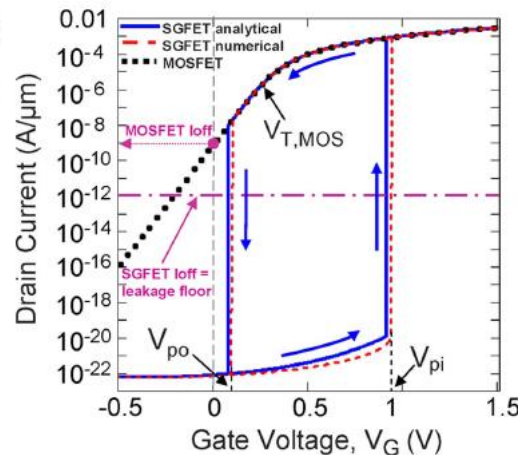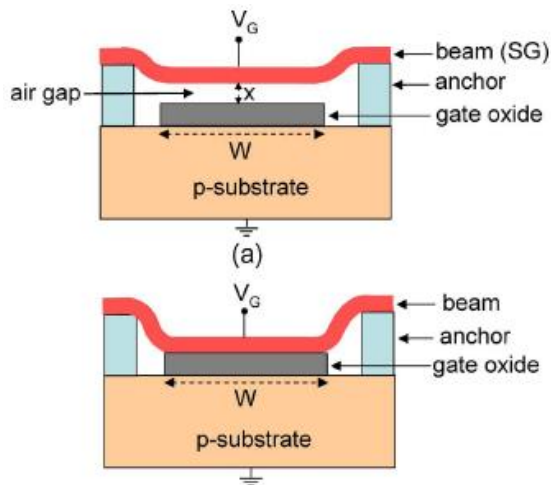
- V_{pi} within V_{DD} of transistor
- V_{pi} at weak inversion/accumulation region
- $V_{po} > 0$, suspended structure rigid enough
- Bandwidth consideration – Scaling to NEMS dimensions

Akarvadar, Eggimann, Tsamados, Chauhan, Wan, Ionescu, Howe, Wong, *et al.*, *IEEE Trans. Electron Dev.* **55**, 48-59 (2008)
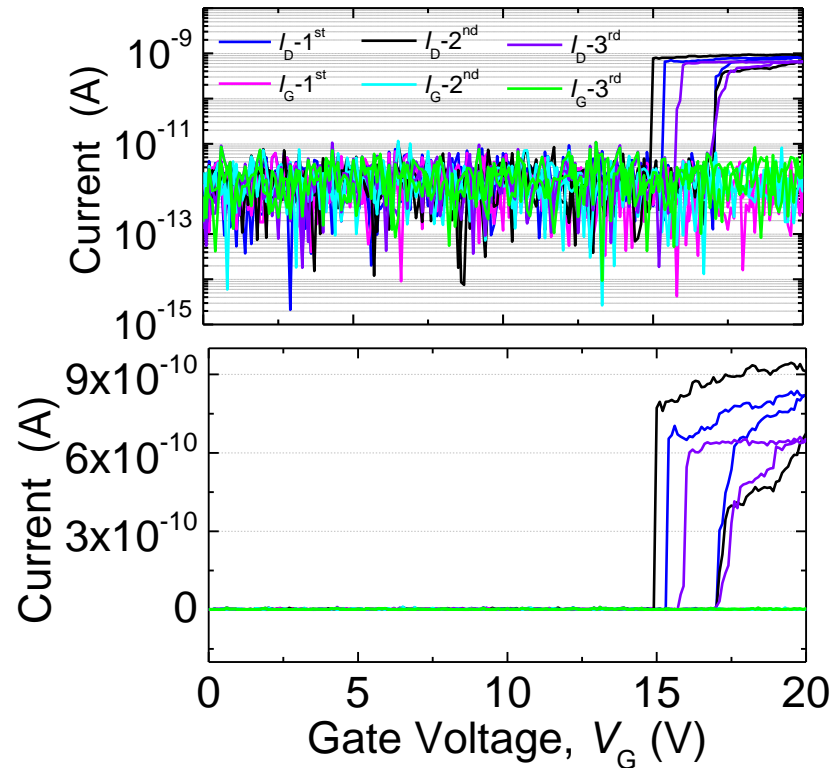
MOSFET: sub-threshold leakage current

Microelectromechanical systems (MEMS) and nanoelectromechanical systems (NEMS) switch

Pure mechanical switch: cantilever

MOSFET: sub-threshold leakage current

Microelectromechanical systems (MEMS) and nanoelectromechanical systems (NEMS) switch

Pure mechanical switch: cantilever

- **Abrupt switching!**
- ***I-V* Characteristics**
  - Switch-On voltage, V_{On}
  - Switch-Off voltage, V_{Off}
  - On State Current/Resistance, I_{ON}/R_{ON}
  - Off-State Current

T. He, *et al.*, *IEDM*, 108-111 (2013)

Tunnel FETs
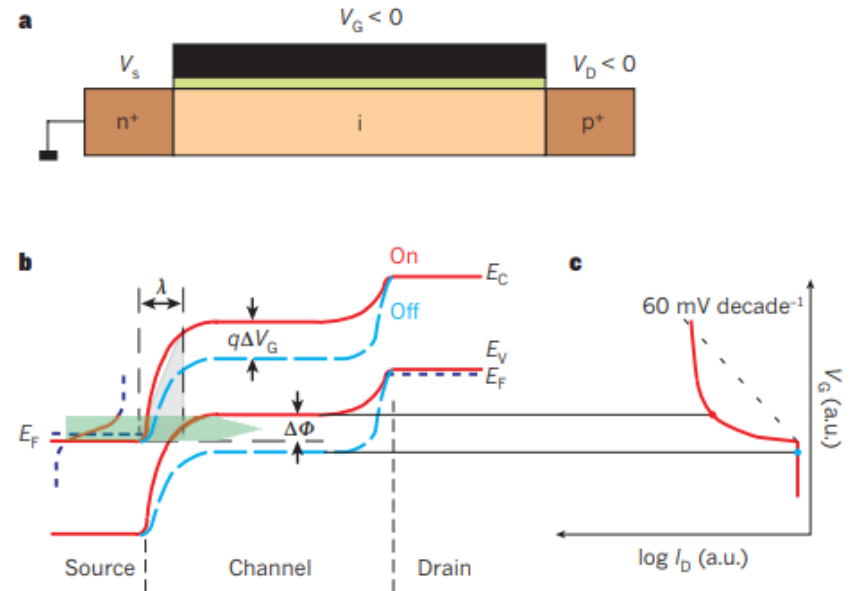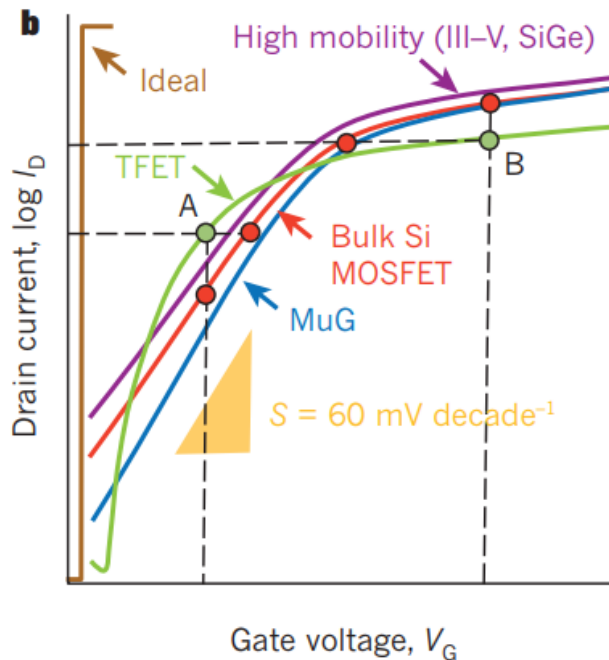
MOSFET: sub-threshold leakage current

Tunnel FETs

Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec

Woo Young Choi, *Member, IEEE*, Byung-Gook Park, *Member, IEEE*, Jong Duk Lee, *Member, IEEE*, and Tsu-Jae King Liu, *Fellow, IEEE*

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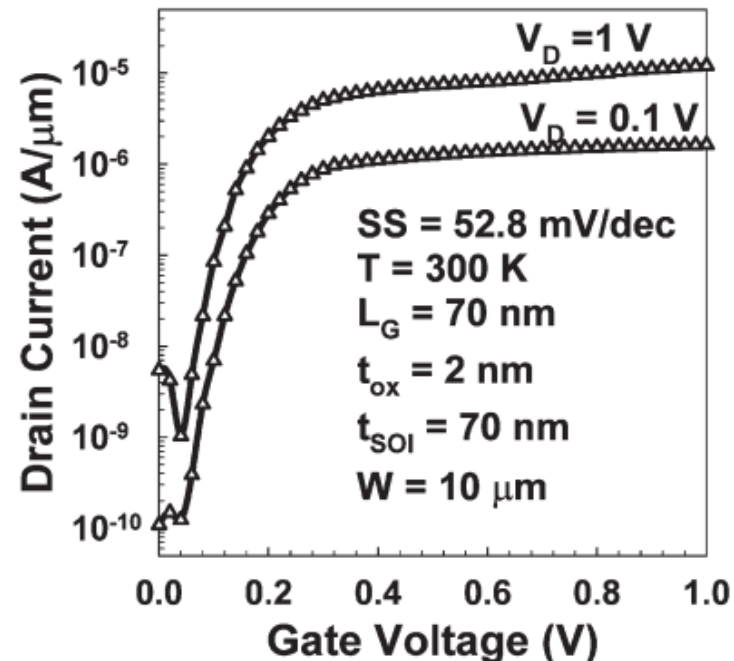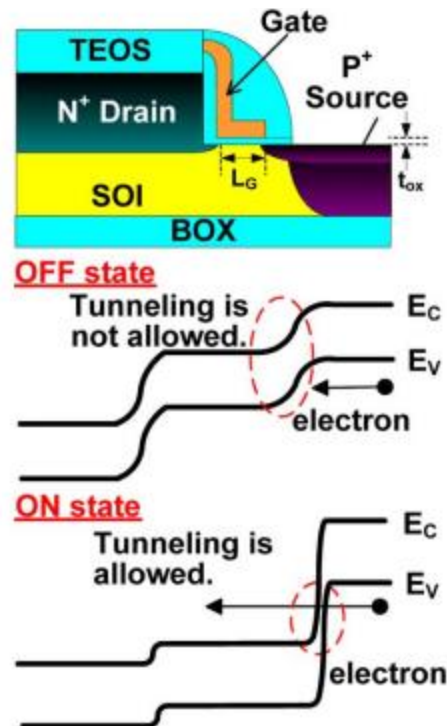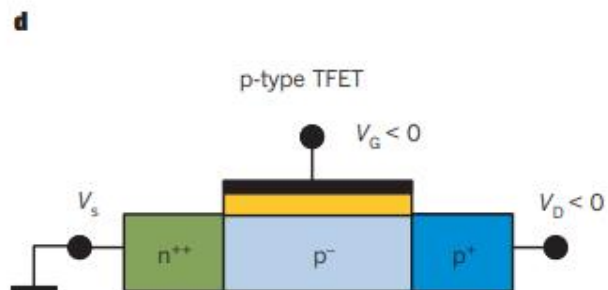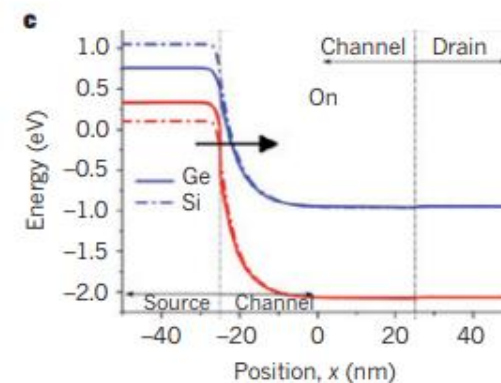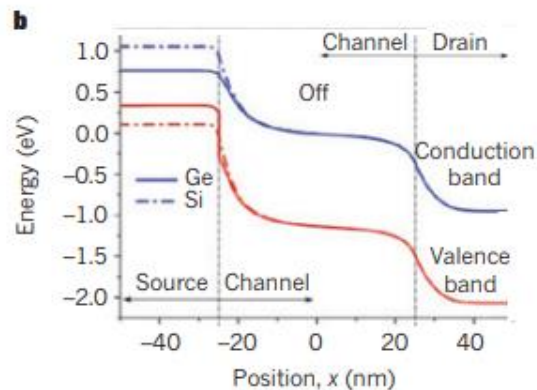
MOSFET: sub-threshold leakage current
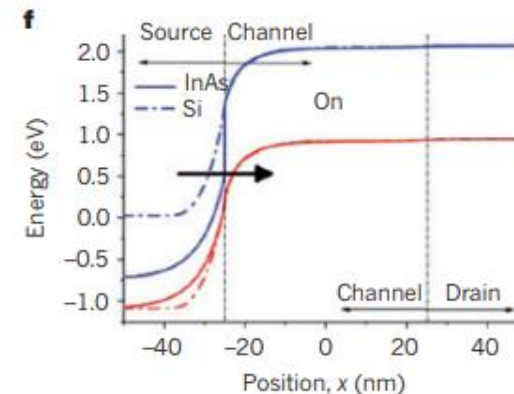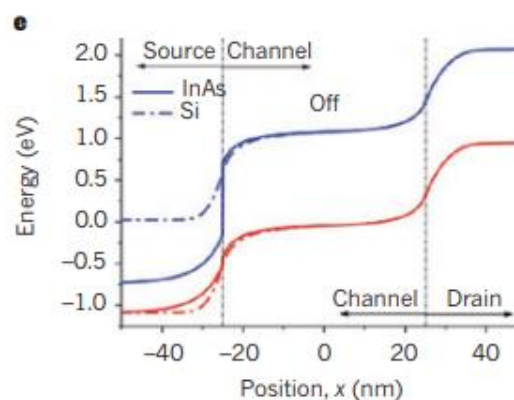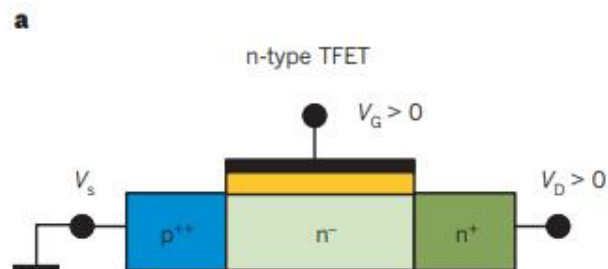
Tunnel FETs

MOSFET: sub-threshold leakage current

Tunnel FETs
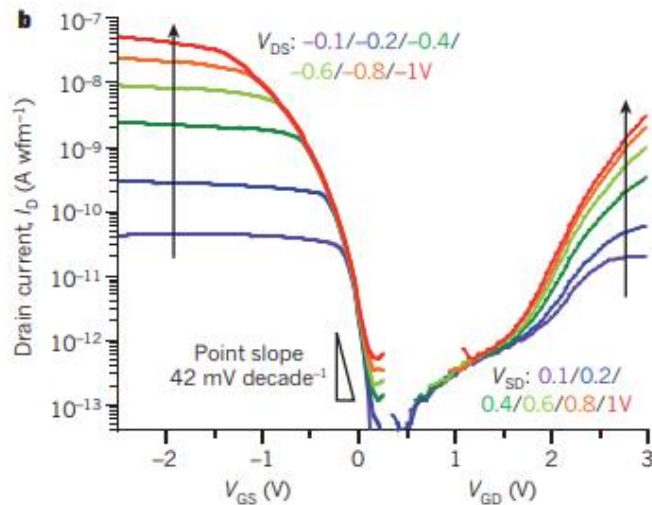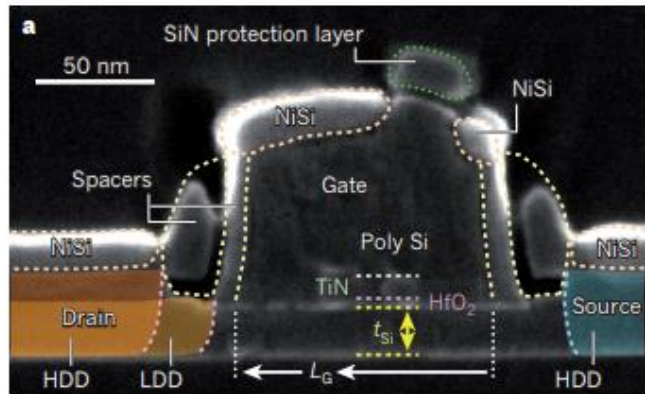
all-Si technology, silicon on insulator (SOI) TFET
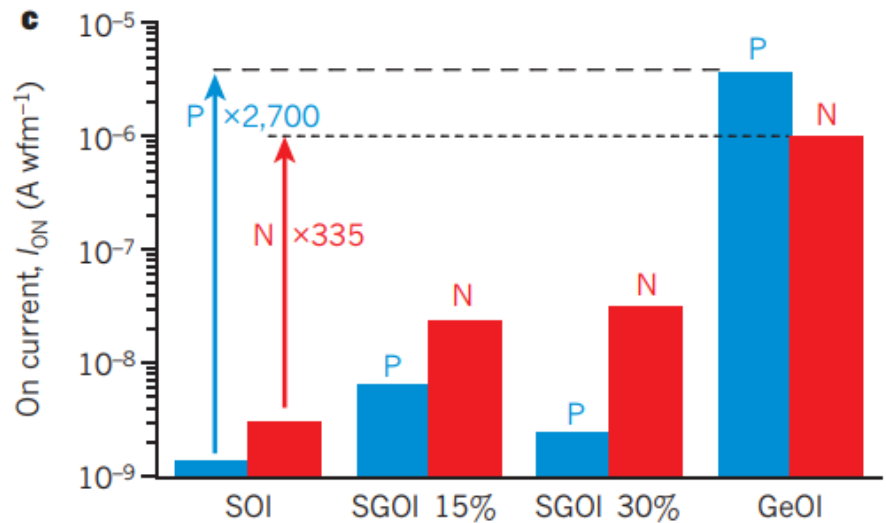
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MOSFET: channel length modulation effect

Charge sharing $\rightarrow$ threshold voltage V_T dependent on V_{ds}
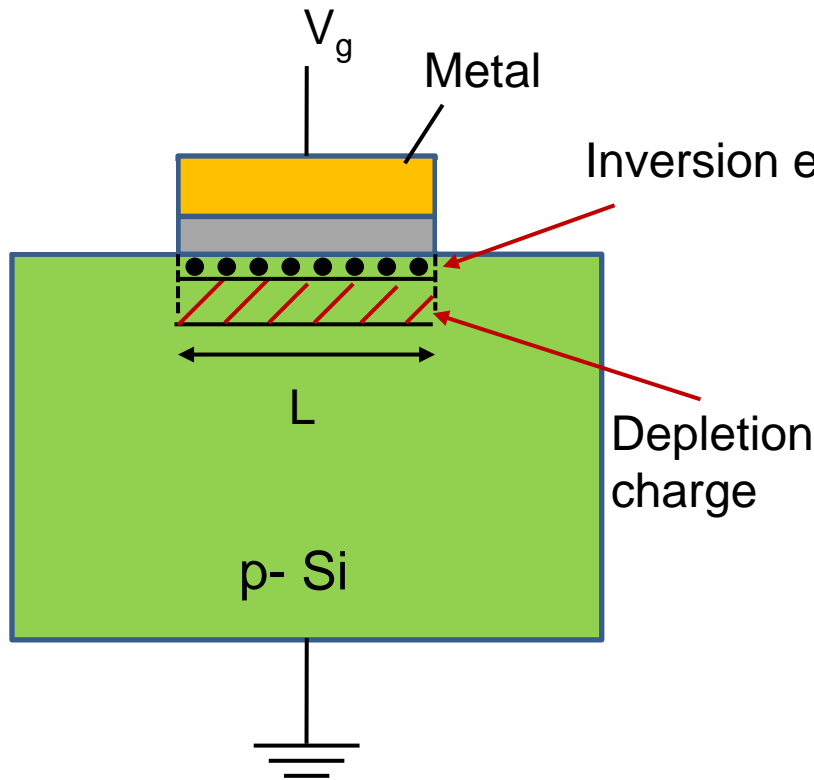
Metal-oxide-semiconductor (MOS)
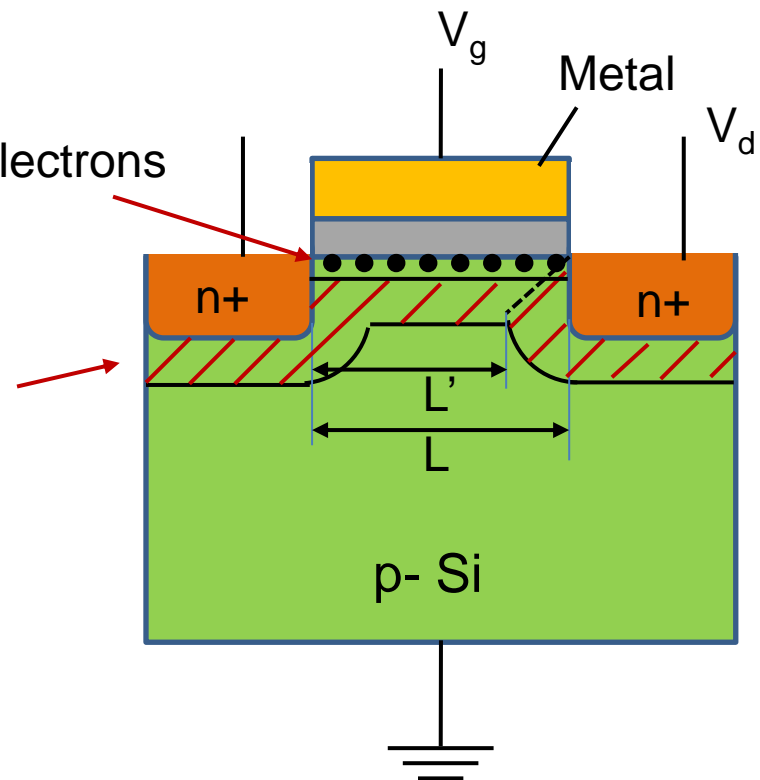
Metal-oxide-semiconductor (MOS)

MOSFET: channel length modulation effect

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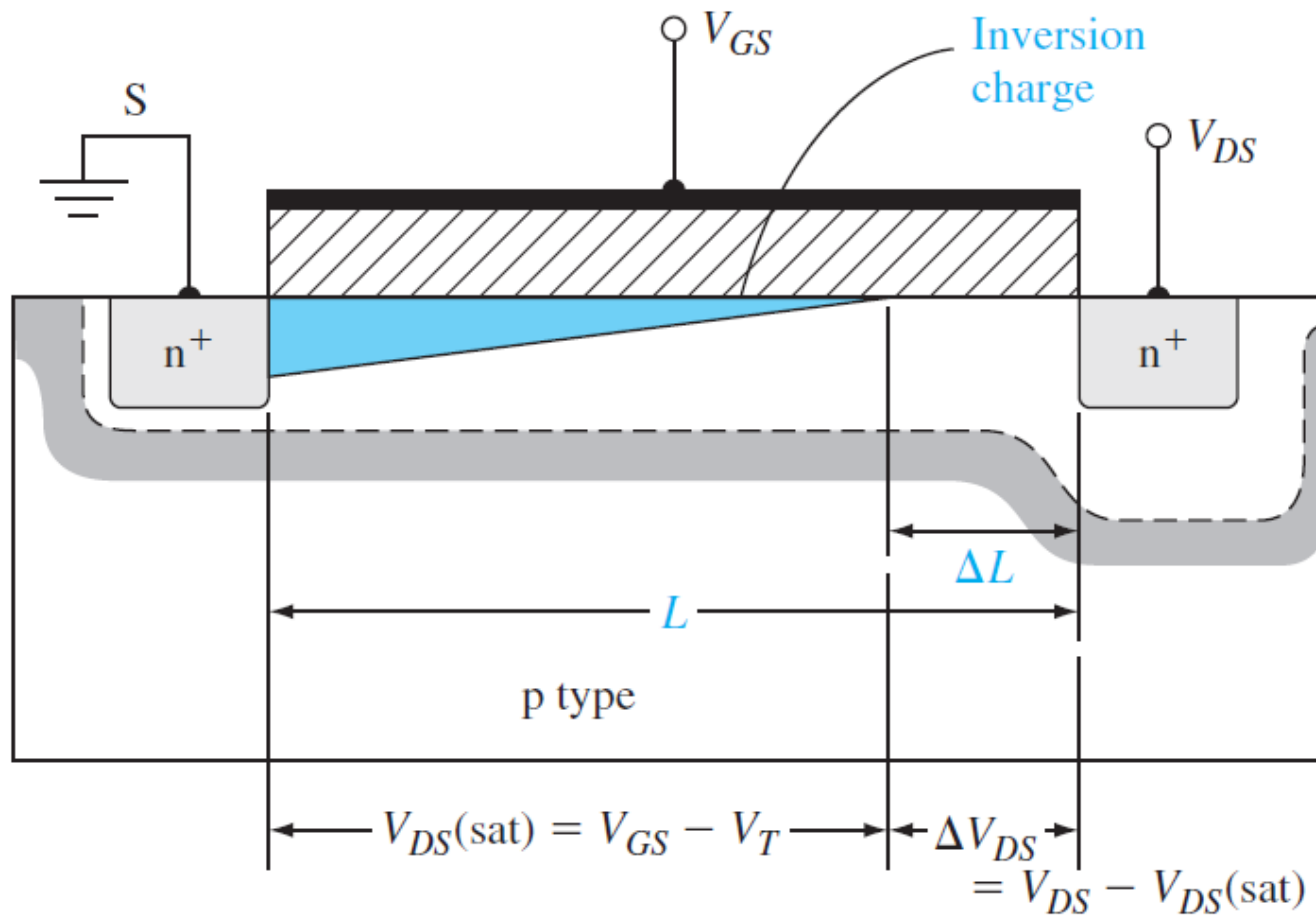
MOSFET: channel length modulation effect

If *L* is large

What Happens at Larger V_{DS}?

$V_{GS} > V_T$:

$V_{DS} = V_{GS} - V_T$
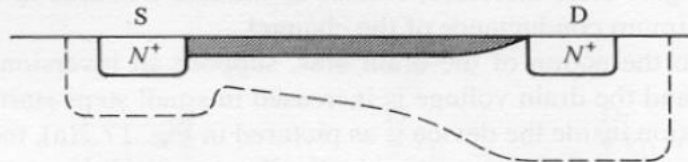
Inversion-layer is "pinched-off" at the drain end

$V_{DS} > V_{GS} - V_T$
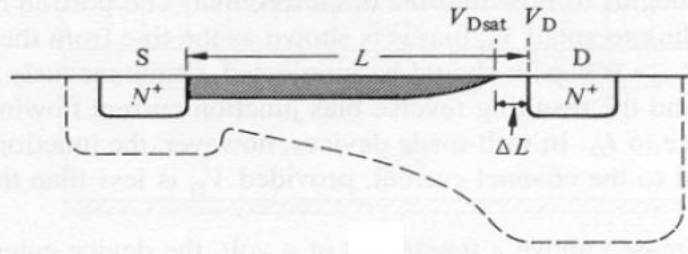
As V_{DS} increases above $V_{GS} - V_T \equiv V_{DSAT}$,

$$I_D = \mu_n C_{ox} \frac{W}{L} \left(V_{GS} - V_T - \frac{1}{2} V_{DS} \right) V_{DS}$$

I_D will not increase after $V_{ds} \geq V_{gs} - V_T$

$$I_D = \mu_n C_{ox} \frac{W}{L} \left(V_{GS} - V_T - \frac{1}{2} V_{DS} \right) V_{DS} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)(V_{GS} - V_T)$$

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MOSFET: Channel-length modulation effect

Short channel

If L is small, the effect of ΔL to reduce the inversion-layer "resistor" length is significant

$\rightarrow I_D$ increases noticeably with ΔL (*i.e.* with V_{DS})

$I_D = I_D'(1 + \lambda V_{DS})$

λ is the slope

I_D' is the intercept

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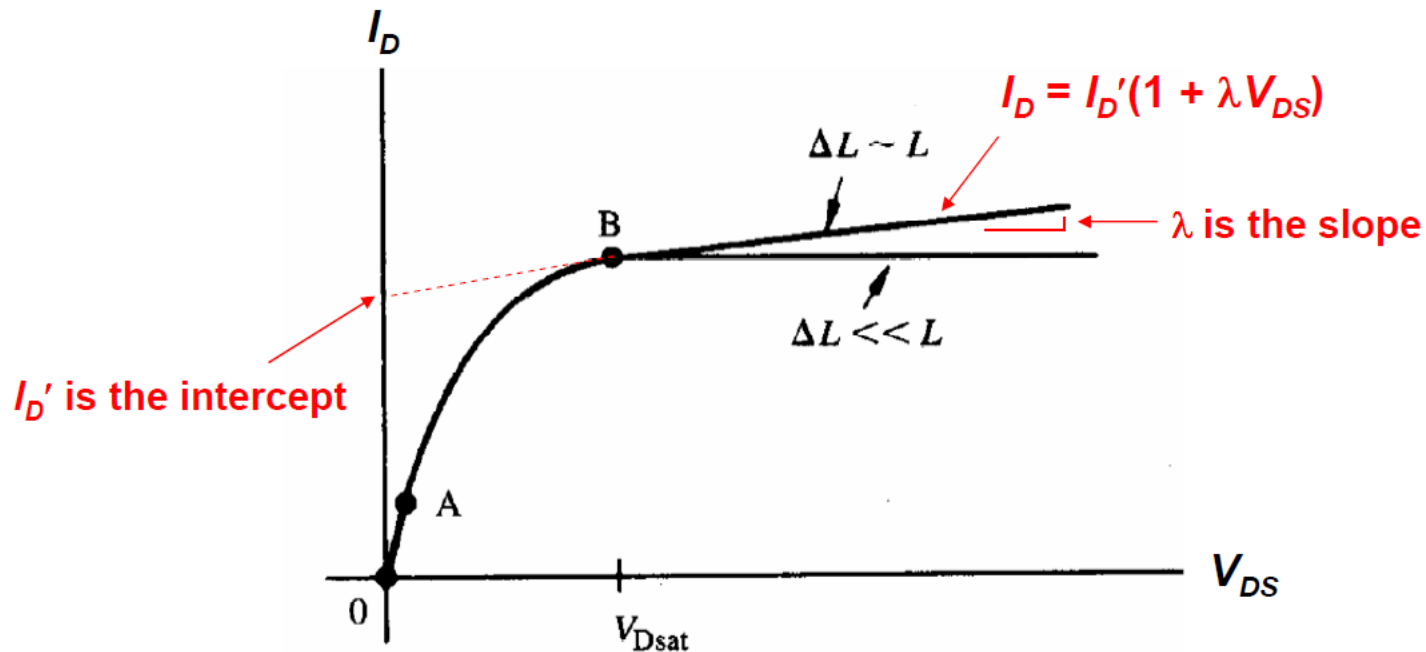
MOSFET: Channel-length modulation effect

- As compared to an n-channel MOSFET, the signs of all the voltages and the currents are reversed:

Short-channel PMOSFET *I-V*
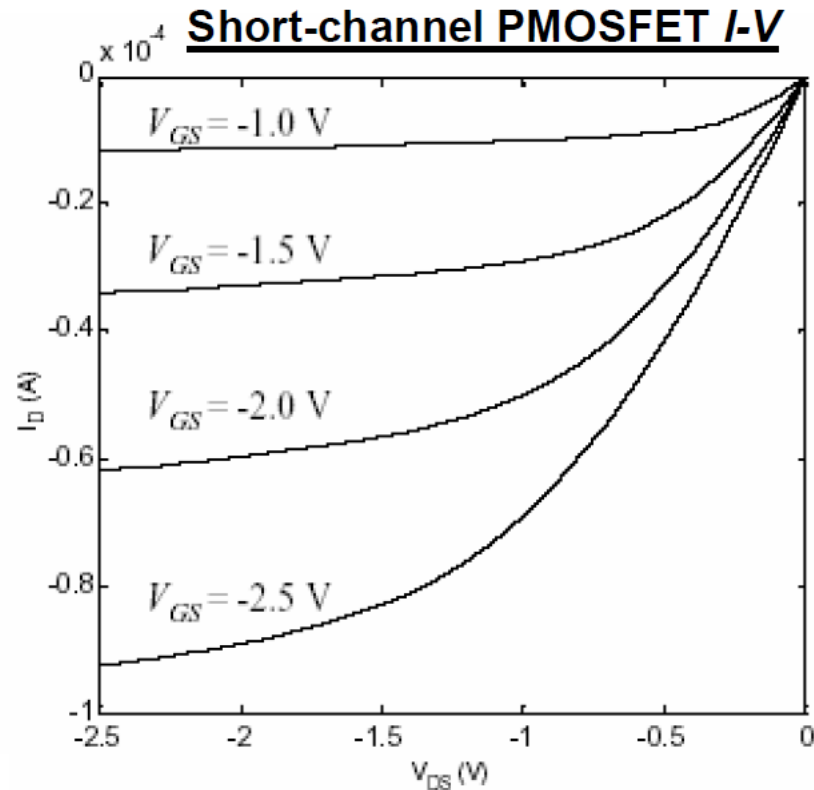
MOSFET: Channel-length modulation effect

Short channel

For a n⁺p junction, essentially all of the applied reverse-biased voltage is across the low-doped p region. Space charge width

$$x_p = \sqrt{\frac{2\epsilon_s}{eN_a}(\phi_{fp} + V_{DS})}$$

ΔL is the total space charge width minus the space charge width that exists when $V_{DS} = V_{DS}$ (sat)

$$\Delta L = \sqrt{\frac{2\epsilon_s}{eN_a}}\left[\sqrt{\phi_{fp} + V_{DS}(\text{sat}) + \Delta V_{DS}} - \sqrt{\phi_{fp} + V_{DS}(\text{sat})}\right]$$

$$\Delta V_{DS} = V_{DS} - V_{DS}(\text{sat})$$

MOSFET: Channel-length modulation effect

Short channel

Drain current is inversely proportional to the channel length, the actual current

$$I'_D = \left(\frac{L}{L - \Delta L} \right) I_D$$

The output resistance is no longer infinite

$$I'_D = \frac{k'_n}{2} \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \right]$$
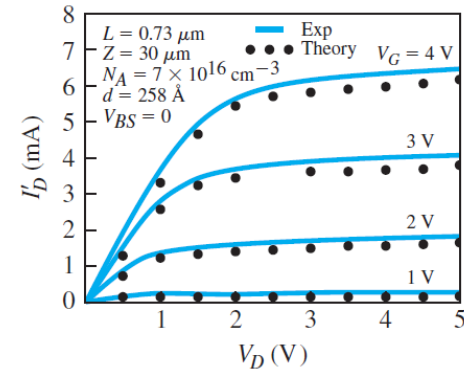
λ is the channel length modulation parameter

Output resistance

$$r_o = \left(\frac{\partial I'_D}{\partial V_{DS}} \right)^{-1} = \left\{ \frac{k'_n}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot \lambda \right\}^{-1}$$
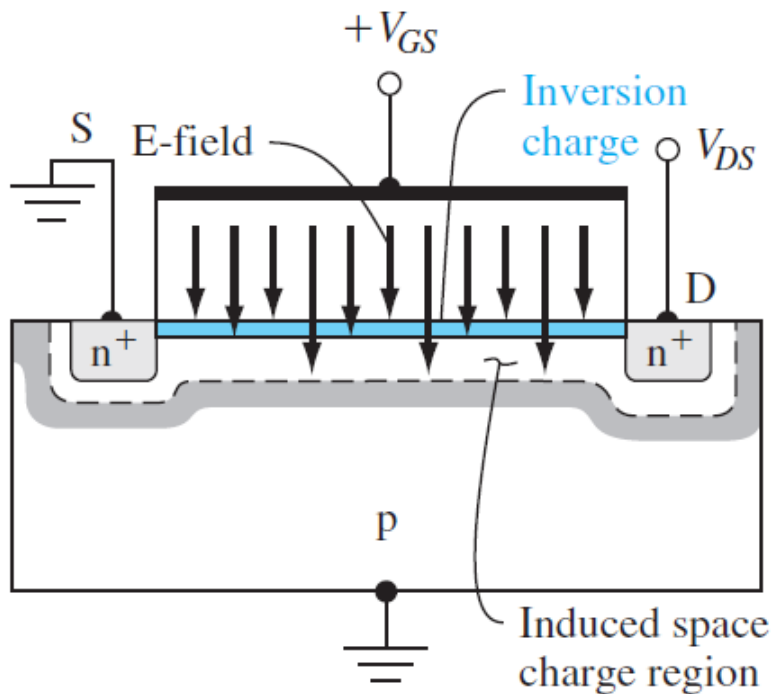
λ is usually small

$$r_o \cong \frac{1}{\lambda I_D}$$

MOSFET: Mobility variation

Mobility not a constant

- Variation of mobility with gate voltage
- Effective carrier mobility decreases as the carrier approaches the velocity saturation limit

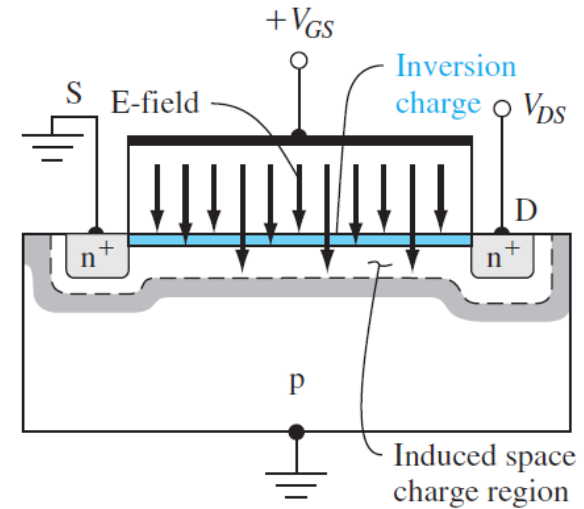Why mobility changes with gate voltage?

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MOSFET: Mobility variation

Mobility not a constant

Why mobility changes with gate voltage?

Electrons scatter at the surface, due to coulomb force: surface scattering

If there positive fixed oxide charge near the oxide-semiconductor interface, the mobility will be further reduced due to the additional coulomb interaction

Electric field

$$E_{\text{eff}} = \frac{1}{\epsilon_s}\left(\left|Q'_{SD}(\max)\right| + \frac{1}{2}Q'_n\right)$$

MOSFET: Mobility variation

Mobility not a constant

Oxide

S — D

Space charge region

Inversion layer
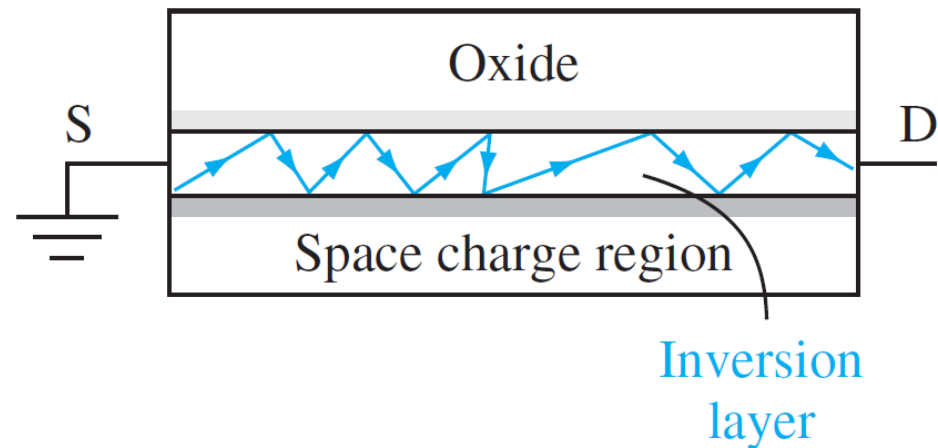
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$$\mu_{\text{eff}} = \mu_0 \left(\frac{E_{\text{eff}}}{E_0} \right)^{-1/3}$$

Slope $= -1/3$

Electron mobility ($\text{cm}^2/\text{V}\cdot\text{s}$) vs. Effective field in inversion layer, E_{eff} (V/cm)