JOINT INSTITUTE
交大密西根学院

Ve270 Introduction to Logic Design

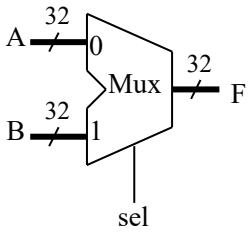
Homework 5

Assigned: June 11, 2020

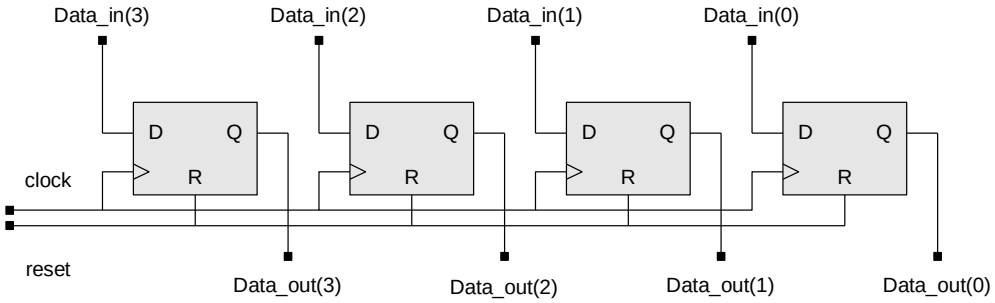
Due: June 18, 2020, 2:00pm.

A pop quiz will be given on the due date.

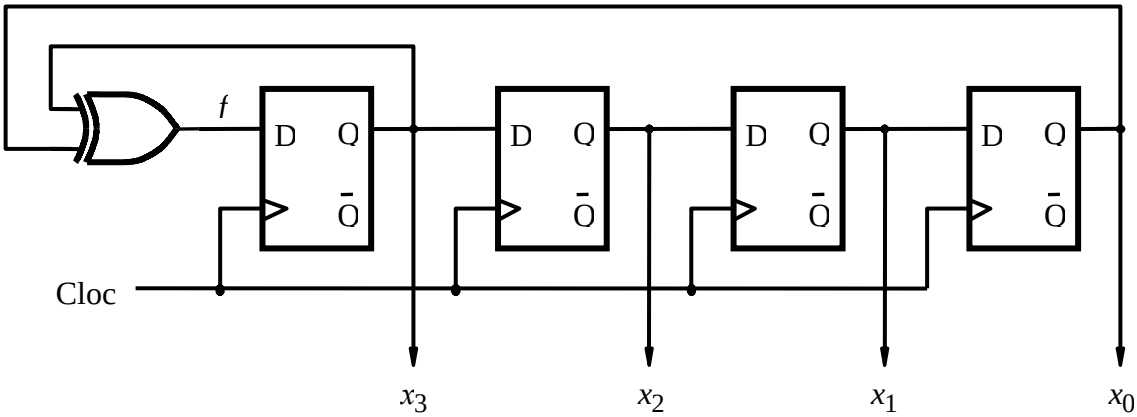
1. Describe a 32-bit 2-to-1 MUX in Verilog. Simulate your Verilog module. (20 points)



2. Model the following circuit with Verilog HDL. The circuit should be modeled by instantiating four D flip-flops. Simulate your Verilog module. (20 points)



3. Model the following circuit with Verilog HDL. Simulate your Verilog module. (20 Points)



4. Design a 4-bit down-counter that has three control inputs: `CE` enables counting down, `clear` synchronously resets the counter to all 0s, and `set` synchronously sets the counter

to all 1s. Design the counter using MUXes and gates and D flip flops without any external control signal (e.g. reset or set). Model the circuit in Verilog HDL. Simulate your Verilog module. (20 Points)

5. Design a 4-bit up-counter with a `CE` (count enable) and `load` control inputs and an additional output `upper` that outputs a `1` whenever the counter is within the upper half of the counter's range, `8` to `15`, otherwise `0`. Design the counter using MUXes and gates and D flip flops without any external control signal (e.g. reset or set). Model the circuit in Verilog HDL. Simulate your Verilog module. (20 Points)

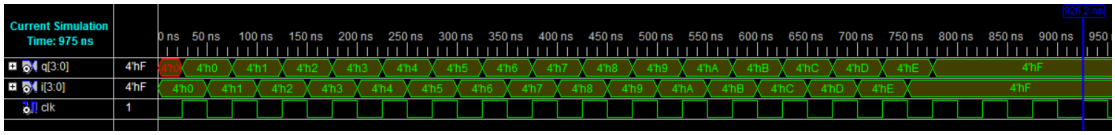
HW5 Report

Q1. (IF Q1 is “Describe a 4-bit register in Verilog. Simulate your Verilog module.”)

Verilog Code:

```
21  module Q1(i, o, clk);
22     input [3:0] i;
23     input clk;
24     output [3:0] o;
25     reg [3:0] o;
26     always @(posedge clk) begin
27        o<=i;
28     end
29  endmodule
```

Simulation Result:



// (Make sure all the characters in the figure are still visible)

Q2.

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