Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

High-Performance Computing Lab for CSE **2024**

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Solution for Project 1a

Due date: 11 March 2024, 23:59

HPC Lab for CSE 2024 — Submission Instructions
(Please, notice that following instructions are mandatory: submissions that don't comply with, won't be considered)

- Assignments must be submitted to Moodle (i.e. in electronic format).
- Provide both executable package and sources (e.g. C/C++ files, Matlab). If you are using libraries, please add them in the file. Sources must be organized in directories called:
  Project_number_lastname_firstname
  and the file must be called:
  project_number_lastname_firstname.zip
  project_number_lastname_firstname.pdf
- The TAs will grade your project by reviewing your project write-up, and looking at the implementation you attempted, and benchmarking your code's performance.
- You are allowed to discuss all questions with anyone you like; however: (i) your submission must list anyone you discussed problems with and (ii) you must write up your submission independently.

1. Euler warm-up [10 points]

1. The module system is a tool used to manage software environments on a Euler. It allows us to configure their environment by dynamically loading or unloading software modules. These modules adjust system variables to ensure that the necessary binaries and libraries are accessible. You use it by loading specific software versions with module load and unloading them with module unload when done.
2. Slurm is a tool used in big computer clusters to help manage who gets to use the computers and when. It schedules tasks and makes sure everything runs smoothly by allocating resources like processors and memory. It's like the traffic controller for a cluster of computers.
3. see hostname.cpp
4. see slurm_job_one.sh
5. see slurm_job_two.sh

2. Performance characteristics [50 points]

2.1. Peak performance

Source: `https://scicomp.ethz.ch/wiki/Euler#Euler_VII_.E2.80.94_phase_1`

Table 1: Euler VII Phase 1 and Phase 2 Specifications

Phase	Compute Nodes	CPUs per Node	CPU	Clock Speed (GHz)
Phase 1	292	2	AMD EPYC 7H12	2.6
Phase 2	248	2	AMD EPYC 7763	2.45

$$
\begin{aligned}
n_{\text{super}} &= \frac{1}{TP} = 2 \\
n_{\text{FMA}} &= 2 \\
n_{\text{SMID}} &= 4
\end{aligned}
$$

Values are the same for both Euler VII Phase 1 and 2.
Source for FMA, TP and : `https://uops.info/table.html`
Source for the SIMD values: "Software Optimization Guide for AMD EPYC™ 7002 Processors" and Software Optimization Guide for AMD EPYC™ 7003 Processors"

$$
\begin{aligned}
P_{\text{core}} &= n_{\text{super}} \cdot n_{\text{FMA}} \cdot n_{\text{SMID}} \cdot f \\
P_{\text{CPU}} &= P_{\text{core}} \cdot \#\text{Cores} \\
P_{\text{node}} &= P_{\text{core}} \cdot \#\text{CPUs} \\
P_{\text{EulerVII}} &= P_{\text{node}} \cdot \#\text{Nodes}
\end{aligned}
$$

Table 2: Peak Performance Comparison

Metric	Phase 1	Phase 2
P_{core}	41.6 GFLOP/s	39.2 GFLOP/s
P_{CPU}	2.66 TFLOP/s	2.51 TFLOP/s
P_{node}	5.32 TFLOP/s	5.02 TFLOP/s
P_{EulerVII}	1.55 PFLOP/s	1.24 PFLOP/s

2.2. Memory Hierarchies

2.2.1. Cache and main memory size

Table 3: Cache and Main Memory Sizes

Phase	L1 (KB)	L2 (KB)	L3 (MB)	Main Memory (GB)
Phase 1	32	512	16	256
Phase 2	32	512	32	256

The only difference between the cache sizes of Phase 1 and Phase 2 is the L3 cache size. Phase 2 has twice the L3 cache size of Phase 1.

2.3. Bandwidth: STREAM benchmark

2.4. Performance model: A simple roofline model