Verilog is a widely used **Hardware Description Language (HDL)** that enables engineers to model, design, and simulate digital electronic systems. Unlike traditional programming languages that execute sequentially, Verilog describes hardware that operates **concurrently**, meaning different parts of the circuit function in parallel, just like real-world electronics.

It allows designers to work at various levels of abstraction, from high-level behavioral descriptions (what the circuit does) to detailed gate-level implementations (how it's physically built). This flexibility makes Verilog suitable for designing everything from simple logic gates to complex microprocessors and entire Systems-on-Chip (SoCs).

Verilog code is processed by **synthesis tools** that translate the high-level descriptions into actual physical gates and interconnections (a netlist), which can then be fabricated onto an Application-Specific Integrated Circuit (ASIC) or programmed onto a Field-Programmable Gate Array (FPGA). It's an indispensable tool in modern digital circuit design, bridging the gap between abstract design concepts and tangible hardware.