RISC-V is an open-source instruction set architecture (ISA) based on the principles of Reduced Instruction Set Computer (RISC). Unlike proprietary ISAs like ARM or x86, RISC-V is freely available for anyone to use, modify, and distribute without licensing fees or royalties.

Conceived at the University of California, Berkeley, in 2010, RISC-V has rapidly gained traction due to its simplicity, modularity, and extensibility. Its design emphasizes a small, efficient base instruction set (like RV32I for 32-bit integer operations). It allows designers to add optional extensions (e.g., for floating-point, vector, or atomic operations) to tailor processors for specific applications.

This open approach fosters innovation, reduces development costs, and promotes transparency, making RISC-V ideal for diverse applications, from tiny embedded systems and IoT devices to high-performance computing and data centers. The growing global RISC-V ecosystem, supported by a non-profit foundation, signifies its potential to revolutionize the semiconductor industry.