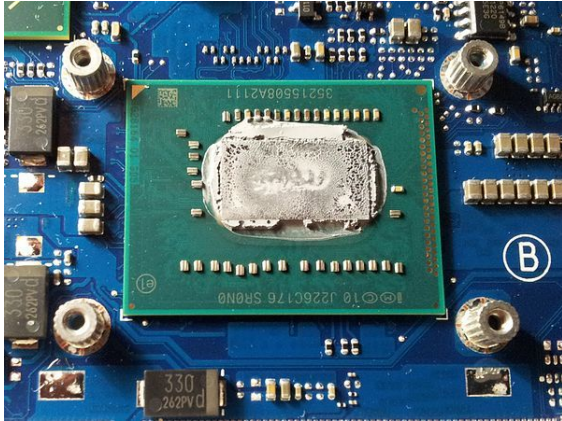


Ivy Bridge (microarchitecture)

This article is about the Intel microarchitecture. For other uses, see [Ivy Bridge](#).



Ivy Bridge processor

Ivy Bridge is the [codename](#) for a “third generation” line of processors based on the 22 nm manufacturing process developed by Intel. The name is also applied more broadly to the 22 nm die shrink of the Sandy Bridge microarchitecture based on [FinFET](#) (“3D”) [tri-gate transistors](#), which is also used in the [Xeon](#) and [Core i7 Ivy Bridge-EX](#) (Ivytown), [Ivy Bridge-EP](#) and [Ivy Bridge-E](#) microprocessors released in 2013.

Ivy Bridge processors are backwards compatible with the Sandy Bridge platform, but such systems might require a firmware update (vendor specific).^[2] In 2011, Intel released the 7-series [Panther Point](#) chipsets with integrated USB 3.0 to complement Ivy Bridge.^[3]

Volume production of Ivy Bridge chips began in the third quarter of 2011.^[4] [Quad-core](#) and dual-core-mobile models launched on 29 April 2012 and 31 May 2012 respectively.^[5] Core i3 desktop processors, as well as the first 22 nm [Pentium](#), were announced and available the first week of September, 2012.^[6]

1 Overview

The Ivy Bridge CPU microarchitecture is a shrink from Sandy Bridge and remains largely unchanged. Like its predecessor, Sandy Bridge, Ivy Bridge was also primarily developed by Intel’s Israel branch, located in Haifa, Israel.^[7] Notable improvements include:^{[8][9]}

- 22 nm [Tri-gate transistor](#) (“3-D”) technology (up to 50% less power consumption at the same performance level as 2-D planar transistors).^[10]
- A new random number generator and the [RdRand](#) instruction,^[11] codenamed Bull Mountain.^[12]

2 Ivy Bridge features and performance

The mobile and desktop Ivy Bridge chips also include significant changes over Sandy Bridge:

- [F16C](#)^[13] (16-bit Floating-point conversion instructions).
- [RdRand](#) instruction (Intel Secure Key).^[14]
- [PCI Express 3.0](#) support (not on Core i3 and ULV processors).^[15]
- [Max CPU multiplier](#) of 63 (57 for Sandy Bridge).^[16]
- [RAM](#) support up to 2800 [MT/s](#) in 200 MHz increments.^[16]
- The built-in [GPU](#) has 6 or 16 execution units (EUs), compared to Sandy Bridge’s 6 or 12.^[17]
- [Intel HD Graphics](#) with [DirectX 11](#), [OpenGL 3.1](#), and [OpenCL 1.1](#) support. [OpenGL 4.0](#) is supported with 10.18.10.4425 [WHQL](#) drivers^{[18][19]} and later drivers.
- [DDR3L](#) and [configurable TDP](#) (cTDP) for mobile processors.^[20]
- Multiple [4K](#) video playback.
- [Intel Quick Sync Video](#) version 2.^[17]
- Up to three displays are supported (with some limitations: with chipset of 7-series and using two of them with DisplayPort or eDP).^[21]
- A 14- to 19-stage [instruction pipeline](#), depending on the [micro-operation cache](#) hit or miss.^[22]

2.1 Benchmark comparisons

Compared to its predecessor, Sandy Bridge:

- 3% to 6% increase in CPU performance when compared clock for clock^{[25][26]}
- 25% to 68% increase in integrated GPU performance.^[27]

2.2 Thermal performance and heat issues when overclocking

Ivy Bridge's temperatures are reportedly 10 °C higher compared to Sandy Bridge when a CPU is **overclocked**, even at default voltage setting.^[28] Impress PC Watch, a Japanese website, performed experiments that confirmed earlier speculations that this is because Intel used a poor quality (and perhaps lower cost) **thermal interface material** (thermal paste, or "TIM") between the chip and the **heat spreader**, instead of the **fluxless** solder of previous generations.^{[29][30][31]} The mobile Ivy Bridge processors are not affected by this issue because they do not use a heat spreader between the chip and cooling system.

Enthusiast reports describe the TIM used by Intel as low-quality,^[31] and not up to par for a "premium" CPU, with some speculation that this is by design to encourage sales of prior processors.^[29] Further analyses caution that the processor can be damaged or void its warranty if home users attempt to remedy the matter.^{[29][32]} The TIM has much lower **thermal conductivity**, causing heat to trap on the die.^[28] Experiments with replacing this TIM with a higher-quality one or other heat removal methods showed a substantial temperature drop, and improvements to the increased voltages and overclocking sustainable by Ivy Bridge chips.^{[29][33]}

Intel claims that the smaller die of Ivy Bridge and the related increase in thermal density is expected to result in higher temperatures when the CPU is overclocked; Intel also stated that this is as expected and will likely not improve in future revisions.^[34]

2.3 Models and steppings

All Ivy Bridge processors with one, two, or four cores report the same CUID model 0x000306A9, and are built in four different configurations differing in the number of cores, L3 cache and GPU execution units.

3 Ivy Bridge-E/EN/EP/EX features

Ivy Bridge-E family is the follow-up to **Sandy Bridge-E**, using the same CPU core as the Ivy Bridge processor, but in **LGA 2011**, **LGA 1356** and **LGA 2011-1**^[39] packages for workstations and servers.

- Dual memory controllers for Ivy Bridge-EP and Ivy Bridge-EX^[40]
- Up to 12 CPU cores and 30 MB of L3 cache for Ivy Bridge-EP^[40]
- Up to 15 CPU cores and 37.5 MB L3 cache for Ivy Bridge-EX^[41] (released on 18 February 2014 as Xeon E7 v2^[42])
- Thermal design power between 50 W and 155 W^[43]
- Support for up to eight **DIMMs** of DDR3-1866 memory per socket, with reductions in memory speed depending on the number of DIMMs per **channel**^{[44][45][46]}
- No integrated GPU
- Ivy Bridge-EP introduced new hardware support for interrupt virtualization, branded as **APICv**.^{[47][48]}

3.1 Models and steppings

The Ivy Bridge-E family is made in three different versions, by number of cores, and for three market segments: the basic Ivy Bridge-E is a single-socket processor sold as Core i7-49xx and is only available in the six-core **S1 stepping**, with some versions limited to four active cores.

Ivy Bridge-EN (Xeon E5-14xx v2 and Xeon E5-24xx v2) is the model for single- and dual-socket servers using LGA 1356 with up to 10 cores, while Ivy Bridge-EP (Xeon E5-16xx v2, Xeon E5-26xx v2 and Xeon E5-46xx v2) scales up to four LGA 2011 sockets and up to 12 cores per chip.

There are in fact three die "flavors" for the Ivy Bridge-EP, meaning that they are manufactured and organized differently, according to the number of cores an Ivy Bridge-EP CPU includes:^[49]

- The largest is an up-to-12-core die organized as three four-core columns with up to 30 MB L3 cache in two banks between the cores; these cores are linked by three rings of interconnects.
- The intermediate is an up-to-10-core die organized as two five-core columns with up to 25 MB L3 cache in a single bank between the cores; the cores are linked by two rings of interconnects.
- The smallest is an up-to-six-core die organized as two three-core columns with up to 15 MB L3 cache in a single bank between the cores; the cores are linked by two rings of interconnects.

Ivy Bridge-EX has up to 15 cores and scales to 8 sockets. The 15-core die is organized into three columns of five cores, with three interconnect rings connecting two columns per ring; each five-core column has a separate

L3 cache.^[50] The processor is supposed to have a new “Run Sure” technology, speculated by the odd number of cores to involve keeping one in reserve.^[51]

4 List of Ivy Bridge processors

Processors featuring Intel’s HD 4000 graphics (or HD P4000 for Xeon) are set in **bold**. Other processors feature HD 2500 graphics unless indicated by N/A.

4.1 Desktop processors

List of announced desktop processors, as follows:

1. Requires a compatible motherboard.

Suffixes to denote:

- K – Unlocked (adjustable CPU multiplier up to 63 bins)
- S – Performance-optimized lifestyle (low power with 65 W TDP)
- T – Power-optimized lifestyle (ultra low power with 35–45 W TDP)
- P – No on-die video chipset
- X – Extreme performance (adjustable CPU ratio with no ratio limit)

4.2 Server processors

Additional high-end server processors based on the Ivy Bridge architecture, code named Ivytown, were announced September 10, 2013 at the **Intel Developer Forum**, after the usual one year interval between consumer and server product releases.^{[55][56][57]}

The Ivy Bridge-EP processor line announced in September 2013 has up to 12 cores and 30 MB third level cache, with rumors of Ivy Bridge-EX up to 15 cores and an increased third level cache of up to 37.5 MB,^{[58][59]} although an early leaked lineup of Ivy Bridge-E included processors with a maximum of 6 cores.^[60]

Both Core-i7 and Xeon versions are produced: the Xeon versions marketed as **Xeon E5-1400 V2** act as drop-in replacements for the existing Sandy Bridge-EN based Xeon E5, **Xeon E5-2600 V2** versions act as drop-in replacements for the existing Sandy Bridge-EP based Xeon E5, while Core-i7 versions designated i7-4820K, i7-4930K and i7-4960X were released on 10 September 2013, remaining compatible with the X79 and LGA 2011 hardware.^{[59][61]}

For the intermediate **LGA 1356** socket, Intel launched the **Xeon E5-2400 V2** (codenamed Ivy Bridge-EN) series in January 2014.^[62] These have up to 10 cores.^[63]

A new Ivy Bridge-EX line marketed as **Xeon E7 V2** had no corresponding predecessor using the Sandy Bridge microarchitecture but instead followed the older **Westmere-EX** processors.

1. Requires a compatible motherboard.

4.3 Mobile processors

Suffixes to denote:

- M – Mobile processor
- Q – Quad-core
- U – Ultra-low power
- X – “Extreme”
- Y – Extreme ultra-low power

5 Roadmap

Intel demonstrated the **Haswell** architecture in September 2011, which began release in 2013 as the successor to **Sandy Bridge** and **Ivy Bridge**.^[66]

6 See also

- **List of Intel CPU microarchitectures**

7 Notes

- [1] Transistor counts for M-2, H-2 and HM-4 were determined by a comparison of transistor counts in Sandy Bridge and HE-4. Performing a comparative analysis gave counts of 108 million transistors per core, 67 million transistors per 1 MB of L3 cache, 88 million transistors for the memory controller and other chip features, and roughly 21 million transistors for each execution unit inside the Intel HD 4000. All this is an attempt to determine the transistor count mathematically, and is not backed by any sources. Thus, these transistor counts may be inaccurate.

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