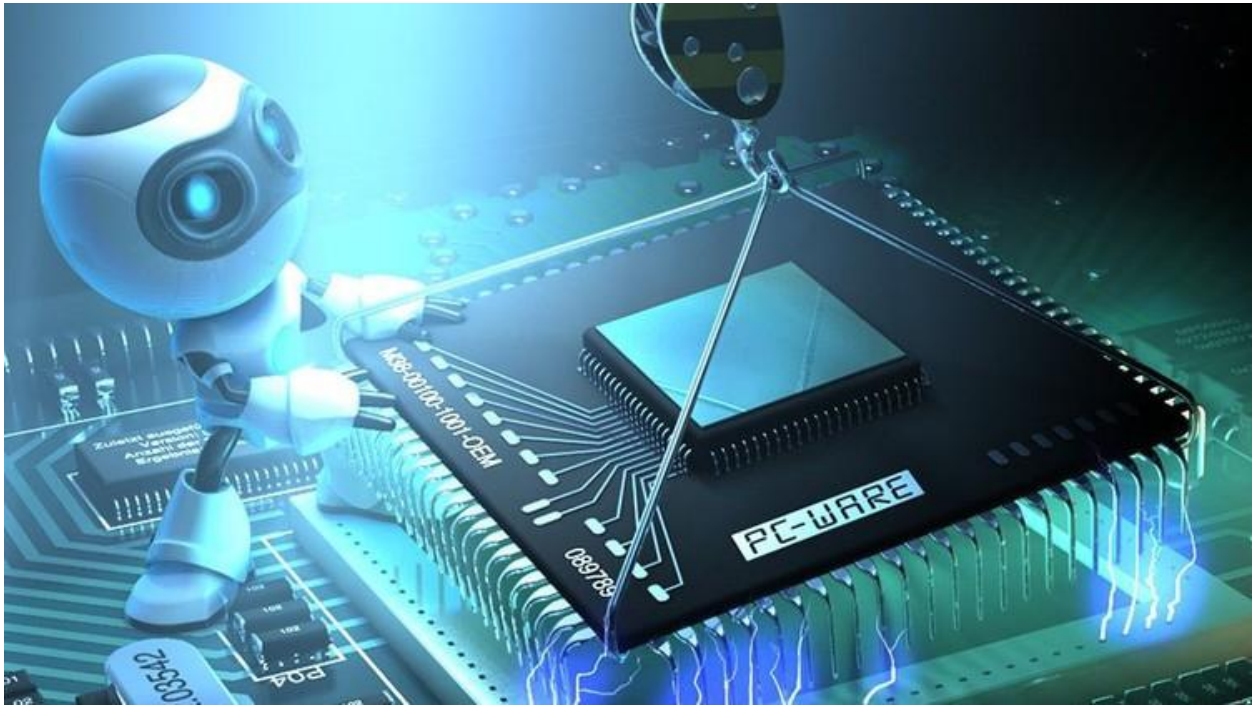
Flags and Sequencing Instructions



Condition Codes (FLAGS)

- Implicitly activated after executing any arithmetic instruction
- Stored in a special register (32 bits) of the processor: **EFLAGS**

Condition Codes (FLAGS)

ADDL op1, op2 ; **op2 ← op2 + op1**

- **CF (Carry Flag): Carry of bit 31 of the sum.**
- **ZF (Zero Flag): ZF = 1 if t == 0**
- **SF (Sign Flag): SF = 1 if t < 0**
- **OF (Overflow Flag): OF = 1 if**

  (op2>0 && op1>0 && op2+op1<0) || (op2<0 && op1<0 && op2+op1>0)

CMP Instruction and FLAGS

CMPL op1, op2 ; op2 - op1 and flags are activated

- **CF (Carry Flag): Carry of most significant bit of the subtraction.**
- **ZF (Zero Flag): ZF = 1 if op2 == op1**
- **SF (Sign Flag): SF = 1 if (op2 - op1) < 0 → (op2 < op1)**
- **OF (Overflow Flag): OF = 1 if**

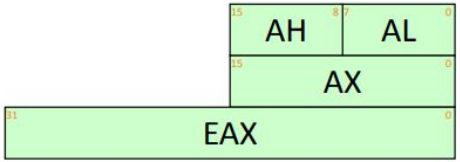
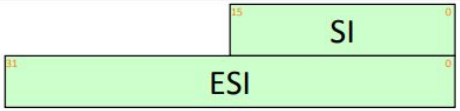
  (op2>0 && op1<0 && op2-op1<0) || (op2<0 && op1>0 && op2-op1>0)

Flags and Sequencing Instructions

Instructions	Flags	Description
JE etiq	ZF	Equal / Zero
JNE etiq	~ZF	Non-equal / Non-zero
JS etiq	SF	Negative
JNS etiq	~SF	Non-negative
JG etiq	~(SF^OF)&~ZF	Greater (with sign)
JGE etiq	~(SF^OF)	Greater or equal (with sign)
JL etiq	(SF^OF)	Less (with sign)
JLE etic	(SF^OF)|ZF	Less or equal (with sign)
JA etiq	~CF&~ZF	Greater (without sign)
JAE etiq	~CF	Greater or equal (without sign)
JB etiq	CF	Less (without sign)
JBE etiq	CF^ZF	Less or equal (without sign)

Programmer Vision

Available registers

32 bits	16 bits	8 bits	
%eax	%ax	%ah,%al	
%ebx	%bx	%bh,%bl	
%ecx	%cx	%ch,%cl	
%edx	%dx	%dh,%dl	
%esi	%si		
%edi	%di		
%esp	%sp		Reserved for specific use of subroutines
%ebp	%bp		
%eip			Program counter
%eflags			Status word