MIDWESTERN STATE UNIVERSITY

DEPARTMENT OF COMPUTER SCIENCE
CMPS 3023: Logic Design
Fall semester 2025

Project Assignment
Due: 11/27/2025

This project is to be performed either individually or by a group of at most 3 students. Use the VHDL compiler or the graphical designer and simulator to design an application specific integrated circuit that implements the newest element of the x86 family, the 7986 (almost 8086) microprocessor in accordance with the specifications below.

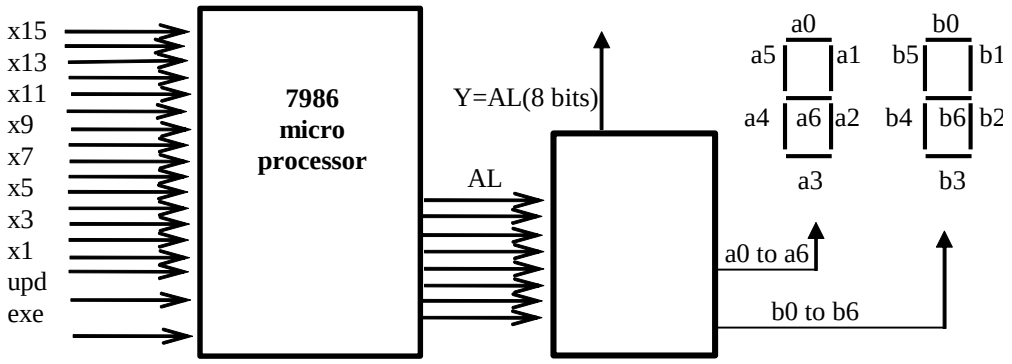
For this project, you are to complete the design (using VHDL and components design or schematics capture) and the simulation of an 8-bit processor, which includes four registers AL, BL, CL and DL, and will execute the instruction set shown on table 1.

Table 1. 7986 Instruction set

Mnemonic	**Action**	
ADD R1,R2	Add reg2 to reg1	0000 0000 11 reg2 reg1
XOR R1,R2	Xor reg2 to reg1	0011 0000 11 reg2 reg1
MOV R1,R2	Copy reg2 to reg1	1000 1000 11 reg2 reg1
MOV R,imm	Copy immdata to reg	1011 0 reg immdata
OR AL,imm	OR AL with immdata	0000 1100 immdata
AND AL,imm	AND AL with immda	0010 0100 immdata
SHL R,1	Shirt Left reg by 1	1101 0000 1110 0 reg
SHR R,1	Shift Right reg by 1	1101 0000 1110 1 reg
NEG R	Change reg sign (2's compl)	1111 0110 1101 1 reg
OUT R	Displays contents of reg	1110 0110 1100 0 reg

AL = 000, BL = 011, CL= 001, DL= 010

The block diagram of the 7986 processor is shown on Figure 1. The machine has 18 input signals and 22 output signals. The 18 input signals consist of 16 bits used for instructions and 2 extra bits used to clock the operations: one clock signal will command the execution of the operation (EXE) and the other will update the destination register (UPD) (these two bits cannot be zero at the same time). From the 22 output signals, 14 output bits are connected to two seven-segment displays and should show the value contained in AL (in hexadecimal format), except when instructed to do it differently by the instruction OUT. The remaining 8 signals are the binary value in AL or whatever register being displayed.



VERY IMPORTANT:

1. Clock signals activate circuit components when they are zero.
2. 7-segment lights go ON when their signal is zero (OFF when it is one)

Project report:

Use Quartus, computer word processing and drawing tools of your choice to generate your results. It must consist of the following items:

1. Block diagram of the circuit implementation (show major components like registers, logic units, multiplexers, connections, etc.).

2. Printout of the circuit schematics or VHDL code used to implement the design.

3. Electronic copy of the .vhd or the .bdf file required to run the simulation (uploaded to D2L).

4. Brief description of the experiment with the simulation (which instructions and output images).

Your project is due on November 27, 2025. You need to start working NOW!!!! Anything that you try to do in the last week before the due date will not work for sure. Time is an important factor in this project. **If you write your solution in VHDL and the entire solution has less than 3 entities described, then your maximum grade is 50.** If your project does not work or you cannot justify why it does not work, then your grade will be zero. Acceptable justifications are based on software limitations only, and in this case you must show you had every component defined and tested and only the integration failed. Failure in reporting the simulation will reduce your grade by 40 points. **NO EXTENSIONS!!**