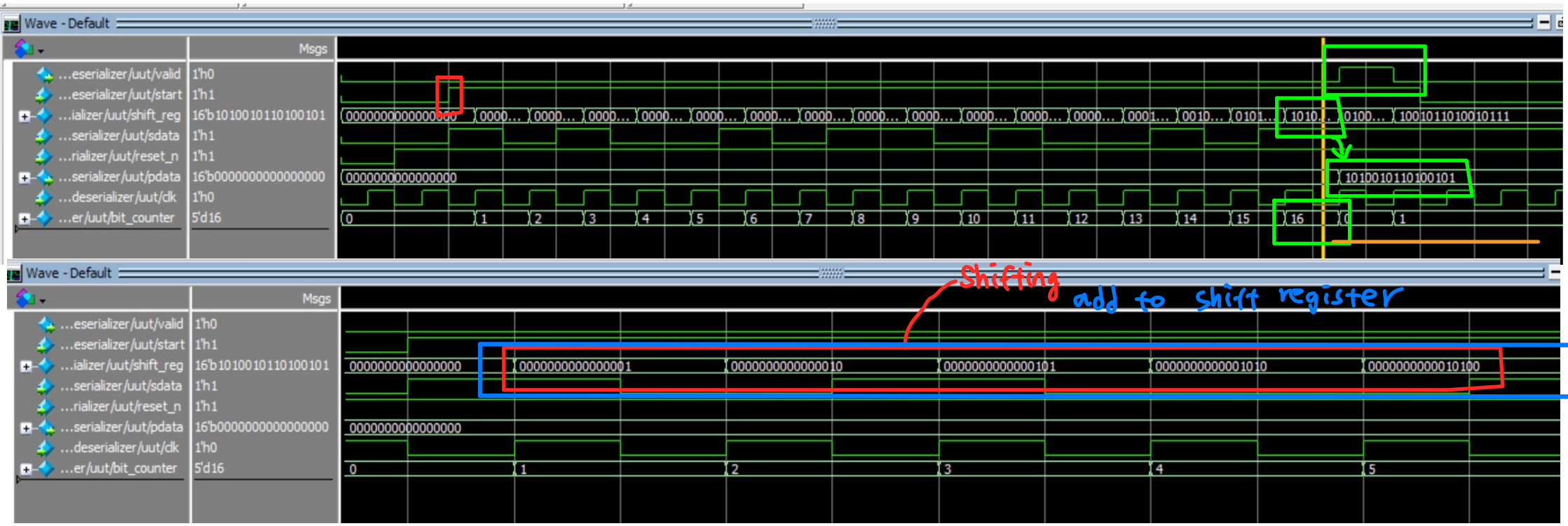

Testcase: 1010 0101 1010 0101

clk: The clock signal used to synchronize the deserialization process.
reset_n: Active-low reset signal to initialize the module.
sdata: The serial data input.
start: A control signal to begin deserialization.
pdata: The 16-bit parallel data output.
valid: A signal that indicates when the parallel data is ready.

How It Works:

1. When the start signal is asserted, the Deserializer begins shifting in serial data (sdata) into the shift_reg.
2. The shift_reg accumulates the incoming serial data, with each bit shifting into the register on each clock cycle.
3. Once 16 bits have been received (indicated by bit_counter reaching 16), the parallel data (pdata) is output from the shift_reg, and the valid signal is asserted to indicate that the data is ready.
4. The bit_counter resets, and the module is ready to start deserializing the next serial data stream.