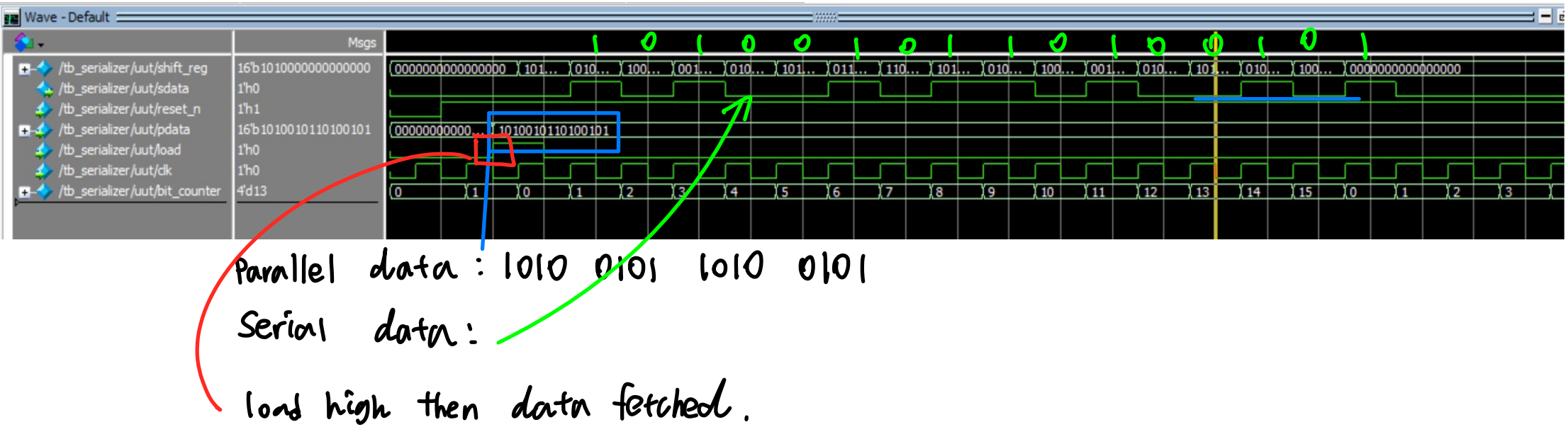

clk: The clock signal used to synchronize the serialization process.
reset_n: Active-low reset signal to initialize the module.
pdata: The 16-bit parallel data input.
load: A control signal to load the parallel data into the shift register.
sdata: The serialized output data.

How It Works:
When the load signal is asserted, the parallel data (pdata) is loaded into the shift_reg.

The shift register then shifts the data left on each clock cycle, outputting the most significant bit (MSB) first through sdata.

The bit_counter tracks the position of the bits being serialized and stops the process once all bits are transmitted.