UCI
EECS 119
Project # 4
Design of 4-bit Binary Up/Down Counter Prepared by

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Introduction:

The objective of this project is to design, implement, and verify a complete 4-bit synchronous up/down counter using CMOS technology. The work begins at the fundamental building-block level by designing a transistor-level JK flip-flop, constructing its schematic, generating a corresponding layout, and validating correctness through DRC, LVS, and post-layout parasitic simulations. Once the JK flip-flop cell is verified, it is instantiated hierarchically to form the sequential stages of a 4-bit counter, integrated with the necessary combinational gating to support both counting directions. The project emphasizes the full custom design flow—including schematic capture, layout creation following design rules, hierarchical cell integration, and electrical verification—as well as functional validation through transient simulations that demonstrate up-counting, down-counting, and correct response to control inputs. This laboratory reinforces concepts in CMOS logic design, sequential circuit behavior, transistor-level implementation of memory elements, and the practical considerations required to produce a reliable multi-bit digital system.

Theory:

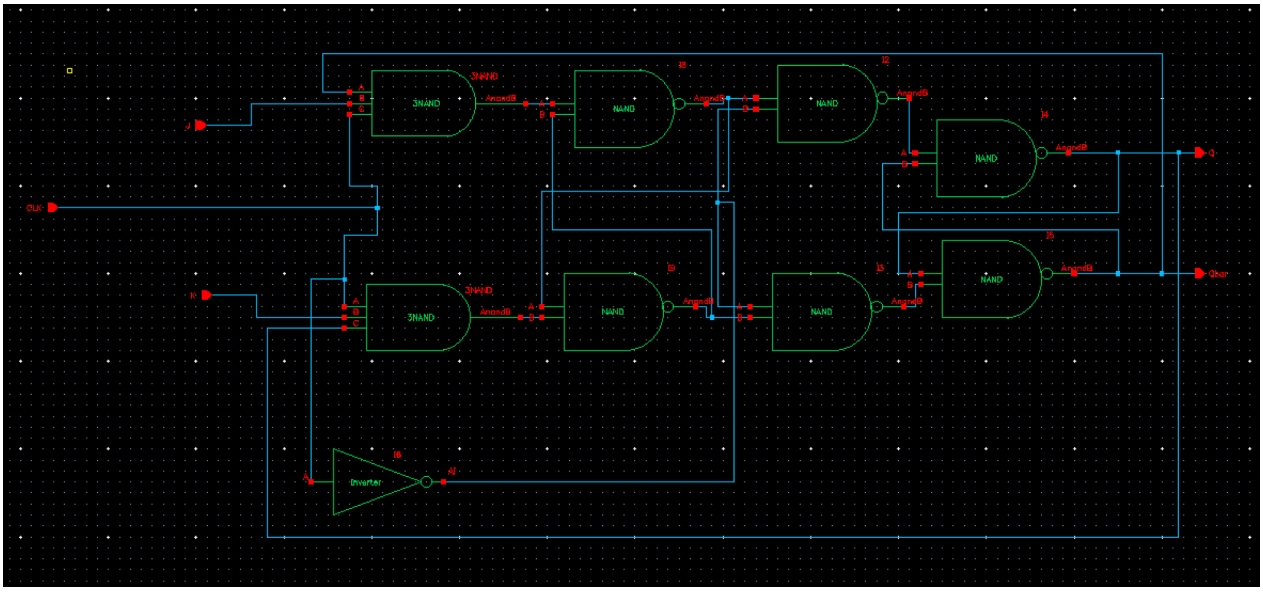
A JK flip-flop is a fundamental CMOS sequential element that stores one bit of state and updates its output on a clock edge. In CMOS, each gate consists of complementary PMOS pull-up and NMOS pull-down networks, providing full logic swing and low static power. A master–slave arrangement ensures edge-triggered operation by allowing one latch to update while the other is isolated.

A 4-bit synchronous up/down counter is formed by cascading four JK flip-flops, where each stage toggles when all lower-order bits satisfy J = K = 1. Additional gating controlled by an Up/Down signal determines whether toggle conditions propagate in the count-up or count-down direction. Because all flip-flops share the same clock, the design avoids ripple delays and ensures clean, glitch-free transitions. At the transistor level, propagation delay and switching behavior are influenced by NAND gate depth and parasitic interconnect capacitances, but the overall counting sequence remains stable and predictable. This combination of CMOS flip-flops and minimal combinational logic yields a reliable binary counter suitable for hierarchical digital design.

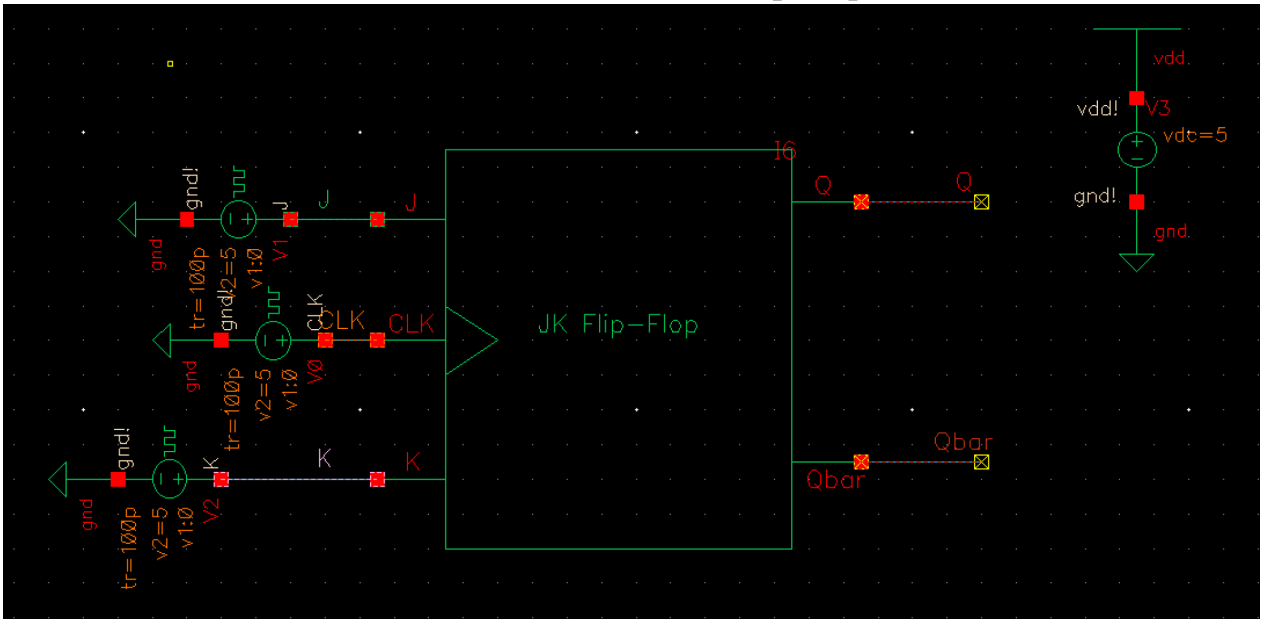
Design: (Simulation Layout Questions)

1. A.

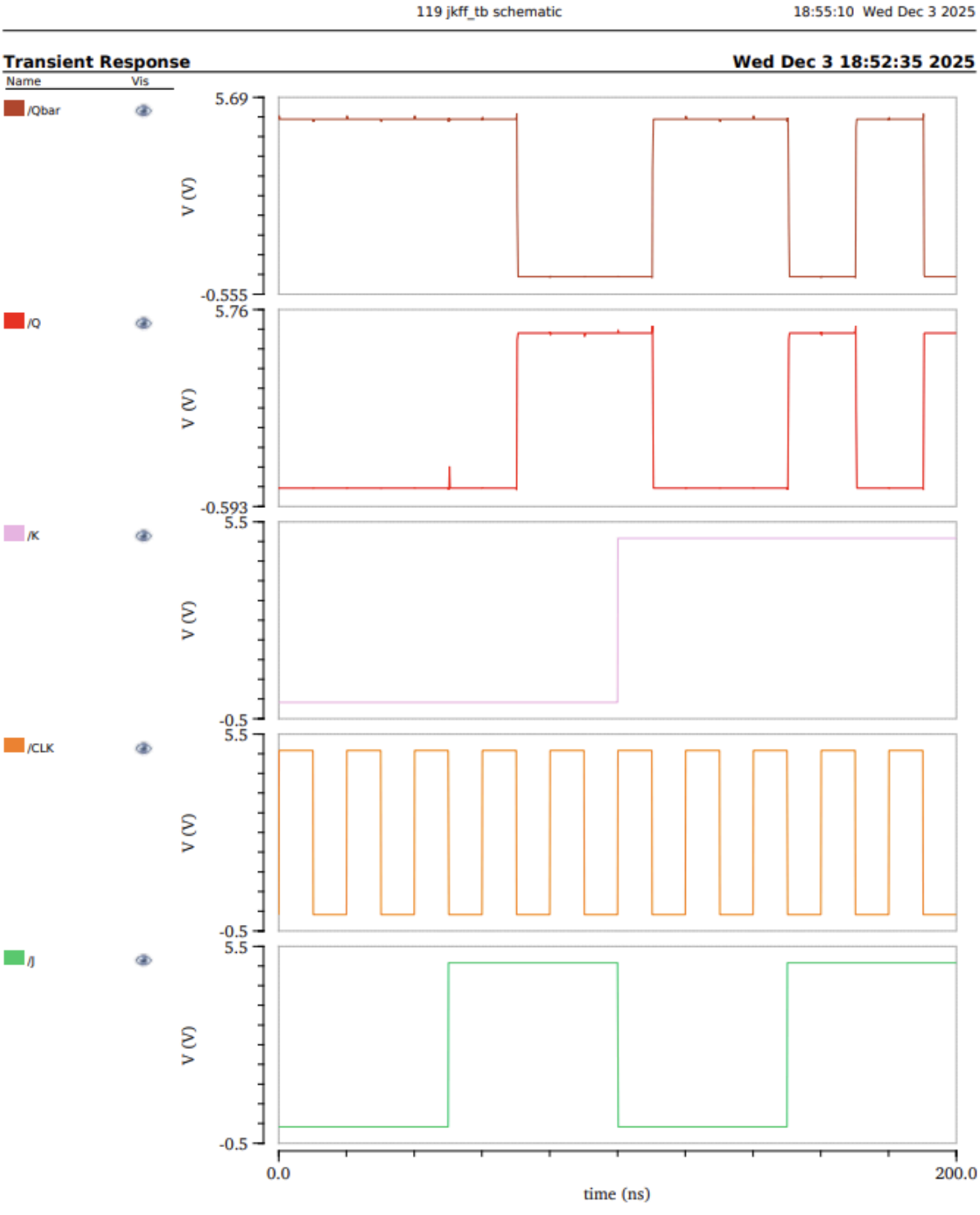
Circuit Schematic



Circuit Schematic of JK Flip-Flop

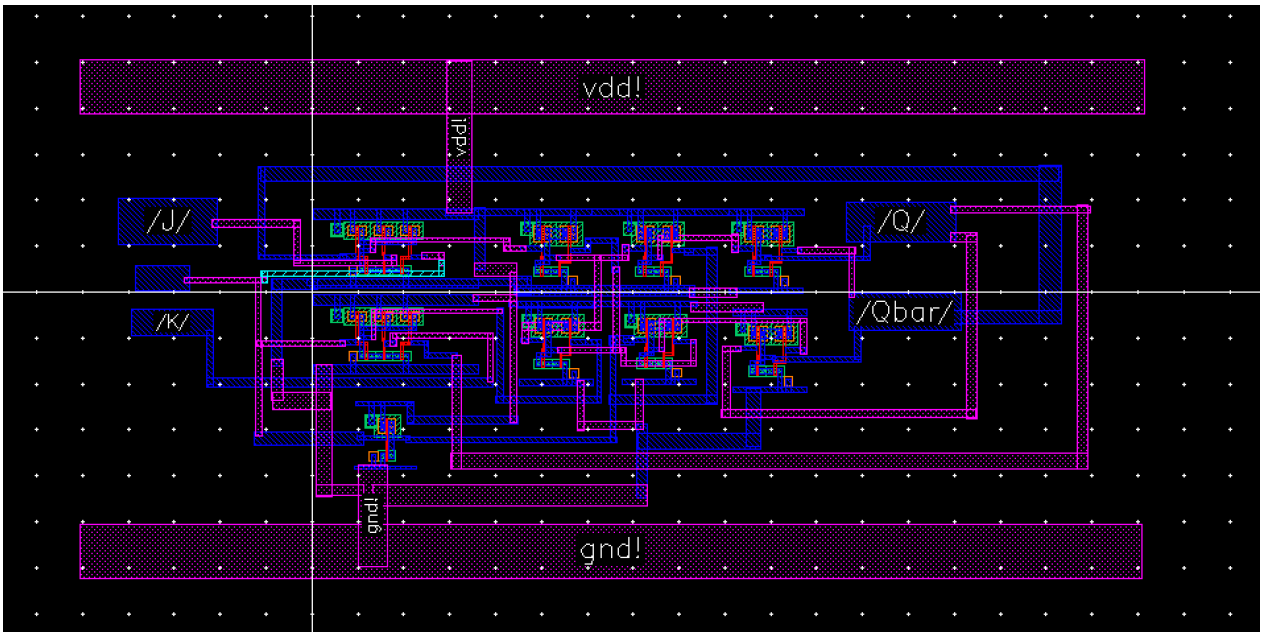


JK Flip-Flop Symbol & Test Bench Schematic

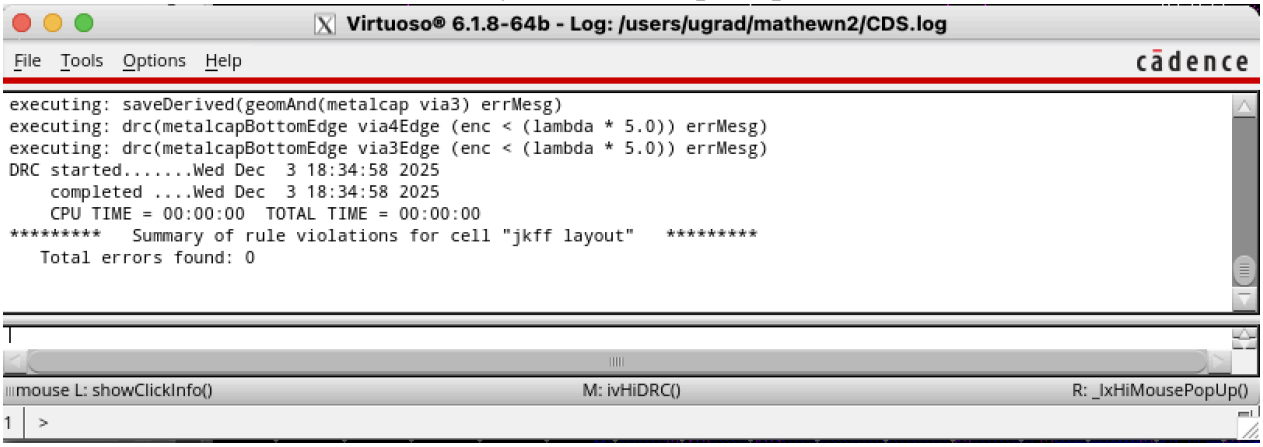


Output Waveform

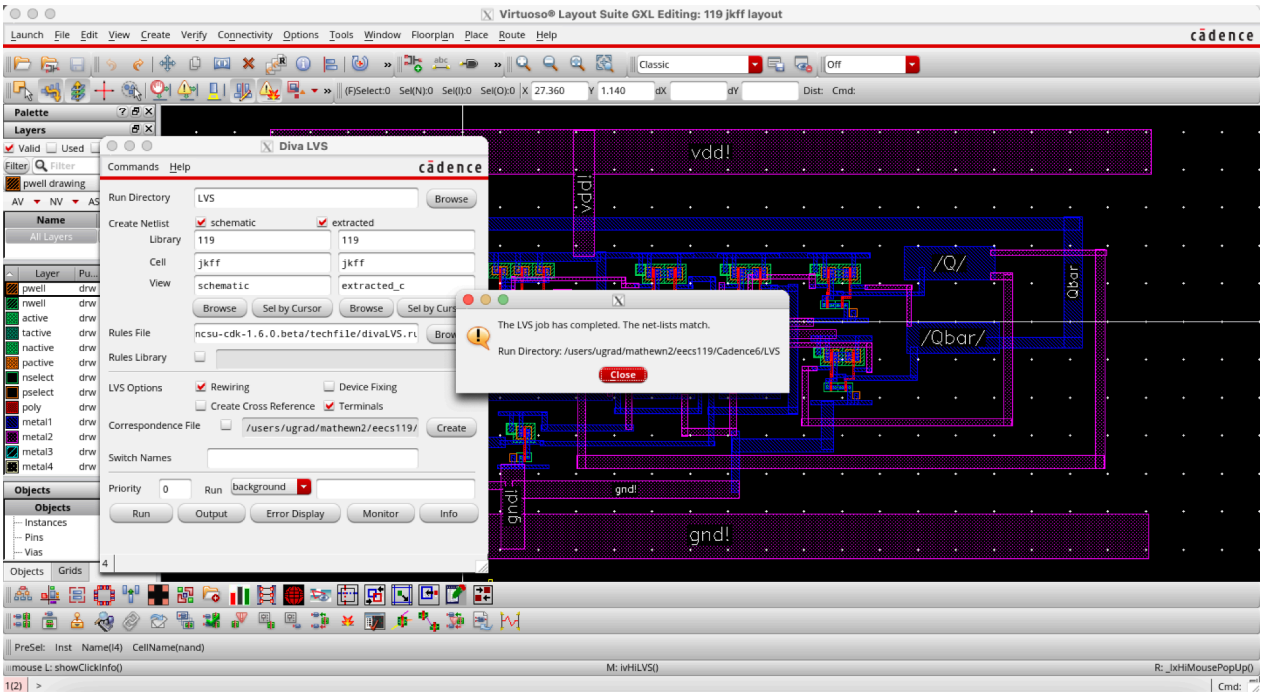
B.



Layout of JK Flip-Flop

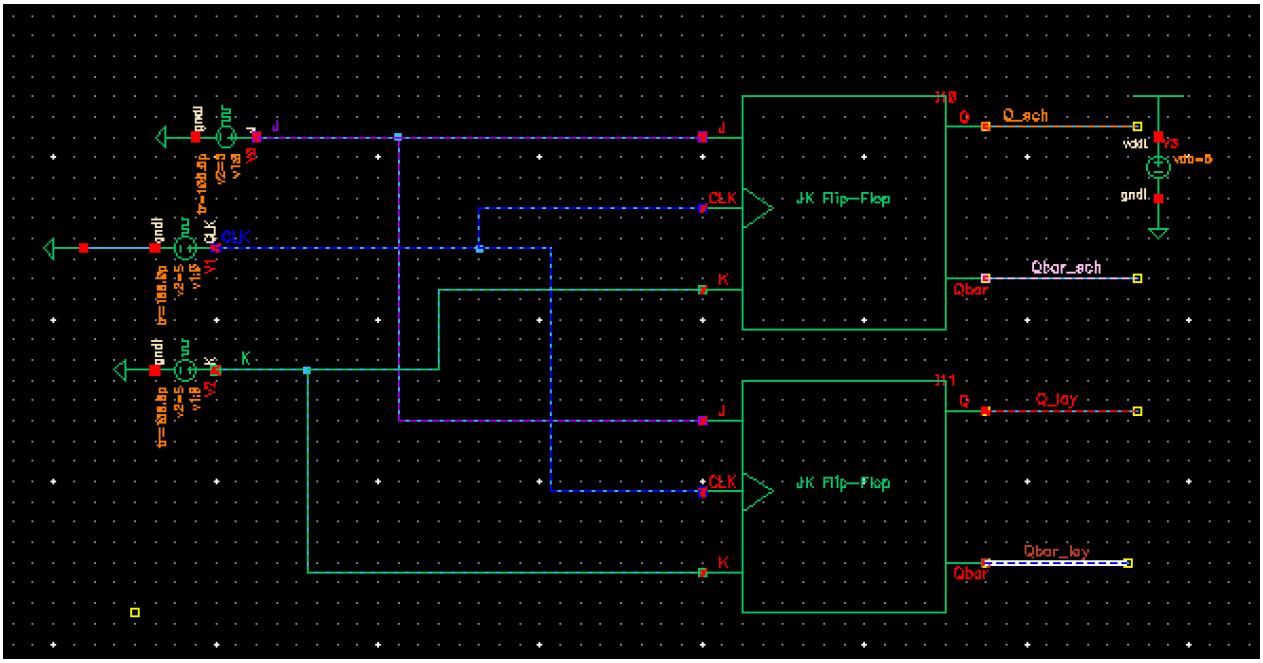


DRC of JK Flip-Flop

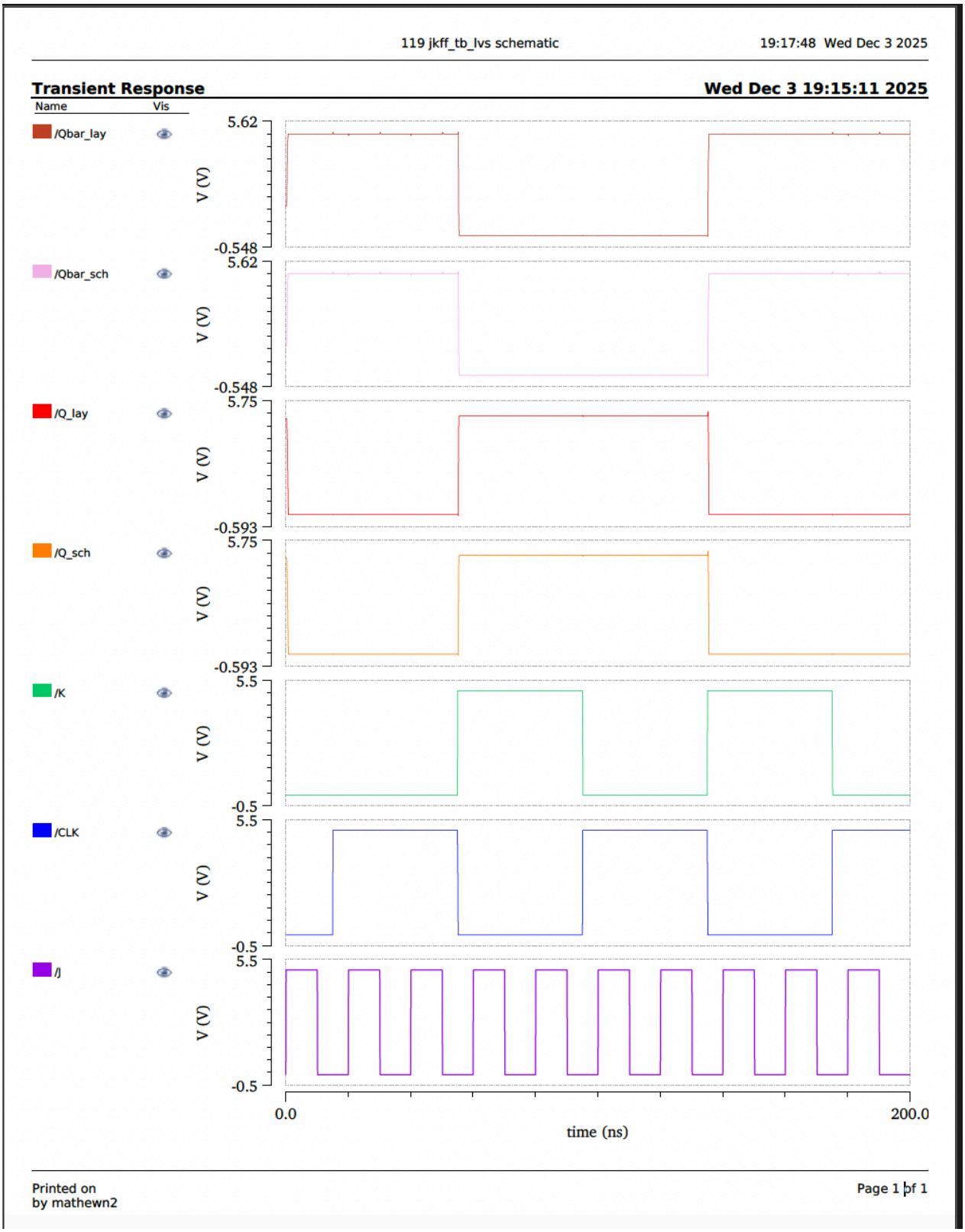


LVS of JK Flip-Flop

C.

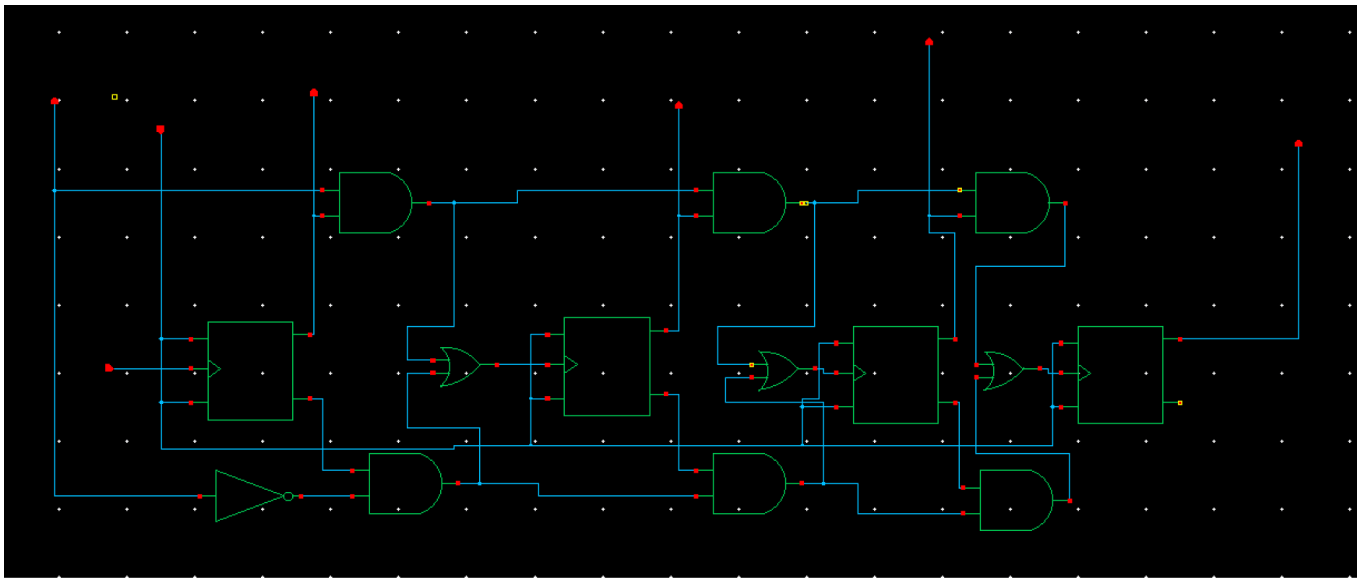


JK Flip-Flop Parasitic Capacitance Schematic

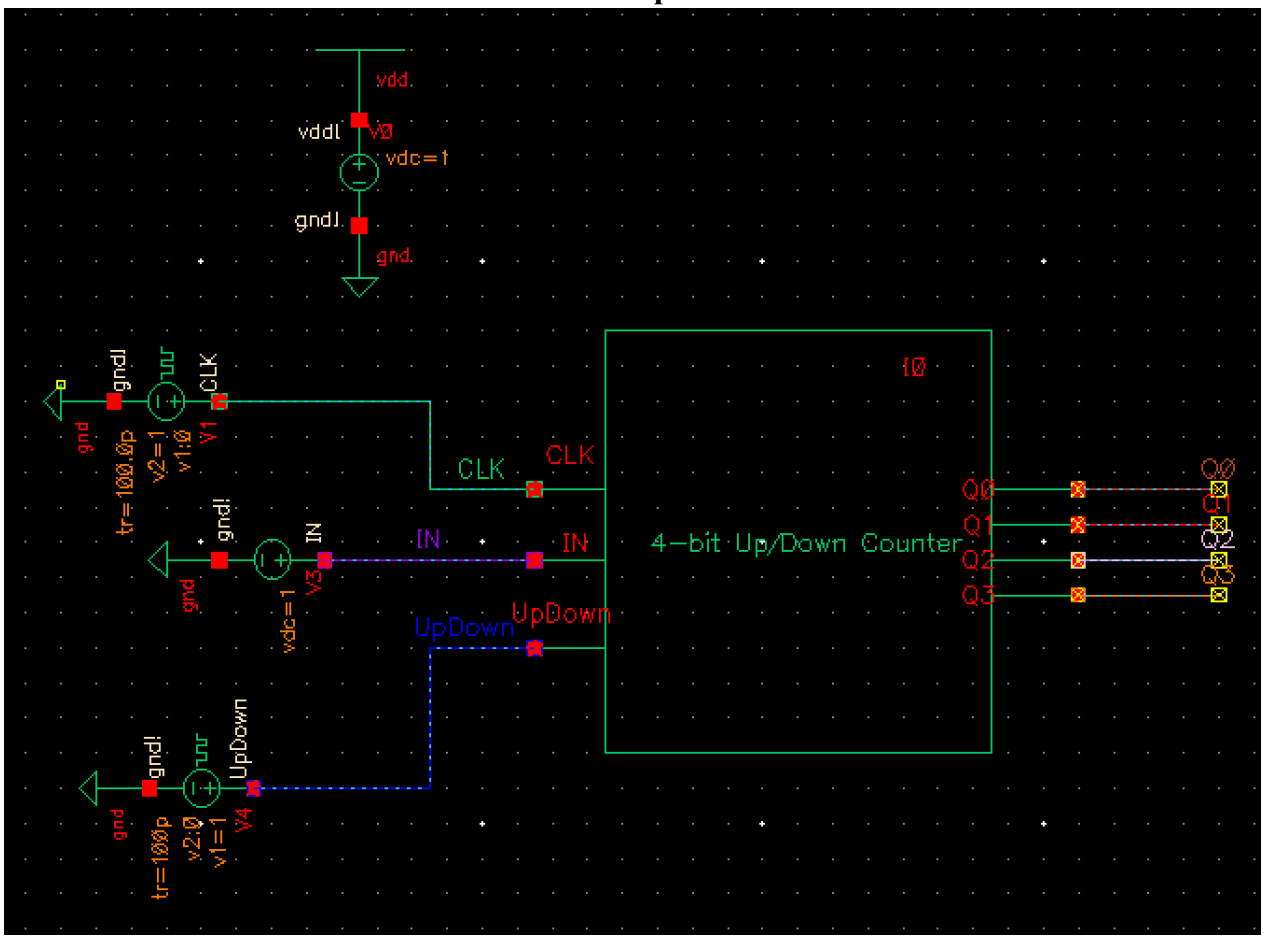


Layout and Schematic look similar

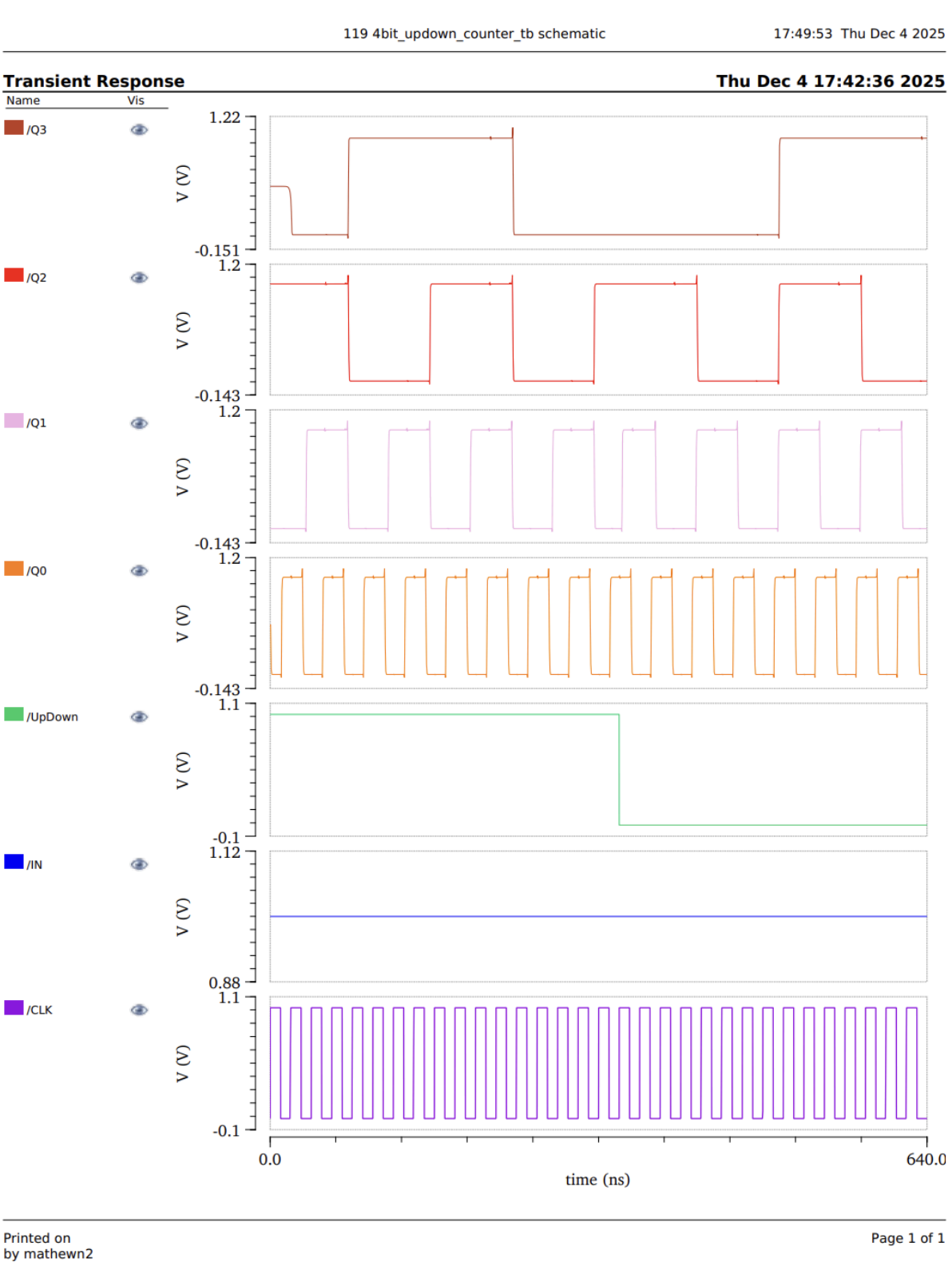
D.



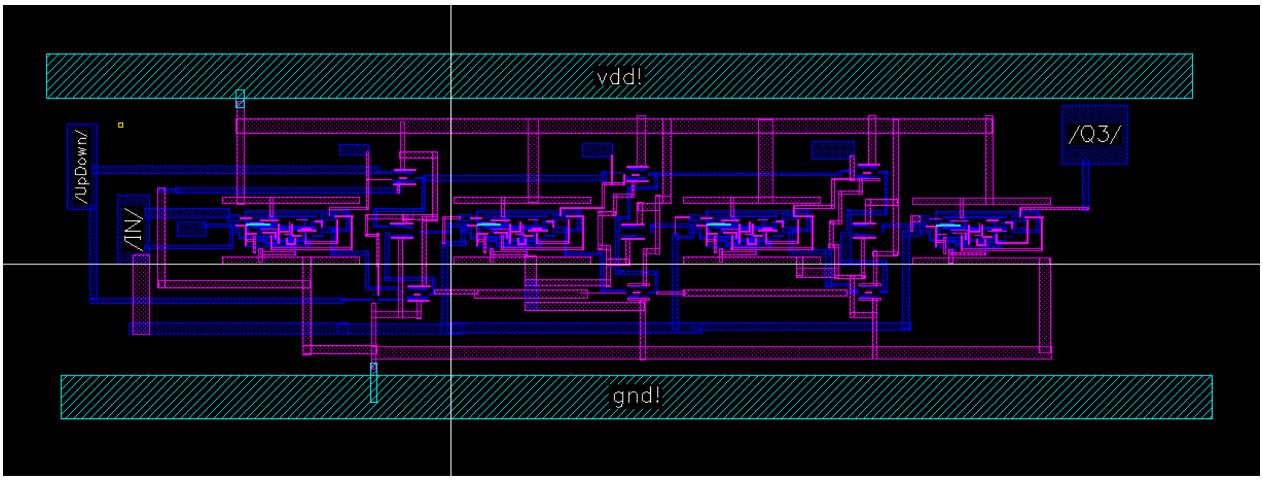
Schematic of 4-bit Up/Down Counter



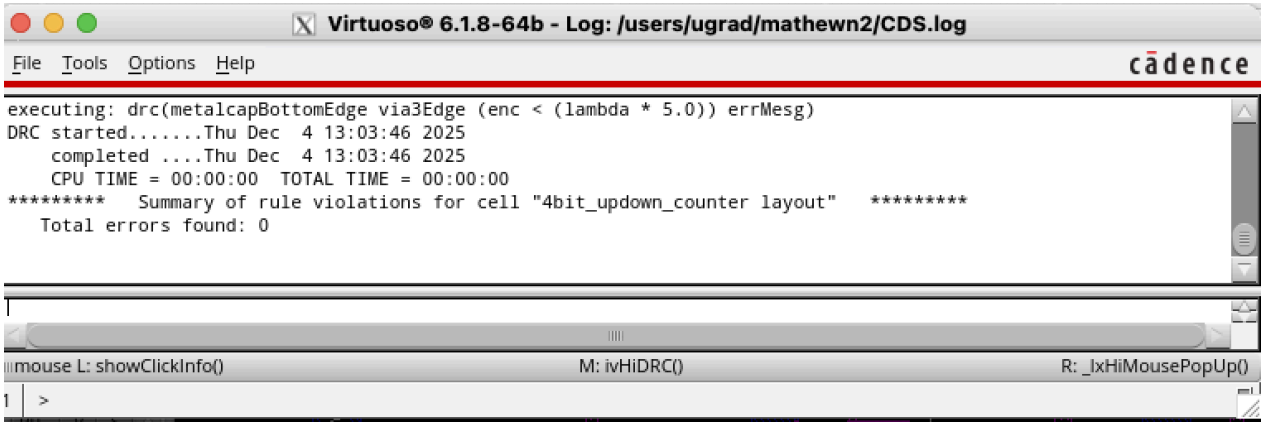
Symbol and Testbench for 4-bit Up/Down Counter



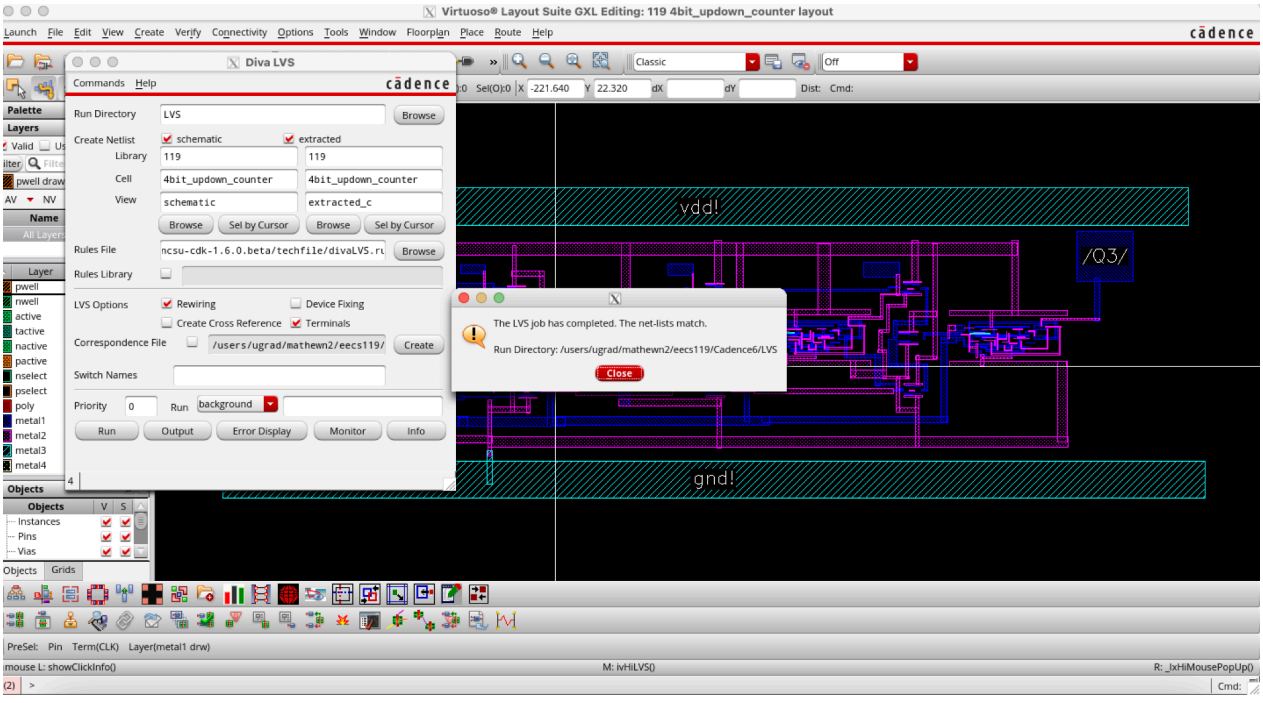
Waveform of 4-bit UpDown, 20ns change-of-state. Starts at initial value 1101 (13) at t=0



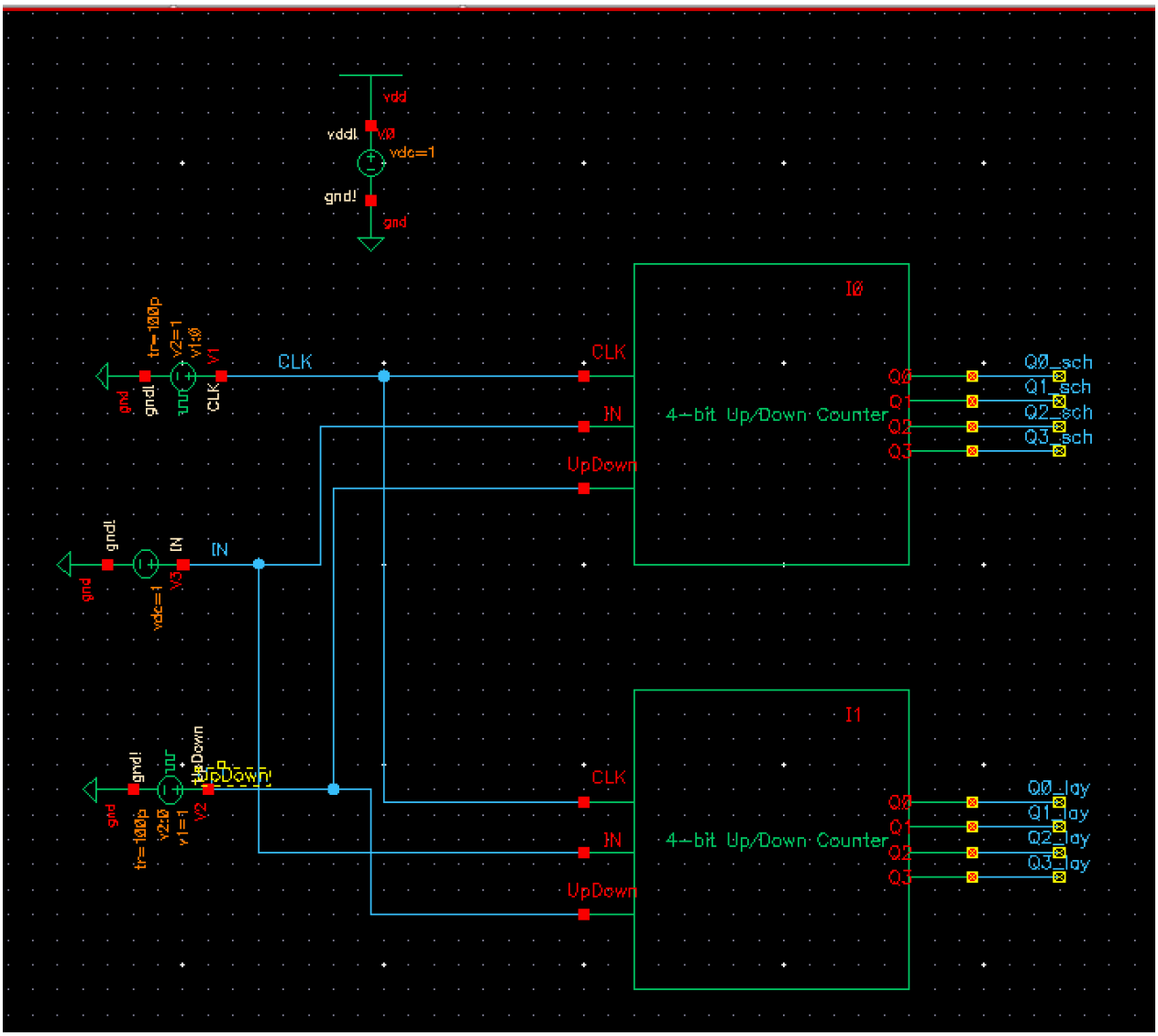
Layout of 4-bit Up/Down Counter



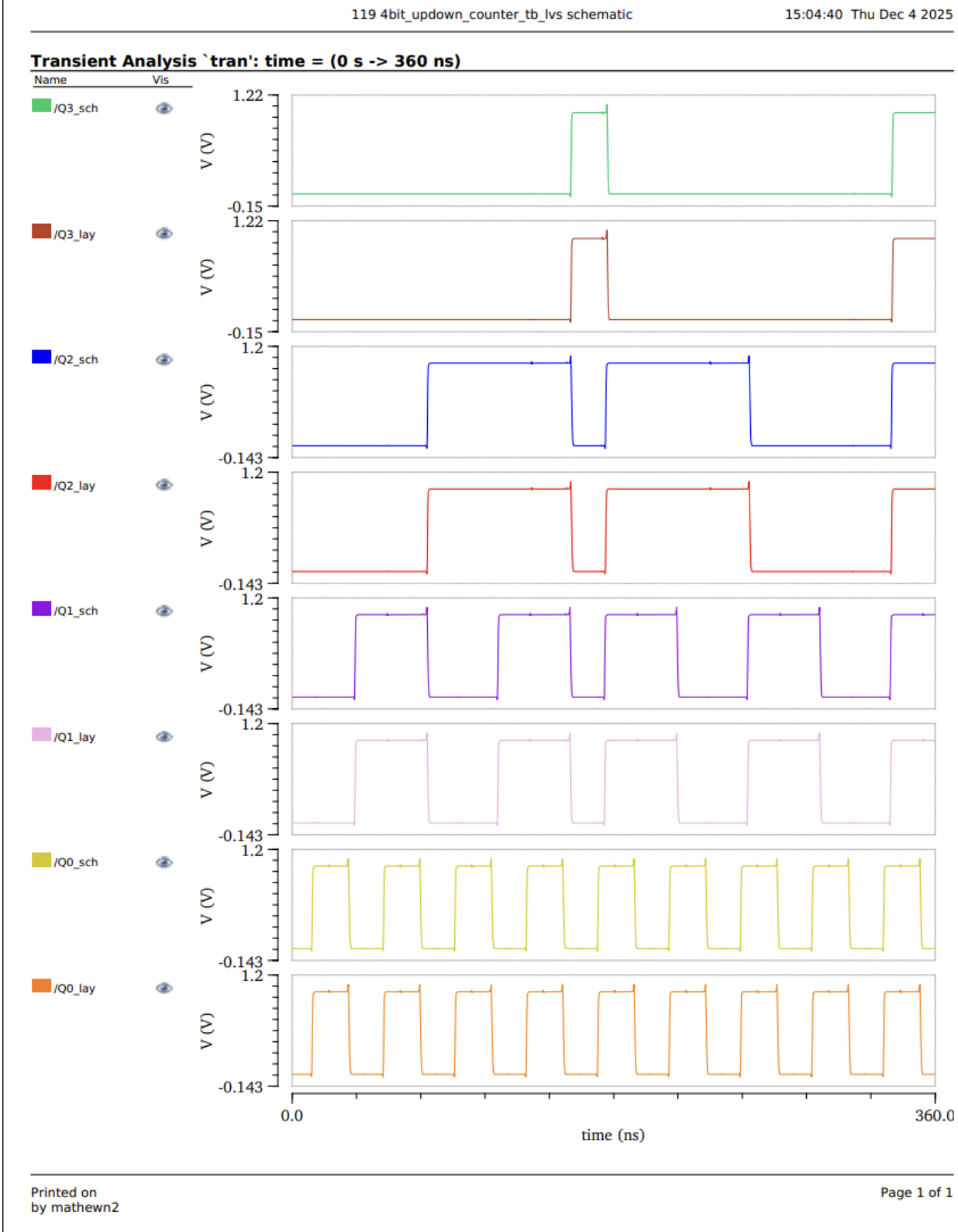
No DRC Errors



LVS Matches



Layout vs Schematic Parasitic Testbench Schematic



Layout and Schematic Output Matches

Conclusion:

In this project, we extended the CMOS design workflow to the implementation of sequential logic by constructing, simulating, and verifying a transistor-level JK flip-flop and a hierarchical 4-bit synchronous up/down counter. By first designing and LVS-verifying the NAND-based master–slave JK flip-flop, we established a robust sequential building block that reliably toggles, sets, and resets in response to clocked inputs. Integrating four of these flip-flops with the necessary gating logic demonstrated how synchronous counters propagate toggle conditions across multiple stages and how direction control can be implemented through simple combinational networks. Through layout generation, DRC correction, and careful resolution of LVS mismatches, we gained practical experience managing metal routing, via placement, power distribution, and the importance of maintaining clean net connectivity. Post-layout simulations highlighted the effects of parasitic capacitances and interconnect delays on timing behavior, providing insight into how physical design decisions influence real circuit performance. Overall, this project reinforced the connection between transistor-level CMOS implementation and higher-level digital system behavior, illustrating how well-designed sequential elements form the foundation of larger synchronous architectures.

Bibliography:

[1] R. Jacob Baker (2019), *CMOS: Circuit Design, Layout, and Simulation*, 4th Edition, Wiley-IEEE Press.

[2] Adel S. Sedra and Kenneth C. Smith (2020), *Microelectronic Circuits*, 8th Edition, Oxford University Press.