Introduction to Digital Logic Design Lab
EECS 31L

Lab #5 : RISC-V Single Cycle Processor

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1 Objective

In this lab, we are to complete the design of the RISC-V Single Cycle Processor. As in our previous lab, we were to complete the Datapath design, which consists of the FlipFlop, ALU, RegFile, and several other components. We are to now implement the DataPath along with two other lower level modules: Controller and ALU Controller, and a higher level module: Processor.

2 Procedure

In this lab, I implemented the RISC-V Single Cycle by first, understanding how the modules correlate to each other, and then observing the diagram as seen below.

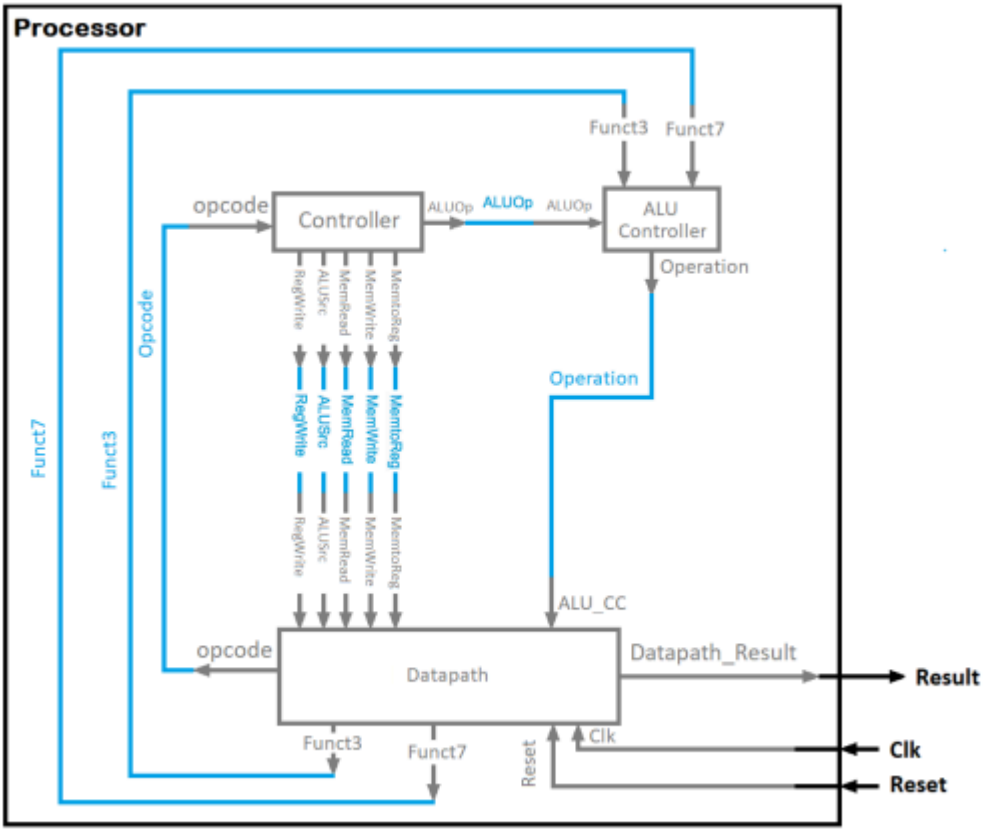


Figure 1 : Processor.

The Controller is one of the modules that handles the7-bits opcode input and outputs the RegWrite, ALUSrc, MemRead, MemWrite, MemtoReg, and the 2-bit ALUOp. The Controller determines the inputs of the Datapath. The ALUSrc and MemtoReg are used to control multiplexers in the Datapath. The RegWrite, MemRead, and MemWrite are use for controlling the reading and writing in the register file and data memory in the Datapath. The ALUOp is a 2-bit control signal for the ALUController. See the diagram below.

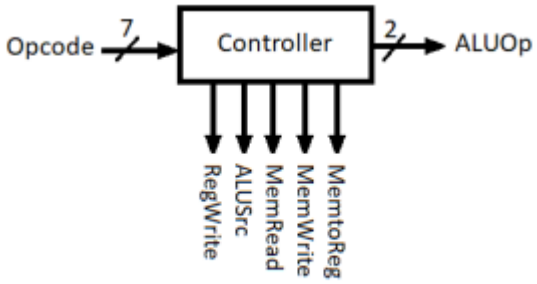


Figure 2 : Controller.

The ALUController has three inputs: ALUOp, Funct3, and Funct7. The ALUOp is a 2-bit input that comes from the Controller module. The Funct3 and Funct7 are 3-bit and 7-bit inputs, respectively, that come frmo the Datapath. The output of the ALUControler is the 4-bit Operation that essentially becomes an input for the Datapath. See the diagram below:

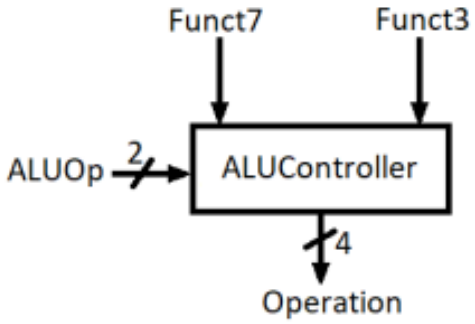


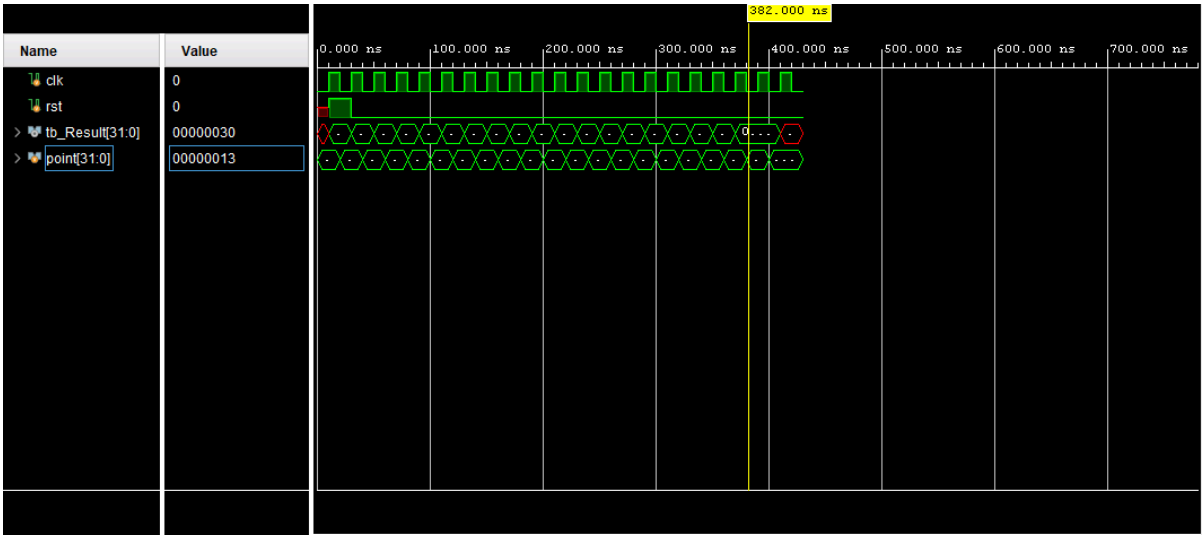
Figure 3 : ALUController.

The Datapath was designed in the previous Lab, and is a sub-module for our Processor. The Operation output from the ALUController serves as the input for the ALU_CC, for the Datapath. The outputs from the Controller excluding the ALUOp become inputs for the Datapath. The Datapath has a clk and reset. The Datapath outputs include Funct3, Funct7, Opcode, and the Datapath_Result. The Datapath_Result, is the result of our processor design. (Scroll above to the processor design to view the Datapath module.)

The higher level module, the Processor, combines the three sub-modules together as seen in the picture as provided earlier. The processor contains the Datapath, the Controller, and the ALUController. The Blue lines in the Processor design are the wires that are use for the designated modules here is my implementation of the wires:

```
wire RegWrite;
wire ALUSrc;
wire MemRead;
wire MemWrite;
wire MemtoReg;
wire [3:0] Operation;
wire [6:0] Opcode;
wire [6:0] Funct7;
wire [2:0] Funct3;
wire [1:0] ALUOp;
```

3 Simulation Results



In this lab, I have successfully implemented the design of the RISC-V Single Cycle Processor. Evidently, I passed all 20 test cases:

```
The number of correct test cases is:        20
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Back to the waveform, the above waveform can verify my design. The selected signal of the waveform is at 382 ns, which reverse to the test case 19, which at this specific time, the clock is low (i,e. clk = 0), and the reset signal is deactivated (i.e. rst = 0). The processor's result output (i.e. Result) is a value of 30 (i.e. 32'h000000030) which corresponds to the processor executing the SW instruction. The SW instruction stores a value from a register into memory at the address specified by the the immediate value which in this test case, the result being 30 suggests that the processor executed the SW instruction and stored 30 into memory successfully. When the condition is true, "point" increments which further suggests that the test case has passed hence this test case output the expected result at the time specified.