Introduction to Digital Logic Design Lab
EECS 31L

Lab #4 : RISC-V Single Cycle Processor

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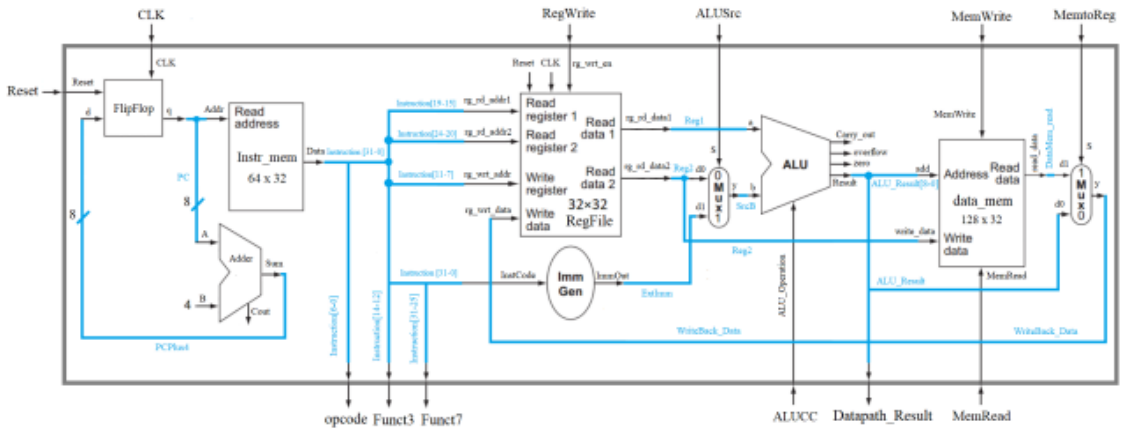
1 Objective

Give a brief summary or a high-level overview of the design. Use a block diagram for your design to explain inputs, outputs and the relation between them. If your design has more than one module, explain how they are related.

In this lab I have implemented the Datapath, a crucial part of the RISC-V Single Cycle Processor. The Datapath consists of instructions executing inwith using the program counter to supply the instruction address to the instruction memory. Within the Datapath, we use components that we have implemented from previous labs that are important components in the RISC-V Datapath. Those components include the Flip Flop, Instruction Memory, Immediate Generator, Register File, and the 2 to 1 Multiplexer. One more additional component is designed in this lab and that is the data memory.

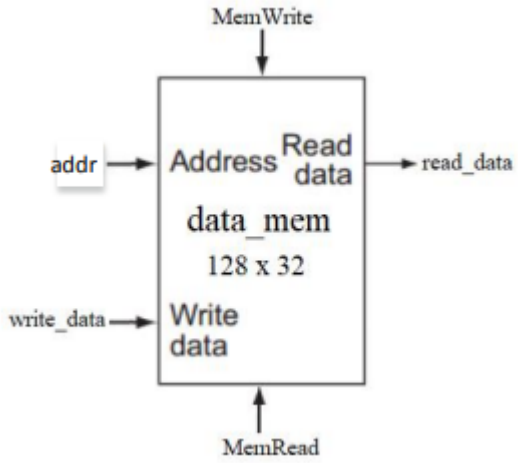
2 Procedure

Figure 1 : RISC-V Datapath.



In this lab, I had modeled the design by working on developing each component piece by piece. All components in this lab were created before in other labs, however, the Data Memory was a new component.

Data Memory:



In the Data Memory, there are several inputs: MemWrite, addr, write_data, and MemRead. There is one output: read_data. The Data Memory can store 128 bits with 32 bits, where 9 bits are required to for the address line. Therefore, the Data Memory is 128x32. The MemWrite is equal to 1 then it writes to the memory location specified by the address. The MemRead is equal to 1 then it reads the data from the memory location specified by the address and assigns it to the output.

Then, in the Datapath, I worked on instantiating each component, and worked on establishing all 10 of the wires.

3 Simulation Results

Given the testbench code in the lab instructions, I get the intended waveform (click the waveform blue llnk to see waveform. With the given components (ALU, Flip Flop, etc.), the testbench, and the intended waveform given in the instruction lab manual my design implementation works as expected. This proves that I have implemented the RISC-V Datapath, along with the Data Memory. This can further prove the logic in the wiring diagram as provided above and explained earlier. So, using this information, I implemented the logic in the given diagram for my Datapath design, scaled the size of input and output datra for each 2-to-1 Mux to 32 bits, created the Data Memory, and verified the Data Path wiring logic using the testbench provided.