



KP2182X

High Performance Quasi-Resonant Primary Side Regulation CV/CC Power Switch with Single Failure Protections

FEATURES

- Integrated with Power MOSFET
- High Efficiency Quasi-Resonant Primary Side Regulation (QR-PSR) Control
- High-Precision CC and CV Regulation
- Low Standby Power <75mW@265Vac
- Multi-Mode PSR Control
- Audio Noise Free Operation
- Fast Dynamic Response
- Optimized EMI Performance
- Built-in Cable Drop Compensation (CDC)
- Single Failure Protections for Power Supply
- Build in Protections:
 - Short Load Protection (FB SLP)
 - On-Chip Thermal Shutdown (OTP)
 - FB Over Voltage Protection (FB OVP)
 - VDD OVP & UVP & Clamp
- Available with SOP-7/8, DIP-8 and ASOP-6 Package

APPLICATIONS

- Battery Chargers for Cellular Phones
- AC-DC Power Adapter

GENERAL DESCRIPTION

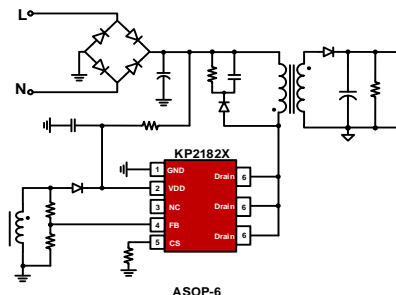
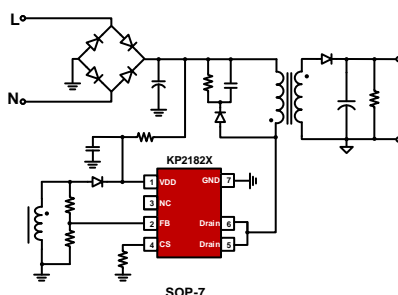
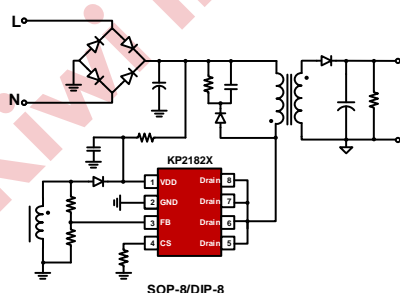
KP2182X is a family of high performance Quasi Resonant (QR) Primary Side Regulation (PSR) PWM power switch with high precision CV/CC control ideal for charger applications. At full load, the switch operates in quasi-resonant (QR) mode in the universal line voltage to optimize efficiency and thermal performance.

The IC can achieve audio noise free operation and optimized dynamic response. The built-in Cable Drop Compensation (CDC) function and line CC compensation can provide excellent CV, CC performance.

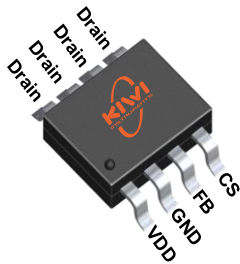
KP2182X integrates functions and protections of Under Voltage Lockout (UVLO), VDD over Voltage Protection (VDD OVP), Cycle-by-cycle Current Limiting (OCP), Short Load Protection (FB SLP), FB over Voltage Protection (FB OVP), On-Chip Thermal Shutdown, VDD Clamping, etc.

KP2182X also integrates single failure protections, which can ensure there is no damage to IC and no over voltage of output when IC pin open or short failure happens.

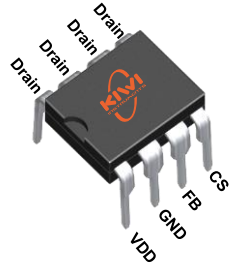
TYPICAL APPLICATION CIRCUIT



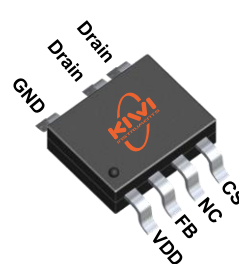
Pin Configuration



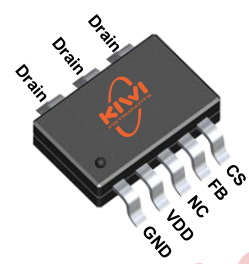
SOP-8



DIP-8



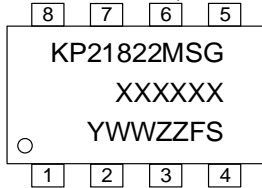
SOP-7



ASOP-6

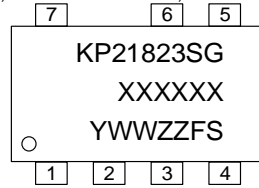
Marking Information

XXXXXX: Wafer Lot Code
Y: Year Code
WW: Week Code, 01-52
ZZ: Serial Number, 01-99 or A0-ZZ
F, S: Control Number, 1-9 or A-Z, a-z



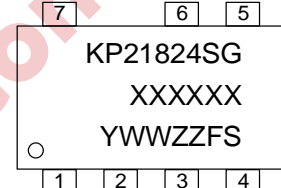
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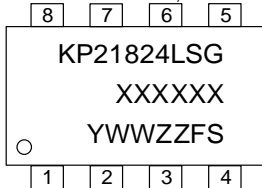
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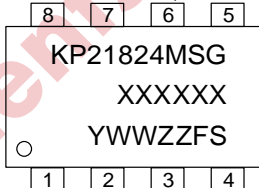
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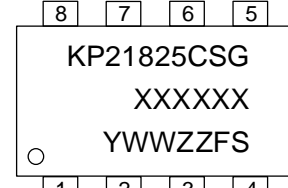
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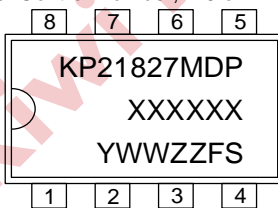
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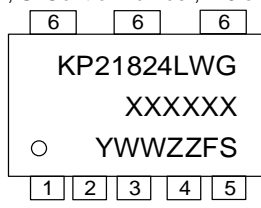
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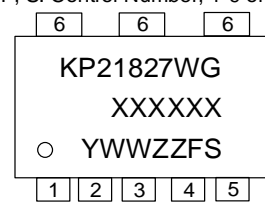
DIP-8

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ZZ: Serial Number, 01-99 or A0-ZZ
F, S: Control Number, 1-9 or A-Z, a-z



ASOP-6

XXXXXX: Wafer Lot Code
Y: Year Code
WW: Week Code, 01-52
ZZ: Serial Number, 01-99 or A0-ZZ
F, S: Control Number, 1-9 or A-Z, a-z



ASOP-6

Typical Output Power Table⁽¹⁾

Product	Package	230VAC \pm 15% ⁽²⁾	85-265VAC
		Adapter ⁽³⁾	Adapter ⁽³⁾
KP21822M	SOP-8	15W	12W
KP21823	SOP-7	18W	15W
KP21824	SOP-7	21W	18W
KP21824L	SOP-8	21W	18W
KP21824M	SOP-8	21W	18W
KP21825C	SOP-8	24W	21W
KP21824L	ASOP-6	24W	21W
KP21827M	DIP-8	27W	24W
KP21827	ASOP-6	27W	24W

(1) The Max. output power is limited by junction temperature.

(2) 230VAC or 100/115VAC with voltage doublers.

(3) Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern as a heat sink at 50°C ambient.

Pin Description

Pin Number ASOP-6	Pin Number SOP-8/DIP-8	Pin Number SOP-7	Pin Name	I/O ⁽⁴⁾	Description
1	2	7	GND	G	The Ground of the IC
2	1	1	VDD	P	IC Power Supply Pin
3	-	3	NC	-	No Connect
4	3	2	FB	I	System Feedback and Demagnetization Detection Pin
5	4	4	CS	I	Current Sense Input Pin
6	5, 6, 7, 8	5,6	Drain	P	The Power MOSFET Drain

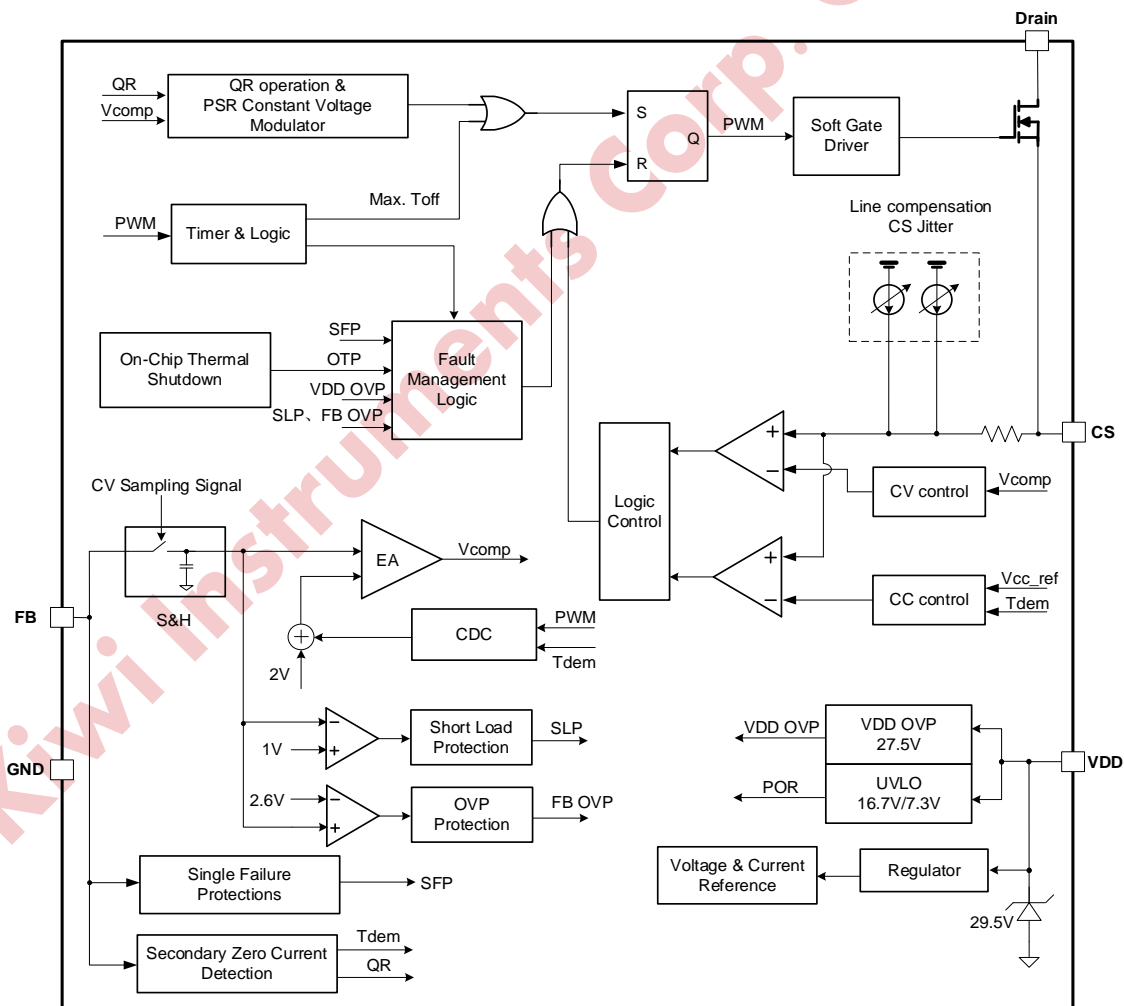
(4) I - Input; P - Power; G - Ground

Ordering Information

Part Number ⁽⁵⁾	Description
KP21822MSG A	SOP-8, Halogen free, in T&R, 4000Pcs/Reel
KP21823SG A	SOP-7, Halogen free, in T&R, 4000Pcs/Reel
KP21824SG A	SOP-7, Halogen free, in T&R, 4000Pcs/Reel
KP21824LSG A	SOP-8, Halogen free, in T&R, 4000Pcs/Reel
KP21824MSG A	SOP-8, Halogen free, in T&R, 4000Pcs/Reel
KP21825CSG A	SOP-8, Halogen free, in T&R, 4000Pcs/Reel
KP21827MDP	DIP-8, Pb free, 50Pcs/Tube
KP21824LWGA	ASOP-6, Halogen free, in T&R, 5000Pcs/Reel
KP21827WGA	ASOP-6, Halogen free, in T&R, 5000Pcs/Reel

(5) Suffix "A" - Tape&Reel

Block Diagram





KP2182X

High Performance Quasi-Resonant Primary Side Regulation
CV/CC Power Switch with Single Failure Protections

Absolute Maximum Ratings⁽⁶⁾

Parameter		Value	Unit
VDD DC Supply Voltage		-0.3 to 33	V
VDD DC Clamp Current		5	mA
Drain pin Voltage Range		-0.3 to 650	V
FB Voltage Range		-0.7 to 5.5	V
CS Voltage Range		-0.3 to 5.5	V
Package Thermal Resistance---Junction to Ambient (SOP-7/8)		165	°C/W
Package Thermal Resistance---Junction to Ambient (DIP-8)		105	°C/W
Package Thermal Resistance---Junction to Ambient (ASOP-6)		120	°C/W
Maximum Junction Temperature		165	°C
Storage Temperature Range		-40 to 165	°C
Lead Temperature (Soldering, 10sec.)		260	°C
ESD Capability, HBM (Human Body Model)		3	kV
ESD Capability, CDM (Charged Device Model)		2	kV
Maximum MOSFET Continuous Drain Current	KP21822M	2	A
	KP21823	3	A
	KP21824	2	A
	KP21824M	4	A
	KP21824L(SOP-8)	4	A
	KP21825C	2.7	A
	KP21827M	7	A
	KP21824L(ASOP-6)	4	A
	KP21827	3.5	A
Maximum MOSFET Pulse Drain Current	KP21822M	8	A
	KP21823	12	A
	KP21824	8	A
	KP21824M	16	A
	KP21824L(SOP-8)	16	A
	KP21825C	8.1	A
	KP21827M	28	A
	KP21824L(ASOP-6)	16	A
	KP21827	10.5	A

Recommended Operation Conditions

Parameter	Value	Unit
Supply Voltage, VDD	9 to 25	V
Operating Junction Temperature	-40 to 125	°C

Electrical Characteristics (T_A= 25°C, VDD=10V, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage Section (VDD Pin)						
I _{VDD_st}	Start-up current into VDD pin	VDD < VDD _{on}	0	0.5	15	μA
I _{VDD_Op}	Operation Current ⁽⁷⁾		200	330	500	μA
V _{DD_ON}	VDD Under Voltage Lockout Exit		15.5	16.7	17.5	V
V _{DD_OFF}	VDD Under Voltage Lockout Enter		6	7.3	8	V
V _{DD_OVP}	VDD OVP Threshold		25	27.5	30	V
V _{DD_Clamp}	VDD Zener Clamp Voltage	I(V _{DD}) > 8 mA	27.5	29.5	31.5	V
Control Function Section (FB Pin)						
V _{FBREF}	Internal Error Amplifier (EA) Reference Input		1.97	2.0	2.02	V
V _{FB_SLP}	Short Load Protection (SLP) Threshold ⁽⁷⁾			1		V
T _{FB_Short}	Short Load Protection (SLP) Debounce Time ⁽⁷⁾			50		ms
V _{FB_OVP}	FB Over Voltage Protection Threshold ⁽⁷⁾			2.6		V
T _{FB_OVP}	FB Over Voltage Protection Debounce Time			3		Cycle
V _{FB_DEM}	Demagnetization Comparator Threshold (FB < 1.4V)	Upper Threshold		20		mV
		Lower Threshold		-20		mV
	Demagnetization Comparator Threshold (FB > 1.4V)	Upper Threshold		50		mV
		Lower Threshold		-170		mV
T _{on_max}	Maximum ON time ⁽⁷⁾			32		μs
T _{blank}	Leading Edge Blanking Time	Light Load ⁽⁷⁾	1.8	2	2.2	μs
		Heavy Load ⁽⁷⁾	3.1	3.5	3.9	μs
T _{off_max}	Maximum OFF time ⁽⁷⁾		3.4	3.9	4.5	ms
F _{max}	Maximum Switching Frequency ⁽⁷⁾		90	100	110	kHz

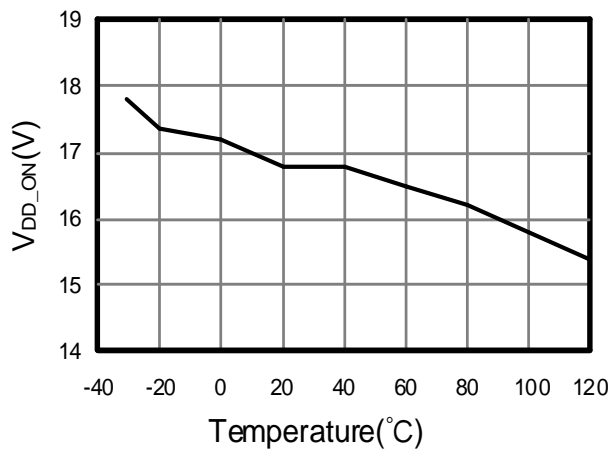
CDC	Maximum Cable Drop Compensation, $V_{cdc} / V_{out}^{(7)}$			3		%
Current Sense Input Section (CS Pin)						
T_{LEB}	CS Input Leading Edge Blanking Time			400		ns
V_{cs_max}	Maximum Current limiting threshold ⁽⁷⁾		755	785	815	mV
V_{cs_min}	Minimum Current limiting threshold ⁽⁷⁾		170	180	190	mV
T_{D_OC}	Over Current Detection and Control Delay			100		ns
CC Loop						
V_{CC_ref}	CC Loop Reference		0.33	0.34	0.35	V
On-Chip Thermal Shutdown						
T_{SD}	Thermal Shutdown ⁽⁷⁾		150	155	160	°C
T_{RC}	Thermal Recovery ⁽⁷⁾		120	125	130	°C
Power MOSFET Section (Drain Pin)						
$V_{BR}^{(8)}$	Power MOSFET Drain Source Breakdown Voltage		650			V
$R_{ds(on)}$	Static Drain-Source On Resistance	KP21822M		5.3	6.4	Ω
		KP21823		2.9	3.5	Ω
		KP21824		2.2	2.5	Ω
		KP21824M		2.2	2.6	Ω
		KP21824L(SOP-8)		2.6	3.1	Ω
		KP21825C		1.6	1.8	Ω
		KP21827M		1.2	1.4	Ω
		KP21824L(ASOP-6)		2.6	3.1	Ω
		KP21827		1.25	1.45	Ω

(6) Stresses listed as the above "Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.

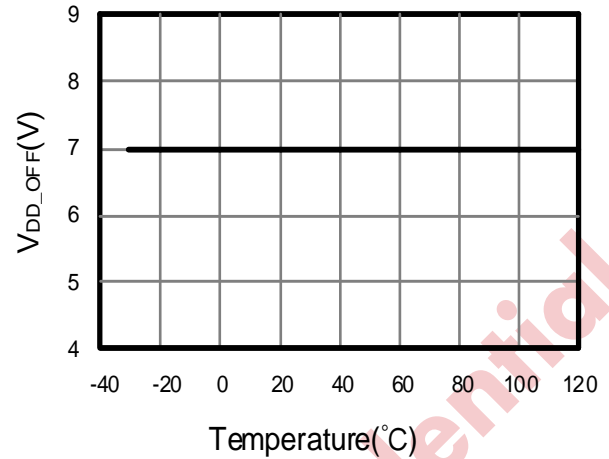
(7) Guaranteed by the Design.

(8) For KP21824L(SOP-8/ASOP-6), MOSFET minimum drain to source breakdown voltage is 620V and the MOSFET can withstand 650V voltage spike with duration below 200ns.

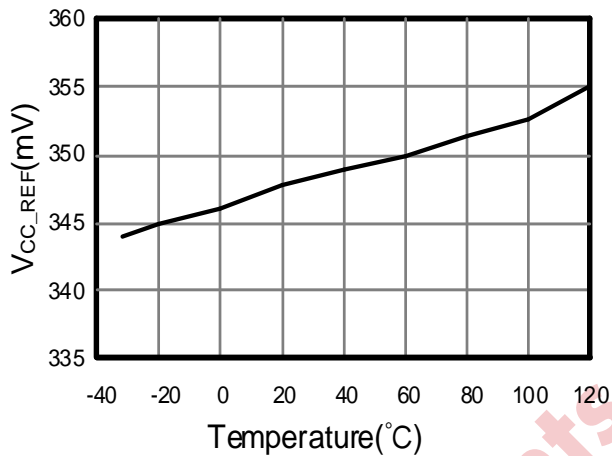
Characterization Plots



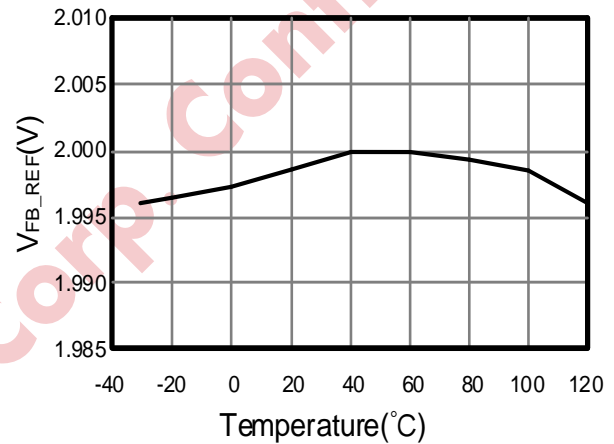
V_{DD_ON} vs Temperature



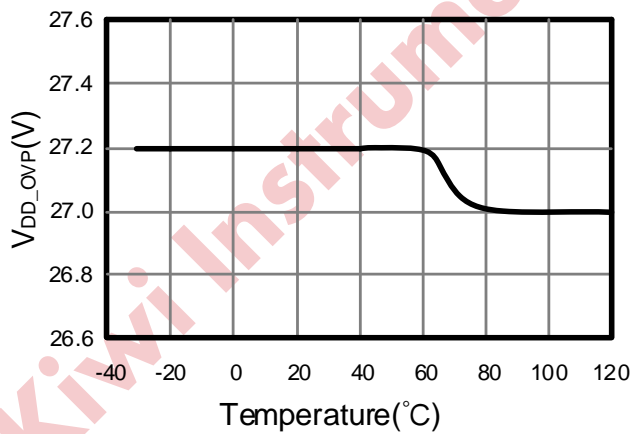
V_{DD_OFF} vs Temperature



V_{CC_REF} vs Temperature



V_{FB_REF} vs Temperature



V_{DD_OVP} vs Temperature

Operation Description

KP2182X is a high performance, multi-mode Quasi Resonant Primary Side Regulation (QR-PSR) power switch ideal for charger applications. At full load, the switch operates in quasi-resonant (QR) mode in the universal line voltage to optimize efficiency and thermal performance.

● System Start-Up Operation

Before the IC starts to work, KP2182X consumes only I_{VDD_st} (typically 0.5 μA) which allows a large value startup resistor to be used to minimize the standby power loss. When VDD reaches turn-on voltage V_{DD_ON} (typically 16.7V), KP2182X begins switching. The hold-up capacitor continues to supply VDD before the auxiliary winding of the transformer takes control.

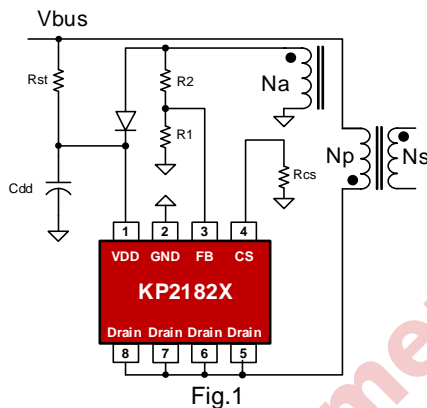


Fig.1

● PSR Constant Voltage Modulation (PSR-CV Mode)

In Primary Side Regulation (PSR) control, the output voltage is sensed on the auxiliary winding when transformer energy is transferred to the secondary side. Fig.2 illustrates the timing waveform of CV sampling signal, demagnetization signal in KP2182X. When the CV sampling process is over, the internal sample/hold (S&H) circuit captures the error signal and amplifies it through the internal Error Amplifier (EA). The output of EA is sent to the PSR CV Modulator (PSR-CVM) for high-precision CV regulation. The internal reference voltage V_{FBREF} is trimmed to be 2V.

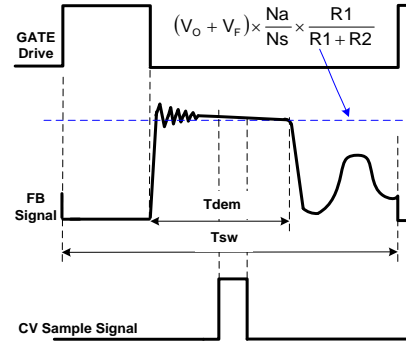


Fig.2

Fig.2 also illustrates the equation for “demagnetization plateau”,

$$V_{FB} = (V_O + V_F) \times \frac{N_a}{N_s} \times \frac{R_1}{R_1 + R_2}$$

where V_O and V_F are the output voltage and diode forward voltage; R_1 and R_2 are the resistor divider connected from the auxiliary winding to FB Pin, N_s and N_a are secondary winding and auxiliary winding respectively.

● PSR Constant Current Modulation (PSR-CC Mode)

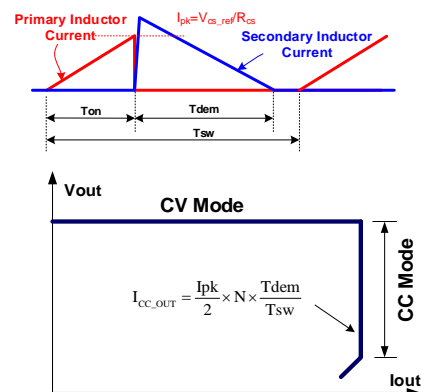


Fig.3

Referring to Fig.3 above, the primary peak current, transformer turns ratio, secondary demagnetization time (T_{dem}), and switching period (T_{sw}) determines the secondary average output current I_{out} . Ignoring leakage inductance effects, the equation for average output current is shown in Fig.3.

In CC mode, the IC operates in QR mode and adjust V_{cc_ref} automatically to achieve constant output current. The average output current can be expressed as:

$$I_{CC_OUT} \cong \frac{1}{2} \times N \times \frac{V_{cc_ref}}{R_{cs}}$$

In the equation above,

N---The turn ratio of primary side winding to secondary side winding.

Rcs---The sensing resistor connected between the power MOSFET source to GND.

Vcc_ref---CC Loop Reference.

● Multi-Mode Control in CV Mode

To meet the tight requirement of average system efficiency and no-load power consumption, a hybrid of frequency modulation (FM) and amplitude modulation (AM) is adopted in KP2182X which is shown in the Fig 4.

At full load, the system operates in QR mode to optimize efficiency and thermal performance. The IC operates in FM+AM mode for high efficiency and audio noise reduction under normal and light load.

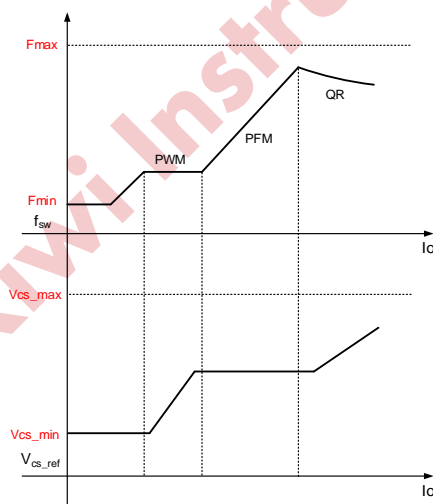


Fig.4

● Cable Drop Compensation (CDC)

In smart phone charger application, the battery is always connected to the adapter with a cable wire which can cause several percentages of voltage drop on the actual battery voltage. KP2182X integrates built-in cable drop compensation (CDC), which is proportional to the output power P_{out} to get a straight constant voltage output curve. The percentage of maximum compensation is 3% of V_o .

● Line CC Compensation

The turn-off delay of MOSFET affects CC performance, and OCP value at high voltage input will be much larger than at low voltage input without compensation. KP2182X integrates built-in line CC compensation to achieve excellent line CC regulation.

● Optimized Dynamic Response

The dynamic response performance is optimized to meet USB charge requirements.

● Audio Noise Free Operation

As mentioned above, the multi-mode CV control with a hybrid of FM and AM can provide audio noise free operation from full load to zero load.

● Single Failure Protections for Power Supply

KP2182X integrates single failure protections, including FB pull-up resistor open protection, FB pull-down resistor open protection, FB pull-down resistor short protection, output rectifier diode or SR short protection, transformer windings short protection, Rcs open protection and IC GND pin open protection. The IC will enter auto recovery protection mode once single failure occurs. This function can ensure there is no damage to IC and no over voltage of output.

● Short Load Protection (FB SLP)

The output is sampled on FB pin and then compared with V_{FB_SLP} (typically 1V).

When sensed FB voltage is below V_{FB_SLP} and lasts for T_{FB_Short} (typically 50ms), the IC will enter into Short Load Protection (SLP) mode, in which the IC will enter into auto recovery protection mode.

● FB Over Voltage Protection (FB OVP)

When sensed FB voltage is above V_{FB_OVP} (typically 2.6V) and lasts for T_{FB_OVP} (typically 3 cycles), the IC will enter into FB Over Voltage Protection (FB OVP) mode, in which the IC will enter into auto recovery protection mode.

● VDD Over Voltage Protection (OVP) and Zener Clamp

When VDD voltage is higher than V_{DD_OVP} (typically 27.5V), the IC will stop switching. This will cause VDD fall down to be lower than V_{DD_OFF} (typically 7.3V) and then the system will restart up again. An internal Zener clamp is integrated to prevent the IC from damage, and the clamp voltage is V_{DD_Clamp} (typically 29.5V).

● On-Chip Thermal Shutdown (OTP)

When the IC temperature is over T_{SD} (typically 155°C), the IC shuts down. Only when the IC temperature drops to T_{RC} (typically 125°C), IC will restart.

● Soft Totem-Pole Gate Driver

KP2182X has a soft totem-pole gate driver with optimized EMI performance. An internal 16V clamp circuit is added for power MOSFET gate protection.

Application Information

● PCB Layout Guidelines

PCB design has a significant impact on the performance of power supply. It is recommended to refer to Figure 5 and Figure 6 when designing primary-side circuit.

1. The main power loop(Loop1) should be as small as possible and the trace should be wide for better efficiency performance.
2. The snubber circuit Loop(Loop2) should be as small as possible.
3. Place VDD capacitor C3 close to the IC to ensure the VDD loop(Loop3) is small.
4. The ground node of auxiliary winging should be connected directly to the negative node of the bus capacitor (Line1 as shown in Fig.5)
5. VDD capacitor C3 and FB pull-down resistor R5 should be connected directly to the IC GND pin firstly, and then connects them to the negative node of the bus capacitor with a single point (Line2 as shown in Fig.5)

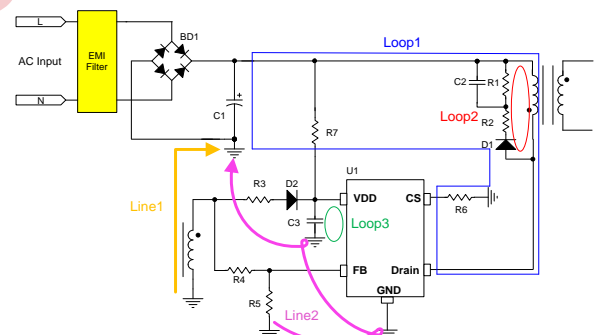


Fig.5

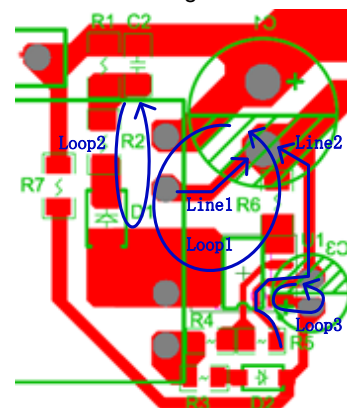
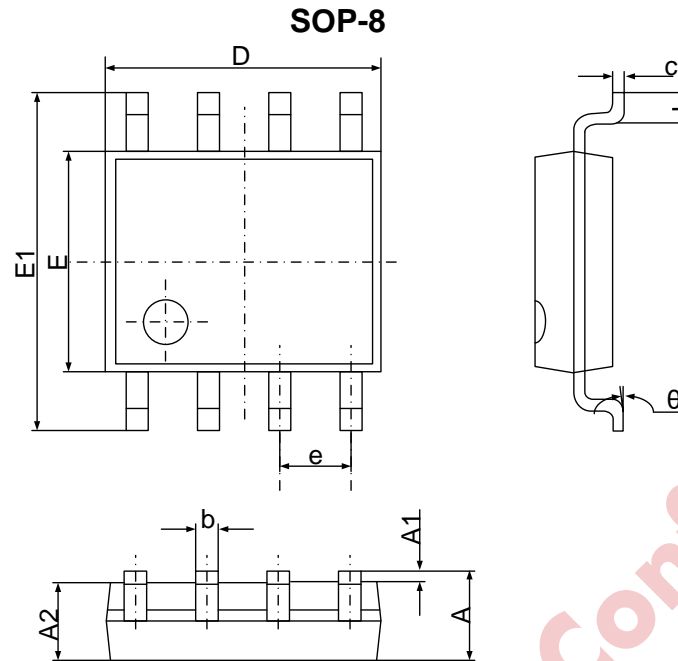


Fig.6

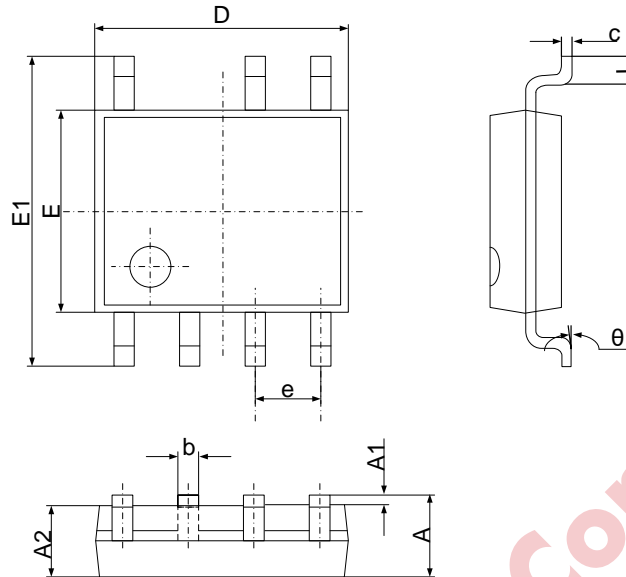
Package Dimension



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.300	1.500	0.051	0.059
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Dimension

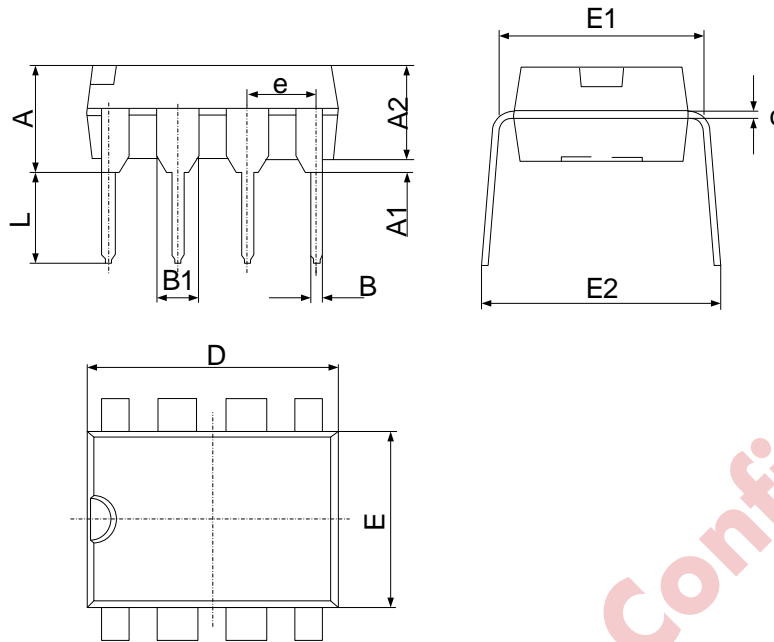
SOP-7



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.300	1.500	0.051	0.059
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Dimension

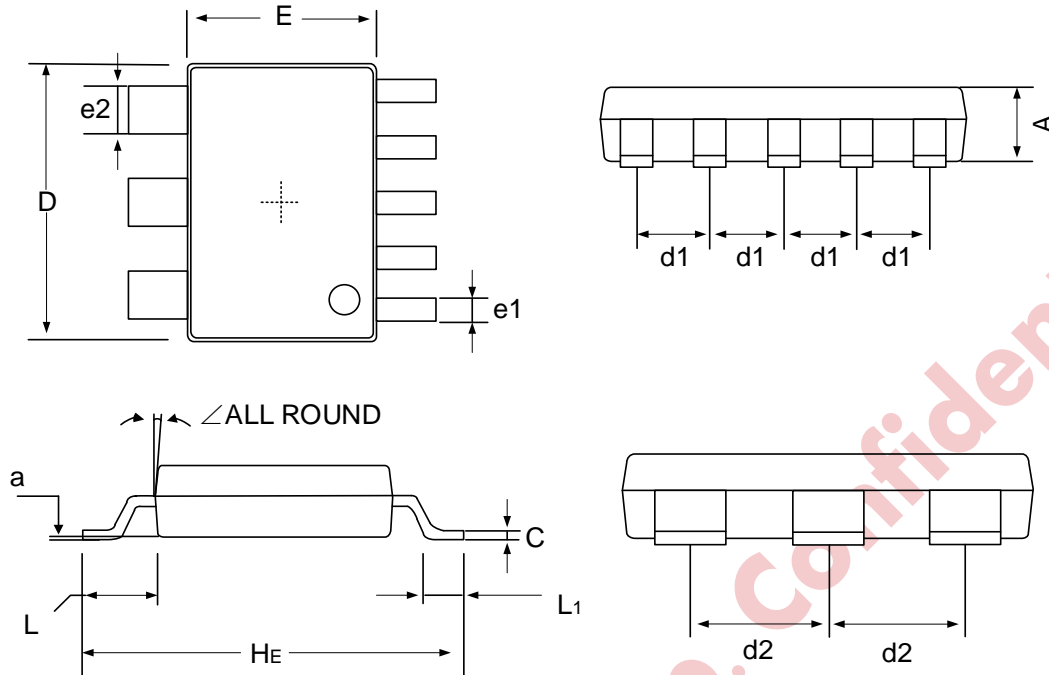
DIP-8



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	3.600	4.150	0.142	0.163
A1	0.510	-	0.020	-
A2	3.150	3.400	0.124	0.134
B	0.380	0.560	0.015	0.022
B1	1.524 (BSC)		0.060 (BSC)	
C	0.200	0.350	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.500	0.244	0.256
E1	7.620 (REF)		0.300 (REF)	
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	7.620	9.300	0.300	0.366

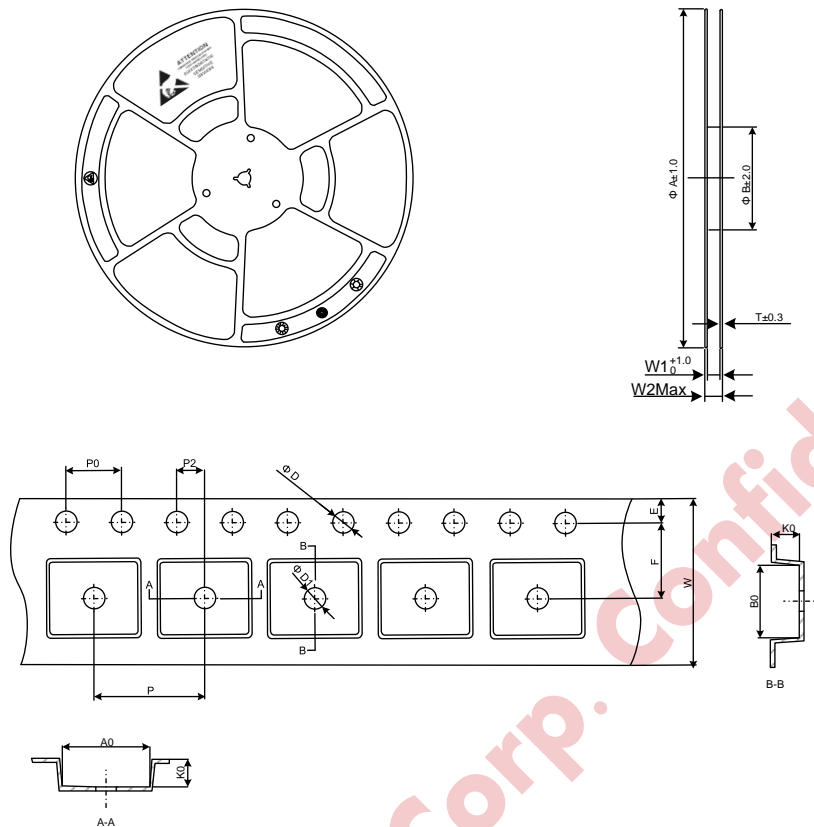
Package Dimension

ASOP-6



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.050	1.150	1.250	0.041	0.045	0.049
a	0.200 (REF)			0.008 (REF)		
C	0.150	0.200	0.220	0.006	0.008	0.009
D	6.000	6.200	6.400	0.236	0.244	0.252
d1	1.250	1.300	1.350	0.049	0.051	0.053
d2	1.950	2.000	2.050	0.077	0.079	0.081
E	3.700	3.900	4.100	0.146	0.154	0.161
e1	0.350	0.400	0.450	0.014	0.016	0.018
e2	1.550	1.600	1.650	0.061	0.063	0.065
HE	5.900	6.000	6.100	0.232	0.236	0.240
L	0.950	1.050	1.150	0.037	0.041	0.045
L1	0.400	-	0.800	0.016	-	0.031
∠	12°					

Tape and Reel Information

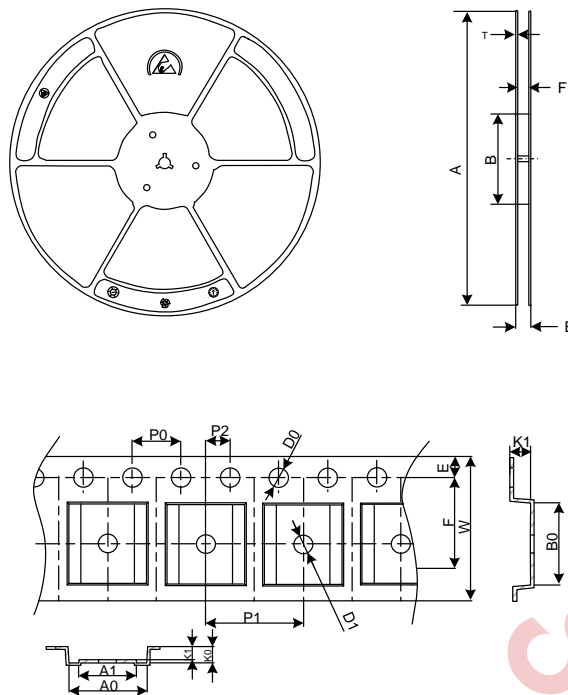


Reel Dimensions (mm)				
A	B (Inner Diameter)	W1	W2Max	T
330	100	12.4	18.4	1.5

Tape Dimensions			
Symbol	Dimensions (mm)	Symbol	Dimensions (mm)
E	1.75 ± 0.10	W	12.00 ± 0.10
F	5.50 ± 0.10	P	8.00 ± 0.10
P2	2.00 ± 0.10	A0	6.60 ± 0.10
D	$1.50^{+0.1}_0$	B0	5.30 ± 0.10
D1	1.55 ± 0.05	K0	1.90 ± 0.10
P0	4.00 ± 0.10		

Packing Quantity				
Package	Pcs/Reel	Reels/Box	Boxes/Carton	Pcs/Carton
SOP-7	4000	2	8	64000
SOP-8	4000	2	8	64000

Tape and Reel Information



Reel Dimensions (mm)				
A	B (Inner Diameter)	E	F	T
330±2	100±1	16.9±0.5	12.7 ⁺² _{-0.5}	2.1±0.2

Tape Dimensions			
Symbol	Dimensions (mm)	Symbol	Dimensions (mm)
A0	6.40±0.10	K1	1.50±0.10
B0	6.60±0.10	E	1.75±0.10
K0	1.70±0.10	F	5.50±0.05
P0	4.00±0.10	D0	1.55±0.05
P1	8.00±0.10	D1	1.55±0.05
P2	2.00±0.05	W	12.0±0.30
A1	3.80±0.10		

Packing Quantity				
Package	Pcs/Reel	Reels/Box	Boxes/Carton	Pcs/Carton
ASOP-6	5000	2	5	50000

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