אוניברסיטת בן גוריון בנגב

בית הספר להנדסת חשמל ומחשבים

דו"ח פרויקט גמר- מעבדת ארכיטקטורה ומאיצי חומרה

MCU

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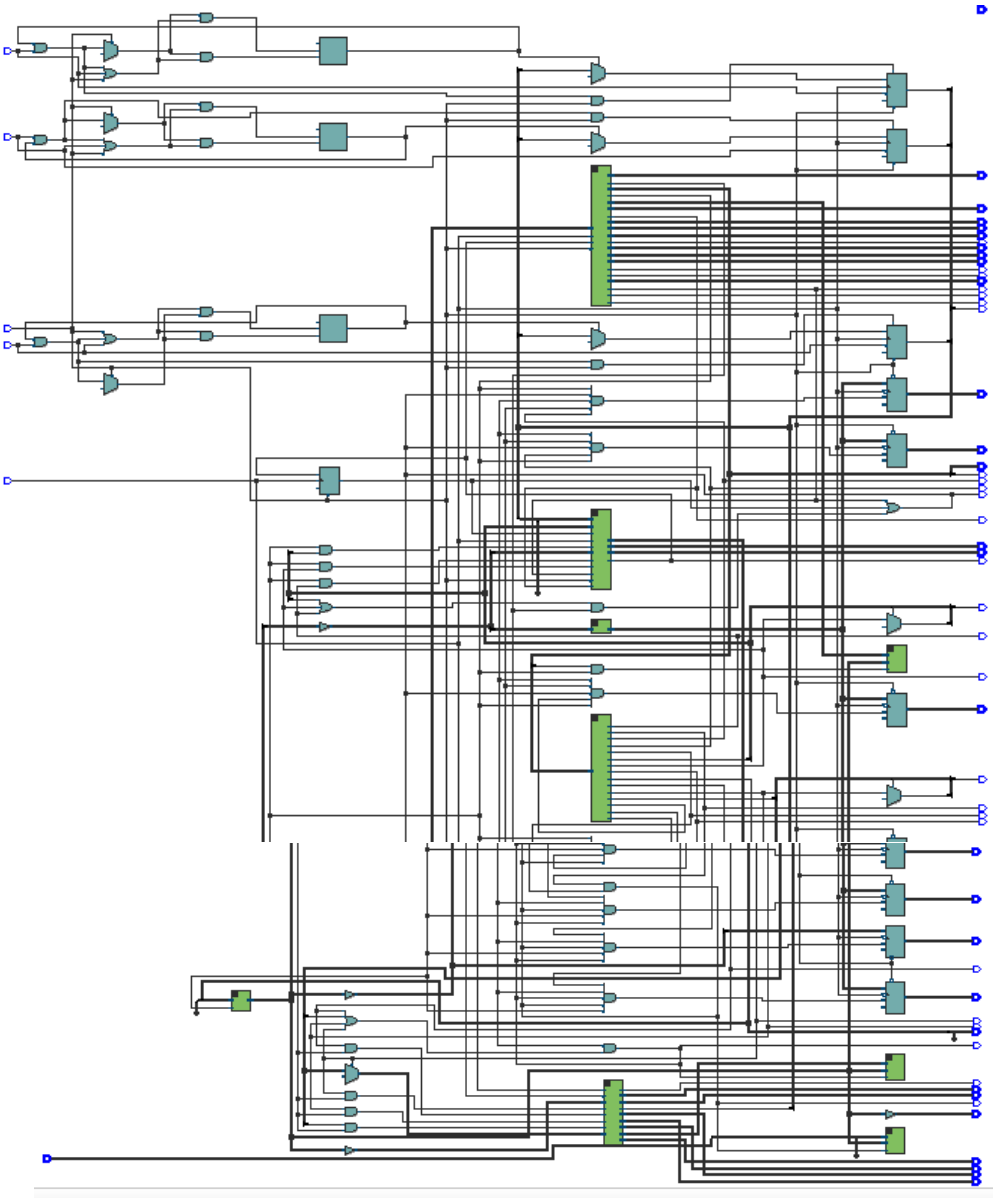
MCU

This project implementing an MCU unit which include MIPS pipeline CPU with integrated components for GPIO interfacing using LEDs and HEX displays as outputs, switches as inputs, a basic timer unit with PWM and interrupt generation, and an interrupt handler to facilitate communication between the CPU and the peripherals.

This project aims to provide a comprehensive example of designing a MIPS-based system with basic I/O, timing, and interrupt functionalities.

RTL:



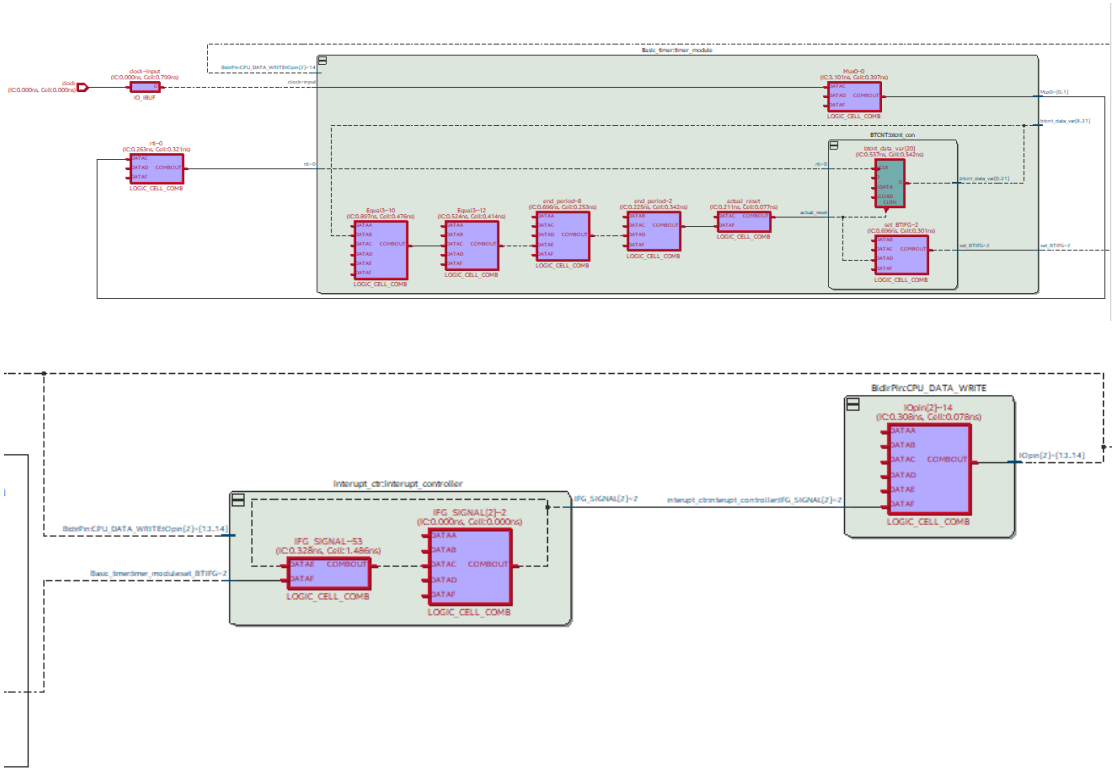
Timing:

Slow 1100mV 85C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	
1	37.62 MHz	37.62 MHz	clock

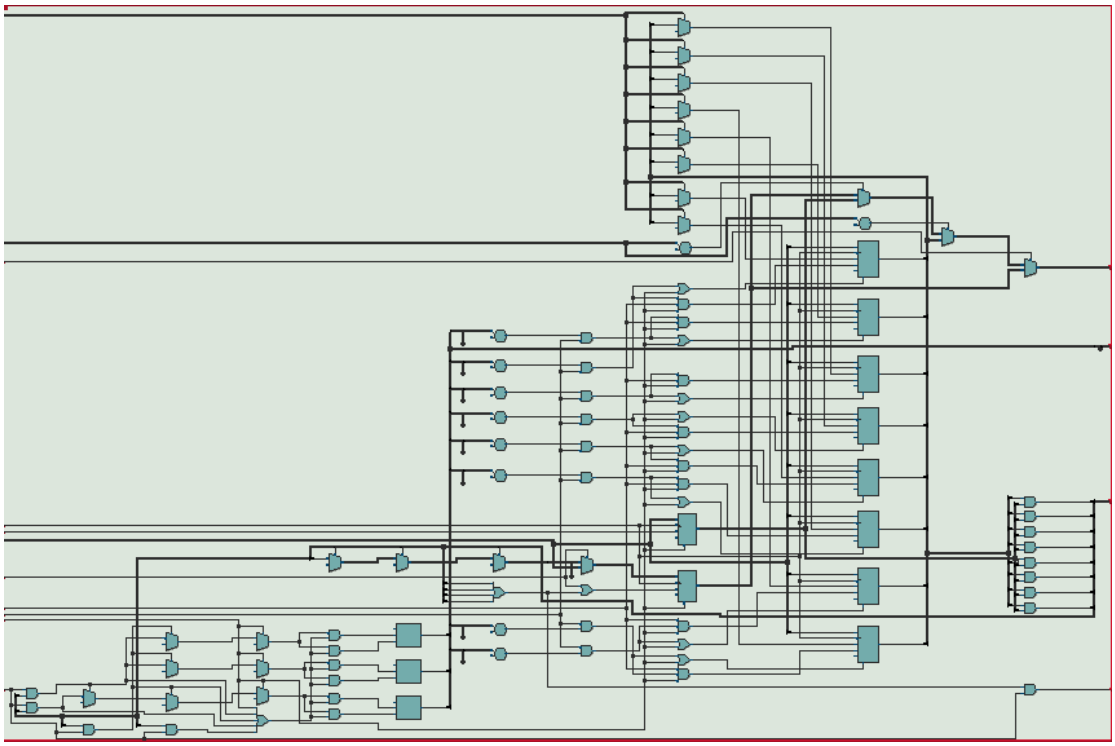
In lab 5, we showed that our CPU's frequency is 58 Mhz. We inferred that the peripheral components added a significant critical path as described in the following figures:

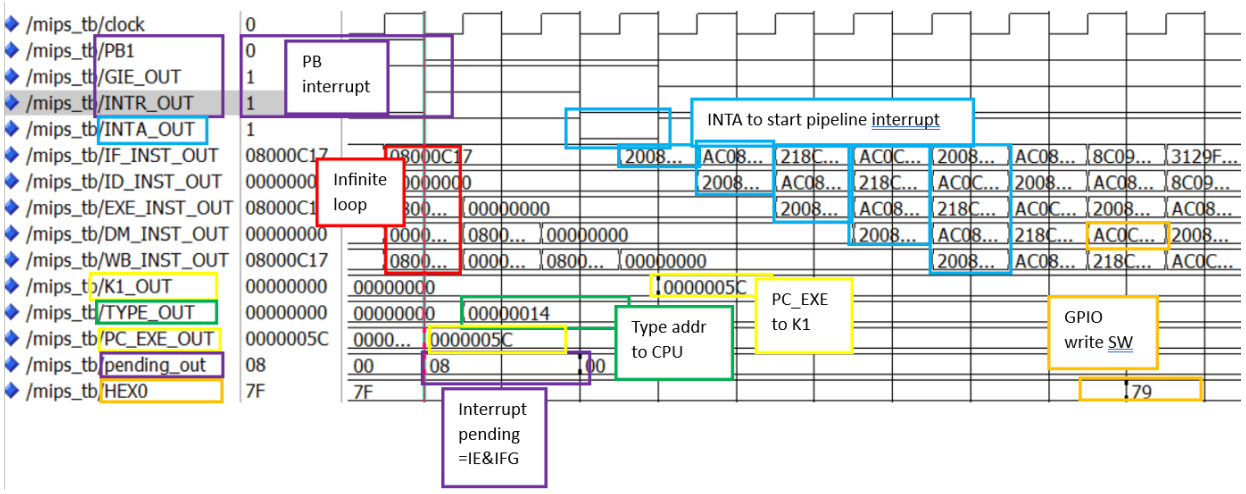


The critical path is an interupt request commming from the Basic Timer module, via the interupt controller.

INTERRUPT CONTROLLER

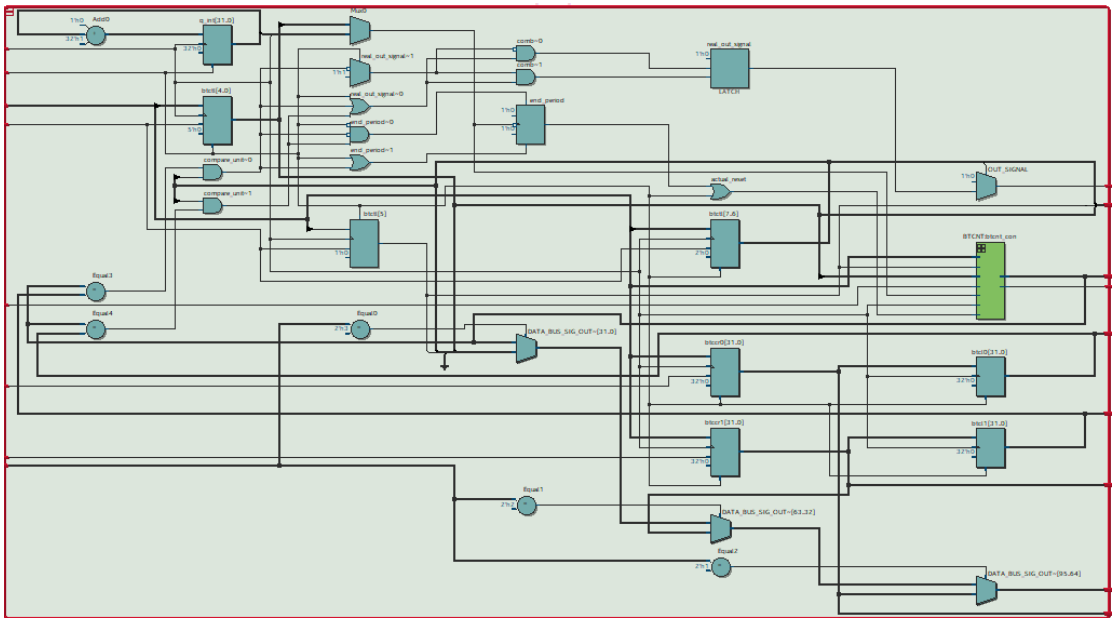
The interrupt controller manages interrupts generated by the timer unit and external push buttons. It interacts with the CPU's interrupt enable (IE) and interrupt flag (IFG) registers. If the Global Interrupt Enable (GIE) flag is set in the IE register, and an interrupt condition is met (such as a timer compare match or a push button press), the handler generates an interrupt signal (INTR) that prompts the CPU to jump to the specified memory address (PC of mem[type]).

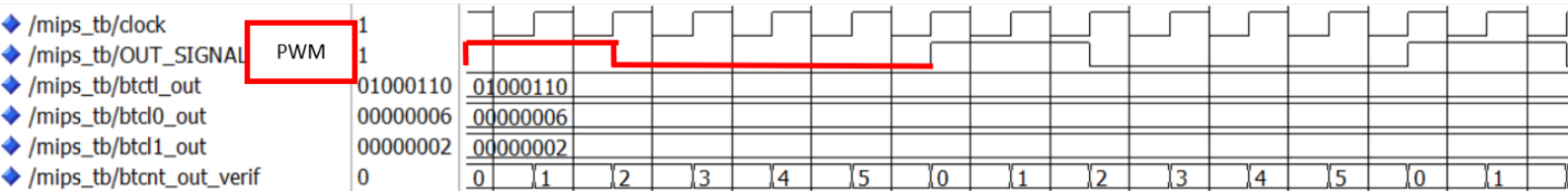




BASIC TIMER

The timer unit is composed of the Basic Timer Control and Clock Registers (BTCCR0, BTCCR1, BTCTL) and generates a PWM signal. The BTCCR0 and BTCCR1 registers set the timer period and compare value respectively, while the BTCTL register configures timer settings. The timer also generates an interrupt when the timer reaches the compare value, indicated by the Basic Timer Interrupt Flag (BTIFG).

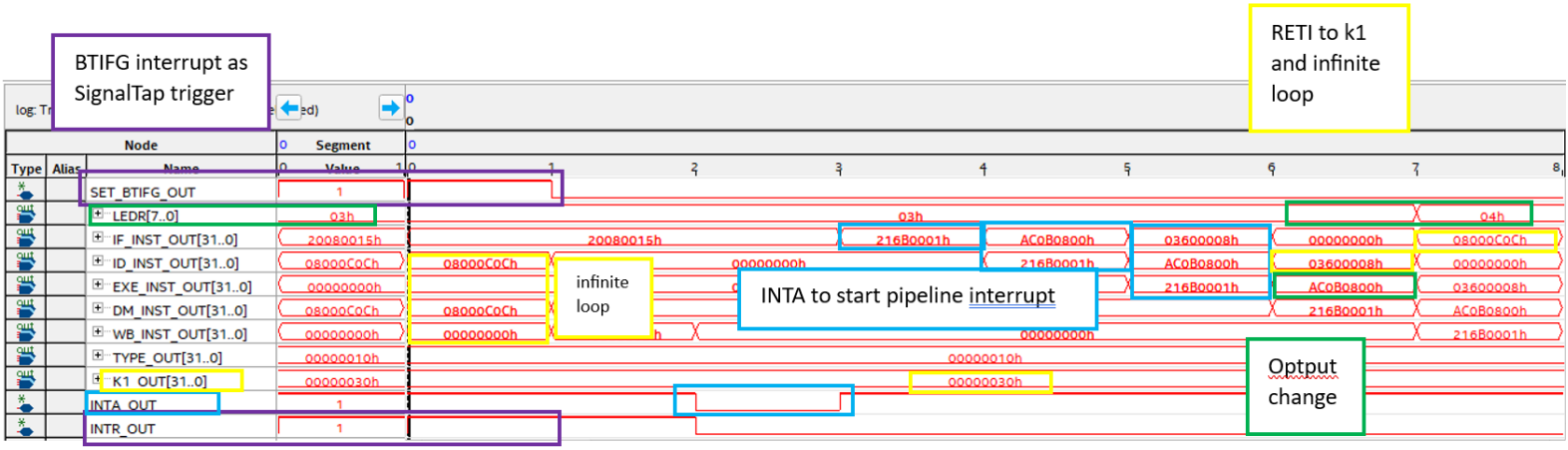




GPI/GPO

The GPI and GPO interfaces control LEDs and HEX displays for output and reads switches for input. The output components can be read by the CPU via addresses 0x800 (LEDS) and 0x804 , 0x805, 0x808, 0x80C, 0x80D (Hexs). The input components are eight switches with address 0x810.

SIGNAL TAP



Flow Status	In progress - Mon
Quartus Prime Version	21.1.0 Build 842 1
Revision Name	MCU
Top-level Entity Name	MCU
Family	Cyclone V
Device	5CSXFC6D6F31C
Timing Models	Final
Logic utilization (in ALMs)	N/A
Total registers	11234
Total pins	229
Total virtual pins	426
Total block memory bits	2,715,648
Total DSP Blocks	2
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0