sfp_clk_init module is used to configure Si5324 clock generation chip on NetFPGA-SUME board. The corresponding register values for a desired configuration of Si5324 are stored to a ROM inside the module. Upon release of its reset pin, sfp_clk_init module immediately programs the chip with the register values stored in its ROM through i2c interface.

Note: After downloading the module, the following extra actions must be performed:

i. A ROM IP must be generated with the name “si5324_regs_rom”. The configuration details of the ROM (depth, width, etc.) are given below in the document.
ii. i2c controller component core must be downloaded from opencores.org repository via the following link:
http://opencores.com/project,i2c

If the module is instantiated as it is, and input clock (CLK) frequency of the module is set to 100 MHz, it will create 156.25 MHz reference clock for SFP connectors.

If a different configuration is desired, the user may use the Silicon Labs - DSPLLsim software to create a specific frequency plan for the device and to get the required register configuration for that specific configuration. DSPLLsim software could be downloaded using the below link:

http://www.silabs.com/Support%20Documents/Software/PrecisionClock_EVBSoftware.zip

Upon getting the corresponding register configuration list from DSPLLsim software for a desired frequency plan, the next action for the user to take is to store this list in the module ROM through a .coe file. Please refer to the following default coe file:

…\pcores\nf_sume_sfp_clk_init\xci\si5324_regs_rom\Si5324_regs_init.coe

This coe file creates 156.25 MHz clock when the module is run with 100 MHz clock (the module input clock “CLK” pin is directly connected to Si5324 CLKIN port after conversion to LVDS). The coe file is basically this:

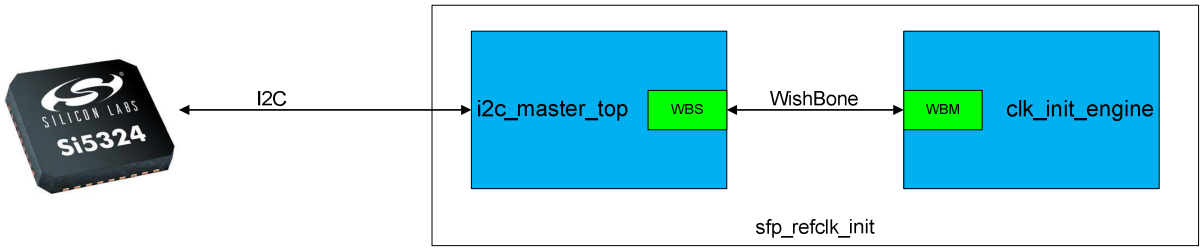
memory_initialization_radix=16;

memory_initialization_vector=

0014 01E4 02A2 0315 0492 05ED 062D 072A 0800 09C0 0A00 0B42 1329 143E 15FF 16DF 171F 183F 1900 1F00 2000 2107 2200 2300 2407 28C0 2900 2AF9 2B00 2C00 2D31 2E00 2F00 3031 3700 831F 8402 8901 8A0F 8BFF 8E00 8F00 8840;

Each entry of ROM is composed of address and value of a register. For example, consider the first entry 0014: 00 is the address of the register, 14 is the value of the register with that address, which is 00 in this case. The number of entries in the ROM is fixed, which is 43. So for any configuration, each of these 43 registers must be written.

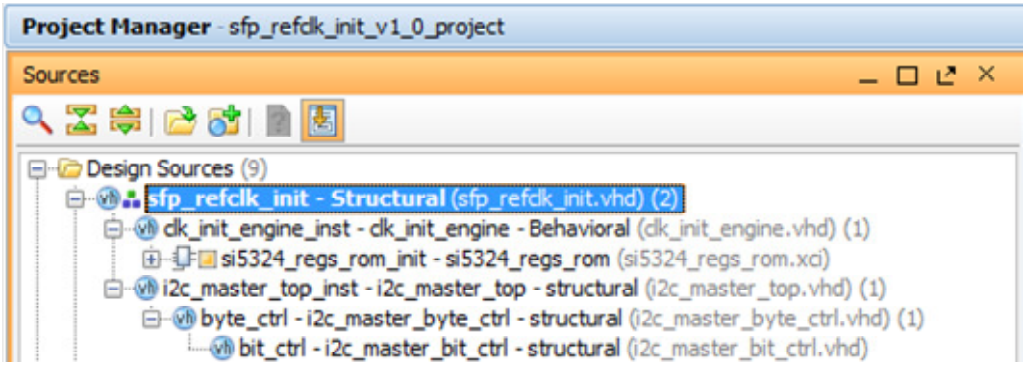
Here is the block diagram of the core:



i2c_master_top is a i2c controller core which is available in opencores.org , please download the module from the link below:

http://opencores.com/project,i2c

When you instantiated the sources in your RTL project, it must look like this:



“si5324_regs_rom” must be generated with the following configuration:

Depth: **64**, Data Width: **16**, Input: **Non Registered**, Output: **Registered**, coefficients file: **si5324_regs_init.coe**

About CLK and RST: RST is active high. CLK is 100 MHz. It needs some modification if another clock frequency is needed. The document will be updated with the required modification soon, or please feel free to contact me for this or any other question/feedback.

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