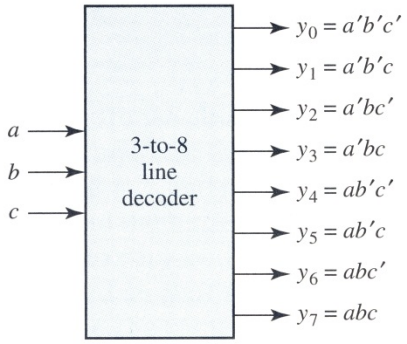
DSD Midterm exam 11/16 2011

1. Use the K-map method to find the minimized sum-of-product expression for each F: **(8%)**
   a) **(4%)** $\mathrm{F}(W,X,Y,Z) = \prod M(0,1,2,5,8,9,10,15) * \prod D(7,13,14)$
   b) **(4%)** $\mathrm{F}(A,B,C,D,E) = \sum m\,(0,2,4,8,9,11,13,15,18,20,22,25,29,31) + \sum d(6,10,19,23,27)$

2. Hazards in circuit design: **(12%)**
   a) There are two kinds of static hazards, what are they? Give an example of a static hazard and explain how to avoid it. **(8%)**
   b) Give an example to illustrate when will a dynamic hazard occur? **(4%)**

3. Realize an one-bit full adder using a 3-to-8 line decoder as Fig 1 below and
   (a) Two **OR** gates. **(5%)**
   (b) Two **NOR** gates. **(5%)**

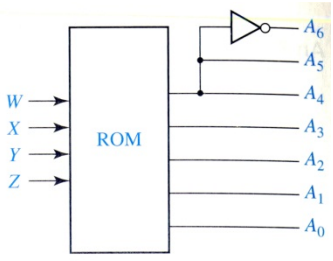
FIGURE
A 3-to-8 Line Decoder

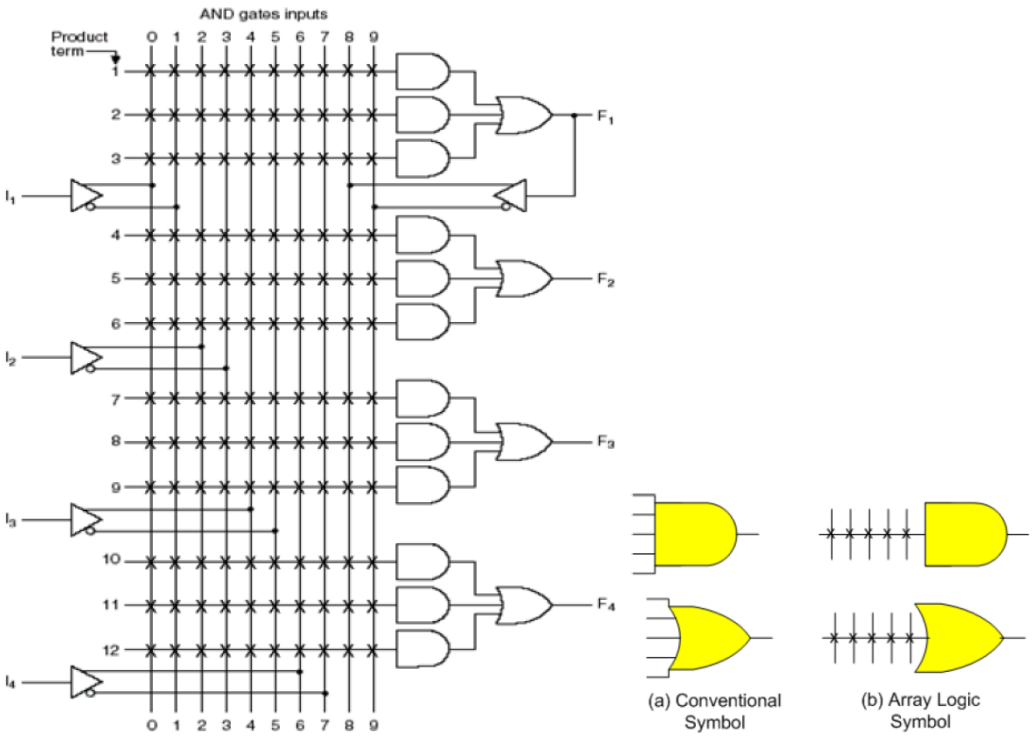


4. If the ROM in the hexadecimal to ASCII code converter of FIGURE is replaced with a PAL, give the internal connection diagram. **(20%)**

FIGURE
Hexadecimal-to-ASCII Code Converter

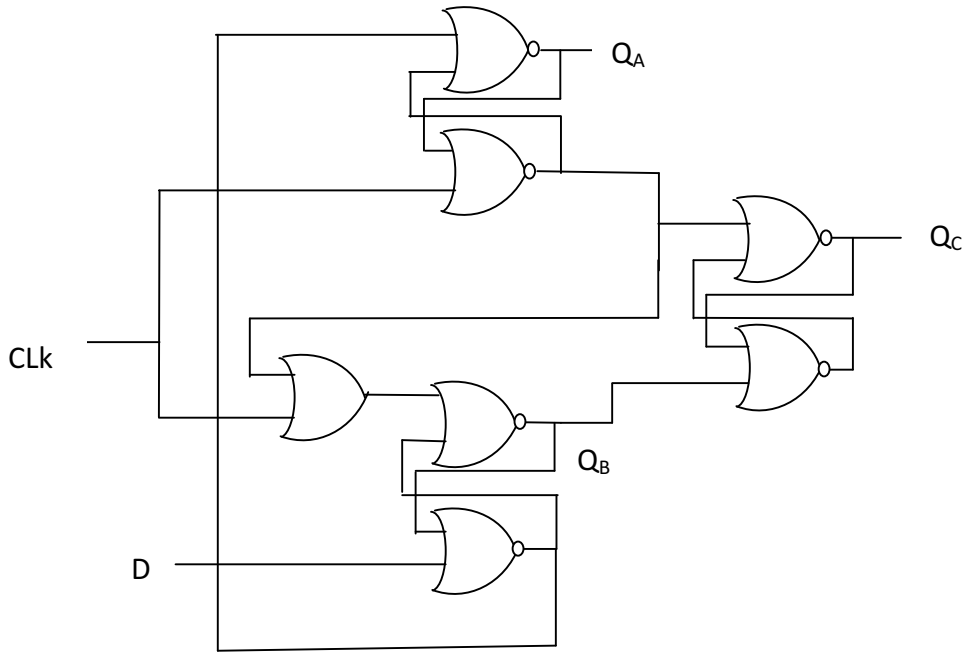
Input W X Y Z	Hex Digit	ASCII Code for Hex Digit A_6 A_5 A_4 A_3 A_2 A_1 A_0
0 0 0 0	0	0 1 1 0 0 0 0
0 0 0 1	1	0 1 1 0 0 0 1
0 0 1 0	2	0 1 1 0 0 1 0
0 0 1 1	3	0 1 1 0 0 1 1
0 1 0 0	4	0 1 1 0 1 0 0
0 1 0 1	5	0 1 1 0 1 0 1
0 1 1 0	6	0 1 1 0 1 1 0
0 1 1 1	7	0 1 1 0 1 1 1
1 0 0 0	8	0 1 1 1 0 0 0
1 0 0 1	9	0 1 1 1 0 0 1
1 0 1 0	A	1 0 0 0 0 0 1
1 0 1 1	B	1 0 0 0 0 1 0
1 1 0 0	C	1 0 0 0 0 1 1
1 1 0 1	D	1 0 0 0 1 0 0
1 1 1 0	E	1 0 0 0 1 0 1
1 1 1 1	F	1 0 0 0 1 1 0

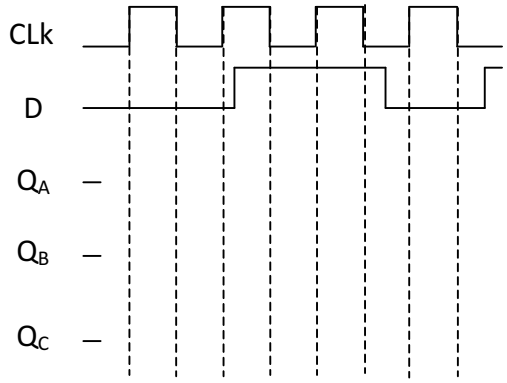




Example of PAL structure

5. This is an optimal implementation for master-slave flip flops. It only requires 7 2-input gates. Please draw the waveform for QA ,QB ,QC according to the waveform of the clock and b of the following circuit. Assume QA ,QB , and QC = 0 initially. **(20%)**





6. (20%)(you can choose either (a) or (b) below, but not both.)

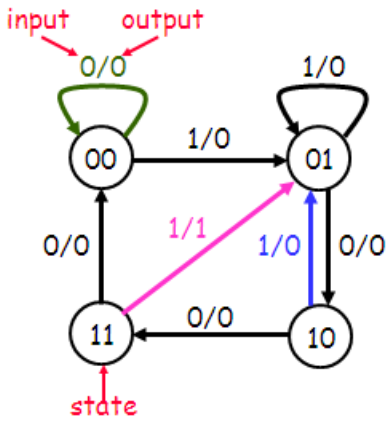
(a) (20%) A sequential circuit has two D flip-flops A, B, and two input X, Y

The circuit is described by the following input equations:

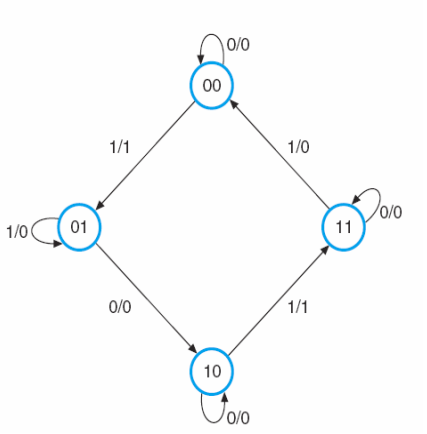
$D_A = X'A + XY$ $D_B = X'A + XB$ $Z = XB$ where X' is the compliment of X

Please first draw the circuit and derive the state table, and then draw the state diagram.

(b) (20%)Please design the synchronous schematic of the given state diagram (a) by using positive edge clock trigger JK flip-flop, state diagram (b) by using positive edge trigger clock D flip-flop. **(20%)**



(a)



(b) wo

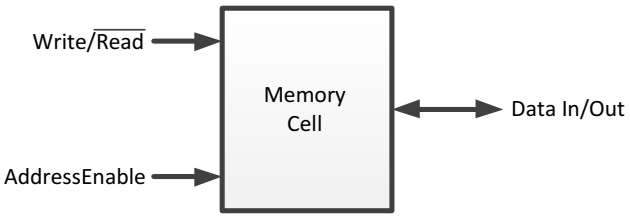
Output Transitions			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N: Present State
Q_{N+1}: Next State
X: "don't care"

Output Transitions			Flip-Flop Inputs
Q_N		Q_{N+1}	D
0	→	0	0
0	→	1	1
1	→	0	0
1	→	1	1

Q_N: Present State
Q_{N+1}: Next State
X: "don't care"

7. Please design the circuits as follows:
   (a), Using D type latch to design a one-bit memory cell with a Data_IO signal, a AddressEnable signal and a RW signal, which store the data at Data_IO to memory when both RW signal and AddressEnable is high. Output the stored data to Data_IO when RW is low and Address. **(5%)**



   (b), Design a schematic for Z = ABC + AD + C'D using only 2-input NAND gates. Use as few gates as possible. **(5%)**
   (c) Implement ABDE' + A'B' + C using three 3-input-NOR and one 2-input-NOR gates. Note: your input can be A, A', B, B', C, C', D, D', E and E' but output is F. **(4%)**

8. Consider the two Boolean functions, F1 and F2, given by the following truth table:

	x	y	z	F_2	F_2'	F_1	F_1'
0	0	0	0	0	1	0	1
1	0	0	1	1	0	0	1
2	0	1	0	0	1	0	1
3	0	1	1	0	1	1	0
4	1	0	0	1	0	0	1
5	1	0	1	0	1	1	0
6	1	1	0	0	1	1	0
7	1	1	1	1	0	1	0

   (a) Express F1 & F2 in its sum-of-product canonical form. **(4%)**
   (b) Express F1 & F2 in its product-of- sum canonical form. **(4%)**

9. Consider a simple car alarm system involving three sensors. "G" is 0 or 1 if the ignition is OFF or ON, respectively. "D" is 0 if all doors are CLOSED and 1 if any door is OPEN. "L" is 0 or 1 if the headlights are OFF or ON, respectively. The output "ALARM" should be 1 (HIGH) in the following cases:
   1. The headlights are ON while the ignition is OFF.
   2. Any door is OPEN while the ignition is ON.
   (a) Build the truth table (G,D,L, ALARM), construct the K-map, and derive the simplified sum-of-products expression for ALARM. **(4%)**
   (b) Implement the ALARM function using exactly four 2-input NAND gates. Do not use complemented inputs. **(4%)**