NTU CISE Digital System and Labs 2014 MIDTERM (2014-04-23)

. (12%) Convert the following Boolean expressions or K-map into **Sum of Products** with the indicated number of literals. Recall that a literal is either a variable or its negation.

(Hint: You may use K-map to speed up the computing)

i) F (A, B, C, D) = Σ (2, 3, 10, 11, 12, 13, 14, 15) (reduce to 4 literals)

ii) A'C' + ABC + AC' (reduce to 3 literals)

iii) A'B(D' + C'D) + B(A + A'CD) (reduce to 1 literal)

iv) (B' + A) • (B + C) (reduce to 4 literals)

v)

C \ AB	00	01	11	10
00	0	0	0	0
01	1	0	0	1
11	1	0	0	1
10	1	1	1	1

(reduce to 4 literals)

vi)

C \ AB	00	01	11	10
00	X	0	0	1
01	0	X	0	1
11	0	0	X	X
10	1	0	0	X

(reduce to 4 literals)

(10%) Consider the 5-bit binary equation "comparator" : The first 2-bit is input A, the third bit is operator bit C where 0 means "add" while 1 means "subtract", and the last 2-bit is input B. Both A and B are binary signed integer. If the equation occurs overflow (cannot be represented by 2-bit binary signed integer), the ouput K will be 1, otherwise, K will be 0.

For example: 11 0 10 = -1 + (-2) = -3 (overflow), output = 1
00 1 11 = 0 – (-1) = 1 (safe), output = 0

i) Draw the K-map for K

ii) Write the Boolean expressions for the output K

(3%) (a) Demonstrate that a 2-bit NOR gate is a universal logic element. You can do this by showing how they can be used to make: NOT, AND, OR, and XOR gates.

(6%) (b) Is an XOR gate a universal logic element? Why or why not?

(3%) (c) What about a 2-input NAND gate?

ote that each input of the NOR gate must be used, it cannot be left unconnected.

(12%) You are a testing assistant in the bulb factory. The factory has just produced 256 new bulbs numbered from 0 to 255 in binary number and needs you to examine them. So you design a series of tests shown as below. If the bulb checked in some round, the entry of the bulb should be set as 1, or 0 if unchecked. But this list is a waste of paper, the boss ask you to simplify the list to Boolean function. Please satisfy his requirement.

No.	Binary number $[N_7N_6\ldots N_0]$	R_0	R_1	……	R_n
0	00000000	1			
1	00000001	1			
2	00000010	1			
3	00000011	1			
. .	. .	. .	. .	. .	. .
254	11111110	0			
255	11111111	0			

For instance, you have tested the first 4 bulbs (No.0 ~ No.3) bulbs in Round 0, so you write down the Boolean function as $R_0 = \overline{N_7} \cdot \overline{N_6} \cdot \overline{N_5} \cdot \overline{N_4} \cdot \overline{N_3} \cdot \overline{N_2}$

Please finish the rest (as simple as possible):

i) R_1 = Test the even numbers

ii) R_2 = Test the multiples of 8

iii) R_3 = Divide the bulbs into quarters. Test the 2^{nd} and the 3^{rd} quarter

iv) R_4 = Test all except for the last 32 bulbs

v) R_5 = Test all except for the multiple of 16

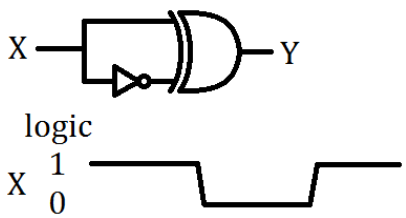
vi) R_6 = Test No.129 and No. 219 only

For a circuit with an inverter and an exclusive or gate, suppose that the exclusive or gate has no time delay:

(4%) (a) What the output signal Y will be like with the input signal X?

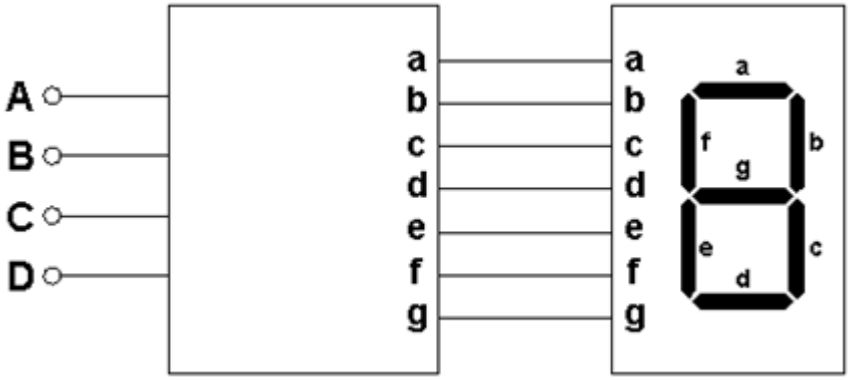
(4%) (b) Why does Y have such relationship with X?

(4%) (c) What can the circuit do in real life?



(12%) The following figure shows how the hexadecimal 7-segment display decoder works. DCBA is a 4-bit binary number input, then the decoder will transfer the binary number into segment signal. Assume that 1 is for segment "on" while 0 is segment "off".

For instance, if DCBA represent the digit "0", which means all the segment except for "g" should be on. So the decoder will send (1, 1, 1, 1, 1, 1, 0) to the 7-segment display. Answer the following questions:

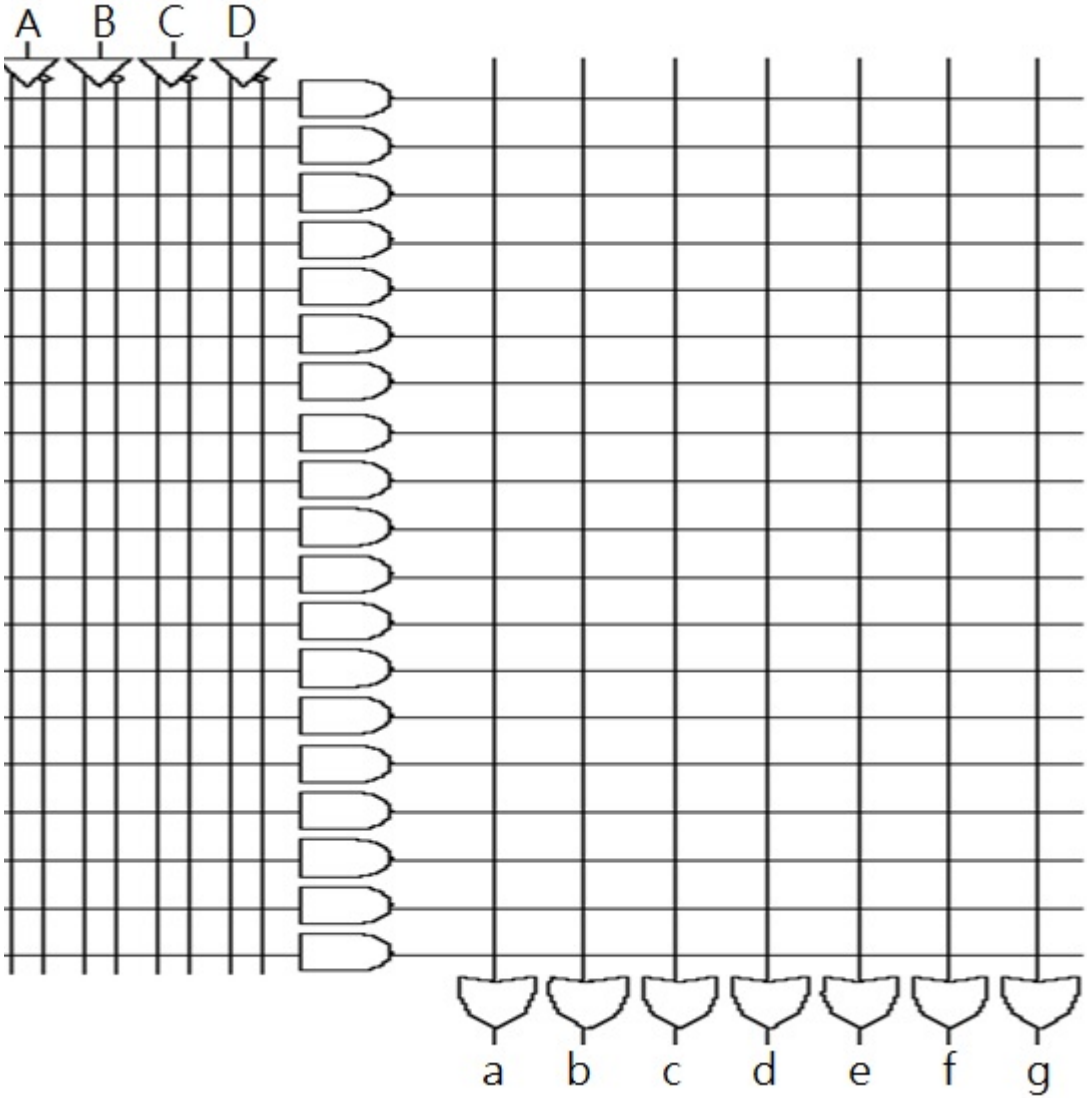


(2%) (a) If this decoder can only display decimal number (0 - 9), how many bits are needed for the input?

(2%) (b) How many bits for the input of 7-segment are valid **at most**?

(4%) (c) Write the truth table for this **hexadecimal** 7-segment display system

(4%) (d) Draw the PLA implementation of this decoder in the following template



(10%) Find a function to detect an error in the representation of a decimal digit in BCD. In other words, write an equation with value 1 when the input are any one of the six unused bit combinations in the BCD code (10, 11, 12, 13, 14, 15), and value 0 otherwise. Please implement it with only NAND gates and inverters.

Optional problem, you can choose either problem A or B below to answer:

oblem A:

(a) (20%) A sequential circuit has two JK flip-flops with state outputs A, B, and two input X, Y
(Note: inputs to flip-flop A are called JA, KA, while inputs to B are called JB, KB, circuit output is called Z)
The circuit is described by the following input equations:
JA = XA + XY, KA= X'Y, and JB =XA, KB = Y, Z = YB where X' is the compliment of X
Please
(i) (10%) draw the above circuit and derive the state tables,
(ii) (10%) then draw the state diagram of this circuit.

oblem B:

(b) (20%) (Verilog HDL – Code Debugging)

Identify syntax errors and inappropriate code then correct them and explain: 2pts for each error.

```
module 16x16-MAC (out, rst, op1, op2)
input clk, rst;
input [15:0] op1, op2;
output [39:0] out;
reg [31:0] product;
assign product = op1 * op2;
//40-bit accumulator after 16x16 multiplier
always @(posedge clk || negedge rst)
  if(rst) out= 0;
  else out = out + product;
endmodules
```