DSDL Midterm

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1. (5%) Please calculate following translate

(a) $(11010.11)_2 = (\quad)_{10}$

(b) $(41)_{10} = (\quad)_2$

(a) $(11010.11)_2 = (2^4+2^3+2^1+2^{-1}+2^{-2})_{10} = (16+8+2+0.5+0.75)_{10} = (26.75)_{10}$.

(b) $(41)_{10} = (32+8+1)_{10} = (2^5+2^3+2^0)_{10} = (101001)_2$

2. (10%) Prove the identity of each of the following Boolean equations, using algebraic manipulation.

(a) $(A+B)(\bar{A}+C)(B+C)=(A+B)(\bar{A}+C)$

(b) $AB+AC+BC=\overline{(A+B)(A+C)(B+C)}$

(a) $(A+B)(\bar{A}+C)(B+C)$

$=(A\bar{A}+AC+\bar{A}B+BC)(B+C)$

$=ABC+\bar{A}B+BC+AC+\bar{A}BC$

$=BC+\bar{A}B+AC$

$=BC+\bar{A}B+AC+A\bar{A}$

$=(A+B)(\bar{A}+C)$

(b) $\overline{(A+B)(A+C)(B+C)}$

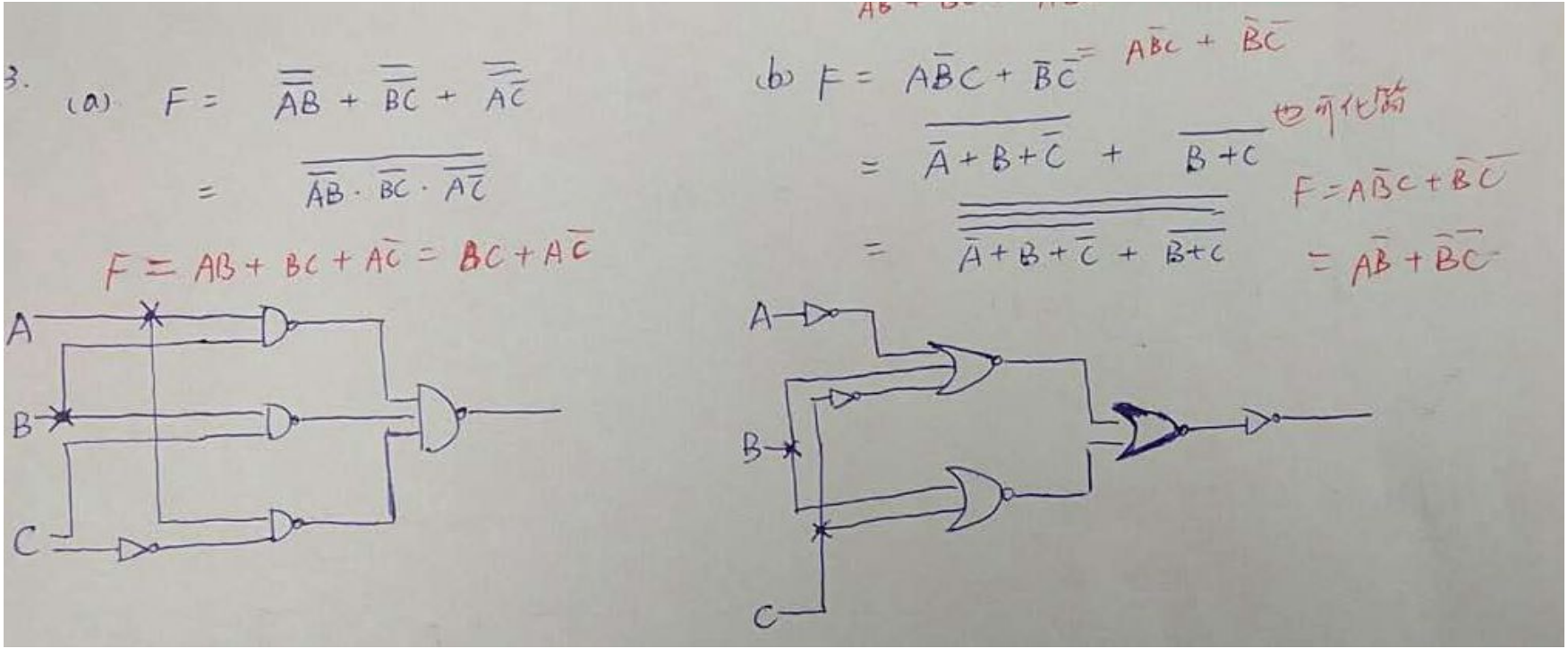
$=\overline{A+B}+\overline{A+C}+\overline{B+C}$

$=\bar{A}\cdot\bar{B}+\bar{A}\cdot\bar{C}+\bar{B}\cdot\bar{C}$

3. (20%) Please draw the logic circle design of following Boolean functions.

(a) $F = AB + BC + A\overline{C}$ (logic circle design only use NAND and NOT gates)

(b) $F = A\overline{B}C + \overline{B}\overline{C}$ (logic circle design only use NOR and NOT gates)

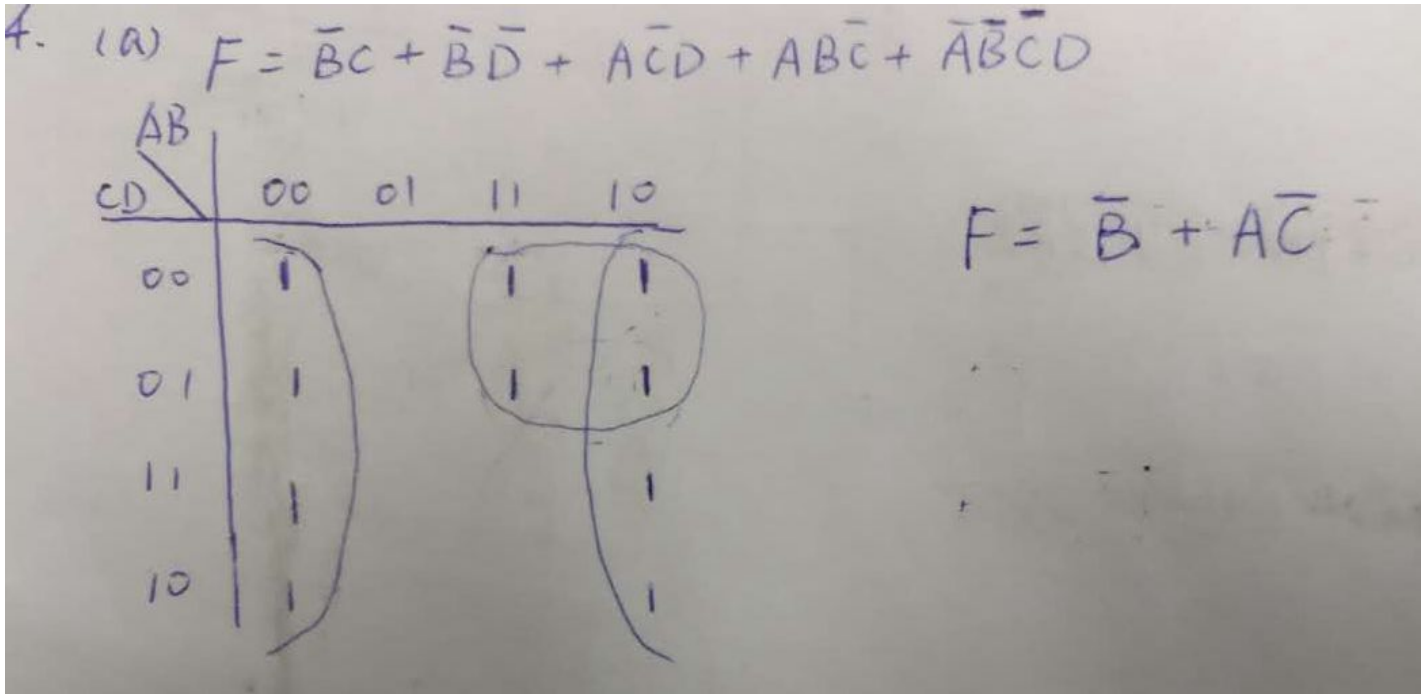


4. (15%) Use the K-map method to find the minimized sum-of-product expressions:

(a) $F = \overline{B}C + \overline{B}\overline{D} + A\overline{C}D + AB\overline{C} + \overline{A}\overline{B}\overline{C}D$

(b) $F(A,B,C,D) = \sum m(1,7,9,10,11,12,13,15)$

(c) $F(A,B,C,D) = \sum m(5,6,9,10) + \sum d(0,1,2,13,14,15)$



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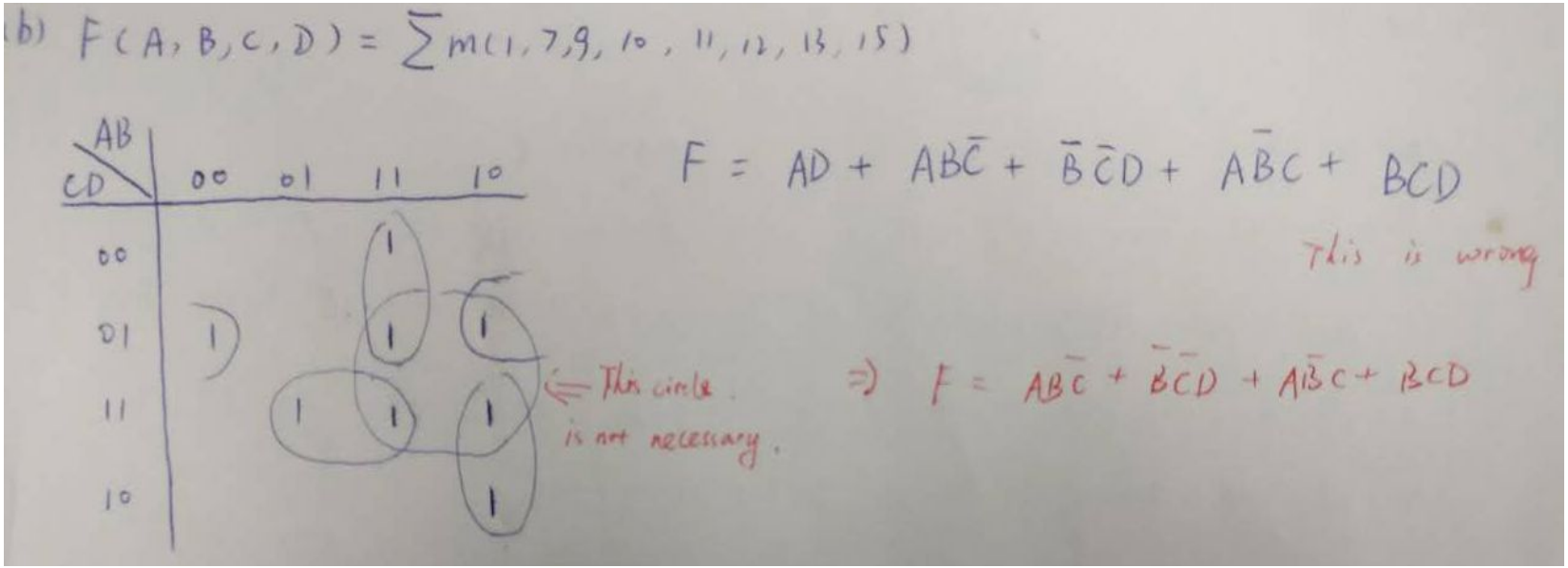

4. (15%) Use the K-map method to find the minimized sum-of-product expressions:

(a) $F = \overline{B}C + \overline{B}\overline{D} + A\overline{C}D + AB\overline{C} + \overline{A}\overline{B}\overline{C}D$

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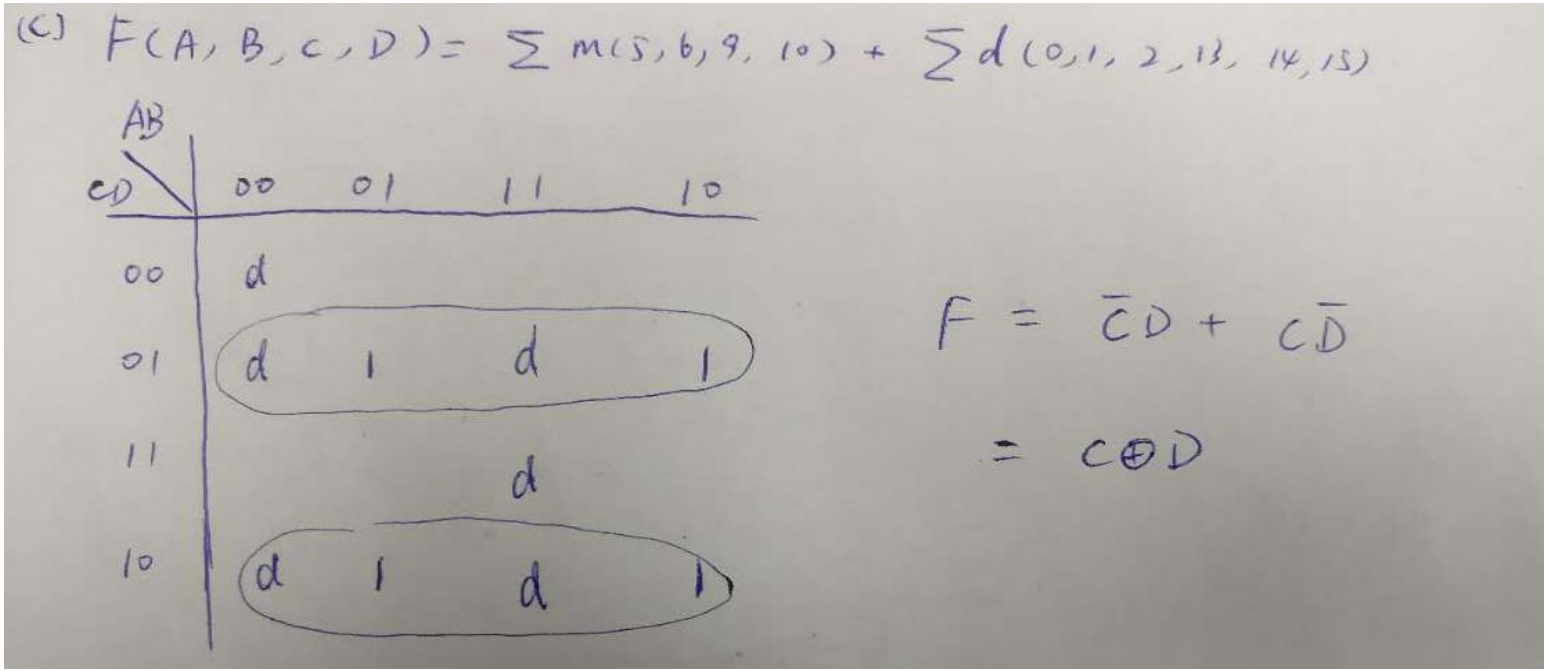


5. (15%) Implement the following functions using decoders and any size OR gates you may need:

(a) F(P,Q,R) = (PQ+R)' using a 3:8 decoder

(b) F(P,Q,R,S,T) = P'Q'R'(S+T) using a 2:4 decoder

5. (a) $F(P,Q,R) = (PQ+R)'$

$= (PQ)' \cdot R'$

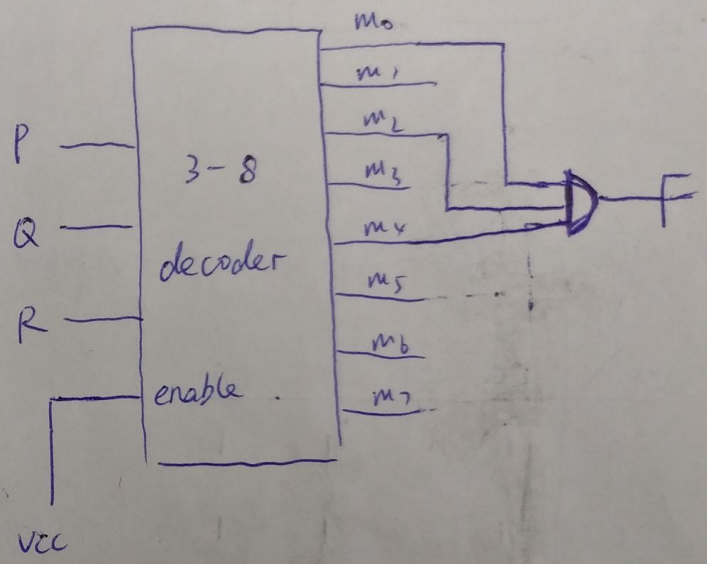
$= (P'+Q') \cdot R'$

$= P'R' + Q'R'$

$= P'QR' + P'Q'R' + PQ'R' + P'Q'R'$

$= P'QR' + PQ'R' + P'Q'R'$

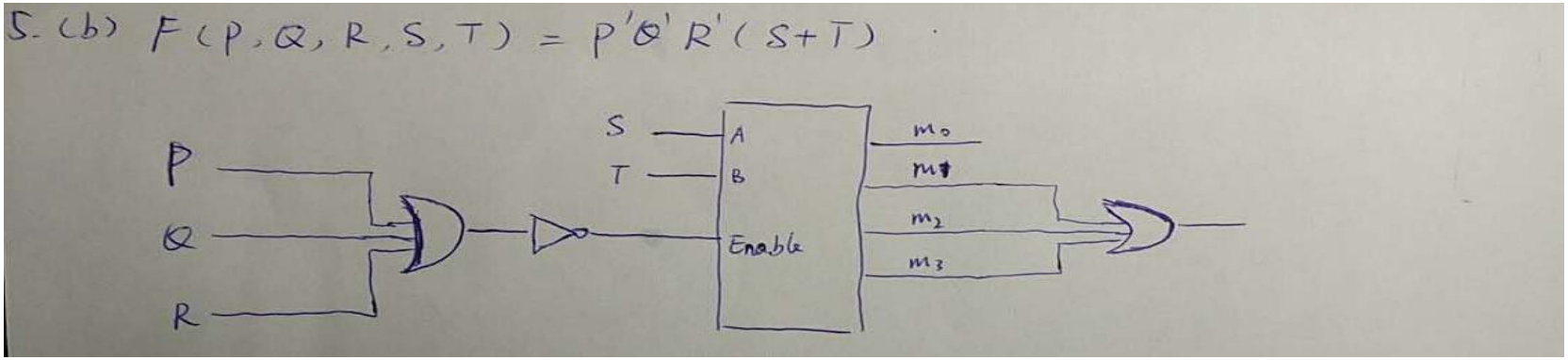
$= \sum m(0,2,4)$

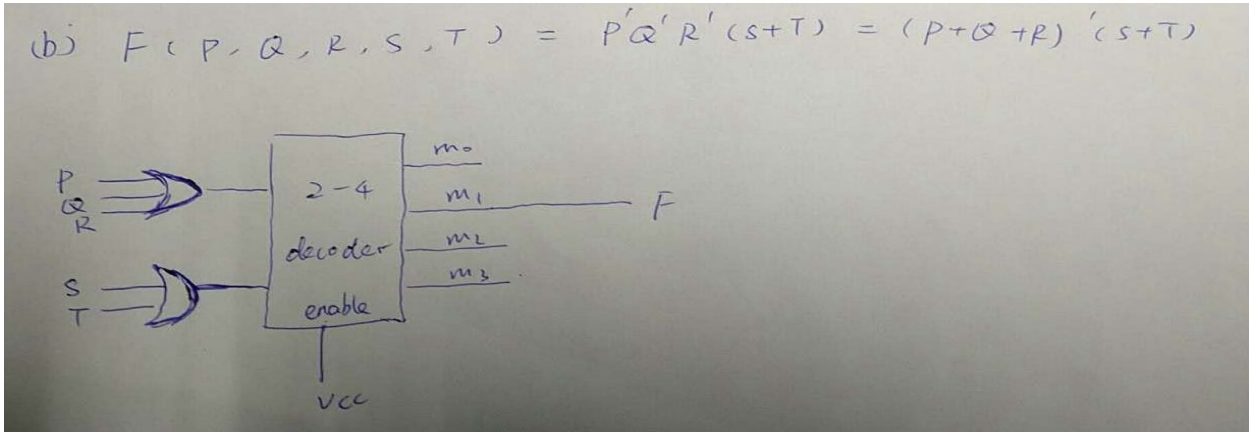


5. (15%) Implement the following functions using decoders and any size OR gates you may need:

(a) F(P,Q,R) = (PQ+R)' using a 3:8 decoder

(b) F(P,Q,R,S,T) = P'Q'R'(S+T) using a 2:4 decoder



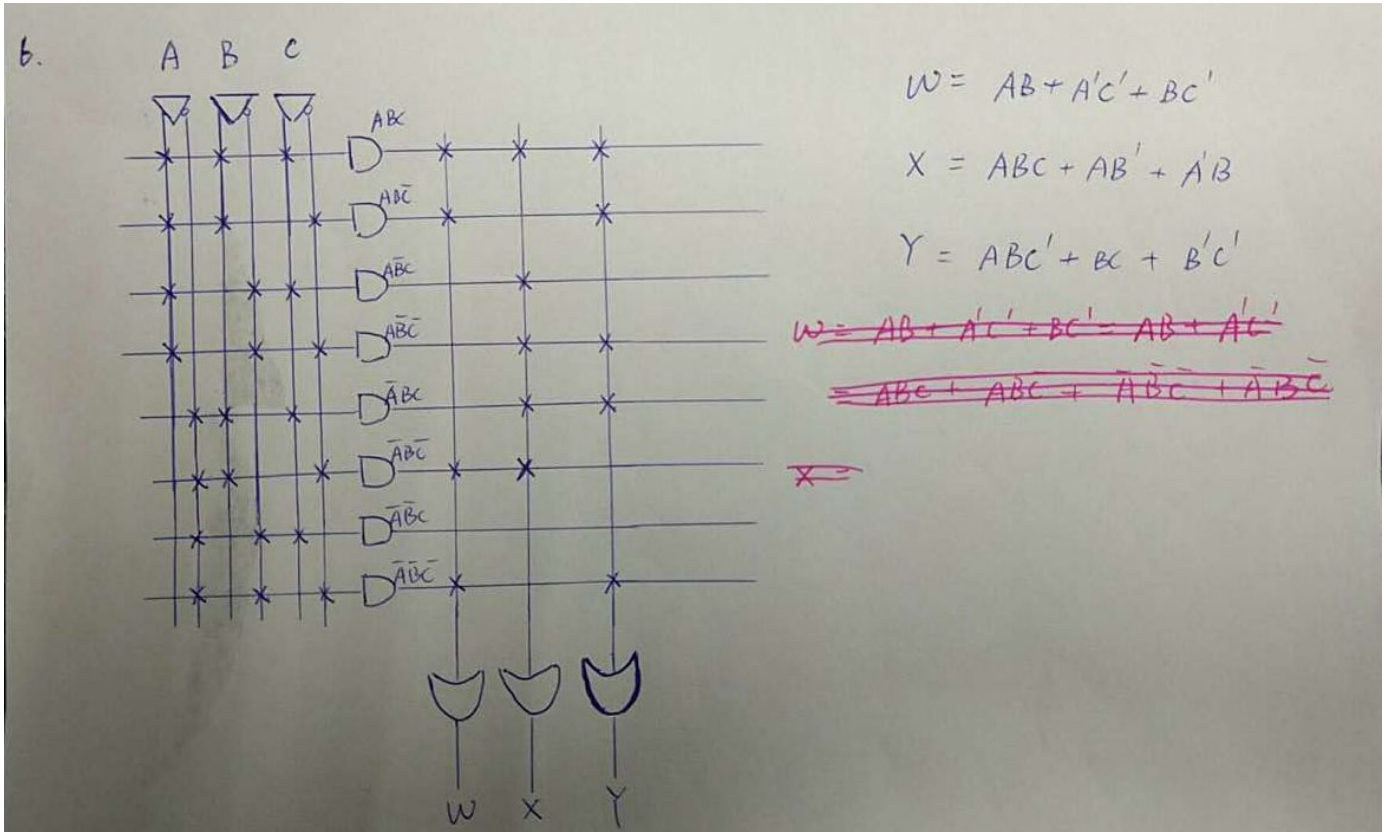


6. (15%) Map the following functions to the PLA below:

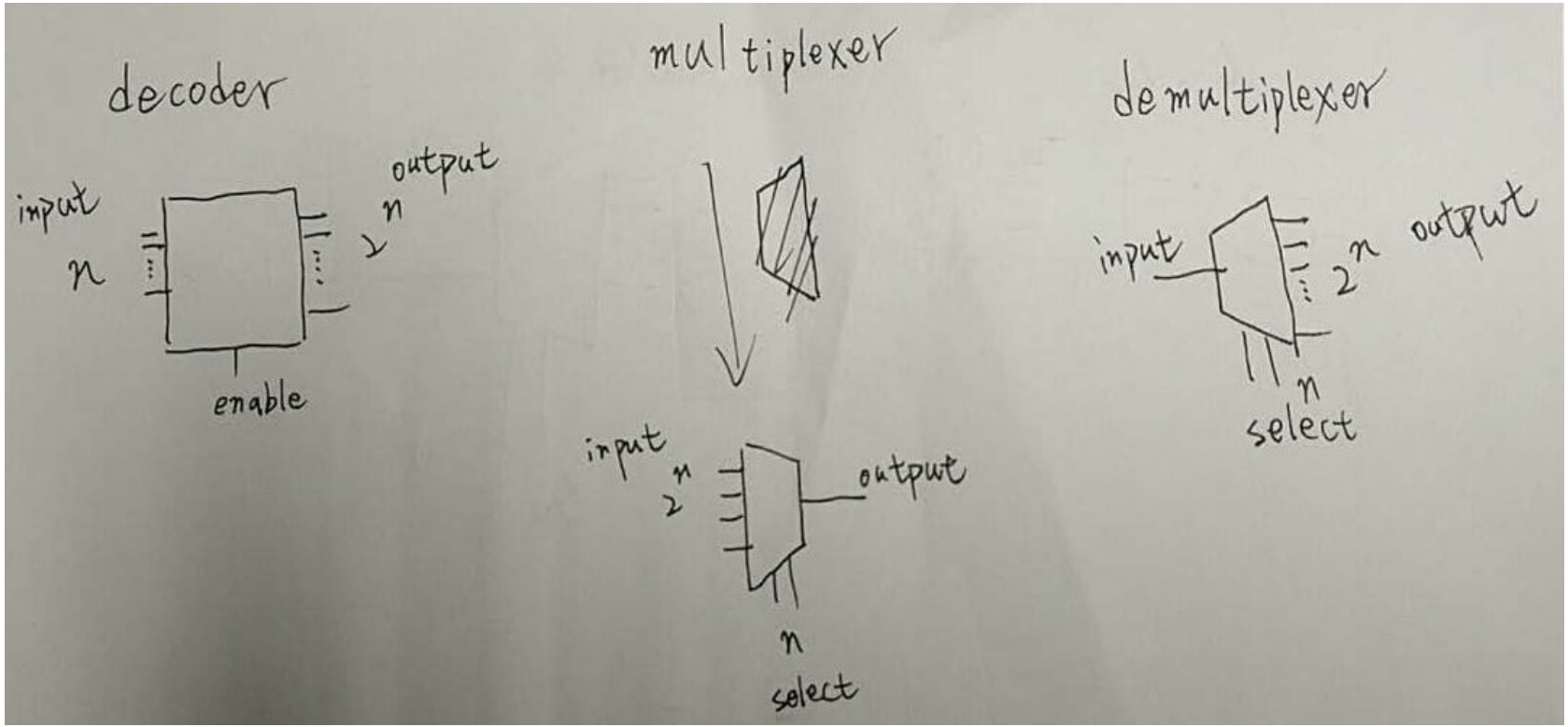
W = AB + A'C' + BC'

X = ABC + AB' + A'B

Y = ABC' + BC + B'C'



7. (10%) Define and differentiate the following terms: decoder, demultiplexer, and multiplexer. Mention the number of inputs, outputs, enable, and select bits, if any.



8. （10%）(Verilog HDL) Take a look at the following Verilog program.

a. (3%) Can a Verilog module name start with a number?

b. (4%) Do “clk” below need to be declared in the parameter list?

c. (3%) Should the module end with “endmodule” or “endmodules”?

```
module 16x16-MAC (out, rst, op1, op2)
input clk, rst;
input [15:0] op1, op2;
output [39:0] out;
reg [31:0] product;
assign product = op1 * op2;
//40-bit accumulator after 16x16 multiplier
always @(posedge clk || negedge rst)
  if(rst) out = 0;
  else out = out + product;
endmodules
```