

8. (Verilog HDL – Code Debugging: 15pts)

Identify syntax errors and inappropriate code then correct them and explain: 1.5pts for each error.

```
module 16x16-MAC (out, rst, op1, op2)

input clk, rst;

input [15:0] op1, op2;

output [39:0] out;

reg [31:0] product;

assign product = op1 * op2;

//40-bit accumulator after 16x16 multiplier

always @(posedge clk || negedge rst)

    if(rst) out= 0;

    else out = out + product;

endmodules
```

8. (Verilog HDL – Code Debugging: 15pts)

Identify syntax errors and inappropriate code then correct them and explain: 1.5pts for each error.

```
module 16x16-MAC (out, clk, reset, op1, op2) ;

// module name cannot be started with number, and ended with ";"

input clk, reset;

input [15:0] op1, op2;

output [39:0] out;

reg [39:0] out;

wire [31:0] product;

assign product = op1 * op2;

//40-bit accumulator after 16x16 multiplier

always @(posedge clk or negedge reset)

    if(!reset) out <= 0;

    else out <= out + product;

endmodule
```