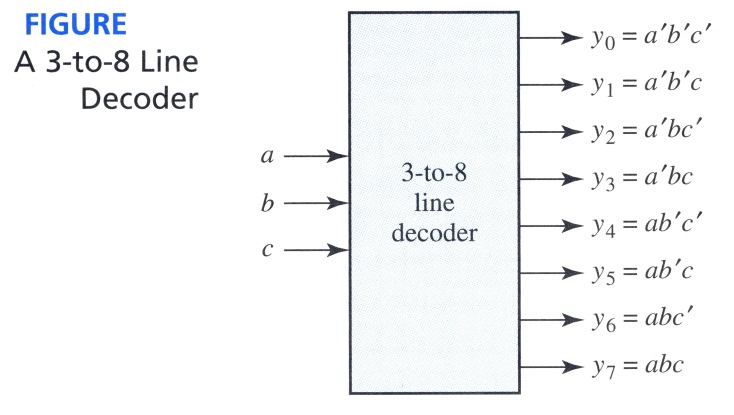
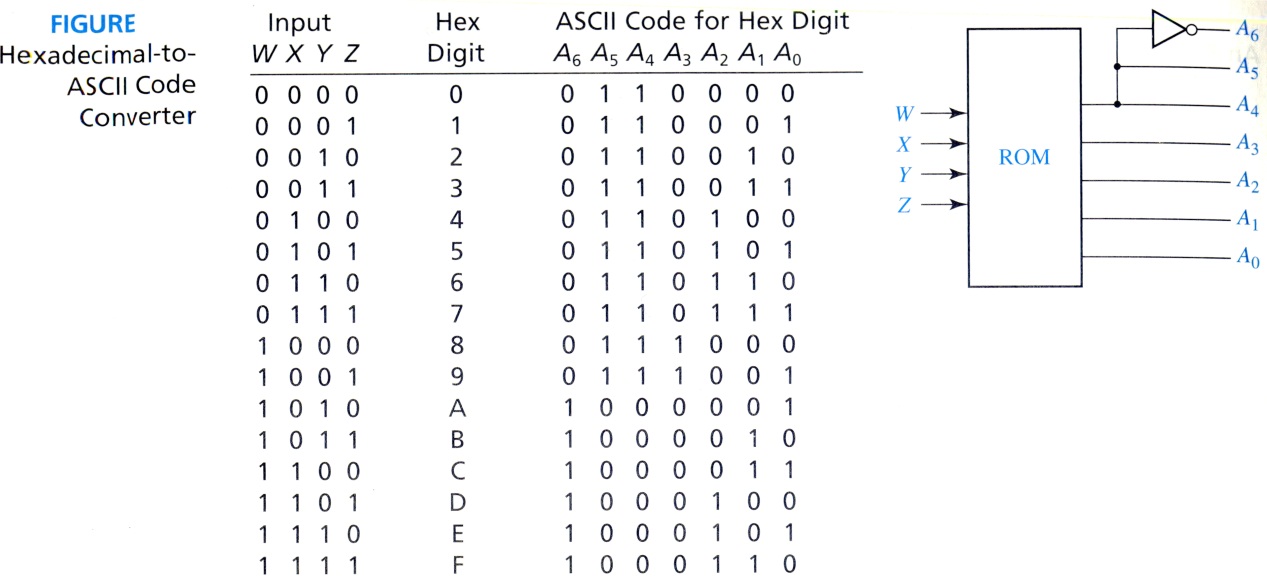
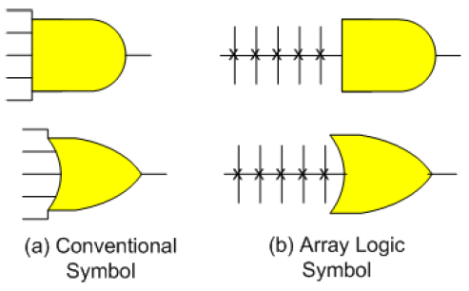
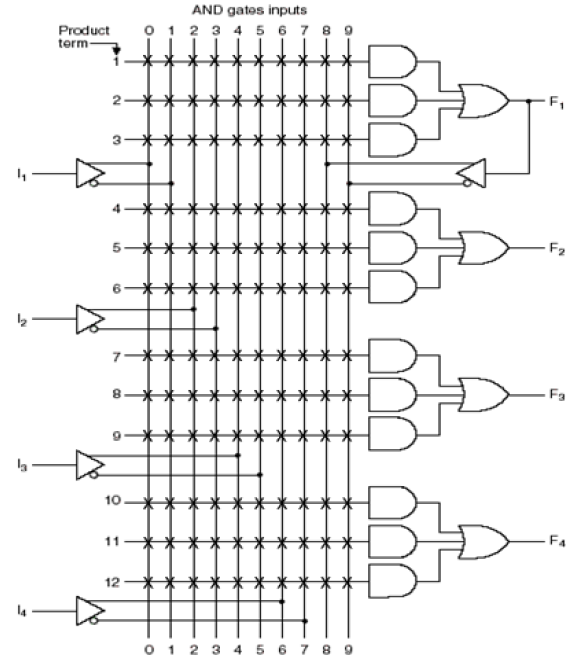
**DSD Midterm exam 11/16 2011**

1. Use the K-map method to find the minimized sum-of-product expression for each F: **(8%)**
2. **(4%)**
3. **(4%)**
4. Hazards in circuit design: **(12%)**
5. There are two kinds of static hazards, what are they? Give an example of a static hazard and explain how to avoid it. **(8%)**
6. Give an example to illustrate when will a dynamic hazard occur? **(4%)**
7. Realize an one-bit full adder using a 3-to-8 line decoder as Fig 1 below and
8. Two **OR** gates. **(5%)**
9. Two **NOR** gates. **(5%)**



1. If the ROM in the hexadecimal to ASCII code converter of FIGURE is replaced with a PAL, give the internal connection diagram. **(20%)**





Example of PAL structure

1. This is an optimal implementation for master-slave flip flops. It only requires 7 2-input gates. Please draw the waveform for QA ,QB ,QC according to the waveform of the clock and b of the following circuit. Assume QA ,QB , and QC = 0 initially. **(20%)**

QA

CLk

QC

QB

D

CLk

D

QA

QB

QC

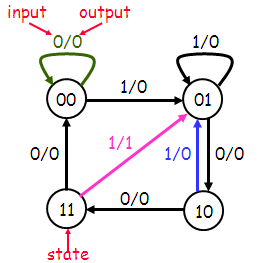
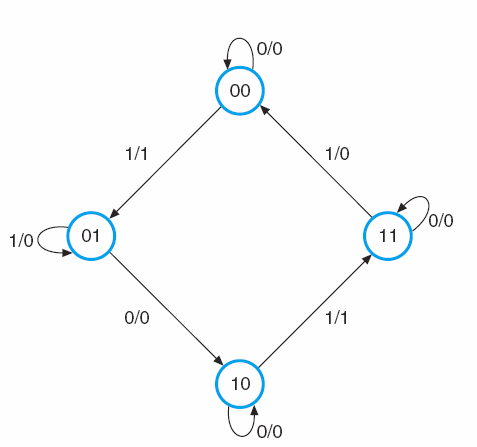
1. (20%)(you can choose either (a) or (b) below, but not both.)
2. (20%) A sequential circuit has two D flip-flops A, B, and two input X, Y

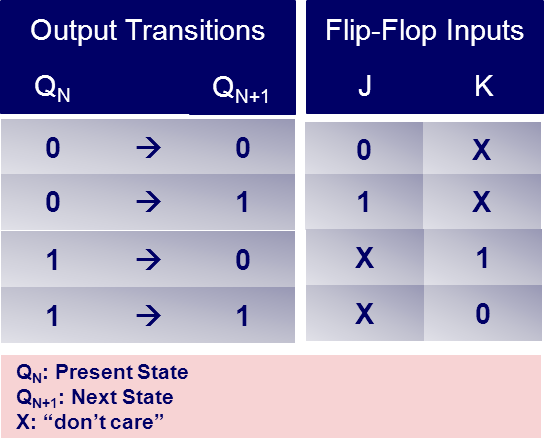
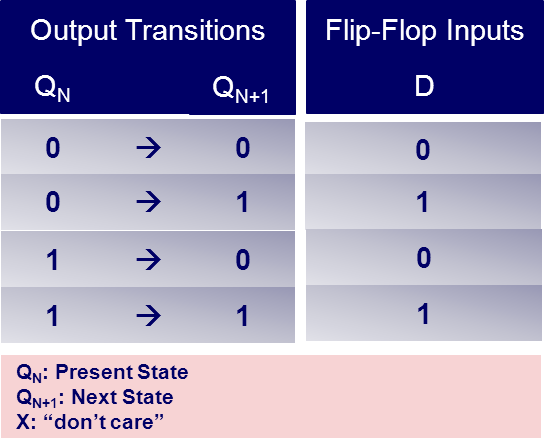
The circuit is described by the following input equations:

DA = X’A + XY DB = X’A + XB Z = XB where X’ is the compliment of X

Please first draw the circuit and derive the state table, and then draw the state diagram.

(b) (20%)Please design the synchronous schematic of the given state diagram (a) by using positive edge clock trigger JK flip-flop, state diagram (b) by using positive edge trigger clock D flip-flop. **(20%)**

(a) (b) wo 

1. Please design the circuits as follows:

(a), Using D type latch to design a one-bit memory cell with a Data\_IO signal, a AddressEnable signal and a RW signal, which store the data at Data\_IO to memory when both RW signal and AddressEnable is high. Output the stored data to Data\_IO when RW is low and Address. **(5%)**



(b), Design a schematic for Z = ABC + AD + C’D using only 2-input NAND gates. Use as few gates as possible. **(5%)**  
(c) Implement ABDE’ + A’B’ + C using three 3-input-NOR and one 2-input-NOR gates. Note: your input can be A, A’, B, B’, C, C’, D, D’, E and E’ but output is F. **(4%)**

1. Consider the two Boolean functions, F1 and F2, given by the following truth table:  
     
   (a) Express F1 & F2 in its sum-of-product canonical form. **(4%)**  
   (b) Express F1 & F2 in its product-of- sum canonical form. **(4%)**
2. Consider a simple car alarm system involving three sensors. “G” is 0 or 1 if the ignition is OFF or ON, respectively. “D” is 0 if all doors are CLOSED and 1 if any door is OPEN. “L” is 0 or 1 if the headlights are OFF or ON, respectively. The output “ALARM” should be 1 (HIGH) in the following cases:  
   1. The headlights are ON while the ignition is OFF.  
   2. Any door is OPEN while the ignition is ON.  
   (a) Build the truth table (G,D,L, ALARM), construct the K-map, and derive the simplified sum-of-products expression for ALARM. **(4%)**  
   (b) Implement the ALARM function using exactly four 2-input NAND gates. Do not use complemented inputs. **(4%)**