



Microprocessor & Computer Architecture
MPCA-Laboratory
UE20CS252

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Section : K

Programs

1. Write a program in ARM7TDMI-ISA to copy a block of N data items from Location A to Location B.
a. Use Half word (.Hword directive)

NOTEPAD FILE:

W2P11.s - Notepad

File Edit Format View Help

.DATA

A: .HWORD 10,20,30,40,50

B: .HWORD 0,0,0,0,0

.TEXT

LDR R1,=A

LDR R2,=B

MOV R5,#1 ;counter

L1:LDRH R3,[R1]

STRH R3,[R2]

ADD R1,R1,#2

ADD R2,R2,#2

ADD R5,R5,#1

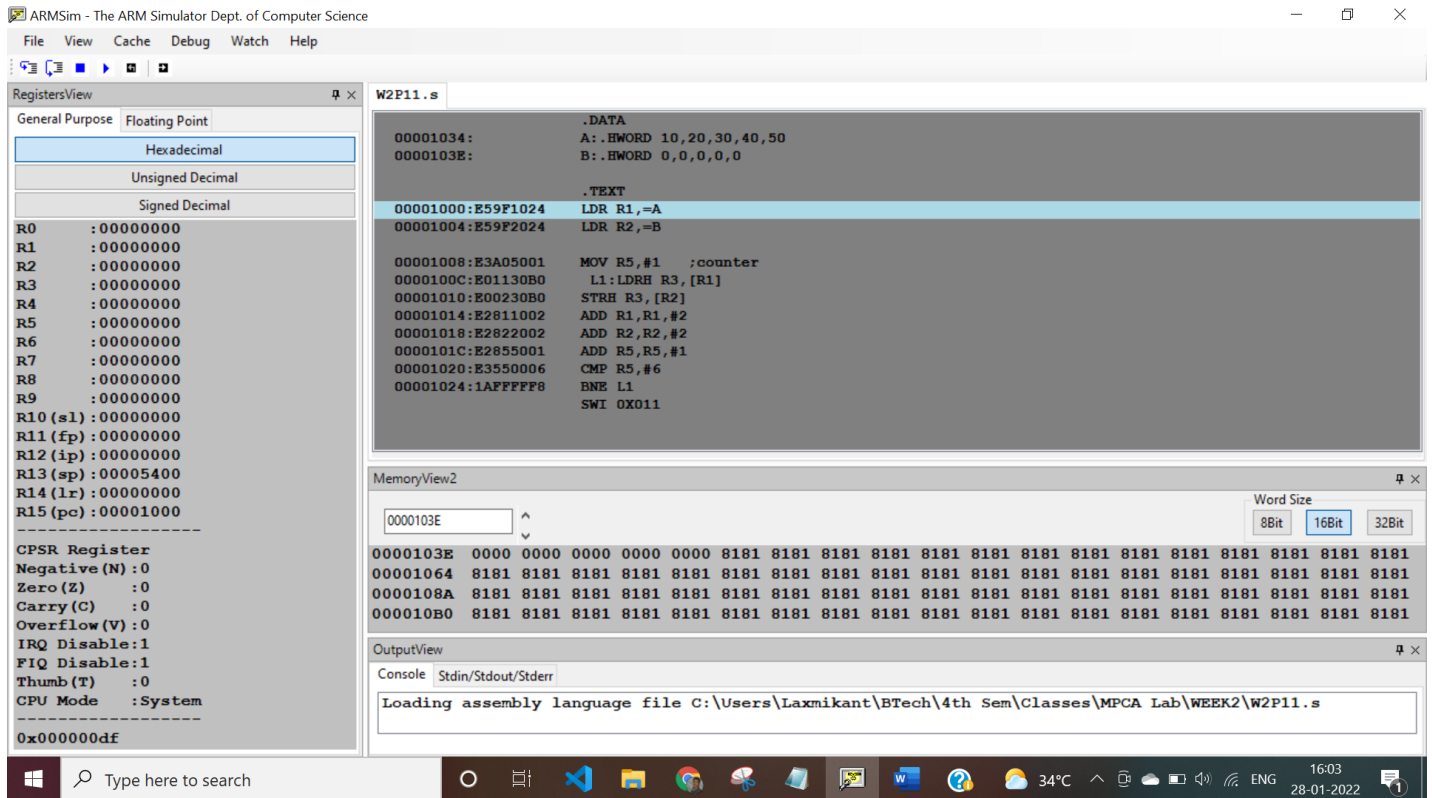
CMP R5,#6

BNE L1

SWI 0X011

OUTPUT SCREENSHOT:

Before execution:



The screenshot shows the ARMSim interface before execution. The RegistersView window displays the initial state of the registers, with R0 through R15 all set to 0x00000000. The CPSR Register shows the system mode. The MemoryView2 window shows the initial memory state, with the first 16 bytes of memory (0x00000000 to 0x0000000F) all set to 0x00000000. The OutputView window shows the console output, which is empty.

RegistersView

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 00000000
R1 : 00000000
R2 : 00000000
R3 : 00000000
R4 : 00000000
R5 : 00000000
R6 : 00000000
R7 : 00000000
R8 : 00000000
R9 : 00000000
R10 (s1) : 00000000
R11 (fp) : 00000000
R12 (ip) : 00000000
R13 (sp) : 00005400
R14 (lr) : 00000000
R15 (pc) : 00001000

CPSR Register

Negative (N) : 0
Zero (Z) : 0
Carry (C) : 0
Overflow (V) : 0
IRQ Disable : 1
FIQ Disable : 1
Thumb (T) : 0
CPU Mode : System

0x000000df

W2P11.s

.DATA
00001034: A: .HWORD 10,20,30,40,50
0000103E: B: .HWORD 0,0,0,0,0

.TEXT
00001000:E59F1024 LDR R1,=A
00001004:E59F2024 LDR R2,=B

00001008:E3A05001 MOV R5,#1 ;counter
0000100C:E01130B0 L1:LDHR R3,[R1]
00001010:E00230B0 STRH R3,[R2]
00001014:E2811002 ADD R1,R1,#2
00001018:E2822002 ADD R2,R2,#2
0000101C:E2855001 ADD R5,R5,#1
00001020:E3550006 CMP R5,#6
00001024:1AFFFFF8 BNE L1
SWI 0X011

MemoryView2

Word Size 8Bit 16Bit 32Bit

0000103E 0000 0000 0000 0000 0000 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181

00001064 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181

0000108A 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181

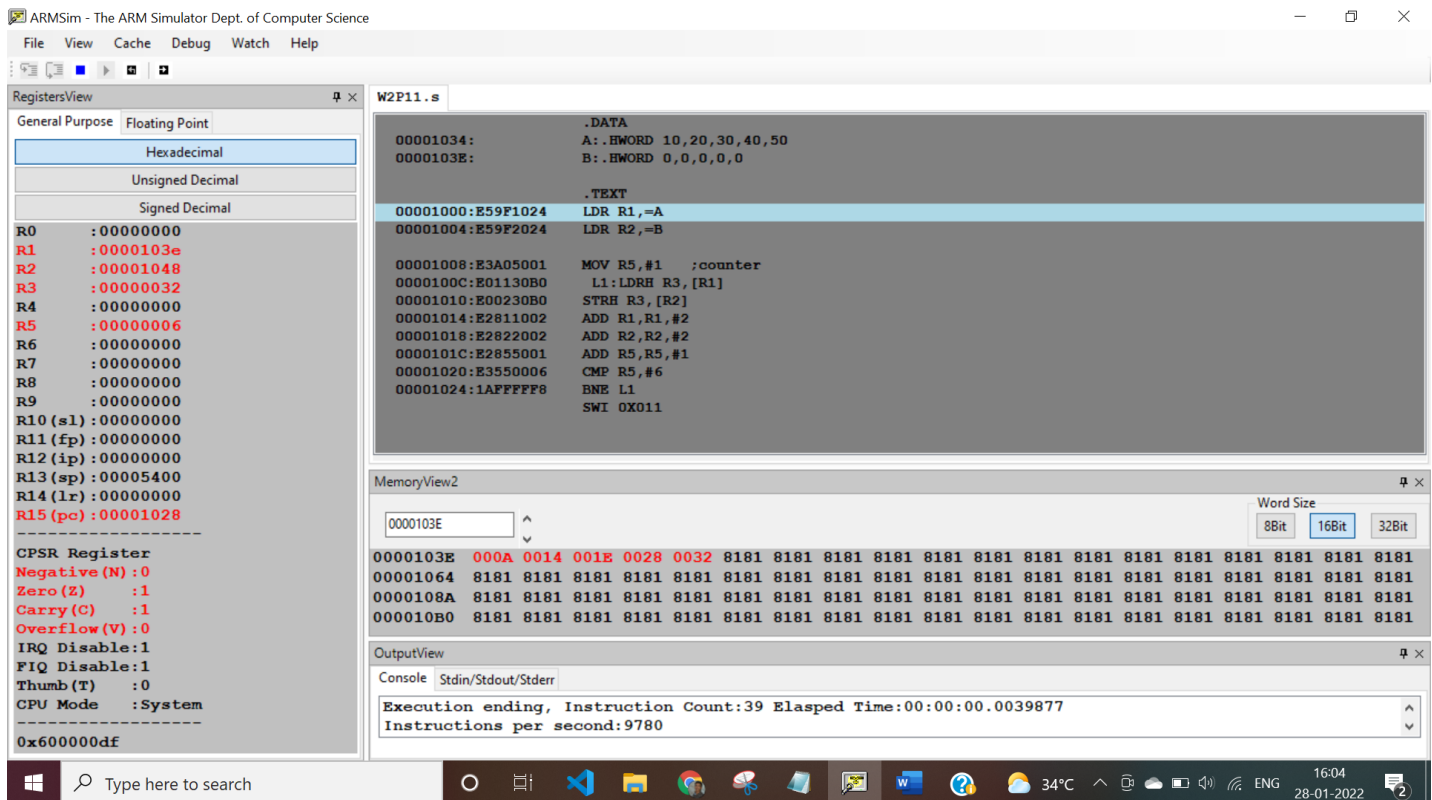
000010B0 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181

OutputView

Console Stdin/Stdout/Stderr

Loading assembly language file C:\Users\Laxmikant\BTech\4th Sem\Classes\MPCA Lab\WEEK2\W2P11.s

After execution:



The screenshot shows the ARMSim interface after execution. The RegistersView window displays the final state of the registers. R0 is 0x00000000, R1 is 0x0000103e, R2 is 0x00001048, R3 is 0x00000032, R4 is 0x00000000, R5 is 0x00000006, R6 is 0x00000000, R7 is 0x00000000, R8 is 0x00000000, R9 is 0x00000000, R10 (s1) is 0x00000000, R11 (fp) is 0x00000000, R12 (ip) is 0x00000000, R13 (sp) is 0x00005400, R14 (lr) is 0x00000000, and R15 (pc) is 0x00001028. The CPSR Register shows the system mode. The MemoryView2 window shows the final memory state, with the first 16 bytes of memory (0x00000000 to 0x0000000F) all set to 0x00000000. The OutputView window shows the console output, which includes the execution ending message and the instruction count and elapsed time.

RegistersView

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 00000000
R1 : 0000103e
R2 : 00001048
R3 : 00000032
R4 : 00000000
R5 : 00000006
R6 : 00000000
R7 : 00000000
R8 : 00000000
R9 : 00000000
R10 (s1) : 00000000
R11 (fp) : 00000000
R12 (ip) : 00000000
R13 (sp) : 00005400
R14 (lr) : 00000000
R15 (pc) : 00001028

CPSR Register

Negative (N) : 0
Zero (Z) : 1
Carry (C) : 1
Overflow (V) : 0
IRQ Disable : 1
FIQ Disable : 1
Thumb (T) : 0
CPU Mode : System

0x600000df

W2P11.s

.DATA
00001034: A: .HWORD 10,20,30,40,50
0000103E: B: .HWORD 0,0,0,0,0

.TEXT
00001000:E59F1024 LDR R1,=A
00001004:E59F2024 LDR R2,=B

00001008:E3A05001 MOV R5,#1 ;counter
0000100C:E01130B0 L1:LDHR R3,[R1]
00001010:E00230B0 STRH R3,[R2]
00001014:E2811002 ADD R1,R1,#2
00001018:E2822002 ADD R2,R2,#2
0000101C:E2855001 ADD R5,R5,#1
00001020:E3550006 CMP R5,#6
00001024:1AFFFFF8 BNE L1
SWI 0X011

MemoryView2

Word Size 8Bit 16Bit 32Bit

0000103E 000A 0014 001E 0028 0032 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181

00001064 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181

0000108A 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181

000010B0 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181

OutputView

Console Stdin/Stdout/Stderr

Execution ending, Instruction Count:39 Elapsed Time:00:00:00.0039877
Instructions per second:9780

After execution:

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 00000000
R1 : 00001039
R2 : 0000103e
R3 : 00000032
R4 : 00000000
R5 : 00000006
R6 : 00000000
R7 : 00000000
R8 : 00000000
R9 : 00000000
R10 (s1): 00000000
R11 (fp): 00000000
R12 (ip): 00000000
R13 (sp): 00005400
R14 (lr): 00000000
R15 (pc): 00001028

CPSR Register
Negative (N): 0
Zero (Z): 1
Carry (C): 1
Overflow (V): 0
IRQ Disable: 1
FIQ Disable: 1
Thumb (T): 0
CPU Mode : System
0x600000df

w2p12.s

```
.DATA
00001034: A:.byte 10,20,30,40,50
00001039: B:.byte 0,0,0,0,0

.TEXT
00001000:E59F1024 LDR R1,=A
00001004:E59F2024 LDR R2,=B

00001008:E3A05001 MOV R5,#1 ;counter
0000100C:E5D13000 L1:LDRB R3,[R1]
00001010:E5C23000 STRB R3,[R2]
00001014:E2811001 ADD R1,R1,#1
00001018:E2822001 ADD R2,R2,#1
0000101C:E2855001 ADD R5,R5,#1
00001020:E3550006 CMP R5,#6
00001024:1AFFFFF8 BNE L1
SWI 0X011
```

MemoryView2

Word Size 8Bit 16Bit 32Bit

00001039

```
00001039 0A 14 1E 28 32 00 00 81 81 81 81 81 81 81 81 81 81 .. (2.....
00001050 81 81 81 81 81 81 81 81 81 81 81 81 81 81 81 81 .....
00001067 81 81 81 81 81 81 81 81 81 81 81 81 81 81 81 81 .....
0000107E 81 81 81 81 81 81 81 81 81 81 81 81 81 81 81 81 .....
```

OutputView

Console Stdin/Stdout/Stderr

```
Execution ending, Instruction Count:39 Elapsed Time:00:00:00.0069732
Instructions per second:5592
```

2. Write a program in ARM7TDMI-ISA to find the sum of N data items in the memory. Store the result in the memory location.
 - a. Use Half word (.Hword directive)

NOTEPAD FILE:

W2P22.s - Notepad

File Edit Format View Help

.DATA

A: .HWORD 10,20,30,40,50

SUM: .HWORD 0

.TEXT

LDR R1,=A

LDR R2,=SUM

MOV R4,#0

MOV R5,#1

L1:LDRH R3,[R1]

ADD R4,R4,R3

ADD R1,R1,#2

ADD R5,R5,#1

CMP R5,#6

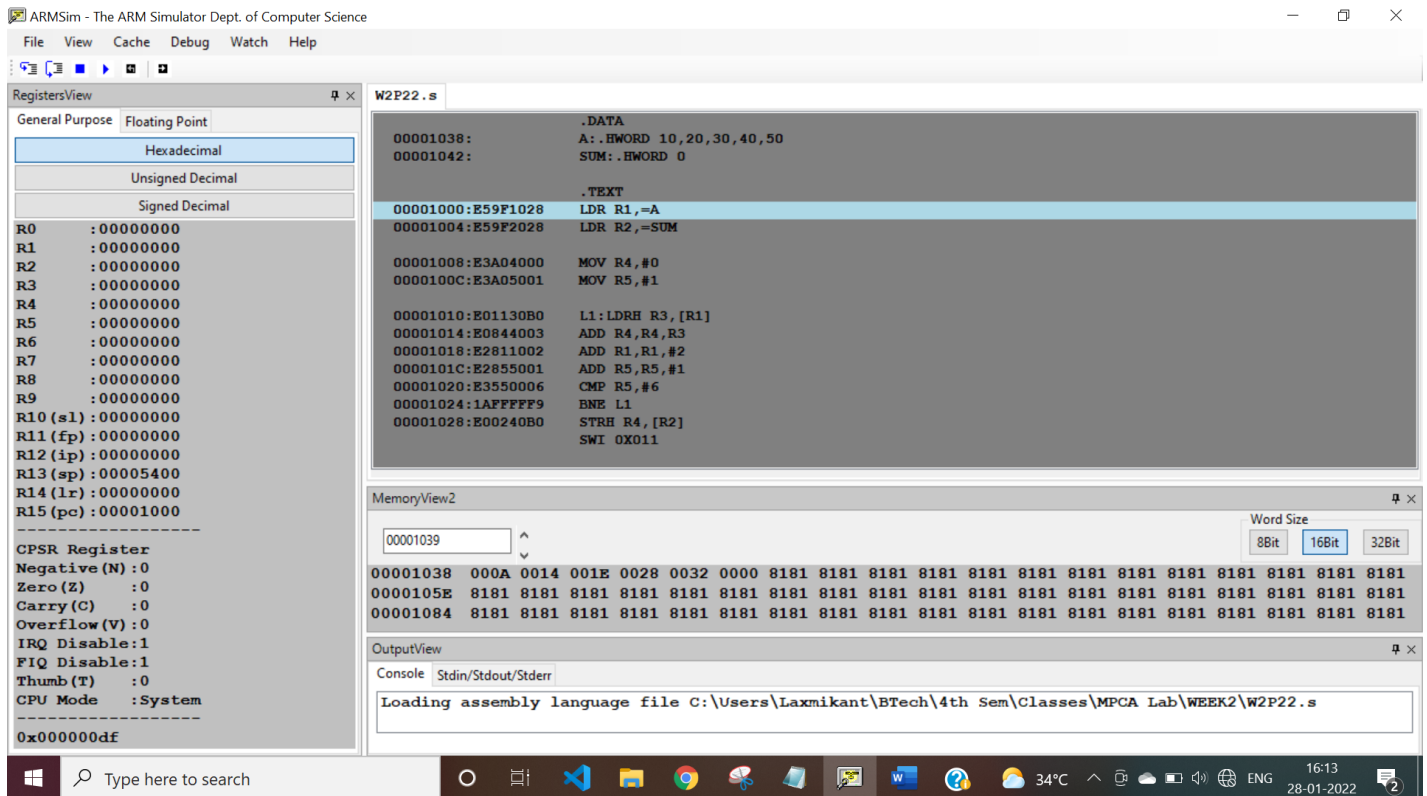
BNE L1

STRH R4,[R2]

SWI 0X011

OUTPUT SCREENSHOT:

Before execution:



The screenshot shows the ARMSim interface before execution. The RegistersView window displays the initial state of the registers, with R0 through R15 all set to 0x00000000. The CPSR Register shows the Zero (Z) flag set to 0. The MemoryView2 window shows the initial memory state, with the first 16 bytes of memory (00001038 to 00001084) containing the initial values of the data and text sections. The OutputView window shows the console output, which is empty.

RegistersView

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 00000000
R1 : 00000000
R2 : 00000000
R3 : 00000000
R4 : 00000000
R5 : 00000000
R6 : 00000000
R7 : 00000000
R8 : 00000000
R9 : 00000000
R10 (s1) : 00000000
R11 (fp) : 00000000
R12 (ip) : 00000000
R13 (sp) : 00005400
R14 (lr) : 00000000
R15 (pc) : 00001000

CPSR Register

Negative (N) : 0
Zero (Z) : 0
Carry (C) : 0
Overflow (V) : 0
IRQ Disable : 1
FIQ Disable : 1
Thumb (T) : 0
CPU Mode : System

0x000000df

W2P22.s

.DATA
00001038: A: .HWORD 10,20,30,40,50
00001042: SUM: .HWORD 0

.TEXT
00001000:E59F1028 LDR R1,=A
00001004:E59F2028 LDR R2,=SUM
00001008:E3A04000 MOV R4,#0
0000100C:E3A05001 MOV R5,#1
00001010:E01130B0 L1: LDRH R3,[R1]
00001014:E0844003 ADD R4,R4,R3
00001018:E2811002 ADD R1,R1,#2
0000101C:E2855001 ADD R5,R5,#1
00001020:E3550006 CMP R5,#6
00001024:1AFFFFFFF9 BNE L1
00001028:E00240B0 STRH R4,[R2]
SWI 0X011

MemoryView2

Word Size 8Bit 16Bit 32Bit

00001039

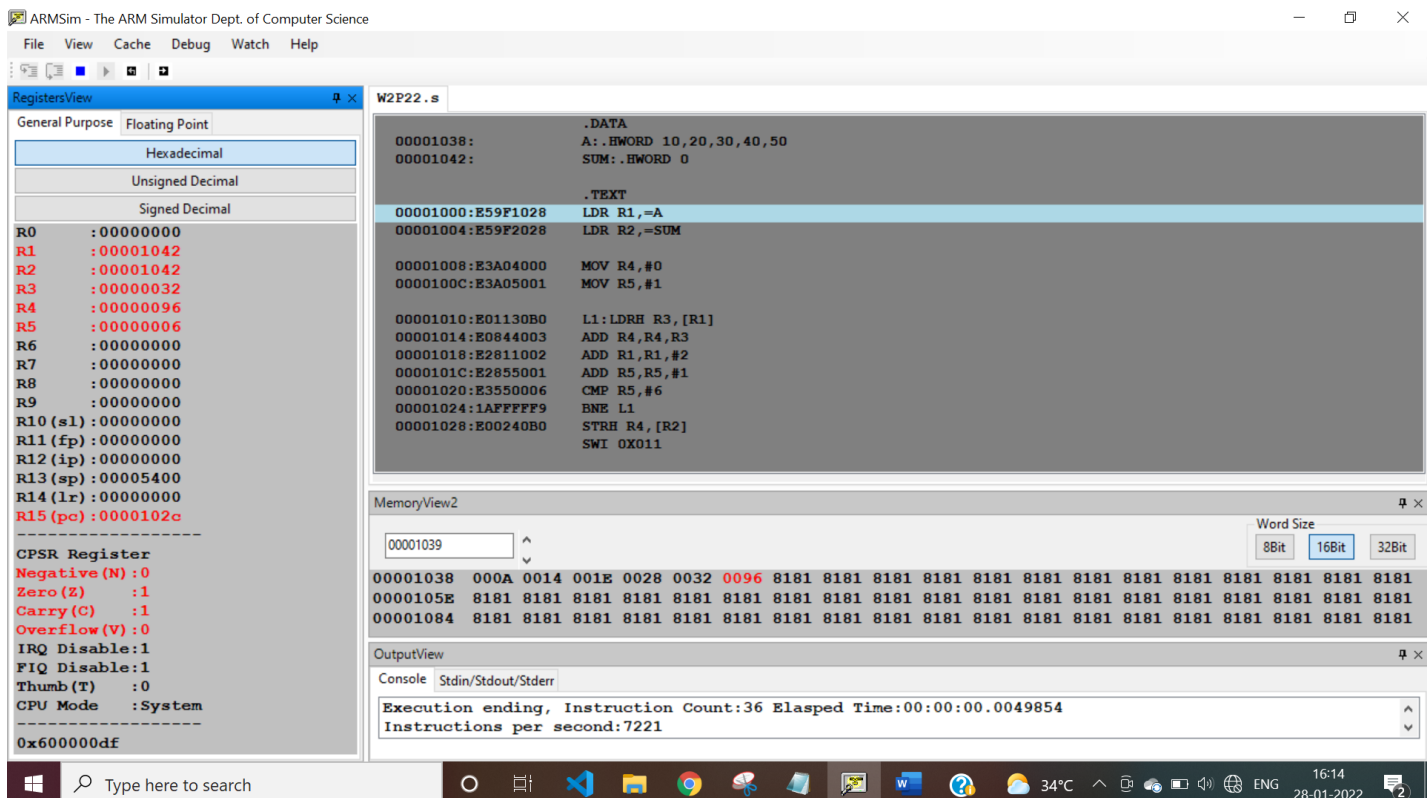
00001038 000A 0014 001E 0028 0032 0000 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181
0000105E 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181
00001084 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181

OutputView

Console Stdin/Stdout/Stderr

Loading assembly language file C:\Users\Laxmikant\BTEch\4th Sem\Classes\MPCA Lab\WEEK2\W2P22.s

After execution:



The screenshot shows the ARMSim interface after execution. The RegistersView window displays the final state of the registers, with R0 through R15 updated to their final values. The CPSR Register shows the Zero (Z) flag set to 1. The MemoryView2 window shows the final memory state, with the first 16 bytes of memory (00001038 to 00001084) containing the final values of the data and text sections. The OutputView window shows the console output, which includes the execution ending message and the instruction count and elapsed time.

RegistersView

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 00000000
R1 : 00001042
R2 : 00001042
R3 : 00000032
R4 : 00000096
R5 : 00000006
R6 : 00000000
R7 : 00000000
R8 : 00000000
R9 : 00000000
R10 (s1) : 00000000
R11 (fp) : 00000000
R12 (ip) : 00000000
R13 (sp) : 00005400
R14 (lr) : 00000000
R15 (pc) : 0000102c

CPSR Register

Negative (N) : 0
Zero (Z) : 1
Carry (C) : 1
Overflow (V) : 0
IRQ Disable : 1
FIQ Disable : 1
Thumb (T) : 0
CPU Mode : System

0x600000df

W2P22.s

.DATA
00001038: A: .HWORD 10,20,30,40,50
00001042: SUM: .HWORD 0

.TEXT
00001000:E59F1028 LDR R1,=A
00001004:E59F2028 LDR R2,=SUM
00001008:E3A04000 MOV R4,#0
0000100C:E3A05001 MOV R5,#1
00001010:E01130B0 L1: LDRH R3,[R1]
00001014:E0844003 ADD R4,R4,R3
00001018:E2811002 ADD R1,R1,#2
0000101C:E2855001 ADD R5,R5,#1
00001020:E3550006 CMP R5,#6
00001024:1AFFFFFFF9 BNE L1
00001028:E00240B0 STRH R4,[R2]
SWI 0X011

MemoryView2

Word Size 8Bit 16Bit 32Bit

00001039

00001038 000A 0014 001E 0028 0032 0096 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181
0000105E 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181
00001084 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181 8181

OutputView

Console Stdin/Stdout/Stderr

Execution ending, Instruction Count:36 Elapsed Time:00:00:00.0049854
Instructions per second:7221

b. Use Byte wise (.Byte directive)

NOTEPAD FILE:

```
W2P23.s - Notepad
File Edit Format View Help

.DATA
A: .byte 10,20,30,40,50
SUM: .byte 0

.TEXT
LDR R1,=A
LDR R2,=SUM

MOV R4,#0
MOV R5,#1

L1:LDRB R3,[R1]
ADD R4,R4,R3
ADD R1,R1,#1
ADD R5,R5,#1
CMP R5,#6
BNE L1
STRB R4,[R2]
SWI 0X011
```

OUTPUT SCREENSHOT:

Before execution:

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 00000000
R1 : 00000000
R2 : 00000000
R3 : 00000000
R4 : 00000000
R5 : 00000000
R6 : 00000000
R7 : 00000000
R8 : 00000000
R9 : 00000000
R10 (s1) : 00000000
R11 (fp) : 00000000
R12 (ip) : 00000000
R13 (sp) : 00005400
R14 (lr) : 00000000
R15 (pc) : 00001000

CPSR Register
Negative (N) : 0
Zero (Z) : 0
Carry (C) : 0
Overflow (V) : 0
IRQ Disable : 1
FIQ Disable : 1
Thumb (T) : 0
CPU Mode : System
0x000000dF

W2P23.s

```
.DATA
00001038: A: .byte 10,20,30,40,50
0000103D: SUM: .byte 0

.TEXT
00001000:E59F1028 LDR R1,=A
00001004:E59F2028 LDR R2,=SUM

00001008:E3A04000 MOV R4,#0
0000100C:E3A05001 MOV R5,#1

00001010:E5D13000 L1:LDRB R3,[R1]
00001014:E0844003 ADD R4,R4,R3
00001018:E2811001 ADD R1,R1,#1
0000101C:E2855001 ADD R5,R5,#1
00001020:E3550006 CMP R5,#6
00001024:1AFFFFF9 BNE L1
00001028:E5C24000 STRB R4,[R2]
SWI 0X011
```

MemoryView2

00001038 ^
v

Word Size 8Bit 16Bit 32Bit

00001038 0A 14 1E 28 32 00 00 00 81 ..(2.....
0000104F 81
00001066 81

OutputView

Console Stdin/Stdout/Stderr

Loading assembly language file C:\Users\Laxmikant\BTech\4th Sem\Classes\MFCA Lab\WEEK2\W2P23.s

16:19
28-01-2022

After execution:

ARMsim - The ARM Simulator Deft. of Computer Science

File View Cache Debug Watch Help

RegistersView

General Purpose Floating Point

Hexadecimal
Unsigned Decimal
Signed Decimal

Register	Value
R0	:00000000
R1	:0000103d
R2	:0000103d
R3	:00000032
R4	:00000096
R5	:00000006
R6	:00000000
R7	:00000000
R8	:00000000
R9	:00000000
R10 (sl)	:00000000
R11 (fp)	:00000000
R12 (ip)	:00000000
R13 (sp)	:00005400
R14 (lr)	:00000000
R15 (pc)	:0000102c

CPSR Register

Negative (N) : 0
Zero (Z) : 1
Carry (C) : 1
Overflow (V) : 0
IRQ Disable: 1
FIQ Disable: 1
Thumb (T) : 0
CPU Mode : System

0x600000df

W2P23.s

```
.DATA
00001038:      A:.byte 10,20,30,40,50
0000103D:      SUM:.byte 0

.TEXT
00001000:E59F1028 LDR R1,=A
00001004:E59F2028 LDR R2,=SUM

00001008:E3A04000 MOV R4,#0
0000100C:E3A05001 MOV R5,#1

00001010:E5D13000 L1:LDRB R3,[R1]
00001014:E0844003 ADD R4,R4,R3
00001018:E2811001 ADD R1,R1,#1
0000101C:E2855001 ADD R5,R5,#1
00001020:E3550006 CMP R5,#6
00001024:1AFFFFF9 BNE L1
00001028:E5C24000 STRB R4,[R2]
SWI 0X011
```

MemoryView2

Word Size
8Bit 16Bit 32Bit

00001038 ^
v

Address	Hex	ASCII
00001038	0A 14 1E 28 32 96 00 00	81 81 81 81 81 81 81 81 .. (2.....
0000104F	81 81 81 81 81 81 81 81	81 81 81 81 81 81 81 81
00001066	81 81 81 81 81 81 81 81	81 81 81 81 81 81 81 81

OutputView

Console Stdin/Stdout/Stderr

```
Execution ending, Instruction Count:36 Elapsed Time:00:00:00.0458405
Instructions per second:785
```