

# **MPCA LAB WEEK-5**

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**ROLL NO.: 55**

**SECTION : K**

**DATE : 26-02-2022**

**PROGRAM 1 :** Write a program in ARM7TDMI-ISA to multiply 2 matrices of order 3. i.e., implement  $c[i][j] = c[i][j] + a[i][j] \times b[i][j]$ .

**a. Use MLA instruction :**

**CODE :**

```
MATRIX_MUL - Notepad
File Edit Format View Help
.DATA
A: .WORD 1,2,3,4,5,6,7,8,9
B: .WORD 1,2,3,4,5,6,7,8,9
C: .WORD 0,0,0,0,0,0,0,0,0

.TEXT
LDR R0,=A
LDR R1,=B
LDR R2,=C
MOV R3,#0 ;INNER LOOP COUNT I INDEX
MOV R4,#0 ;OUTER LOOP J INDEX
MOV R10,#3 ;NUMBER OF ELEMENTS IN ROW
MOV R12,#4
MOV R9,#0
MOV R13,#0
MOV R9,#0

LOOP2:
MLA R8,R3,R10,R13
MOV R8,R8,LSL #2

LOOP1:|
MLA R11,R3,R10,R4
MLA R12,R14,R10,R9

MOV R11,R11,LSL #2
MOV R12,R12,LSL #2
LDR R5,[R0,R11] ;R0 value not updated
LDR R6,[R1,R12] ;R1 value not updated
MLA R7,R5,R6,R7
ADD R4,R4,#1
ADD R14,R14,#1
CMP R4,#3
BNE LOOP1
STR R7,[R2,R8]
MOV R7,#0
MOV R4,#0
MOV R14,#0
ADD R9,R9,#1
ADD R13,R13,#1
CMP R13,#3
BNE LOOP2

MOV R9,#0
MOV R13,#0
ADD R3,R3,#1
CMP R3,#3
BNE LOOP2

SWI 0X11
```

# OUTPUT :

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView 4 x

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 4256  
R1 : 4292  
R2 : 4328  
R3 : 3  
R4 : 0  
R5 : 9  
R6 : 9  
R7 : 0  
R8 : 32  
R9 : 0  
R10 (s1) : 3  
R11 (fp) : 32  
R12 (ip) : 32  
R13 (sp) : 0  
R14 (lr) : 0  
R15 (pc) : 4240

CPSR Register

Negative (N) : 0  
Zero (Z) : 1  
Carry (C) : 1  
Overflow (V) : 0  
IRQ Disable : 1  
FIQ Disable : 1  
Thumb (T) : 0  
CPU Mode : System

0x600000df

MATRIX\_MUL.S

```
.DATA
000010A0: A: .WORD 1,2,3,4,5,6,7,8,9
000010C4: B: .WORD 1,2,3,4,5,6,7,8,9
000010E8: C: .WORD 0,0,0,0,0,0,0,0,0

.TEXT
00001000:E59F008C LDR R0,=A
00001004:E59F108C LDR R1,=B
00001008:E59F208C LDR R2,=C
0000100C:E3A03000 MOV R3,#0 ;INNER LOOP COUNT I INDEX
00001010:E3A04000 MOV R4,#0 ;OUTER LOOP J INDEX
00001014:E3A0A003 MOV R10,#3 ;NUMBER OF ELEMENTS IN ROW
00001018:E3A0C004 MOV R12,#4
0000101C:E3A09000 MOV R9,#0
00001020:E3A0D000 MOV R13,#0
00001024:E3A09000 MOV R9,#0

00001028:
00001028:E028DA93 MLA R8,R3,R10,R13
0000102C:E1A08108 MOV R8,R8,LSL #2

00001030:
00001030:E02B4A93 MLA R11,R3,R10,R4
00001034:E02C9A9E MLA R12,R14,R10,R9
```

MemoryView1

Word Size

8Bit 16Bit 32Bit

000010E8

000010E8	0000001E	00000024	0000002A	00000042	00000051	00000060	00000066	0000007E	00000096	81818181
00001110	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181
00001138	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181
00001160	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181

OutputView

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30°C

ENG

13:37

26-02-2022

## b. Use MUL instruction :

### CODE :

```
MATRIX_MUL_BY_MUL - Notepad
File Edit Format View Help
|.DATA
A:.WORD 1,2,3,4,5,6,7,8,9
B:.WORD 1,2,3,4,5,6,7,8,9
C:.WORD 0,0,0,0,0,0,0,0,0

.TEXT
LDR R0,=A
LDR R1,=B
LDR R2,=C
MOV R3,#0 ;INNER LOOP COUNT I INDEX
MOV R4,#0 ;OUTER LOOP J INDEX
MOV R10,#3 ;NUMBER OF ELEMENTS IN ROW
MOV R12,#4
MOV R9,#0
MOV R13,#0
MOV R9,#0
MOV R7,#0

LOOP2:
MUL R8,R3,R10
ADD R8,R8,R13
MOV R8,R8,LSL #2

LOOP1:
MUL R11,R3,R10
ADD R11,R11,R4
MUL R12,R14,R10
ADD R12,R12,R9
MOV R11,R11,LSL #2
MOV R12,R12,LSL #2
LDR R5,[R0,R11] ;R0 value not updated
LDR R6,[R1,R12] ;R1 value not updated
STR R7,[R2,R8]

MUL R6,R5,R6
ADD R7,R7,R6

ADD R4,R4,#1
ADD R14,R14,#1
CMP R4,#3
BNE LOOP1

STR R7,[R2,R8]
MOV R7,#0
MOV R4,#0
MOV R14,#0
ADD R9,R9,#1
ADD R13,R13,#1
CMP R13,#3
BNE LOOP2

MOV R9,#0
MOV R13,#0
ADD R3,R3,#1
CMP R3,#3
BNE LOOP2

SWI 0X11
```

# OUTPUT :

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView

General Purpose Floating Point

Hexadecimal  
Unsigned Decimal  
Signed Decimal

R0 : 4280  
R1 : 4316  
R2 : 4352  
R3 : 3  
R4 : 0  
R5 : 9  
R6 : 81  
R7 : 0  
R8 : 32  
R9 : 0  
R10 (s1) : 3  
R11 (fp) : 32  
R12 (ip) : 32  
R13 (sp) : 0  
R14 (lr) : 0  
R15 (pc) : 4264

CPSR Register  
Negative (N) : 0  
Zero (Z) : 1  
Carry (C) : 1  
Overflow (V) : 0  
IRQ Disable : 1  
FIQ Disable : 1  
Thumb (T) : 0  
CPU Mode : System  
0x600000df

MATRIX\_MUL\_BY\_MUL.S

```
.DATA
A: .WORD 1,2,3,4,5,6,7,8,9
B: .WORD 1,2,3,4,5,6,7,8,9
C: .WORD 0,0,0,0,0,0,0,0,0

.TEXT
00001000:E59F00A4 LDR R0,=A
00001004:E59F10A4 LDR R1,=B
00001008:E3A02C11 LDR R2,=C
0000100C:E3A03000 MOV R3,#0 ;INNER LOOP COUNT I INDEX
00001010:E3A04000 MOV R4,#0 ;OUTER LOOP J INDEX
00001014:E3A0A003 MOV R10,#3 ;NUMBER OF ELEMENTS IN ROW
00001018:E3A0C004 MOV R12,#4
0000101C:E3A09000 MOV R9,#0
00001020:E3A0D000 MOV R13,#0
00001024:E3A09000 MOV R9,#0
00001028:E3A07000 MOV R7,#0

0000102C: LOOP2:
0000102C:E0080A93 MUL R8,R3,R10
00001030:E088800D ADD R8,R8,R13
00001034:E1A08108 MOV R8,R8,LSL #2

00001038: LOOP1:
```

MemoryView1

Word Size  
8Bit 16Bit 32Bit

00001100

00001100	0000001E	00000024	0000002A	00000042	00000051	00000060	00000066	0000007E	00000096	81818181
00001128	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181
00001150	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181
00001178	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181

OutputView

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**PROGRAM 2 :** Write a program in ARM7TDMI-ISA to find the NORM of a square matrix of order n.

**CODE :**

```
NORM - Notepad
File Edit Format View Help

.DATA
A: .WORD 4,8,2,4,-7,8,1,3,-5
B: .WORD 0
.TEXT
LDR R0,=A
LDR R1,=B
MOV R2,#0 ;STORES NORM
MOV R6,#0 ;COUNTER I FOR OUTER LOOP
MOV R7,#0 ;COUNTER J FOR INNER LOOP

LOOP1:
MOV R3,#0
MOV R7,#0
LOOP2:
LDR R4,[R0],#4
CMP R4,#0
BGE LOOP3
MVN R4,R4
ADD R4,R4,#1
LOOP3:
ADD R7,R7,#1
ADD R3,R3,R4
CMP R7,#3
BNE LOOP2
CMP R2,R3
BGE LOOP4
MOV R2,R3
LOOP4:
ADD R6,R6,#1
CMP R6,#3
BNE LOOP1

STR R2,[R1]
SWI 0x11
```

**OUTPUT :**

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 4236  
R1 : 4236  
R2 : 19  
R3 : 9  
R4 : 5  
R5 : 0  
R6 : 3  
R7 : 3  
R8 : 0  
R9 : 0  
R10 (s1) : 0  
R11 (fp) : 0  
R12 (ip) : 0  
R13 (sp) : 21504  
R14 (lr) : 0  
R15 (pc) : 4188

CPSR Register

Negative (N) : 0  
Zero (Z) : 1  
Carry (C) : 1  
Overflow (V) : 0  
IRQ Disable: 1  
FIQ Disable: 1  
Thumb (T) : 0  
CPU Mode : System

0x600000df

NORM.S

```
.DATA
00001068: A: .WORD 4,8,2,4,-7,8,1,3,-5
0000108C: B: .WORD 0

.TEXT
00001000:E59F0058 LDR R0,=A
00001004:E59F1058 LDR R1,=B
00001008:E3A02000 MOV R2,#0 ;STORES NORM
0000100C:E3A06000 MOV R6,#0 ;COUNTER I FOR OUTER LOOP
00001010:E3A07000 MOV R7,#0 ;COUNTER J FOR INNER LOOP

00001014: LOOP1:
00001014:E3A03000 MOV R3,#0
00001018:E3A07000 MOV R7,#0

0000101C: LOOP2:
0000101C:E4904004 LDR R4,[R0],#4

00001020:E3540000 CMP R4,#0
00001024:AA000001 BGE LOOP3
00001028:E1E04004 MVN R4,R4
0000102C:E2844001 ADD R4,R4,#1
00001030: LOOP3:
```

MemoryView1

0000108C

Word Size 8Bit 16Bit 32Bit

0000108C	00000013	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181
000010B4	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181
000010DC	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181
00001104	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181

OutputView

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26°C

19:16

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**PROGRAM 3 :** Write a program in ARM7TDMI-ISA to find the ROWSUM of a matrix.

**CODE :**

```
*ROW_SUM - Notepad
File Edit Format View Help
.DATA
A: .WORD 1,2,3,4,5,6,7,8,9
C: .WORD 0,0,0
.TEXT
LDR R0,=A
LDR R2,=C
MOV R3,#0 ;INNER LOOP COUNT I INDEX
MOV R4,#0 ;OUTER LOOP J INDEX
MOV R10,#3 ;NUMBER OF ELEMENTS IN ROW
MOV R12,#4
MOV R9,#0

LOOP1:MOV R14,R9,LSL #2
MLA R11,R3,R10,R4
MOV R11,R11,LSL #2
ADD R4,R4,#1
MLA R12,R3,R10,R4
MOV R12,R12,LSL #2
ADD R4,R4,#1
MLA R13,R3,R10,R4
MOV R13,R13,LSL #2
LDR R5,[R0,R11] ;R0 value not updated
LDR R6,[R0,R12]
LDR R8,[R0,R13]
ADD R1,R5,R6
ADD R7,R8,R1
STR R7,[R2,R14]
ADD R9,R9,#1
MOV R4,#0
ADD R3,R3,#1
CMP R3,#3
BNE LOOP1
SWI 0X11
```

# OUTPUT :

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 4216  
R1 : 15  
R2 : 4252  
R3 : 3  
R4 : 0  
R5 : 7  
R6 : 8  
R7 : 24  
R8 : 9  
R9 : 3  
R10 (s1) : 3  
R11 (fp) : 24  
R12 (ip) : 28  
R13 (sp) : 32  
R14 (lr) : 8  
R15 (pc) : 4204

CPSR Register

Negative (N) : 0  
Zero (Z) : 1  
Carry (C) : 1  
Overflow (V) : 0  
IRQ Disable : 1  
FIQ Disable : 1  
Thumb (T) : 0  
CPU Mode : System

0x600000df

ROW\_SUM.S

```
00001020:E02B4A93 MLA R11,R3,R10,R4
00001024:E1A0B10B MOV R11,R11,LSL #2
00001028:E2844001 ADD R4,R4,#1
0000102C:E02C4A93 MLA R12,R3,R10,R4
00001030:E1A0C10C MOV R12,R12,LSL #2
00001034:E2844001 ADD R4,R4,#1
00001038:E02D4A93 MLA R13,R3,R10,R4
0000103C:E1A0D10D MOV R13,R13,LSL #2
00001040:E790500B LDR R5,[R0,R11] ;R0 value not updated
00001044:E790600C LDR R6,[R0,R12]
00001048:E790800D LDR R8,[R0,R13]
0000104C:E0851006 ADD R1,R5,R6
00001050:E0887001 ADD R7,R8,R1
00001054:E782700E STR R7,[R2,R14]
00001058:E2899001 ADD R9,R9,#1
0000105C:E3A04000 MOV R4,#0
00001060:E2833001 ADD R3,R3,#1
00001064:E3530003 CMP R3,#3
00001068:1AFFFFEB BNE LOOP1
0000106C:EF000011 SWI 0X11
```

MemoryView1

Word Size

8Bit 16Bit 32Bit

0000109C

0000109C	00000006	0000000F	00000018	81818181	81818181	81818181	81818181	81818181	81818181	81818181
000010C4	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181
000010EC	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181
00001114	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181

OutputView

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