Himax HM01B0 UPduino Shield

User Guide

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
FPGA	Field-Programmable Gate Array
FTDI	Future Technology Devices International
I²S	Inter-IC Sound
LED	Light-Emitting Diode
SOIC	Small Outline Integrated Circuit
SPI	Serial Peripheral Interface
USB	Universal Serial Bus

1. Introduction

The Himax HM01B0 UPduino Shield is an evaluation and development platform based on the iCE40™ UltraPlus FPGA (Field-Programmable Gate Array). It consists of two boards – the UPduino v2.0 and the Himax HM01B0 Aapter Board. The UPduino v2.0 is an efficient, low-cost base platform designed by Gnarly Grey, including the iCE40UP5K FPGA, and basic power and programming control. The Himax HM01B0 Adapter Board adds a camera with a low-power Himax image sensor, two microphones, and multiple LEDs for quick visual feedback.

This flexible and powerful platform enables designers to investigate and experiment with key features of the iCE40 UltraPlus FPGA and assists with rapid prototyping and testing of specific designs.

Key features of the Himax HM01B0 UPduino Shield include:

- UPduino v2.0
    - iCE40 FPGA - iCE40UP5K-SG48I (5K LUTs, 39 I/Os, 120 Kbits Embedded Block RAM, 1 PLL and more in a 7 mm x 7 mm 48-pin QFN package.)
    - USB connection for UART and device programming
    - On-board Boot Flash
    - RGB LED
- Himax HM01B0 Adapter Board
    - Camera module with Himax HM01B0 image sensor
    - Two I^{2}S microphones
    - Six green LEDs
- Also included with the kit
    - 3 ft Micro USB cable for programming and power
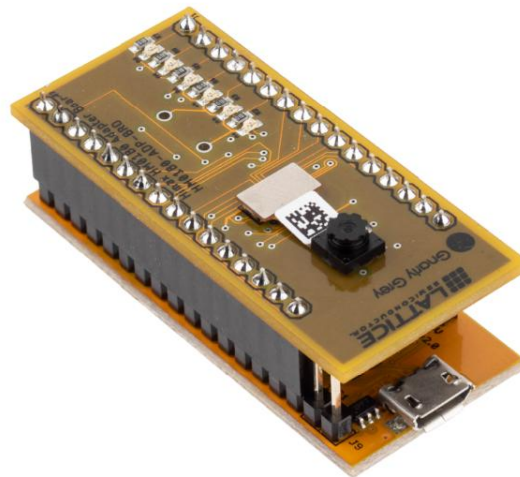   - QuickStart Guide

Figure 1.1. Himax HM01B0 UPduino Shield

1.1. Further Information

This board features an iCE40UP5K-SG48I FPGA. More information about this FPGA can be found on the Lattice web site at: www.latticesemi.com/iCE40UltraPlus. A complete description of this device can be found in iCE40 UltraPlus Family Data Sheet (FPGA-DS-02008).

2. Power Supply

External 5 V Power from the USB Connector (J7) provides power to the entire two board set.

Alternately, power can be applied to headers on the UPduino v2.0 board:

- J6 - 5.0 V
- J9 – Ground

3. Board Overview

The following diagrams show key features of the Himax HM01B0 Adapter and UPduino v2.0 boards.
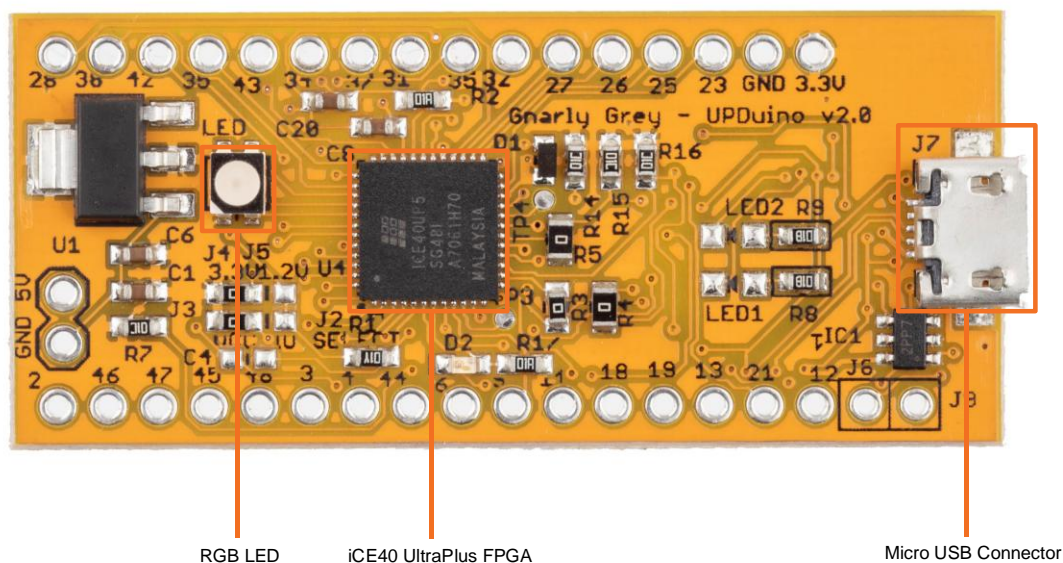
RGB LED   iCE40 UltraPlus FPGA   Micro USB Connector

Figure 3.1. UPduino v2.0 – Front View
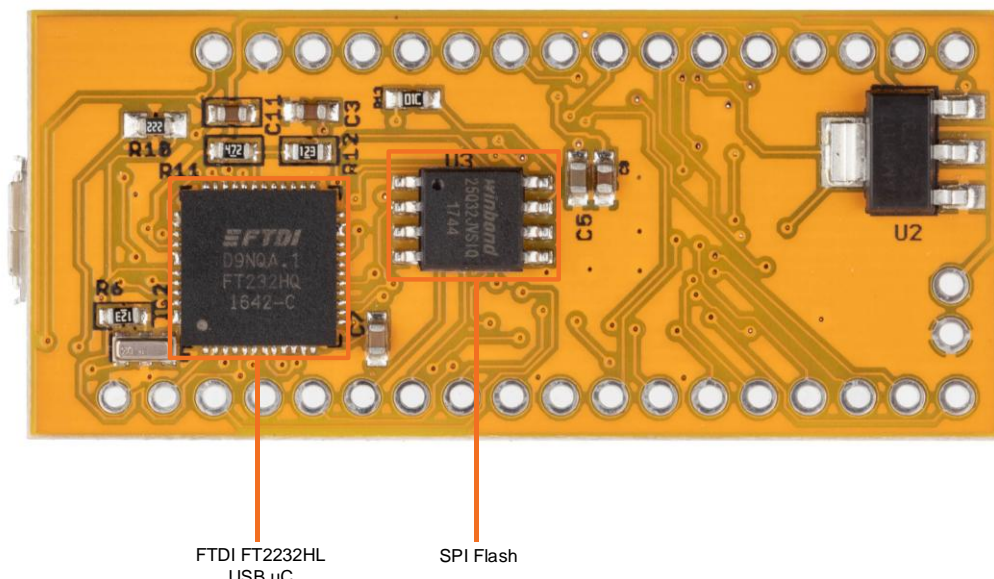
FTDI FT2232HL   SPI Flash
USB uC

Figure 3.2. UPduino v2.0 – Back View

Camera Module with
Himax HM01B0 Sensor

Holes for Microphone
Audio Input

LEDs

Figure 3.3. Himax HM01B0 Adapter Board – Front View

Dual I2S Microphones

Figure 3.4. Himax HM01B0 Adapter Board – Back View

4.   iCE40 UltraPlus Pin Summary

The following is a reference to indicate the connection of the iCE40 UltraPlus FPGA I/O pins on each board.

Table 4.1. Upstream Connector Mapping

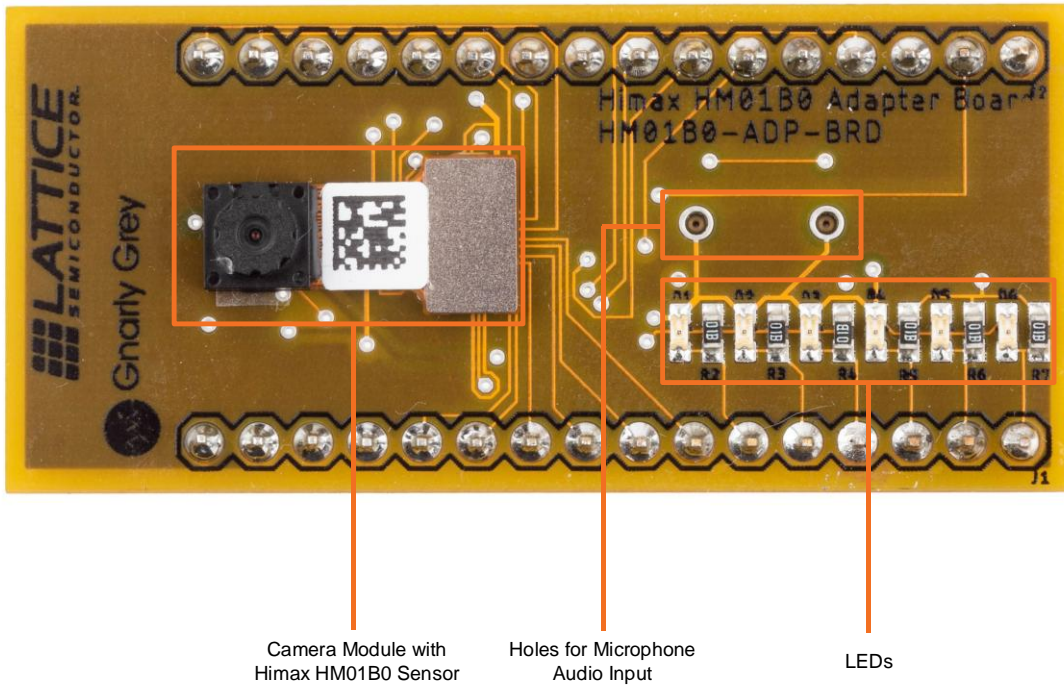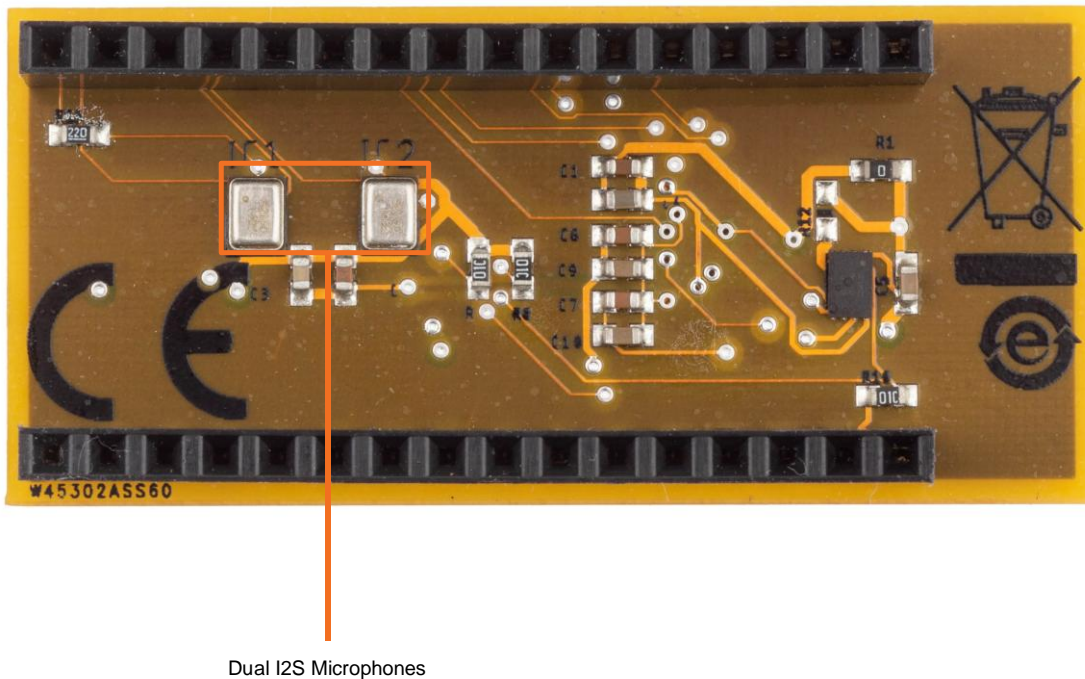| SG48	Function	Pin Type	Bank	Differential Pair	UPduino v2.0	Himax HM01B0 Adapter
1	VCCIO_2	VCCIO	2	–	–	–
2	IO B_6a	PIO	2	–	JP6-16	I2S data
3	IO B_9b	DPIO	2	COMP_of_IOB_8a	JP6-11	Molex1 – 8: SDA
4	IO B_8a	DPIO	2	TRUE_of_IOB_9b	JP6-10	Molex1 – 7: SCL
5	VCC	VCC	VCC	–	–	–
6	IO B_13b	DPIO	1	COMP_of_IOB_12a	JP6-8	Molex1 – 5: FVLD
7	CDONE	CONFIG	1	–	LED – D2	–
8	creset_b	CONFIG	1	–	–	–
9	IO B_16a	PIO	1	–	JP6-7	Molex1 – 4: TRIG
10	IO B_18a	PIO	1	–	TP3	–
11	IO B_20a	PIO	1	–	JP6-6	MCLK
12	IO B_22a	DPIO	1	TRUE_of_IOB_23b	JP6-1	Molex1 – 18: D1
13	IO B_24a	DPIO	1	TRUE_of_IOB_25b	JP6-3	RESET_CAM (NC)
14	IO B_32a_SPI_SO	DPIO/CONFIG_SPI	1	–	SPI Flash – SDO	–
15	IO B_34a_SPI_SCK	DPIO/CONFIG_SPI	1	–	SPI Flash – SCK	–
16	IO B_35b_SPI_SS	DPIO/CONFIG_SPI	1	–	SPI Flash – CS	–
17	IO B_33b_SPI_SI	DPIO/CONFIG_SPI	1	–	SPI Flash – SDI	–
18	IO B_31b	PIO	1	–	JP6- 5	PWDN (NC)
19	IO B_29b	PIO	1	–	JP6- 4	Molex1 – 16: PCLK
20	IO B_25b_G3	DPIO/GBIN	1	COMP_of_IOB_24a	TP4	–
21	IO B_23b	DPIO	1	COMP_of_IOB_22a	JP6- 2	Molex1 – 17: D0
22	SPI_V$_{CCIO1}$	VCCIO	1	–	–	–
23	IOT_37a	DPIO/I3C	0	TRUE_of_IOT_36b	JP5- 3	D9
24	VPP_2V5	VPP	VPP	–	–	–
25	IOT_36b	DPIO/I3C	0	COMP_of_IOT_37a	JP5- 4	D8
26	IOT_39a	DPIO	0	TRUE_of_IOT_38b	JP5- 5	Molex1 – 24: D7
27	IOT_38b	DPIO	0	COMP_of_IOT_39a	JP5- 6	Molex1 – 23: D6
28	IOT_41a	PIO	0	–	JP5- 16	LED5
29	VCCPLL	VCCPLL		–	–	–
30	VCC	VCC	VCC	–	–	–
31	IOT_42b	DPIO	0	COMP_of_IOT_43a	JP5- 9	Molex1 – 20: D3
32	IOT_43a	DPIO	0	TRUE_of_IOT_42b	JP5- 7	Molex1 – 22: D5
33	VCCIO_0	VCCIO	0	–	–	–
34	IOT_44b	DPIO	0	COMP_of_IOT_45a	JP5- 11	LEDO
35	IOT_46b_G0	DPIO/GBIN	0	–	JP5- 8	Mole x1 – 21: D4
36	IOT_48b	DPIO	0	COMP_of_IOT_49a	JP5- 13	LED2
37	IOT_45a_G1	DPIO/GBIN	0	TRUE_of_IOT_44b	JP5- 10	Molex1 – 19: D2
38	IOT_50b	DPIO	0	COMP_of_IOT_51a	JP5- 15	LED4
39	RGB0	LED	0	–	RGB LED – Red	–
40	RGB1	LED	0	–	RGB LED – Green	–
41	RGB2	LED	0	–	RGB LED – Blue	–
42	IOT_51a	DPIO	0	TRUE_of_IOT_50b	JP5- 14	LED3
43	IOT_49a	DPIO	0	TRUE_of_IOT_48b	JP5- 12	LED1

SG48	Function	Pin Type	Bank	Differential Pair	UPduino v2.0	Himax HM01B0 Adapter
44	IO B_3b_G6	DPIO/GBIN	2	COMP_of_IOB_2a	JP6- 9	Molex1 – 6: LVLD
45	IO B_5b	DPIO	2	COMP_of_IOB_4a	JP6- 13	U2 – 2: STBY
46	IO B_0a	PIO	2	–	JP6- 15	I25 Clk
47	IO B_2a	DPIO	2	TRUE_of_IOB_3b	JP6- 14	I25 WS
48	IO B_4a	DPIO	2	TRUE_of_IOB_5b	JP6- 12	–
Paddle	GND	GND	GND	–	–	Molex1 – 9: INT

FPGA-UG-02081-1.0

5. Software Requirements

Install the following software before you begin developing designs for the board:

- Lattice Radiant 1.0 (or higher)
  - Used for developing your own custom designs for the iCE40 UltraPlus FPGA
  - Download at: www.latticesemi.com/radiant
- Radiant Programmer 1.0 (or higher)
  - Used to program the iCE40 UltraPlus FPGA
  - This is included with Radiant software installation, or as a stand-alone tool.
  - Download at: www.latticesemi.com/radiant

6. Board Configuration and Programming

6.1. Board Configuration

The iCE40 UltraPlus on Himax HM01B0 UPduino Shield can be programmed via the included micro-USB cable using a PC running Lattice Radiant Programmer software. After the software is installed and launched, and the USB cable is connected to the board, see below for programming procedures.

There are two modes to program the iCE40 UltraPlus FPGA on the UPduino v2.0 board.

- **SPI Flash Programming (default):** In this mode, the on-board SPI Flash is programmed, which in-turn programs the iCE40 UltraPlus FPGA at power-up or reset. This allows the user program to be stored in non-volatile memory when the board is powered-off or reset. This is the default programming mode.
- **Direct CRAM Programming:** In this mode, the iCE40 UltraPlus FPGA CRAM memory is programmed directly. This may allow for more rapid reconfiguration (if you need to regularly re-program the iCE40 UltraPlus while debugging), but the program is not be retained when the board is powered-off. To use this mode, a modification to the board is required.

The default programming mode is SPI Flash programming. To change the programming mode, resistor R4 and R3 must be removed and replaced in the orientation shown in Figure 6.1.

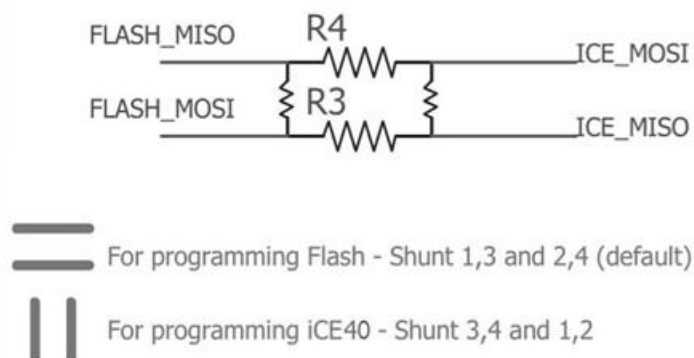**Figure 6.1. Programming Settings**

6.2. Programming the SPI Flash

To program the SPI Flash:

1. Set board resistors to horizontal for SPI Flash programming.

    Note: This is the default mode.

2. Connect the Himax HM01B0 UPduino Shield via USB cable to PC with Radiant Programmer installed.

3. Start Radiant Programmer.

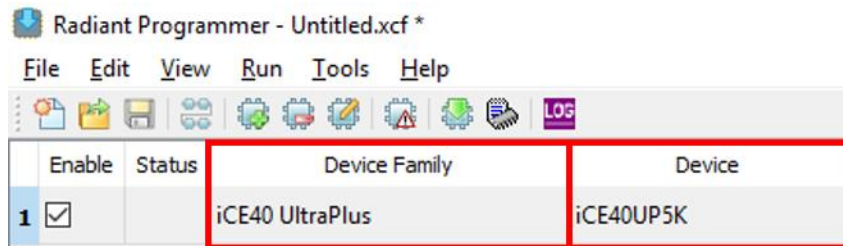4. Set **Device Family** to **iCE40 UltraPlu**s and **Device** to **iCE40UP5K** as shown in Figure 6.2.

Figure 6.2. Device Family and Device Setting

5. Click the iCE40 UltraPlus row, and select **Edit > Device Properties**.

6. In the **Device Properties** dialog box, apply the settings below that are common to the three files to program (see Figure 6.3).

    a. Under **Device Operation**, select the options below:
    -   **Target Memory — External SPI Flash Memory (SPI FLASH)**
    -   **Port Interface — SPI**
    -   **Access Mode— Direct Programming**
    -   **Operation — Erase, Program, Verify**

    b. Under **Programming Options**, select the option below:
    -   **Programming File — <Select desired file to program>**

    c. Under **SPI Flash Options**, select the options below:
    -   **Family — SPI Serial Flash**
    -   **Vendor — Winbond**
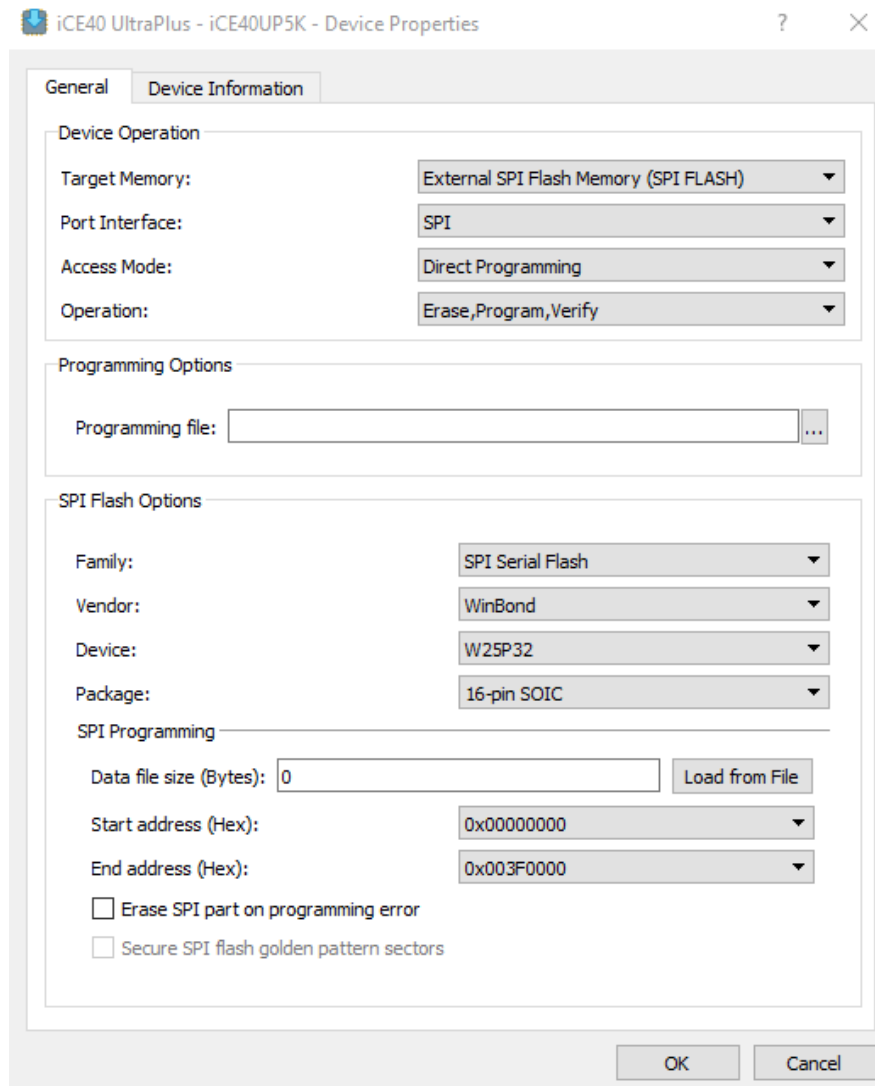   -   **Device — W25P32**
    -   **Package —16-pin SOIC**

Figure 6.3. Onboard SPI Flash Device Properties Settings

7. Click **OK** to close the Device Properties window.

8. Click the **Program** button in Radiant Programmer to program the Onboard SPI Flash.

6.3. Programming the CRAM Directly

To program the CRAM directly:

1. Set board resistors to vertical for CRAM Programming.

2. Connect the Himax HM01B0 UPduino Shield via USB cable to PC with Radiant Programmer installed.

3. Start Radiant Programmer.

4. Set **Device Family** to **iCE40 UltraPlus** and **Device** to **iCE40UP5K** as shown in Figure 6.4.

5. Click the iCE40 UltraPlus row, and select **Edit > Device Properties**.
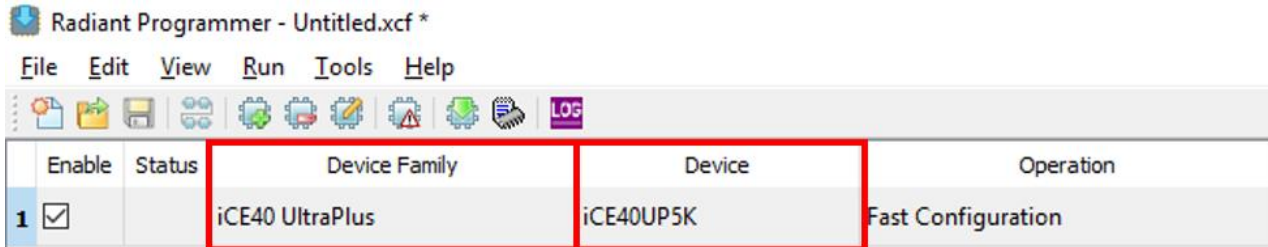
Figure 6.4. Device Family and Device Settings

6. In the **Device Properties** dialog box, apply the as shown in Figure 6.5.
   - **Target Memory — Compressed Random Access Memory (CRAM)**
   - **Port Interface — Slave SPI**
   - **Access Mode — Direct Programming**
   - **Operation — Fast Configuration**

7. Click **OK** to close the **Device Properties** window.

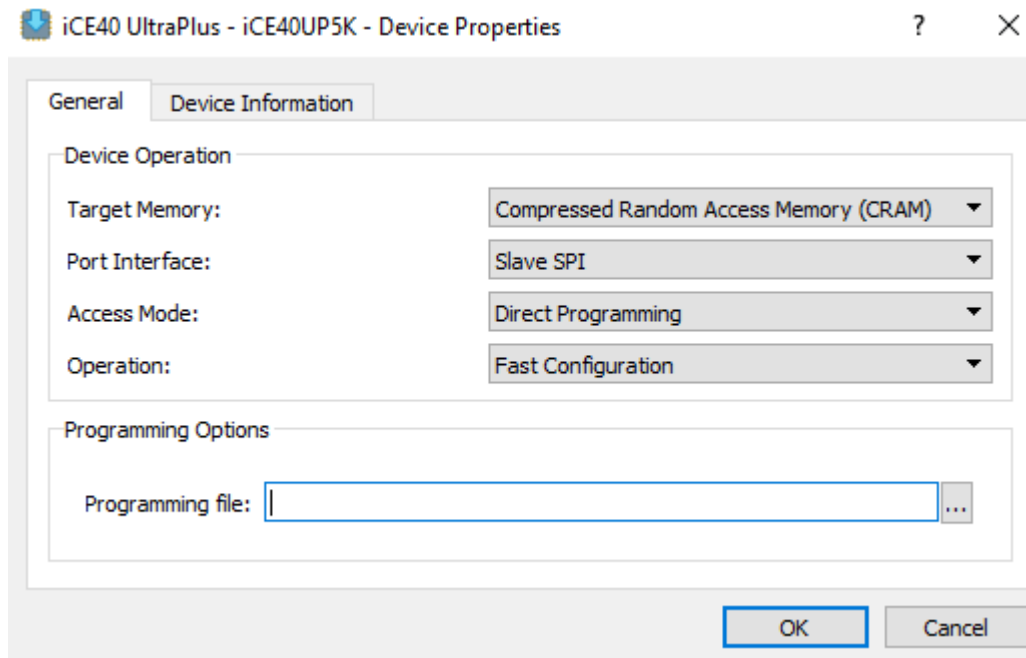8. Click the **Program** button in Radiant Programmer to begin programming.

Figure 6.5. Device Properties for iCE40 Device Configuration Memory

7. Storage and Handling

Static electricity can shorten the life span of electronic components. Observe these tips to prevent damage that can occur from electrostatic discharge:

- Use antistatic precautions such as operating on an antistatic mat and wearing an antistatic wristband.
- Store the development board in the provided packaging.
- Touch a metal USB housing to equalize voltage potential between you and the board.

8. Ordering Information

Table 8.1. Reference Part Number

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
Himax HM01B0 UPduino Shield	HM01B0-UPD-EVN	

References

For more information, refer to

- iCE40 Ultra Plus Family Data Sheet (FPGA-DS-02008)
- www.latticesemi.com/iCE40UltraPlus

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.
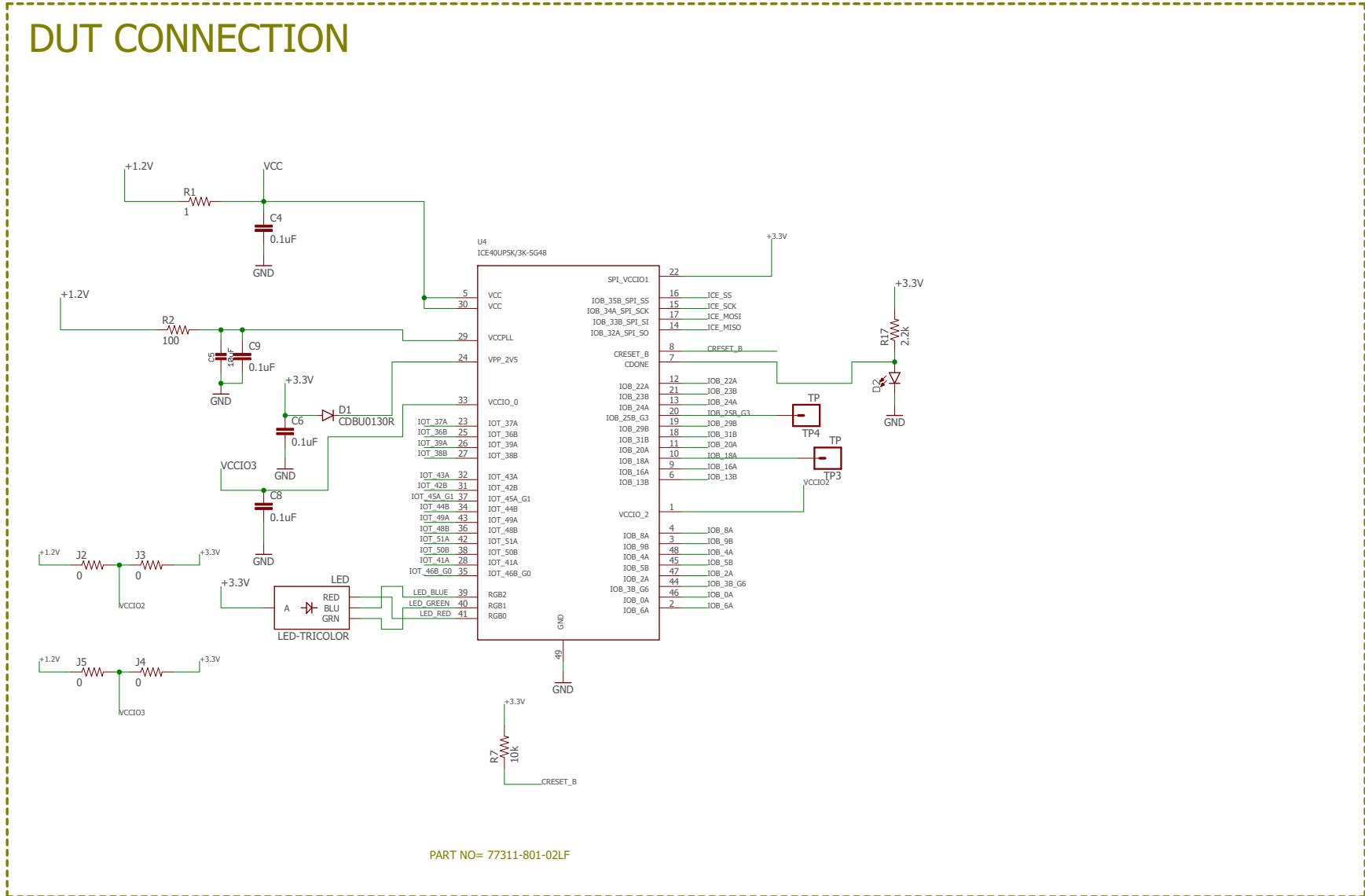
Appendix A. Himax HM01B0 UPduino Shield Board Schematics
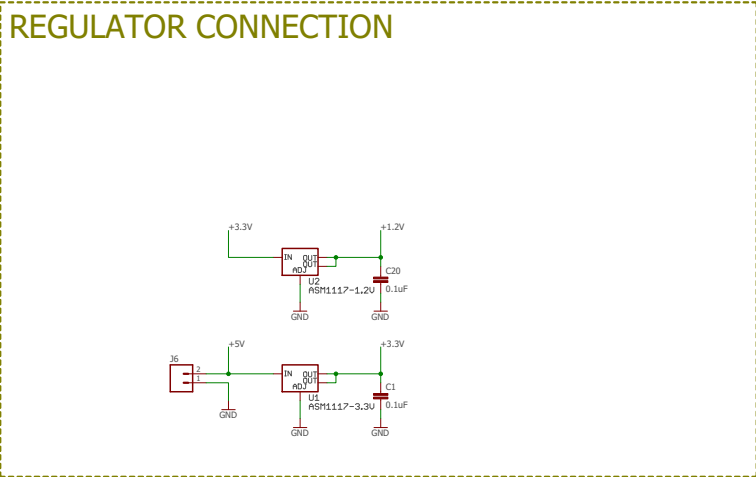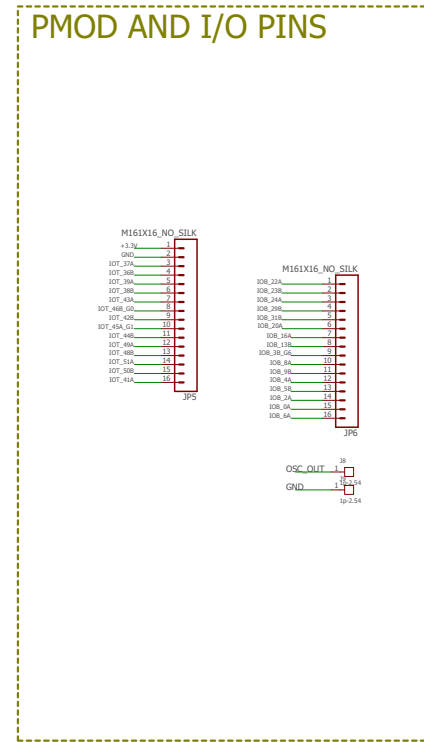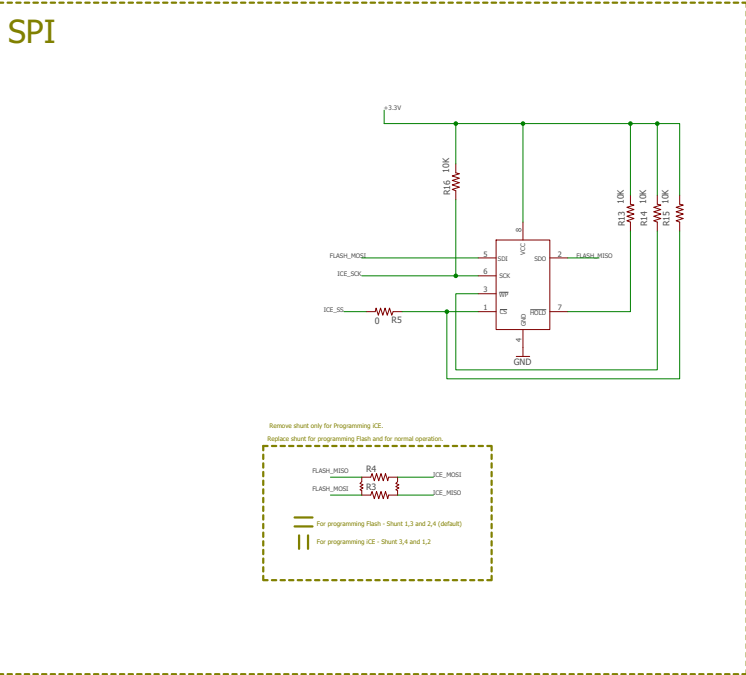

Figure A.1. UPduino 2.0 FPGA Schematic

LATTICE SEMICONDUCTOR

SPI

PMOD AND I/O PINS

REGULATOR CONNECTION
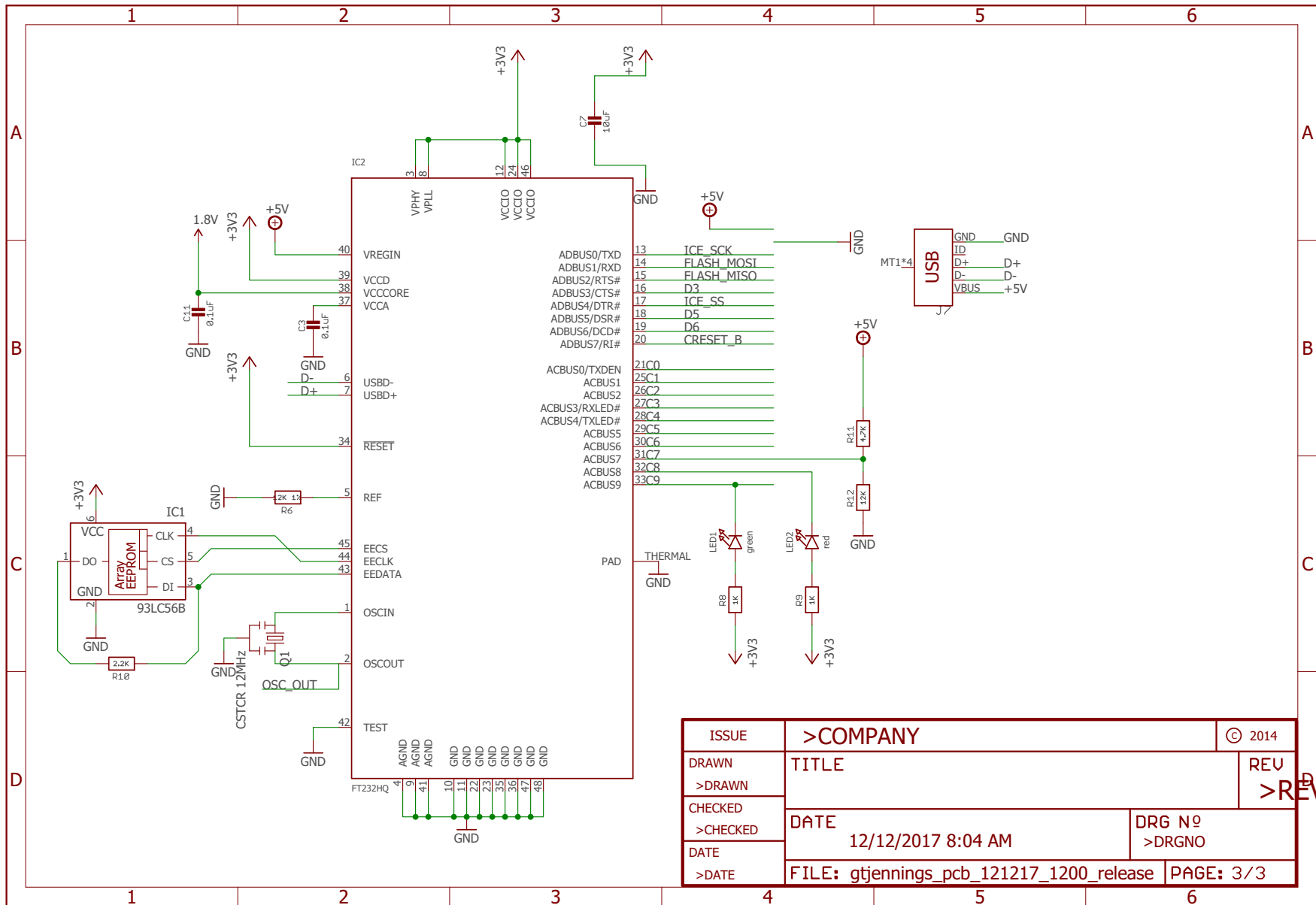
Figure A.2. UPduino 2.0 SPI Flash/I/O Pins/Regulator Connections

Figure A.3. UPduino 2.0 FTDI Chip Connection
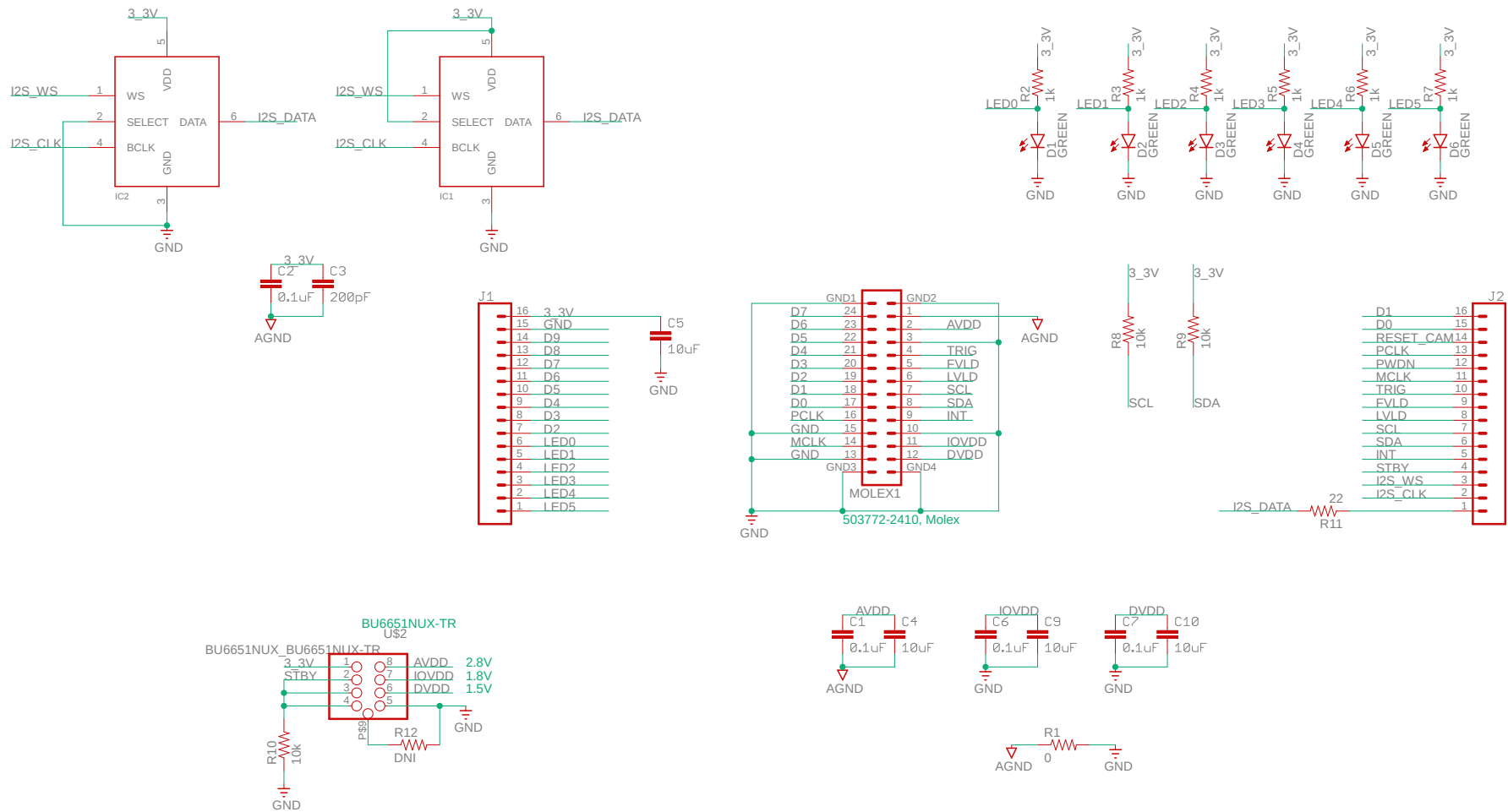
Figure A.4. Himax HM01B0 Adapter Board Schematic

Revision History

Revision 1.0, November 2018

Section	Change Summary
All	Initial release.