Chapter 6

Digital Video Interfaces

Pro-Video Component Interfaces

Pro-video equipment, such as that used within studios, has unique requirements and therefore its own set of digital video interconnect standards. Table 6.1 lists the various pro-video parallel and serial digital interface standards.

Video Timing

Rather than digitize and transmit the blanking intervals, special sequences are inserted into the digital video stream to indicate the start of active video (SAV) and end of active video (EAV). These EAV and SAV sequences indicate when horizontal and vertical blanking is present and which field is being transmitted. They also enable the transmission of ancillary data such as digital audio, teletext, captioning, etc. during the blanking intervals.

The EAV and SAV sequences must have priority over active video data or ancillary data to ensure that correct video timing is always maintained at the receiver. The receiver decodes the EAV and SAV sequences to recover the video timing.

The video timing sequence of the encoder is controlled by three timing signals discussed in Chapter 4: H (horizontal blanking), V (vertical blanking), and F (Field 1 or Field 2). A zero-to-one transition of H triggers an EAV sequence while a one-to-zero transition triggers an SAV sequence. F and V are allowed to change only at EAV sequences.

Usually, both 8-bit and 10-bit interfaces are supported, with the 10-bit interface used to transmit 2 bits of fractional video data to minimize cumulative processing errors and to support 10-bit ancillary data.

YCbCr or R′G′B′ data may not use the 10-bit values of 0x000–0x003 and 0x3FC–0x3FF, or the 8-bit values of 0x00 and 0xFF, since they are used for timing information.

Active Resolution (H × V)	Total Resolution[1] (H × V)	Display Aspect Ratio	Frame Rate (Hz)	1× Y Sample Rate (MHz)	SDTV or HDTV	Digital Parallel Standard	Digital Serial Standard
720 × 480i	858 × 525i	4:3	29.97	13.5	SDTV	BT.656 BT.799 SMPTE 125M	BT.656 BT.799
720 × 480p	858 × 525p	4:3	59.94	27	SDTV	–	BT.1362 SMPTE 294M
720 × 576i	864 × 625i	4:3	25	13.5	SDTV	BT.656 BT.799	BT.656 BT.799
720 × 576p	864 × 625p	4:3	50	27	SDTV	–	BT.1362
960 × 480i	1144 × 525i	16:9	29.97	18	SDTV	BT.1302 BT.1303 SMPTE 267M	BT.1302 BT.1303
960 × 576i	1152 × 625i	16:9	25	18	SDTV	BT.1302 BT.1303	BT.1302 BT.1303
1280 × 720p	1650 × 750p	16:9	59.94	74.176	HDTV	SMPTE 274M	–
1280 × 720p	1650 × 750p	16:9	60	74.25	HDTV	SMPTE 274M	–
1920 × 1080i	2200 × 1125i	16:9	29.97	74.176	HDTV	BT.1120 SMPTE 274M	BT.1120 SMPTE 292M
1920 × 1080i	2200 × 1125i	16:9	30	74.25	HDTV	BT.1120 SMPTE 274M	BT.1120 SMPTE 292M
1920 × 1080p	2200 × 1125p	16:9	59.94	148.35	HDTV	BT.1120 SMPTE 274M	–
1920 × 1080p	2200 × 1125p	16:9	60	148.5	HDTV	BT.1120 SMPTE 274M	–
1920 × 1080i	2376 × 1250i	16:9	25	74.25	HDTV	BT.1120	BT.1120
1920 × 1080p	2376 × 1250p	16:9	50	148.5	HDTV	BT.1120	–

Table 6.1. Pro-Video Parallel and Serial Digital Interface Standards for Various Component Video Formats. [1]i = interlaced, p = progressive.

The EAV and SAV sequences are shown in Table 6.2. The status word is defined as:

F = "0" for Field 1 F = "1" for Field 2
V = "1" during vertical blanking
H = "0" at SAV H = "1" at EAV
P3–P0 = protection bits

$P3 = V \oplus H$
$P2 = F \oplus H$
$P1 = F \oplus V$
$P0 = F \oplus V \oplus H$

where $\oplus$ represents the exclusive-OR function. These protection bits enable 1- and 2-bit errors to be detected and 1-bit errors to be corrected at the receiver. For most progressive video systems, F is usually a "0" since there is no field information.

For 4:2:2 YCbCr data, after each SAV sequence, the stream of active data words always begins with a Cb sample, as shown in Figure 6.1. In the multiplexed sequence, the co-sited samples (those that correspond to the same point on the picture) are grouped as Cb, Y, Cr. During blanking intervals, unless ancillary data is present, 10-bit Y or R′G′B′ values should be set to 0x040 and 10-bit CbCr values should be set to 0x200.

The receiver detects the EAV and SAV sequences by looking for the 8-bit 0xFF 0x00 0x00 preamble. The status word (optionally error corrected at the receiver, see Table 6.3) is used to recover the H, V, and F timing signals.

Ancillary Data

Ancillary data packets are used to transmit non-video information (such as digital audio, closed captioning, teletext, etc.) during the blanking intervals. A wide variety of ITU-R and SMPTE specifications describe the various ancillary data formats.

During horizontal blanking, ancillary data may be transmitted in the interval between the EAV and SAV sequences. During vertical blanking, ancillary data may be transmitted in the interval between the SAV and EAV sequences. Multiple ancillary packets may be present in a horizontal or vertical blanking interval, but they must be contiguous with each other.

	8-bit Data								10-bit Data	
	D9 (MSB)	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
preamble	1	1	1	1	1	1	1	1	1	1
	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0
status word	1	F	V	H	P3	P2	P1	P0	0	0

Table 6.2. EAV and SAV Sequence.

Received D5–D2	Received F, V, H (Bits D8–D6)							
	000	**001**	**010**	**011**	**100**	**101**	**110**	**111**
0000	000	000	000	*	000	*	*	111
0001	000	*	*	111	*	111	111	111
0010	000	*	*	011	*	101	*	*
0011	*	*	010	*	100	*	*	111
0100	000	*	*	011	*	*	110	*
0101	*	001	*	*	100	*	*	111
0110	*	011	011	011	100	*	*	011
0111	100	*	*	011	100	100	100	*
1000	000	*	*	*	*	101	110	*
1001	*	001	010	*	*	*	*	111
1010	*	101	010	*	101	101	*	101
1011	010	*	010	010	*	101	010	*
1100	*	001	110	*	110	*	110	110
1101	001	001	*	001	*	001	110	*
1110	*	*	*	011	*	101	110	*
1111	*	001	010	*	100	*	*	*

Notes:
* = uncorrectable error.

Table 6.3. SAV and EAV Error Correction at Decoder.

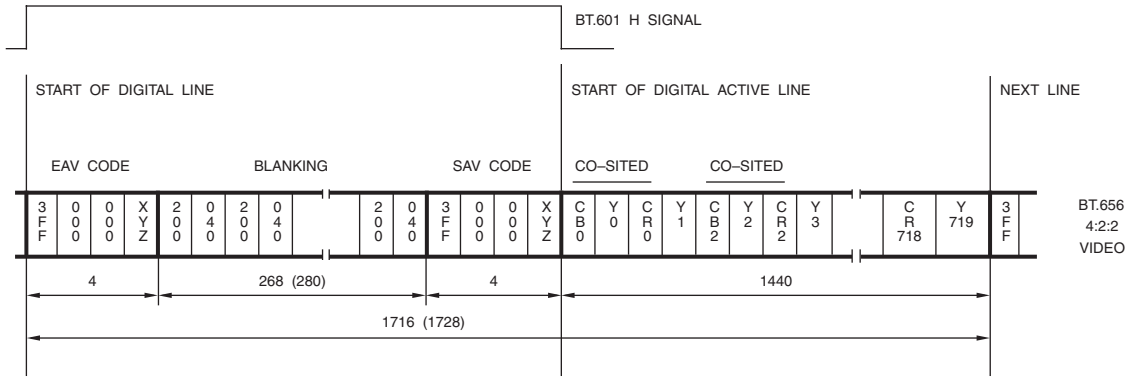


Figure 6.1. BT.656 Parallel Interface Data For One Scan Line. 480i; 4:2:2 YCbCr; 720 active samples per line; 27 MHz clock; 10-bit system. The values for 576i systems are shown in parentheses.

There are two types of ancillary data formats. The older Type 1 format uses a single data ID word to indicate the type of ancillary data; the newer Type 2 format uses two words for the data ID. The general packet format is shown in Table 6.4.

Data ID (DID)

DID indicates the type of data being sent. The assignment of most of the DID values is controlled by the ITU and SMPTE to ensure equipment compatibility. A few DID values are available that don't require registration.

Secondary ID (SDID, Type 2 Only)

SDID is also part of the data ID for Type 2 ancillary formats. The assignment of most of the SDID values is also controlled by the ITU and SMPTE to ensure equipment compatibility. A few SDID values are available that don't require registration.

Data Block Number (DBN, Type 1 Only)

DBN is used to allow multiple ancillary packets (sharing the same DID) to be put back together at the receiver. This is the case when there are more than 255 user data words required to be transmitted, thus requiring more than one ancillary packet to be used. The DBN value increments by one for each consecutive ancillary packet.

Data Count (DC)

DC specifies the number of user data words in the packet. In 8-bit applications, it specifies the six MSBs of an 8-bit value, so the number of user data words must be an integral number of four.

User Data Words (UDW)

Up to 255 user data words may be present in the packet. In 8-bit applications, the number of user data words must be an integral number of four. Padding words may be added to ensure an integral number of four user data words are present.

User data may not use the 10-bit values of 0x000–0x003 and 0x3FC–0x3FF, or the 8-bit values of 0x00 and 0xFF, since they are used for timing information.

Parallel Interfaces

25-pin Parallel Interface

This interface is used to transfer SDTV resolution 4:2:2 YCbCr data. 8-bit or 10-bit data and a clock are transferred. The individual bits are labeled D0–D9, with D9 being the most significant bit. The pin allocations for the signals are shown in Table 6.5.

Y has a nominal 10-bit range of 0x040–0x3AC. Values less than 0x040 or greater than 0x3AC may be present due to processing. During blanking, Y data should have a value of 040_H, unless other information is present.

Cb and Cr have a nominal 10-bit range of 0x040–0x3C0. Values less than 0x040 or greater than 0x3C0 may be present due to processing. During blanking, CbCr data should have a value of 0x200, unless other data is present.

Signal levels are compatible with ECL-compatible balanced drivers and receivers. The generator must have a balanced output with a maximum source impedance of 110 Ω; the signal must be 0.8–2.0V peak-to-peak measured across a 110-Ω load. At the receiver, the transmission line is terminated by 110 ±10 Ω.

	8-bit Data								10-bit Data	
	D9 (MSB)	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ancillary data flag (ADF)	0	0	0	0	0	0	0	0	0	0
	1	1	1	1	1	1	1	1	1	1
	1	1	1	1	1	1	1	1	1	1
data ID (DID)	$\overline{D8}$	even parity	value of 0000 0000 to 1111 1111							
data block number or SDID	$\overline{D8}$	even parity	value of 0000 0000 to 1111 1111							
data count (DC)	$\overline{D8}$	even parity	value of 0000 0000 to 1111 1111							
user data word 0	value of 00 0000 0100 to 11 1111 1011									
:										
user data word N	value of 00 0000 0100 to 11 1111 1011									
checksum	$\overline{D8}$	sum of D0–D8 of data ID through last user data word. Preset to all zeros; carry is ignored.								

Table 6.4. Ancillary Data Packet General Format.

Pin	Signal	Pin	Signal
1	clock	**14**	clock–
2	system ground A	**15**	system ground B
3	D9	**16**	D9–
4	D8	**17**	D8–
5	D7	**18**	D7–
6	D6	**19**	D6–
7	D5	**20**	D5–
8	D4	**21**	D4–
9	D3	**22**	D3–
10	D2	**23**	D2–
11	D1	**24**	D1–
12	D0	**25**	D0–
13	cable shield		

Table 6.5. 25-Pin Parallel Interface Connector Pin Assignments. For 8-bit interfaces, D9–D2 are used.

27 MHz Parallel Interface

This BT.656 and SMPTE 125M interface is used for 480i and 576i systems with an aspect ratio of 4:3. Y and multiplexed CbCr information at a sample rate of 13.5 MHz are multiplexed into a single 8-bit or 10-bit data stream, at a clock rate of 27 MHz.

The 27 MHz clock signal has a clock pulse width of 18.5 ±3 ns. The positive transition of the clock signal occurs midway between data transitions with a tolerance of ±3 ns (as shown in Figure 6.2).

To permit reliable operation at interconnect lengths of 50–200 meters, the receiver must use frequency equalization, with typical characteristics shown in Figure 6.3. This example enables operation with a range of cable lengths down to zero.

36 MHz Parallel Interface

This BT.1302 and SMPTE 267M interface is used for 480i and 576i systems with an aspect ratio of 16:9. Y and multiplexed CbCr information at a sample rate of 18 MHz are multiplexed into a single 8-bit or 10-bit data stream, at a clock rate of 36 MHz.

The 36 MHz clock signal has a clock pulse width of 13.9 ±2 ns. The positive transition of the clock signal occurs midway between data transitions with a tolerance of ±2 ns (as shown in Figure 6.4.

To permit reliable operation at interconnect lengths of 40–160 meters, the receiver must use frequency equalization, with typical characteristics shown in Figure 6.3.

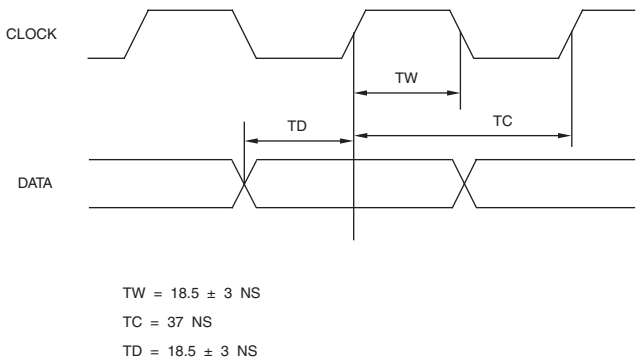


Figure 6.2. 25-Pin 27 MHz Parallel Interface Waveforms.

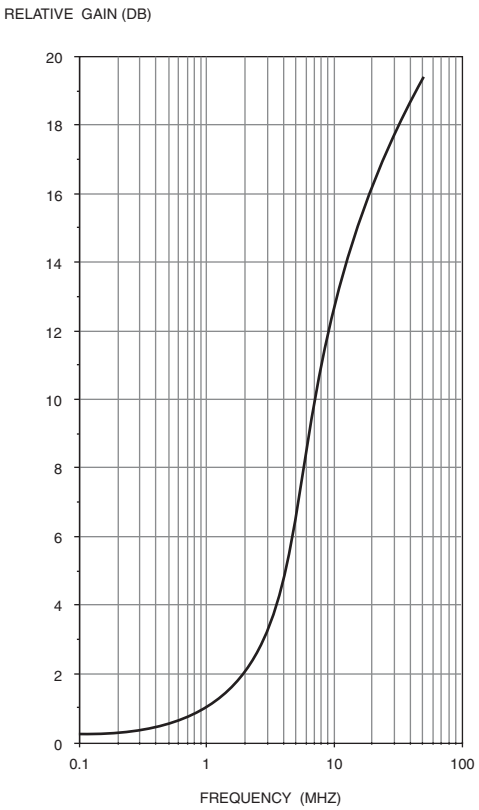


Figure 6.3. Example Line Receiver Equalization Characteristics for Small Signals.

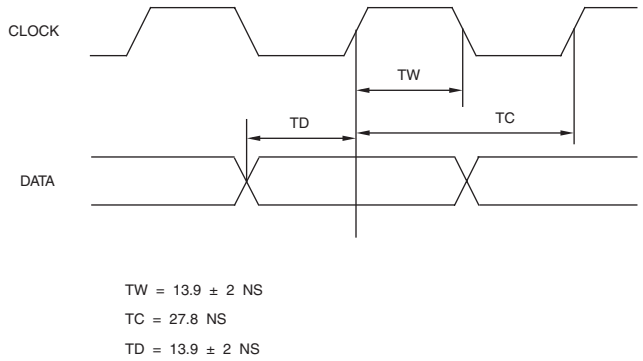


Figure 6.4. 25-Pin 36 MHz Parallel Interface Waveforms.

93-pin Parallel Interface

This interface is used to transfer HDTV resolution R′G′B′ data, 4:2:2 YCbCr data, or 4:2:2:4 YCbCrK data. The pin allocations for the signals are shown in Table 6.6. The most significant bits are R9, G9, and B9.

When transferring 4:2:2 YCbCr data, the green channel carries Y information and the red channel carries multiplexed CbCr information.

When transferring 4:2:2:4 YCbCrK data, the green channel carries Y information, the red channel carries multiplexed CbCr information, and the blue channel carries K (alpha keying) information.

Y has a nominal 10-bit range of 0x040–0x3AC. Values less than 040_H or greater than 0x3AC may be present due to processing. During blanking, Y data should have a value of 0x040, unless other information is present.

Cb and Cr have a nominal 10-bit range of 0x040–0x3C0. Values less than 0x040 or greater than 0x3C0 may be present due to processing. During blanking, CbCr data should have a value of 0x200, unless other information is present.

R′G′B′ and K have a nominal 10-bit range of 0x040–0x3AC. Values less than 0x040 or greater than 0x3AC may be present due to processing. During blanking, R′G′B′ data should have a value of 0x040, unless other information is present.

Signal levels are compatible with ECL-compatible balanced drivers and receivers. The generator must have a balanced output with a maximum source impedance of 110 Ω; the signal must be 0.6–2.0V peak-to-peak measured across a 110-Ω load. At the receiver, the transmission line must be terminated by 110 ±10 Ω.

74.25 and 74.176 MHz Parallel Interface

This ITU-R BT.1120 and SMPTE 274M interface is primarily used for HDTV systems.

The 74.25 or 74.176 MHz (74.25/1.001) clock signal has a clock pulse width of 6.73 ±1.48 ns. The positive transition of the clock signal occurs midway between data transitions with a tolerance of ±1 ns (as shown in Figure 6.5).

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	clock	**26**	GND	**51**	B2	**76**	GND
2	G9	**27**	GND	**52**	B1	**77**	GND
3	G8	**28**	GND	**53**	B0	**78**	GND
4	G7	**29**	GND	**54**	R9	**79**	B4–
5	G6	**30**	GND	**55**	R8	**80**	B3–
6	G5	**31**	GND	**56**	R7	**81**	B2–
7	G4	**32**	GND	**57**	R6	**82**	B1–
8	G3	**33**	clock–	**58**	R5	**83**	B0–
9	G2	**34**	G9–	**59**	R4	**84**	R9–
10	G1	**35**	G8–	**60**	R3	**85**	R8–
11	G0	**36**	G7–	**61**	R2	**86**	R7–
12	B9	**37**	G6–	**62**	R1	**87**	R6–
13	B8	**38**	G5–	**63**	R0	**88**	R5–
14	B7	**39**	G4–	**64**	GND	**89**	R4–
15	B6	**40**	G3–	**65**	GND	**90**	R3–
16	B5	**41**	G2–	**66**	GND	**91**	R2–
17	GND	**42**	G1–	**67**	GND	**92**	R1–
18	GND	**43**	G0–	**68**	GND	**93**	R0–
19	GND	**44**	B9–	**69**	GND		
20	GND	**45**	B8–	**70**	GND		
21	GND	**46**	B7–	**71**	GND		
22	GND	**47**	B6–	**72**	GND		
23	GND	**48**	B5–	**73**	GND		
24	GND	**49**	B4	**74**	GND		
25	GND	**50**	B3	**75**	GND		

Table 6.6. 93-Pin Parallel Interface Connector Pin Assignments. For 8-bit interfaces, bits 9–2 are used.

To permit reliable operation at interconnect lengths greater than 20 meters, the receiver must use frequency equalization.

148.5 and 148.35 MHz Parallel Interface

This BT.1120 and SMPTE 274M interface is used for HDTV systems.

The 148.5 or 148.35 MHz (148.5/1.001) clock signal has a clock pulse width of 3.37 ±0.74 ns. The positive transition of the clock signal occurs midway between data transitions with a tolerance of ±0.5 ns (similar to Figure 6.5).

To permit reliable operation at interconnect lengths greater than 14 meters, the receiver must use frequency equalization.

Applications

One or more parallel interfaces may be used to transfer various video formats between equipment.

4:2:2 YCbCr - Interlaced SDTV

The ITU-R BT.656 and BT.1302 parallel interfaces were developed to transfer BT.601 4:2:2 YCbCr digital video between equipment. SMPTE 125M and 267M further clarify the operation for 480i systems.

Figure 6.6 illustrates the timing for one scan line for the 4:3 aspect ratio, using a 27 MHz sample clock. Figure 6.7 shows the timing for one scan line for the 16:9 aspect ratio, using a 36 MHz sample clock. The 25-pin parallel interface is used.

4:4:4:4 YCbCrK - Interlaced SDTV

The ITU-R BT.799 and BT.1303 parallel interfaces were developed to transfer BT.601 4:4:4:4 YCbCrK digital video between equipment. K is an alpha keying signal, used to mix two video sources, discussed in Chapter 7. SMPTE RP-175 further clarifies the operation for 480i systems.

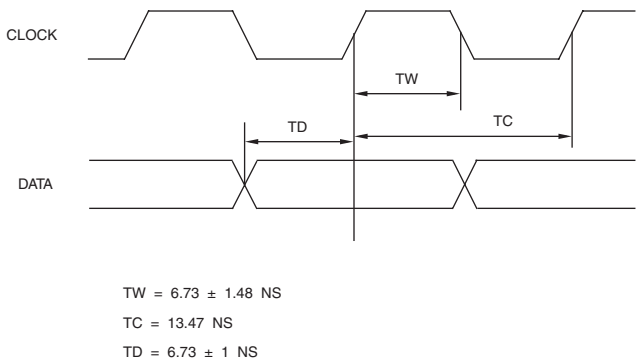


Figure 6.5. 93-Pin 74.25 and 74.176 MHz Parallel Interface Waveforms.

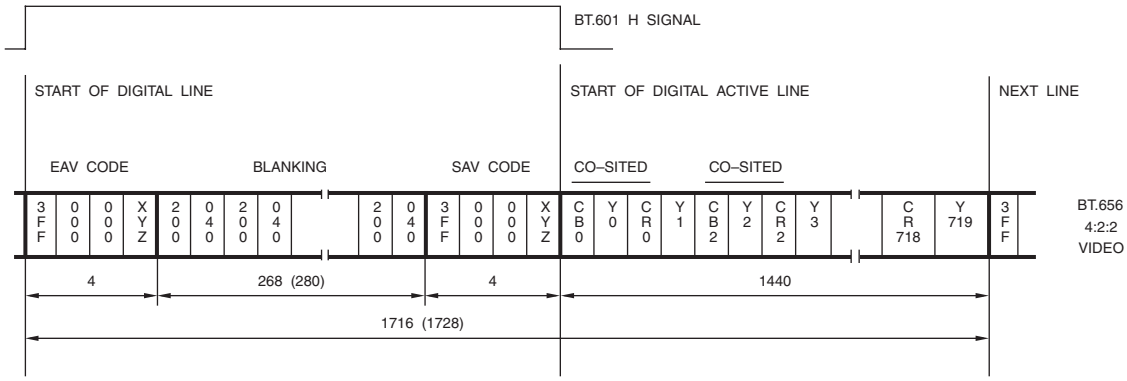


Figure 6.6. BT.656 and SMPTE 125M Parallel Interface Data for One Scan Line. 480i; 4:2:2 YCbCr; 720 active samples per line; 27 MHz clock; 10-bit system. The values for 576i systems are shown in parentheses.

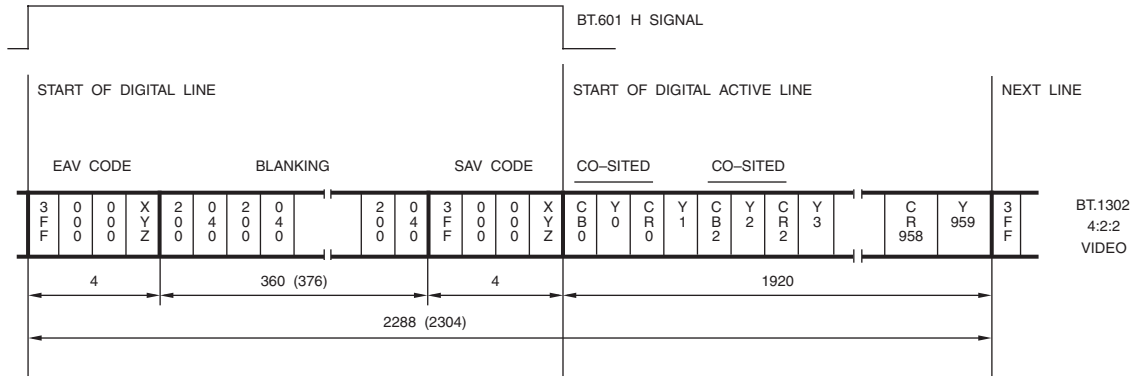


Figure 6.7. BT.1302 and SMPTE 267M Parallel Interface Data for One Scan Line. 480i; 4:2:2 YCbCr; 960 active samples per line; 36 MHz clock; 10-bit system. The values for 576i systems are shown in parentheses.

Two transmission links are used. Link A contains all the Y samples plus those Cb and Cr samples located at even-numbered sample points. Link B contains samples from the keying channel and the Cb and Cr samples from the odd-numbered sampled points. Although it may be common to refer to Link A as 4:2:2 and Link B as 2:2:4, Link A is not a true 4:2:2 signal since the CbCr data was sampled at 13.5 MHz, rather than 6.75 MHz.

Figure 6.8 shows the contents of links A and B when transmitting 4:4:4:4 YCbCrK video data. Figure 6.9 illustrates the contents when transmitting R′G′B′K video data. If the keying signal (K) is not present, the K sample values should have a 10-bit value of $3AC_H$.

Figure 6.10 illustrates the YCbCrK timing for one scan line for the 4:3 aspect ratio, using a 27 MHz sample clock. Figure 6.11 shows the YCbCrK timing for one scan line for the 16:9 aspect ratio, using a 36 MHz sample clock. Two 25-pin parallel interfaces are used.

RGBK - Interlaced SDTV

BT.799 and BT.1303 also support transferring BT.601 R′G′B′K digital video between equipment. For additional information, see the 4:4:4:4 YCbCrK interface. SMPTE RP-175 further clarifies the operation for 480i systems. The G′ samples are sent in the Y locations, the R′ samples are sent in the Cr locations, and the B′ samples are sent in the Cb locations.

4:2:2 YCbCr - Progressive SDTV

ITU-R BT.1362 defines two 10-bit 4:2:2 YCbCr data streams (Figure 6.12), using a 27 MHz sample clock. SMPTE 294M further clarifies the operation for 480p systems. What stream is used for which scan line is shown in Table 6.7.

4:2:2 YCbCr - Interlaced HDTV

The ITU-R BT.1120 parallel interface was developed to transfer interlaced HDTV 4:2:2 YCbCr digital video between equipment. SMPTE 274M further clarifies the operation for 29.97 and 30 Hz systems.

Figure 6.13 illustrates the timing for one scan line for the 1920 × 1080i active resolutions. The 93-pin parallel interface is used with a sample clock rate of 74.25 MHz (25 or 30 Hz frame rate) or 74.176 MHz (29.97 Hz frame rate).

4:2:2:4 YCbCrK - Interlaced HDTV

BT.1120 also supports transferring HDTV 4:2:2:4 YCbCrK digital video between equipment. SMPTE 274M further clarifies the operation for 29.97 and 30 Hz systems.

Figure 6.14 illustrates the timing for one scan line for the 1920 × 1080i active resolutions. The 93-pin parallel interface is used with a sample clock rate of 74.25 MHz (25 or 30 Hz frame rate) or 74.176 MHz (29.97 Hz frame rate).

RGB - Interlaced HDTV

BT.1120 also supports transferring HDTV R′G′B′ digital video between equipment. SMPTE 274M further clarifies the operation for 29.97 and 30 Hz systems.

Figure 6.15 illustrates the timing for one scan line for the 1920 × 1080i active resolutions. The 93-pin parallel interface is used with a sample clock rate of 74.25 MHz (25 or 30 Hz frame rate) or 74.176 MHz (29.97 Hz frame rate).

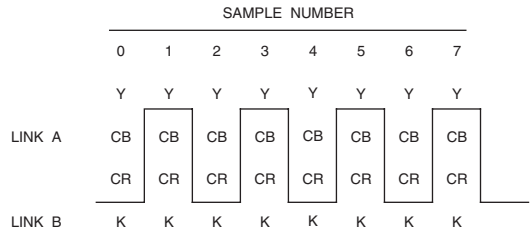


Figure 6.8. Link Content Representation for YCbCrK Video Signals.

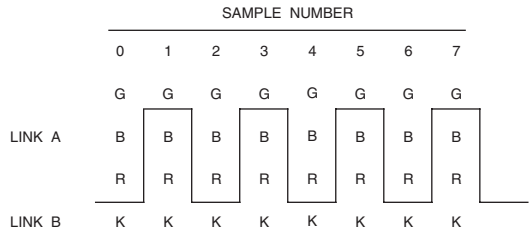


Figure 6.9. Link Content Representation for R′G′B′K Video Signals.

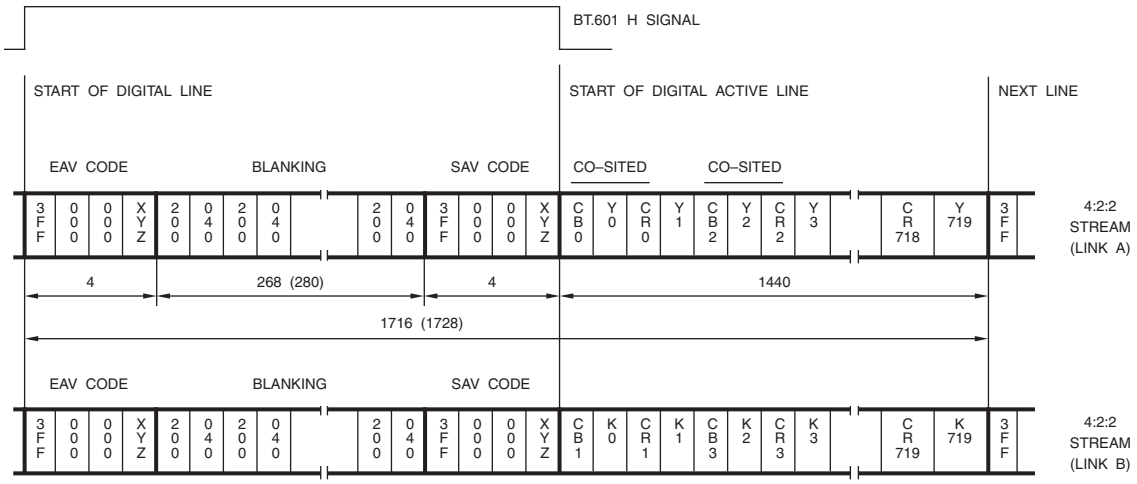


Figure 6.10. BT.799 and SMPTE RP-175 Parallel Interface Data for One Scan Line. 480i; 4:4:4:4 YCbCrK; 720 active samples per line; 27 MHz clock; 10-bit system. The values for 576i systems are shown in parentheses.

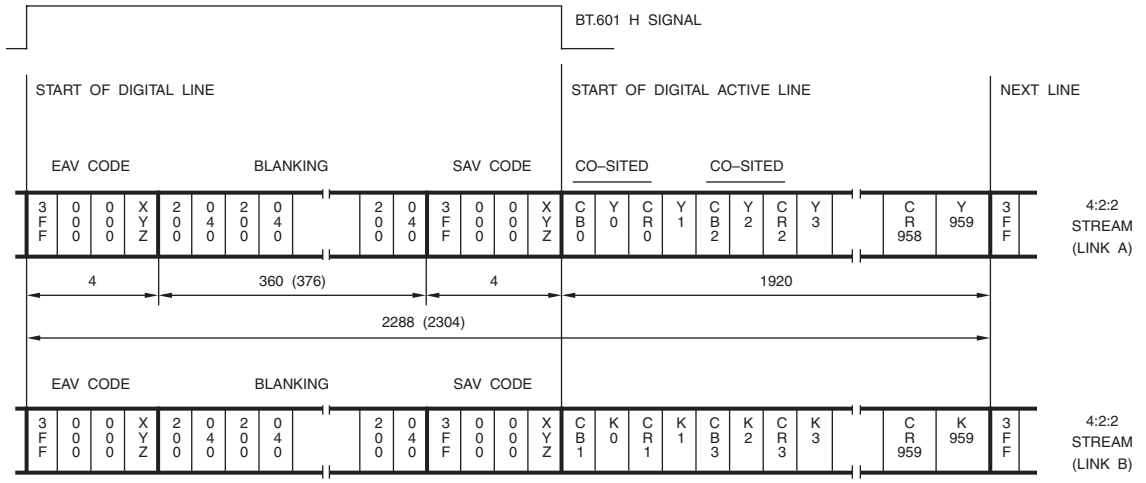


Figure 6.11. BT.1303 Parallel Interface Data for One Scan Line. 480i; 4:4:4:4 YCbCrK; 960 active samples per line; 36 MHz clock; 10-bit system. The values for 576i systems are shown in parentheses.

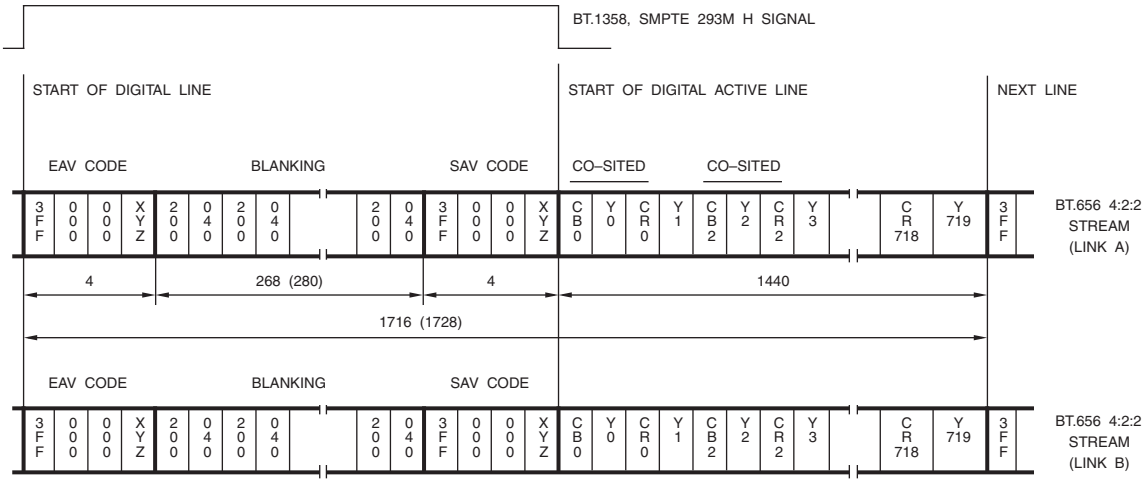


Figure 6.12. BT.1362 and SMPTE 294M Parallel Data for Two Scan Lines. 480p; 4:2:2 YCbCr; 720 active samples per line; 27 MHz clock; 10-bit system. The values for 576p systems are shown in parentheses.

480p (525p) System				576p (625p) System			
Link A	**Link B**	**Link A**	**Link B**	**Link A**	**Link B**	**Link A**	**Link B**
7	8	6	7	1	2	4	5
9	10	:	:	3	4	6	7
:	:	522	523	:	:	8	9
523	524	524	525	621	622	:	:
525	1	1	2	623	624	620	621
2	3	3	4	625	1	622	623
4	5	5	6	2	3	624	625

Table 6.7. BT.1362 and SMPTE 294M Scan Line Numbering and Link Assignment.

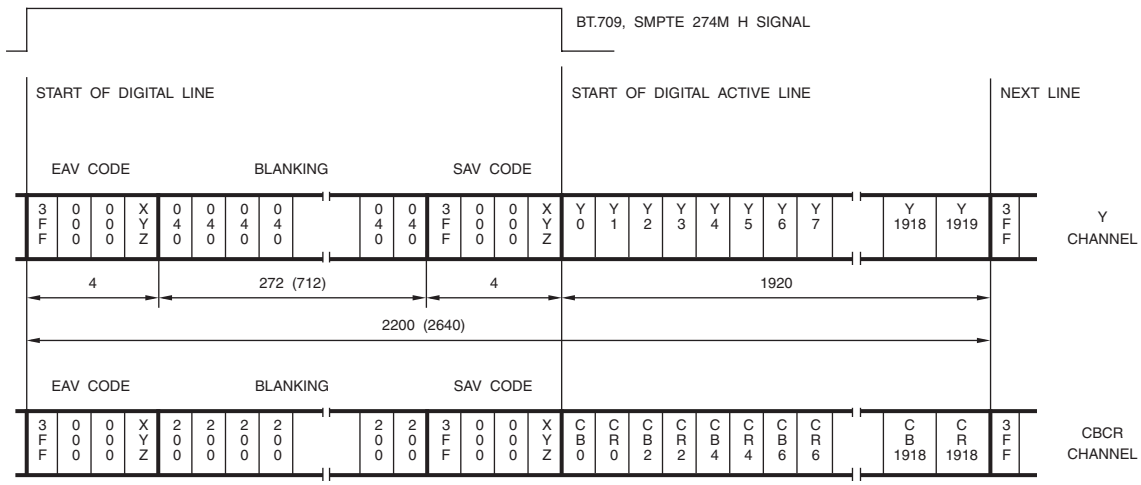


Figure 6.13. BT.1120 and SMPTE 274M Parallel Interface Data for One Scan Line. 1080i29.97, 1080i30, 1080p59.94, and 1080p60 systems; 4:2:2 YCbCr; 1920 active samples per line; 74.176, 74.25, 148.35, or 148.5 MHz clock; 10-bit system. The values for 1080i25 and 1080p50 systems are shown in parentheses.

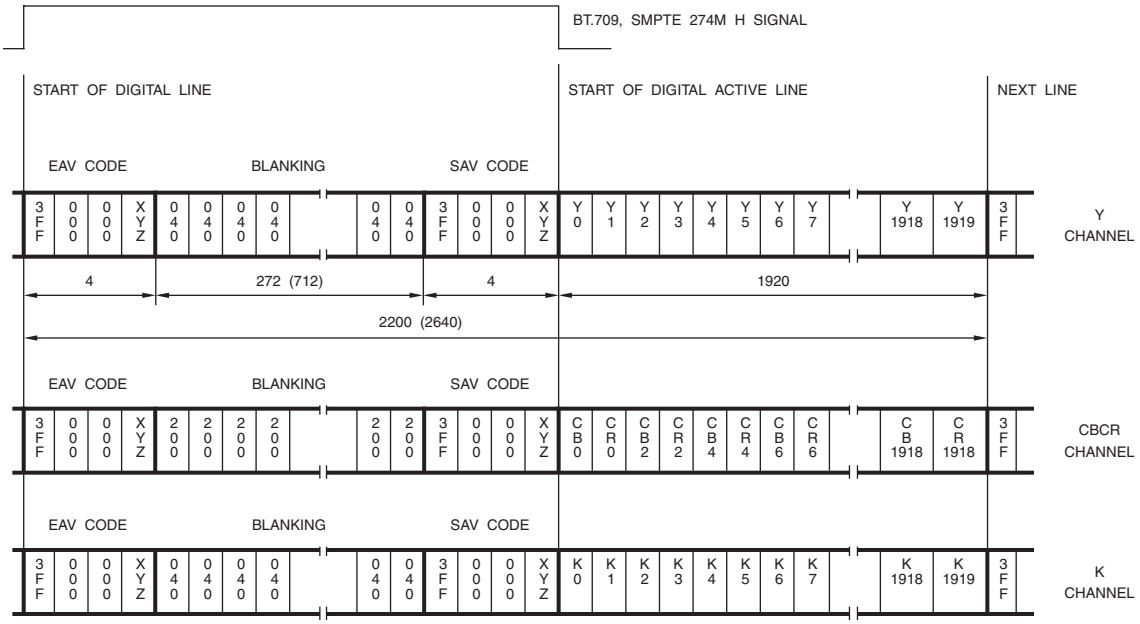


Figure 6.14. BT.1120 and SMPTE 274M Parallel Interface Data for One Scan Line. 1080i29.97, 1080i30, 1080p59.94, and 1080p60 systems; 4:2:2:4 YCbCrK; 1920 active samples per line; 74.176, 74.25, 148.35, or 148.5 MHz clock; 10-bit system. The values for 1080i25 and 1080p50 systems are shown in parentheses.

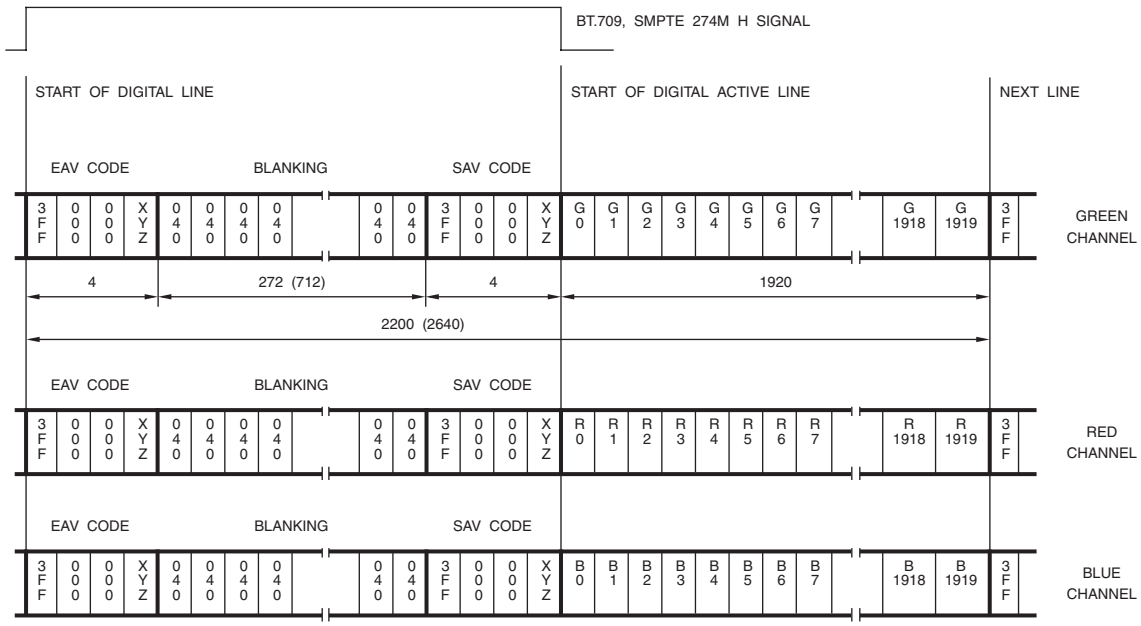


Figure 6.15. BT.1120 and SMPTE 274M Parallel Interface Data for One Scan Line. 1080i29.97, 1080i30, 1080p59.94, and 1080p60 systems; R′G′B′; 1920 active samples per line; 74.176, 74.25, 148.35, or 148.5 MHz clock; 10-bit system. The values for 1080i25 and 1080p50 systems are shown in parentheses.

4:2:2 YCbCr - Progressive HDTV

The ITU-R BT.1120 and SMPTE 274M parallel interfaces were developed to transfer progressive HDTV 4:2:2 YCbCr digital video between equipment.

Figure 6.13 illustrates the timing for one scan line for the 1920 × 1080p active resolutions. The 93-pin parallel interface is used with a sample clock rate of 148.5 MHz (24, 25, 30, 50, or 60 Hz frame rate) or 148.35 MHz (23.98, 29.97, or 59.94 Hz frame rate).

Figure 6.16 illustrates the timing for one scan line for the 1280 × 720p active resolutions. The 93-pin parallel interface is used with a sample clock rate of 74.25 MHz (24, 25, 30, 50, or 60 Hz frame rate) or 74.176 MHz (23.98, 29.97, or 59.94 Hz frame rate).

4:2:2:4 YCbCrK - Progressive HDTV

BT.1120 and SMPTE 274M also support transferring HDTV 4:2:2:4 YCbCrK digital video between equipment.

Figure 6.14 illustrates the timing for one scan line for the 1920 × 1080p active resolutions. The 93-pin parallel interface is used with a sample clock rate of 148.5 MHz (24, 25, 30, 50, or 60 Hz frame rate) or 148.35 MHz (23.98, 29.97, or 59.94 Hz frame rate).

Figure 6.17 illustrates the timing for one scan line for the 1280 × 720p active resolutions. The 93-pin parallel interface is used with a sample clock rate of 74.25 MHz (24, 25, 30, 50, or 60 Hz frame rate) or 74.176 MHz (23.98, 29.97, or 59.94 Hz frame rate).

RGB - Progressive HDTV

BT.1120 and SMPTE 274M also support transferring HDTV R′G′B′ digital video between equipment.

Figure 6.15 illustrates the timing for one scan line for the 1920 × 1080p active resolutions. The 93-pin parallel interface is used with a sample clock rate of 148.5 MHz (24, 25, 30, 50, or 60 Hz frame rate) or 148.35 MHz (23.98, 29.97, or 59.94 Hz frame rate).

Figure 6.18 illustrates the timing for one scan line for the 1280 × 720p active resolutions. The 93-pin parallel interface is used with a sample clock rate of 74.25 MHz (24, 25, 30, 50, or 60 Hz frame rate) or 74.176 MHz (23.98, 29.97, or 59.94 Hz frame rate).

Serial Interfaces

The parallel formats can be converted to a serial format (Figure 6.19), allowing data to be transmitted using a 75-Ω coaxial cable or optical fiber.

For cable interconnect, the generator has an unbalanced output with a source impedance of 75 Ω; the signal must be 0.8V ±10% peak-to-peak measured across a 75-Ω load. The receiver has an input impedance of 75 Ω.

In an 8-bit environment, before serialization, the 0x00 and 0xFF codes during EAV and SAV are expanded to 10-bit values of 0x000 and 0x3FF, respectively. All other 8-bit data is appended with two least significant "0" bits before serialization.

The 10 bits of data are serialized (LSB first) and processed using a scrambled and polarity-free NRZI algorithm:

$$G(x) = (x^9 + x^4 + 1)(x + 1)$$

The input signal to the scrambler (Figure 6.20) uses positive logic (the highest voltage represents a logical one; lowest voltage represents a logical zero).

The formatted serial data is output at the 10× sample clock rate. Since the parallel clock may contain large amounts of jitter, deriving the 10× sample clock directly from an unfiltered parallel clock may result in excessive signal jitter.

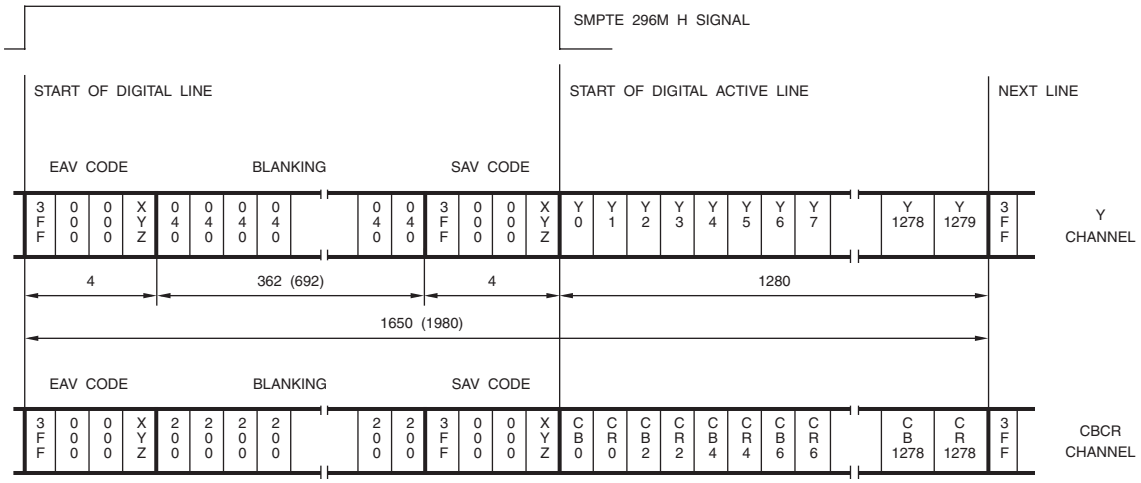


Figure 6.16. SMPTE 274M Parallel Interface Data for One Scan Line. 720p59.94 and 720p60 systems; 4:2:2 YCbCr; 1280 active samples per line; 74.176 or 74.25 MHz clock; 10-bit system. The values for 720p50 systems are shown in parentheses.

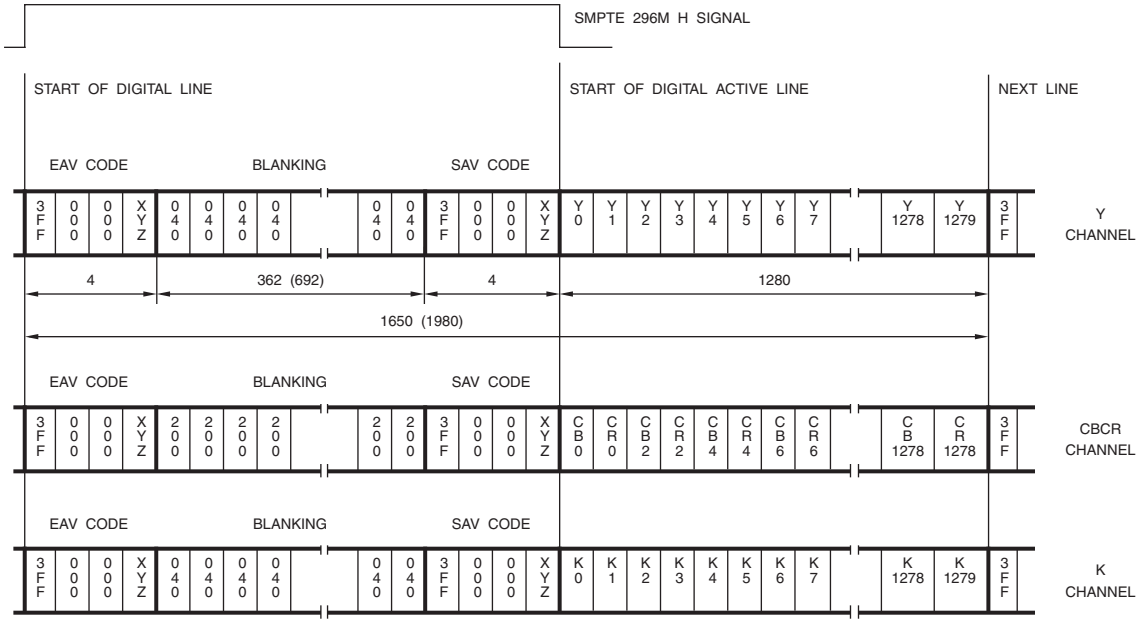


Figure 6.17. SMPTE 274M Parallel Interface Data for One Scan Line. 720p59.94 and 720p60 systems; 4:2:2:4 YCbCrK; 1280 active samples per line; 74.176 or 74.25 MHz clock; 10-bit system. The values for 720p50 systems are shown in parentheses.

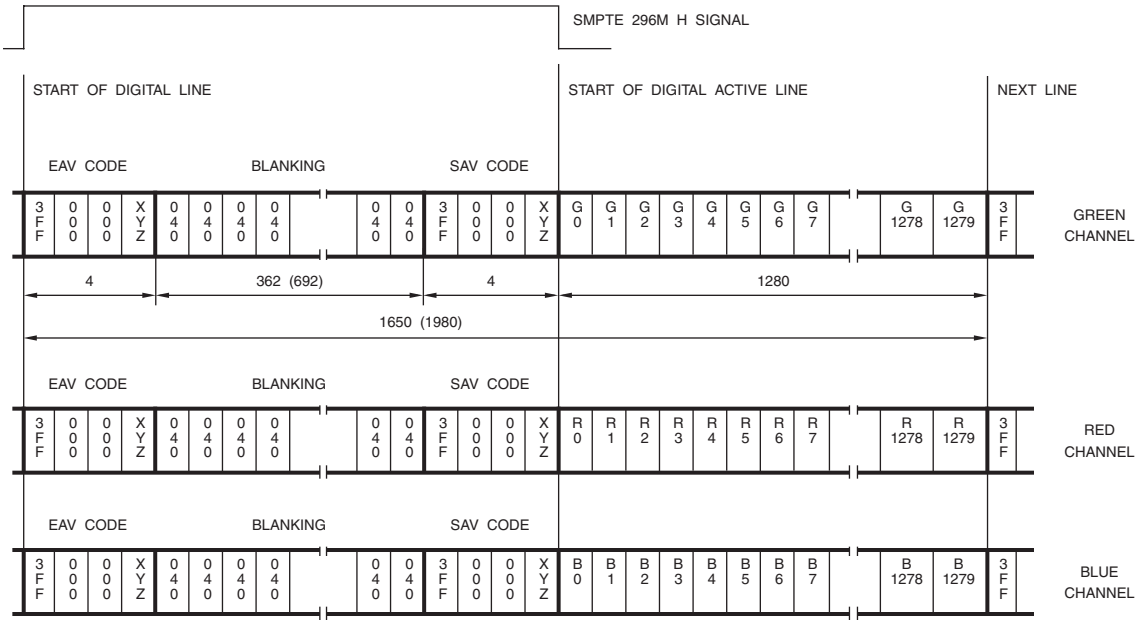


Figure 6.18. SMPTE 274M Parallel Interface Data for One Scan Line. 720p59.94 and 720p60 systems; R′G′B′; 1280 active samples per line; 74.176 or 74.25 MHz clock; 10-bit system. The values for 720p50 systems are shown in parentheses.

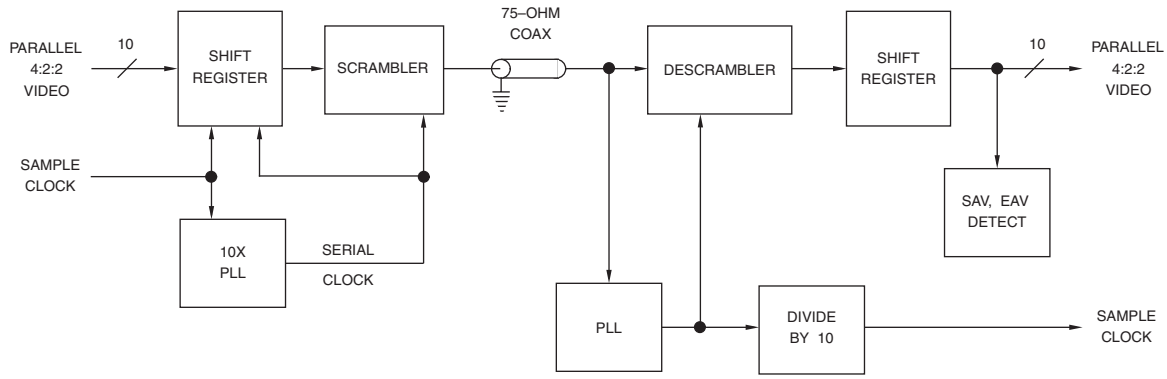


Figure 6.19. Serial Interface Block Diagram.

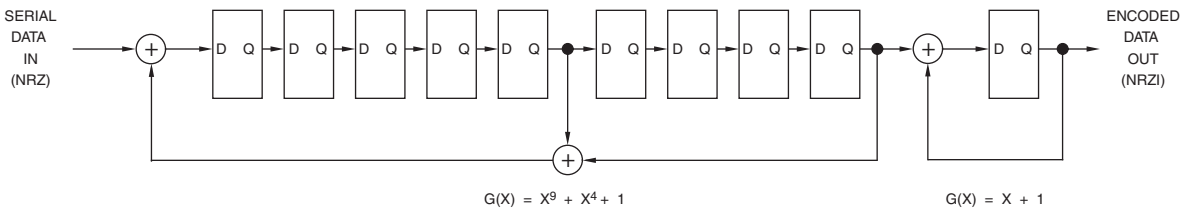


Figure 6.20. Typical Scrambler Circuit.

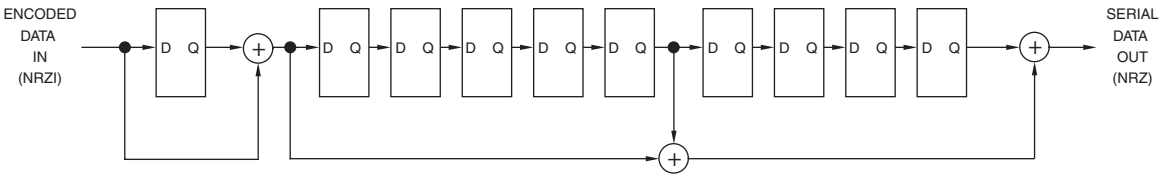


Figure 6.21. Typical Descrambler Circuit.

At the receiver, phase-lock synchronization is done by detecting the EAV and SAV sequences. The PLL is continuously adjusted slightly each scan line to ensure that these patterns are detected and to avoid bit slippage. The recovered 10× sample clock is divided by ten to generate the sample clock, although care must be taken not to mask word-related jitter components. The serial data is low- and high-frequency equalized, inverse scrambling performed (Figure 6.21), and deserialized.

270 Mbps Serial Interface

This BT.656 and SMPTE 259M interface (also called SDI) converts a 27 MHz parallel stream into a 270 Mbps serial stream. The 10× PLL generates a 270 MHz clock from the 27 MHz clock signal. This interface is primarily used for 480i and 576i 4:3 systems.

360 Mbps Serial Interface

This BT.1302 and SMPTE 259M interface converts a 36 MHz parallel stream into a 360 Mbps serial stream. The 10× PLL generates a 360 MHz clock from the 36 MHz clock signal. This interface is primarily used for 480i and 576i 16:9 systems.

540 Mbps Serial Interface

This SMPTE 344M interface converts a 54 MHz parallel stream, or two 27 MHz parallel streams, into a 540 Mbps serial stream. The 10× PLL generates a 540 MHz clock from the 54 MHz clock signal. This interface is primarily used for 480p and 576p 4:3 systems.

1.485 and 1.4835 Gbps Serial Interface

This BT.1120 and SMPTE 292M interface multiplexes two 74.25 or 74.176 (74.25/1.001) MHz parallel streams (Y and CbCr) into a single 1.485 or 1.4835 Gbps serial stream. A 20× PLL generates a 1.485 GHz clock from the 74.25 or 74.176 MHz clock signal. This interface is used for HDTV systems.

Before multiplexing the two parallel streams together, line number and CRC information (Table 6.8) is added to each stream after each EAV sequence. The CRC is used to

	D9 (MSB)	D8	D7	D6	D5	D4	D3	D2	D1	D0
LN0	$\overline{D8}$	L6	L5	L4	L3	L2	L1	L0	0	0
LN1	$\overline{D8}$	0	0	0	L10	L9	L8	L7	0	0
CRC0	$\overline{D8}$	crc8	crc7	crc6	crc5	crc4	crc3	crc2	crc1	crc0
CRC1	$\overline{D8}$	crc17	crc16	crc15	crc14	crc13	crc12	crc11	crc10	crc9

Table 6.8. Line Number and CRC Data.

detect errors in the active video and EAV. It consists of two words generated by the polynomial:

$$CRC = x^{18} + x^5 + x^4 + 1$$

The initial value is set to zero. The calculation starts with the first active line word and ends at the last word of the line number (LN1).

Applications

One or more serial interfaces may be used to transfer various video formats between equipment.

RGBK - Interlaced SDTV

BT.799 and BT.1303 also define a R′G′B′K serial interface. The two 10-bit R′G′B′K parallel streams in Figure 6.10 are serialized using two 270 or 360 Mbps serial interfaces.

4:2:2 YCbCr - Progressive SDTV

ITU-R BT.1362 and SMPTE 294M also define a 4:2:2 YCbCr serial interface. The two 10-bit 4:2:2 YCbCr parallel streams in Figure 6.12 are serialized using two 270 Mbps serial interfaces.

4:2:2 YCbCr - Interlaced HDTV

BT.1120 and SMPTE 292M also define a 4:2:2 YCbCr serial interface. The two 10-bit 4:2:2 YCbCr parallel streams shown in Figure 6.13 are multiplexed together, then serialized using a 1.485 or 1.4835 Gbps serial interface.

Pro-Video Composite Interfaces

Digital composite video is essentially a digital version of a composite analog (M) NTSC or (B, D, G, H, I) PAL video signal. The sample clock rate is four times F_{SC}: about 14.32 MHz for (M) NTSC and about 17.73 MHz for (B, D, G, H, I) PAL.

Usually, both 8-bit and 10-bit interfaces are supported, with the 10-bit interface used to transmit 2 bits of fractional video data to minimize cumulative processing errors and to support 10-bit ancillary data.

Table 6.9 lists the digital composite levels. Video data may not use the 10-bit values of 0x000–0x003 and 0x3FC–0x3FF, or the 8-bit values of 0x00 and 0xFF, since they are used for timing information.

NTSC Video Timing

There are 910 total samples per scan line, as shown in Figure 6.22. Horizontal count 0 corresponds to the start of active video, and a horizontal count of 768 corresponds to the start of horizontal blanking.

Sampling is along the ±I and ±Q axes (33°, 123°, 213°, and 303°). The sampling phase at horizontal count 0 of line 10, Field 1 is on the +I axis (123°).

The sync edge values, and the horizontal counts at which they occur, are defined as shown in Figure 6.23 and Tables 6.10–6.12. 8-bit values for one color burst cycle are 45, 83, 75, and 37. The burst envelope starts at horizontal count 857, and lasts for 43 clock cycles, as shown in Table 6.10. Note that the peak amplitudes of the burst are not sampled.

To maintain zero SCH phase, horizontal count 784 occurs 25.6 ns (33° of the subcarrier phase) before the 50% point of the falling edge of horizontal sync, and horizontal count 785 occurs 44.2 ns (57° of the subcarrier phase) after the 50% point of the falling edge of horizontal sync.

PAL Video Timing

There are 1135 total samples per line, except for two lines per frame which have 1137 samples per line, making a total of 709,379 samples per frame. Figure 6.24 illustrates the typical line timing. Horizontal count 0 corresponds to the start of active video, and a horizontal count of 948 corresponds to the start of horizontal blanking.

Sampling is along the ±U and ±V axes (0°, 90°, 180°, and 270°), with the sampling phase at horizontal count 0 of line 1, Field 1 on the +V axis (90°).

8-bit color burst values are 95, 64, 32, and 64, continuously repeated. The swinging burst causes the peak burst (32 and 95) and zero burst (64) samples to change places. The burst envelope starts at horizontal count 1058, and lasts for 40 clock cycles.

Sampling is not H-coherent as with (M) NTSC, so the position of the sync pulses changes from line to line. Zero SCH phase is defined when alternate burst samples have a value of 64.

Ancillary Data

Ancillary data packets are used to transmit information (such as digital audio, closed captioning, and teletext data) during the blanking intervals. ITU-R BT.1364 and SMPTE 291M describe the ancillary data formats.

The ancillary data formats are the same as for digital component video, discussed earlier in this chapter. However, instead of a 3-word preamble, a one-word ancillary data flag is used, with a 10-bit value of $3FC_H$. There may be multiple ancillary data flags following the TRS-ID, with each flag identifying the beginning of another ancillary packet.

Ancillary data may be present within the following word number boundaries (see Figures 6.25 through 6.30).

NTSC	*PAL*	
795–849	972–1035	horizontal sync period
795–815	972–994	equalizing pulse periods
340–360	404–426	
795–260	972–302	vertical sync periods
340–715	404–869	

Video Level	(M) NTSC	(B, D, G, H, I) PAL
peak chroma	972	1040 (limited to 1023)
white	800	844
peak burst	352	380
black	280	256
blank	240	256
peak burst	128	128
peak chroma	104	128
sync	16	4

Table 6.9. 10-Bit Video Levels for Digital Composite Video Signals.

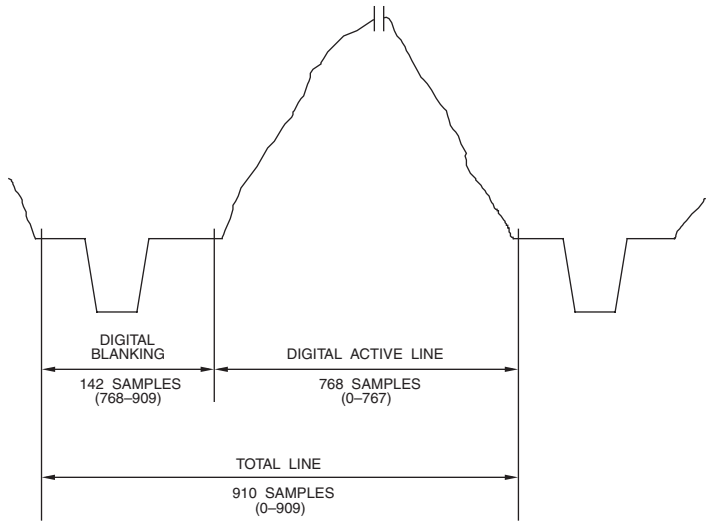


Figure 6.22. Digital Composite (M) NTSC Analog and Digital Timing Relationship.

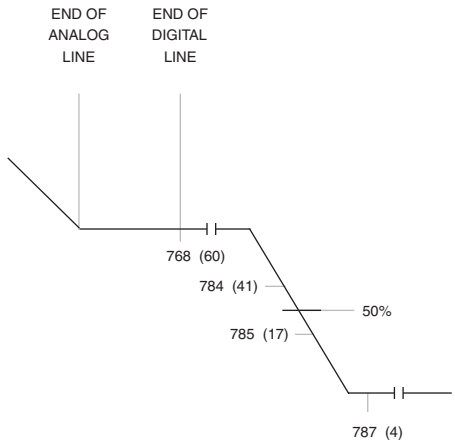


Figure 6.23. Digital Composite (M) NTSC Sync Timing. The horizontal counts are shown with the corresponding 8-bit sample values in parentheses.

Sample	8-bit Hex Value		10-bit Hex Value	
	Fields 1, 3	Fields 2, 4	Fields 1, 3	Fields 2, 4
768–782	3C	3C	0F0	0F0
783	3A	3A	0E9	0E9
784	29	29	0A4	0A4
785	11	11	044	044
786	04	04	011	011
787–849	04	04	010	010
850	06	06	017	017
851	17	17	05C	05C
852	2F	2F	0BC	0BC
853	3C	3C	0EF	0EF
854–856	3C	3C	0F0	0F0
857	3C	3C	0F0	0F0
858	3D	3B	0F4	0EC
859	37	41	0DC	104
860	36	42	0D6	10A
861	4B	2D	12C	0B4
862	49	2F	123	0BD
863	25	53	096	14A
864	2D	4B	0B3	12D
865	53	25	14E	092
866	4B	2D	12D	0B3
867	25	53	092	14E
868	2D	4B	0B3	12D
869	53	25	14E	092
870	4B	2D	12D	0B3
871	25	53	092	14E
872	2D	4B	0B3	12D
873	53	25	14E	092

Table 6.10a. Digital Values During the Horizontal Blanking Intervals for Digital Composite (M) NTSC Video Signals.

Sample	8-bit Hex Value		10-bit Hex Value	
	Fields 1, 3	Fields 2, 4	Fields 1, 3	Fields 2, 4
874	4B	2D	12D	0B3
875	25	53	092	14E
876	2D	4B	0B3	12D
877	53	25	14E	092
878	4B	2D	12D	0B3
879	25	53	092	14E
880	2D	4B	0B3	12D
881	53	25	14E	092
882	4B	2D	12D	0B3
883	25	53	092	14E
884	2D	4B	0B3	12D
885	53	25	14E	092
886	4B	2D	12D	0B3
887	25	53	092	14E
888	2D	4B	0B3	12D
889	53	25	14E	092
890	4B	2D	12D	0B3
891	25	53	092	14E
892	2D	4B	0B3	12D
893	53	25	14E	092
894	4A	2E	129	0B7
895	2A	4E	0A6	13A
896	33	45	0CD	113
897	44	34	112	0CE
898	3F	39	0FA	0E6
899	3B	3D	0EC	0F4
900–909	3C	3C	0F0	0F0

Table 6.10b. Digital Values During the Horizontal Blanking Intervals for Digital Composite (M) NTSC Video Signals.

Fields 1, 3			Fields 2, 4		
Sample	**8-bit Hex Value**	**10-bit Hex Value**	**Sample**	**8-bit Hex Value**	**10-bit Hex Value**
768–782	3C	0F0	**313–327**	3C	0F0
783	3A	0E9	**328**	3A	0E9
784	29	0A4	**329**	29	0A4
785	11	044	**330**	11	044
786	04	011	**331**	04	011
787–815	04	010	**332–360**	04	010
816	06	017	**361**	06	017
817	17	05C	**362**	17	05C
818	2F	0BC	**363**	2F	0BC
819	3C	0EF	**364**	3C	0EF
820–327	3C	0F0	**365–782**	3C	0F0
328	3A	0E9	**783**	3A	0E9
329	29	0A4	**784**	29	0A4
330	11	044	**785**	11	044
331	04	011	**786**	04	011
332–360	04	010	**787–815**	04	010
361	06	017	**816**	06	017
362	17	05C	**817**	17	05C
363	2F	0BC	**818**	2F	0BC
364	3C	0EF	**819**	3C	0EF
365–782	3C	0F0	**820–327**	3C	0F0

Table 6.11. Equalizing Pulse Values During the Vertical Blanking Intervals for Digital Composite (M) NTSC Video Signals.

Fields 1, 3			Fields 2, 4		
Sample	**8-bit Hex Value**	**10-bit Hex Value**	**Sample**	**8-bit Hex Value**	**10-bit Hex Value**
782	3C	0F0	**327**	3C	0F0
783	3A	0E9	**328**	3A	0E9
784	29	0A4	**329**	29	0A4
785	11	044	**330**	11	044
786	04	011	**331**	04	011
787–260	04	010	**332–715**	04	010
261	06	017	**716**	06	017
262	17	05C	**717**	17	05C
263	2F	0BC	**718**	2F	0BC
264	3C	0EF	**719**	3C	0EF
265–327	3C	0F0	**720–782**	3C	0F0
328	3A	0E9	**783**	3A	0E9
329	29	0A4	**784**	29	0A4
330	11	044	**785**	11	044
331	04	011	**786**	04	011
332–715	04	010	**787–260**	04	010
716	06	017	**261**	06	017
717	17	05C	**262**	17	05C
718	2F	0BC	**263**	2F	0BC
719	3C	0EF	**264**	3C	0EF
720–782	3C	0F0	**265–327**	3C	0F0

Table 6.12. Serration Pulse Values During the Vertical Blanking Intervals for Digital Composite (M) NTSC Video Signals.

User data may not use the 10-bit values of 0x000–0x003 and 0x3FC–0x3FF, or the 8-bit values of 0x00 and 0xFF, since they are used for timing information.

Parallel Interface

The SMPTE 244M 25-pin parallel interface is based on that used for 27 MHz 4:2:2 digital component video (Table 6.5), except for the timing differences. This interface is used to transfer SDTV resolution digital composite data. 8-bit or 10-bit data and a 4× F_{SC} clock are transferred.

Signal levels are compatible with ECL-compatible balanced drivers and receivers. The generator must have a balanced output with a maximum source impedance of 110 Ω; the signal must be 0.8–2.0V peak-to-peak measured across a 110-Ω load. At the receiver, the transmission line must be terminated by 110 ±10 Ω.

The clock signal is a 4× F_{SC} square wave, with a clock pulse width of 35 ±5 ns for (M) NTSC or 28 ±5 ns for (B, D, G, H, I) PAL. The positive transition of the clock signal occurs midway between data transitions with a tolerance of ±5 ns (as shown in Figure 6.31).

To permit reliable operation at interconnect lengths of 50–200 meters, the receiver must use frequency equalization, with typical characteristics shown in Figure 6.3. This example enables operation with a range of cable lengths down to zero.

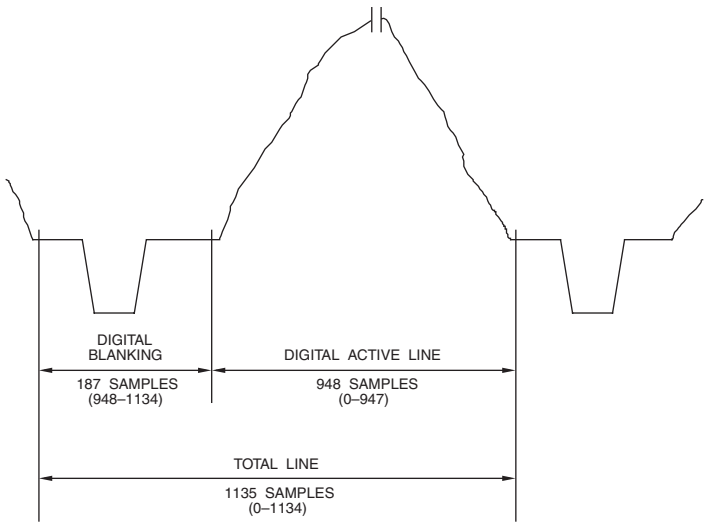


Figure 6.24. Digital Composite (B, D, G, H, I) PAL Analog and Digital Timing Relationship.

Serial Interface

The parallel format can be converted to a SMPTE 259M serial format (Figure 6.32), allowing data to be transmitted using a 75-Ω coaxial cable (or optical fiber). This interface converts the 14.32 or 17.73 MHz parallel stream into a 143 or 177 Mbps serial stream. The 10× PLL generates the 143 or 177 MHz clock from the 14.32 or 17.73 MHz clock signal.

For cable interconnect, the generator has an unbalanced output with a source impedance of 75 Ω; the signal must be 0.8V ±10% peak-to-peak measured across a 75-Ω load. The receiver has an input impedance of 75 Ω.

The 10 bits of data are serialized (LSB first) and processed using a scrambled and polarity-free NRZI algorithm:

$$G(x) = (x^9 + x^4 + 1)(x + 1)$$

This algorithm is the same as used for digital component video discussed earlier. In an 8-bit environment, 8-bit data is appended with two least significant "0" bits before serialization.

The input signal to the scrambler (Figure 6.20) uses positive logic (the highest voltage represents a logical one; lowest voltage represents a logical zero). The formatted serial data is output at the 40× F_{SC} rate.

At the receiver, phase-lock synchronization is done by detecting the TRS-ID sequences. The PLL is continuously adjusted slightly each scan line to ensure that these patterns are detected and to avoid bit slippage. The recovered 10× clock is divided by ten to generate the 4× F_{SC} sample clock. The serial data is low- and high-frequency equalized, inverse scrambling performed (Figure 6.21), and deserialized.

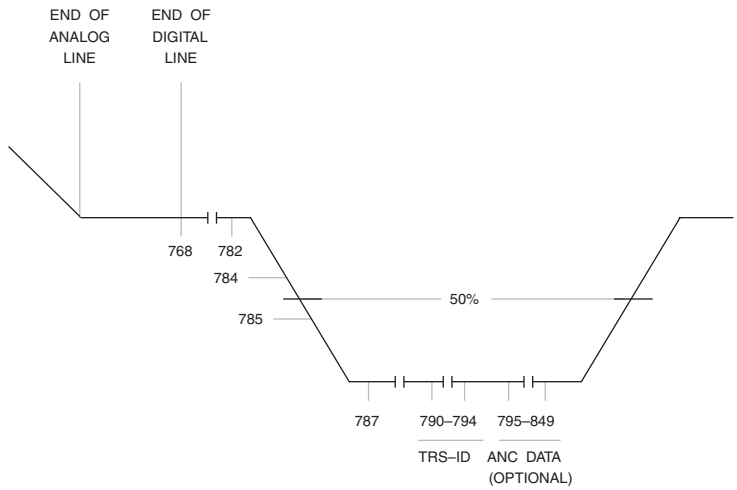


Figure 6.25. (M) NTSC TRS-ID and Ancillary Data Locations During Horizontal Sync Intervals.

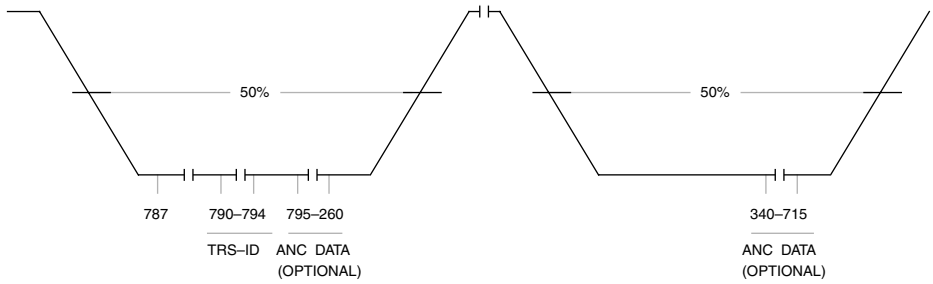


Figure 6.26. (M) NTSC TRS-ID and Ancillary Data Locations During Vertical Sync Intervals.

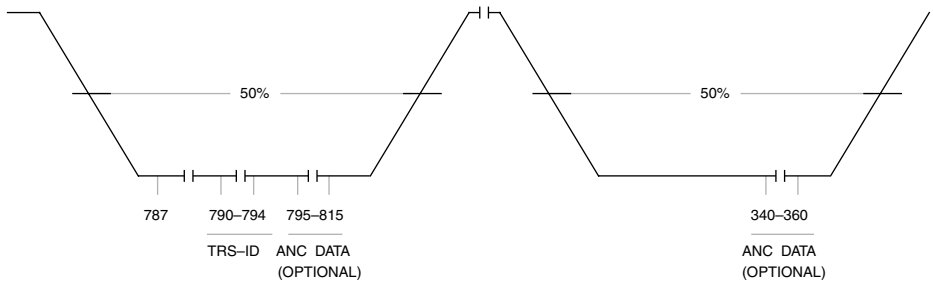


Figure 6.27. (M) NTSC TRS-ID and Ancillary Data Locations During Equalizing Pulse Intervals.

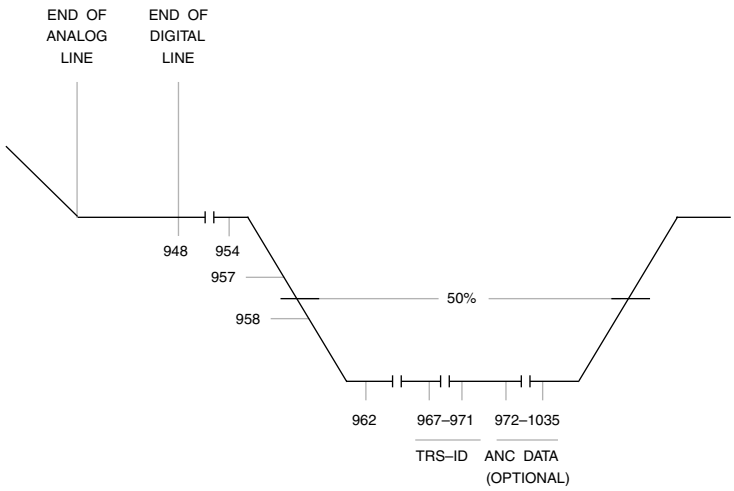


Figure 6.28. (B, D, G, H, I) PAL TRS-ID and Ancillary Data Locations During Horizontal Sync Intervals.

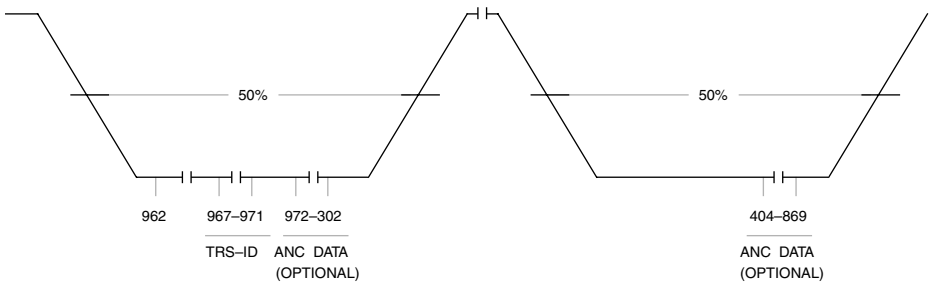


Figure 6.29. (B, D, G, H, I) PAL TRS-ID and Ancillary Data Locations During Vertical Sync Intervals.

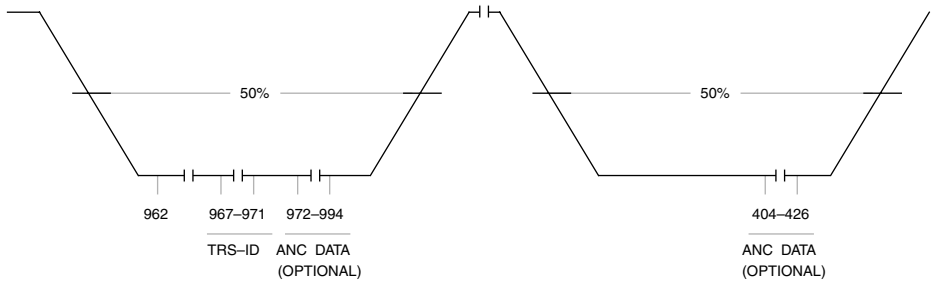


Figure 6.30. (B, D, G, H, I) PAL TRS-ID and Ancillary Data Locations During Equalizing Pulse Intervals.

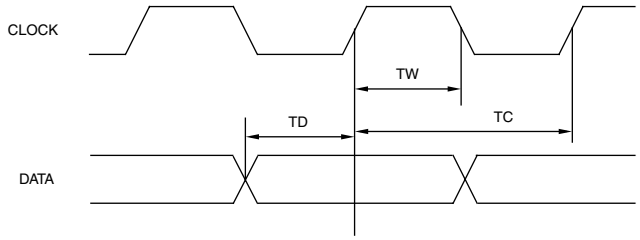
TRS-ID

When using the serial interface, a special five-word sequence, known as the TRS-ID, must be inserted into the digital video stream during the horizontal sync time. The TRS-ID is present only following sync leading edges which identify a horizontal transition, and occupies horizontal counts 790–794, inclusive (NTSC) or 967–971, inclusive (PAL). Table 6.13 shows the TRS-ID format; Figures 6.25 through 6.30 show the TRS-ID locations for digital composite (M) NTSC and (B, D, G, H, I) PAL video signals.

The line number ID word at horizontal count 794 (NTSC) or 971 (PAL) is defined as shown in Table 6.14.

PAL requires the reset of the TRS-ID position relative to horizontal sync once per field on only one of lines 625–4 and 313–317 due to the 25 Hz offset. All lines have 1135 samples except the two lines used for reset, which have 1137 samples. The two additional samples are numbered 1135 and 1136, and occur just prior to the first active picture sample (sample 0).

Due to the 25 Hz offset, the samples occur slightly earlier each line. Initial determination of the TRS-ID position should be done on line 1, Field 1, or a nearby line. The TRS-ID location always starts at sample 967, but the distance from the leading edge of sync varies due to the 25 Hz offset.



TW = 35 ± 5 NS (M) NTSC; 28 ± 5 NS (B, D, G, H, I) PAL
TC = 69.84 NS (M) NTSC; 56.39 NS (B, D, G, H, I) PAL
TD = 35 ± 5 NS (M) NTSC; 28 ± 5 NS (B, D, G, H, I) PAL

Figure 6.31. Digital Composite Video Parallel Interface Waveforms.

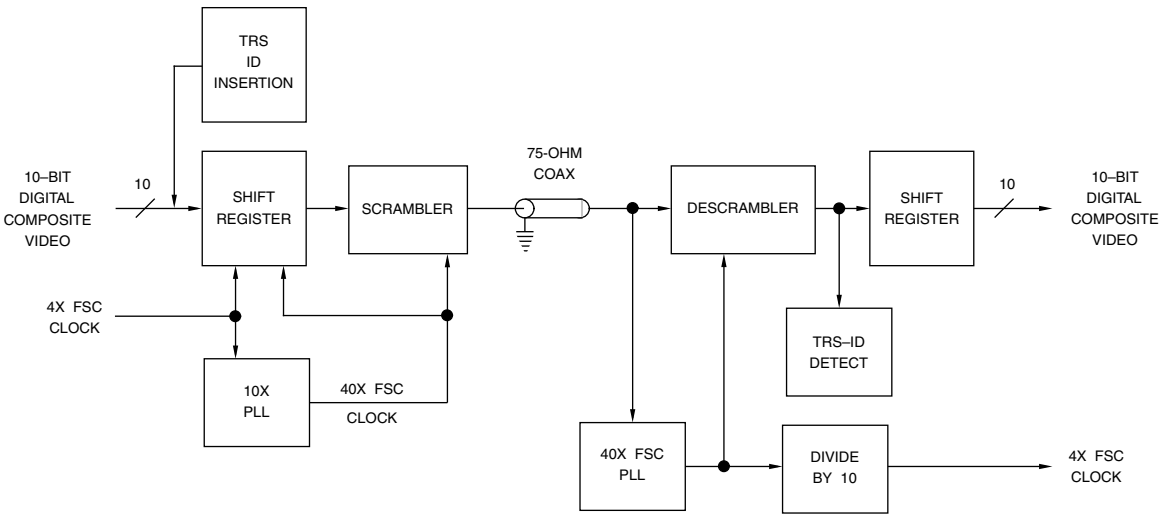


Figure 6.32. Serial Interface Block Diagram.

	D9 (MSB)	D8	D7	D6	D5	D4	D3	D2	D1	D0
TRS word 0	1	1	1	1	1	1	1	1	1	1
TRS word 1	0	0	0	0	0	0	0	0	0	0
TRS word 2	0	0	0	0	0	0	0	0	0	0
TRS word 3	0	0	0	0	0	0	0	0	0	0
line number ID	$\overline{D8}$	EP	line number ID							

Note:
EP = even parity for D0–D7.

Table 6.13. TRS-ID Format.

D2	D1	D0	(M) NTSC	(B, D, G, H, I) PAL
0	0	0	line 1–263 field 1	line 1–313 field 1
0	0	1	line 264–525 field 2	line 314–625 field 2
0	1	0	line 1–263 field 3	line 1–313 field 3
0	1	1	line 264–525 field 4	line 314–625 field 4
1	0	0	not used	line 1–313 field 5
1	0	1	not used	line 314–625 field 6
1	1	0	not used	line 1–313 field 7
1	1	1	not used	line 314–625 field 8

D7–D3	(M) NTSC	(B, D, G, H, I) PAL
$1 \le x \le 30$	line number 1–30 [264–293]	line number 1–30 [314–343]
x = 31	line number ≥ 31 [294]	line number ≥ 31 [344]
x = 0	not used	not used

Table 6.14. Line Number ID Word at Horizontal Count 794 (NTSC) or 971 (PAL).

Pro-Video Transport Interfaces

Serial Data Transport Interface (SDTI)

SMPTE 305M and ITU-R BT.1381 define a Serial Data Transport Interface (SDTI) that enables transferring data between equipment. The physical layer uses the 270 or 360 Mbps BT.656, BT.1302, and SMPTE 259M digital component video serial interface. Figure 6.33 illustrates the signal format.

A 53-word header is inserted immediately after the EAV sequence, specifying the source, destination, and data format. Table 6.15 illustrates the header contents.

The payload data is defined within BT.1381 and by other application-specific standards such as SMPTE 326M. It may consist of MPEG-2 program or transport streams, DV streams, etc., and uses either 8-bit words plus even parity and $\overline{D8}$, or 9-bit words plus $\overline{D8}$.

Line Number

The line number specifies a value of 1–525 (480i systems) or 1–625 (576i systems). L0 is the least significant bit.

Line Number CRC

The line number CRC applies to the data ID through the line number, for the entire 10 bits. C0 is the least significant bit. It is an 18-bit value, with an initial value set to all ones:

$$CRC = x^{18} + x^5 + x^4 + x^1$$

Code and AAI

The 4-bit code value (CD3–CD0) specifies the length of the payload (the user data contained between the SAV and EAV sequences):

0000	4:2:2 YCbCr video data
0001	1440 word payload (uses 270 Mbps interface)
0010	1920 word payload (uses 360 Mbps interface)
1000	143 Mbps digital composite video

The 4-bit authorized address identifier (AAI) value, AAI3–AAI0, specifies the format of the destination and source addresses:

0000	unspecified format
0001	IPv6 address

Destination and Source Addresses

These specify the address of the source and destination devices. A universal address is indicated when all address bits are zero and AAI3–AAI0 = 0000.

Block Type

The block type value specifies the segmentation of the payload. BL7–BL6 indicate the payload block structure:

00	fixed block size without ECC
01	fixed block size with ECC
10	unassigned
11	variable block size

BL5–BL0 indicate the segmentation for fixed block sizes. Variable block sizes are indicated by BL7–BL0 having a value of 11000001. The ECC format is application-dependent.

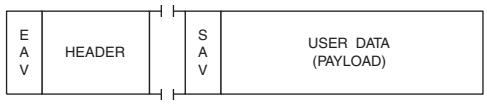


Figure 6.33. SDTI Signal Format.

Payload CRC Flag

The CRCF bit indicates whether or not the payload CRC is present at the end of the payload:

0 no CRC
1 CRC present

Header CRC

The header CRC applies to the code and AAI word through the last reserved data word, for the entire 10 bits. C0 is the least significant bit. It is an 18-bit value, with an initial value set to all ones:

$$CRC = x^{18} + x^5 + x^4 + x^1$$

High Data-Rate Serial Data Transport Interface (HD-SDTI)

SMPTE 348M and ITU-R BT.1577 define a High Data-Rate Serial Data Transport Interface (HD-SDTI) that enables transferring data between equipment. The physical layer uses the 1.485 (or 1.485/1.001) Gbps SMPTE 292M digital component video serial interface.

Figure 6.34 illustrates the signal format. Two data channels are multiplexed onto the single HD-SDTI stream such that one 74.25 (or 74.25/1.001) MHz data stream occupies the Y data space and the other 74.25 (or 74.25/1.001) MHz data stream occupies the CbCr data space.

A 49-word header is inserted immediately after the line number CRC data, specifying the source, destination, and data format. Table 6.16 illustrates the header contents.

The payload data is defined by other application-specific standards. It may consist of MPEG-2 program or transport streams, DV streams, etc., and uses either 8-bit words plus even parity and $\overline{D8}$, or 9-bit words plus $\overline{D8}$.

Code and AAI

The 4-bit code value (CD3–CD0) specifies the length of the payload (the user data contained between the SAV and EAV sequences):

0000 4:2:2 YCbCr video data
0001 1440 word payload
0010 1920 word payload
0011 1280 word payload
1000 143 Mbps digital composite video
1001 2304 word payload (extended mode)
1010 2400 word payload (extended mode)
1011 1440 word payload (extended mode)
1100 1728 word payload (extended mode)
1101 2880 word payload (extended mode)
1110 3456 word payload (extended mode)
1111 3600 word payload (extended mode)

	10-bit Data									
	D9 (MSB)	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ancillary data flag (ADF)	0	0	0	0	0	0	0	0	0	0
	1	1	1	1	1	1	1	1	1	1
	1	1	1	1	1	1	1	1	1	1
data ID (DID)	$\overline{D8}$	EP	0	1	0	0	0	0	0	0
SDID	$\overline{D8}$	EP	0	0	0	0	0	0	0	1
data count (DC)	$\overline{D8}$	EP	0	0	1	0	1	1	1	0
line number	$\overline{D8}$	EP	L7	L6	L5	L4	L3	L2	L1	L0
	$\overline{D8}$	EP	0	0	0	0	0	0	L9	L8
line number CRC	$\overline{D8}$	C8	C7	C6	C5	C4	C3	C2	C1	C0
	$\overline{D8}$	C17	C16	C15	C14	C13	C12	C11	C10	C9
code and AAI	$\overline{D8}$	EP	AAI3	AAI2	AAI1	AAI0	CD3	CD2	CD1	CD0
destination address	$\overline{D8}$	EP	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
	$\overline{D8}$	EP	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8
	:									
	$\overline{D8}$	EP	DA127	DA126	DA125	DA124	DA123	DA122	DA121	DA120
source address	$\overline{D8}$	EP	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0
	$\overline{D8}$	EP	SA15	SA14	SA13	SA12	SA11	SA10	SA9	SA8
	:									
	$\overline{D8}$	EP	SA127	SA126	SA125	SA124	SA123	SA122	SA121	SA120

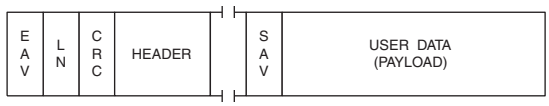
Note:
EP = even parity for D0–D7.

Table 6.15a. SDTI Header Structure.

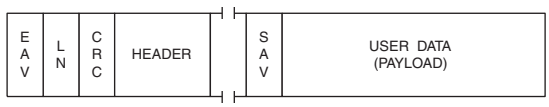
	10-bit Data									
	D9 (MSB)	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
block type	$\overline{D8}$	EP	BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0
payload CRC flag	$\overline{D8}$	EP	0	0	0	0	0	0	0	CRCF
reserved	$\overline{D8}$	EP	0	0	0	0	0	0	0	0
reserved	$\overline{D8}$	EP	0	0	0	0	0	0	0	0
reserved	$\overline{D8}$	EP	0	0	0	0	0	0	0	0
reserved	$\overline{D8}$	EP	0	0	0	0	0	0	0	0
reserved	$\overline{D8}$	EP	0	0	0	0	0	0	0	0
header CRC	$\overline{D8}$	C8	C7	C6	C5	C4	C3	C2	C1	C0
	$\overline{D8}$	C17	C16	C15	C14	C13	C12	C11	C10	C9
checksum	$\overline{D8}$	Sum of D0–D8 of data ID through last header CRC word. Preset to all zeros; carry is ignored.								

Note:
EP = even parity for D0–D7.

Table 6.15b. SDTI Header Structure (continued).



C CHANNEL



Y CHANNEL

Figure 6.34. HD-SDTI Signal Format. LN = line number (two 10-bit words), CRC = line number CRC (two 10-bit words).

	10-bit Data									
	D9 (MSB)	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ancillary data flag (ADF)	0	0	0	0	0	0	0	0	0	0
	1	1	1	1	1	1	1	1	1	1
	1	1	1	1	1	1	1	1	1	1
data ID (DID)	$\overline{D8}$	EP	0	1	0	0	0	0	0	0
SDID	$\overline{D8}$	EP	0	0	0	0	0	0	1	0
data count (DC)	$\overline{D8}$	EP	0	0	1	0	1	0	1	0
code and AAI	$\overline{D8}$	EP	AAI3	AAI2	AAI1	AAI0	CD3	CD2	CD1	CD0
destination address	$\overline{D8}$	EP	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
	$\overline{D8}$	EP	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8
	:									
	$\overline{D8}$	EP	DA127	DA126	DA125	DA124	DA123	DA122	DA121	DA120
source address	$\overline{D8}$	EP	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0
	$\overline{D8}$	EP	SA15	SA14	SA13	SA12	SA11	SA10	SA9	SA8
	:									
	$\overline{D8}$	EP	SA127	SA126	SA125	SA124	SA123	SA122	SA121	SA120
block type	$\overline{D8}$	EP	BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0
payload CRC flag	$\overline{D8}$	EP	0	0	0	0	0	0	0	0
reserved	$\overline{D8}$	EP	0	0	0	0	0	0	0	0

Note:
EP = even parity for D0–D7.

Table 6.16a. HD-SDTI Header Structure.

	10-bit Data									
	D9 (MSB)	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
reserved	$\overline{D8}$	EP	0	0	0	0	0	0	0	0
reserved	$\overline{D8}$	EP	0	0	0	0	0	0	0	0
reserved	$\overline{D8}$	EP	0	0	0	0	0	0	0	0
reserved	$\overline{D8}$	EP	0	0	0	0	0	0	0	0
header CRC	$\overline{D8}$	C8	C7	C6	C5	C4	C3	C2	C1	C0
	$\overline{D8}$	C17	C16	C15	C14	C13	C12	C11	C10	C9
checksum	$\overline{D8}$	Sum of D0–D8 of data ID through last header CRC word. Preset to all zeros; carry is ignored.								

Note:
EP = even parity for D0–D7.

Table 6.16b. HD-SDTI Header Structure (continued).

The extended mode advances the timing of the SAV sequence, shortening the blanking interval, so that the payload data rate remains a constant 129.6 (or 129.6/1.001) MBps.

The 4-bit authorized address identifier (AAI) format is the same as for SDTI.

Destination and Source Addresses

The source and destination address formats are the same as for SDTI.

Block Type

The block type format is the same as for SDTI.

Header CRC

The header CRC applies to the DID through the last reserved data word, for the entire 10 bits. C0 is the least significant bit. It is an 18-bit value, with an initial value set to all ones:

$$CRC = x^{18} + x^5 + x^4 + x^1$$

IC Component Interfaces

Many solutions for transferring digital video between chips are derived from the pro-video interconnect standards. Chips for the pro-video market typically support 10 or 12 bits of data per video component, while chips for the consumer market typically use 8 bits of data per video component. BT.601 and BT.656 are the most popular interfaces.

YCbCr Values: 8-bit Data

Y has a nominal range of 0x10–0xEB. Values less than 10_H or greater than $0xEB_H$ may be present due to processing. Cb and Cr have a nominal range of 0x10–0xF0. Values less than 0x10 or greater than 0xF0 may be present due to processing. YCbCr data may not use the values of 00_H and FF_H since those values may be used for timing information.

During blanking, Y data should have a value of 0x10 and CbCr data should have a value of 0x80, unless other information is present.

YCbCr Values: 10-bit Data

For higher accuracy, pro-video solutions typically use 10-bit YCbCr data. Y has a nominal range of 0x040–0x3AC. Values less than 0x040 or greater than 0x3AC may be present due to processing. Cb and Cr have a nominal range of 040_H–$3C0_H$. Values less than 0x040 or greater than 0x3C0 may be present due to processing. The values 0x000–0x003 and 0x3FC–0x3FF may not be used to avoid timing contention with 8-bit systems.

During blanking, Y data should have a value of 0x040 and CbCr data should have a value of 0x200, unless other information is present.

RGB Values: 8-bit Data

Consumer solutions typically use 8-bit R′G′B′ data, with a range of 0x10–0xEB (note that PCs typically use a range of 0x00–0xFF). Values less than 0x10 or greater than 0xEB may be present due to processing.

During blanking, R′G′B′ data should have a value of 0x10, unless other information is present.

RGB Values: 10-bit Data

For higher accuracy, pro-video solutions typically use 10-bit R′G′B′ data, with a nominal range of 0x040–0x3AC. Values less than 0x040 or greater than $0x3AC_H$ may be present due to processing. The values 0x000–0x003 and 0x3FC–0x3FF may not be used to avoid timing contention with 8-bit systems.

During blanking, R′G′B′ data should have a value of 0x040, unless other data is present.

BT.601 Video Interface

The BT.601 video interface has been used for years, with the control signal names and timing reflecting the video standard. Supported active resolutions and sample clock rates are dependent on the video standard and aspect ratio.

Devices usually support multiple data formats to simplify using them in a wide variety of applications.

Video Data Formats

The 24-bit 4:4:4 YCbCr data format is shown in Figure 6.35. Y, Cb, and Cr are each 8 bits, and all are sampled at the same rate, resulting in 24 bits of data per sample clock. Pro-video solutions typically use a 30-bit interface, with the Y, Cb, and Cr streams each being

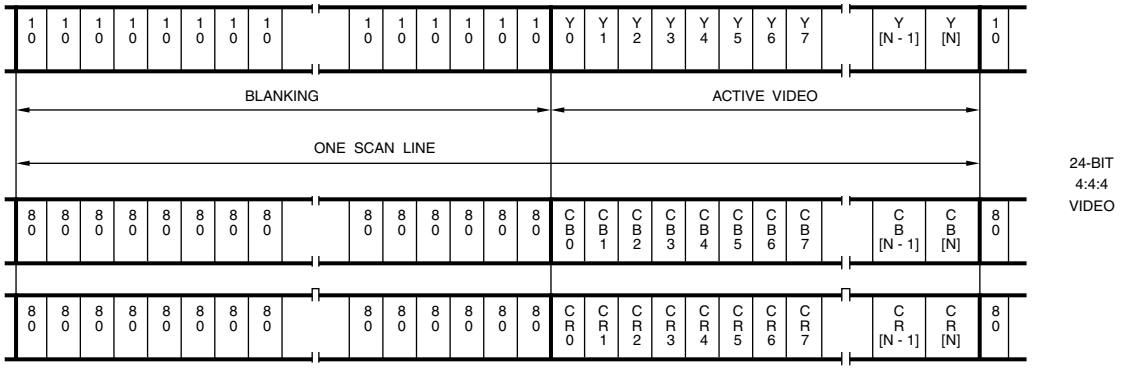


Figure 6.35. 24-Bit 4:4:4 YCbCr Data Format.

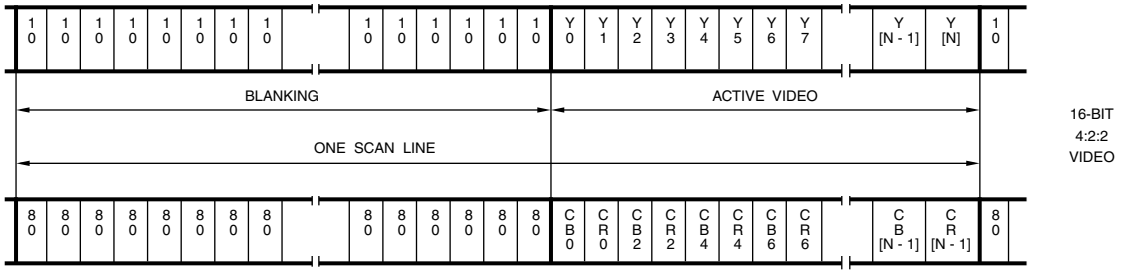


Figure 6.36. 16-Bit 4:2:2 YCbCr Data Format.

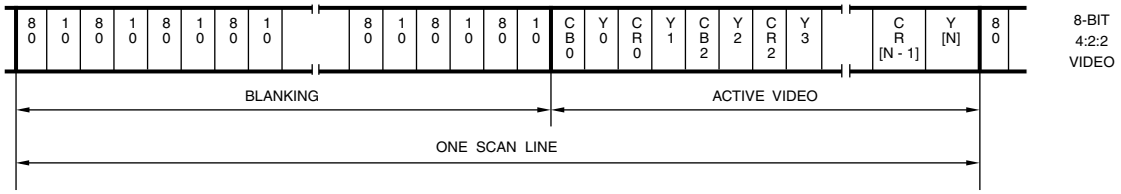


Figure 6.37. 8-Bit 4:2:2 YCbCr Data Format.

10 bits. Y0, Cb0, and Cr0 are the least significant bits.

The 16-bit 4:2:2 YCbCr data format is shown in Figure 6.36. Cb and Cr are sampled at one-half the Y sample rate, then multiplexed together. The CbCr stream of active data words always begins with a Cb sample. Pro-video solutions typically use a 20-bit interface, with the Y and CbCr streams each being 10 bits.

The 8-bit 4:2:2 YCbCr data format is shown in Figure 6.37. The Y and CbCr streams from the 16-bit 4:2:2 YCbCr format are simply multiplexed at 2× the sample clock rate. The YCbCr stream of active data words always begins with a Cb sample. Pro-video solutions typically use a 10-bit interface.

Tables 6.17 and 6.18 illustrate the 15-bit RGB, 16-bit RGB, and 24-bit RGB formats. For the 15-bit RGB format, the unused bit is sometimes used for keying (alpha) information. R0, G0, and B0 are the least significant bits.

Control Signals

In addition to the video data, there are four control signals:

HSYNC# (or HREF)	horizontal sync
VSYNC# (or VREF)	vertical sync
BLANK# (or ACTIVE)	blanking
CLK	1× or 2× sample clock

For the 8-bit and 10-bit 4:2:2 YCbCr data formats, CLK is a 2× sample clock. For the other data formats, CLK is a 1× sample clock. For sources, the control signals and video data are output following the rising edge of CLK. For receivers, the control signals and video data are sampled on the rising edge of CLK.

While BLANK# is negated, active R′G′B′ or YCbCr video data is present.

HSYNC# is asserted during the horizontal sync time each scan line, with the leading edge indicating the start of a new line. The amount of time that HSYNC# is asserted is usually the same as that specified by the video standard.

VSYNC# is asserted during the vertical sync time each field or frame, with the leading edge indicating the start of a new field or frame. The number of scan lines that VSYNC# is asserted is usually same as that specified by the video standard.

For interlaced video, if the leading edges of VSYNC# and HSYNC# are coincident, the field is Field 1. If the leading edge of VSYNC# occurs mid-line, the field is Field 2. For noninterlaced video, the leading edge of VSYNC# indicates the start of a new frame. Figure 6.38 illustrates the typical HSYNC# and VSYNC# relationships.

Some products use different signal names (such as HREF, VREF, and ACTIVE), different polarity, and slightly different signal timing. Some products can also transfer data and control information using both edges of the clock to reduce pin count or to be able to handle HDTV data rates without increasing pin count.

Receiver Considerations

Assumptions should not be made about the number of samples per line or horizontal blanking interval. Otherwise, the implementation may not work with all sources.

To ensure compatibility between various sources, horizontal counters should be reset by the leading edge of HSYNC#, not by the trailing edge of BLANK#.

To handle real-world sources, a receiver should use a window for detecting whether Field 1 or Field 2 is present. For example, if the leading edge of VSYNC# occurs within ±64 1× clock cycles of the leading edge of HSYNC#, the field is Field 1. Otherwise, the field is Field 2.

Some video sources indicate sync timing by having Y data be an 8-bit value less than 0x10. However, most video ICs do not do this.

24-bit RGB			16-bit RGB (5,6,5)	15-bit RGB (5,5,5)	24-bit 4:4:4 YCbCr			16-bit 4:2:2 YCbCr*	8-bit 4:2:2 YCbCr
Single Clock Edge	Double Clock Edge				Single Clock Edge	Double Clock Edge			
R7					Cr7				
R6					Cr6				
R5					Cr5				
R4					Cr4				
R3					Cr3				
R2					Cr2				
R1					Cr1				
R0					Cr0				
G7			R4	–	Y7			Y7	Cb7, Y7, Cr7
G6			R3	R4	Y6			Y6	Cb6, Y6, Cr6
G5			R2	R3	Y5			Y5	Cb5, Y5, Cr5
G4			R1	R2	Y4			Y4	Cb4, Y4, Cr4
G3	G3	R7	R0	R1	Y3	Y3	Cr7	Y3	Cb3, Y3, Cr3
G2	G2	R6	G5	R0	Y2	Y2	Cr6	Y2	Cb2, Y2, Cr2
G1	G1	R5	G4	G4	Y1	Y1	Cr5	Y1	Cb1, Y1, Cr1
G0	G0	R4	G3	G3	Y0	Y0	Cr4	Y0	Cb0, Y0, Cr0
B7	B7	R3	G2	G2	Cb7	Cb7	Cr3	Cb7, Cr7	
B6	B6	R2	G1	G1	Cb6	Cb6	Cr2	Cb6, Cr6	
B5	B5	R1	G0	G0	Cb5	Cb5	Cr1	Cb5, Cr5	
B4	B4	R0	B4	B4	Cb4	Cb4	Cr0	Cb4, Cr4	
B3	B3	G7	B3	B3	Cb3	Cb3	Y7	Cb3, Cr3	
B2	B2	G6	B2	B2	Cb2	Cb2	Y6	Cb2, Cr2	
B1	B1	G5	B1	B1	Cb1	Cb1	Y5	Cb1, Cr1	
B0	B0	G4	B0	B0	Cb0	Cb0	Y4	Cb0, Cr0	

Table 6.17. Transferring YCbCr and RGB Data over a 12-bit, 16-bit, or 24-bit Interface. *Many designs alternately use the red channel to transfer the multiplexed CbCr data.

24-bit RGB	16-bit RGB (5,6,5)	15-bit RGB (5,5,5)	24-bit 4:4:4 YCbCr	16-bit 4:2:2 YCbCr	8-bit 4:2:2 YCbCr
	R4	–		Y7	
	R3	R4		Y6	
	R2	R3		Y5	
	R1	R2		Y4	
	R0	R1		Y3	
	G5	R0		Y2	
	G4	G4		Y1	
	G3	G3		Y0	
R7	G2	G2	Cr7	Cb7, Cr7	
R6	G1	G1	Cr6	Cb6, Cr6	
R5	G0	G0	Cr5	Cb5, Cr5	
R4	B4	B4	Cr4	Cb4, Cr4	
R3	B3	B3	Cr3	Cb3, Cr3	
R2	B2	B2	Cr2	Cb2, Cr2	
R1	B1	B1	Cr1	Cb1, Cr1	
R0	B0	B0	Cr0	Cb0, Cr0	
G7	R4	–	Y7	Y7	Cb7, Y7, Cr7
G6	R3	R4	Y6	Y6	Cb6, Y6, Cr6
G5	R2	R3	Y5	Y5	Cb5, Y5, Cr5
G4	R1	R2	Y4	Y4	Cb4, Y4, Cr4
G3	R0	R1	Y3	Y3	Cb3, Y3, Cr3
G2	G5	R0	Y2	Y2	Cb2, Y2, Cr2
G1	G4	G4	Y1	Y1	Cb1, Y1, Cr1
G0	G3	G3	Y0	Y0	Cb0, Y0, Cr0
B7	G2	G2	Cb7	Cb7, Cr7	
B6	G1	G1	Cb6	Cb6, Cr6	
B5	G0	G0	Cb5	Cb5, Cr5	
B4	B4	B4	Cb4	Cb4, Cr4	
B3	B3	B3	Cb3	Cb3, Cr3	
B2	B2	B2	Cb2	Cb2, Cr2	
B1	B1	B1	Cb1	Cb1, Cr1	
B0	B0	B0	Cb0	Cb0, Cr0	

Table 6.18. Transferring YCbCr and RGB Data over a 32-bit Interface.

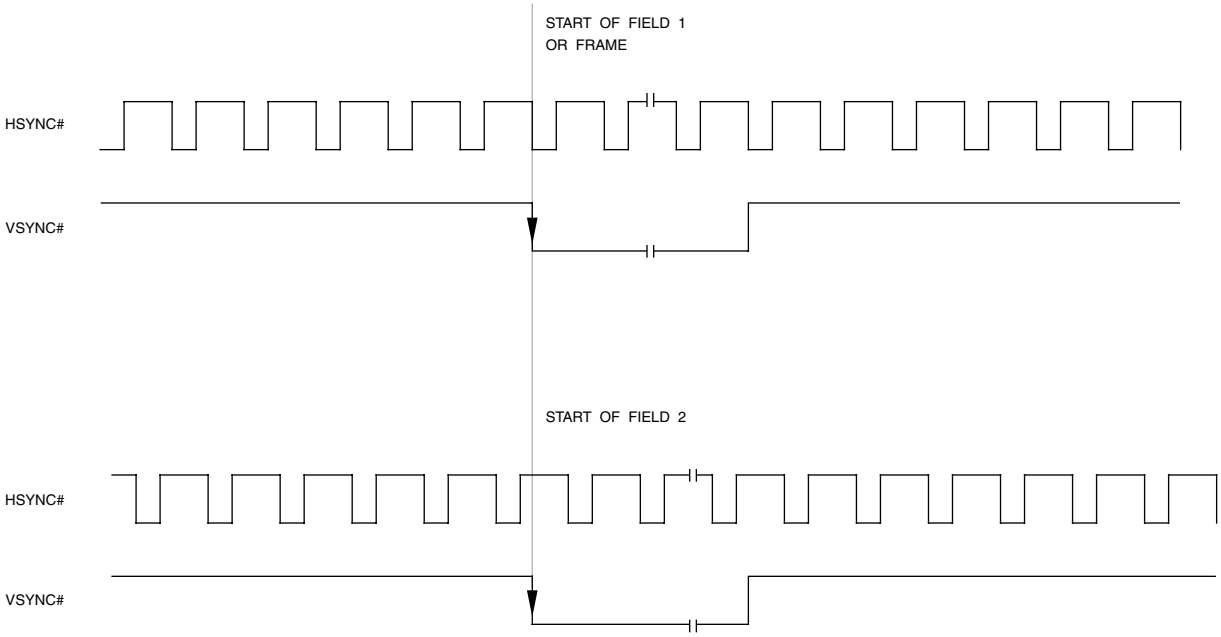


Figure 6.38. Typical HSYNC# and VSYNC# Relationships (Not to Scale). Some products use different signal names (such as HREF, VREF, and ACTIVE), different polarity and slightly different signal timing.

In addition, to allow real-world video and test signals to be passed through with minimum disruption, many ICs now allow the Y data to have a value less than 0x10 during active video. Thus, receiver designs assuming sync timing is present on the Y channel may no longer work.

Video Module Interface (VMI)

VMI (Video Module Interface) was developed in cooperation with several multimedia IC manufacturers. The goal was to standardize the video interfaces between devices such as MPEG decoders, NTSC/PAL decoders, and graphics chips.

Video Data Formats

The VMI specification specifies an 8-bit 4:2:2 YCbCr data format as shown in Figure 6.39. Many devices also support the other YCbCr and R′G′B′ formats discussed in the "BT.601 Video Interface" section.

Control Signals

In addition to the video data, there are four control signals:

HREF	horizontal blanking
VREF	vertical sync
VACTIVE	active video
PIXCLK	2× sample clock

For the 8-bit and 10-bit 4:2:2 YCbCr data formats, PIXCLK is a 2× sample clock. For the other data formats, PIXCLK is a 1× sample clock. For sources, the control signals and video data are output following the rising edge of PIXCLK. For receivers, the control signals and video data are sampled on the rising edge of PIXCLK.

While VACTIVE is asserted, active R′G′B′ or YCbCr video data is present. Although transitions in VACTIVE are allowed, it is intended to allow a hardware mechanism for cropping video data. For systems that do not support a VACTIVE signal, HREF can generally be connected to VACTIVE with minimal loss of function.

To support video sources that do not generate a line-locked clock, a DVALID# (data valid) signal may also be used. While DVALID# is asserted, valid data is present.

HREF is asserted during the active video time each scan line, including during the vertical blanking interval.

VREF is asserted for 6 scan line times, starting one-half scan line after the start of vertical sync.

For interlaced video, the trailing edge of VREF is used to sample HREF. If HREF is asserted, the field is Field 1. If HREF is negated, the field is Field 2. For noninterlaced video, the leading edge of VREF indicates the start of a new frame. Figure 6.40 illustrates the typical HREF and VREF relationships.

Receiver Considerations

Assumptions should not be made about the number of samples per line or horizontal blanking interval. Otherwise, the implementation may not work with all sources.

Video data has input setup and hold times, relative to the rising edge of PIXCLK, of 5 and 0 ns, respectively.

VACTIVE has input setup and hold times, relative to the rising edge of PIXCLK, of 5 and 0 ns, respectively.

HREF and VREF both have input setup and hold times, relative to the rising edge of PIXCLK, of 5 and 5 ns, respectively.

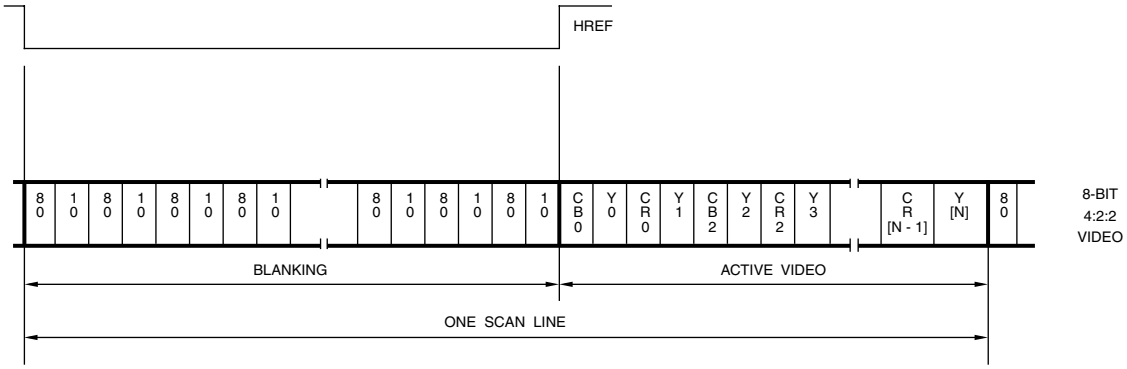


Figure 6.39. VMI 8-bit 4:2:2 YCbCr Data for One Scan Line.

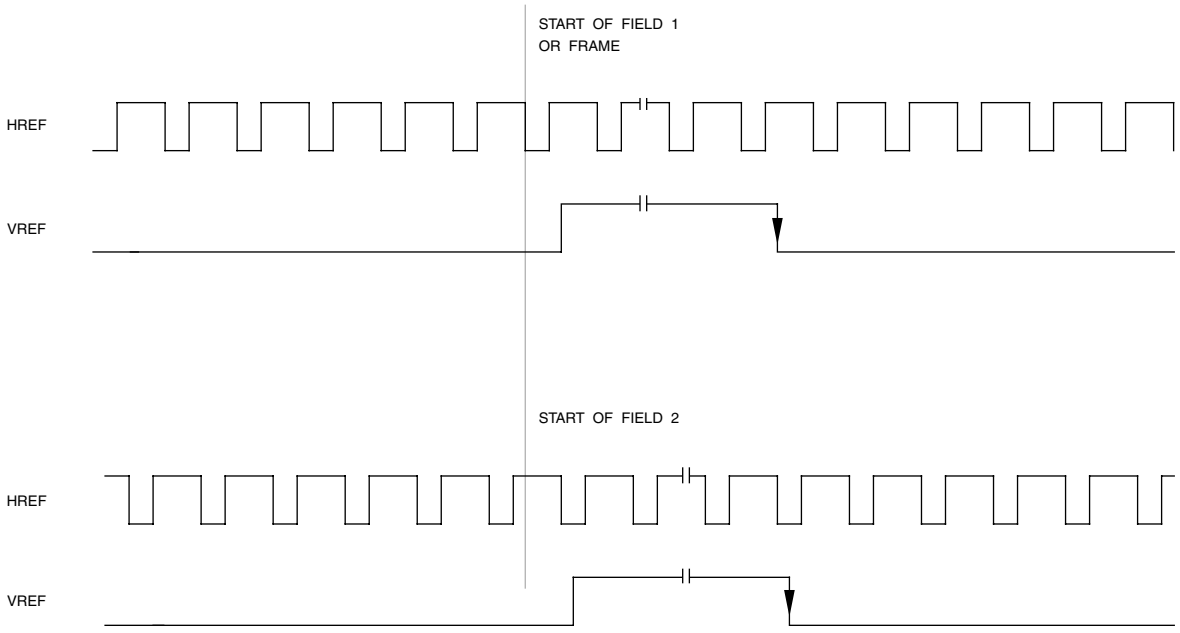


Figure 6.40. VMI Typical HREF and VREF Relationships (Not to Scale).

BT.656 Interface

The BT.656 interface for ICs is based on the pro-video BT.656-type parallel interfaces, discussed earlier in this chapter (Figures 6.1 and 6.9xxx). Using EAV and SAV sequences to indicate video timing reduces the number of pins required. The timing of the H, V, and F signals for common video formats is illustrated in Chapter 4.

Standard IC signal levels and timing are used, and any resolution can be supported.

Video Data Formats

8-bit or 10-bit 4:2:2 YCbCr data is used, as shown in Figures 6.1 and 6.6. Although sources should generate the four protection bits in the EAV and SAV sequences, receivers may choose to ignore them due to the reliability of point-to-point transfers between chips.

Control Signals

CLK is a 2× sample clock. For sources, the video data is output following the rising edge of CLK. For receivers, the video data is sampled on the rising edge of CLK.

To be able to handle HDTV data rates, some designs use a 16-bit or 20-bit YCbCr interface (essentially two BT.656 streams, one for Y data and one for CbCr data) or transfer data using both edges of the clock.

Zoomed Video Port (ZV Port)

An early standard for notebook PCs, the ZV Port was a point-to-point uni-directional bus between the PC Card host adaptor and the graphics controller. It enabled video data to be transferred real time directly from the PC Card into the graphics frame buffer.

The PC Card host adaptor had a special multimedia mode configuration. If a non-ZV PC Card was plugged into the slot, the host adaptor was not switched into the multimedia mode, and the PC Card behaved as expected. Once a ZV card was been plugged in and the host adaptor had been switched to the multimedia mode, the pin assignments changed. As shown in Table 6.19, the PC Card signals A6–A25, SPKR#, INPACK#, and IOIS16# are replaced by ZV Port video signals (Y0–Y7, CbCr0–CbCr7, HREF, VREF, and PCLK) and 4-channel audio signals (MCLK, SCLK, LRCK, and SDATA).

Video Data Formats

16-bit 4:2:2 YCbCr data was used, as shown in Figure 6.36.

Control Signals

In addition to the video data, there were four control signals:

HREF	horizontal reference
VREF	vertical sync
PCLK	1× sample clock

HREF, VREF, and PCLK had the same timing as the VMI interface discussed earlier in this chapter.

PC Card Signal	ZV Port Signal	PC Card Signal	ZV Port Signal	PC Card Signal	ZV Port Signal
A25	CbCr7	A17	Y1	A9	Y0
A24	CbCr5	A16	CbCr2	A8	Y2
A23	CbCr3	A15	CbCr4	A7	SCLK
A22	CbCr1	A14	Y6	A6	MCLK
A21	CbCr0	A13	Y4	SPKR#	SDATA
A20	Y7	A12	CbCr6	IOIS16#	PCLK
A19	Y5	A11	VREF	INPACK#	LRCK
A18	Y3	A10	HREF		

Table 6.19. PC Card vs. ZV Port Signal Assignments.

Video Interface Port (VIP)

The VESA VIP specification is an enhancement to the BT.656 interface for ICs, previously discussed. The primary application is to interface up to four devices to a graphics controller chip, although the concept can easily be applied to other applications.

There are three sections to the interface:

Host Interface:

VIPCLK	host clock
HAD0–HAD7	host address/data bus
HCTL	host control

Video Interface:

PIXCLK	video sample clock
VID0–VID7	lower video data bus
VIDA, VIDB	10-bit data extension
XPIXCLK	video sample clock
XVID0–XVID7	upper video data bus
XVIDA, XVIDB	10-bit data extension

System Interface:

VRST#	reset
VIRQ#	interrupt request

The host interface signals are provided by the graphics controller. Essentially, a 2-, 4-, or 8-bit version of the PCI interface is used. VIPCLK has a frequency range of 25–33 MHz. PIXCLK and XPIXCLK have a maximum frequency of 75 and 80 MHz, respectively.

Video Interface

As with the BT.656 interface, special four-word sequences are inserted into the 8-bit or 10-bit 4:2:2 YCbCr video stream to indicate the start of active video (SAV) and end of active video (EAV). These sequences also indicate when horizontal and vertical blanking are present and which field is being transmitted.

VIP modifies the BT.656 EAV and SAV sequences as shown in Table 6.20. BT.656 uses four protection bits (P0–P3) in the status word since it was designed for long cable connections between equipment. With chip-to-chip interconnect, this protection isn't required, so the bits are used for other purposes. The timing of the H, V, and F signals for common video formats are illustrated in Chapter 4. The status word for VIP is defined as:

T = "0" for task B	T = "1" for task A
F = "0" for Field 1	F = "1" for Field 2
V = "1" during vertical blanking	
H = "0" at SAV	H = "1" at EAV

The task bit, T, is programmable. If BT.656 compatibility is required, it should always be a "1." Otherwise, it may be used to indicate which one of two data streams are present: stream A = "1" and stream B = "0." Alternately, T may be a "0" when raw 2× oversampled VBI data is present, and a "1" otherwise.

The noninterlaced bit, N, indicates whether the source is progressive ("1") or interlaced ("0").

The repeat bit, R, is a "1" if the current field is a repeat field. This occurs only during 3:2 pull-down. The repeat bit (R), in conjunction with the noninterlaced bit (N), enables the graphics controller to handle Bob and Weave, as well as 3:2 pull-down (further discussed in Chapter 7), in hardware.

The extra flag bit, E, is a "1" if another byte follows the EAV. Table 6.21 illustrates the extra flag byte. This bit is valid only during EAV sequences. If the E bit in the extra byte is "1," another extra byte immediately follows. This allows chaining any number of extra bytes together as needed.

	8-bit Data							
	D7 (MSB)	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
preamble	1	1	1	1	1	1	1	1
	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0
status word	T	F	V	H	N	R	0	E

Table 6.20. VIP EAV and SAV Sequence.

	8-bit Data							
	D7 (MSB)	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
extra byte	$\overline{D0}$	user defined						E

Table 6.21. VIP EAV Extra Byte.

Unlike pro-video interfaces, code 0x00 may be used during active video data to indicate an invalid video sample. This is used to accommodate scaled video and square pixel timing.

Video Data Formats

In the 8-bit mode (Figure 6.41), the video interface is similar to BT.656, except for the differences mentioned. XVID0–XVID7 are not used.

In the 16-bit mode (Figure 6.42), SAV sequences, EAV sequences, Y video data, ancillary packet headers, and even-numbered ancillary data values are transferred across the lower 8 bits (VID0–VID7). CbCr video data and odd-numbered ancillary data values are transferred across the upper 8 bits (XVID0–XVID7). Note that "skip data" (value 0x00) during active video must also appear in 16-bit format to preserve the 16-bit data alignment.

10-bit video data is supported by the VIDA, VIDB, XVIDA, and XVIDB signals. VIDA and XVIDA are the least significant bits.

Ancillary Data

Ancillary data packets are used to transmit information (such as digital audio, closed captioning, and teletext data) during the blanking intervals, as shown in Table 6.22. Unlike pro-video interfaces, the 0x00 and 0xFF values may be used by the ancillary data. Note that the ancillary data formats were defined prior to many of the pro-video ancillary data formats, and therefore may not match.

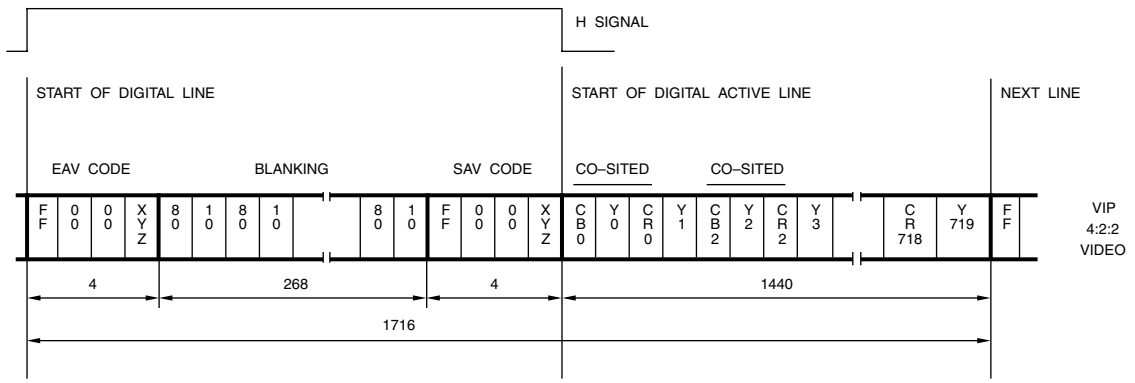


Figure 6.41. VIP 8-Bit Interface Data for One Scan Line. 480i; 720 active samples per line; 27 MHz clock.

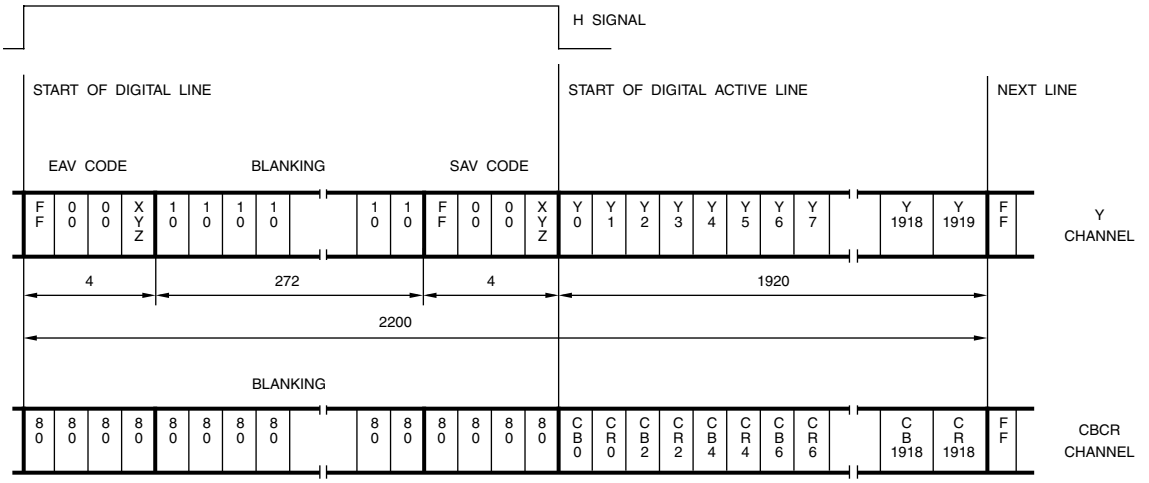


Figure 6.42. VIP 16-Bit Interface Data for One Scan Line. 1080i; 1920 active samples per line; 74.176 or 74.25 MHz clock.

	8-bit Data							
	D7 (MSB)	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ancillary data flag (ADF)	0	0	0	0	0	0	0	0
	1	1	1	1	1	1	1	1
	1	1	1	1	1	1	1	1
data ID (DID)	$\overline{D6}$	EP	0	1	0	DID2	DID1	DID0
SDID	$\overline{D6}$	EP	user defined value					
data count (DC)	$\overline{D6}$	EP	DC5	DC4	DC3	DC2	DC1	DC0
internal data ID 0	user defined value							
internal data ID 1	user defined value							
data word 0	D7	D6	D5	D4	D3	D2	D1	D0
:	:							
data word N	D7	D6	D5	D4	D3	D2	D1	D0
checksum	$\overline{D6}$	EP	CS5	CS4	CS3	CS2	CS1	CS0
optional fill data	$\overline{D6}$	EP	0	0	0	0	0	0

Note:
EP = even parity for D0–D5.

Table 6.22. VIP Ancillary Data Packet General Format.

DID2 of the DID field indicates whether Field 1 or Field 2 ancillary data is present:

0 Field 1
1 Field 2

DID1–DID0 of the DID field indicate the type of ancillary data present:

00 start of field
01 sliced VBI data, lines 1–23
10 end of field VBI data, line 23
11 sliced VBI data, line 24 to end of field

The data count value (DC) specifies the number of D-words (4-byte blocks) of ancillary data present. Thus, the number of data words in the ancillary packet after the DID must be a multiple of four. 1–3 optional fill bytes may be added after the checksum data to meet this requirement.

When DID1–DID0 are "00" or "10," no ancillary data or checksum is present. The data count (DC) value is "00000," and is the last field present in the packet.

Consumer Component Interfaces

Many solutions for transferring digital video between equipment have been developed over the years. HDMI, originally derived from DVI, is the most popular digital video interfaces for consumer equipment.

Digital Visual Interface (DVI)

In 1998, the Digital Display Working Group (DDWG) was formed to address the need for a standardized digital video interface between a PC and VGA monitor, as illustrated in Figure 6.43. The DVI 1.0 specification was released in April 1999.

Designed to transfer uncompressed real-time digital video, DVI supports PC graphics resolutions beyond 1600 × 1200 and HDTV resolutions, including 720p, 1080i, and 1080p.

In 2003, the consumer electronics industry started adding DVI outputs to DVD players and cable/satellite set-top boxes. DVI inputs also started appearing on digital televisions and LCD/plasma monitors.

Technology

DVI is based on the Digital Flat Panel (DFP) Interface, enhancing it by supporting more formats and timings. It also includes support for the High-bandwidth Digital Content Protection (HDCP) specification to deter unauthorized copying of content.

DVI also supports VESA's Extended Display Identification Data (EDID) standard, Display Data Channel (DDC) standard (used to read the EDID), and Monitor Timing Specification (DMT).

DDC and EDID enable automatic display detection and configuration. Extended Display Identification Data (EDID) was created to enable plug and play capabilities of displays. Data is stored in the display, describing the supported video formats. This information is supplied to the source device, over DVI, at the request of the source device. The source device then chooses its output format, taking into account the format of the original video stream and the formats supported by the display. The source device is responsible for the format conversions necessary to supply video in an understandable form to the display.

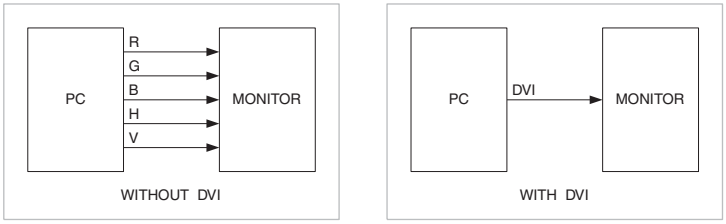


Figure 6.43. Using DVI to Connect a VGA Monitor to a PC.

In addition, the CEA-861 standard specifies mandatory and optionally supported resolutions and timings, and how to include data such as aspect ratio and format information.

TMDS Links

DVI uses transition-minimized differential signaling (TMDS). Eight bits of video data are converted to a 10-bit transition-minimized, DC-balanced value, which is then serialized. The receiver deserializes the data, and converts it back to 8 bits. Thus, to transfer digital R′G′B′ data requires three TMDS signals that comprise one TMDS link.

"TFT data mapping" is supported as the minimum requirement: 1 pixel per clock, 8 bits per channel, MSB justified.

Either one or two TMDS links may be used, as shown in Figures 6.44 and 6.45, depending on the formats and timing required. A system supporting two TMDS links must be able to switch dynamically between formats requiring a single link and formats requiring a dual link. A single DVI connector can handle two TMDS links.

A single TMDS link supports resolutions and timings using a video sample rate of 25–165 MHz. Resolutions and timings using a video sample rate of 165–330 MHz are implemented using two TMDS links, with each TMDS link operating at one-half the frequency. Thus, the two TMDS links share the same clock and the bandwidth is shared evenly between the two links.

Video Data Formats

Typically, 24-bit R′G′B′ data is transferred over a link. For applications requiring more than 8 bits per color component, the second TMDS link may be used for the additional least significant bits.

For PC applications, R′G′B′ data typically has a range of 0x00–0xFF. For consumer applications, R′G′B′ data typically has a range of 0x10–0xEB (values less than 0x10 or greater than 0xEB may be occasionally present due to processing).

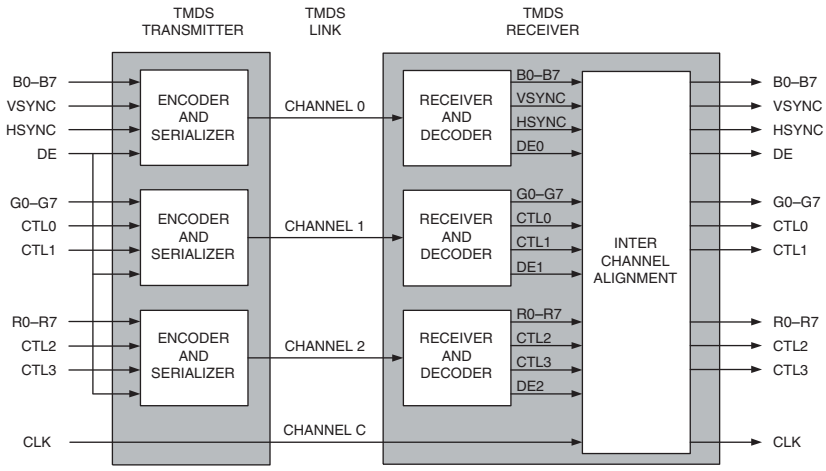


Figure 6.44. DVI Single TMDS Link.

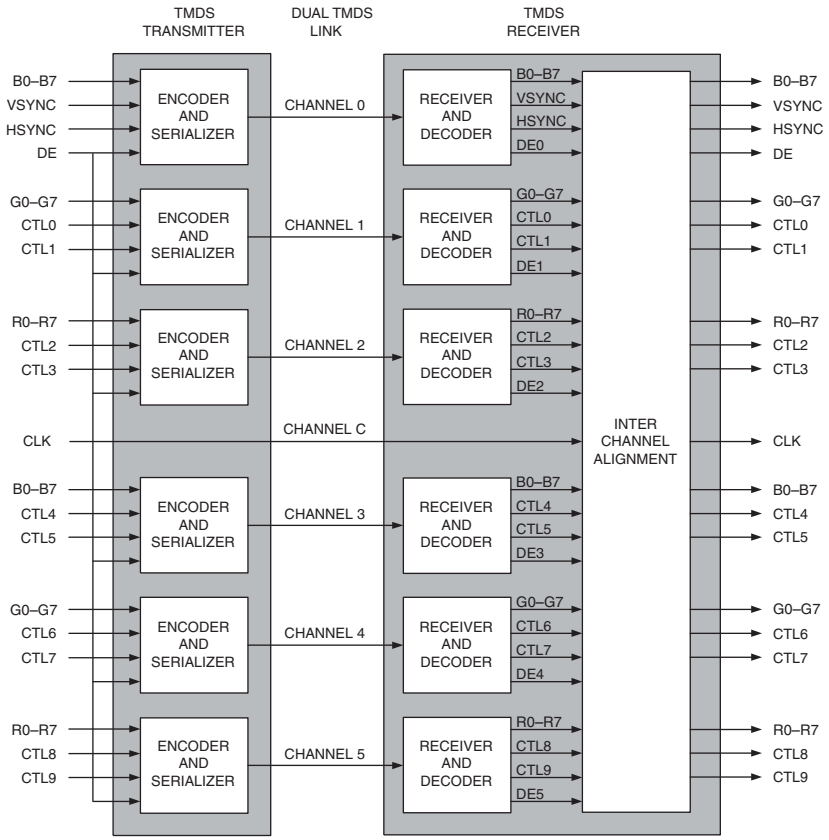


Figure 6.45. DVI Dual TMDS Link.

Control Signals

In addition to the video data, DVI transmitter and receiver chips typically use up to 14 control signals for interfacing to other chips in the system:

HSYNC	horizontal sync
VSYNC	vertical sync
DE	data enable
CTL0–CTL3	reserved (link 0)
CTL4–CTL9	reserved (link 1)
CLK	1× sample clock

While DE is a "1," active video is processed. While DE is a "0," the HSYNC, VSYNC, and CTL0–CTL9 signals are processed. HSYNC and VSYNC may be either polarity.

One issue is that some HDTVs use the falling edge of the YPbPr tri-level sync, rather than the center (rising edge), for horizontal timing. When displaying content from DVI, this results in the image shifting by 2.3%. Providing the ability to adjust the DVI embedded sync timing relative to the YPbPr tri-level sync timing is a useful capability in this case. Many fixed-pixel displays, such as DLP, LCD, and plasma, instead use the DE signal as a timing reference, avoiding the issue.

Digital-Only (DVI-D) Connector

The digital-only connector, which supports dual link operation, contains 24 contacts arranged as three rows of eight contacts, as shown in Figure 6.46. Table 6.23 lists the pin assignments.

Digital-Analog (DVI-I) Connector

In addition to the 24 contacts used by the digital-only connector, the 29-contact digital-analog connector adds five additional contacts to support analog video as shown in Figure 6.47. Table 6.24 lists the pin assignments.

HSYNC	horizontal sync
VSYNC	vertical sync
RED	analog red video
GREEN	analog green video
BLUE	analog blue video

The operation of the analog signals is the same as for a standard VGA connector.

DVI-A is available as a plug (male) connector only and mates to the analog-only pins of a DVI-I connector. DVI-A is only used in adapter cables, where there is the need to convert to or from a traditional analog VGA signal.

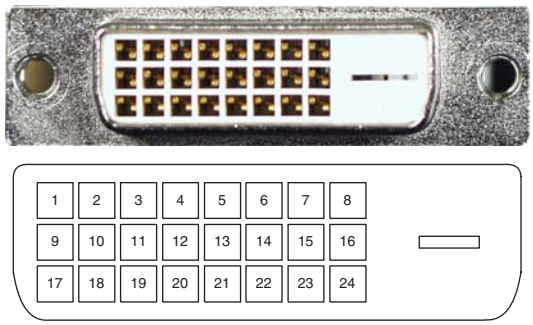


Figure 6.46. DVI-D Connector.

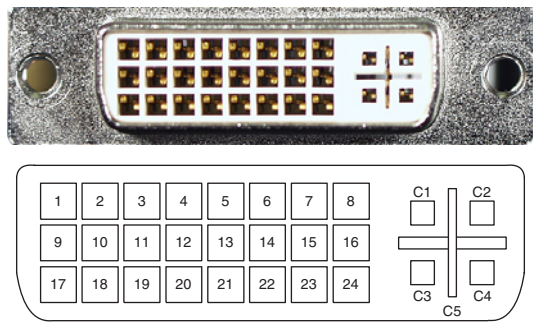


Figure 6.47. DVI-I Connector.

Pin	Signal	Pin	Signal	Pin	SIgnal
1	D2–	**9**	D1–	**17**	D0–
2	D2	**10**	D1	**18**	D0
3	shield	**11**	shield	**19**	shield
4	D4–	**12**	D3–	**20**	D5–
5	D4	**13**	D3	**21**	D5
6	DDC SCL	**14**	+5V	**22**	shield
7	DDC SDA	**15**	ground	**23**	CLK
8	reserved	**16**	Hot Plug Detect	**24**	CLK–

Table 6.23. DVI-D Connector Signal Assignments.

Pin	Signal	Pin	Signal	Pin	SIgnal
1	D2–	**9**	D1–	**17**	D0–
2	D2	**10**	D1	**18**	D0
3	shield	**11**	shield	**19**	shield
4	D4–	**12**	D3–	**20**	D5–
5	D4	**13**	D3	**21**	D5
6	DDC SCL	**14**	+5V	**22**	shield
7	DDC SDA	**15**	ground	**23**	CLK
8	VSYNC	**16**	Hot Plug Detect	**24**	CLK–
C1	RED	**C2**	GREEN	**C3**	BLUE
C4	HSYNC	**C5**	ground		

Table 6.24. DVI-I Connector Signal Assignments.

High-Definition Multimedia Interface (HDMI)

Although DVI handles transferring uncompressed real-time digital RGB video to a display, the consumer electronics industry preferred a smaller, more flexible solution, based on DVI technology. In April 2002, the HDMI working group was formed by Hitachi, Matsushita Electric (Panasonic), Philips, Silicon Image, Sony, Thomson, and Toshiba.

HDMI is capable of replacing up to eight audio cables (7.1 channels) and up to three video cables with a single cable, as illustrated in Figure 6.48. In 2004, the consumer electronics industry started adding HDMI outputs to DVD players and cable/satellite set-top boxes. HDMI inputs started appearing on digital televisions and monitors in 2005.

Through the use of an adaptor cable, HDMI is backwards compatible with equipment using DVI and the CEA-861 DTV profile. However, the advanced features of HDMI, such as digital audio, Consumer Electronics Control (used to enable passing control commands between equipment) and color gamut metadata, are not available.

Technology

HDMI, based on DVI, supports VESA's Extended Display Identification Data (EDID) standard and Display Data Channel (DDC) standard (used to read the EDID).

In addition, the CEA-861 standard specifies mandatory and optionally supported resolutions and timings, and how to include data such as aspect ratio and format information.

HDMI also supports the High-bandwidth Digital Content Protection (HDCP) specification to deter unauthorized copying of content. A common problem is sources not polling the TV often enough (twice per second) to see if its HDCP circuit is active. This results in snow if the TV's HDMI input is deselected, then later selected again.

The 19-pin Type A connector uses a single TMDS link and can therefore carry video signals with a 25–340 MHz sample rate. Video with sample rates below 25 MHz (i.e. 13.5 MHz 480i and 576i) are transmitted using a pixel-repetition scheme.

To support video signals sampled at greater than 340 MHz, the dual-link capability of the 29-pin Type B connector is used.

The 19-pin Type C connector, designed for mobile applications, is a smaller version of the Type A connector.

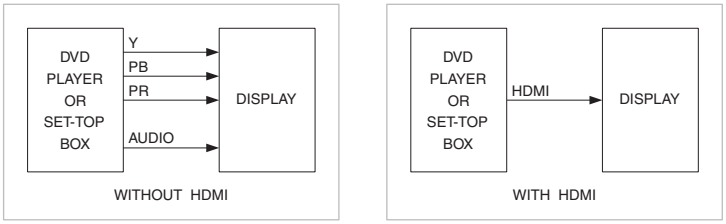


Figure 6.48. Using HDMI Eliminates Confusing Cable Connections for Consumers.

Video Data Formats

HDMI supports R′G′B′, 4:4:4 YCbCr, 4:2:2 YCbCr, 4:4:4 xvYCC and 4:2:2 xvYCC. 24, 30, 36 or 48 bits per pixel can be transferred; color depths greater than 24 bits per pixel are called "deep color".

Video data is either "full range" (0x00–0xFF for 8-bit RGB data) or "limited range" (0x10–0xEB for 8-bit RGB or Y data, 0x10–0xF0 for 8-bit CbCr data; values less than or greater than these may be present).

R′G′B′ data may be either "full range" or "limited range", except for the 640 × 480 resolution which must always be "full range".

YCbCr and xvYCC video data must always be "limited range".

Audio Data Formats

Driven by the DVD-Audio standard, audio support consists of 1–8 uncompressed audio streams with a sample rate of up to 48, 96, or 192 kHz, depending on the video format. It can alternately carry a compressed multi-channel audio stream at sample rates up to 192 kHz.

Digital Flat Panel (DFP) Interface

The VESA DFP interface was developed for transferring uncompressed digital video from a computer to a digital flat panel display. It supports VESA's Plug and Display (P&D) standard, Extended Display Identification Data (EDID) standard, Display Data Channel (DDC) standard, and Monitor Timing Specification (DMT). DDC and EDID enable automatic display detection and configuration. Only TFT data mapping is supported: 1 pixel per clock, 8 bits per channel, MSB justified.

Like DVI, DFP uses transition-minimized differential signaling (TMDS). 8 bits of video data are converted to a 10-bit transition-minimized, DC-balanced value, which is then serialized. The receiver deserializes the data, and converts it back to 8 bits. Thus, to transfer digital R′G′B′ data requires three TMDS signals that comprise one TMDS link. Cable lengths may be up to 5 meters.

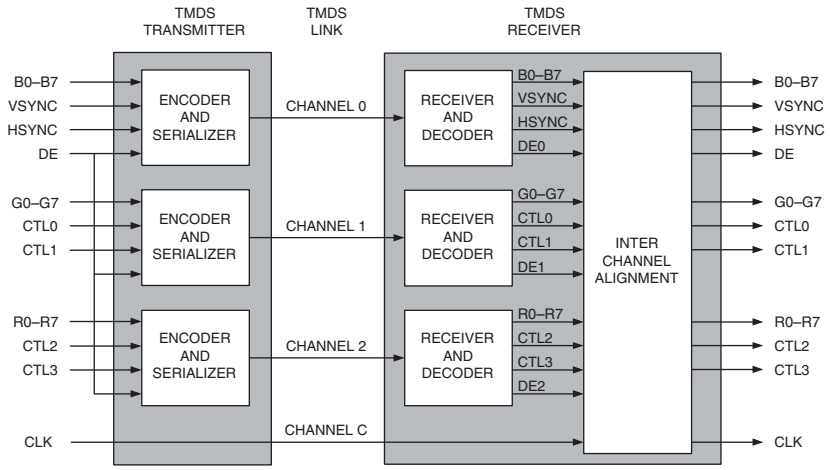


Figure 6.49. DFP TMDS Link.

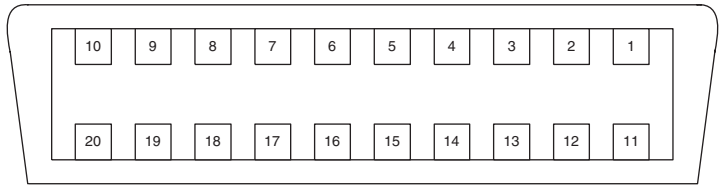


Figure 6.50. DFP Connector.

TMDS Links

A single TMDS link, as shown in Figure 6.49, supports formats and timings requiring a clock rate of 22.5–160 MHz.

Video Data Formats

24-bit R′G′B′ data is transferred over the link, as shown in Figure 6.49.

Control Signals

In addition to the video data, DFP transmitter and receiver chips typically use up to 8 control signals for interfacing to other chips in the system:

HSYNC	horizontal sync
VSYNC	vertical sync
DE	data enable
CTL0–CTL3	reserved
CLK	1× sample clock

While DE is a "1," active video is processed. While DE is a "0," the HSYNC, VSYNC, and CTL0–CTL3 signals are processed. HSYNC and VSYNC may be either polarity.

Connector

The 20-pin mini-D ribbon (MDR) connector contains 20 contacts arranged as two rows of ten contacts, as shown in Figure 6.25. Table 6.39 lists the pin assignments.

Pin	Signal	Pin	Signal
1	D1	**11**	D2
2	D1–	**12**	D2–
3	shield	**13**	shield
4	shield	**14**	shield
5	CLK	**15**	D0
6	CLK–	**16**	D0–
7	ground	**17**	no connect
8	+5V	**18**	Hot Plug Detect
9	no connect	**19**	DDC SDA
10	no connect	**20**	DDC SCL

Table 6.25. DFP Connector Signal Assignments.

Open LVDS Display Interface (OpenLDI)

OpenLDI was developed for transferring uncompressed digital video from a computer to a digital flat panel display. It enhances the FPD-Link standard used to drive the displays of laptop computers, and adds support for VESA's Plug and Display (P&D) standard, Extended Display Identification Data (EDID) standard, and Display Data Channel (DDC) standard. DDC and EDID enable automatic display detection and configuration.

Unlike DVI and DFP, OpenLDI uses low-voltage differential signaling (LVDS). Cable lengths may be up to 10 meters.

LVDS Link

The LVDS link, as shown in Figure 6.51, supports formats and timings requiring a clock rate of 32.5–160 MHz.

Eight serial data lines (A0–A7) and two sample clock lines (CLK1 and CLK2) are used. The number of serial data lines actually used is dependent on the pixel format, with the serial data rate being 7× the sample clock rate. The CLK2 signal is used in the dual pixel modes for backwards compatibility with FPD-Link receivers.

Video Data Formats

18-bit single pixel, 24-bit single pixel, 18-bit dual pixel, or 24-bit dual pixel R′G′B′ data is transferred over the link. Table 6.26 illustrates the mapping between the pixel data bit number and the OpenLDI bit number.

The 18-bit single pixel R′G′B′ format uses three 6-bit R′G′B′ values: R0–R5, G0–G5, and B0–B5. OpenLDI serial data lines A0–A2 are used to transfer the data.

The 24-bit single pixel R′G′B′ format uses three 8-bit R′G′B′ values: R0–R7, G0–G7, and B0–B7. OpenLDI serial data lines A0–A3 are used to transfer the data.

The 18-bit dual pixel R′G′B′ format represents two pixels as three upper/lower pairs of 6-bit R′G′B′ values: RU0–RU5, GU0–GU5, BU0–BU5, RL0–RL5, GL0–GL5, BL0–BL5. Each upper/lower pair represents two pixels. OpenLDI serial data lines A0–A2 and A4–A6 are used to transfer the data.

The 24-bit dual pixel R′G′B′ format represents two pixels as three upper/lower pairs of 8-bit R′G′B′ values: RU0–RU7, GU0–GU7, BU0–BU7, RL0–RL7, GL0–GL7, BL0–BL7. Each upper/lower pair represents two pixels. OpenLDI serial data lines A0–A7 are used to transfer the data.

Control Signals

In addition to the video data, OpenLDI transmitter and receiver chips typically use up to seven control signals for interfacing to other chips in the system:

HSYNC	horizontal sync
VSYNC	vertical sync
DE	data enable
CNTLE	reserved
CNTLF	reserved
CLK1	1× sample clock
CLK2	1× sample clock

During unbalanced operation, the DE, HSYNC, VSYNC, CNTLE, and CNTLF levels are sent as unencoded bits within the A2 and A6 bitstreams.

During balanced operation (used to minimize short- and long-term DC bias), a DC Balance bit is sent within each of the A0–A7 bitstreams to indicate whether the data is unmodified or inverted. Since there is no room left for the control signals to be sent directly, the DE level is sent by slightly modifying the

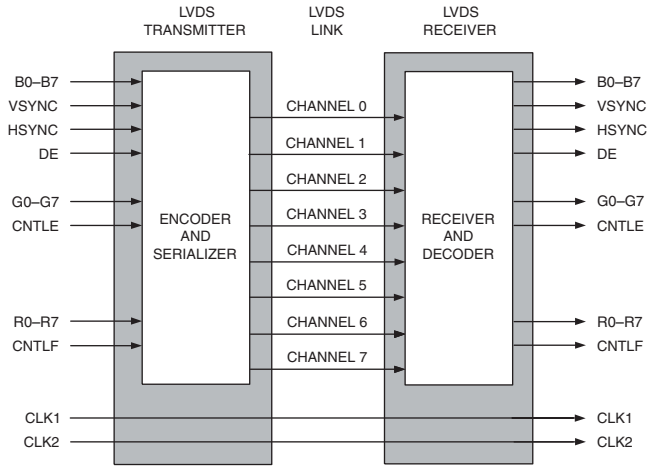


Figure 6.51. OpenLDI LVDS Link.

18 Bits per Pixel Bit Number	24 Bits per Pixel Bit Number	OpenLDI Bit Number
5	7	5
4	6	4
3	5	3
2	4	2
1	3	1
0	2	0
	1	7
	0	6

Table 6.26. OpenLDI Bit Number Mappings.

timing of the falling edge of the CLK1 and CLK2 signals. The HSYNC, VSYNC, CNTLE, and CNTLF levels are sent during the blanking intervals using 7-bit code words on the A0, A1, A5, and A4 signals, respectively.

Connector

The 36-pin mini-D ribbon (MDR) connector is similar to the one shown in Figure 6.50, except that there are two rows of eighteen contacts. Table 6.27 lists the pin assignments.

Gigabit Video Interface (GVIF)

The Sony GVIF was developed for transferring uncompressed digital video using a single differential signal, instead of the multiple signals that DVI, DFP, and OpenLDI use. Cable lengths may be up to 10 meters.

GVIF Link

The GVIF link, as shown in Figure 6.52, supports formats and timings requiring a clock rate of 20–80 MHz. For applications requiring higher clock rates, more than one GVIF link may be used.

The serial data rate is 24× the sample clock rate for 18-bit R′G′B′ data, or 30× the sample clock rate for 24-bit R′G′B′ data.

Video Data Formats

18-bit or 24-bit R′G′B′ data, plus timing, is transferred over the link. The 18-bit R′G′B′ format uses three 6-bit R′G′B′ values: R0–R5, G0–G5, and B0–B5. The 24-bit R′G′B′ format uses three 8-bit R′G′B′ values: R0–R7, G0–G7, and B0–B7.

Pin	Signal	Pin	Signal	Pin	Signal
1	A0–	13	+5V	25	reserved
2	A1–	14	A4–	26	reserved
3	A2–	15	A5–	27	ground
4	CLK1–	16	A6–	28	DDC SDA
5	A3–	17	A7–	29	ground
6	ground	18	CLK2–	30	USB–
7	reserved	19	A0	31	ground
8	reserved	20	A1	32	A4
9	reserved	21	A2	33	A5
10	DDC SCL	22	CLK1	34	A6
11	+5V	23	A3	35	A7
12	USB	24	reserved	36	CLK2

Table 6.27. OpenLDI Connector Signal Assignments.

18-bit R′G′B′ data is converted to 24-bit data by slicing the R′G′B data into six 3-bit values that are in turn transformed into six 4-bit codes. This ensures rich transitions for receiver PLL locking and good DC balance.

24-bit R′G′B′ data is converted to 30-bit data by slicing the R′G′B data into six 4-bit values that are in turn transformed into six 5-bit codes.

Control Signals

In addition to the video data, there are six control signals:

HSYNC	horizontal sync
VSYNC	vertical sync
DE	data enable
CTL0	reserved
CTL1	reserved
CLK	1× sample clock

If any of the HSYNC, VSYNC, DE, CTL0, or CTL1 signals change, during the next CLK cycle a special 30-bit format is used. The first 6 bits are header data indicating the new levels of HSYNC, VSYNC, DE, CTL0, or CTL1. This is followed by 24 bits of R′G′B′ data (unencoded except for inverting the odd bits).

Note that during the blanking periods, non-video data, such as digital audio, may be transferred. The CTL signals may be used to indicate when non-video data is present.

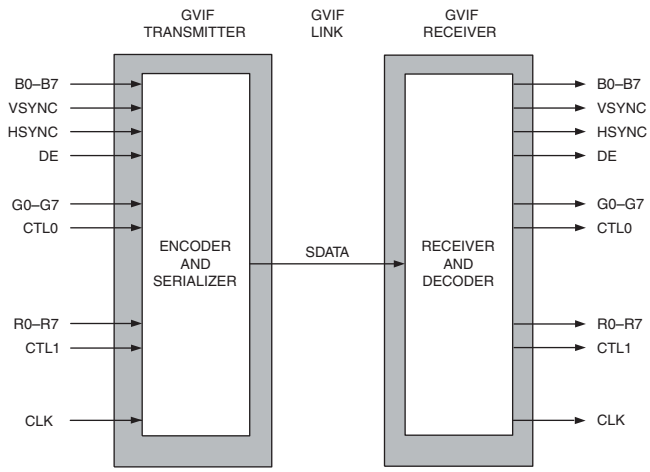


Figure 6.52. GVIF Link.

Consumer Transport Interfaces

Several transport interfaces, such as USB 2.0, Ethernet, and IEEE 1394, are available for consumer products. Of course, each standard has its own advantages and disadvantages.

USB 2.0

Well known in the PC market for connecting peripherals to a PC, there is growing interest in using USB (Universal Serial Bus) 2.0 to transfer compressed audio/video data between products.

USB 2.0 is capable of operating up to 480 Mbps and supports an isochronous mode to guarantee data delivery timing. Thus, it can easily transfer compressed real-time audio/video data from a cable/satellite set-top box or DVD player to a digital television. DTCP (Digital Transmission Copy Protection) may be used to encrypt the audio and video content over USB.

Due to USB's lower cost and widespread usage, many companies are interested in using USB 2.0 instead of IEEE 1394 to transfer compressed audio/video data between products. However, some still prefer IEEE 1394 since the methods for transferring various types of data are much better defined.

USB On-the-Go

With portable devices increasing in popularity, there was a growing desire for them to communicate directly with each other without requiring a PC or other USB host.

On-the-Go addresses this desire by allowing a USB device to communicate directly with other On-the-Go products. It also features a smaller USB connector and low power features to preserve battery life.

Ethernet

With the widespread adoption of home networks, DSL, and FTTH (Fiber-to-the-Home), Ethernet has become a common interface for transporting digital audio and video data. Initially used for file transfers, streaming of real-time compressed video over wired (802.3) or wireless (802.11) Ethernet networks is now becoming common.

Ethernet supports up to 1 Gbps. DTCP/IP (Digital Transmission Copy Protection for Internet Protocol) may be used to encrypt the audio and video content over wired or wireless networks.

IEEE 1394

IEEE 1394 was originally developed by Apple Computer as Firewire. Designed to be a generic interface between devices, 1394 specifies the physical characteristics; separate application-specific specifications describe how to transfer data over the 1394 network.

1394 is a transaction-based packet technology, using a bi-directional serial interconnect that features hot plug-and-play. This enables devices to be connected and disconnected without affecting the operation of other devices connected to the network.

Guaranteed delivery of time-sensitive data is supported, enabling digital audio and video to be transferred in real time. In addition, multiple independent streams of digital audio and video can be carried.

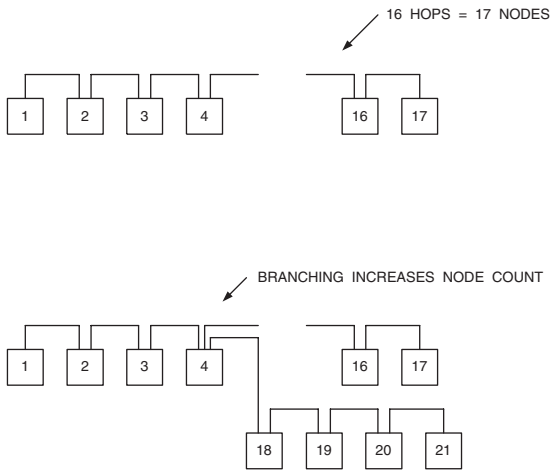


Figure 6.53. IEEE 1394 Network Topology Examples.

Specifications

The original 1394-1995 specification supports bit-rates of 98.304, 196.608, and 393.216 Mbps.

The 1394A-2000 specification clarifies areas that were vague and led to system interoperability issues. It also reduces the overhead lost to bus control, arbitration, bus reset duration, and concatenation of packets. 1394A-2000 also introduces advanced power-saving features. The electrical signaling method is also common between 1394-1995 and 1394A-2000, using data-strobe (DS) encoding and analog-speed signaling.

The 1394B-2002 specification adds support for bit-rates of 786.432, 1572.864, and 3145.728 Mbps. It also includes

- 8B/10B encoding technique used by Gigabit Ethernet
- Continuous dual simplex operation
- Longer distance (up to 100 meters over Cat5)
- Changes the speed signaling to a more digital method
- Three types of ports: Legacy (1395A compatible), Beta, and Bilingual (supports both Legacy and Beta). Connector keying ensures that incompatible connections cannot physically be made.

Endian Issues

1394 uses a big-endian architecture, defining the most significant bit as bit 0. However, many processors are based on the little endian architecture which defines the most significant bit as bit 31 (assuming a 32-bit word).

Network Topology

Like many networks, there is no designated bus master. The tree-like network structure has a root node, branching out to logical nodes in other devices (Figure 6.53). The root is responsible for certain control functions, and is chosen during initialization. Once chosen, it retains that function for as long as it

remains powered on and connected to the network.

A network can include up to 63 nodes, with each node (or device) specified by a 6-bit physical identification number. Multiple networks may be connected by bridges, up to a system maximum of 1,023 networks, with each network represented by a separate 10-bit bus ID. Combined, the 16-bit address allows up to 64,449 nodes in a system. Since device addresses are 64 bits, and 16 of these bits are used to specify nodes and networks, 48 bits remain for memory addresses, allowing up to 256TB of memory space per node.

Node Types

Nodes on a 1394 bus may vary in complexity and capability (listed simplest to most complex):

Transaction nodes respond to asynchronous communication, implement the minimal set of control status registers (CSR), and implement a minimal configuration ROM.

Isochronous nodes add a 24.576 MHz clock used to increment a cycle timer register that is updated by cycle start packets.

Cycle master nodes add the ability to generate the 8 kHz cycle start event, generate cycle start packets, and implement a bus timer register.

Isochronous resource manager (IRM) nodes add the ability to detect bad self-ID packets, determine the node ID of the chosen IRM, and implement the channels available, bandwidth available, and bus manager ID registers. At least one node must be capable of acting as an IRM to support isochronous communication.

Bus manager (BM) nodes are the most complex. This level adds responsibility for storing every self-ID packet in a topology map and analyzing that map to produce a speed map of the entire bus. These two maps are used to manage the bus. Finally, the BM must be able to activate the cycle master node, write configuration packets to allow optimization of the bus, and act as the power manager.

Node Ports

In the network topology, a one-port device is known as a "leaf" device since it is at the end of a network branch. They can be connected to the network, but cannot expand the network.

Two-port devices can be used to form daisy-chained topologies. They can be connected to and continue the network, as shown in Figure 6.53. Devices with three or more ports are able to branch the network to the full 63-node capability.

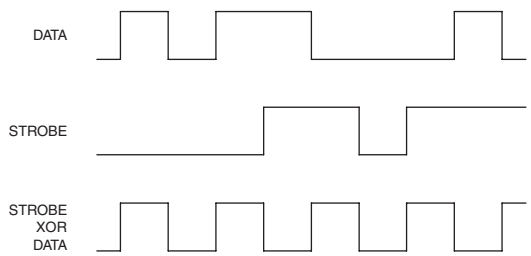


Figure 6.54. IEEE 1394 Data and Strobe Signal Timing.

It is important to note that no loops or parallel connections are allowed within the network. Also, there are no reserved connectors—any connector may be used to add a new device to the network.

Since 1394-1995 mandates a maximum of 16 cable hops between any two nodes, a maximum of 17 peripherals can be included in a network if only two-port peripherals are used. Later specifications implement a ping packet to measure the round-trip delay to any node, removing the 16 hop limitation.

For 1394-1995 and 1394A-2000, a 4- or 6-pin connector is used. The 6-pin connector can provide power to peripherals. For 1394B-2002, the 9-pin Beta and Bilingual connector includes power, two extra pins for signal integrity, and one pin for reserved for future use.

Figure 6.54 illustrates the 1394-1995 and 1394A-2000 data and strobe timing. The strobe signal changes state on every bit period for which the data signal does not. Therefore, by exclusive-ORing the data and strobe signals, the clock is recovered.

Physical Layer

The typical hardware topology of a 1394 network consists of a physical layer (PHY) and link layer (LINK), as shown in Figure 6.55. The 1394-1995 standard also defined two software layers, the transaction layer and the bus management layer, parts of which may be implemented in hardware.

The PHY transforms the point-to-point network into a logical physical bus. Each node is also essentially a data repeater since data is

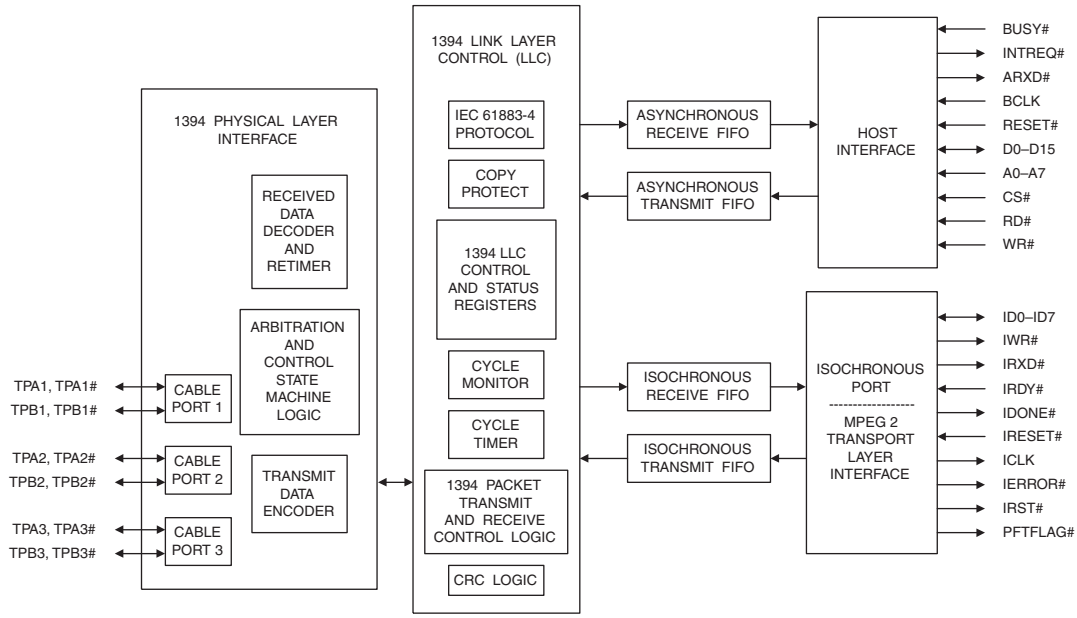


Figure 6.55. IEEE 1394 Typical Physical and Link Layer Block Diagrams.

reclocked at each node. The PHY also defines the electrical and mechanical connection to the network. Physical signaling circuits and logic responsible for power-up initialization, arbitration, bus-reset sensing, and data signaling are also included.

Link Layer

The Link provides interfacing between the physical layer and application layer, formatting data into packets for transmission over the network. It supports both asynchronous and isochronous data.

Asynchronous Data

Asynchronous packets are guaranteed delivery since after an asynchronous packet is received, the receiver transmits an acknowledgment to the sender, as shown in Figure 6.56. However, there is no guaranteed bandwidth. This type of communication is useful for commands, non-real-time data, and error-free transfers.

The delivery latency of asynchronous packets is not guaranteed and depends upon the network traffic. However, the sender may continually retry until an acknowledgment is received.

Asynchronous packets are targeted to one node on the network or can be sent to all nodes, but cannot be broadcast to a subset of nodes on the bus.

The maximum asynchronous packet size is:

512 * (n / 100) bytes

n = network speed in Mbps

Isochronous Data

Isochronous communications have a guaranteed bandwidth, with up to 80% of the network bandwidth available for isochronous use. Up to 63 independent isochronous channels are available, although the 1394 Open Host Controller Interface (OHCI) currently only supports 4–32 channels. This type of communi-

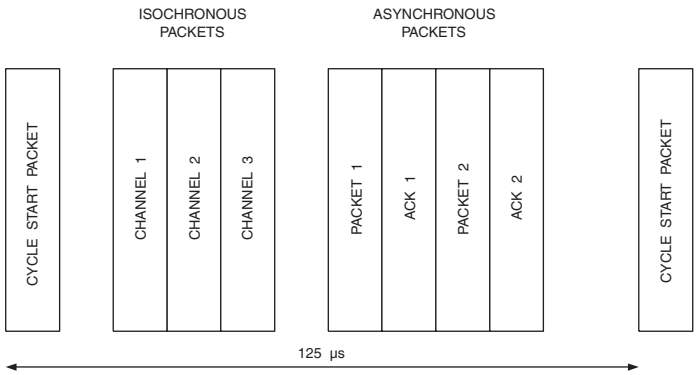


Figure 6.56. IEEE 1394 Isochronous and Asynchronous Packets.

cation is useful for real-time audio and video transfers since the maximum delivery latency of isochronous packets is calculable and may be targeted to multiple destinations. However, the sender may not retry sending a packet.

The maximum isochronous packet size is:

1024 * (n / 100) bytes

n = network speed in Mbps

Isochronous operation guarantees a time slice each 125 µs. Since time slots are guaranteed, and isochronous communication takes priority over asynchronous, isochronous bandwidth is assured.

Once an isochronous channel is established, the sending device is guaranteed to have the requested amount of bus time for that channel every isochronous cycle. Only one device may send data on a particular channel, but any number of devices may receive data on a channel. A device may use multiple isochronous channels as long as capacity is available.

Transaction Layer

The transaction layer supports asynchronous write, read, and lock commands. A lock combines a write with a read by producing a round trip routing of data between the sender and receiver, including processing by the receiver.

Bus Management Layer

The bus management layer control functions of the network at the physical, link, and transaction layers.

Digital Transmission Content Protection (DTCP)

To prevent unauthorized copying of content, the DTCP system was developed. Although originally designed for 1394, it is applicable to any digital network that supports bi-directional communications, such as USB and Ethernet.

Device authentication, content encryption, and renewability (should a device ever be compromised) are supported by DTCP. The Digital Transmission Licensing Administrator (DTLA) licenses the content protection system and distributes cipher keys and device certificates.

DTCP outlines four elements of content protection:

1. Copy control information (CCI)
2. Authentication and key exchange (AKE)
3. Content encryption
4. System renewability

Copy Control Information (CCI)

CCI allows content owners to specify how their content can be used, such as "copy-never," "copy-one-generation," "no-more-copies," and "copy-free." DTCP is capable of securely communicating copy control information between devices. Two different CCI mechanisms are supported: *embedded* and *encryption mode indicator.*

Embedded CCI is carried within the content stream. Tampering with the content stream results in incorrect decryption, maintaining the integrity of the embedded CCI.

The *encryption mode indicator* (EMI) provides a secure, yet easily accessible, transmission of CCI by using the two most significant bits of the sync field of the isochronous packet header. Devices can immediately determine the CCI of the content stream without decoding the content. If the two EMI bits are tampered with, the encryption and decryption modes do not match, resulting in incorrect content decryption.

Authentication and Key Exchange (AKE)

Before sharing content, a device must first verify that the other device is authentic. DTCP includes a choice of two authentication levels: *full* and *restricted*. Full authentication can be used with all content protected by the system. Restricted authentication enables the protection of "copy-one-generation" and "no-more-copies" content only.

Full Authentication

Compliant devices are assigned a unique public/private key pair and a device certificate by the DTLA, both stored within the device so as to prevent their disclosure. In addition, devices store other necessary constants and keys.

Full authentication uses the public key-based digital signature standard (DSS) and Diffie-Hellman (DH) key exchange algorithms. DSS is a method for digitally signing and verifying the signatures of digital documents to verify the integrity of the data. DH key exchange is used to establish control-channel symmetric cipher keys, which allows two or more devices to generate a shared key.

Initially, the receiver sends a request to the source to exchange device certificates and random challenges. Then, each device calculates a DH key exchange first-phase value. The devices then exchange signed messages that contain the following elements:

1. The other device's random challenge
2. The DH key-exchange first-phase value
3. The renewability message version number of the newest system renewability message (SRM) stored by the device

The devices check the message signatures using the other device's public key to verify that the message has not been tampered with and also verify the integrity of the other device's certificate. Each device also examines the certificate revocation list (CRL) embedded in its system renewability message (SRM) to verify that the other device's certificate has not been revoked due to its security having been compromised. If no errors have occurred, the two devices have successfully authenticated each other and established an authorization key.

Restricted Authentication

Restricted authentication may be used between sources and receivers for the exchange of "copy-one-generation" and "no-more-copies" contents. It relies on the use of a shared secret to respond to a random challenge.

The source initiates a request to the receiver, requests its device ID, and sends a random challenge. After receiving the challenge back from the source, the receiver computes a response and sends it to the source.

The source compares this response with similar information generated by the source using its service key and the ID of the receiver. If the comparison matches its own calculation, the receiver has been verified and authenticated. The source and receiver then each calculate an authorization key.

Content Encryption

To ensure interoperability, all compliant devices must support the 56-bit M6 baseline cipher. Additional content protection may be supported by using additional, optional ciphers.

System Renewability

Devices that support full authentication can receive and process SRMs that are created by the DTLA and distributed with content. Sys-

tem renewability is used to ensure the long-term system integrity by revoking the device IDs of compromised devices.

SRMs can be updated from other compliant devices that have a newer list, from media with prerecorded content, or via compliant devices with external communication capability (Internet, phone, cable, network, and so on).

Example Operation

For this example, the source has been instructed to transmit a copy-protected system stream of content.

The source initiates the transmission of content marked with the copy protection status: "copy-one-generation," "copy-never," "no-more-copies," or "copy-free."

Upon receiving the content stream, the receiver determines the copy protection status. If marked "copy never," the receiver requests that the source initiate full authentication. If the content is marked "copy once" or "no more copies," the receiver will request full authentication if supported, or restricted authentication if it isn't.

When the source receives the authentication request, it proceeds with the requested type of authentication. If full authentication is requested but the source can only support restricted authentication, then restricted authentication is used.

Once the devices have completed the authentication procedure, a content-channel encryption key (content key) is exchanged between them. This key is used to encrypt the content at the source device and decrypt the content at the receiver.

1394 Open Host Controller Interface (OHCI)

The 1394 Open Host Controller Interface (OHCI) specification is an implementation of the 1394 link layer, with additional features to support the transaction and bus management layers. It provides a standardized way of interacting with the 1394 network.

Home AV Interoperability (HAVi)

Home AV Interoperability (HAVi) is another layer of protocols for 1394. HAVi is directed at making 1394 devices plug-and-play interoperable in a 1394 network whether or not a PC host is present.

Serial Bus Protocol (SBP-2)

The ANSI Serial Bus Protocol 2 (SBP-2) defines standard way of delivering command and status packets over 1394 for devices such DVD players, printers, scanners, hard drives, and other devices.

IEC 61883 Specifications

Certain types of isochronous signals, such as MPEG-2 and the IEC 61834, SMPTE 314M, and ITU-R BT.1618 digital video (DV) standards, use specific data transport protocols and formats. When this data is sent isochronously over a 1394 network, special packetization techniques are used.

The IEC 61883 series of specifications define the details for transferring various application-specific data over 1394:

IEC 61883-1 = General specification

IEC 61883-2 = SD-DVCR data transmission 25 Mbps continuous bit-rate

IEC 61883-3 = HD-DVCR data transmission

IEC 61883-4 = MPEG-2 TS data transmission bit-rate bursts up to 44 Mbps

IEC 61883-5 = SDL-DVCR data transmission

IEC 61883-6 = Audio and music data transmission

IEC 61883-7 = Transmission of ITU-R BO.1294 System B

IEC 61883-1

IEC 61883-1 defines the general structure for transferring digital audio and video data over 1394. It describes the general packet format, data flow management, and connection management for digital audio and video data, and also the general transmission rules for control commands.

A common isochronous packet (CIP) header is placed at the beginning of the data field of isochronous data packets, as shown in Figure 6.57. It specifies the source node, data block size, data block count, time stamp, type of real-time data contained in the data field, etc.

A connection management procedure (CMP) is also defined for making isochronous connections between devices.

In addition, a functional control protocol (FCP) is defined for exchanging control commands over 1394 using asynchronous data.

IEC 61883-2

IEC 61883-2 and SMPTE 396M define the CIP header, data packet format, and transmission timing for IEC 61834, SMPTE 314M, and ITU-R BT.1618 digital video (DV) standards over 1394. Active resolutions of 720 × 480 (at 29.97 frames per second) and 720 × 576 (at 25 frames per second) are supported.

DV data packets are 488 bytes long, made up of 8 bytes of CIP header and 480 bytes of DV data, as shown in Figure 6.57. Figure 6.58 illustrates the frame data structure.

Each of the 720 × 480 4:1:1 YCbCr frames are compressed to 103,950 bytes, resulting in a 4.9:1 compression ratio. Including overhead and audio increases the amount of data to 120,000 bytes.

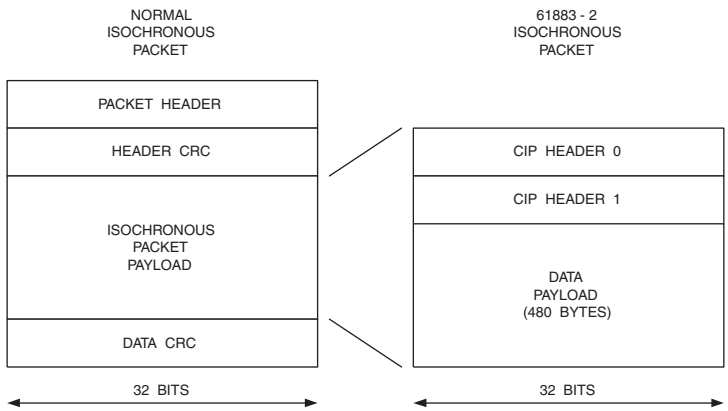


Figure 6.57. 61883-2 Isochronous Packet Formatting.

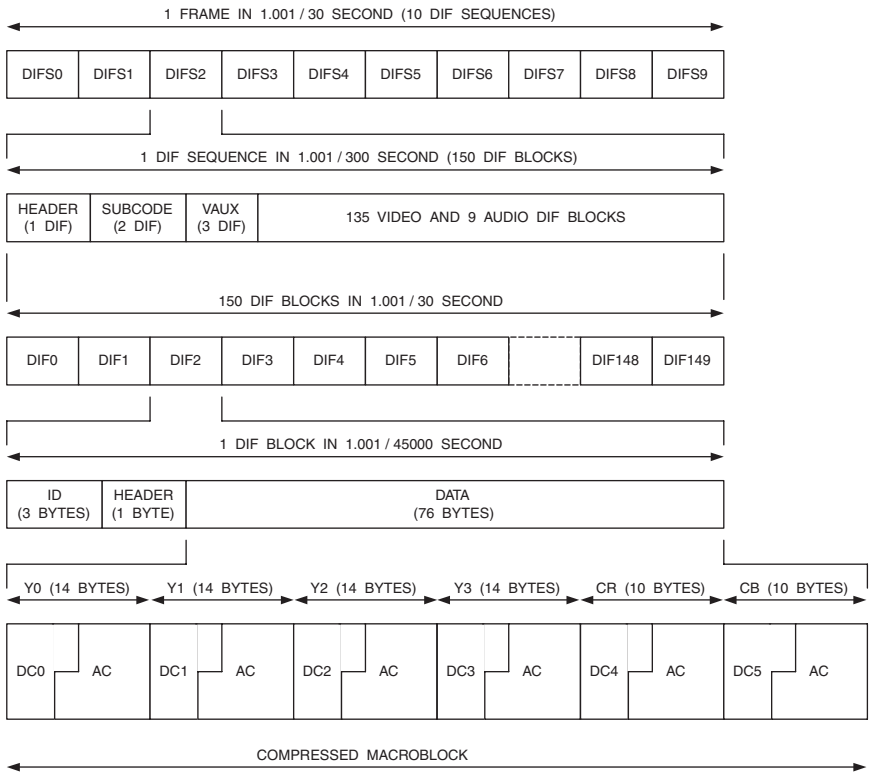


Figure 6.58. IEC 61834, SMPTE 314M, and ITU-R BT.1618 Packet Formatting for 720 × 480 Systems (4:1:1 YCbCr).

The compressed 720 × 480 frame is divided into 10 DIF (data in frame) sequences. Each DIF sequence contains 150 DIF blocks of 80 bytes each, used as follows:

135 DIF blocks for video

9 DIF blocks for audio

6 DIF blocks used for Header, Subcode, and Video Auxiliary (VAUX) information

Figure 6.59 illustrates the DIF sequence structure in detail. The audio DIF blocks contain both audio data and audio auxiliary data (AAUX). IEC 61834 supports four 32-kHz, 12-bit nonlinear audio signals or two 48-, 44.1-, or 32-kHz, 16-bit audio signals. SMPTE 314M and ITU-R BT.1618 at 25 Mbps support two 48-kHz 16-bit audio signals, while the 50 Mbps version supports four. Video auxiliary data (VAUX) DIF blocks include recording date and time, lens aperture, shutter speed, color balance, and other camera setting data. The subcode DIF blocks store a variety of information, the most important of which is timecode.

Each video DIF block contains 80 bytes of compressed macroblock data:

3 bytes for DIF block ID information

1 byte for the header that includes the quantization number (QNO) and block status (STA)

14 bytes each for Y0, Y1, Y2, and Y3

10 bytes each for Cb and Cr

As the 488-byte packets come across the 1394 network, the start of a video frame is determined. Once the start of a frame is detected, 250 valid packets of data are collected to have a complete DV frame; each packet contains 6 DIF blocks of data. Every 15th packet is a null packet and should be discarded. Once 250 valid packets of data are in the buffer, discard the CIP headers. If all went well, you have a frame buffer with a 120,000 byte compressed DV frame in it.

720 × 576 frames may use either the 4:2:0 YCbCr format (IEC 61834) or the 4:1:1 YCbCr format (SMPTE 314M and ITU-R BT.1618), and require 12 DIF sequences. Each 720 × 576 frame is compressed to 124,740 bytes. Including overhead and audio increases the amount of data to 144,000 bytes, requiring 300 packets to transfer.

Note that the organization of data transferred over 1394 differs from the actual DV recording format since error correction is not required for digital transmission. In addition, although the video blocks are numbered in sequence in Figure 6.59, the sequence does not correspond to the left-to-right, top-to-bottom transmission of blocks of video data. Compressed macroblocks are shuffled to minimize the effect of errors and aid in error concealment. Audio data also is shuffled. Data is transmitted in the same shuffled order as recorded.

To illustrate the video data shuffling, DV video frames are organized as 50 superblocks, with each superblock being composed of 27 compressed macroblocks, as shown in Figure 6.60. A group of 5 superblocks (one from each superblock column) make up one DIF sequence. Table 6.28 illustrates the transmission order of the DIF blocks. Additional information on the DV data structure is available in Chapter 11.

IEC 61883-4

IEC 61883-4 defines the CIP header, data packet format, and transmission timing for MPEG-2 transport streams over 1394.

It is most efficient to carry an integer number of 192 bytes (188 bytes of MPEG-2 data plus 4 bytes of time stamp) per isochronous packet, as shown in Figure 6.61. However, MPEG data rates are rarely integer multiples of the isochronous data rate. Thus, it is more

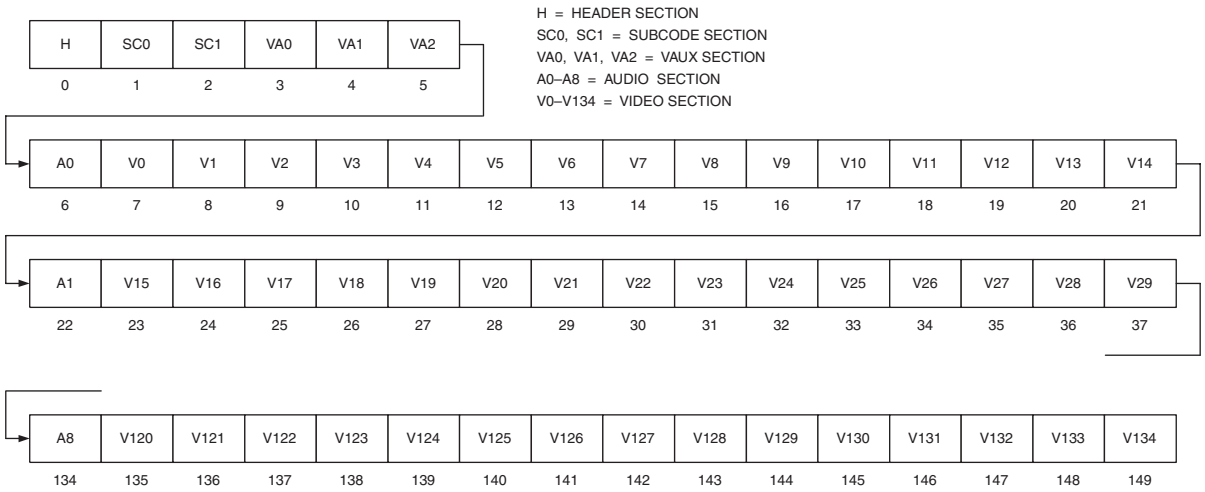


Figure 6.59. IEC 61834, SMPTE 314M, and ITU-R BT.1618 DIF Sequence Detail (25 Mbps).

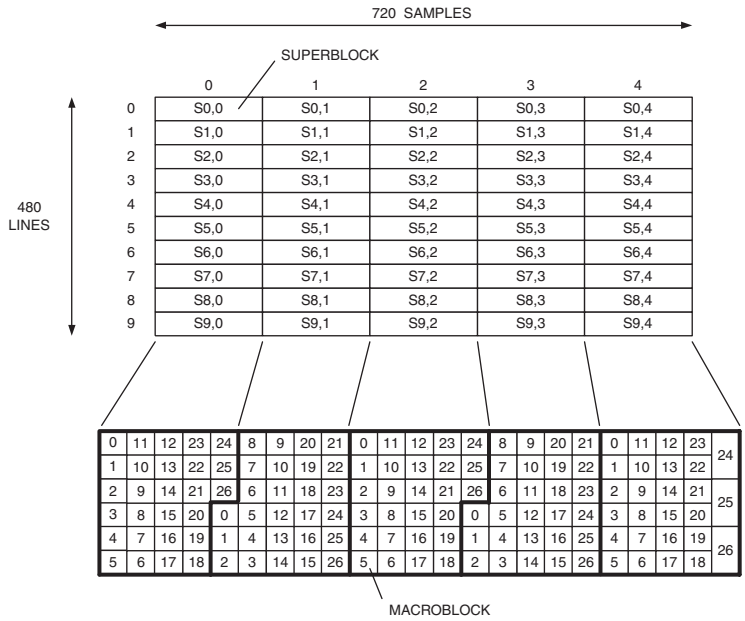


Figure 6.60. Relationship Between Superblocks and Macroblocks (720 × 480, 4:1:1 YCbCr).

DIF Sequence Number	Video DIF Block Number	Compressed Macroblock		DIF Sequence Number	Video DIF Block Number	Compressed Macroblock	
		Superblock Number	Macroblock Number			Superblock Number	Macroblock Number
0	0	2, 2	0	:			
	1	6, 1	0	n–1	0	1, 2	0
	2	8, 3	0		1	5, 1	0
	3	0, 0	0		2	7, 3	0
	4	4, 4	0		3	n–1, 0	0
	:				4	3, 4	0
	133	0, 0	26		:		
	134	4, 4	26		133	n–1, 0	26
1	0	3, 2	0		134	3, 4	26
	1	7, 1	0				
	2	9, 3	0				
	3	1, 0	0				
	4	5, 4	0				
	:						
	133	1, 0	26				
	134	5, 4	26				

Note:
1. n = 10 for 480-line systems, n = 12 for 576-line systems.

Table 6.28. Video DIF Blocks and Compressed Macroblocks for 25 Mbps.

efficient to divide the MPEG packets into smaller components of 24 bytes each to maximize available bandwidth. The transmitter then uses an integer number of data blocks (restricted multiples of 0, 1, 2, 4, or 8) placing them in an isochronous packet and adding the 8-byte CIP header.

50 Mbps DV

Like the 25 Mbps DV format, the 50 Mbps DV format supports 720 × 480i30 and 720 × 576i25 sources. However, the 50 Mbps DV format uses 4:2:2 YCbCr rather than 4:1:1 YCbCr.

As previously discussed, the source packet size for the 25 Mbps DV streams is 480 bytes (consisting of 6 DIF blocks). The 250 packets (300 packets for 576i25 systems) of 480-byte data are transferred over a 25 Mbps channel.

The source packet size for the 50 Mbps DV streams is 960 bytes (consisting of 12 DIF blocks). The first 125 packets (150 packets for 576i25 systems) of 960-byte data are sent over one 25 Mbps channel and the next 125 packets (150 packets for 576i25 systems) of 960-byte data are sent over a second 25 Mbps channel.

100 Mbps DV

100 Mbps DV streams support 1920 × 1080i30, 1920 × 1080i25, and 1280 × 720p60 sources. 1920 × 1080i30 sources are horizontally scaled to 1280 × 1080i30. 1920 × 1080i25 sources are horizontally scaled to 1440 × 1080i25. 1280 × 720p60 sources are horizontally scaled to 960 × 720p60. The 4:2:2 YCbCr format is used.

The source packet size for the 100 Mbps DV streams is 1920 bytes (consisting of 24 DIF blocks). The first 63 packets (75 packets for 1080i25 systems) of 1920-byte data are sent over one 25 Mbps channel, the next 62 packets (75 packets for 1080i25 systems) of 1920-byte data are sent over a second 25 Mbps channel, the next 63 packets (75 packets for 1080i25 systems) of 1920-byte data are sent over a third 25 Mbps channel, and the last 62 packets (75 packets for 1080i25 systems) of 1920-byte data are sent over a fourth 25 Mbps channel.

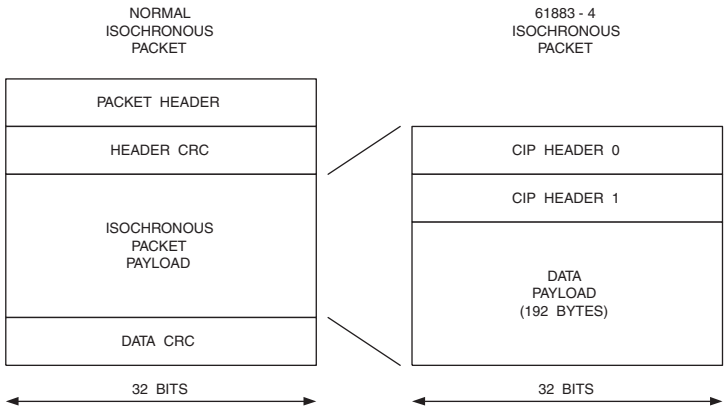


Figure 6.61. 61883-4 Isochronous Packet Formatting.

Digital Camera Specification

The 1394 Trade Association has written a specification for 1394-based digital video cameras. This was done to avoid the silicon and software cost of implementing the full IEC 61883 specification.

Seven resolutions are defined, with a wide range of format support:

160 × 120	4:4:4 YCbCr
320 × 240	4:2:2 YCbCr
640 × 480	4:1:1, 4:2:2 YCbCr, 24-bit RGB
800 × 600	4:2:2 YCbCr, 24-bit RGB
1024 × 768	4:2:2 YCbCr, 24-bit RGB
1280 × 960	4:2:2 YCbCr, 24-bit RGB
1600 × 1200	4:2:2 YCbCr, 24-bit RGB

Supported frame rates are 1.875, 3.75, 7.5, 15, 30, and 60 frames per second.

Isochronous packets are used to transfer the uncompressed digital video data over the 1394 network.

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