Chapter 5

Analog Video Interfaces

For years, the primary video signal used by the consumer market has been composite NTSC or PAL video (see Figures 8.2 and 8.13). Attempts have been made to support S-video, but, until recently, it has been largely limited to S-VHS VCRs and high-end televisions.

With the introduction of DVD players, digital set-top boxes, and DTV, there has been renewed interest in providing high-quality video to the consumer market. This equipment not only supports very high-quality composite and S-video signals, but many devices also allow the option of using analog R′G′B′ or YPbPr video.

Using analog R′G′B′ or YPbPr video eliminates NTSC/PAL encoding and decoding artifacts. As a result, the picture is sharper and has less noise. More color bandwidth is also available, increasing the horizontal detail.

S-Video Interface

The RCA phono connector (consumer market) or BNC connector (pro-video market) transfers a composite NTSC or PAL video signal, made by adding the intensity (Y) and color (C) video signals together. The television then has to separate these Y and C video signals in order to display the picture. The problem is that the Y/C separation process is never perfect, as discussed in Chapter 9.

Many video components now support a 4-pin “S1” S-video connector, illustrated in Figure 5.1 (the female connector viewpoint). This connector keeps the intensity (Y) and color (C) video signals separate, eliminating the Y/C separation process in the TV. As a result, the picture is sharper and has less noise. Figures 9.2 and 9.3 illustrate the Y signal, and Figures 9.10 and 9.11 illustrate the C signal.

NTSC and PAL VBI (vertical blanking interval) data, discussed in Chapter 8, may be present on the 480i or 576i Y video signal.

The "S2" version adds a +5V DC offset to the C signal when a widescreen (16:9) anamorphic program (horizontally squeezed by 25%) is present. A 16:9 TV detects the DC offset and horizontally expands the 4:3 image to fill the screen, restoring the correct aspect ratio of the program. The "S3" version also supports using a +2.3V offset when a program is letterboxed.

The IEC 60933-5 standard specifies the S-video connector, including signal levels.

Extended S-Video Interface

The PC market also uses an extended S-Video interface. This interface has 7 pins, as shown in Figure 5.1, and is backwards compatible with the 4-pin interface.

The use of the three additional pins varies by manufacturer. They may be used to support an I^2C interface (SDA bi-directional data pin and SCL clock pin), +12V power, a composite NTSC/PAL video signal (CVBS), or analog R′G′B′ or YPbPr video signals.

SCART Interface

Most consumer video components in Europe support one or two 21-pin SCART connectors (also known as Peritel, Peritelevision, and Euroconnector). This connection allows analog R′G′B′ video or S-video, composite video, and analog stereo audio to be transmitted between equipment using a single cable. The composite video signal must always be present, as it provides the basic video timing for the analog R′G′B′ video signals. Note that the 700 mV R′G′B′ signals do not have a blanking pedestal or sync information, as illustrated in Figure 5.4.

PAL VBI (vertical blanking interval) data, discussed in Chapter 8, may be present on the 576i composite video signal.

There are now several types of SCART pinouts, depending on the specific functions implemented, as shown in Tables 5.1 through 5.3. Pinout details are shown in Figure 5.2.

The CENELEC EN 50049–1 and IEC 60933 standards specify the basic SCART connector, including signal levels.

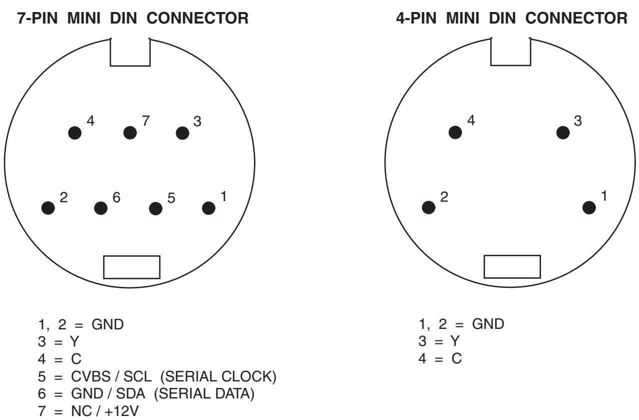

Figure 5.1. S-Video Connector and Signal Names.

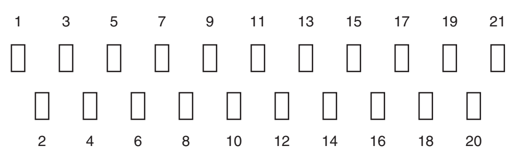

Figure 5.2. SCART Connector.

Pin	Function	Signal Level	Impedance
1	right audio out	0.5V rms	< 1K ohm
2	right audio in	0.5V rms	> 10K ohm
3	left / mono audio out	0.5V rms	< 1K ohm
4	ground - for pins 1, 2, 3, 6		
5	ground - for pin 7		
6	left / mono audio in	0.5V rms	> 10K ohm
7	blue (or C) video in / out	0.7V (or 0.3V burst)	75 ohms
8	status and aspect ratio in / out	9.5V–12V = 4:3 source 4.5V–7V = 16:9 source 0V–2V = inactive source	> 10K ohm
9	ground - for pin 11		
10	data 2		
11	green video in / out	0.7V	75 ohms
12	data 1		
13	ground - for pin 15		
14	ground - for pin 16		
15	red (or C) video in / out	0.7V (or 0.3V burst)	75 ohms
16	RGB control in / out	1–3V = RGB, 0–0.4V = composite	75 ohms
17	ground - for pin 19		
18	ground - for pin 20		
19	composite (or Y) video out	1V	75 ohms
20	composite (or Y) video in	1V	75 ohms
21	ground - for pins 8, 10, 12, shield		

Note:

Often, the SCART 1 connector supports composite video and RGB, the SCART 2 connector supports composite video and S-Video, and the SCART 3 connector supports only composite video. SCART connections may also be used to add external decoders or descramblers to the video path, the video signal goes out and comes back in.

The RGB control signal controls the TV switch between the composite and RGB inputs, enabling the overlaying of text onto the video, even the internal TV program. This enables an external teletext or closed captioning decoder to add information over the current program. If pin 16 is held high, signifying RGB signals are present, the sync is still carried on the Composite Video pin. Some devices (such as DVD players) may provide RGB on a SCART and hold pin 16 permanently high.

When a source becomes active, it sets a 12V level on pin 8. This causes the TV to automatically switch to that SCART input. When the source stops, the signal returns to 0V and TV viewing is resumed. If an anamorphic 16:9 program is present, the source raises the signal on pin 8 to only 6V. This causes the TV to switch to that SCART input and at the same time enable the video processing for anamorphic 16:9 programs.

Table 5.1. SCART Connector Signals.

SDTV RGB Interface

Some SDTV consumer video equipment supports an analog R′G′B′ video interface. NTSC and PAL VBI (vertical blanking interval) data, discussed in Chapter 8, may be present on 480i or 576i R′G′B′ video signals. Three separate RCA phono connectors (consumer market) or BNC connectors (pro-video and PC market) are used.

The horizontal and vertical video timing are dependent on the video standard, as discussed in Chapter 4. For sources, the video signal at the connector should have a source impedance of 75Ω ±5%. For receivers, video inputs should be AC-coupled and have a 75-Ω ±5% input impedance. The three signals must be coincident with respect to each other within ±5 ns.

Sync information may be present on just the green channel, all three channels, as a separate composite sync signal, or as separate horizontal and vertical sync signals. A gamma of 1/0.45 is used.

7.5 IRE Blanking Pedestal

As shown in Figure 5.3, the nominal active video amplitude is 714 mV, including a 7.5 ±2 IRE blanking pedestal. A 286 ±6 mV composite sync signal may be present on just the green channel (consumer market), or all three channels (pro-video market). DC offsets up to ±1V may be present.

Analog R′G′B′ Generation

Assuming 10-bit D/A converters (DACs) with an output range of 0–1.305V (to match the video DACs used by the NTSC/PAL encoder in Chapter 9), the 10-bit YCbCr to R′G′B′ equations are:

$$R' = 0.591(Y - 64) + 0.810(Cr - 512)$$

$$G' = 0.591(Y - 64) - 0.413(Cr - 512) - 0.199(Cb - 512)$$

$$B' = 0.591(Y - 64) + 1.025(Cb - 512)$$

R′G′B′ has a nominal 10-bit range of 0–518 to match the active video levels used by the NTSC/PAL encoder in Chapter 9. Note that negative values of R′G′B′ should be supported at this point.

To implement the 7.5 IRE blanking pedestal, a value of 42 is added to the digital R′G′B′ data during active video. 0 is added during the blanking time.

After the blanking pedestal is added, the R′G′B′ data is clamped by a blanking signal that has a raised cosine distribution to slow the slew rate of the start and end of the video signal. For 480i and 576i systems, blank rise and fall times are 140 ±20 ns. For 480p and 576p systems, blank rise and fall times are 70 ±10 ns.

Composite sync information may be added to the R′G′B′ data after the blank processing has been performed. Values of 16 (sync present) or 240 (no sync) are assigned. The sync rise and fall times should be processed to generate a raised cosine distribution (between 16 and 240) to slow the slew rate of the sync signal. For 480i and 576i systems, sync rise and fall times are 140 ±20 ns, and horizontal sync width at the 50% point is 4.7 ±0.1 µs. For 480p and 576p systems, sync rise and fall times are 70 ±10 ns, and horizontal sync width at the 50% point is 2.33 ±0.05 µs.

At this point, we have digital R′G′B′ with sync and blanking information, as shown in Figure 5.3 and Table 5.2. The numbers in parentheses in Figure 5.3 indicate the data value for a 10-bit DAC with a full-scale output value of 1.305V. The digital R′G′B′ data drives

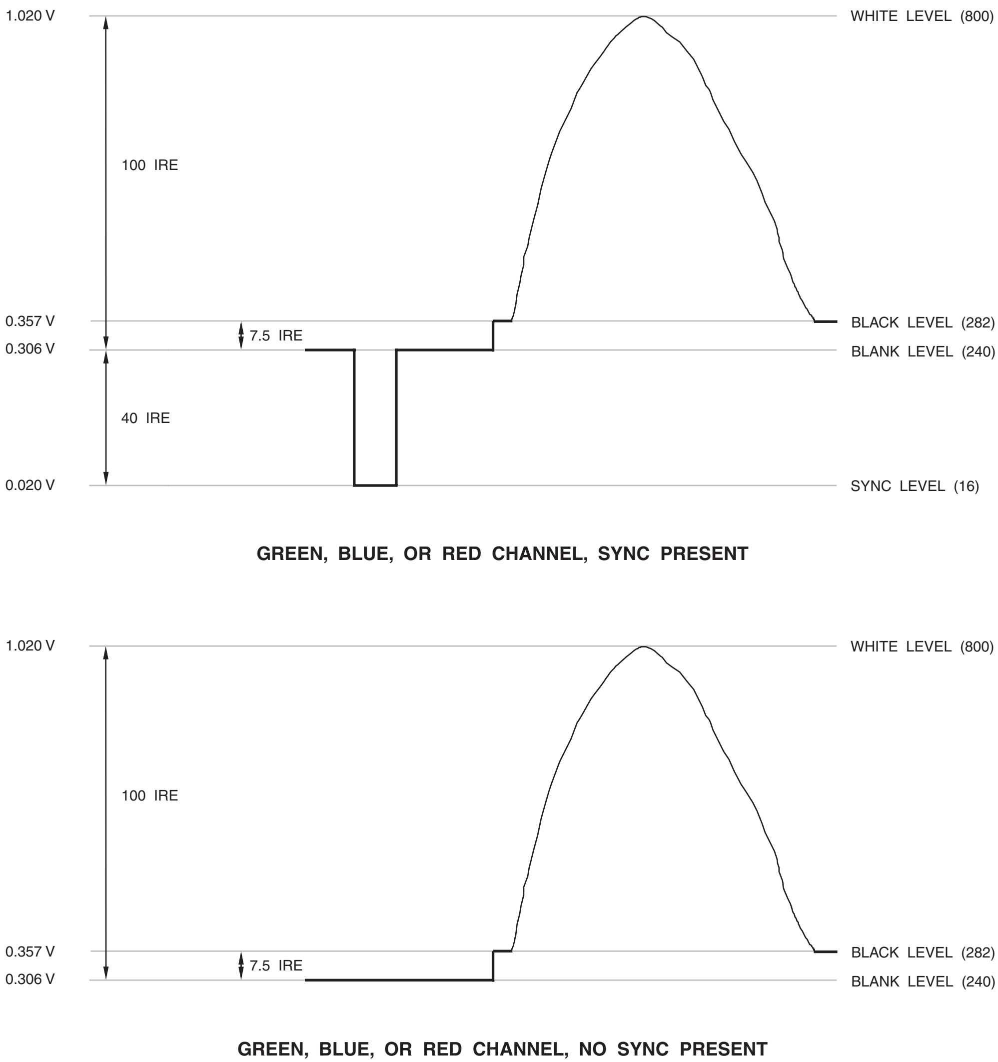

Figure 5.3. SDTV Analog RGB Levels. 7.5 IRE blanking level.

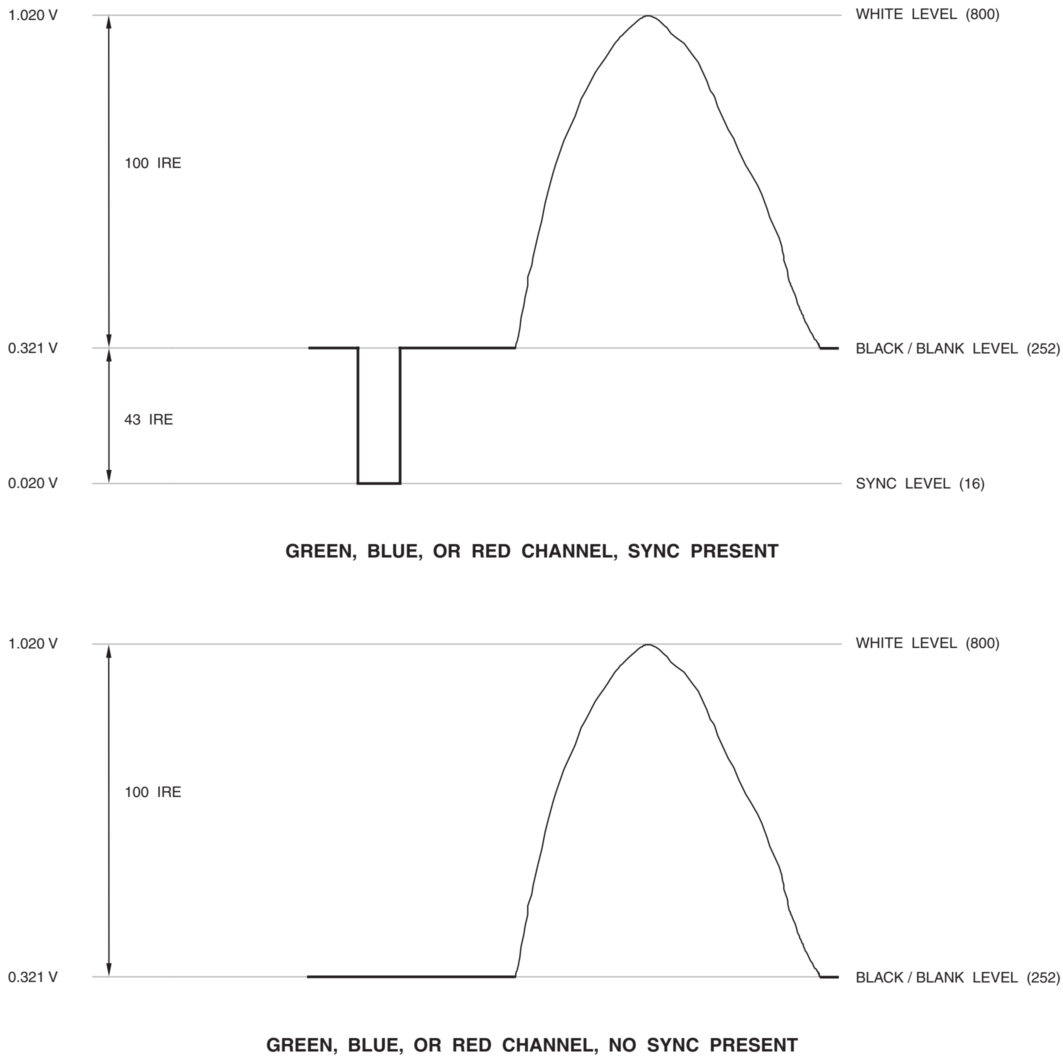

Figure 5.4. SDTV Analog RGB Levels. 0 IRE blanking level.

three 10-bit DACs to generate the analog R´G´B´ video signals.

As the sample-and-hold action of the DAC introduces a $(\sin x)/x$ characteristic, the video data may be digitally filtered by a $[(\sin x)/x]^{-1}$ filter to compensate. Alternately, as an analog lowpass filter is usually present after each DAC, the correction may take place in the analog filter.

Video Level	7.5 IRE Blanking Pedestal	0 IRE Blanking Pedestal
white	800	800
black	282	252
blank	240	252
sync	16	16

Table 5.2. SDTV 10-Bit R´G´B´ Values.

Analog R´G´B´ Digitization

Assuming 10-bit A/D converters (ADCs) with an input range of 0–1.305V (to match the video ADCs used by the NTSC/PAL decoder in Chapter 9), the 10-bit R´G´B´ to YCbCr equations are:

$$Y = 0.506(R' - 282) + 0.992(G' - 282) + 0.193(B' - 282) + 64$$

$$Cb = -0.291(R' - 282) - 0.573(G' - 282) + 0.864(B' - 282) + 512$$

$$Cr = 0.864(R' - 282) - 0.724(G' - 282) - 0.140(B' - 282) + 512$$

R´G´B´ has a nominal 10-bit range of 282–800 to match the active video levels used by the NTSC/PAL decoder in Chapter 9. Table 5.2 and Figure 5.3 illustrate the 10-bit R´G´B´ values for the white, black, blank, and (optional) sync levels.

0 IRE Blanking Pedestal

As shown in Figure 5.4, the nominal active video amplitude is 700 mV, with no blanking pedestal. A 300 ±6 mV composite sync signal may be present on just the green channel (consumer market), or all three channels (pro-video market). DC offsets up to ±1V may be present.

Analog R´G´B´ Generation

Assuming 10-bit DACs with an output range of 0–1.305V (to match the video DACs used by the NTSC/PAL encoder in Chapter 9), the 10-bit YCbCr to R´G´B´ equations are:

$$R' = 0.625(Y - 64) + 0.857(Cr - 512)$$

$$G' = 0.625(Y - 64) - 0.437(Cr - 512) - 0.210(Cb - 512)$$

$$B' = 0.625(Y - 64) + 1.084(Cb - 512)$$

R´G´B´ has a nominal 10-bit range of 0–548 to match the active video levels used by the NTSC/PAL encoder in Chapter 9. Note that negative values of R´G´B´ should be supported at this point.

The R´G´B´ data is processed as discussed when using a 7.5 IRE blanking pedestal. However, no blanking pedestal is added during active video, and the sync values are 16–252 instead of 16–240.

At this point, we have digital R´G´B´ with sync and blanking information, as shown in Figure 5.4 and Table 5.2. The numbers in parentheses in Figure 5.4 indicate the data value for a 10-bit DAC with a full-scale output value of 1.305V. The digital R´G´B´ data drives three 10-bit DACs to generate the analog R´G´B´ video signals.

Analog R′G′B′ Digitization

Assuming 10-bit ADCs with an input range of 0–1.305V (to match the video ADCs used by the NTSC/PAL decoder in Chapter 9), the 10-bit R′G′B′ to YCbCr equations are:

$$Y = 0.478(R' - 252) + 0.938(G' - 252) + 0.182(B' - 252) + 64$$

$$Cb = -0.275(R' - 252) - 0.542(G' - 252) + 0.817(B' - 252) + 512$$

$$Cr = 0.817(R' - 252) - 0.685(G' - 252) - 0.132(B' - 252) + 512$$

R′G′B′ has a nominal 10-bit range of 252–800 to match the active video levels used by the NTSC/PAL decoder in Chapter 9. Table 5.2 and Figure 5.4 illustrate the 10-bit R′G′B′ values for the white, black, blank, and (optional) sync levels.

HDTV RGB Interface

Some HDTV consumer video equipment supports an analog R′G′B′ video interface. Three separate RCA phono connectors (consumer market) or BNC connectors (pro-video and PC market) are used.

The horizontal and vertical video timing are dependent on the video standard, as discussed in Chapter 4. For sources, the video signal at the connector should have a source impedance of 75Ω ±5%. For receivers, video inputs should be AC-coupled and have a 75-Ω ±5% input impedance. The three signals must be coincident with respect to each other within ±5 ns.

Sync information may be present on just the green channel, all three channels, as a separate composite sync signal, or as separate horizontal and vertical sync signals. A gamma of 1/0.45 is used.

As shown in Figure 5.5, the nominal active video amplitude is 700 mV, and has no blanking pedestal. A ±300 ±6 mV tri-level composite sync signal may be present on just the green channel (consumer market), or all three channels (pro-video market). DC offsets up to ±1V may be present.

Analog R′G′B′ Generation

Assuming 10-bit DACs with an output range of 0–1.305V (to match the video DACs used by the NTSC/PAL encoder in Chapter 9), the 10-bit YCbCr to R′G′B′ equations are:

$$R' = 0.625(Y - 64) + 0.963(Cr - 512)$$

$$G' = 0.625(Y - 64) - 0.287(Cr - 512) - 0.114(Cb - 512)$$

$$B' = 0.625(Y - 64) + 1.136(Cb - 512)$$

R′G′B′ has a nominal 10-bit range of 0–548 to match the active video levels used by the NTSC/PAL encoder in Chapter 9. Note that negative values of R′G′B′ should be supported at this point.

The R′G′B′ data is clamped by a blanking signal that has a raised cosine distribution to slow the slew rate of the start and end of the video signal. For 1080i and 720p systems, blank rise and fall times are 54 ±20 ns. For 1080p systems, blank rise and fall times are 27 ±10 ns.

Composite sync information may be added to the R′G′B′ data after the blank processing has been performed. Values of 16 (sync low), 488 (high sync), or 252 (no sync) are assigned. The sync rise and fall times should be processed to generate a raised cosine distribution to slow the slew rate of the sync signal. For 1080i systems, sync rise and fall times are 54 ±20 ns, and the horizontal sync low and high widths at the 50% points are 593 ±40 ns. For

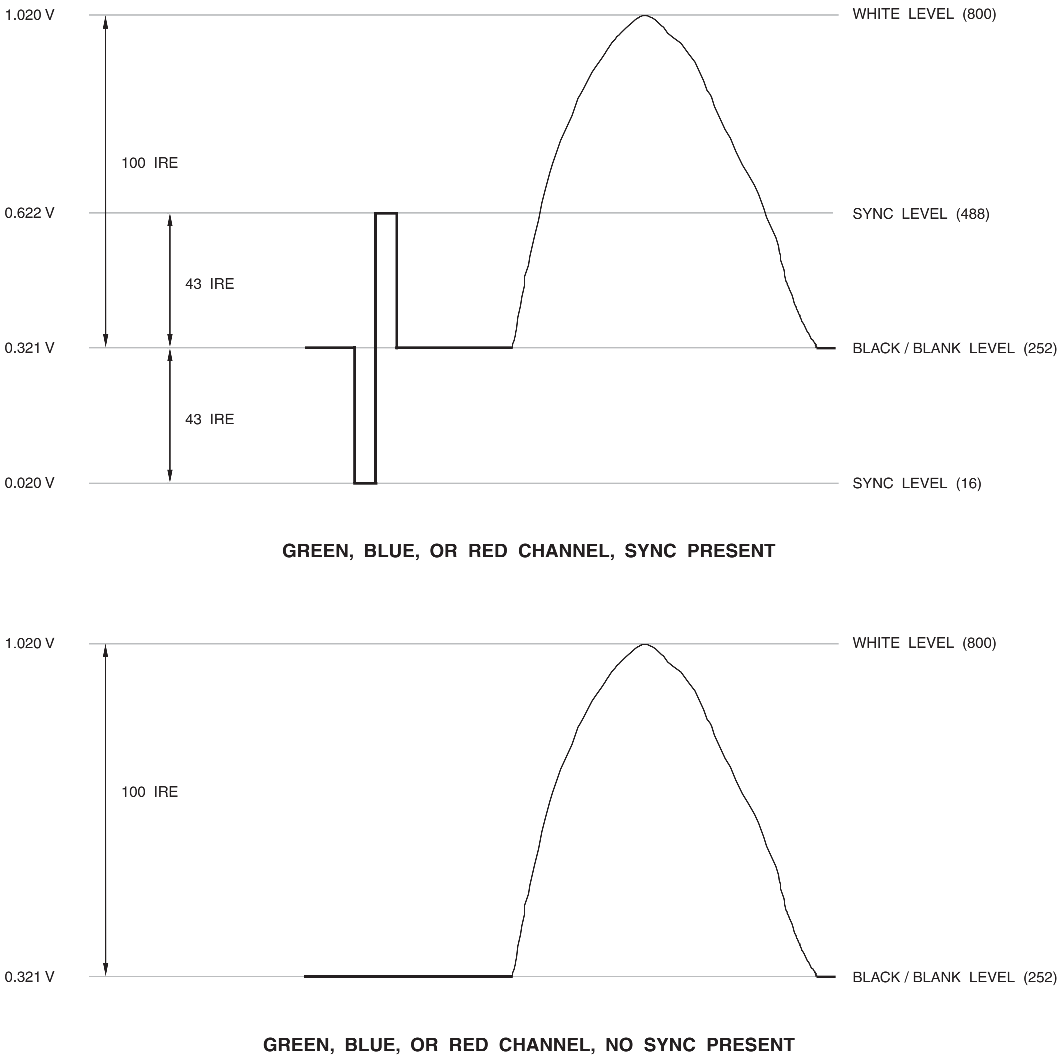

Figure 5.5. HDTV Analog RGB Levels. 0 IRE blanking level.

720p systems, sync rise and fall times are 54 ±20 ns, and the horizontal sync low and high widths at the 50% points are 539 ±40 ns. For 1080p systems, sync rise and fall times are 27 ±10 ns, and the horizontal sync low and high widths at the 50% points are 296 ±20 ns.

At this point, we have digital R′G′B′ with sync and blanking information, as shown in Figure 5.5 and Table 5.3. The numbers in parentheses in Figure 5.5 indicate the data value for a 10-bit DAC with a full-scale output value of 1.305V. The digital R′G′B′ data drive three 10-bit DACs to generate the analog R′G′B′ video signals.

Video Level	0 IRE Blanking Pedestal
white	800
sync high	488
black	252
blank	252
sync low	16

Table 5.3. HDTV 10-Bit R′G′B′ Values.

Analog R′G′B′ Digitization

Assuming 10-bit ADCs with an input range of 0–1.305V (to match the video ADCs used by the NTSC/PAL decoder in Chapter 9), the 10-bit R′G′B′ to YCbCr equations are:

$$Y = 0.341(R' - 252) + 1.143(G' - 252) + 0.115(B' - 252) + 64$$

$$Cb = -0.188(R' - 252) - 0.629(G' - 252) + 0.817(B' - 252) + 512$$

$$Cr = 0.817(R' - 252) - 0.743(G' - 252) - 0.074(B' - 252) + 512$$

R′G′B′ has a nominal 10-bit range of 252–800 to match the active video levels used by the NTSC/PAL decoder in Chapter 9. Table 5.3 and Figure 5.5 illustrate the 10-bit R′G′B′ values for the white, black, blank, and (optional) sync levels.

Constrained Image

Due to the limited availability of copy protection technology for high-definition analog interfaces, some standards and DRM implementations only allow a *constrained image* to be output. A constrained image has an effective maximum resolution of 960 × 540p, although the total number of video samples and the video timing remain unchanged (for example, 1280 × 720p or 1920 × 1080i).

In these situations, the full resolution image is still available via an approved secure digital video output, such as HDMI.

SDTV YPbPr Interface

Some SDTV consumer video equipment supports an analog YPbPr video interface. NTSC and PAL VBI (vertical blanking interval) data, discussed in Chapter 8, may be present on 480i or 576i Y video signals. Three separate RCA phono connectors (consumer market) or BNC connectors (pro-video market) are used.

The horizontal and vertical video timing are dependent on the video standard, as discussed in Chapter 4. For sources, the video signal at the connector should have a source impedance of 75Ω ±5%. For receivers, video inputs should be AC-coupled and have a 75-Ω ±5% input impedance. The three signals must be coincident with respect to each other within ±5 ns.

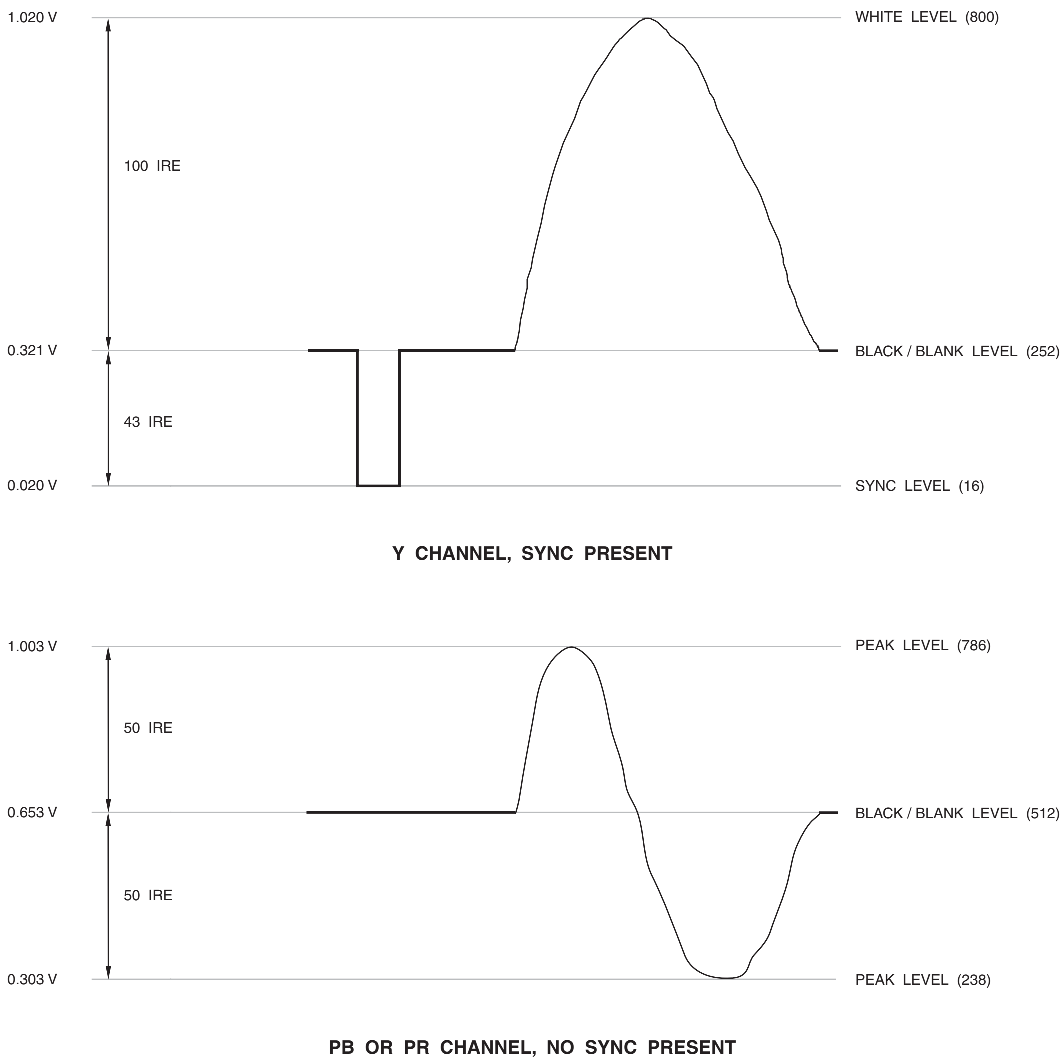

Figure 5.6. EIA-770.2 SDTV Analog YPbPr Levels. Sync on Y.

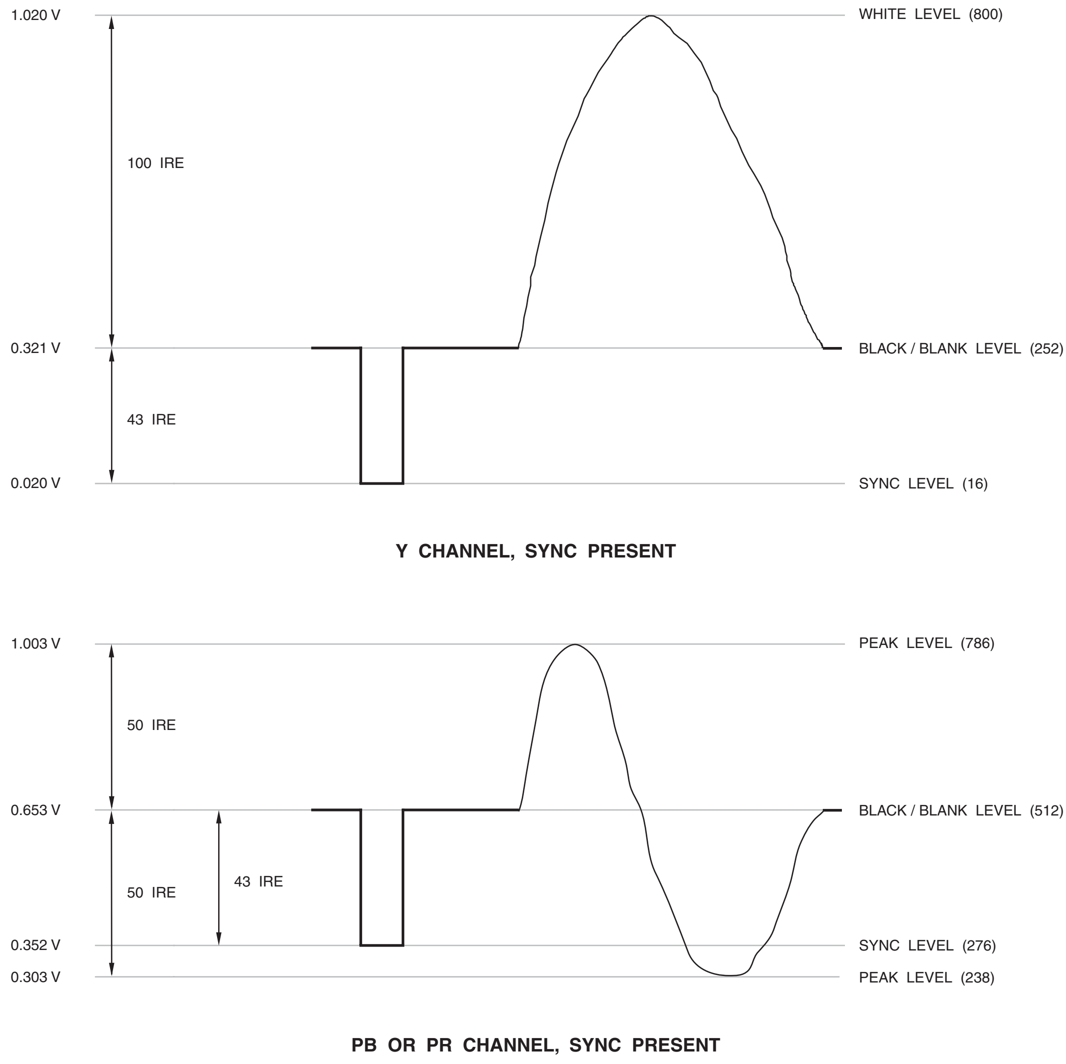

Figure 5.7. SDTV Analog YPbPr Levels. Sync on YPbPr.

		White	Yellow	Cyan	Green	Magenta	Red	Blue	Black
Y	IRE	100	88.6	70.1	58.7	41.3	29.9	11.4	0
	mV	700	620	491	411	289	209	80	0
Pb	IRE	0	–50	16.8	–33.1	33.1	–16.8	50	0
	mV	0	–350	118	–232	232	–118	350	0
Pr	IRE	0	8.1	–50	–41.8	41.8	50	–8.1	0
	mV	0	57	–350	–293	293	350	–57	0
Y	64 to 940	940	840	678	578	426	326	164	64
Cb	64 to 960	512	64	663	215	809	361	960	512
Cr	64 to 960	512	585	64	137	887	960	439	512

Table 5.4. EIA-770.2 SDTV YPbPr and YCbCr 100% Color Bars. YPbPr values relative to the blanking level.

		White	Yellow	Cyan	Green	Magenta	Red	Blue	Black
Y	IRE	75	66.5	52.6	44	31	22.4	8.6	0
	mV	525	465	368	308	217	157	60	0
Pb	IRE	0	–37.5	12.6	–24.9	24.9	–12.6	37.5	0
	mV	0	–262	88	–174	174	–88	262	0
Pr	IRE	0	6.1	–37.5	–31.4	31.4	37.5	–6.1	0
	mV	0	43	–262	–220	220	262	–43	0
Y	64 to 940	721	646	525	450	335	260	139	64
Cb	64 to 960	512	176	625	289	735	399	848	512
Cr	64 to 960	512	567	176	231	793	848	457	512

Table 5.5. EIA-770.2 SDTV YPbPr and YCbCr 75% Color Bars. YPbPr values relative to the blanking level.

For consumer products, composite sync is present on only the Y channel. For pro-video applications, composite sync is present on all three channels. A gamma of 1/0.45 is specified.

As shown in Figures 5.6 and 5.7, the Y signal consists of 700 mV of active video (with no blanking pedestal). Pb and Pr have a peak-to-peak amplitude of 700 mV. A 300 ±6 mV composite sync signal is present on just the Y channel (consumer market), or all three channels (pro-video market). DC offsets up to ±1V may be present. The 100% and 75% YPbPr color bar values are shown in Tables 5.4 and 5.5.

Analog YPbPr Generation

Assuming 10-bit DACs with an output range of 0–1.305V (to match the video DACs used by the NTSC/PAL encoder in Chapter 9), the 10-bit YCbCr to YPbPr equations are:

$$Y = ((800 - 252)/(940 - 64))(Y - 64)$$

$$Pb = ((800 - 252)/(960 - 64))(Cb - 512)$$

$$Pr = ((800 - 252)/(960 - 64))(Cr - 512)$$

Y has a nominal 10-bit range of 0–548 to match the active video levels used by the NTSC/PAL encoder in Chapter 9. Pb and Pr have a nominal 10-bit range of 0 to ±274. Note that negative values of Y should be supported at this point.

The YPbPr data is clamped by a blanking signal that has a raised cosine distribution to slow the slew rate of the start and end of the video signal. For 480i and 576i systems, blank rise and fall times are 140 ±20 ns. For 480p and 576p systems, blank rise and fall times are 70 ±10 ns.

Composite sync information is added to the Y data after the blank processing has been performed. Values of 16 (sync present) or 252 (no sync) are assigned. The sync rise and fall times should be processed to generate a raised cosine distribution (between 16 and 252) to slow the slew rate of the sync signal.

Composite sync information may also be added to the PbPr data after the blank processing has been performed. Values of 276 (sync present) or 512 (no sync) are assigned. The sync rise and fall times should be processed to generate a raised cosine distribution (between 276 and 512) to slow the slew rate of the sync signal.

For 480i and 576i systems, sync rise and fall times are 140 ±20 ns, and horizontal sync width at the 50% point is 4.7 ±0.1 μs. For 480p and 576p systems, sync rise and fall times are 70 ±10 ns, and horizontal sync width at the 50% point is 2.33 ±0.05 μs.

At this point, we have digital YPbPr with sync and blanking information, as shown in Figures 5.6 and 5.7 and Table 5.6. The numbers in parentheses in Figures 5.6 and 5.7 indicate the data value for a 10-bit DAC with a full-scale output value of 1.305V. The digital YPbPr data drive three 10-bit DACs to generate the analog YPbPr video signals.

Video Level	Y	PbPr
white	800	512
black	252	512
blank	252	512
sync	16	276

Table 5.6. SDTV 10-Bit YPbPr Values.

Analog YPbPr Digitization

Assuming 10-bit ADCs with an input range of 0–1.305V (to match the video ADCs used by the NTSC/PAL decoder in Chapter 9), the 10-bit YPbPr to YCbCr equations are:

$$Y = 1.5985(Y - 252) + 64$$

$$Cb = 1.635(Pb - 512) + 512$$

$$Cr = 1.635(Pr - 512) + 512$$

Y has a nominal 10-bit range of 252–800 to match the active video levels used by the NTSC/PAL decoder in Chapter 9. Table 5.6 and Figures 5.6 and 5.7 illustrate the 10-bit YPbPr values for the white, black, blank, and (optional) sync levels.

VBI Data for 480p Systems

CGMS Type A

CEA-805, IEC 61880–2, and EIA-J CPR–1204–1 define the format of CGMS (Copy Generation Management System) data on line 41 for 480p systems. The waveform is illustrated in Figure 5.8.

A sample clock rate of 27 MHz (59.94 Hz frame rate) or 27.027 MHz (60 Hz frame rate) is used. Each data bit is 26 clock cycles, or 963 ±30 ns, wide with a maximum rise and fall time of 50 ns. A logical “1” has an amplitude of 70 ±10 IRE; a logical “0” has an amplitude of 0 ±5 IRE.

The 2-bit start symbol begins 156 clock cycles, or about 5.778 µs, after 0_H. It consists of a “1” followed by a “0.”

The 6-bit header follows the start symbol, and defines the nature of the payload data as shown in Table 5.7. The End of Message immediately follows the last packet of any data service that uses more than one packet. It has an associated payload consisting of all zeros. ECCI is a data service that may use more than one packet, thus requiring the use of the End of Message.

The 14-bit payload for CGMS data is shown in Table 5.8. The 14-bit payload for ECCI data is currently “reserved,” consisting of all ones.

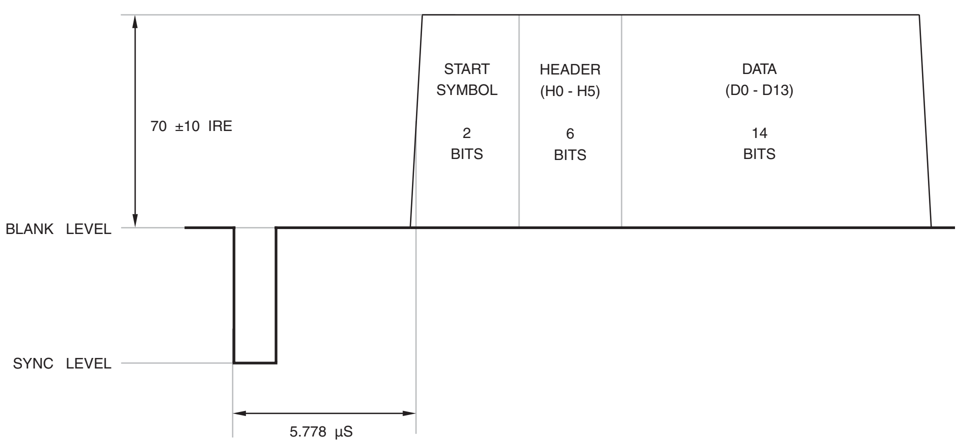

Figure 5.8. CEA-805, IEC 61880–2, and EIA-J CPR–1204–1 Line 41 Timing.

H0	H1	Aspect Ratio	Picture Display Format
0	0	4:3	normal
0	1	4:3	letter box
1	0	16:9	normal
1	1	CEA-805 Type A packet	

H2	H3	H4	H5	Service Name
0	0	0	0	CGMS (see Table 5.8)
0	0	0	1	Extended Copy Control Information (ECCI)
0	0	1	0	reserved
:				
1	1	1	0	
1	1	1	1	End of Message (default if no copyright information)

Table 5.7. CEA-805, IEC 61880–2, and EIA-J CPR–1204–1 Line 41 Header Format. The H2-H5 bits must be "0000" if Type A packet is indicated.

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13
G0	G1	G2	G3	ASB	0	0	0	CRC = $x^6 + x + 1$					

G0–G1: CGMS Definition
- 00 copying permitted
- 01 no more copies (one copy has already been made)
- 10 one copy permitted
- 11 no copying permitted

G2–G3: Analog Protection Service (valid only if both G0–G1 are “01” or “10”)
- 00 no Analog Protection Service
- 01 PSP on, color striping off
- 10 PSP on, 2-line color striping on
- 11 PSP on, 4-line color striping on

ASB: Analog Source Bit
- 0 not analog pre-recorded medium
- 1 analog pre-recorded medium

Table 5.8. CEA-805, IEC 61880–2, and EIA-J CPR–1204–1 Line 41 CGMS Service Format.

CGMS Type B

CEA-805 defines the format of CGMS (Copy Generation Management System) data on line 40 for 480p systems. The waveform is illustrated in Figure 5.9.

A sample clock rate of 27 MHz (59.94 Hz frame rate) or 27.027 MHz (60 Hz frame rate) is used. Each data bit is four clock cycles, or 148 ±18.5 ns, wide with a maximum rise and fall time of 37 ns. A logical “1” has an amplitude of 70 ±10 IRE; a logical “0” has an amplitude of 0 ±5 IRE.

The 2-bit start symbol begins 156 clock cycles, or about 5.778 µs, after 0_H. It consists of a “1” followed by a “0.”

The 6-bit header follows the start symbol, and defines the nature of the payload data as shown in Table 5.9.

The 16-byte payload is shown in Table 5.10.

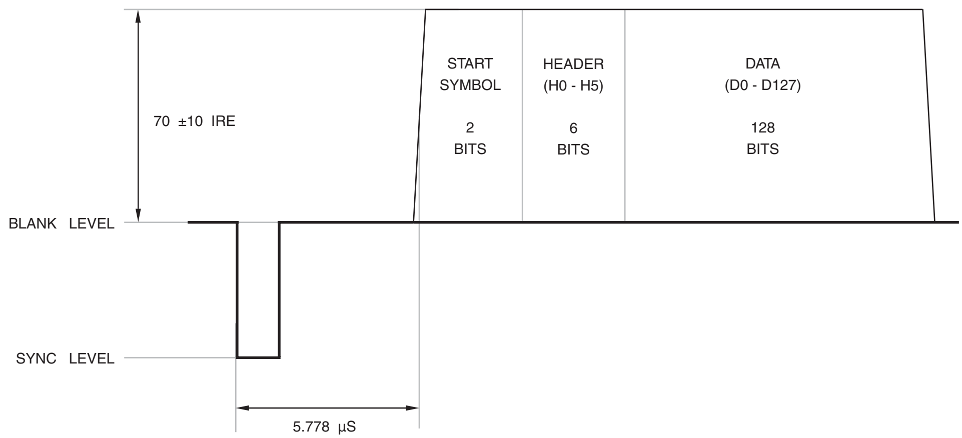

Figure 5.9. CEA-805 Line 40 Timing.

H0	H1	H2	H3	H4	H5	Service Name
0	0	0	0	0	0	reserved for future use
:						
1	1	0	0	0	1	
1	1	0	0	1	0	Type B packet
1	1	0	0	1	0	reserved for future use
:						
1	1	1	1	1	1	

Table 5.9. CEA-805 Line 40 Header Format.

D7	D6	D5	D4	D3	D2	D1	D0
version number = 0000 0001							
length of payload packet = 0001 0000							
AR1	AR0	ASB	A0	1	B0	S1	S0
C3	C2	C1	C0	R3	R2	R1	R0
RCI	1	1	1	G3	G2	G1	G0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
line number of end of top bar (lower 8 bits)							
line number of end of top bar (upper 8 bits)							
line number of start of bottom bar (lower 8 bits)							
line number of start of bottom bar (upper 8 bits)							
pixel number of end of left bar (lower 8 bits)							
pixel number of end of left bar (upper 8 bits)							
pixel number of start of right bar (lower 8 bits)							
pixel number of start of right bar (upper 8 bits)							
1	1	CRC = $x^6 + x + 1$					

AR1–AR0: Intended display aspect ratio
- 00 4:3 normal
- 01 4:3 letterbox
- 10 16:9 normal
- 11 reserved

ASB: Analog Source Bit

A0: Active Format Description (AFD) data flag
- 0 no AFD data (R0–R3)
- 1 AFD data (R0–R3) valid

B0: Bar data (for letterboxing)
- 0 no bar data
- 1 bar data present

S1–S0: Scan data (amount of overscan and underscan is not indicated)
- 00 no data
- 01 overscanned (television)
- 10 underscanned (computer)
- 11 reserved

C3–C0: Colorimetry
- 0000 no data
- 0001 BT.601
- 0010 BT.709
- 0011 reserved
- : :
- 1111 reserved

R0–R3: Active Format Description (AFD) active_format value (refer to Table 13.56)

RCI: Redistribution Control Information (RCI) flag

G0–G1: CGMS Definition (refer to Table 5.8)

G2–G3: Analog Protection Services (refer to Table 5.8)

Table 5.10. CEA-805 Line 40 Payload Format.

VBI Data for 576p Systems

CGMS

IEC 62375 defines the format of CGMS (Copy Generation Management System) and widescreen signaling (WSS) data on line 43 for 576p systems. The waveform is illustrated in Figure 5.10. This standard allows a WSS-enhanced 16:9 TV to display programs in their correct aspect ratio.

Data Timing

CGMS and WSS data is normally on line 43, as shown in Figure 5.10. However, due to video editing, the data may reside on any line between 43–47.

The clock frequency is 10 MHz (±1 kHz). The signal waveform should be a sine-squared pulse, with a half-amplitude duration of 100 ±10 ns. The signal amplitude is 500 mV ±5%.

The NRZ data bits are processed by a bi-phase code modulator, such that one data period equals 6 elements at 10 MHz.

Data Content

The WSS consists of a run-in code, a start code, and 14 bits of data, as shown in Table 5.11.

Run-In

The run-in consists of 29 elements of a specific sequence at 10 MHz, shown in Table 5.11.

Start Code

The start code consists of 24 elements of a specific sequence at 10 MHz, shown in Table 5.11.

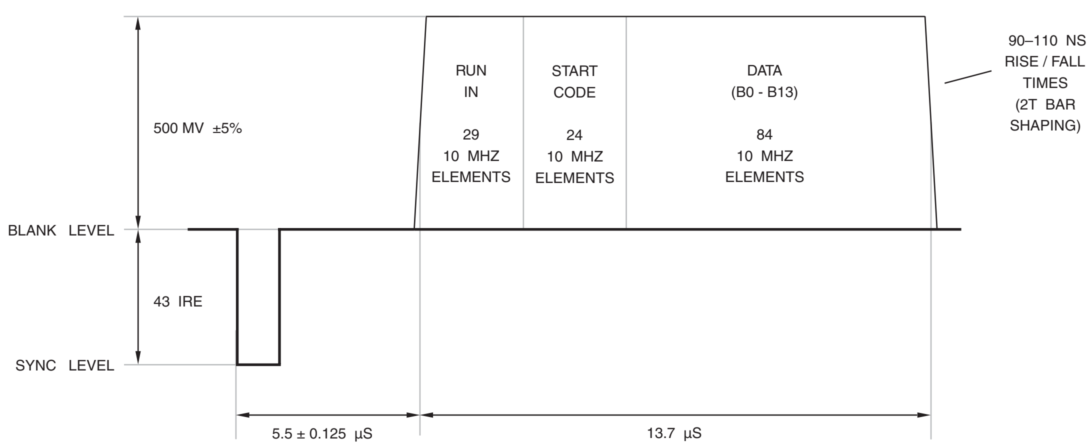

Figure 5.10. IEC 62375 Line 43 CGMS Timing.

Group 1 Data

The group 1 data consists of 4 data bits that specify the aspect ratio. Each data bit generates 6 elements at 10 MHz. b0 is the LSB.

Table 5.11 lists the data bit assignments and usage. The number of active lines listed in Table 5.12 are for the exact aspect ratio (a = 1.33, 1.56, or 1.78).

The aspect ratio label indicates a range of possible aspect ratios (a) and number of active lines:

4:3	$a \le 1.46$	527–576
14:9	$1.46 < a \le 1.66$	463–526
16:9	$1.66 < a \le 1.90$	405–462
>16:9	$a > 1.90$	< 405

To allow automatic selection of the display mode, a 16:9 receiver should support the following minimum requirements:

Case 1: The 4:3 aspect ratio picture should be centered on the display, with black bars on the left and right sides.

Case 2: The 14:9 aspect ratio picture should be centered on the display, with black bars on the left and right sides. Alternately, the picture may be displayed using the full display width by using a small (typically 8%) horizontal geometrical error.

Case 3: The 16:9 aspect ratio picture should be displayed using the full width of the display.

Case 4: The >16:9 aspect ratio picture should be displayed as in Case 3 or use the full height of the display by zooming in.

Group 3 Data

The group 3 data consists of three data bits that specify subtitles. Each data bit generates six elements at 10 MHz. Data bit b8 is the LSB.

b9, b10: open subtitles

00	no
01	outside active picture
10	inside active picture
11	reserved

Group 4 Data

The group 4 data consists of three data bits that specify surround sound and copy protection. Each data bit generates six elements at 10 MHz. Data bit b11 is the LSB.

b11: surround sound

0	no
1	yes

b12: copyright

0	no copyright asserted or unknown
1	copyright asserted

b13: copy protection

0	copying not restricted
1	copying restricted

run-in	29 elements at 10 MHz	1 1111 0001 1100 0111 0001 1100 0111 (0x1F1C71C7)
start code	24 elements at 10 MHz	0001 1110 0011 1100 0001 1111 (0x1E3C1F)
group 1 (aspect ratio)	24 elements at 10 MHz "0" = 000 111 "1" = 111 000	b0, b1, b2, b3
group 2 (enhanced services)	24 elements at 10 MHz "0" = 000 111 "1" = 111 000	b4, b5, b6, b7 (b4, b5, b6 and b7 = "0" since reserved)
group 3 (subtitles)	18 elements at 10 MHz "0" = 000 111 "1" = 111 000	b8, b9, b10 (b8 = "0" since reserved)
group 4 (reserved)	18 elements at 10 MHz "0" = 000 111 "1" = 111 000	b11, b12, b13

Table 5.11. IEC 62375 Line 43 WSS Information.

b0, b1, b2, b3	Aspect Ratio Label	Format	Position On 4:3 Display	Active Lines	Minimum Requirements
0001	4:3	full format	–	576	case 1
1000	14:9	letterbox	center	504	case 2
0100	14:9	letterbox	top	504	case 2
1101	16:9	letterbox	center	430	case 3
0010	16:9	letterbox	top	430	case 3
1011	> 16:9	letterbox	center	–	case 4
0111	14:9	full format	center	576	–
1110	16:9	full format (anamorphic)	–	576	–

Table 5.12. IEC 62375 Group 1 (Aspect Ratio) Data Bit Assignments and Usage.

HDTV YPbPr Interface

Most HDTV consumer video equipment supports an analog YPbPr video interface. Three separate RCA phono connectors (consumer market) or BNC connectors (pro-video market) are used.

The horizontal and vertical video timing is dependent on the video standard, as discussed in Chapter 4. For sources, the video signal at the connector should have a source impedance of 75Ω ±5%. For receivers, video inputs should be AC-coupled and have a 75-Ω ±5% input impedance. The three signals must be coincident with respect to each other within ±5 ns.

For consumer products, composite sync is present on only the Y channel. For pro-video applications, composite sync is present on all three channels. A gamma of 1/0.45 is specified.

As shown in Figures 5.11 and 5.12, the Y signal consists of 700 mV of active video (with no blanking pedestal). Pb and Pr have a peak-to-peak amplitude of 700 mV. A ±300 ±6 mV composite sync signal is present on just the Y channel (consumer market), or all three channels (pro-video market). DC offsets up to ±1V may be present. The 100% and 75% YPbPr color bar values are shown in Tables 5.13 and 5.14.

Analog YPbPr Generation

Assuming 10-bit DACs with an output range of 0–1.305V (to match the video DACs used by the NTSC/PAL encoder in Chapter 9), the 10-bit YCbCr to YPbPr equations are:

$$Y = ((800 - 252)/(940 - 64))(Y - 64)$$

$$Pb = ((800 - 252)/(960 - 64))(Cb - 512)$$

$$Pr = ((800 - 252)/(960 - 64))(Cr - 512)$$

Y has a nominal 10-bit range of 0–548 to match the active video levels used by the NTSC/PAL encoder in Chapter 9. Pb and Pr have a nominal 10-bit range of 0 to ±274. Note that negative values of Y should be supported at this point.

The YPbPr data is clamped by a blanking signal that has a raised cosine distribution to slow the slew rate of the start and end of the video signal. For 1080i and 720p systems, blank rise and fall times are 54 ±20 ns. For 1080p systems, blank rise and fall times are 27 ±10 ns.

Composite sync information is added to the Y data after the blank processing has been performed. Values of 16 (sync low), 488 (high sync), or 252 (no sync) are assigned. The sync rise and fall times should be processed to generate a raised cosine distribution to slow the slew rate of the sync signal.

Composite sync information may be added to the PbPr data after the blank processing has been performed. Values of 276 (sync low), 748 (high sync), or 512 (no sync) are assigned. The sync rise and fall times should be processed to generate a raised cosine distribution to slow the slew rate of the sync signal.

For 1080i systems, sync rise and fall times are 54 ±20 ns, and the horizontal sync low and high widths at the 50% points are 593 ±40 ns. For 720p systems, sync rise and fall times are 54 ±20 ns, and the horizontal sync low and high widths at the 50% points are 539 ±40 ns. For 1080p systems, sync rise and fall times are 27 ±10 ns, and the horizontal sync low and high widths at the 50%-points are 296 ±20 ns.

At this point, we have digital YPbPr with sync and blanking information, as shown in Figures 5.11 and 5.12 and Table 5.15. The numbers in parentheses in Figures 5.11 and 5.12 indicate the data value for a 10-bit DAC with a full-scale output value of 1.305V. The digital

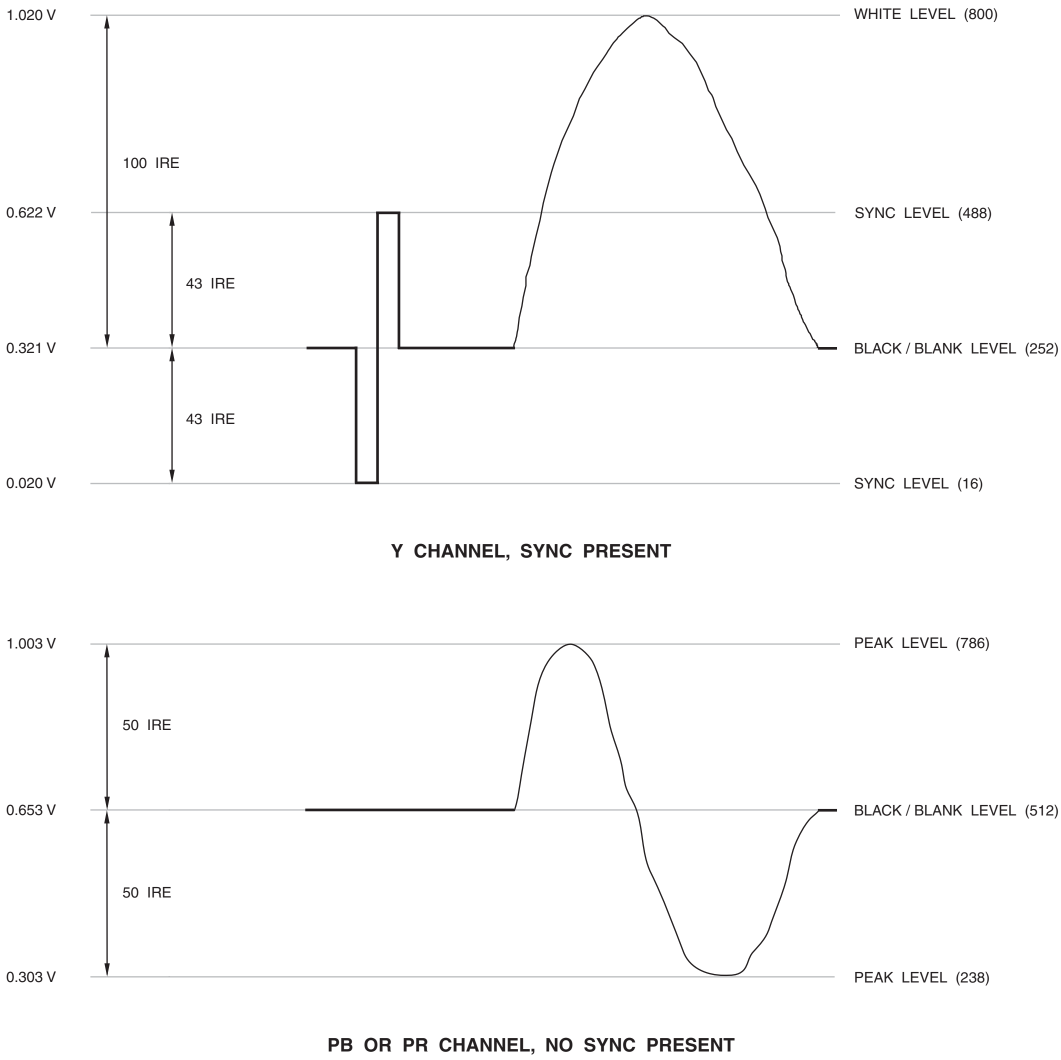

Figure 5.11. EIA-770.3 HDTV Analog YPbPr Levels. Sync on Y.

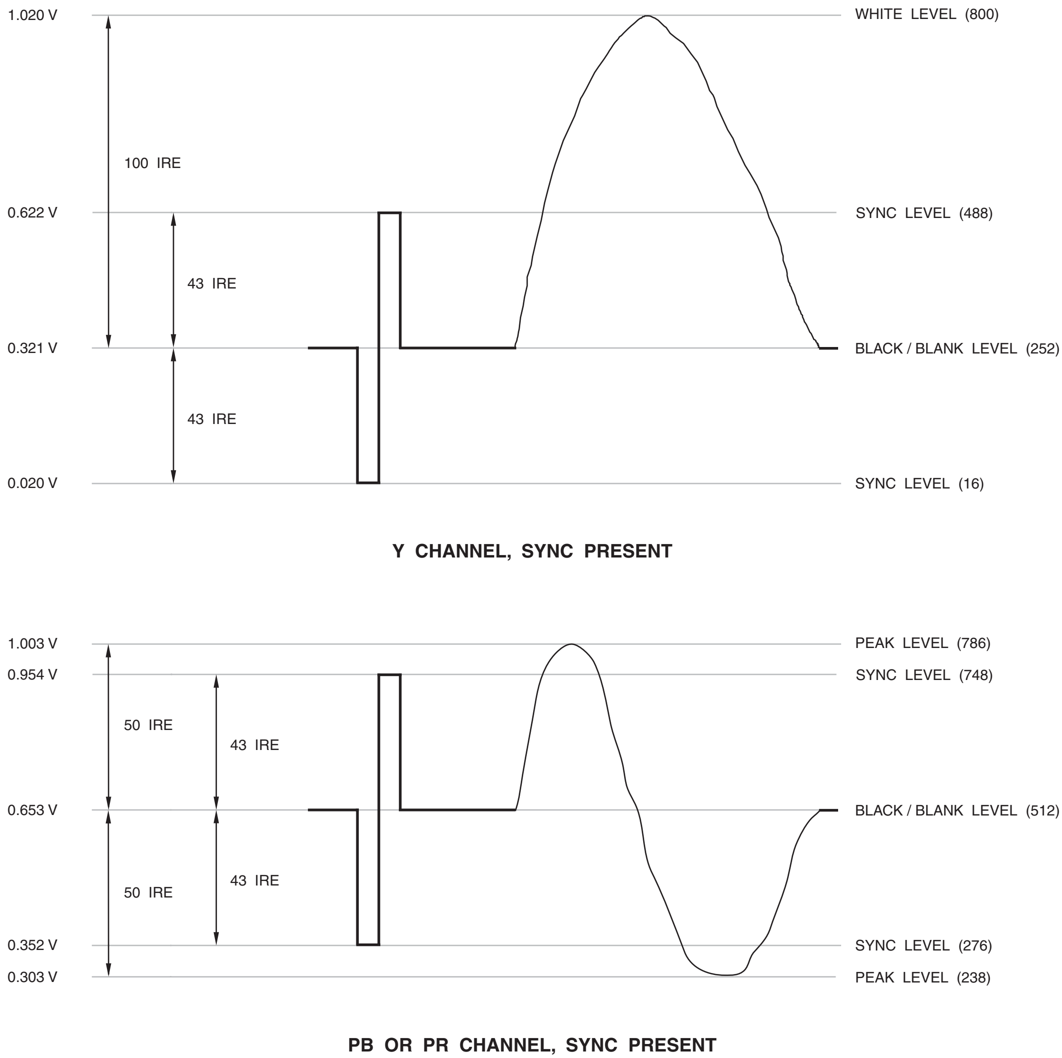

Figure 5.12. SMPTE 274M and 296M HDTV Analog YPbPr Levels. Sync on YPbPr.

		White	Yellow	Cyan	Green	Magenta	Red	Blue	Black
Y	IRE	100	92.8	78.7	71.5	28.5	21.3	7.2	0
	mV	700	650	551	501	200	149	50	0
Pb	IRE	0	–50	11.4	–38.5	38.5	–11.4	50	0
	mV	0	–350	80	–270	270	–80	350	0
Pr	IRE	0	4.6	–50	–45.4	45.4	50	–4.6	0
	mV	0	32	–350	–318	318	350	–32	0
Y	64 to 940	940	877	753	690	314	251	127	64
Cb	64 to 960	512	64	614	167	857	410	960	512
Cr	64 to 960	512	553	64	106	918	960	471	512

Table 5.13. EIA-770.3 HDTV YPbPr and YCbCr 100% Color Bars. YPbPr values relative to the blanking level.

		White	Yellow	Cyan	Green	Magenta	Red	Blue	Black
Y	IRE	75	69.6	59	53.7	21.3	16	5.4	0
	mV	525	487	413	376	149	112	38	0
Pb	IRE	0	–37.5	8.6	–28.9	28.9	–8.6	37.5	0
	mV	0	–263	60	–202	202	–60	263	0
Pr	IRE	0	3.5	–37.5	–34	34	37.5	–3.5	0
	mV	0	24	–263	–238	238	263	–24	0
Y	64 to 940	721	674	581	534	251	204	111	64
Cb	64 to 960	512	176	589	253	771	435	848	512
Cr	64 to 960	512	543	176	207	817	848	481	512

Table 5.14. EIA-770.3 HDTV YPbPr and YCbCr 75% Color Bars. YPbPr values relative to the blanking level.

YPbPr data drives three 10-bit DACs to generate the analog YPbPr video signals.

Video Level	Y	PbPr
white	800	512
sync high	488	748
black	252	512
blank	252	512
sync low	16	276

Table 5.15. HDTV 10-Bit YPbPr Values.

Analog YPbPr Digitization

Assuming 10-bit ADCs with an input range of 0–1.305V (to match the video ADCs used by the NTSC/PAL decoder in Chapter 9), the 10-bit YPbPr to YCbCr equations are:

$$Y = 1.5985(Y - 252) + 64$$

$$Cb = 1.635(Pb - 512) + 512$$

$$Cr = 1.635(Pr - 512) + 512$$

Y has a nominal 10-bit range of 252–800 to match the active video levels used by the NTSC/PAL decoder in Chapter 9. Table 5.15 and Figures 5.11 and 5.12 illustrate the 10-bit YPbPr values for the white, black, blank, and (optional) sync levels.

VBI Data for 720p Systems

CGMS Type A

CEA-805 and EIA-J CPR–1204–2 define the format of CGMS (Copy Generation Management System) data on line 24 for 720p systems. The waveform is illustrated in Figure 5.13.

A sample clock rate of 74.176 MHz (59.94 Hz frame rate) or 74.25 MHz (60 Hz frame rate) is used. Each data bit is 58 clock cycles, or 782 ±30 ns, wide with a maximum rise and fall time of 50 ns. A logical “1” has an amplitude of 70 ±10 IRE; a logical “0” has an amplitude of 0 ±5 IRE.

The 2-bit start symbol begins 232 clock cycles, or about 3.128 µs, after 0_H. It consists of a “1” followed by a “0.”

The 6-bit header and 14-bit CGMS payload data format is the same as for 480p systems discussed earlier in this chapter.

CGMS Type B

CEA-805 defines the format of CGMS (Copy Generation Management System) data on line 23 for 720p systems. The waveform is illustrated in Figure 5.14.

A sample clock rate of 74.176 MHz (59.94 Hz frame rate) or 74.25 MHz (60 Hz frame rate) is used. Each data bit is eight clock cycles, or 107.7 ±18.5 ns, wide with a maximum rise and fall time of 37 ns. A logical “1” has an amplitude of 70 ±10 IRE; a logical “0” has an amplitude of 0 ±5 IRE.

The 2-bit start symbol begins 232 clock cycles, or about 3.128 µs, after 0_H. It consists of a “1” followed by a “0.”

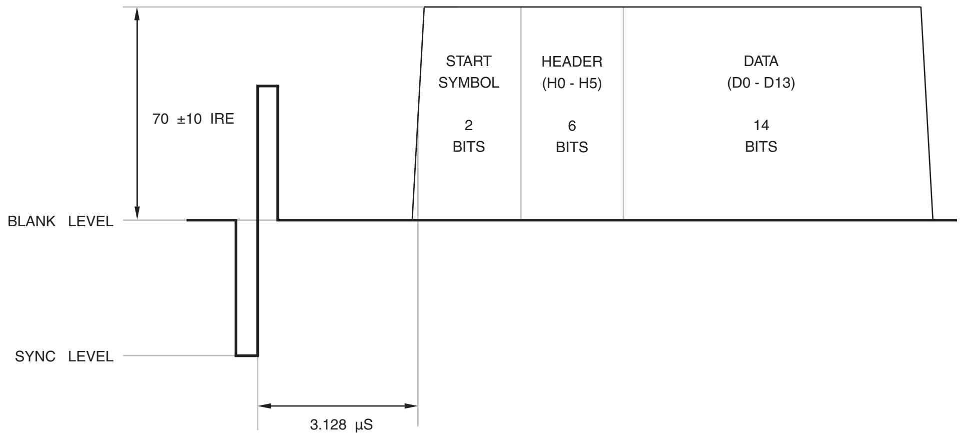

Figure 5.13. CEA-805 and EIA-J CPR–1204–2 Line 24 Timing.

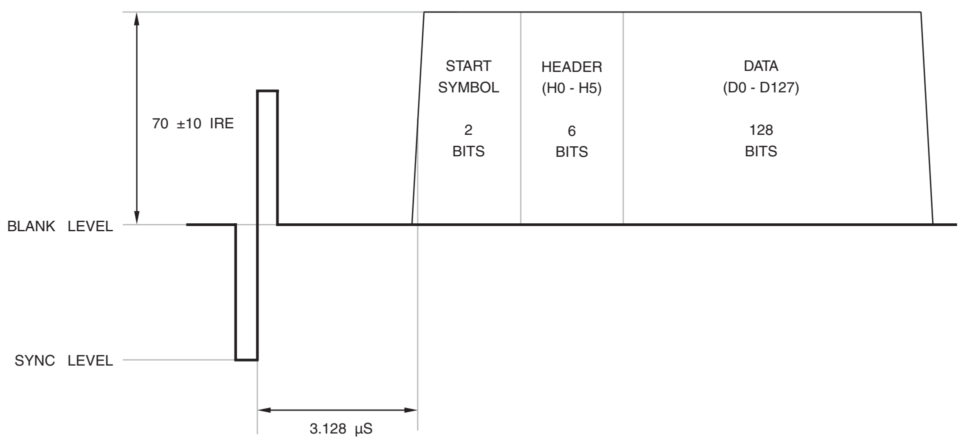

Figure 5.14. CEA-805 Line 23 Timing.

The 6-bit header and 16-byte payload data format is the same as for 480p systems discussed earlier in this chapter.

VBI Data for 1080i Systems

CGMS Type A

CEA-805 and EIA-J CPR–1204–2 define the format of CGMS (Copy Generation Management System) data on lines 19 and 582 for 1080i systems. The waveform is illustrated in Figure 5.15.

A sample clock rate of 74.176 MHz (59.94 Hz field rate) or 74.25 MHz (60 Hz field rate) is used. Each data bit is 77 clock cycles, or 1038 ±30 ns, wide with a maximum rise and fall time of 50 ns. A logical "1" has an amplitude of 70 ±10 IRE; a logical "0" has an amplitude of 0 ±5 IRE.

The 2-bit start symbol begins 308 clock cycles, or about 4.152 µs, after 0_H. It consists of a "1" followed by a "0."

The 6-bit header and 14-bit CGMS payload data format is the same as for 480p systems discussed earlier in this chapter.

CGMS Type B

CEA-805 defines the format of CGMS (Copy Generation Management System) data on lines 18 and 581 for 1080i systems. The waveform is illustrated in Figure 5.16.

A sample clock rate of 74.176 MHz (59.94 Hz frame rate) or 74.25 MHz (60 Hz frame rate) is used. Each data bit is ten clock cycles, or 134.6 ±18.5 ns, wide with a maximum rise and fall time of 37 ns. A logical "1" has an amplitude of 70 ±10 IRE; a logical "0" has an amplitude of 0 ±5 IRE.

The 2-bit start symbol begins 308 clock cycles, or about 4.152 µs, after 0_H. It consists of a "1" followed by a "0."

The 6-bit header and 16-byte payload data format is the same as for 480p systems discussed earlier in this chapter.

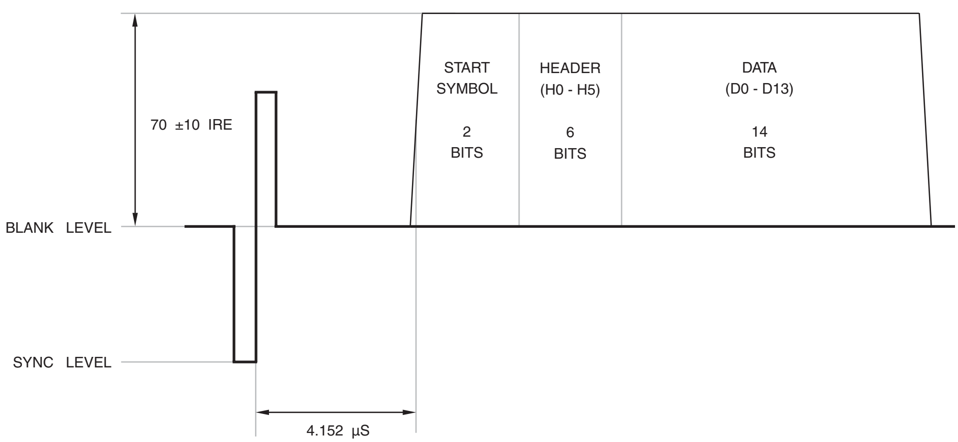

Figure 5.15. CEA-805 and EIA-J CPR–1204–2 Lines 19 and 582 Timing.

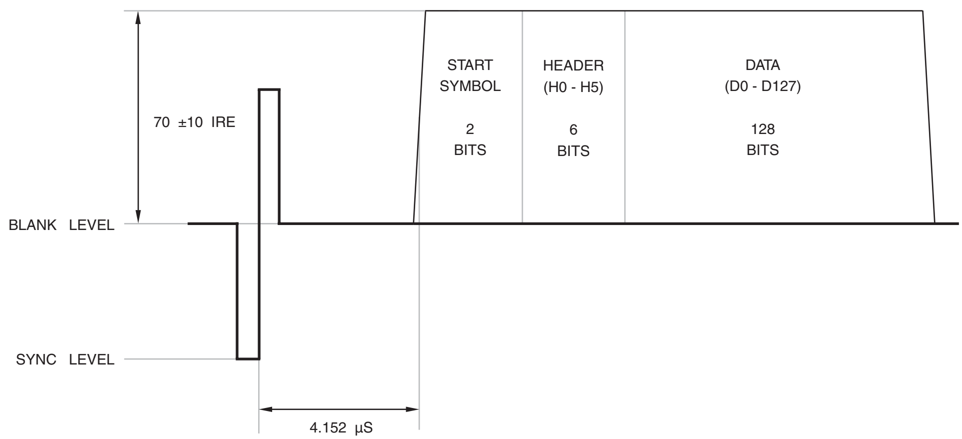

Figure 5.16. CEA-805 Lines 18 and 581 Timing.

Constrained Image

Due to the limited availability of copy protection technology for high-definition analog interfaces. some standards and DRM implementations only allow a *constrained image* to be output. A constrained image has an effective maximum resolution of 960 × 540p, although the total number of video samples and the video timing remain unchanged (for example, 1280 × 720p60 or 1920 × 1080i30).

In these situations, the full resolution image is still available via an approved secure digital video output, such as HDMI.

D-Connector Interface

A 14-pin female D-connector (EIA-J CP–4120 standard, EIA-J RC–5237 connector) is optionally used on some high-end consumer equipment in Japan, Hong Kong, and Singapore. It is used to transfer EIA 770.2 or EIA 770.3 interlaced or progressive analog YPbPr video.

There are five flavors of the D-connector, referred to as D1, D2, D3, D4, and D5, each used to indicate supported video formats, as shown in Table 5.16. Figure 5.17 illustrates the connector and Table 5.17 lists the pin names.

Three line signals (Line 1, Line 2, and Line 3) indicate the resolution and frame rate of the YPbPr source video, as indicated in Table 5.18.

	480i	480p	720p	1080i	1080p
D1	×				
D2	×	×			
D3	×	×		×	
D4	×	×	×	×	
D5	×	×	×	×	×

Table 5.16. D-Connector Supported Video Formats.

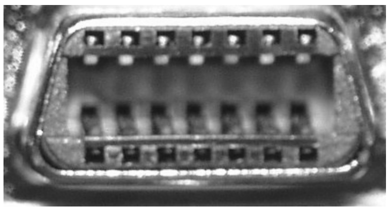

Figure 5.17. D-Connector.

Pin	Function	Signal Level	Impedance
1	Y	0.700V + sync	75 ohms
2	ground - Y		
3	Pb	±0.350V	75 ohms
4	ground - Pb		
5	Pr	±0.350V	75 ohms
6	ground - Pr		
7	reserved 1		
8	line 1	0V, 2.2V, or 5V[1]	10K ±3K ohm
9	line 2	0V, 2.2V, or 5V[1]	10K ±3K ohm
10	reserved 2		
11	line 3	0V, 2.2V, or 5V[1]	10K ±3K ohm
12	ground - detect plugged		
13	reserved 3		
14	detect plugged	0V = plugged in[2]	> 100K ohm

Notes:
1. 2.2V has range of 2.2V ±0.8V. 5V has a range of 5V ±1.5V.
2. Inside equipment, pin 12 is connected to ground and pin 14 is pulled to 5V through a resistor. Inside each D-Connector plug, pins 12 and 14 are shorted together.

Table 5.17. D-Connector Pin Descriptions.

Resolution		Frame Rate	Line 1 Scan Lines	Line 2 Frame Rate	Line 3 Aspect Ratio	Chromaticity and Reference White	Color Space Equations	Gamma Correction	Sync Amplitude on Y
1920x1080		30i	5V	0V	5V	EIA-770.3	EIA-770.3	EIA-770.3	±0.300V[3]
		25i[2]	5V	2.2V	5V				
		30p	5V	2.2V	5V				
		25p[2]	5V	2.2V	5V				
		24p[2]	5V	2.2V	5V				
		24sF[2]	5V	2.2V	5V				
1280x720		60p	2.2V	5V	5V				
		50p[2]	2.2V	2.2V	5V				
		30p	2.2V	2.2V	5V				
		25p[2]	2.2V	2.2V	5V				
		24p[2]	2.2V	2.2V	5V				
640x480		60p[2]	0V	5V	0V	EIA-770.2	EIA-770.2	EIA-770.2	–0.300V[3]
720x480	16:9 Squeeze	60p	0V	5V	5V				
	16:9 Squeeze	30i	0V	0V	5V				
	16:9 Letterbox	30i	0V	0V	2.2V				
	4:3	30i	0V	0V	0V				

Notes:
1. 60p, 30i, 30p, and 24p frame rates also include the 59.94p, 29.97i, 29.97p, and 23.976p frame rates.
2. Not part of EIAJ CP-4120 specification, but commonly supported by equipment.
3. Relative to the blanking level.

Table 5.18. Voltage Levels of Line Signals for Various Video Formats for D-Connector.

Other Pro-Video Analog Interfaces

Tables 5.19 and 5.20 list some other common component analog video formats. The horizontal and vertical timing is the same as for 525-line (M) NTSC and 625-line (B, D, G, H, I) PAL. The 100% and 75% color bar values are shown in Tables 5.21 through 5.24. The SMPTE, EBU N10, 625-line Betacam, and 625-line MII values are the same as for SDTV YPbPr.

VGA Interface

Table 5.25 and Figure 5.18 illustrate the 15-pin VGA connector used by computer equipment, and some consumer equipment, to transfer analog RGB signals. The analog RGB signals do not contain sync information and have no blanking pedestal, as shown in Figure 5.4.

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12. SMPTE 253M–1998, *Television—Three-Channel RGB Analog Video Interface*.
13. SMPTE 274M–2005, *Television—1920 × 1080 Image Sample Structure, Digital Representation and Digital Timing Reference Sequences for Multiple Picture Rates*.
14. SMPTE 293M–2003, *Television—720 × 483 Active Line at 59.94 Hz Progressive Scan Production—Digital Representation*.
15. SMPTE RP-160–1997, *Three-Channel Parallel Analog Component High-Definition Video Interface*.

Format	Output Signal	Signal Amplitudes (volts)	Notes
SMPTE, EBU N10	Y	+0.700	0% setup on Y 100% saturation three wire = (Y + sync), (R′–Y), (B′–Y)
	sync	–0.300	
	R′–Y, B′–Y	±0.350	
525-Line Betacam[1]	Y	+0.714	7.5% setup on Y only 100% saturation three wire = (Y + sync), (R′–Y), (B′–Y)
	sync	–0.286	
	R′–Y, B′–Y	±0.467	
625-Line Betacam[1]	Y	+0.700	0% setup on Y 100% saturation three wire = (Y + sync), (R′–Y), (B′–Y)
	sync	–0.300	
	R′–Y, B′–Y	±0.350	
525-Line MII[2]	Y	+0.700	7.5% setup on Y only 100% saturation three wire = (Y + sync), (R′–Y), (B′–Y)
	sync	–0.300	
	R′–Y, B′–Y	±0.324	
625-Line MII[2]	Y	+0.700	0% setup on Y 100% saturation three wire = (Y + sync), (R′–Y), (B′–Y)
	sync	–0.300	
	R′–Y, B′–Y	±0.350	

Notes:
1. Trademark of Sony Corporation.
2. Trademark of Matsushita Corporation.

Table 5.19. Common Pro-Video Component Analog Video Formats.

Format	Output Signal	Signal Amplitudes (volts)	Notes
SMPTE, EBU N10	G′, B′, R′	+0.700	0% setup on G′, B′, and R′ 100% saturation three wire = (G′ + sync), B′, R′
	sync	–0.300	
NTSC (setup)	G′, B′, R′	+0.714	7.5% setup on G′, B′, and R′ 100% saturation three wire = (G′ + sync), B′, R′
	sync	–0.286	
NTSC (no setup)	G′, B′, R′	+0.714	0% setup on G′, B′, and R′ 100% saturation three wire = (G′ + sync), B′, R′
	sync	–0.286	
MII[1]	G′, B′, R′	+0.700	7.5% setup on G′, B′, and R′ 100% saturation three wire = (G′ + sync), B′, R′
	sync	–0.300	

Notes:
1. Trademark of Matsushita Corporation.

Table 5.20. Common Pro-Video RGB Analog Video Formats.

		White	Yellow	Cyan	Green	Magenta	Red	Blue	Black
Y	**IRE**	100	89.5	72.3	61.8	45.7	35.2	18.0	7.5
	mV	714	639	517	441	326	251	129	54
B′–Y	**IRE**	0	–65.3	22.0	–43.3	43.3	–22.0	65.3	0
	mV	0	–466	157	–309	309	–157	466	0
R′–Y	**IRE**	0	10.6	–65.3	–54.7	54.7	65.3	–10.6	0
	mV	0	76	–466	–391	391	466	–76	0

Table 5.21. 525-Line Betacam 100% Color Bars. Values are relative to the blanking level.

		White	Yellow	Cyan	Green	Magenta	Red	Blue	Black
Y	**IRE**	76.9	69.0	56.1	48.2	36.2	28.2	15.4	7.5
	mV	549	492	401	344	258	202	110	54
B′–Y	**IRE**	0	–49.0	16.5	–32.5	32.5	–16.5	49.0	0
	mV	0	–350	118	–232	232	–118	350	0
R′–Y	**IRE**	0	8.0	–49.0	–41.0	41.0	49.0	–8.0	0
	mV	0	57	–350	–293	293	350	–57	0

Table 5.22. 525-Line Betacam 75% Color Bars. Values are relative to the blanking level.

		White	Yellow	Cyan	Green	Magenta	Red	Blue	Black
Y	IRE	100	89.5	72.3	61.8	45.7	35.2	18.0	7.5
	mV	700	626	506	433	320	246	126	53
B′–Y	IRE	0	–46.3	15.6	–30.6	30.6	–15.6	46.3	0
	mV	0	–324	109	–214	214	–109	324	0
R′–Y	IRE	0	7.5	–46.3	–38.7	38.7	46.3	–7.5	0
	mV	0	53	–324	–271	271	324	–53	0

Table 5.23. 525-Line MII 100% Color Bars. Values are relative to the blanking level.

		White	Yellow	Cyan	Green	Magenta	Red	Blue	Black
Y	IRE	76.9	69.0	56.1	48.2	36.2	28.2	15.4	7.5
	mV	538	483	393	338	253	198	108	53
B′–Y	IRE	0	–34.7	11.7	–23.0	23.0	–11.7	34.7	0
	mV	0	–243	82	–161	161	–82	243	0
R′–Y	IRE	0	5.6	–34.7	–29.0	29.0	34.7	–5.6	0
	mV	0	39	–243	–203	203	243	–39	0

Table 5.24. 525-Line MII 75% Color Bars. Values are relative to the blanking level.

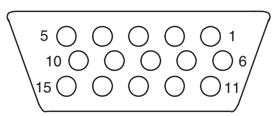

Figure 5.18. VGA 15-Pin D-SUB Female Connector.

Pin	Function	Signal Level	Impedance
1	red	0.7v	75 ohms
2	green	0.7v	75 ohms
3	blue	0.7v	75 ohms
4	ground		
5	ground		
6	ground - red		
7	ground - green		
8	ground - blue		
9	+5V DC		
10	ground - HSYNC		
11	ground - VSYNC		
12	DDC SDA (data)	≥ 2.4v	
13	HSYNC (horizontal sync)	≥ 2.4v	
14	VSYNC (vertical sync)	≥ 2.4v	
15	DDC SCL (clock)	≥ 2.4v	

Notes:
1. DDC = Display Data Channel.

Table 5.25. VGA Connector Signals.