Yiqin Wang

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Objectives

Obtain a full-time job, after graduation from UCLA MS after April 2019, on Analog/Digital Circuit Analysis/Design, VLSI Design or Computational vision.

Education Backgrounds

M.S., Electrical Engineering. University of California, Los Angeles, expected March 2019 GPA: 3.283/4.00

B.S., Electrical Engineering. University of California, Santa Barbara, June 2017 GPA: 3.47/4.00 with 5 times Dean's Honors (ENGR)

Relevant course work:

- Analog and Digital Integrated Circuit Design and Electronics
- Signal Analysis
- Digital/Analog Signal Processing
- VLSI Circuit and System
- Software/Hardware Interference
- Mix-signal Circuit Design
- Communication
- Capstone project

Qualifications

- Five years plus of lab and project-related work of Analog/Digital circuit analyzing, circuit testing and logic design, mostly focus on mixed-signal integrated circuits, VLSI circuit and computer vision.
- Currently working as rotational candidate at Professor Achuta Kadambi's Visual Machines Group (http://visual.ee.ucla.edu/)
- Worked as Electrical Engineering internship at Bossa Nova Technologies LLC (rebrand as Sound & Bright https://www.soundnbright.com/).
- Interests on mixed-signal circuit design, RF wireless communication and pattern recognizing/machine learning now.
- Developed skills including: measuring data, coding control circuits, programming on different hardware plate, software/hardware interface, EDA design, I2C and I2S communication, analog circuit design, digital circuit design.
- Software/Hardware competencies: Linux, Arduino, FPGA, C, Embedded C, C++, MATLAB, Verilog, XlinxSDK, Vivado, Quartus II, Microsoft Office, Latex, HSPICE, Sue, Max, Cosmospice, ModelSim, LPCXpresso, Cadence, ExpressPCB, TINA, FLIR system.
- Fluent communication in English and Chinese (familiarity with Japanese, self-learnt Spanish).

Research

Rotational Candidate in Visual Machines Group **August 2018 – Now**

- Focusing on the thesis topic about non-line-of-sight vision systems in the context of sparse approximation.
- Ordered and set up all the computational imaging system including projector,

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FLIR digital camera and thermal camera. Set up the MATLAB programs for image capturing and analysis.

- Performed the candidate project about image separation and synthetic aperture imaging, depth mapping and polarization
- Setup the Visual Machines Group lab space with Professor Achuta and other graduate students.

Internships and Jobs

Instructor for CSM51A (logic design) summer CEED (Center for Excellence in Engineering and Diversity) program in UCLA September 2018 – September 2018

- Prepared the material including lecture, 7 homework, midterm and final for 11 students.
- Lectured for 2 weeks about the logic design topics which will normally covered in regular CSM51A for 3 or more weeks.
- Graded the homework and gave the students help through office hour and emails.

Internship in Bossa Nova Technologies March 2018 – August 2018

- Tested and validated the functionality of 12 pre-designed PCBs of different components such as power, control panels, demodulation, rectifier, gain-control amplifier and photodiode receiver of MCRQ interferometer by senior engineers. Discussed and helped the senior engineers to improve the design or change design based on the errors found.
- Redesign the PCB layout of 12 different circuits in ExpressPCB to make the circuit clear and easy to test. Figured out the best way of circuit layout, which has the smallest interference between signals and power and reduce the possible area.
- Ordering, soldering and debugging all the potential errors in PCB. Correctly figured out over 40 errors in different circuit designs, such as mismatch in capacitors and transistors, amplifier gain error and imaginary solder.

Internship in Tonghui Electronic Co. August 2016 – September 2016

- Participated in a product design group and understood the difference between a commercial design and a campus research-project based design.
- Assisted their senior engineers to examine the integrated circuit on PCB and recorded the data. Provided possible solutions based on observation and testing results analysis. There were 5 changes been made based my suggestion.
- Understood how to change the design based on the customer's demand.

Projects

12 bit SAR ADC Design April 2018 – June 2018

- Worked as a class project on building up a SAR ADC for IEEE 801.12c using Cadance 45nm CMOS. Successfully meet all the specs including INL/DNL <

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1LSB, SFNR > 60dB while sampling rate 80MS/s. The power is around 10mW.
- Worked on the part to verify the behavior correctness of the SAR ADC. Used Monte Carlo in Cadence to verify the error.

Monte Carlo Circuit Testing Project **April 2018 – June 2018**
- Worked as a class project on digital circuit logic chain validation. Use Matlab and Hspice to simulate a logic gate chain in transistor level about 360 variables based on high dimensional hyper-spherical clustering and sampling.
- Successfully reduce the number of simulations of high sigma situation from 3M using Monte Carlo to 18k samples while maintaining the fom around 0.01 while the failure probability is 3% away from the probability using Monte Carlo.

3D Non-volatile RAM Design **January 2017 – March 2018**
- Worked as a class project on digital circuit design on the topic of 3D Non-volatile RAM using 45nm CMOS technology in Cadence.
- Implemented the algorithm in multilevel circuit structure. The design are targeting to minimize the delay and leakage in the whole 7 layer memory cells.

Gear Faults Detection using Time-Frequency Analysis **January 2017 – March 2018**
- Worked as a class project on gear faults detection from gearbox using time-frequency analysis (TFR). Implemented the algorithm of different methods of TFRs including STFT, Wigner-Ville Distribution, Choi-William Distribution and Continues Wavelet Transfer in Matlab and able to figure out faults like teeth break, gear break and worn down.

Neural Network Project **September 2017 – December 2017**
- Designed the algorithm of neural network in deep learning, which takes the image data as input, and calculate which number from 0-9 has the highest possibility in Verilog.
- Used IC complier to post-synthesis the area and power, which is in order to make the neural network system consume less energy while maintaining the accuracy over 83%.

Power Amplifier Project **September 2017 – December 2017**
- Designed a fully differential power amplifier based on 45nm CMOS technology, meet the specs including 1V peak to peak swing, 40dB gain, 2GHz bandwidth, 60 degree phase margin.
- Used Cadence to build up the entire circuit and verify the design, successfully recreate the above specifications.

EE Senior Capstone Project with SONOS Inc. **September 2016 – June 2017**
- Lead the group of multidiscipline students to design how the Digital Signal

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Processing block will reduce the noise and echo when recording the voice file and filter the actual needed voice command in 3 months.

- Designed the circuit to rectify the incoming signal and amplify it with the microprocessor LPC 4088.
- Cooperated highly with Computer Engineering group and Mechanical Engineering group to figure out how to implement the PCB and how to fit it inside of pre-designed prototype case. Successfully made 4 prototypes and finally 2 working devices.

CAD Design **January 2017 – March 2017**

- Designed a system design automation based on the master and slave bridge.

Tetris Project **January 2017 – March 2017**

- Designed the classic Tetris game based on C.
- Used the LPCXpresso environment to understand the I2C communication in the project to print the Tetris to LCD screen.

Chromatic Tuner **September 2016 – December 2016**

- Designed a Chromatic Tuner on Nexys4 DDR development board from Digilent.
- Optimized the code to read the user input accurately and optimized the FFT function to detect the corresponding frequencyprecisely.

Communication system using acoustic link **April 2016 – June 2016**

- Designed the low filter which could cut certain frequency or above in order to eliminate noise.
- Designed the transmittal system and tested the whole system with a pilot signal with its matched component.
- Optimized the speed of code for better user experience.

Acoustic phased array **April 2016 – June 2016**

- Designed the delay stage and amplifier stage to drive a certain numbers of speaker combination rings and make the sound to focus on certain location.
- Wrote the Matlab simulation code to locate the focus points of speaker ring and graph the corresponding sound intensity.
- Constructed the speaker rings on a stable board on minimize the noise.

FPGA logic design **April 2016 – June 2016**

- Designed logic structure of a fully functionaladder and thunderbird tail light.
- Implemented the design using Verilog and downloaded the code to FPGA to test the correctness.
- Improved the stability and performance of the tail light by considering all the possible combination of input, including the false trigger or false input.
- Researched about how the hardware design based on software code.

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Special Skills

Evaluated leadership and participation in laboratory and working scenario

- Assisted colleagues in designing, implementing and presenting projects in labs and company.
- Co-organized and –facilitated teaching assistant or senor engineers in debugging and testing circuits.
- Contributed to solving problems with others and sharing ideas. Lead the group to find solutions with others.

Advanced design abilities and self-correct skills

- Used different tools and programs to model particular circuits and monitor the signal when hand checking is highly impossible.
- Checked the project constantly and try to fully understand and fix the problems by my own at first time.
- Presented various solutions for signal problem and comparing to seek the best one.

Illustrated presentations skills and communication skills

- Presented the essence of interviews with professors clearly using PowerPoint, posters and live demo.
- Performed fluent speeches about science research in front of crowd.

Organized assembling abilities

- Built most circuit projects in laboratory by hands and tools.
- Packaged different electrical elements together precisely and swiftly.
- Redesigned the blueprint when mistakes occur.

Friendly and helpful coworking skills in different culture and background

- Worked with different engineers from different background and culture. Respected all equally and nicely.
- Treated everyone fairly and respectfully in different situation. Helped one of my students in CEED program with body difficulties.