CNT_EPP

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity cnt_epp is
  port (
    CLK      : in    std_logic;
    RST      : in    std_logic;
    ASTRB    : in    std_logic;
    DSTRB    : in    std_logic;
    DATA     : inout std_logic_vector(7 downto 0);
    PWRITE   : in    std_logic;
    PWAIT    : out   std_logic;
    DATO_RD  : in    std_logic_vector(7 downto 0);
    CE_RD    : out   std_logic;
    DIR      : out   std_logic_vector (7 downto 0);
    DIR_VLD  : out   std_logic;
    DATO     : out   std_logic_vector (7 downto 0);
    DATO_VLD : out   std_logic);
end ;

architecture rtl of cnt_epp is

  signal DFAS : std_logic ;
  signal DFDS : std_logic ;
  signal ASBD : std_logic ;
  signal DSBD : std_logic ;

begin
  PWAIT <= '1' when(ASTRB='0' or DSTRB='0') else '0';

  process (DSTRB,PWRITE, DATO_RD) is
  begin  -- process
    if DSTRB='0' and PWRITE='1' then
      CE_RD <= '1';
                  DATA <= DATO_RD;
    else
      CE_RD <= '0';
                  DATA <= (others => 'Z');
    end if;
  end process;

  process (CLK, RST) is
  begin  -- process
    if RST = '1' then
      ASBD <= '1';
    elsif CLK'event and CLK = '1' then
      ASBD <= ASTRB;
    end if;
  end process;

  DFAS <= '1' when (ASTRB='1' and ASBD='0') else '0';
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```
  process (CLK, RST) is
  begin  -- process
    if RST = '1' then
      DIR_VLD <= '0';
    elsif CLK'event and CLK = '1' then
      DIR_VLD <= DFAS;
    end if;
  end process;

  process (CLK, RST) is
  begin  -- process
    if RST = '1' then
      DIR <= (others => '0');
    elsif CLK'event and CLK = '1' then
      if DFAS='1' then
        DIR <= DATA;
      end if;
    end if;
  end process;

  process (CLK, RST) is
  begin  -- process
    if RST = '1' then
      DSBD <=  '1';
    elsif CLK'event and CLK = '1' then
      DSBD <= DSTRB;
    end if;
  end process;

  DFDS <= '1' when (DSTRB='1' and DSBD='0' and PWRITE='0') else '0';

  process (CLK, RST) is
  begin  -- process
    if RST = '1' then
      DATO_VLD <= '0';
    elsif CLK'event and CLK = '1' then
      DATO_VLD <= DFDS;
    end if;
  end process;

  process (CLK, RST) is
  begin  -- process
    if RST = '1' then
      DATO <= (others => '0');
    elsif CLK'event and CLK = '1' then
      if DFDS='1' then
        DATO <= DATA;
      end if;
    end if;
  end process;
end rtl;
```