GEN_FUNCIONES_TB

```
library ieee;
use ieee.std_logic_1164.all;

entity gen_funciones_tb is
end entity gen_funciones_tb;

architecture gen_funciones of gen_funciones_tb is

  signal RELOJ  : std_logic := '0';
  signal RST    : std_logic;
  signal ASTRB  : std_logic := '0';
  signal DSTRB  : std_logic := '0';
  signal DATA   : std_logic_vector(7 downto 0):=(others =>'0');
  signal PWRITE : std_logic := '0';
  signal PWAIT  : std_logic;
  signal SYNC   : std_logic;
  signal SCLK   : std_logic;
  signal D1     : std_logic;
  signal D2     : std_logic;

begin  -- architecture gen_funciones

  Device : entity work.epp_device1
    port map (
      DATA   => DATA,
      PWRITE => PWRITE,
      DSTRB  => DSTRB,
      ASTRB  => ASTRB,
      PWAIT  => PWAIT);

  DUT : entity work.gen_funciones
    port map (
      RELOJ  => RELOJ,
      RST    => RST,
      ASTRB  => ASTRB,
      DSTRB  => DSTRB,
      DATA   => DATA,
      PWRITE => PWRITE,
      PWAIT  => PWAIT,
      SYNC   => SYNC,
      SCLK   => SCLK,
      D1     => D1,
      D2     => D2);

          Fin1 : entity work.DAC121S101
            port map(
                    SYNC => SYNC,
                    SCLK => SCLK,
                    DIN  => D1);

          Fin2 : entity work.DAC121S101
```

```
        port map(
                SYNC => SYNC,
                SCLK => SCLK,
                DIN  => D2);

  RELOJ <= not RELOJ after 5 ns;
  RST   <= '1', '0'  after 128 ns;

end architecture gen_funciones;
```