DCM

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_arith.all;
use ieee.numeric_std.all;

library unisim;
use unisim.vcomponents.all;

entity dcm is
port
 (-- Clock in ports
  CLK_IN          : in     std_logic;
  -- Clock out ports
  CLK_OUT         : out    std_logic;
  -- Status and control signals
  RESET           : in     std_logic
 );
end dcm;

architecture xilinx of dcm is
  attribute CORE_GENERATION_INFO : string;
  attribute CORE_GENERATION_INFO of xilinx :
  -- Input clock buffering / unused connectors
  signal clkin1           : std_logic;
  -- Output clock buffering
  signal clk_out1_internal : std_logic;
  signal clkfb            : std_logic;
  signal clk0             : std_logic;
  signal clkfbout          : std_logic;
  signal locked_internal   : std_logic;
  signal status_internal   : std_logic_vector(7 downto 0);
begin

  -- Input buffering
  ------------------------------------
  clkin1_buf : IBUFG
  port map
   (O => clkin1,
    I => CLK_IN);

  -- Clocking primitive
  ------------------------------------

  -- Instantiation of the DCM primitive
  --    * Unused inputs are tied off
  --    * Unused outputs are labeled unused
  dcm_sp_inst: DCM_SP
  generic map
   (CLKDV_DIVIDE         => 2.000,
    CLKFX_DIVIDE         => 1,
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   CLKFX_MULTIPLY       => 4,
   CLKIN_DIVIDE_BY_2    => FALSE,
   CLKIN_PERIOD         => 10.0,
   CLKOUT_PHASE_SHIFT   => "NONE",
   CLK_FEEDBACK         => "1X",
   DESKEW_ADJUST        => "SYSTEM_SYNCHRONOUS",
   PHASE_SHIFT          => 0,
   STARTUP_WAIT         => FALSE)
  port map
   -- Input clock
   (CLKIN               => clkin1,
    CLKFB               => clkfb,
    -- Output clocks
    CLK0                => clk0,
    CLK90               => open,
    CLK180              => open,
    CLK270              => open,
    CLK2X               => open,
    CLK2X180            => open,
    CLKFX               => open,
    CLKFX180            => open,
    CLKDV               => open,
   -- Ports for dynamic phase shift
    PSCLK               => '0',
    PSEN                => '0',
    PSINCDEC            => '0',
    PSDONE              => open,
   -- Other control and status signals
    LOCKED              => locked_internal,
    STATUS              => status_internal,
    RST                 => RESET,
   -- Unused pin, tie low
    DSSEN               => '0');


  -- Output buffering
  -----------------------------------
  clkfb <= clk_out1_internal;


  clkout1_buf : BUFG
  port map
   (O   => clk_out1_internal,
    I   => clk0);


  CLK_OUT <= clk_out1_internal;

end xilinx;
```