Lalith Chandra M

+91 6300 310801 • lalithchandram@gmail.com • linkedin.com/in/lalithchandra • github.com/nogieman

Experience

Vicharak Computers: FPGA Developer Intern June 2025 - Present
Gati: an Edge ML Accelerator. Surat, Gujarat, India

- Built and verified fully parameterized ML-specific compute blocks in Verilog (AveragePool, Sigmoid, Tanh) for Efinix Trion FPGA on Vaaman board(RK3999 ARM processor with FPGA).
- Validated and debugged LPDDR3 and DDR3L memory interfaces on custom PCBs (Frequency and timing parameters, working of on-chip oscillators), performed DDR calibration and training.
- Investigated various FPGA-Based compute logic for Computer vision models and LLMs for reconfigurable edge acceleration.

VLSI Research Intern: National Institute of Technology, Delhi May 2024 - July 2024
Self proposed project.

- Architected a 32-bit approximate image multiplier with Vivado (Verilog for Artix-7 FPGA), achieving 30% lesser power consumption in image processing workloads.
- Completed physical design and functional verification of the multiplier as ASIC for 90nm and 180nm technologies (Cadence Genus, Innovus, NCSim), ensuring design met PPA (Power, Performance, Area) constraints.

Education

Rajiv Gandhi University of Knowledge Technologies, Basar, TS June 2021 - May 2025
B.Tech., Electronics and Communication Engineering 7.77 GPA

Academic Projects

Advanced AXI FireFly Architecture for SNN Acceleration Sep 2024 – May 2025
Enhanced a high-performance VLSI architecture for spiking neural network acceleration (Vivado, Python, SpinalHDL).

- Integrated approximation units into the FireFly accelerator pipeline to improve throughput and reduce area.
- Generated synthesizable verilog from **SpinalHDL (Scala)** and custom blocks integrated at the RTL level.
- Verified functionality using cocotb based testbenches and implemented the synthesized design on an FPGA board.

License Plate Networking (V2V Communication) Sep 2023 – Jan 2024
Proposed and led the design of a vehicle-to-vehicle communication system using license plates as unique identifiers.

- Designed the license plate detection pipeline using a custom-trained **YOLOv8** model, achieving 97% detection accuracy (Python, Google Colab).
- Used **EasyOCR** for text extraction and built a cropping module for clean text generation.
- Delivered the complete detection and recognition module as the core component for further system integration.

Approximate MAC Unit Feb 2024 – May 2024

- Designed an approximate Multiply-Accumulate unit using an 8-bit truncation adder and 11-bit approximate accumulator.
- Verified functionality and power savings using Icarus Verilog (iverilog), Vivado, and GTKWave.

Co-curriculars

Secretary: Entrepreneurship Cell, RGUKT Basar Sep 2022 – Jan 2025

- Progressed from PR Manager to Corporate Relations Manager and finally elected as the Secretary, leading the university's Entrepreneurship Cell.
- Organized large-scale startup hackathons, played a key role in establishing an on-campus incubation center.
- Mentored and supported 3 student startups that advanced to the zonal rounds of IIT Bombay's Eureka! competition.

Technical & Creative Team Member: Department of ECE, RGUKT Basar Sep 2022 – May 2025

- Mentored multiple student projects showcased at the university's AntahPragnya 2025 Technical Festival.
- Led graphic design and on-stage technical operations for major departmental events.
- Designed event posters and produced high-quality promotional videos to boost engagement.

Activities and Achievements

- Invited by Telangana Innovation Cell (TGIC) to attend and was officially sponsored for **Startup Mahakumbh 2024**.
- Moderated the Student Dialogue Panel at Kakatiya Sandbox's 6th and 7th Development Dialogue.
- Moderated at the university's first-ever SDG Summit.
- Secured 1st runner-up at the National Entrepreneurship Challenge (NEC) 2024 and placed in the **Top 9 at NEC 2023**.
- Attended key events including the **Telangana Global AI Summit**, Development Dialogue Expo, and IITB's E-Summit 2023 & 2024.
- Organized an overnight hackathon on campus with 36 participating teams (250+ students) and judged 20+ startup ideas.

Technical Skills

Languages: Verilog, SystemVerilog, Python, C++, Scala
FPGA/EDA Tools: Efinity IDE, Xilinx Vivado, IVerilog, GTKWave, Cadence Genus & Innovus, NCSim
Hardware Platforms: Efinix FPGAs, reconfigurable SBCs, DDR3L/LPDDR3 Memory Interfaces, AXI, UART protocols
Tech Stack: ASIC Design Flow (RTL to GDSII), Linux OS, Python and Bash scripting

Summary

RTL Design engineer with experience in ML accelerators, SoC integration and DDR memory subsystems and reconfigurable computer architecture. Currently working on core FPGA projects at Vicharak for real-time data processing pipelines. Eager to work on cutting-edge FPGA/ASIC design projects, computer architecture.