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A Configurable High-Frequency SSB Signal Generation Method using SDR Approach Implemented on System-on-Chip FPGA

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Abstract – **System on Chip (SoC) has recently been shown as a new growth technology, which is expected to replace traditional method to design software-defined radio (SDR) systems. Due to the advantages SDR technique, the transceivers can process directly and flexibly the high-frequency (HF) signal in the digital domain. This signal then integrates with data processing software by employing standardized protocols. In this paper, we propose a method for generating the HF single-side band (SSB) signal using the SoC FPGA Altera DE10 platform based on the SDR technique. Implementation and experimental results of the SSB audio/voice signal have demonstrated that the proposed method is feasible for integration of designing the HF transceivers based on the SDR approach.**

Keywords – HF Communications, Single-Side Band, System on Chip, FPGA.

I. INTRODUCTION

The high-frequency communication system (HF band) performs receiving and transmitting signals through space by reflecting in the ionosphere [1], [2]. Density of electrons in the ionosphere varying with the solar cycle makes altitude of layers in the ionosphere change and become the semiconductor medium. When the HF waves reach the layers, they will be bent and reflected towards the ground, and keep being reflected on it. Therefore, the waves are reflected continuously. This characteristic helps to transmit waves in the ionosphere. Due to the wave propagation properties in the ionosphere as analyzed above, HF band can be transmitted for very long distance and used in coastal communications [3].

In recent years, the HF-SSBSC transceiver architecture has been developed on programmable hardware platform that includes a set of hardware and software platforms. With this platform, the functions of the radio systems are implemented with software and hardware which can be adjusted to work on programmable process techniques. HF-SSBSC communication systems can be used to replace satellite communication systems in case of no light-of-sight (LoS) for long distance propagation [4]. The next generation HF transceivers are designed and implemented on some modern technology platforms including FPGA, DSP, SOC and other programmable processors [5], [6]. The use of these technologies allows new radio features to be added to existing radio systems without requiring new hardware.

SDR technique plays an important role in the development of radio receivers by enhancing flexibility with programs, meeting standard compatibility and being able to flexibly customize functionality of the system [7]. In this study, we propose an approach of integrating Hard Processor System (HPS) with Linux operating system running on ARM chip to control signal processing modules on FPGA. This method can flexibly configurate parameters of signal processing modules at the high frequency in real-time manner. In addition, a human-machine interface software is developed by using the QT tool-based via graphic interfaces. To the best of our knowledge, the SSB signal generation method using SDR that is implemented on the SoC FPGA Altera DE10 has been not clarified in the literature. This is a potential approach that is likely to grow in both research and development as well as applied product development.

The remainder of the paper is organized as follows. Section II presents SSB modulation and DSS theories including methods to generate SSB modulated signal. Section III provides the proposed SSB signal generation method. The implementation and experimental results are presented and discussed in Section IV. The paper is concluded in Section V.

II. SSB MODULATION AND DSS THEORIES

A. SSB Modulation Methods

Amplitude modulation (AM) technology changes the amplitude of the carrier signal according to the amplitude of the information signals. The principle of AM is the process of multiplying a baseband signal with a sinusoidal HF carrier signal. A center frequency of the generated AM signal is the carrier frequency with varied amplitude. Single-sideband (SSB) modulation can be performed in three methods: band-pass filtering, phase shifting and Weaver method which is the hybrid approach. The first method is shown in Fig. 1. The modulation signal *m(t)* and the carrier frequency f_a are fed into the balance modulation. After the balance modulation, two sidebands are obtained. By using the BPF filter, the upper or lower sideband is selected. The analog audio signal at the modulator input can be expressed as

$$f_{voice}(t) = A_a \cos\left(\omega_a t + \varphi_a\right), \quad (1)$$

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where A_a and φ_a are the amplitude and the phase of the audio signal, respectively.

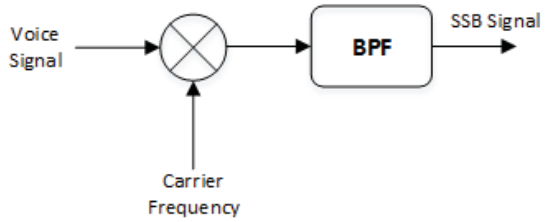


Fig. 1. Diagram of generating SSB signal using band-pass filtering

The DSB (Double-sideband) signal after multiplexed with the high-frequency signal is given by

$$\begin{aligned} f_{DSB}(t) &= A_a \cos(\omega_a t + \varphi_a) \times \cos(\omega_c t) \\ &= \frac{A_a}{2} \cos\left[(\omega_c + \omega_a)t + \varphi_a\right] \\ &+ \frac{A_a}{2} \cos\left[(\omega_c - \omega_a)t - \varphi_a\right]. \end{aligned} \quad (2)$$

SSB Signal then is created by using Band Pass Filter as shown in Figure 1. The SSB signal that uses the phase-shifting method, or the Hartley method is shown in Fig. 2. To generate an SSB signal using the Hartley method, two versions of the original signal are generated, mutually the phase 90^0 out of phase for any single frequency within the operating bandwidth. Each one of these signals then modulates carrier waves (of one frequency) that are also the phase 90^0 out of phase with each other. By either adding or subtracting the resulting signals, we have a lower or upper sideband signal.

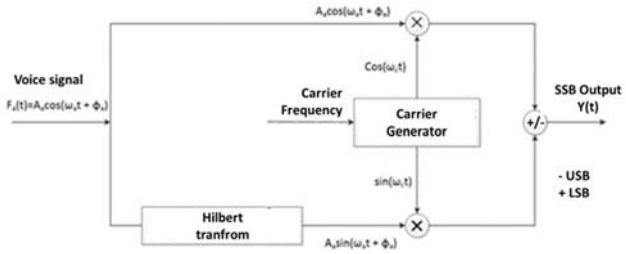


Fig.2. Generating SSB signal by the Hartley method

The SSB signal using the Weaver method is plotted in Fig. 3. The output signal of balance modulator 1 is

$$\begin{aligned} V_1 &= m(t)\sin\omega_0 t = V_m \cos\omega_m t.\sin\omega_0 t \\ &= \frac{V_m}{2}\left[\sin(\omega_0 + \omega_m)t + \sin(\omega_0 - \omega_m)t\right]. \end{aligned} \quad (3)$$

In the Eq. (3), by passing the LPF1, the remaining component becomes $\frac{V_m}{2}\sin(\omega_0 - \omega_m)t$.

The output signal of balance modulator 2 can be expressed as

$$\begin{aligned} V_2 &= m(t)\cos\omega_0 t = V_m \cos\omega_m t.\cos\omega_0 t \\ &= \left[\cos(\omega_0 + \omega_m)t + \cos(\omega_0 - \omega_m)t\right]. \end{aligned} \quad (4)$$

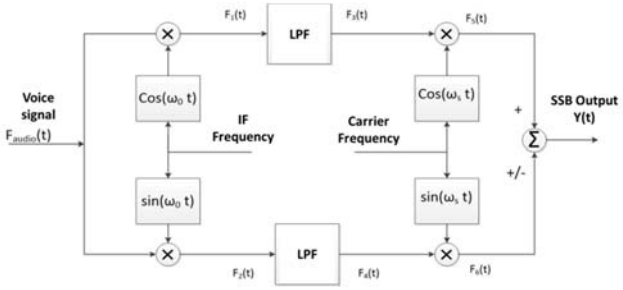


Fig. 3. Generating SSB signal by the Weaver method

In case of the LPF2, the remaining component is $\frac{V_m}{2}\cos(\omega_0 - \omega_m)t$. The output signal of balance modulator 3 is given by

$$\begin{aligned} V_3 &= \sin(\omega_0 - \omega_m)t.\sin(\omega_c t) \\ &= \left[\cos(\omega_c - \omega_0 + \omega_m)t - \cos(\omega_c + \omega_0 - \omega_m)t\right]. \end{aligned} \quad (5)$$

The output signal of balance modulator 4 is expressed as

$$\begin{aligned} V_4 &= \cos(\omega_0 - \omega_m)t.\cos(\omega_c t) \\ &= \left[\cos(\omega_c + \omega_0 - \omega_m)t + \cos(\omega_c - \omega_0 + \omega_m)t\right]. \end{aligned} \quad (6)$$

The SSB signal generated by the adders of V3 and V4 is expressed as

$$V_{SSB} = V_3 + V_4 = \cos(\omega_c - \omega_0 + \omega_m)t. \quad (7)$$

B. HF Generation using DDS

Direct digital synthesis (DDS) is a technique widely used in the generation of radio frequency signals for use in a variety of applications from radio receivers to signal generators.

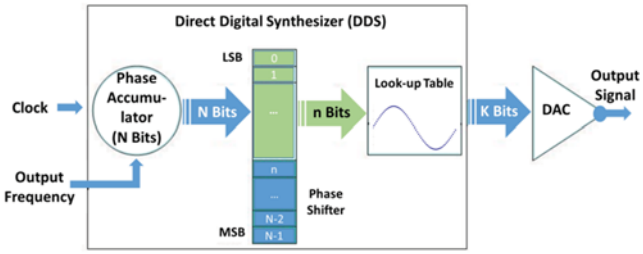
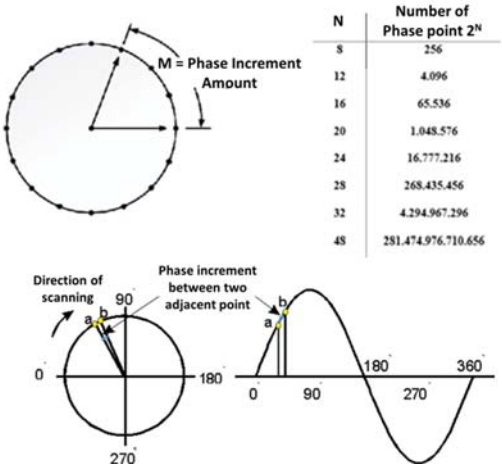


Fig.4. A block diagram of the basic direct digital synthesizer

A direct digital synthesizer operates by storing the points of a waveform in digital format, and then recalling them to generate the waveform. The rate at which the synthesizer completes one waveform then governs the frequency. The block diagram of a basic DDS is illustrated in Fig. 4. The operation can be envisaged more easily by looking at the way that phases progresses over the course of one cycle of the waveform. This can be envisaged as the phase progressing around a circle. As the phase advances around the circle, this corresponds to advances in the waveform. The synthesizer operates by storing various points in the waveform in digital form and then recalling them to generate the waveform. Its

operation can be explained in more detail by considering the phase advances around a circle as shown in Fig. 5.



N	Number of Phase point 2^N
8	256
12	4.096
16	65.536
20	1.048.576
24	16.777.216
28	268.435.456
32	4.294.967.296
48	281.474.976.710.656

Fig. 5. Principle of generating DDS Signal

As the phase advances around the circle this corresponds to advances in the waveform, i.e. the greater the number corresponding to the phase, the greater the point is along the waveform. By successively advancing the number corresponding to the phase it is possible to move further along the waveform cycle. The digital number representing the phase is held in the phase accumulator. The number held here corresponds to the phase and is increased at regular intervals. In this way it can be sent hat the phase accumulator is basically a form of counter. When it is clocked it adds a preset number to the one already held. When it fills up, it resets and starts counting from zero again. This corresponds to reaching one complete circle on the phase diagram and restarting again.

III. The Proposed SSB Signal Generation Method

The SDR approach is used to create the SSB modulated signals highly flexible and highly customizable. The proposed execution model is shown in Fig. 6 and Fig.7. The operation parameters such as HF operating frequencies or the SSB modulation mode can be configured flexibly through the Human Machine Interface (HMI) running on the Linux operating system on Hard Processor System (HPS) of the FPGA DE10-SoC. By using the HMI program, controlling commands interact with the signal generator on the FPGA through changing the step coefficient value of the DDS frequency synthesizer to generate the required signal frequency.

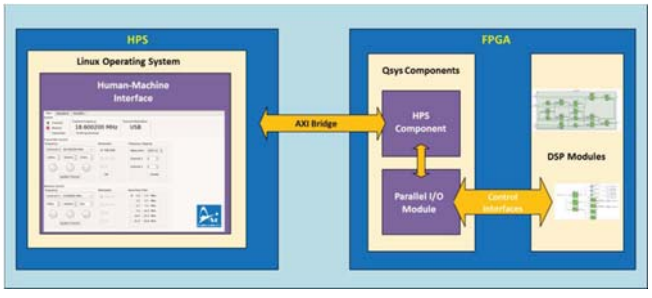


Fig. 6. The proposed model for SSB Sig-Gen on FPGA SoC

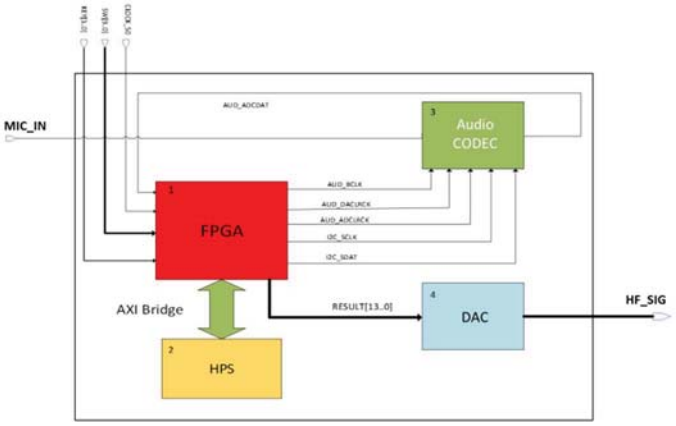


Fig. 7. Block diagram of SSB Sig-Gen on SoC FPGA

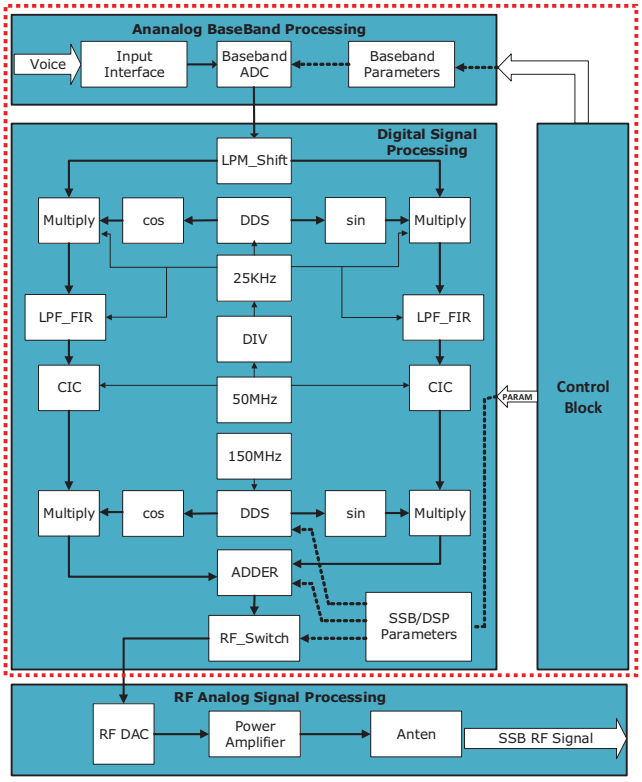


Fig. 8. The detail diagram of SSB Sig-Gen on SoC FPGA

HMI software is developed using the QT programming language and runs on the Lightweight X11 Desktop Environment (LXDE) Linux. LXDE is designed to run on computers with limited hardware configurations such as laptops or embedded PCs. On the DE10 Kit, LXDE Linux is the environment supported by Terasic manufacturer. The QT library packages are also installed in the operating system environment. Therefore, software development based on Qt-FrameWork is easier to develop with support from the manufacturer. The system architecture for the HF SSB signal is illustrated in the Fig. 8. The audio/voice signal is processed by the AudioCODEC module then modulated by the digital processing part to create SSB signal by the FPGA. This signal is then passed to DAC to convert the analog high-

frequency signal. The process of signal generation based on FPGA is controlled by control block which is implemented on HPS and will be presented in the next section.

IV. Implementation and Experimental Results

A. Implementation on Altera SoC DE10 FPGA Platform

Fig.9 shows the diagram of SSB signal generation process with configurable parameters is implemented on AlteraCyclone V SoC DE10 FPGA.The SoC DE10 FPGA includes an integrated hard processor system (HPS) – consisting of processors, peripherals, and memory controller – with the FPGA fabric using a high-bandwidth interconnect backbone. The combination of the HPS with Intel's 28 nm low-power FPGA fabric provide the performance and ecosystem of an applications-class ARM processor with the flexibility, low cost, and low power consumption of the Cyclone V SoC FPGAs [8].

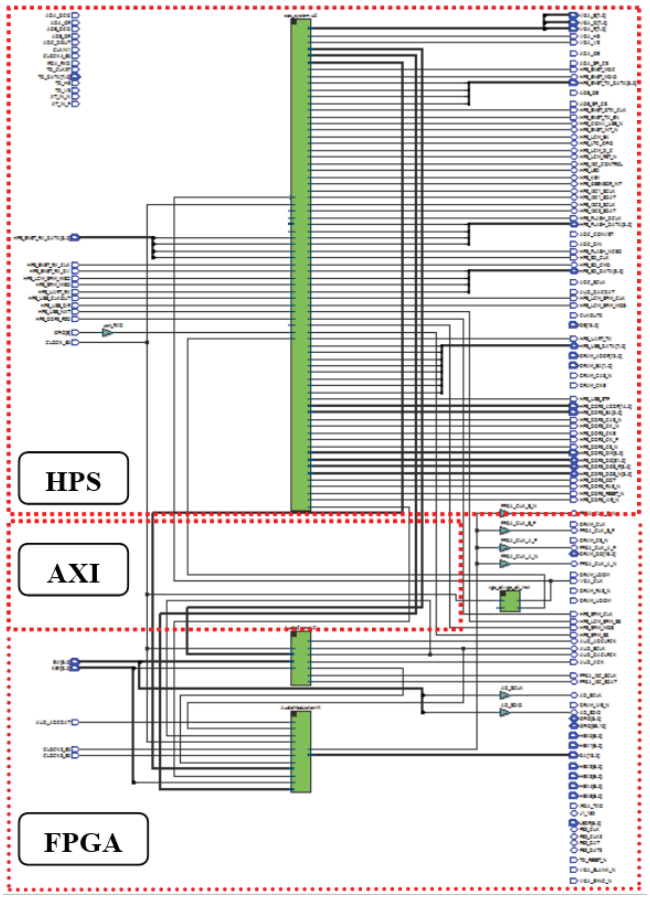


Fig. 9. NetList of control and processing parts on HPS and FPGA

A schematic diagram of blocks in the digital processing block on the FPGA is shown in Fig. 9. The audio signal goes to Micro/Line-in on the FPGA kit to generate audio sample stream then coded with the specific bit length. Base-band signal samples are then multiplied with intermediate frequency signal and finally passed to digital processing modulation. Discrete modulated HF signal samples are converted into analog form using a 14-bit Digital to Analog (D/A) converter channel with 250 MSPS which is fully compatible with Altera SoC FPGA Development boards [9]. The modulated signal goes through the DAC port connecting to the antenna to emit the SSB signal in form of radio wave energy.

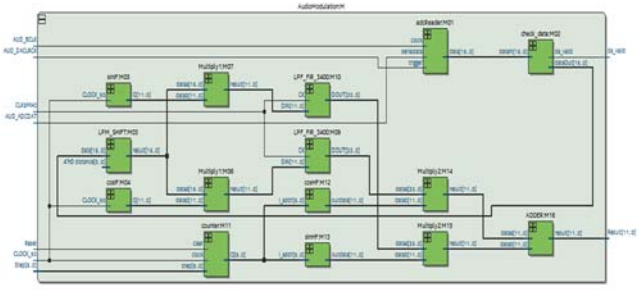


Fig. 10. SSB signal processing implemented on FPGA SoC

The AUD_ADCDAT input is an analogue power source with a frequency of 20-16kHz applied to the adcReader module to convert it into a digital signal corresponding to 16 bits data samples. In fact, the input signal strength is from -6dB to 34dB. It can be sampled in various quantities for different frequencies such as 8kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz and 96kHz over the corresponding number of encoded bits of 12, 16, 24, 32. The signal samples are then multiplied by NCOcosIF and NCOsinIF carriers and then filtered to produce two 90^0-degree phase difference signals. These signals are further multiplied by the high-frequency carrier corresponding to Sine and Cosine. The SSB single-band signal is formed through the two high-frequency multiplier output signals. Numerical digital oscillators use a chip pulse of 50 and 150 MHz to generate two intermediate carriers of cos_2K and sin_2K as well as orthogonal carriers at various HF frequencies, as shown in Fig. 10.

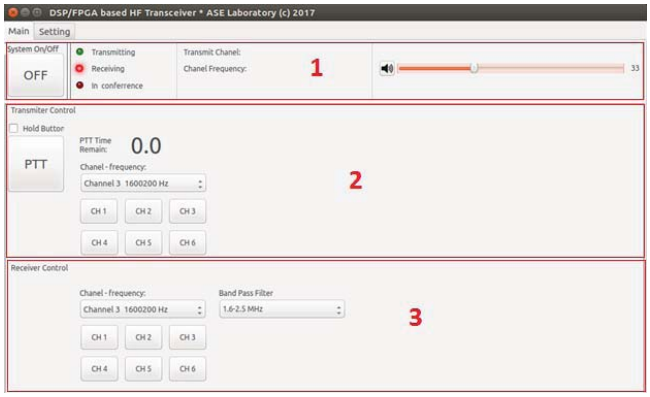


Fig. 11. SSB signal control software implemented on HPS

The software installed on HPS (Fig. 11) controls the operations of the signal processing unit on the FPGA via Advanced Extensible Interface (AXI) Interface. It includes basic functions designed for user friendly in operation. These functions are divided into three areas:

1. The general functional area (number 1 in Fig. 11) includes: On/Off button; Operational status light

(receiver / transmitter); Displays the using channel and frequency; Volume control slider.

2. The transmit control area (number 2 in Fig. 11) includes: PTT Button (Push-To-Talk) and checkbox Hold Button: The default system operates in the receive mode. Hold down will switch the system operation mode to the capture mode until the hold or time out. Users can check the box Hold Button to keep the playback mode when pressing the PTT button. Labels display the remaining countdown time in playback mode before switching to the recording mode (60 seconds in default). The channel selection panel corresponds to the installed frequencies in a total of 51 channels (from Channel 0 to Channel 50). Frequent channel selection buttons have been set (from CH 1 to CH 6).
3. The receiver control area (number 3 in Fig. 11) includes: The channel selection panel corresponds to the installed frequencies in a total of 51 channels (from Channel 0 to Channel 50). Frequent channel selector buttons (CH) are set (from CH 1 to CH 6). The frequency band selection for the band-pass filter at the receiver input.

B. *Experimants and Results*

The experimental model is carried out under the scenario of signal generation function with the standard signal test and measurement of the Aeroflex 3920 equipment [10]. The system model and the test case are shown in Fig. 12.

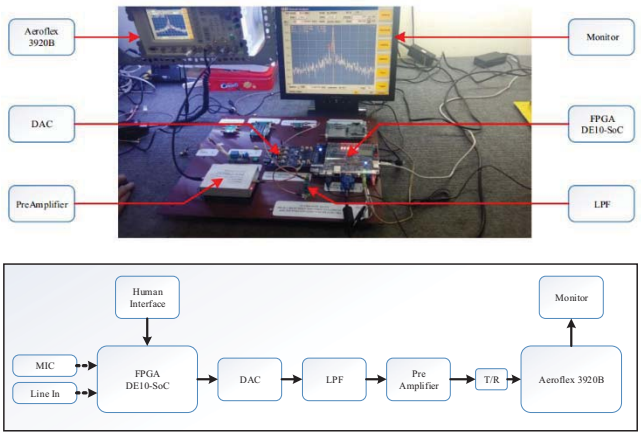
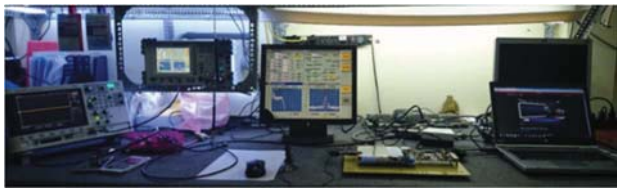
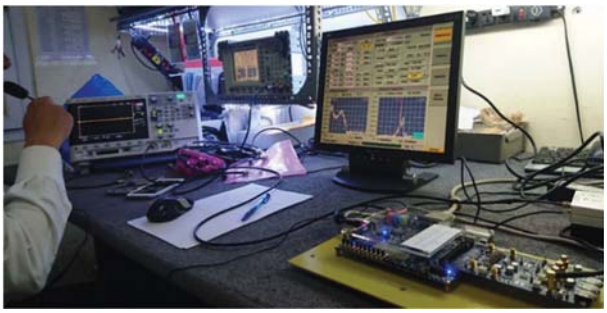


Fig. 12. The testing model for SSB signal generation

The testing model shown in Fig. 12 consists of following main components: Signal sources, Altera FPGA DE10-SoC, Data Conversion High-Speed Mezzanine Card (HSMC), antenna, and cables. Audio/Voice data can be fed from two different sources which are (1) from pre-stored files to enter line-in port or (2) voice signal captured from micro in real-time manner. The input data is sampled by a built-in audio CODEC and send to signal processing modules implemented on FPGA to modulate by SSB methods. The SSB modulated signal going in to HSMC card to convert into analog signal then run through HF amplifier to feed antenna or RF cable connected to measurement devices or receivers. The transmitter side includes: (1) FPGA DE10-SoC: voice/audio signal processing and upconvert to high frequency; (2) DAC: Digital to Analog converter; (3) Low Pass Filter; (4) PreAmplifier; (5) Human-Machine Interface; (6) MIC/Line In port. The receiver side includes: (1) Aeroflex 3920B for analyze and demodulation SSB signal and output voice/audio signal via built-in speakers; (2) Monitor for display signal wave from and spectrum; (3) T/R signal ports. Experimental operation procedures include: Check to confirm tight connection between functional blocks. Select transmit frequency and port for input signal (Micor Line-In). Fig. 13 show the two testing scenarios with different input signal sources. Select frequency and operation mode for receiver. Power on the testing system. Observe the signal displayed on the Monitor. Capture experimental data for each testing scenario. In Figs. 13 and 14, experimental results have shown that HF signals have been generated in the HF band with changing the signal's phase as required for the Sine and Cosine carriers.



(a) Voice signal from pre-stored file



(b) Real-time Signal captured from micro

Fig 13: Testing scenario with different input signal sources

(a) Sine wave form

(b) Cosine wave form

Fig. 14. Wave forms of generated carrier frequency of 7.936MHz

The tested results generate and transmit HF signals by means of SSB modulation with transmit frequency can be configured flexibly by software. The real system can recover voice messages and ensures that the receiving and demodulating side of the sound quality is stable and clear comparing to the original signal from the transmitter. The results obtained with the use of the Aeroflex 3920 standard gauge as well as the use of the SDR receiver shown in Figures 15 and 17 illustrate the feasibility of the

proposed SSB signaling model and the implementation on the SoC FPGA. The experimental results indicated in Aeroflex 3920B show SSB channel bandwidth vary from about 200 KHz to 160 KHzwith SSB signal spectrum for modulated scenarios for baseband signal of sine tone 1KHz (see Fig. 15) and voice signal (see Fig. 16). Fig. 17 shows the spectrum of voice baseband signal which is recovered at the Aeroflex 3920B. The quality of recovered voice is good with frequencies of baseband signal varies within 4KHz as displayed on Aeroflex 3920B's screen.

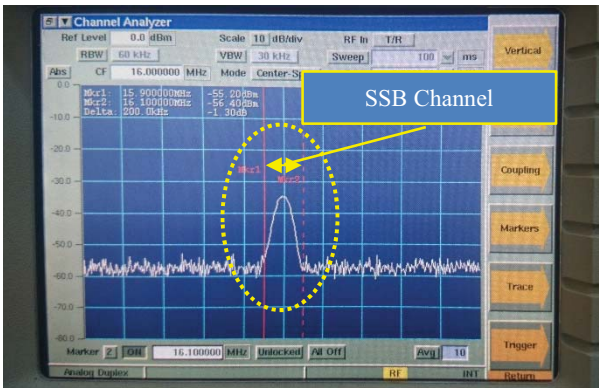


Fig. 15. The SSB signal spectrum of modulated sine tone

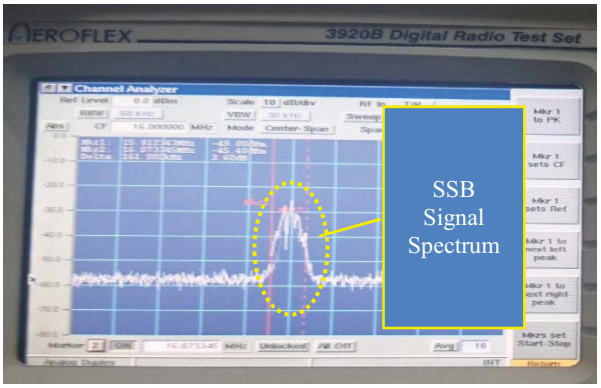


Fig. 16. The SSB signal spectrum of modulated voice

Fig. 17. The recovered voice baseband spectrum

V. CONCLUSION

This work has presented the methodology for generating configurable high frequency single-side band signal which is implemented on the Altera DE10 System on Chip FPGA platform. Experimental results demonstrate that the proposed solution is feasible for integration into SSB short-wave transceivers designing based on SDR approach. Further research will be centered on field testing as well as supplement communication security capability such as frequency hopping feature through the HF radio channels.

ACKNOWLEDGMENT

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