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Lab 3

Part 2

```
## Switches
set_property PACKAGE_PIN V17 [get_ports {c}]
        set_property IOSTANDARD LVCMOS33 [get_ports {c}]
set_property PACKAGE_PIN V16 [get_ports {b}]
        set_property IOSTANDARD LVCMOS33 [get_ports {b}]
set_property PACKAGE_PIN W16 [get_ports {a}]
        set_property IOSTANDARD LVCMOS33 [get_ports {a}]
set_property PACKAGE_PIN W13 [get_ports {e}]
        set_property IOSTANDARD LVCMOS33 [get_ports {e}]
## LEDs
set_property PACKAGE_PIN U16 [get_ports {d0}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d0}]
set_property PACKAGE_PIN E19 [get_ports {d1}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d1}]
set_property PACKAGE_PIN U19 [get_ports {d2}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d2}]
set_property PACKAGE_PIN V19 [get_ports {d3}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d3}]
set_property PACKAGE_PIN W18 [get_ports {d4}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d4}]
set_property PACKAGE_PIN U15 [get_ports {d5}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d5}]
set_property PACKAGE_PIN U14 [get_ports {d6}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d6}]
set_property PACKAGE_PIN V14 [get_ports {d7}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d7}]
```

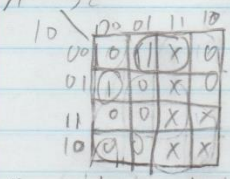
Part 3

Truth table

$x_3x_2x_1x_0$	A	B	C	D	E	F	G	DP	AN0	AN1	AN2	AN3
0000	0	0	0	0	0	0	1	1	0	1	1	1
0001	1	0	0	1	1	1	1	1	0	1	1	1
0010	0	0	1	0	0	1	0	1	0	1	1	1
0011	0	0	0	0	1	1	0	1	0	1	1	1
0100	1	0	0	1	1	0	0	1	0	1	1	1
0101	0	1	0	0	1	0	0	1	0	1	1	1
0110	0	1	0	0	0	0	0	1	0	1	1	1
0111	0	0	0	1	1	1	1	1	0	1	1	1
1000	0	0	0	0	0	0	0	1	0	1	1	1
1001	0	0	0	0	1	0	0	1	0	1	1	1
1010	x	x	x	x	x	x	x	x	1	1	1	1
1011	x	x	x	x	x	x	x	x	1	1	1	1
1100	x	x	x	x	x	x	x	x	1	1	1	1
1101	x	x	x	x	x	x	x	x	1	1	1	1
1110	x	x	x	x	x	x	x	x	1	1	1	1
1111	x	x	x	x	x	x	x	x	1	1	1	1

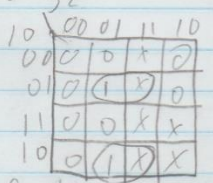
K maps

A



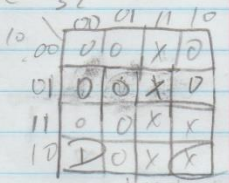
$A = x_2x_1'x_0' + x_3'x_2'x_1'x_0$

B



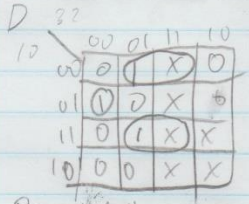
$B = x_2x_1'x_0 + x_2x_1x_0'$

C



$C = x_2'x_1x_0'$

D

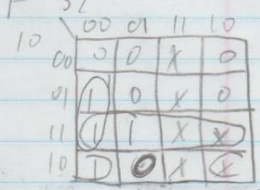


$D = x_2x_1'x_0' + x_2'x_1x_0 + x_3'x_2'x_1'x_0$

E

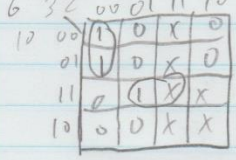
$E = x_2x_1' + x_0'$

F



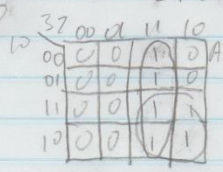
$F = x_1x_0 + x_2'x_1x_0' + x_3'x_2'x_0$

G

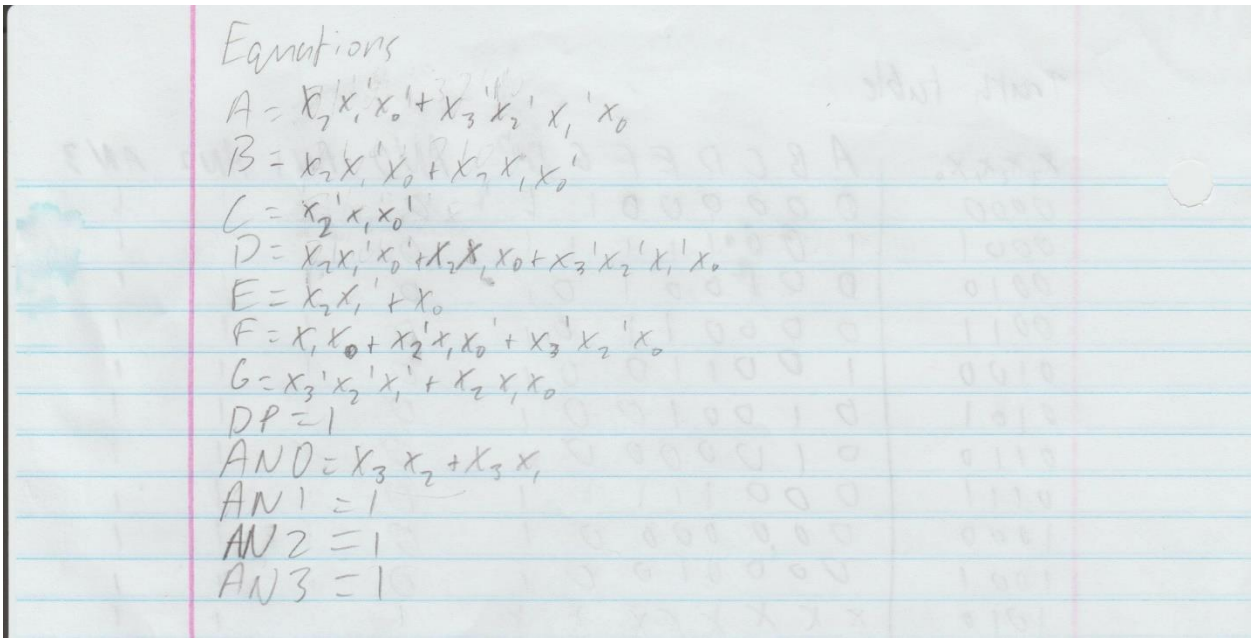


$G = x_3'x_2'x_1' + x_2x_1x_0$

AN0



$AN0 = x_3x_2 + x_1x_0$




```
module BCD_to_7segment(
   input x0,
   input x1,
   input x2,
   input x3,
   output a,
   output b,
   output c,
   output d,
   output e,
   output f,
   output g,
   output dp,
   output an0,
   output an1,
   output an2,
   output an3
   );

   wire x0_not, x1_not, x2_not, x3_not;
   wire a0, a1, b0, b1, d0, d1, d2, e0, f0, f1, f2, g0, g1, an00, an01, high;

   not n0 (x0_not, x0);
   not n1 (x1_not, x1);
   not n2 (x2_not, x2);
   not n3 (x3_not, x3);

   and h0 (a0, x2, x1_not, x0_not);
   and h1 (a1, x3_not, x2_not, x1_not, x0);
```

```
    or h3 (a, a0, a1);
    and h4 (b0, x2, x1_not, x0);
    and h5 (b1, x2, x1, x0_not);
    or h6 (b, b0, b1);
    and h7 (c, x2_not, x1, x0_not);
    and h8 (d0, x2, x1_not, x0_not);
    and h9 (d1, x2, x1, x0);
    and h10 (d2, x3_not, x2_not, x1_not, x0);
    or h11 (d, d2, d1, d0);
    and h12 (e0, x2, x1_not);
    or h13 (e, e0, x0);
    and h14 (f0, x1, x0);
    and h15 (f1, x2_not, x1, x0_not);
    and h16 (f2, x3_not, x2_not, x0);
    or h17 (f, f0, f1, f2);
    and h18 (g0, x3_not, x2_not, x1_not);
    and h19 (g1, x2, x1, x0);
    or h20 (g, g0, g1);
    and h21 (an00, x3, x2);
    and h22 (an01, x3, x1);
    or h23 (an0, an00, an01);
    or h24 (dp, x0, x0_not);
    or h25 (an1, x0, x0_not);
    or h26 (an2, x0, x0_not);
    or h27 (an3, x0, x0_not);

endmodule

module tb_BCD_to_7segment;
    reg x0;
    reg x1;
    reg x2;
    reg x3;
    wire a;
    wire b;
    wire c;
    wire d;
    wire e;
    wire f;
    wire g;
    wire dp;
    wire an0;
    wire an1;
    wire an2;
    wire an3;

    BCD_to_7segment uut (
        .x0(x0),
```

```
    .x1(x1),
    .x2(x2),
    .x3(x3),
    .a(a),
    .b(b),
    .c(c),
    .d(d),
    .e(e),
    .f(f),
    .g(g),
    .dp(dp),
    .an0(an0),
    .an1(an1),
    .an2(an2),
    .an3(an3)
);

initial begin

    x0 = 0;
    x1 = 0;
    x2 = 0;
    x3 = 0;

    #50;

    x0 = 1;
    x1 = 0;
    x2 = 0;
    x3 = 0;
    #50;

    x0 = 0;
    x1 = 1;
    x2 = 0;
    x3 = 0;
    #50;

    x0 = 1;
    x1 = 1;
    x2 = 0;
    x3 = 0;
    #50;

    x0 = 0;
    x1 = 0;
    x2 = 1;
    x3 = 0;
```

```
#50;

x0 = 1;
x1 = 0;
x2 = 1;
x3 = 0;
#50;

x0 = 0;
x1 = 1;
x2 = 1;
x3 = 0;
#50;

x0 = 1;
x1 = 1;
x2 = 1;
x3 = 0;
#50;

x0 = 0;
x1 = 0;
x2 = 0;
x3 = 1;
#50;

x0 = 1;
x1 = 0;
x2 = 0;
x3 = 1;
#50;

x0 = 0;
x1 = 1;
x2 = 0;
x3 = 1;
#50;

x0 = 1;
x1 = 1;
x2 = 0;
x3 = 1;
#50;

x0 = 0;
x1 = 0;
x2 = 1;
x3 = 1;
```

```
        #50;

        x0 = 1;
        x1 = 0;
        x2 = 1;
        x3 = 1;
        #50;

        x0 = 0;
        x1 = 1;
        x2 = 1;
        x3 = 1;
        #50;

        x0 = 1;
        x1 = 1;
        x2 = 1;
        x3 = 1;
        #50;


        end

endmodule
```


```
## Switches
set_property PACKAGE_PIN V17 [get_ports {x0}]
        set_property IOSTANDARD LVCMOS33 [get_ports {x0}]
set_property PACKAGE_PIN V16 [get_ports {x1}]
```

```
        set_property IOSTANDARD LVCMOS33 [get_ports {x1}]
set_property PACKAGE_PIN W16 [get_ports {x2}]
        set_property IOSTANDARD LVCMOS33 [get_ports {x2}]
set_property PACKAGE_PIN W17 [get_ports {x3}]
        set_property IOSTANDARD LVCMOS33 [get_ports {x3}]
set_property PACKAGE_PIN W15 [get_ports {x4}]
        set_property IOSTANDARD LVCMOS33 [get_ports {x4}]
##7 segment display
set_property PACKAGE_PIN W7 [get_ports {a}]
        set_property IOSTANDARD LVCMOS33 [get_ports {a}]
set_property PACKAGE_PIN W6 [get_ports {b}]
        set_property IOSTANDARD LVCMOS33 [get_ports {b}]
set_property PACKAGE_PIN U8 [get_ports {c}]
        set_property IOSTANDARD LVCMOS33 [get_ports {c}]
set_property PACKAGE_PIN V8 [get_ports {d}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d}]
set_property PACKAGE_PIN U5 [get_ports {e}]
        set_property IOSTANDARD LVCMOS33 [get_ports {e}]
set_property PACKAGE_PIN V5 [get_ports {f}]
        set_property IOSTANDARD LVCMOS33 [get_ports {f}]
set_property PACKAGE_PIN U7 [get_ports {g}]
        set_property IOSTANDARD LVCMOS33 [get_ports {g}]

set_property PACKAGE_PIN V7 [get_ports dp]
        set_property IOSTANDARD LVCMOS33 [get_ports dp]

set_property PACKAGE_PIN U2 [get_ports {an0}]
        set_property IOSTANDARD LVCMOS33 [get_ports {an0}]
set_property PACKAGE_PIN U4 [get_ports {an1}]
        set_property IOSTANDARD LVCMOS33 [get_ports {an1}]
set_property PACKAGE_PIN V4 [get_ports {an2}]
        set_property IOSTANDARD LVCMOS33 [get_ports {an2}]
set_property PACKAGE_PIN W4 [get_ports {an3}]
        set_property IOSTANDARD LVCMOS33 [get_ports {an3}]
```