Noah Kessler

Lab 3

Part 2

## Switches

set\_property PACKAGE\_PIN V17 [get\_ports {c}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {c}]

set\_property PACKAGE\_PIN V16 [get\_ports {b}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {b}]

set\_property PACKAGE\_PIN W16 [get\_ports {a}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {a}]

set\_property PACKAGE\_PIN W13 [get\_ports {e}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {e}]

## LEDs

set\_property PACKAGE\_PIN U16 [get\_ports {d0}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {d0}]

set\_property PACKAGE\_PIN E19 [get\_ports {d1}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {d1}]

set\_property PACKAGE\_PIN U19 [get\_ports {d2}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {d2}]

set\_property PACKAGE\_PIN V19 [get\_ports {d3}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {d3}]

set\_property PACKAGE\_PIN W18 [get\_ports {d4}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {d4}]

set\_property PACKAGE\_PIN U15 [get\_ports {d5}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {d5}]

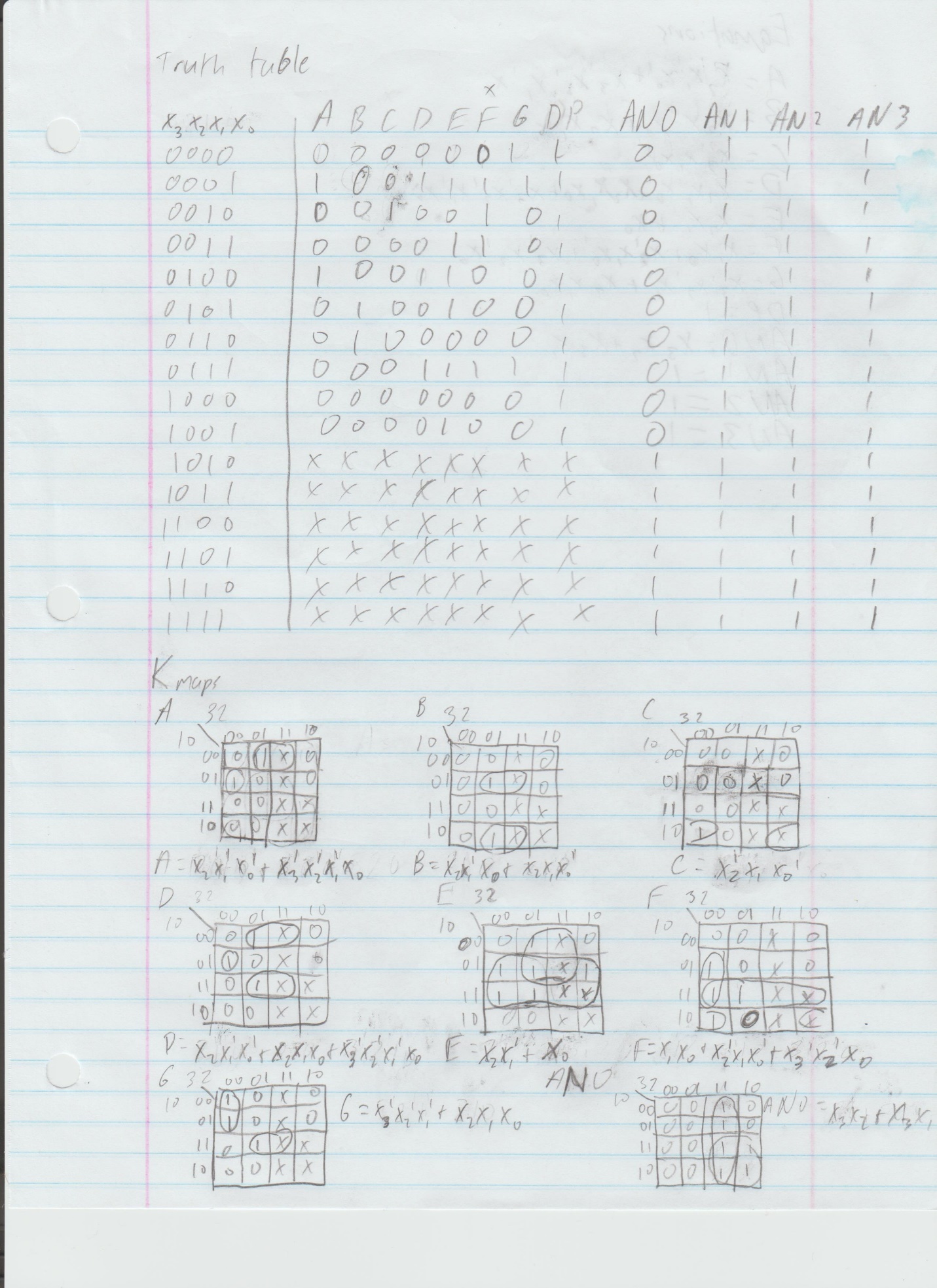
set\_property PACKAGE\_PIN U14 [get\_ports {d6}]

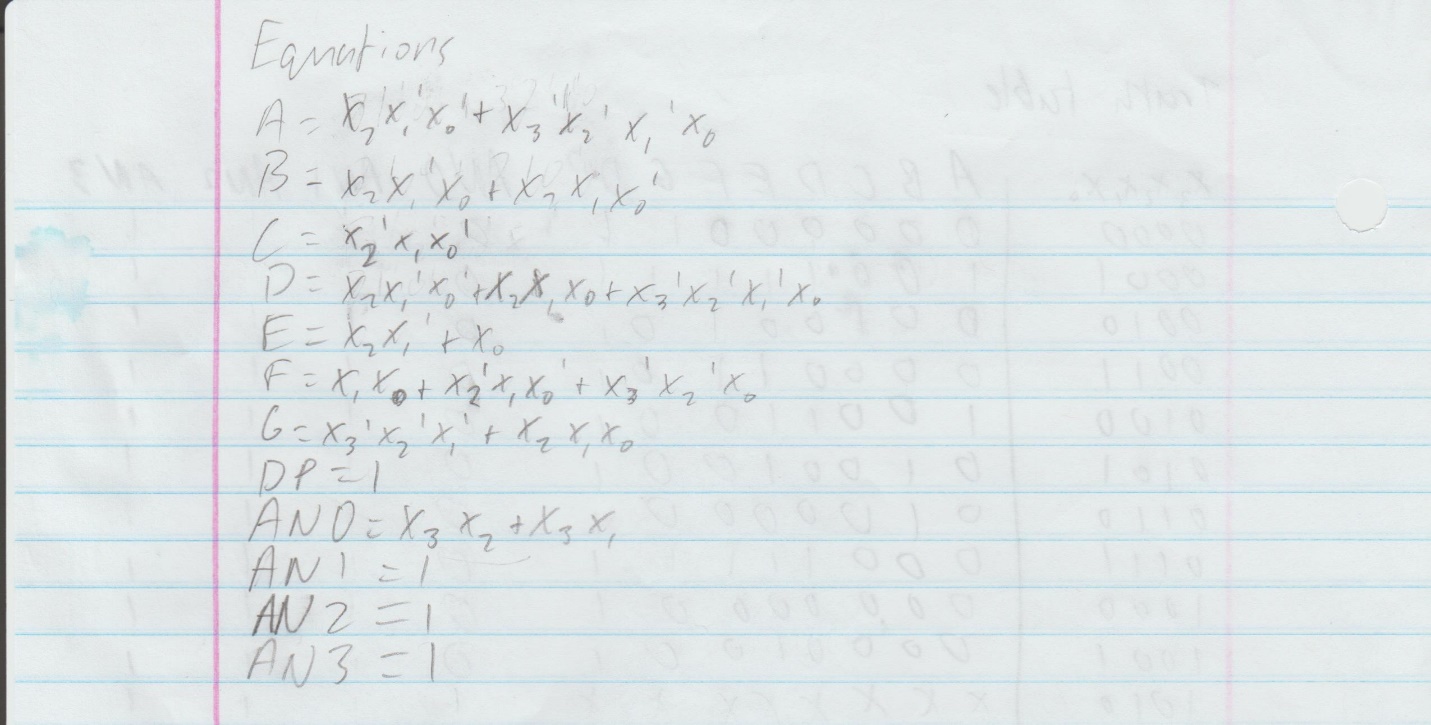
set\_property IOSTANDARD LVCMOS33 [get\_ports {d6}]

set\_property PACKAGE\_PIN V14 [get\_ports {d7}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {d7}]

Part 3





module BCD\_to\_7segment(

input x0,

input x1,

input x2,

input x3,

output a,

output b,

output c,

output d,

output e,

output f,

output g,

output dp,

output an0,

output an1,

output an2,

output an3

);

wire x0\_not, x1\_not, x2\_not, x3\_not;

wire a0, a1, b0, b1, d0, d1, d2, e0, f0, f1, f2, g0, g1, an00, an01, high;

not n0 (x0\_not, x0);

not n1 (x1\_not, x1);

not n2 (x2\_not, x2);

not n3 (x3\_not, x3);

and h0 (a0, x2, x1\_not, x0\_not);

and h1 (a1, x3\_not, x2\_not, x1\_not, x0);

or h3 (a, a0, a1);

and h4 (b0, x2, x1\_not, x0);

and h5 (b1, x2, x1, x0\_not);

or h6 (b, b0, b1);

and h7 (c, x2\_not, x1, x0\_not);

and h8 (d0, x2, x1\_not, x0\_not);

and h9 (d1, x2, x1, x0);

and h10 (d2, x3\_not, x2\_not, x1\_not, x0);

or h11 (d, d2, d1, d0);

and h12 (e0, x2, x1\_not);

or h13 (e, e0, x0);

and h14 (f0, x1, x0);

and h15 (f1, x2\_not, x1, x0\_not);

and h16 (f2, x3\_not, x2\_not, x0);

or h17 (f, f0, f1, f2);

and h18 (g0, x3\_not, x2\_not, x1\_not);

and h19 (g1, x2, x1, x0);

or h20 (g, g0, g1);

and h21 (an00, x3, x2);

and h22 (an01, x3, x1);

or h23 (an0, an00, an01);

or h24 (dp, x0, x0\_not);

or h25 (an1, x0, x0\_not);

or h26 (an2, x0, x0\_not);

or h27 (an3, x0, x0\_not);

endmodule

module tb\_BCD\_to\_7segment;

reg x0;

reg x1;

reg x2;

reg x3;

wire a;

wire b;

wire c;

wire d;

wire e;

wire f;

wire g;

wire dp;

wire an0;

wire an1;

wire an2;

wire an3;

BCD\_to\_7segment uut (

.x0(x0),

.x1(x1),

.x2(x2),

.x3(x3),

.a(a),

.b(b),

.c(c),

.d(d),

.e(e),

.f(f),

.g(g),

.dp(dp),

.an0(an0),

.an1(an1),

.an2(an2),

.an3(an3)

);

initial begin

x0 = 0;

x1 = 0;

x2 = 0;

x3 = 0;

#50;

x0 = 1;

x1 = 0;

x2 = 0;

x3 = 0;

#50;

x0 = 0;

x1 = 1;

x2 = 0;

x3 = 0;

#50;

x0 = 1;

x1 = 1;

x2 = 0;

x3 = 0;

#50;

x0 = 0;

x1 = 0;

x2 = 1;

x3 = 0;

#50;

x0 = 1;

x1 = 0;

x2 = 1;

x3 = 0;

#50;

x0 = 0;

x1 = 1;

x2 = 1;

x3 = 0;

#50;

x0 = 1;

x1 = 1;

x2 = 1;

x3 = 0;

#50;

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x3 = 1;

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x2 = 1;

x3 = 1;

#50;

x0 = 1;

x1 = 0;

x2 = 1;

x3 = 1;

#50;

x0 = 0;

x1 = 1;

x2 = 1;

x3 = 1;

#50;

x0 = 1;

x1 = 1;

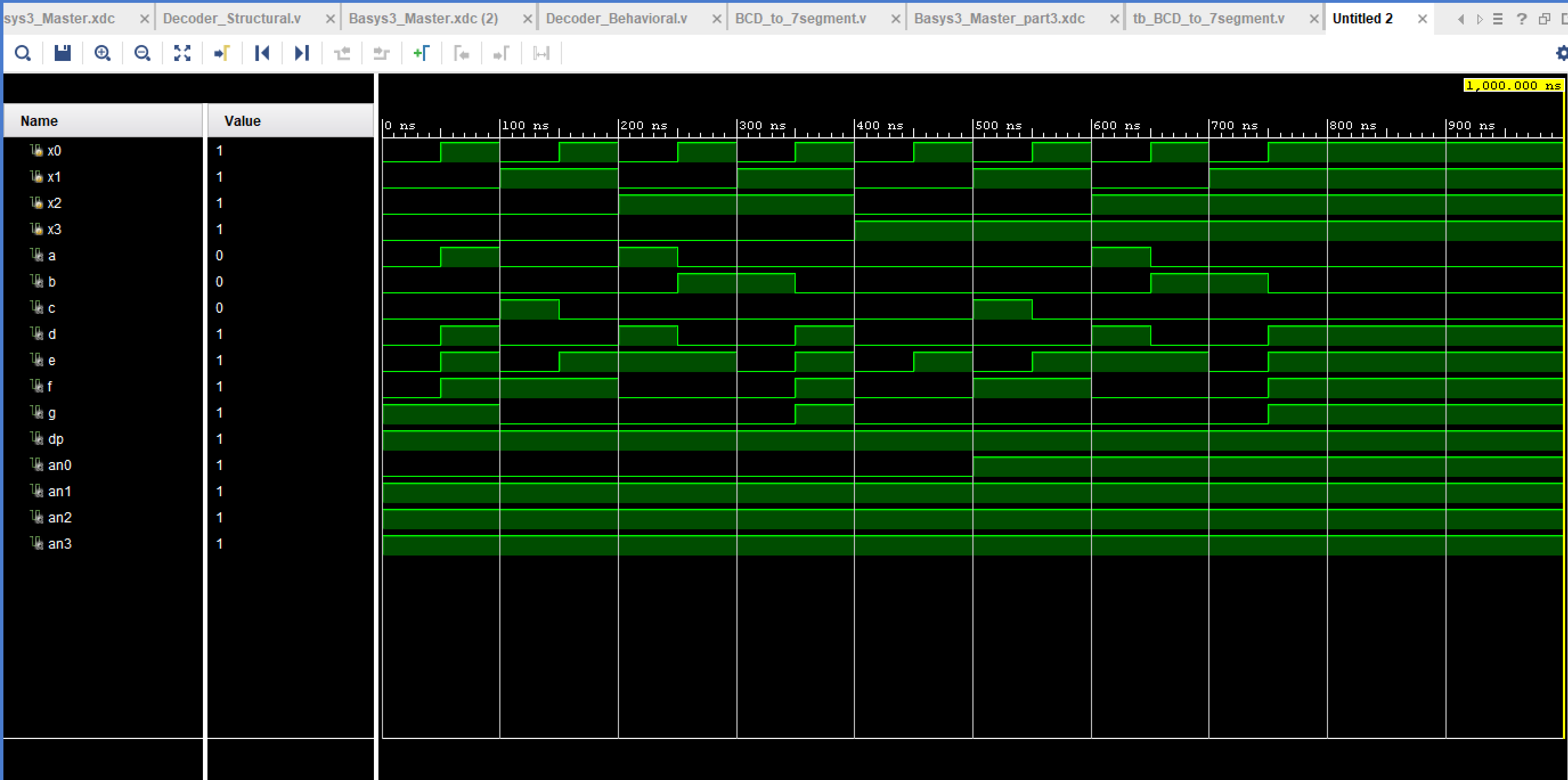
x2 = 1;

x3 = 1;

#50;

end

endmodule



## Switches

set\_property PACKAGE\_PIN V17 [get\_ports {x0}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {x0}]

set\_property PACKAGE\_PIN V16 [get\_ports {x1}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {x1}]

set\_property PACKAGE\_PIN W16 [get\_ports {x2}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {x2}]

set\_property PACKAGE\_PIN W17 [get\_ports {x3}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {x3}]

set\_property PACKAGE\_PIN W15 [get\_ports {x4}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {x4}]

##7 segment display

set\_property PACKAGE\_PIN W7 [get\_ports {a}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {a}]

set\_property PACKAGE\_PIN W6 [get\_ports {b}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {b}]

set\_property PACKAGE\_PIN U8 [get\_ports {c}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {c}]

set\_property PACKAGE\_PIN V8 [get\_ports {d}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {d}]

set\_property PACKAGE\_PIN U5 [get\_ports {e}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {e}]

set\_property PACKAGE\_PIN V5 [get\_ports {f}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {f}]

set\_property PACKAGE\_PIN U7 [get\_ports {g}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {g}]

set\_property PACKAGE\_PIN V7 [get\_ports dp]

set\_property IOSTANDARD LVCMOS33 [get\_ports dp]

set\_property PACKAGE\_PIN U2 [get\_ports {an0}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an0}]

set\_property PACKAGE\_PIN U4 [get\_ports {an1}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an1}]

set\_property PACKAGE\_PIN V4 [get\_ports {an2}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an2}]

set\_property PACKAGE\_PIN W4 [get\_ports {an3}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an3}]