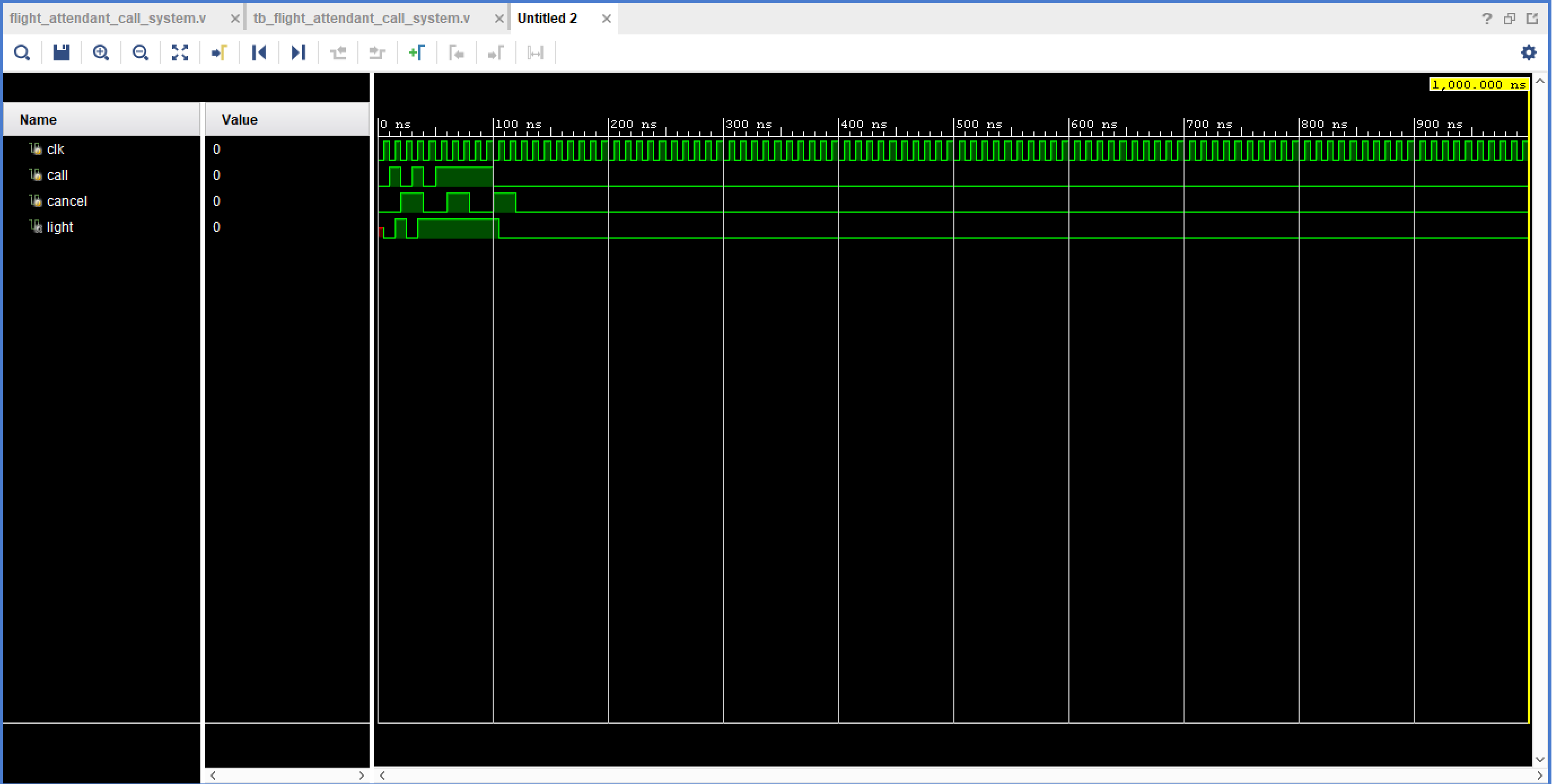
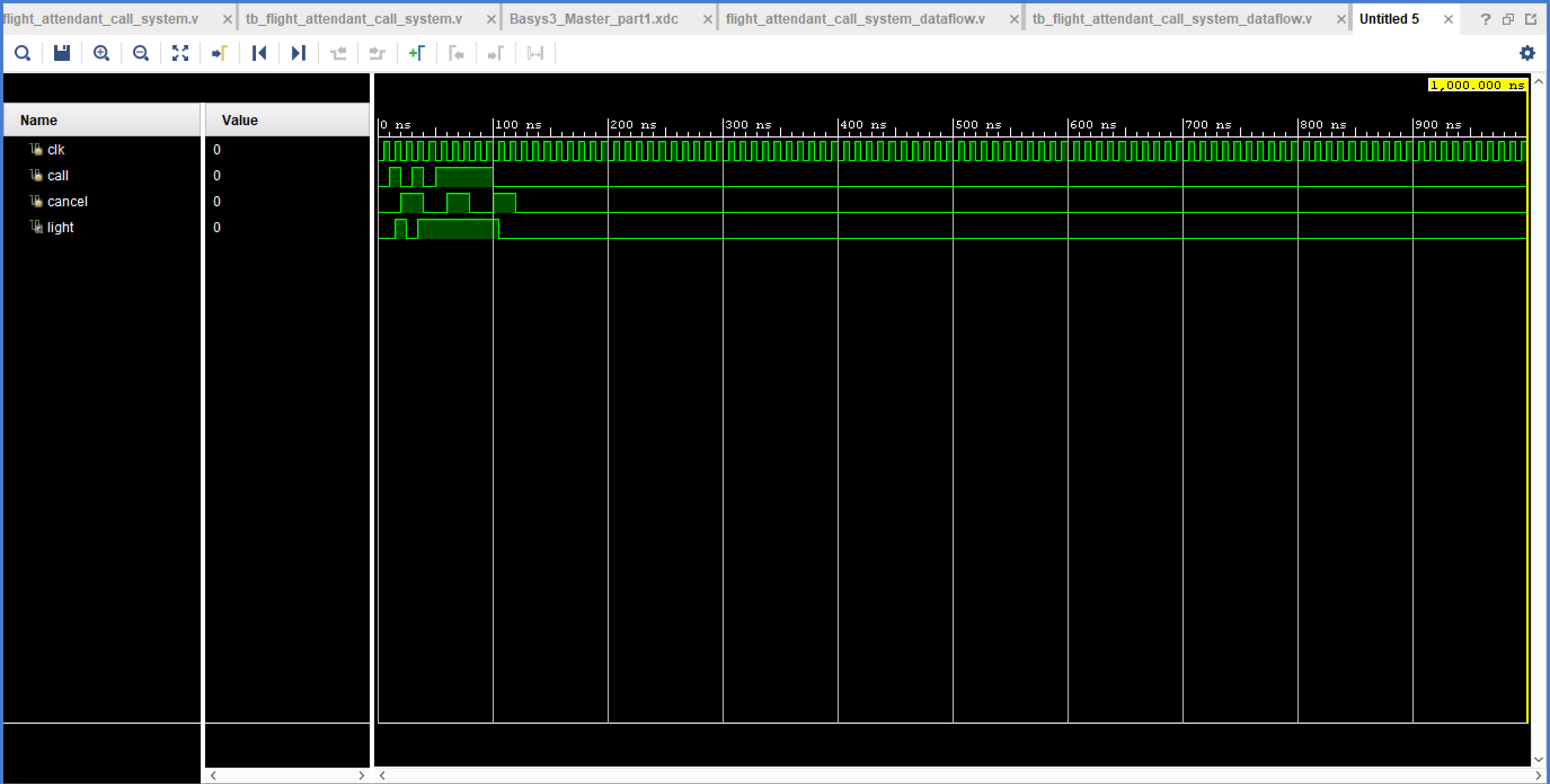
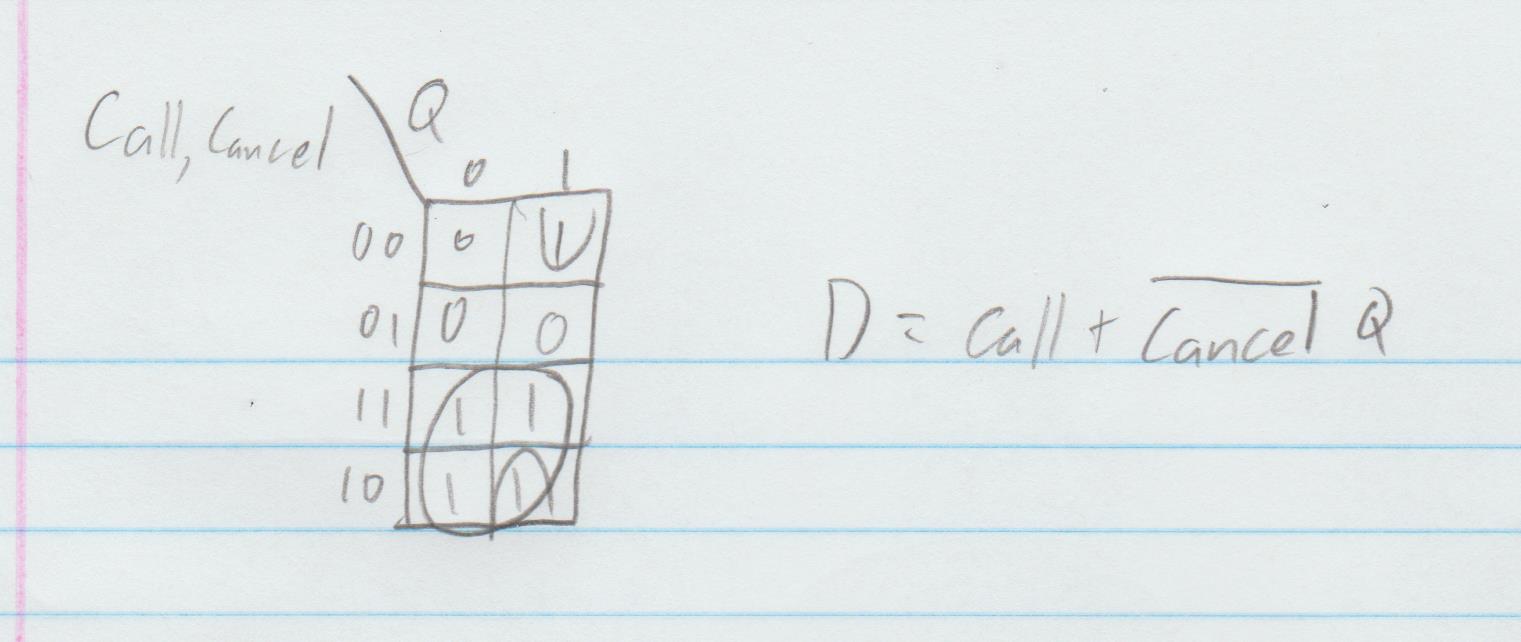
behavioral

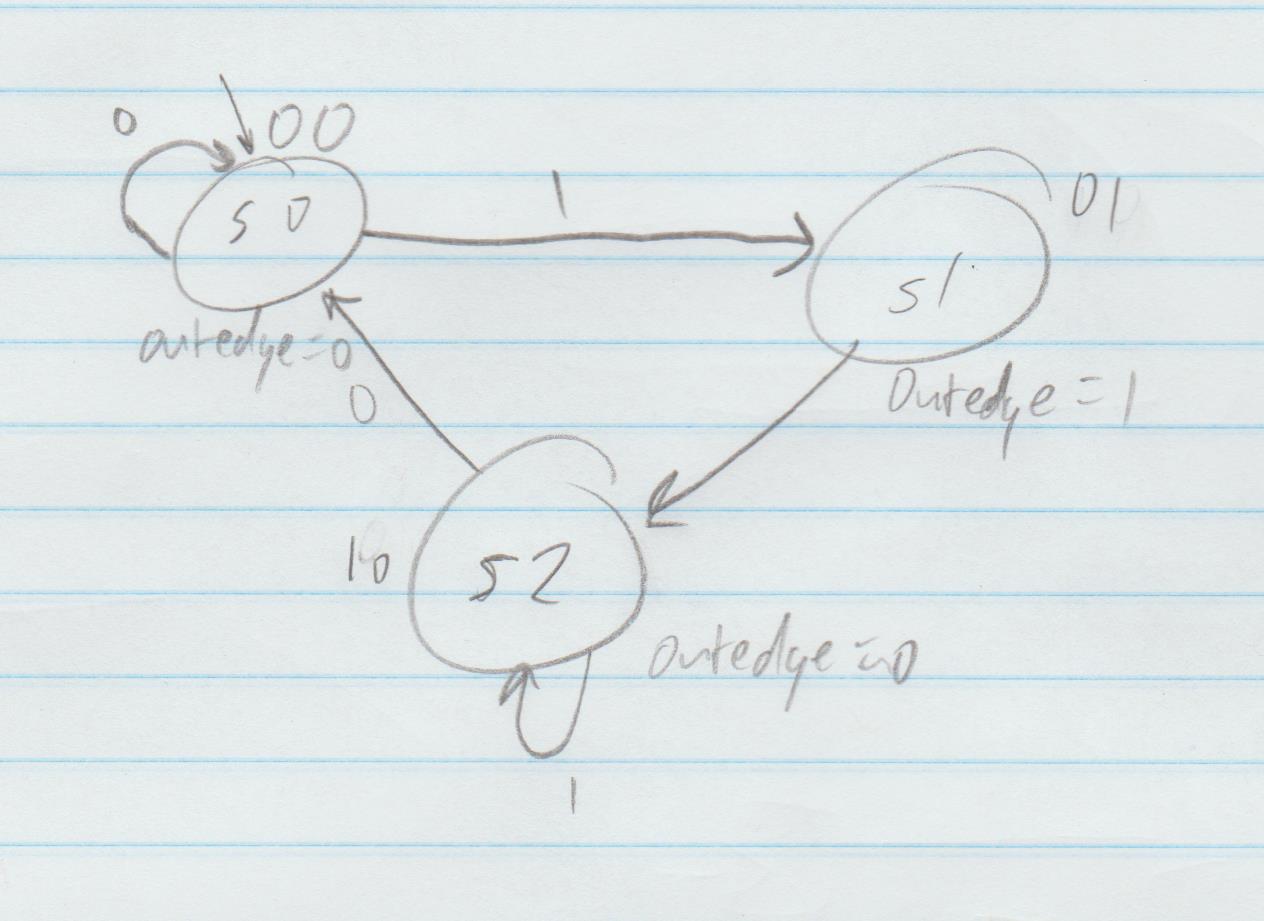


dataflow





Part 2



module tb\_rising\_edge\_detector;

reg clk;

reg signal;

reg reset;

wire outedge;

rising\_edge\_detector uut (

.clk(clk),

.signal(signal),

.reset(reset),

.outedge(outedge)

);

initial begin

clk = 0;

signal = 0;

reset = 0;

#50;

signal = 1;

#50;

signal = 0;

#50;

signal = 1;

#50;

reset = 1;

#50;

reset = 0;

#50;

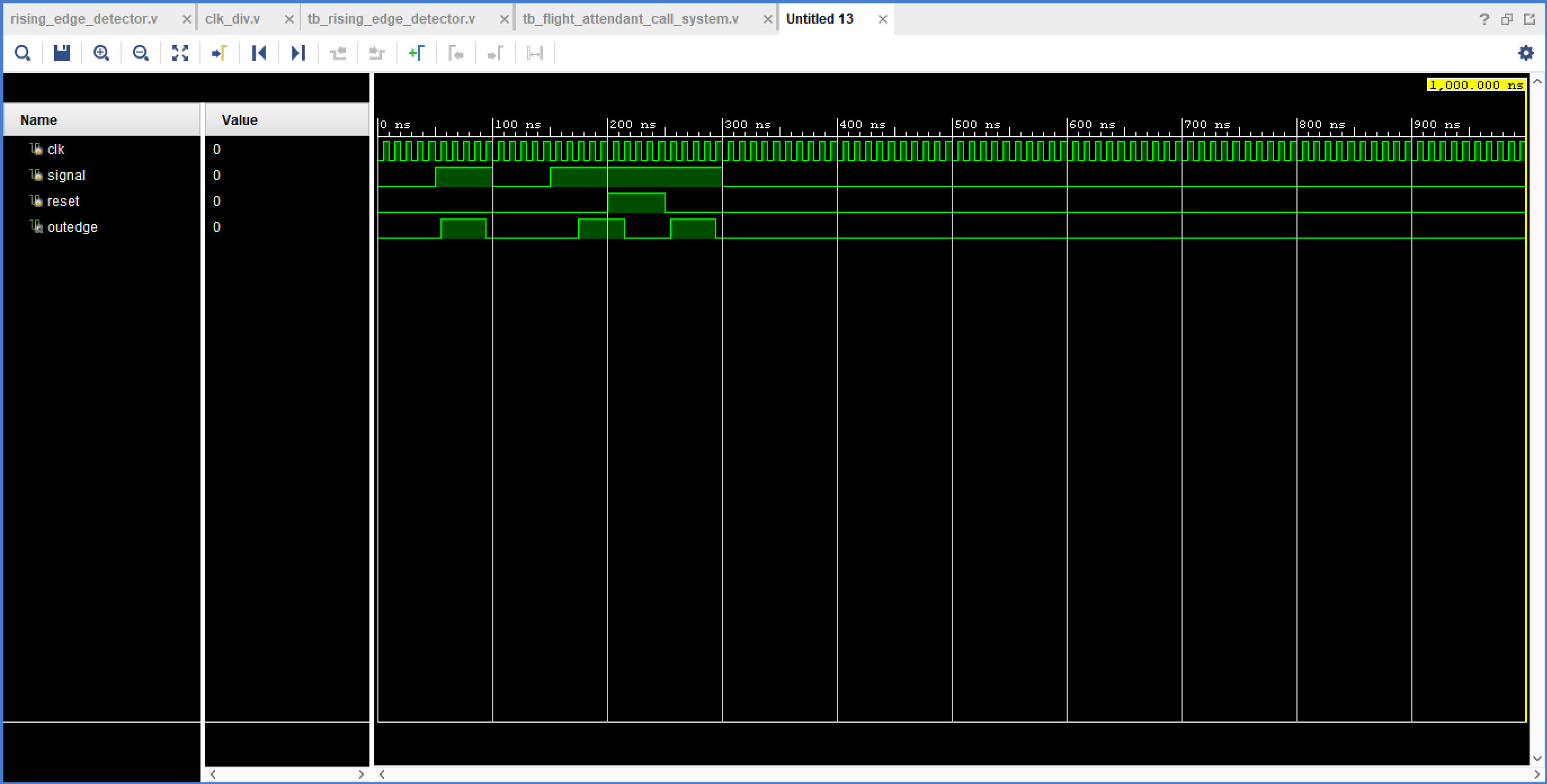
signal = 0;

end

always

#5 clk = ~clk;

Endmodule



## Clock signal

set\_property PACKAGE\_PIN W5 [get\_ports clk]

set\_property IOSTANDARD LVCMOS33 [get\_ports clk]

create\_clock -add -name sys\_clk\_pin -period 10.00 -waveform {0 5} [get\_ports clk]

## Switches

set\_property PACKAGE\_PIN V17 [get\_ports {signal}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {signal}]

## LEDs

set\_property PACKAGE\_PIN U16 [get\_ports {outedge}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {outedge}]

##Buttons

set\_property PACKAGE\_PIN U18 [get\_ports {reset}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {reset}]

Part 3

module tb\_time\_multiplexing\_main;

reg clk;

reg reset;

reg[15:0] sw;

wire[3:0] an;

wire[6:0] sseg;

time\_multiplexing\_main uut (

.clk(clk),

.reset(reset),

.sw(sw),

.an(an),

.sseg(sseg)

);

initial begin

clk = 0;

reset = 1;

sw = 0;

#50;

reset = 0;

sw = 16'h3210;

#50;

sw = 16'h7654;

#50;

sw = 16'hBA98;

#50;

sw = 16'hFEDC;

#50;

sw = 16'h5555;

reset = 1;

#100;

reset = 0;

#50;

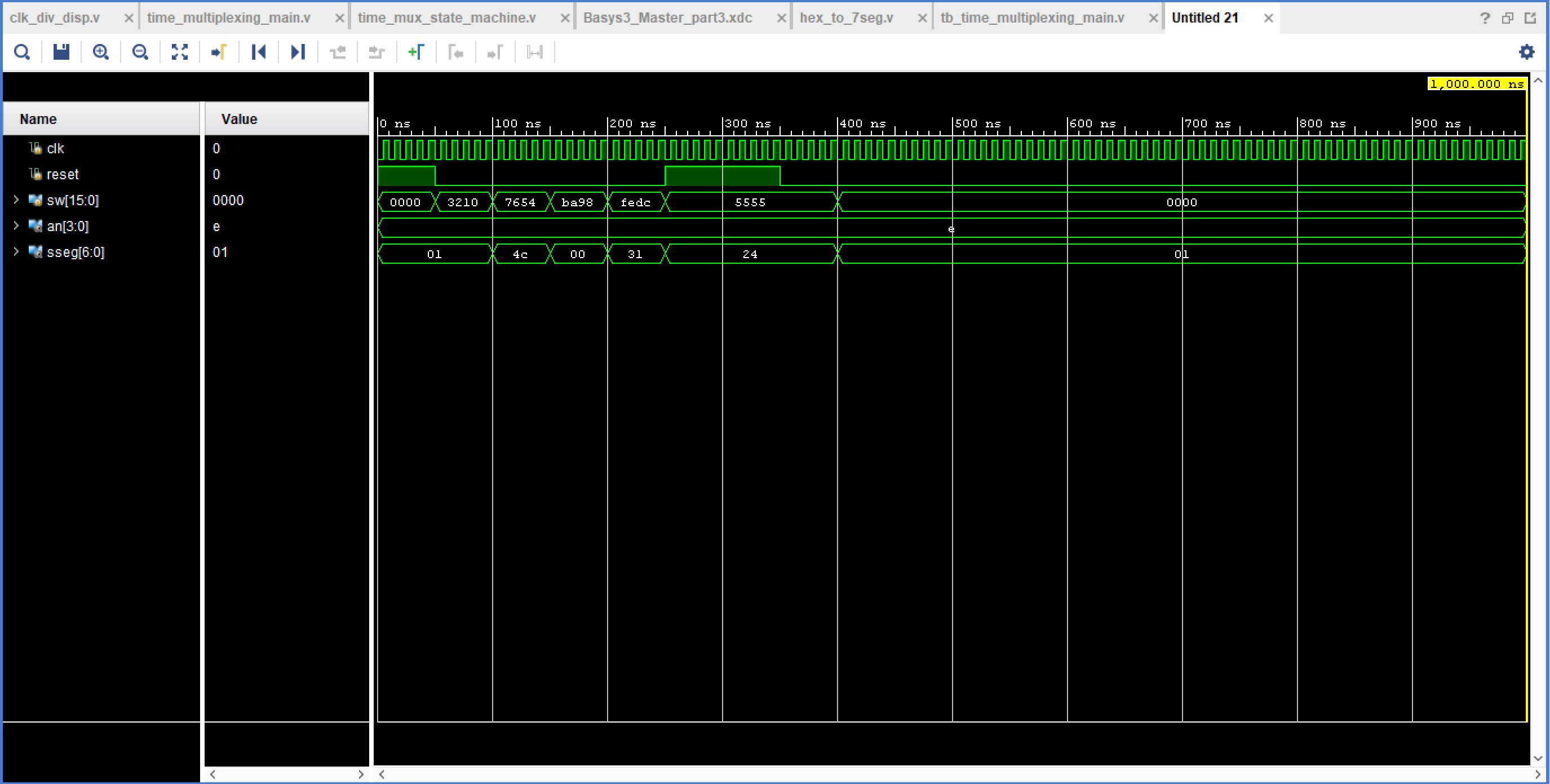
sw = 16'h0000;

end

always

#5 clk = ~clk;

endmodule



## Clock signal

set\_property PACKAGE\_PIN W5 [get\_ports clk]

set\_property IOSTANDARD LVCMOS33 [get\_ports clk]

create\_clock -add -name sys\_clk\_pin -period 10.00 -waveform {0 5} [get\_ports clk]

## Switches

set\_property PACKAGE\_PIN V17 [get\_ports {sw[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[0]}]

set\_property PACKAGE\_PIN V16 [get\_ports {sw[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[1]}]

set\_property PACKAGE\_PIN W16 [get\_ports {sw[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[2]}]

set\_property PACKAGE\_PIN W17 [get\_ports {sw[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[3]}]

set\_property PACKAGE\_PIN W15 [get\_ports {sw[4]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[4]}]

set\_property PACKAGE\_PIN V15 [get\_ports {sw[5]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[5]}]

set\_property PACKAGE\_PIN W14 [get\_ports {sw[6]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[6]}]

set\_property PACKAGE\_PIN W13 [get\_ports {sw[7]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[7]}]

set\_property PACKAGE\_PIN V2 [get\_ports {sw[8]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[8]}]

set\_property PACKAGE\_PIN T3 [get\_ports {sw[9]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[9]}]

set\_property PACKAGE\_PIN T2 [get\_ports {sw[10]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[10]}]

set\_property PACKAGE\_PIN R3 [get\_ports {sw[11]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[11]}]

set\_property PACKAGE\_PIN W2 [get\_ports {sw[12]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[12]}]

set\_property PACKAGE\_PIN U1 [get\_ports {sw[13]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[13]}]

set\_property PACKAGE\_PIN T1 [get\_ports {sw[14]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[14]}]

set\_property PACKAGE\_PIN R2 [get\_ports {sw[15]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[15]}]

##7 segment display

set\_property PACKAGE\_PIN W7 [get\_ports {sseg[6]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sseg[6]}]

set\_property PACKAGE\_PIN W6 [get\_ports {sseg[5]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sseg[5]}]

set\_property PACKAGE\_PIN U8 [get\_ports {sseg[4]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sseg[4]}]

set\_property PACKAGE\_PIN V8 [get\_ports {sseg[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sseg[3]}]

set\_property PACKAGE\_PIN U5 [get\_ports {sseg[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sseg[2]}]

set\_property PACKAGE\_PIN V5 [get\_ports {sseg[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sseg[1]}]

set\_property PACKAGE\_PIN U7 [get\_ports {sseg[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sseg[0]}]

set\_property PACKAGE\_PIN U2 [get\_ports {an[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an[0]}]

set\_property PACKAGE\_PIN U4 [get\_ports {an[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an[1]}]

set\_property PACKAGE\_PIN V4 [get\_ports {an[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an[2]}]

set\_property PACKAGE\_PIN W4 [get\_ports {an[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an[3]}]

##Buttons

set\_property PACKAGE\_PIN U18 [get\_ports {reset}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {reset}]