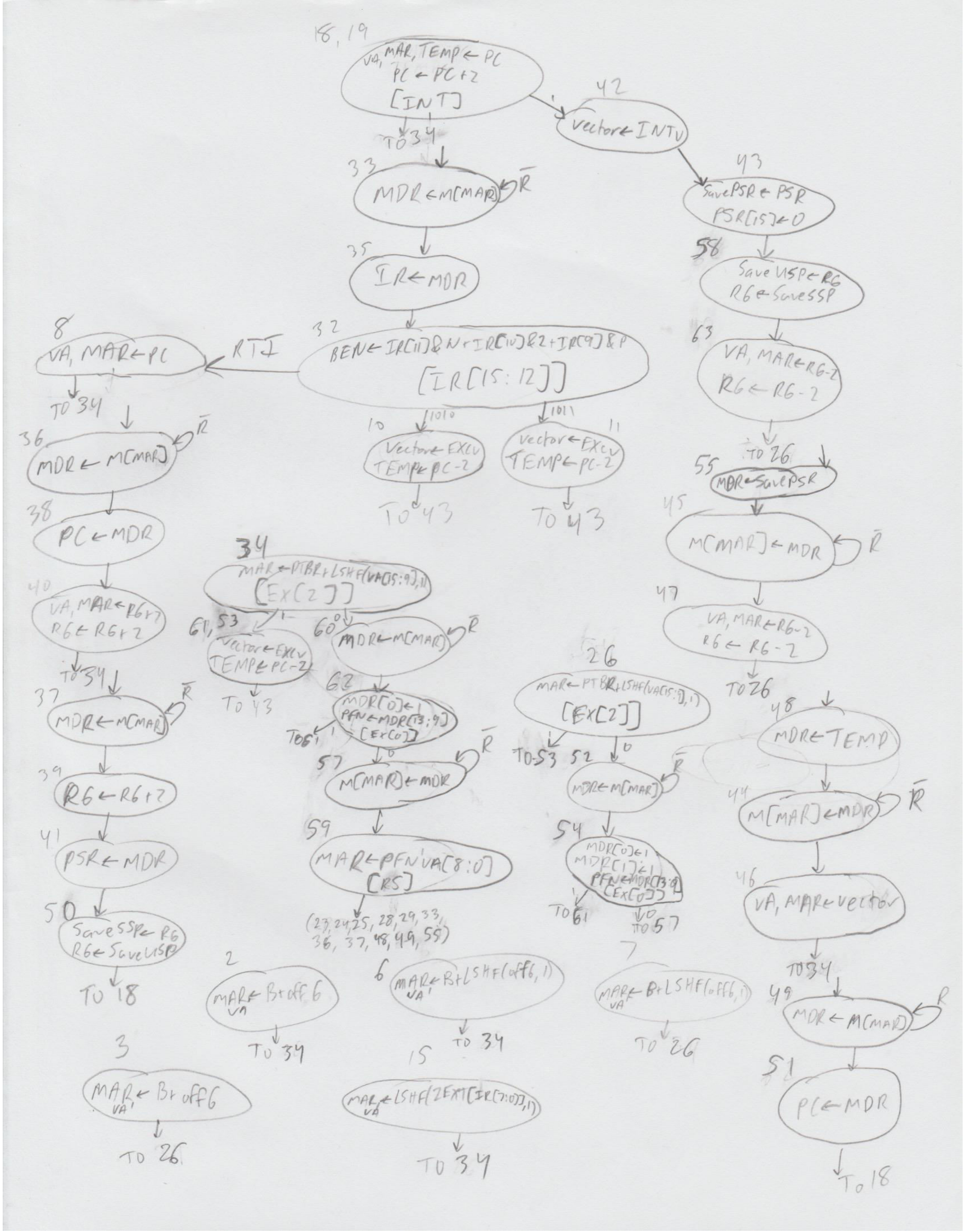
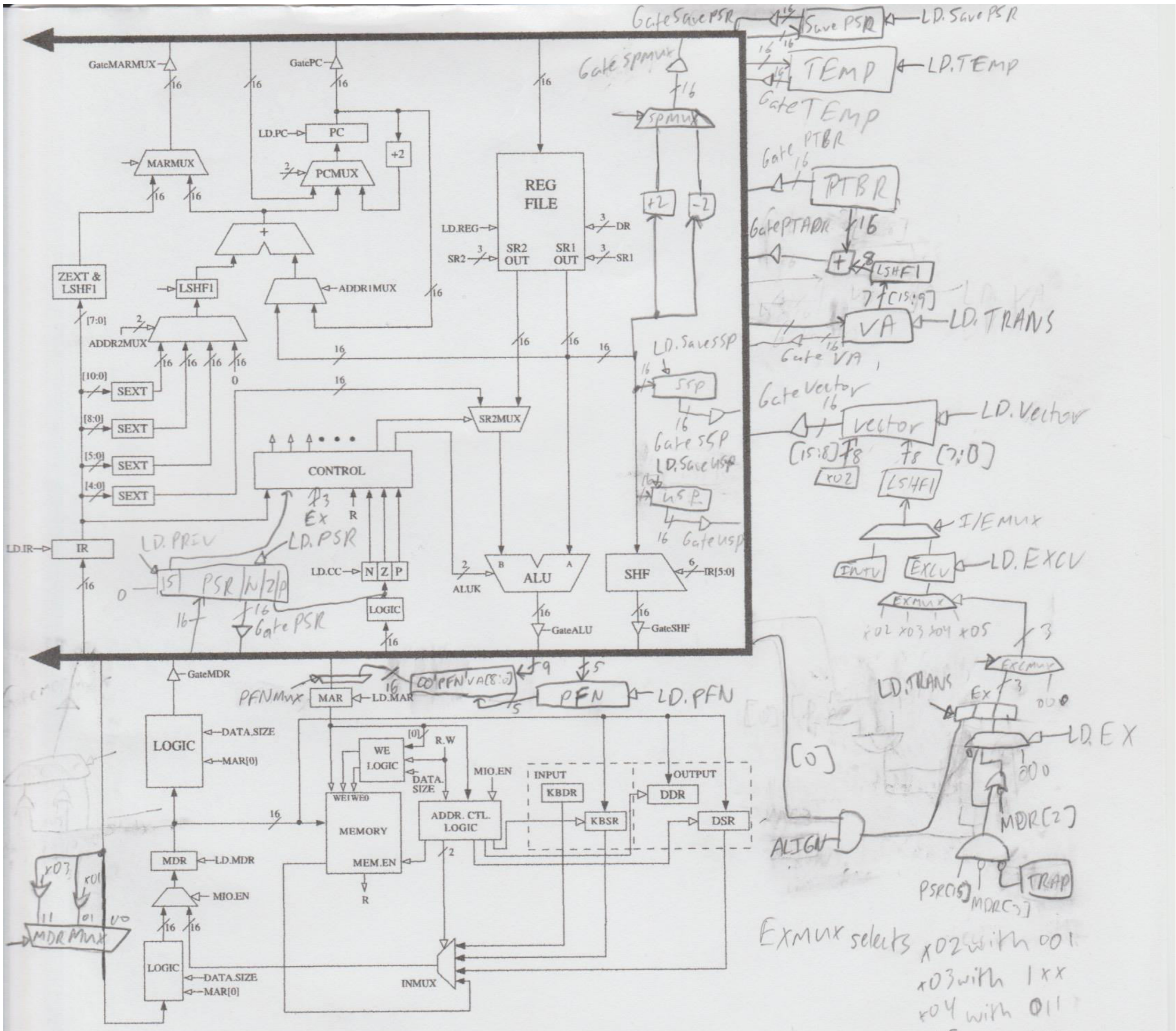
Noah Kessler
Lab 5

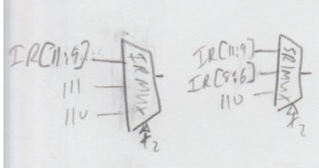


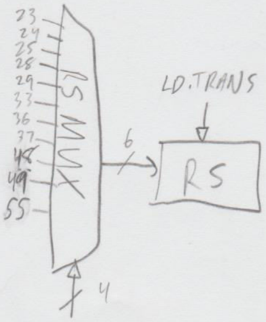
Changes from lab 4:

The main change was memory translation, which takes place starting in states 26 and 34. Loads begin at state 34 and stores begin at state 26. There is a difference because the modify bit in the PTE has to be set if the operation is a store, but not a load. States 26 and 34 check for an unaligned access exception and load the address of the PTE into MAR. The PTE is loaded into MDR, the page frame number is saved, the reference bit is set and the modify bit is set if the access is a store. Then the PTE is saved back into memory, the physical address of the data is loaded into MAR, and it branches back to the previous action to complete the memory access with the correct address. The other changes were branching to state 34 or 26 each time MAR is loaded with a new address and some state number changes to accommodate branching in the translation.

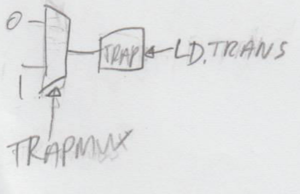


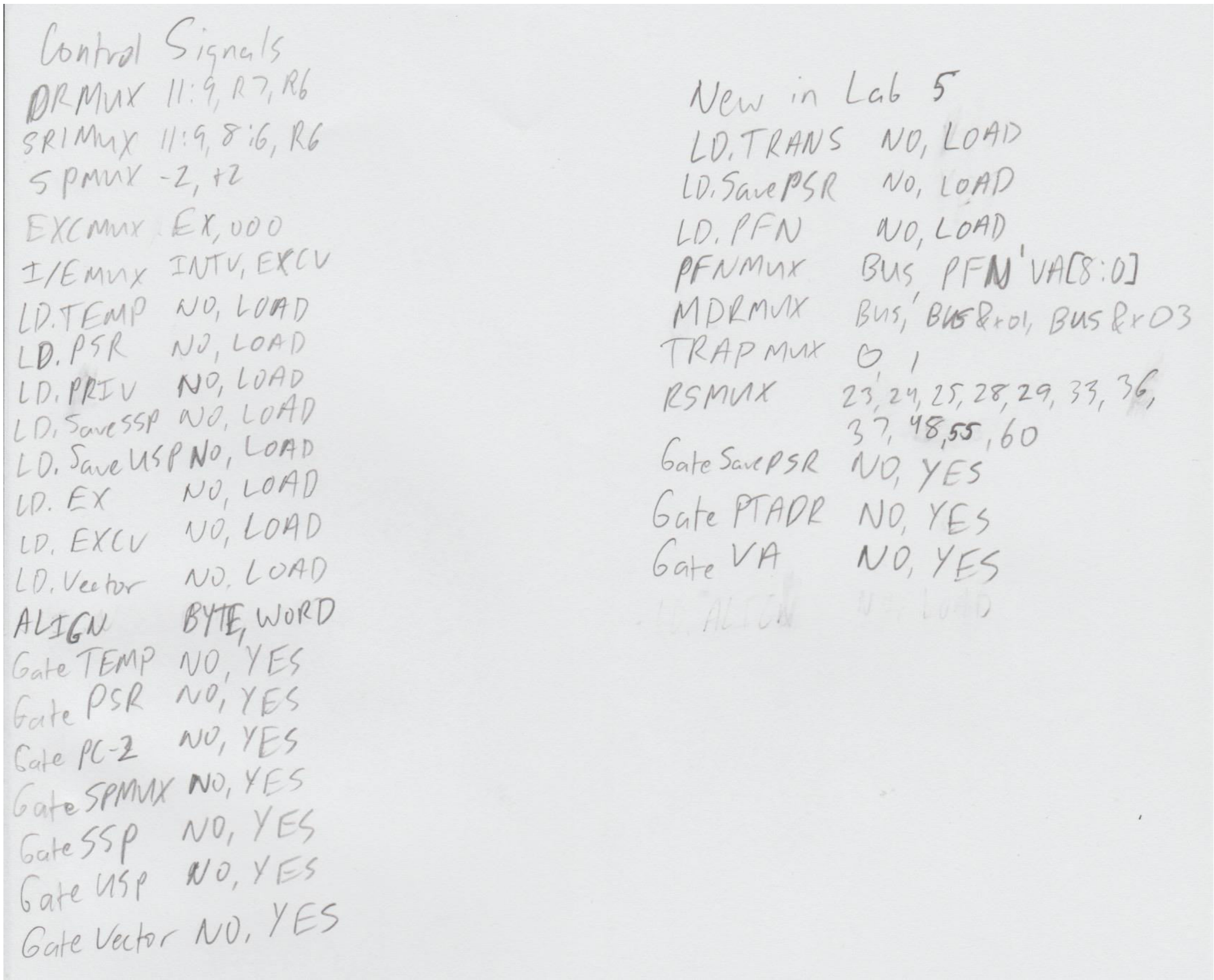
Exmux selects x02 with 001
x03 with 1xx
x04 with 011
x05 with 000





RSMUX selects
23 with x0
24 with x1
25 with x2
28 with x3
29 with x4
33 with x5
36 with x6
37 with x7
48 with x8
49 with x9
55 with xA





Control Signals

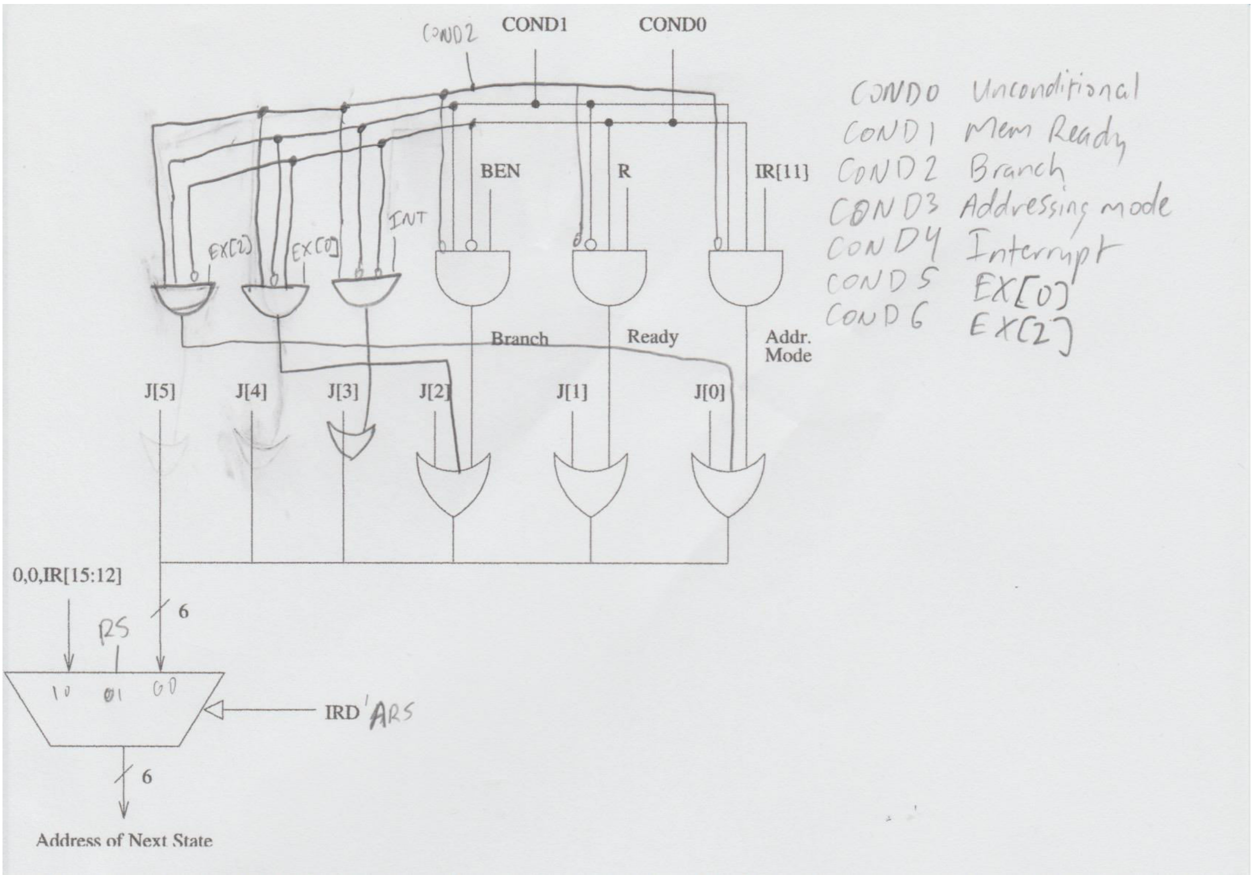
DRMUX	11:9, R7, R6
SR1MUX	11:9, 8:6, R6
SPMUX	-2, +2
EXCMUX	EX, 000
I/EMUX	INTV, EXCV
LD.TEMP	NO, LOAD
LD.PSR	NO, LOAD
LD.PRIV	NO, LOAD
LD.SaveSSP	NO, LOAD
LD.SaveUSP	NO, LOAD
LD.EX	NO, LOAD
LD.EXCV	NO, LOAD
LD.Vector	NO, LOAD
ALIGN	BYTE, WORD
Gate TEMP	NO, YES
Gate PSR	NO, YES
Gate PC-2	NO, YES
Gate SPMUX	NO, YES
Gate SSP	NO, YES
Gate USP	NO, YES
Gate Vector	NO, YES

New in Lab 5

LD.TRANS	NO, LOAD
LD.SavePSR	NO, LOAD
LD.PFN	NO, LOAD
PFNMux	Bus, PFN'VA[8:0]
MDRMUX	Bus, BUS&x01, BUS&x03
TRAPMUX	0, 1
RSMUX	23, 24, 25, 28, 29, 33, 36, 37, 48, 55, 60
Gate SavePSR	NO, YES
Gate PTADR	NO, YES
Gate VA	NO, YES

Changes from lab 4:
SavePSR, PTBR, VA, PFN, TRAP and RS registers have been added. SavePSR saves the PSR when an interrupt or exception is called before it can be pushed onto the stack. PTBR holds to page table base register. VA stores the virtual address when MAR gets the PTBR + offset. PFN stores the page frame number once it is gotten from memory. TRAP stores a 1 if a TRAP instruction is called, because this is needed for exception detection. RS holds the return state while address translation happens. Save PSR is loaded from the bus with LD.SavePSR and drives the bus with GateSavePSR. PFN is loaded with LD.PFN. When PFNMUX is set, MAR[13:9] is loaded with the PFN and MAR[8:0] is loaded from the bus with VA[8:0]. MDRMUX is used in translation to set the modify and reference bits in the PTE before it is stored again. 1 sets reference and 3 sets both. TRAPMUX selects 0 or 1 to load into the TRAP register. RSMUX selects the return state to be loaded into the RS register. GateVA drives the bus with the value stored in the VA register. If LD.TRANS is set, TRAP, RS, VA and EX[2] are all loaded with new values. EX[2] is used to detect unaligned access exceptions. If GatePTADR is set, the BUS is driven with the PTBE value plus the offset in the page table from VA[15:9] * 2. There is a change to the exception detection logic. Unaligned is checked for the same way as before, protection is now when the protection bit is cleared in the PTE and PSR[15] is 1 and the instruction is not a TRAP, and page fault is if the

valid bit of the PTE is cleared. EX[2] is set for unaligned access, EX = 011 for protection exceptions and EX = 001 for page faults. Unaligned access is checked for with EX[2] before loading the PTE, and protection and page fault are checked for with EX[0] before the updated PTE is stored back into memory.



An additional condition bit is needed to select between 6 conditions. Conditions 0-4 are the same as lab 4. COND5 branches if EX[0] is set and COND6 branches if EX[2] is set.