EEE 3101: Digital Logic and Circuits

Universal Gates

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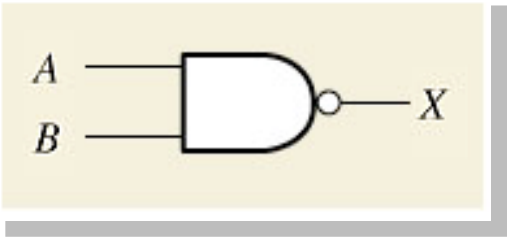
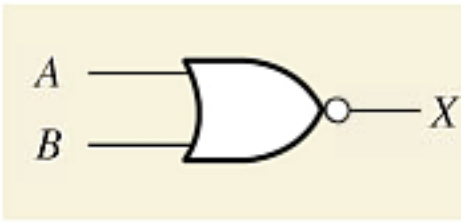
UNIVERSAL GATES

- We can implement **any circuit** with **AND/OR/NOT**, we can also implement **any circuit** with **only NAND** or **NOR** gates.
- We might want to do this because of technology considerations, that is, these gates might be cheaper to implement in silicon or they might be the only type of gates we have available.
- Since we can always use only NAND or NOR gates, these gates are called **universal gates**.

NAND gate



NOR gate



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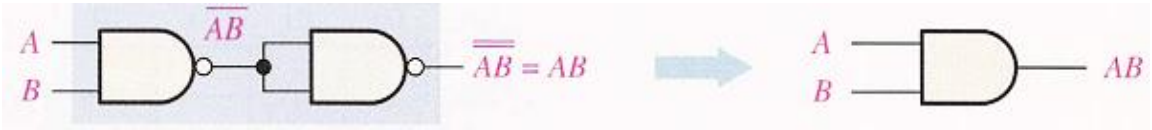
Universal Property of NAND and NOR gates:

The NAND gate as a Universal logic gate:

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

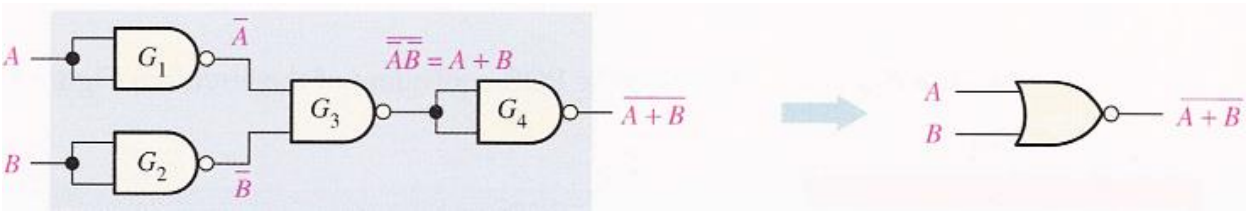
- One NAND gate used as an inverter (**NOT gate**):

- Two NAND gates used as an **AND gate**:



- Three NAND gates used as an **OR gate**:

- Four NAND gates used as a **NOR gate**:



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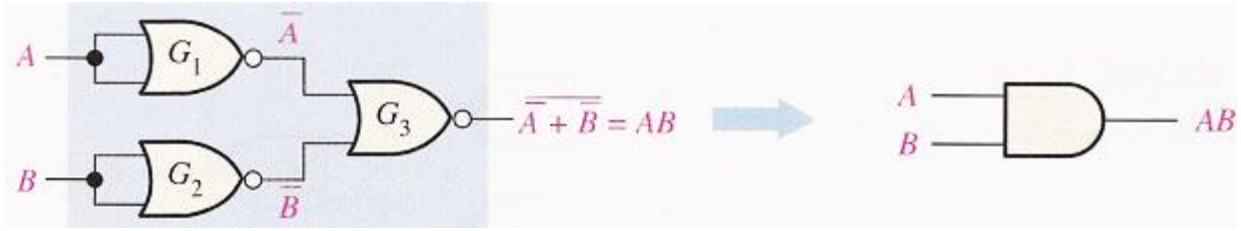
The NOR gate as a Universal logic gate:

•One NOR gate used as an inverter (**NOT gate**):

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

•Two NOR gates used as an **OR gate**:

•Three NOR gates used as an **AND gate**:



•Four NOR gates used as a **NOR gate**:

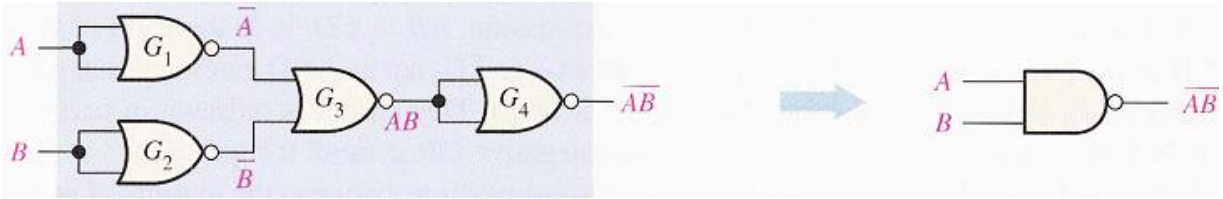


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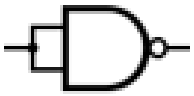
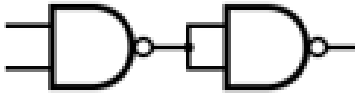
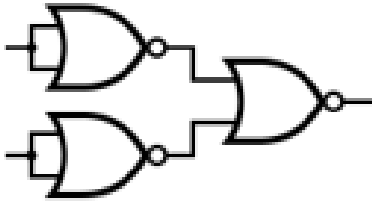
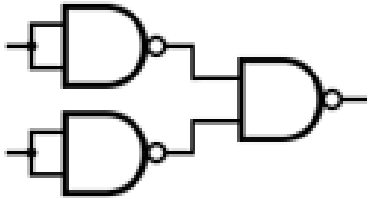
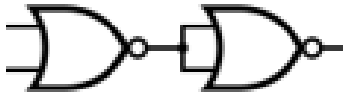
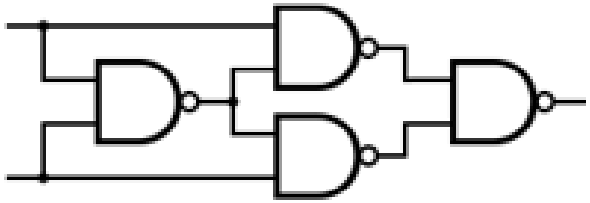
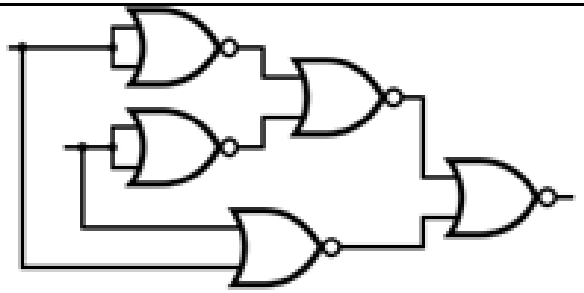
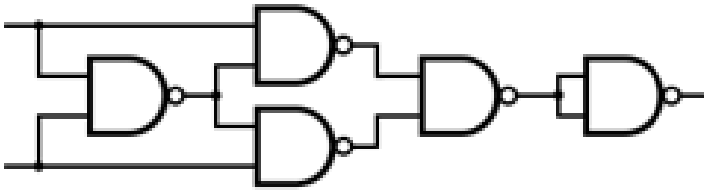
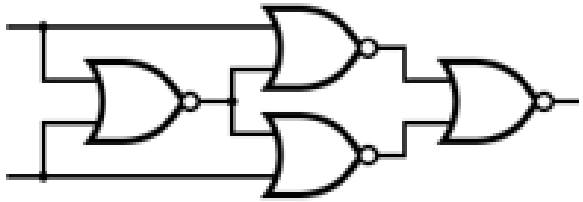
Table 1: Logic gate equivalence with universal gate implementation

	NAND	NOR
NOT		
AND		
OR		
XOR		
XNOR		

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Implementing ANY circuit using Universal gates:

The ability to implement **NOT/AND/OR** with **NAND or NOR** means we can implement **any circuit** using only with **NANDs or NORs** by **only replacing** the AND, OR and NOT gates with their equivalent NAND or NOR implementations.

Procedure:

1) First construct the logic expression using basic gates (AND/OR/NOT),
2) Replace each basic gate with its equivalent universal gate implementation,
3) Cancel two consecutives NOT gates (according to Boolean algebra),
4) Redraw the final circuit.

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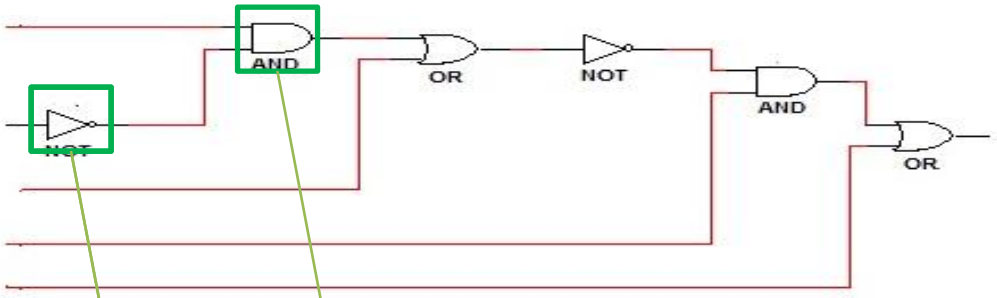
Example: Implement the following expression with (a) NAND gates ONLY, (b) NOR gates ONLY.

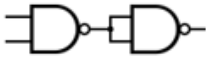
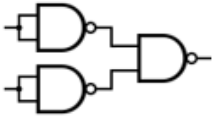
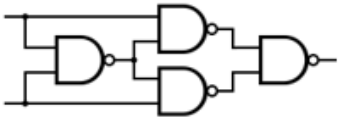
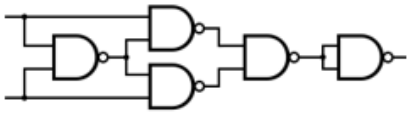
$$Y=(AB'+C)'D+E$$

Solution:

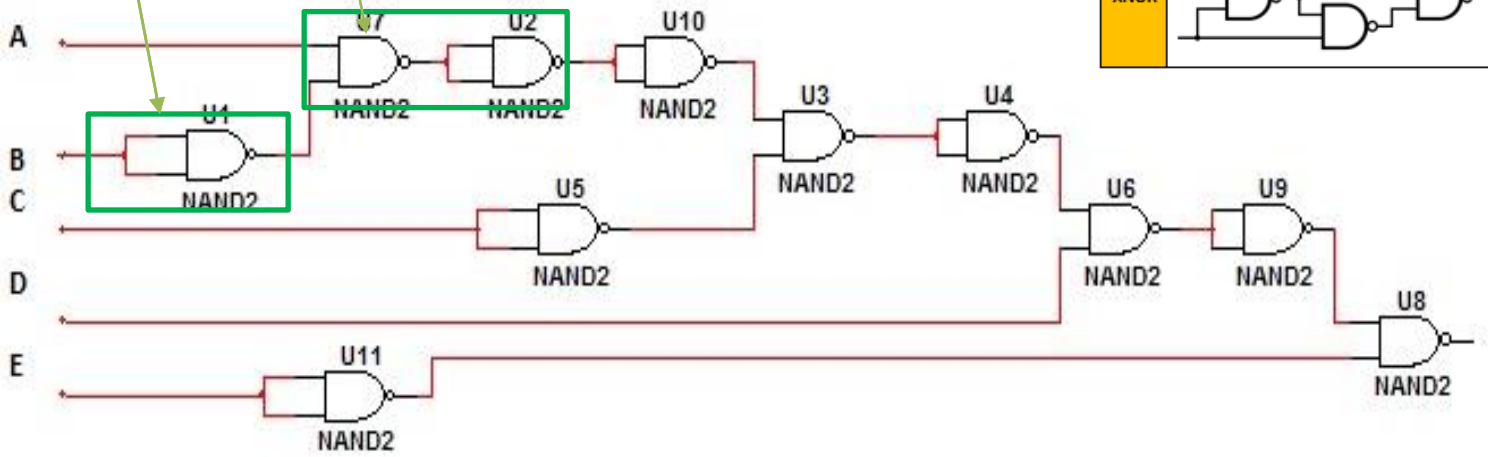
(a) Implementation using NAND gates ONLY:

(i) Implementation with Basic gates:



	NAND
NOT	
AND	
OR	
XOR	
XNOR	

(ii) Replace each basic gate with its equivalent NAND gate implementation from Table 1.



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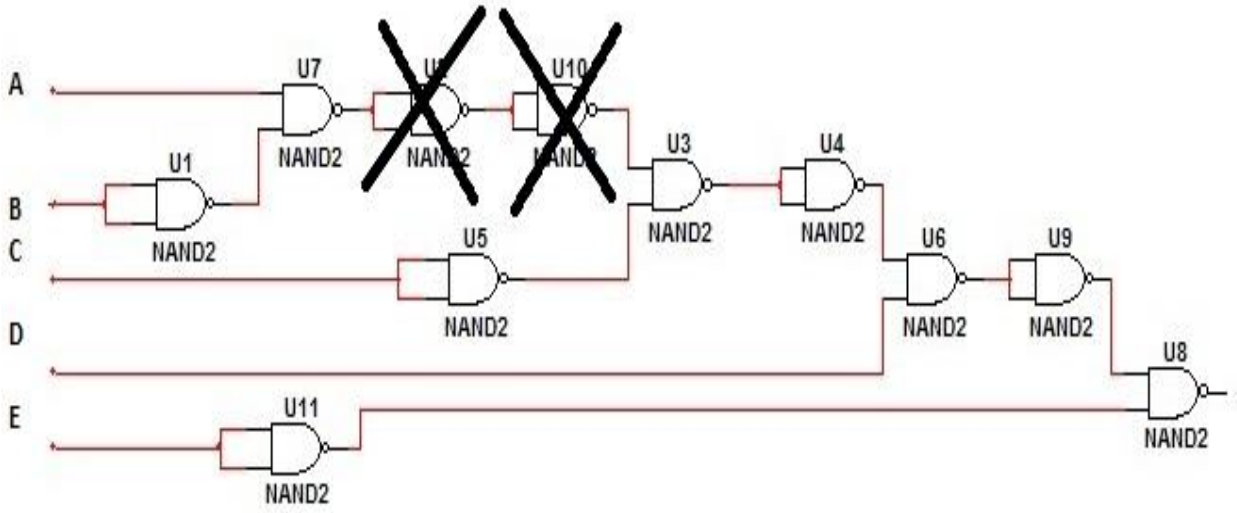
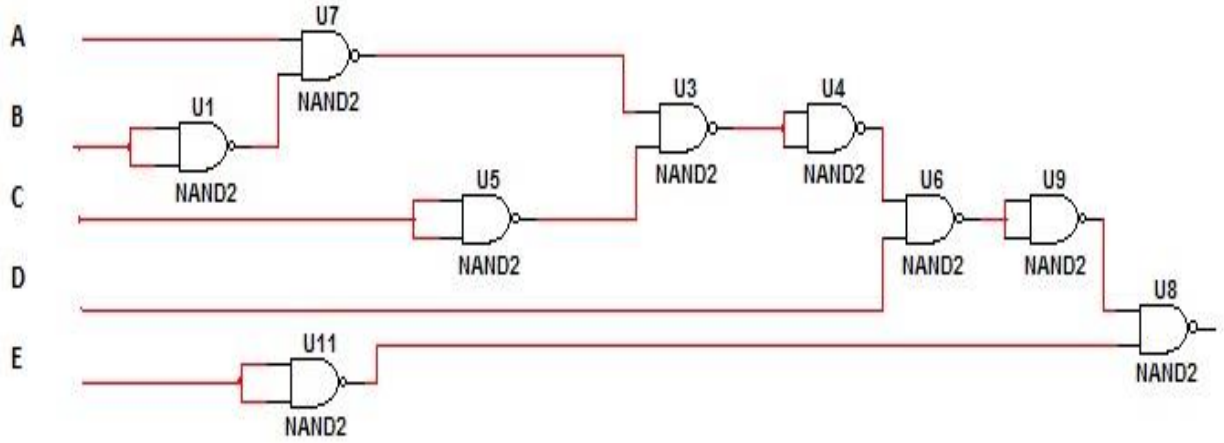
(iii) Cancel two consecutive NOT equivalent gates (according to Boolean algebra).



(iv)Redraw the final circuit.



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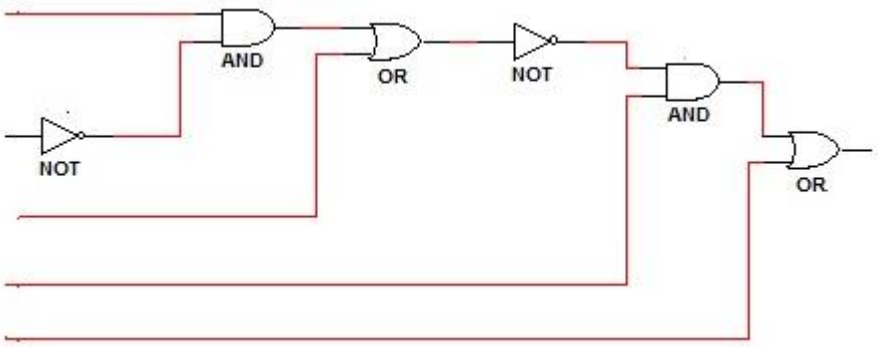
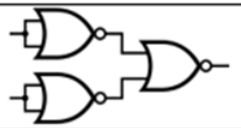
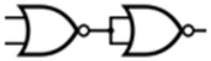
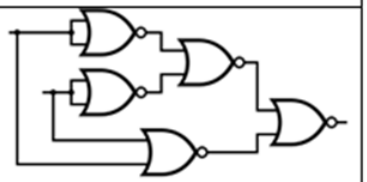
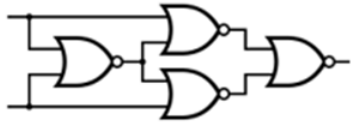
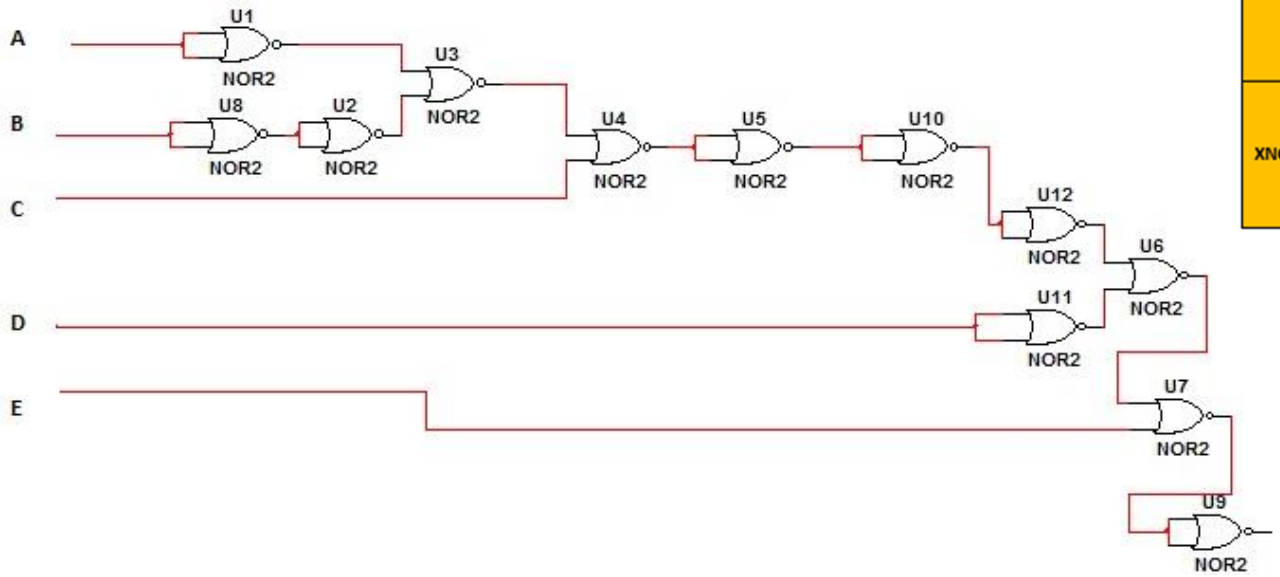
(b) Implementation using NOR gates ONLY:

(i) Implementation with Basic gates:



	NOR
NOT	
AND	
OR	
XOR	
XNOR	

(ii) Replace each basic gate with its equivalent NOR gate implementation from Table 1.



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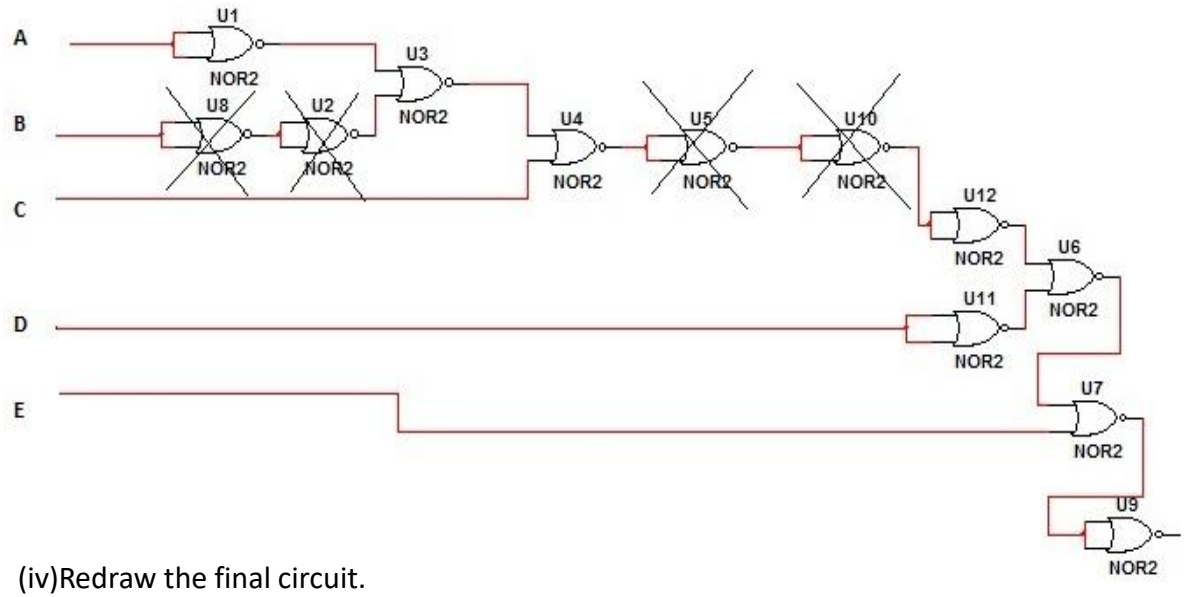
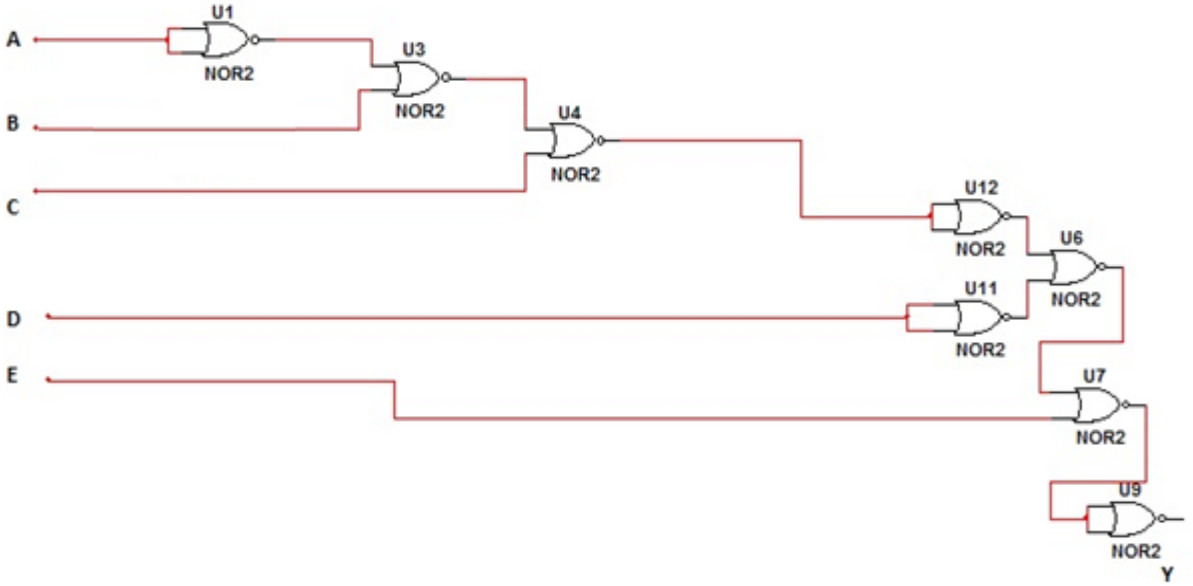
(iii) Cancel two consecutive NOT equivalent gates (according to Boolean algebra).



(iv)Redraw the final circuit.



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Dual Symbols

NAND Logic: a NAND gate can function as either a NAND or a negative-OR

$$\overline{AB} = \overline{A} + \overline{B}$$

NAND — negative-OR

NOR Logic: a NOR gate can function as either a NOR or a negative-AND

$$\overline{A + B} = \overline{A}\,\overline{B}$$

NOR — negative-AND

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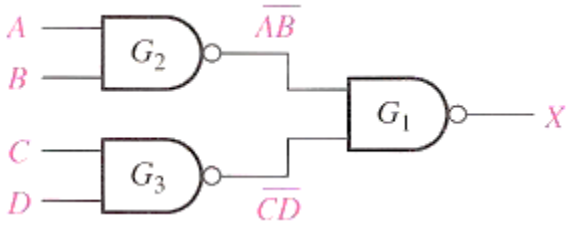
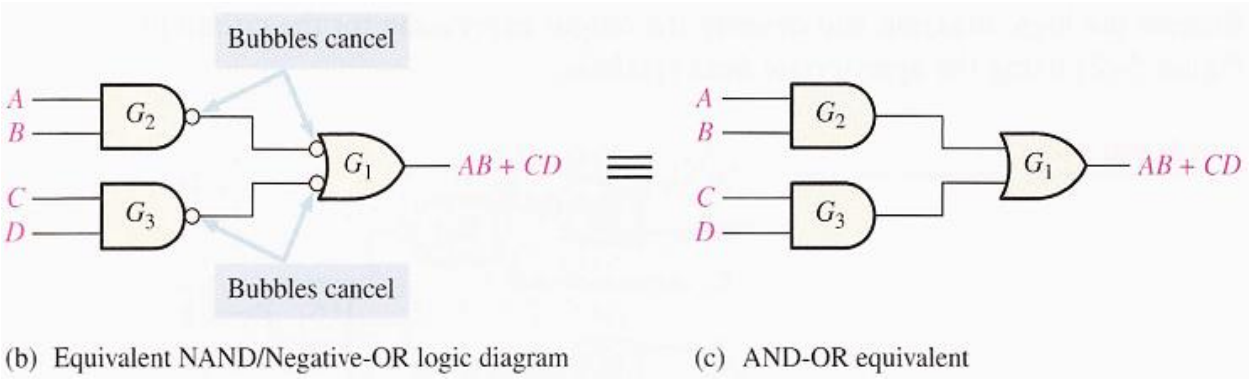
COMBINATIONAL LOGIC USING NAND AND NOR GATES

1) NAND gates:



$$
\begin{aligned}
X &= \overline{(\overline{AB})(\overline{CD})} \\
&= \overline{(\overline{A} + \overline{B})(\overline{C} + \overline{D})} \\
&= (\overline{\overline{A} + \overline{B}}) + (\overline{\overline{C} + \overline{D}}) \\
&= \overline{\overline{A}}\,\overline{\overline{B}} + \overline{\overline{C}}\,\overline{\overline{D}} \\
&= AB + CD
\end{aligned}
$$

NAND Logic Diagrams Using Dual Symbols



(b) Equivalent NAND/Negative-OR logic diagram (c) AND-OR equivalent

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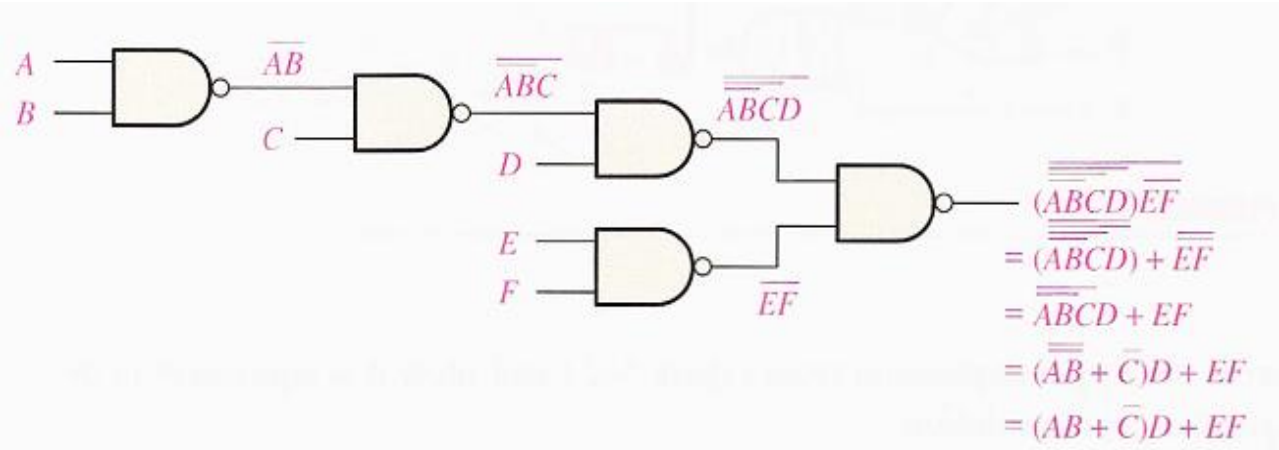
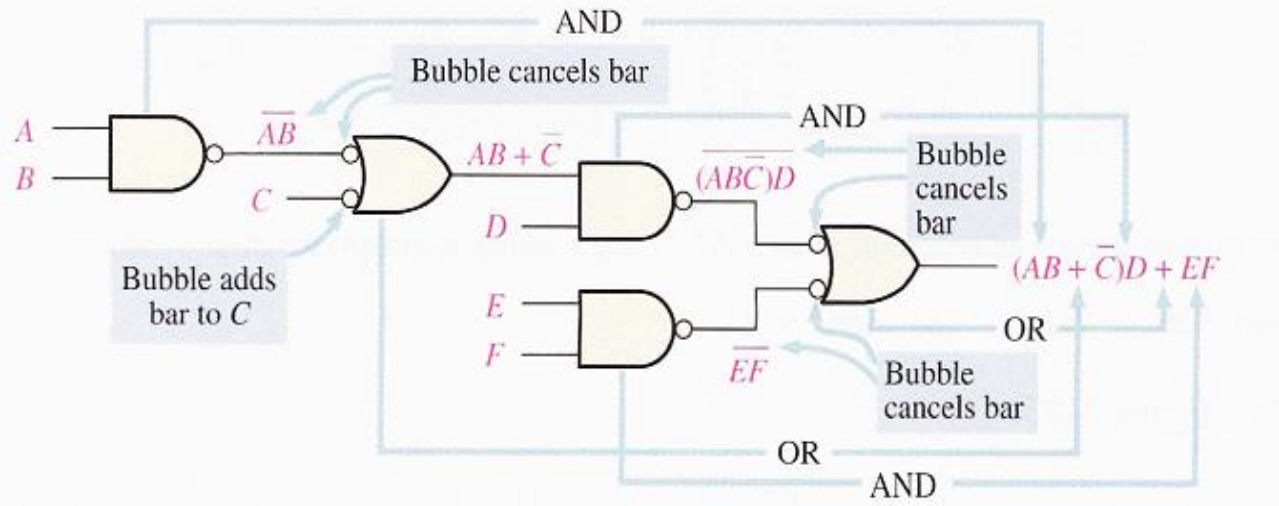
Example:



(a) Several Boolean steps are required to arrive at final output expression.



(b) Output expression can be obtained directly from the function of each gate symbol in the diagram.

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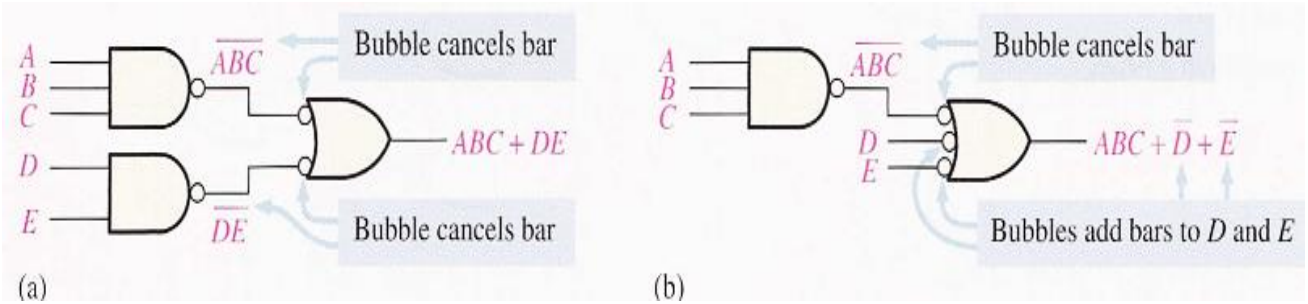
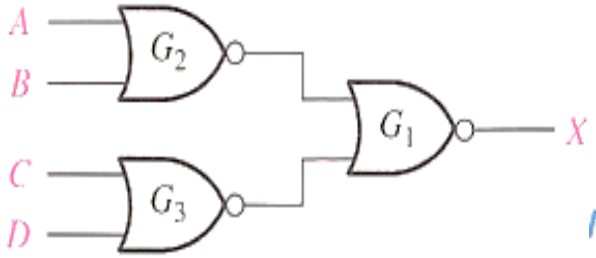
EXAMPLE

Implement each expression with NAND logic using appropriate dual symbols:

(a) $ABC + DE$ (b) $ABC + \overline{D} + \overline{E}$

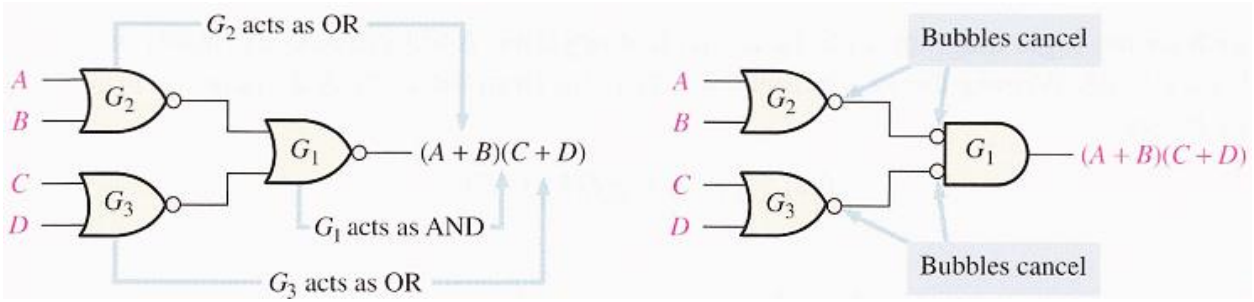


2) NOR gates:



$$X = \overline{\overline{A + B} + \overline{C + D}} = (\overline{\overline{A + B}})(\overline{\overline{C + D}}) = (A + B)(C + D)$$

NOR Logic Diagram Using Dual Symbols



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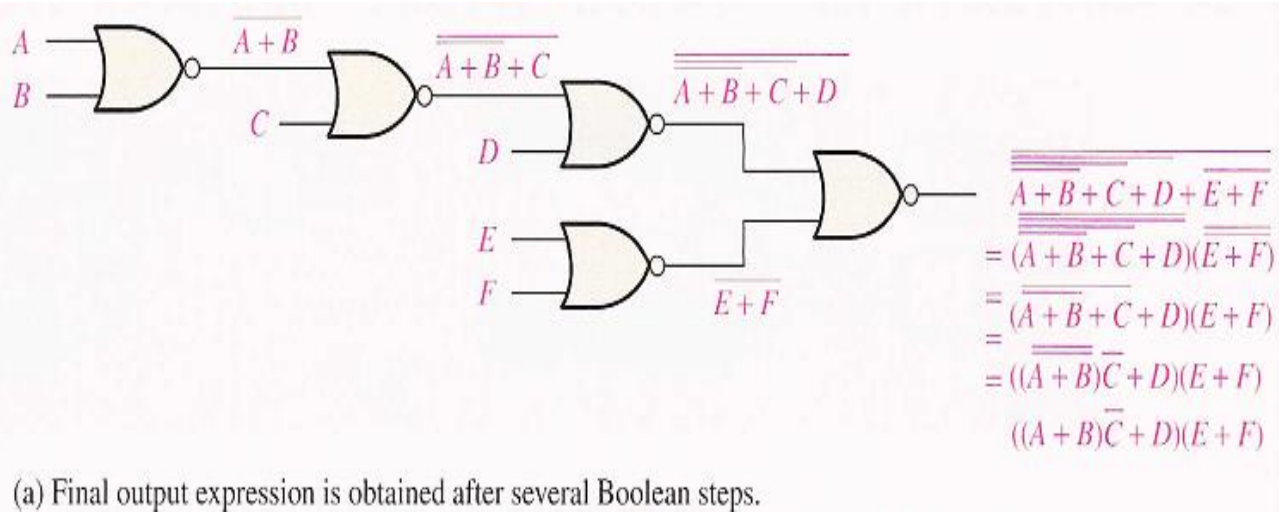
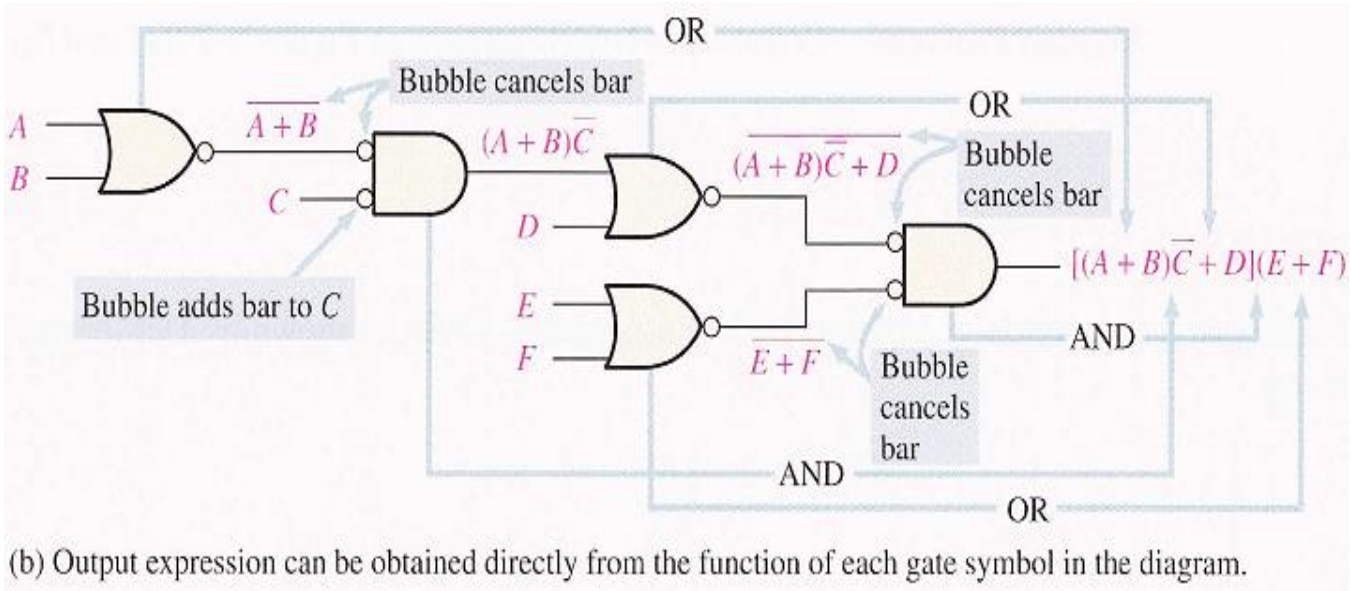
Example:



(a) Final output expression is obtained after several Boolean steps.



(b) Output expression can be obtained directly from the function of each gate symbol in the diagram.

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Reference:

[1] Thomas L. Floyd, "Digital Fundamentals" 11th edition, Prentice Hall.
[2] M. Morris Mano, "Digital Logic & Computer Design" Prentice Hall.

Thanks


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