# American International University – Bangladesh
## Faculty of Engineering
### Department of Electrical and Electronic Engineering

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|---|---|---|---|
| **Course Name:** | Microprocessor and Embedded Systems | **Course Code:** | EEE 4103 |
| **Semester:** | Fall 2023-2024 | **Section:** | L |
| **Faculty Name:** | Protik Parvez Sheikh | | |
| **Assignment No:** | 3 | | |
| **Student Name:** | **NOKIBUL ARFIN SIAM** | | |
| **Student ID:** | **21-44793-1** | **Program Name:** | **BSc in CSE** |
| **Submission Date:** | **27/12/2023** | **Due Date:** | **27/12/2023** |

**Assessment Rubrics:**

| COs-POIs | Excellent [28-30] | Proficient [25-27] | Good [20-24] | Acceptable [10-19] | Unacceptable [1-9] | No Response [0] | Secured Marks |
|---|---|---|---|---|---|---|---|
| **CO3 P.a.4.C.3** | All the problems are solved correctly. The simulation processes are clearly described, and results are generated by combining all possible input patterns with appropriate outcomes. All necessary drawings and computations are shown. | All the problems are solved correctly. The simulation processes are clearly described, and results are generated by combining all possible input patterns with appropriate outcomes. A few necessary drawings and computations are missing. | All the problems are solved correctly. The simulation processes are not clearly described, and results are generated by combining all possible input patterns with appropriate outcomes. Some necessary drawings and computations are missing. | All the problems are not solved correctly. The simulation processes are not clearly described, and results are generated by combining several wrong input patterns with inappropriate outcomes. Some necessary drawings and computations are missing. | All the problems are not solved correctly. The simulation processes are not described, and results are generated by combining mostly wrong input patterns with inappropriate outcomes. Almost all the necessary drawings and computations are missing. | No responses at all | |
| **Comments** | | | | | **Total marks (30)** | | |

**Questions:**

1. Find the baud rate for the asynchronous normal operating mode when the oscillator frequency, fOSC = 24 MHz, and register data is, UBRRn = 111010100101. Calculate the baud error and comment on whether there will be any communication errors or not.
   *[For Arduino Uno, standard Baud rates maybe 300, 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200, etc.]*

2. Determine the necessary register setup to operate a microcontroller in the fast PWM mode in inverting mode. The counter should count to a maximum value of 235 and then reset to the BOTTOM and repeat. Draw the necessary timing waveform. Use a Timer0 of the Arduino Microcontroller.

3. In order to control the speed and rotation of a microcontroller-based DC motor, two Fast PWM signals are set to 40% Non-Inverting PWM Duty Cycle (motor rotates clockwise) and 55% Inverting PWM Duty Cycle (motor rotates counter-clockwise). Determine the values for OCR0A (Inverting Mode) and OCR0B (Non-Inverting Mode).

| **CS12** | **CS11** | **CS10** | **Pre-scaler** |
|---|---|---|---|
| 0 | 1 | 0 | 8 |
| 0 | 1 | 1 | 64 |
| 1 | 0 | 0 | 256 |
| 1 | 1 | 1 | 1024 |

4. Compute the duty cycle and sketch the waveform obtained at port D of the Arduino. Identify the modes of operation and compute the operating frequency of that mode based on the following program segment. Identify the Timer of the Arduino Microcontroller. The system clock frequency is 8 MHz.

```
DDRD |= (1<<PD5);
pinMode(5, OUTPUT);
OCR0A = 200; // Load a value in the OCR0A register
OCR0B= 141; // Load a value in the OCR0A register
// Configure TCCR0A and TCCR0B registers for the mode and pre-scaler
TCCR0A |= (1 << COM0B1) | (1 << COM0A0) | (1<<WGM01) | (1<<WGM00);
TCCR0B |= (1<<WGM02) | (1<<CS01) | (1<<CS00);
```

**Table 1: Clock select function bits and corresponding pre-scaler values (L) and Compare output mode setting bits (R)**

| CSn2 | CSn1 | CSn0 | Pre-scaler | COMnA1 | COMnA0 | Description |
|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 0 | The normal port operation, OC0A disconnected |
| 0 | 1 | 0 | 8 | 0 | 1 | WGM02 = 0; Normal port operation, OC0A disconnected<br>WGM02 = 1; Toggle OC0A on Compare Match |
| 0 | 1 | 1 | 64 | 1 | 0 | Clear OC0A on Compare Match, Set OC0A at BOTTOM (non-inverting mode) |
| 1 | 0 | 0 | 256 | 1 | 1 | Set OC0A on Compare Match, Clear OC0A at BOTTOM (inverting mode) |
| 1 | 0 | 1 | 1024 | | | |

5. Design an adder/subtractor circuit with one selection variable ‘*S*’ and two inputs ‘*A*’ and ‘*B*’: when $S = 0$ the circuit performs $A + B$. When $S = 1$ the circuit performs $A – B$ by taking the 2’s complement of *B*.

6. Sketch a 2-bit Arithmetic Logic Unit (ALU) for the operations listed in Table 1.

**Table 1: Functions of control variables**

| Binary Code | Functions of selection variables | | | | | |
|---|---|---|---|---|---|---|
| | ***A*** | ***B*** | ***D*** | ***F* with $C_{in}$ = 0** | ***F* with $C_{in}$ = 1** | ***H*** |
| 0 0 0 | Input Data | Input Data | None | A-1 | A | 1’s to the output Bus |
| 0 0 1 | R1 | R1 | R1 | A+B | A+B+1 | Shift Left with $I_L = 0$ |
| 0 1 0 | R2 | R2 | R2 | A-B-1 | A-B | No Shift |
| 0 1 1 | R3 | R3 | R3 | A | A+1 | Circulate Left with Carry |
| 1 0 0 | R4 | R4 | R4 | $\bar{A}$ | X | 0’s to the output Bus |
| 1 0 1 | R5 | R5 | R5 | AX**OR** B | X | - |
| 1 1 0 | R6 | R6 | R6 | A **AND** B | X | Circulate-Right with Carry |
| 1 1 1 | R7 | R7 | R7 | A **OR** B | X | Shift Right with $I_R = 0$ |

7. Design a 3-bit shifter circuit for the listed shift functions provided in Table 1.

8. Develop the control words in binary and hexadecimal formats using the information provided in Table 1 for the following micro-operations:
    i. R7←R3+R4
    ii. R3←SHL R3
    iii. R5←R1
    iv. R2←SHR R5

v. R3←CRC R7

One example is shown as follows:

| Micro-operation | *A* | *B* | *D* | *F* | $C_{in}$ | *H* | In Hex |
|---|---|---|---|---|---|---|---|
| R5← CRC (R3+R4) | 011 | 100 | 101 | 001 | 0 | 110 | 7296h |

The necessary bits for the control word are presented in Table 2.

**Table 2: 16-bit control word sequence**

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| *A* | | | *B* | | | *D* | | | *F* | | | $C_{in}$ | *H* | | |

9. Prepare a flow chart that will count the number of 0's in register, R2, and then store the counts in register R5. Determine the outputs of the R5 (in binary) and R2 (in decimal) registers as well as of the carry flag after each clock cycle or timing state. Determine the number of states that are required to complete the operation.

| **Timing States** | **R2** | | | | | | | | **C** | **R5** |
|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| T1 | | | | | | | | | | |
| T2 | | | | | | | | | | |
| T3 | | | | | | | | | | |
| T4 | | | | | | | | | | |
| T5 | | | | | | | | | | |
| T6 | | | | | | | | | | |
| T7 | | | | | | | | | | |
| T8 | | | | | | | | | | |

Q-1

given,

$$f_{osc} = 24\,MHz$$

$$UBRR_n = 111010100101 = 3749\ (\text{decimal})$$

for asyncnonous nonmal mode,

$$\text{Baud rate} = \frac{f_{osc}}{16(UBRR_n+1)} = \frac{24\times10^6}{16(3749+1)}$$

$$= 400\ bps$$

$$\text{Baud error rate} = \frac{\text{stnd. baud rate} - \text{calculated baud rate}}{\text{Stand baud rate}} \times 100$$

$$= \frac{300-400}{300} \times 100$$

$$= -33.3\% > \pm 2\%$$

So, there will be a communication error.

Q-2

for fast pwm in inverting mode using Time0 to count up to 235, required registers are

TCCR0A — to set the timer 0.

$COM0A1 = 1 \rightarrow$ set OC0A to clear on compare match

$COM0A0 = 0 \rightarrow$ set OC0A to clear on compare match.

WGMO1 = 1 → set Timer0 to fast PWM mode.

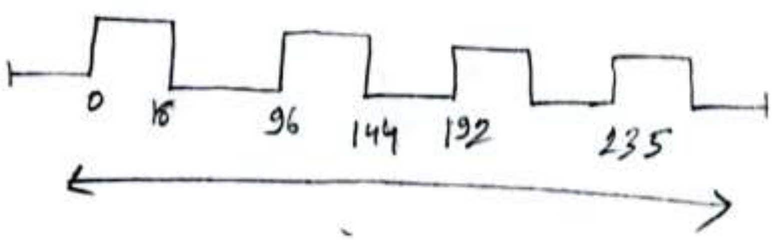
WGM00 = 1 → set Time0 to fast PWM mode.

TCCR0B → to set the prescaler for time0.

→ CS02 = 0 → prescaler of 1.
→ CS01 = 0 → prescaler of 1. ] no prescaler.
→ CS00 = 1 → prescaler of 1.

OCR0A = 235 → set compare value to 235.

Wave form:-




approximate dutycycle: 7.81%.

Q-3

Inverting mode,

$D = 55\%$

We know,

$\therefore OCR0A = 255 - \frac{256D}{100}$

$= 255 - \frac{256 \times 55}{100}$

$= 114.2 \simeq 114$

Non inverting mode:

$D = 40\%$

We know,

$OCR0B = \frac{256 \times 40}{100} - 1$

$= 101.4 \simeq 101$

3

Q-4

It is using timer0 in fast PWM mode with Prescaller of 64.

frequency, f = 8MHz

$$timer0 = \frac{8MHz}{64} = 125\ kHz$$

Operating frequency,

$$f_{pwm} = \frac{f_{t0}}{256 \times Prescaler}$$

$$= \frac{125\ kHz}{256 \times 64} = 7.63\ Hz$$

Duty cycle for OCR0A,

$$OCR0A = \frac{256D}{100} - 1$$

$$\Rightarrow 200 + 1 = \frac{256D}{100}$$

$$\Rightarrow D = \frac{201 \times 100}{256}$$

$$= 78.52\%$$

Duty cycle for OCR0B

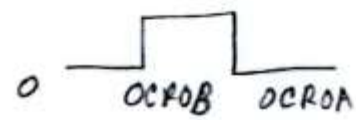
$$\therefore OCR0B = \frac{256D}{100} - 1$$

$$\Rightarrow 141 = \frac{256D}{100} - 1$$

$$\Rightarrow 142 = \frac{256D}{100}$$

$$\Rightarrow D = \frac{142 \times 100}{256} \quad \therefore D = 56.47\%$$

The webform of PWM,




OCR0A signal is high when D = 78.52 %

OCR0B " " " " D = 55.47 %

Q-5

| S | F | x | Y | $C_{in}$ |
|---|---|---|---|---|
| 0 | A+B | A | B | 0 |
| 1 | A-B | A | B' | 1 |

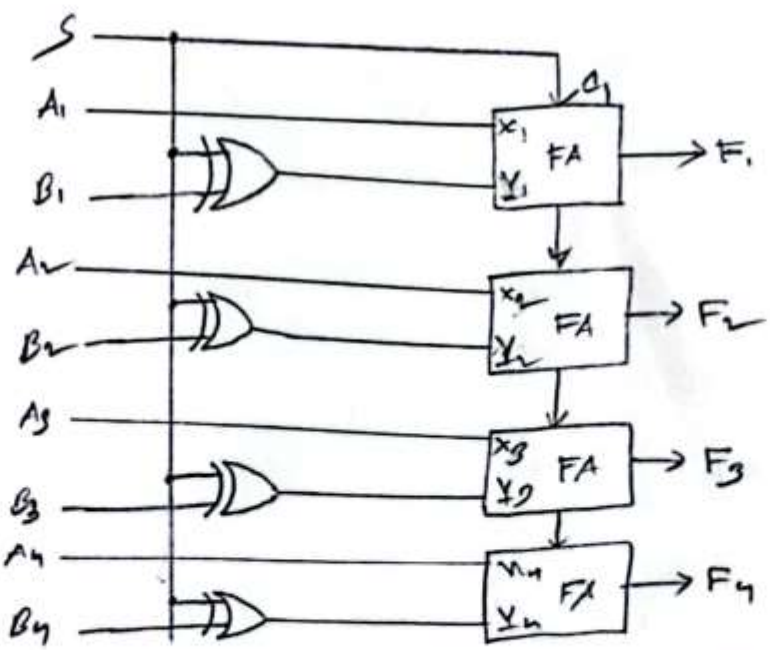
XOR Truth-table

| A | B | C |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

$X_i = A_i$

$Y_i = B_i \text{ XOR } S$

$C_{in} = S$



5

## Q-6

### $X_i$

| $S_2 \backslash S_1S_0$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | A | A | A | A |
| 1 | A | A | A+B | A+$\bar{B}$ |

| $S_2 \backslash S_1S_0$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | A | A | A | A |
| 1 | A | A | A | A |

$= A$

$$X_i = A + S_2 S_1 S_0 B + S_2 S_1 \bar{S_0} \bar{B}$$

| $S_2 \backslash S_1S_0$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | | | | |
| 1 | | | B | $\bar{B}$ |

### $Y_i$

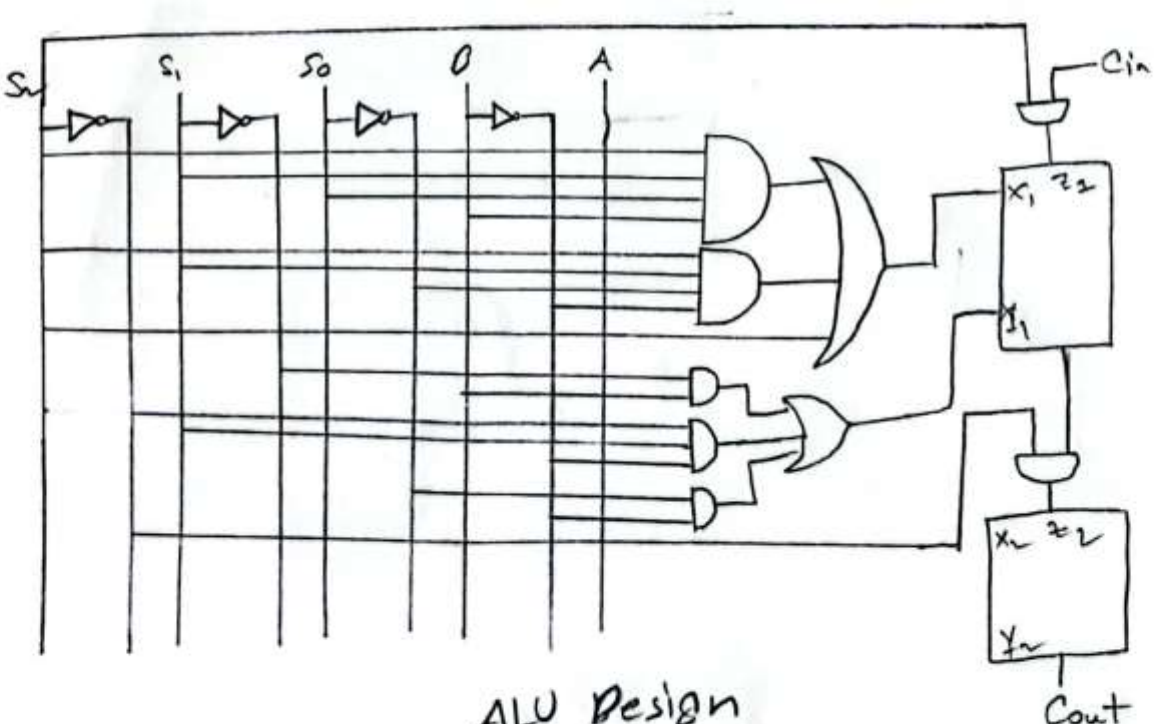
| $S_2 \backslash S_1S_0$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 1 | B | 1 | $\bar{B}$ |
| 1 | 1 | B | 0 | B |

$$Y_i = \bar{S_1} B + \bar{S_2} S_1 \bar{B} + \bar{S_0} \bar{B}$$

### $Z_i$

| $S_2 \backslash S_1S_0$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | $C_{in}$ | $C_{in}$ | $C_{in}$ | $C_{in}$ |
| 1 | 0 | 0 | 0 | 0 |

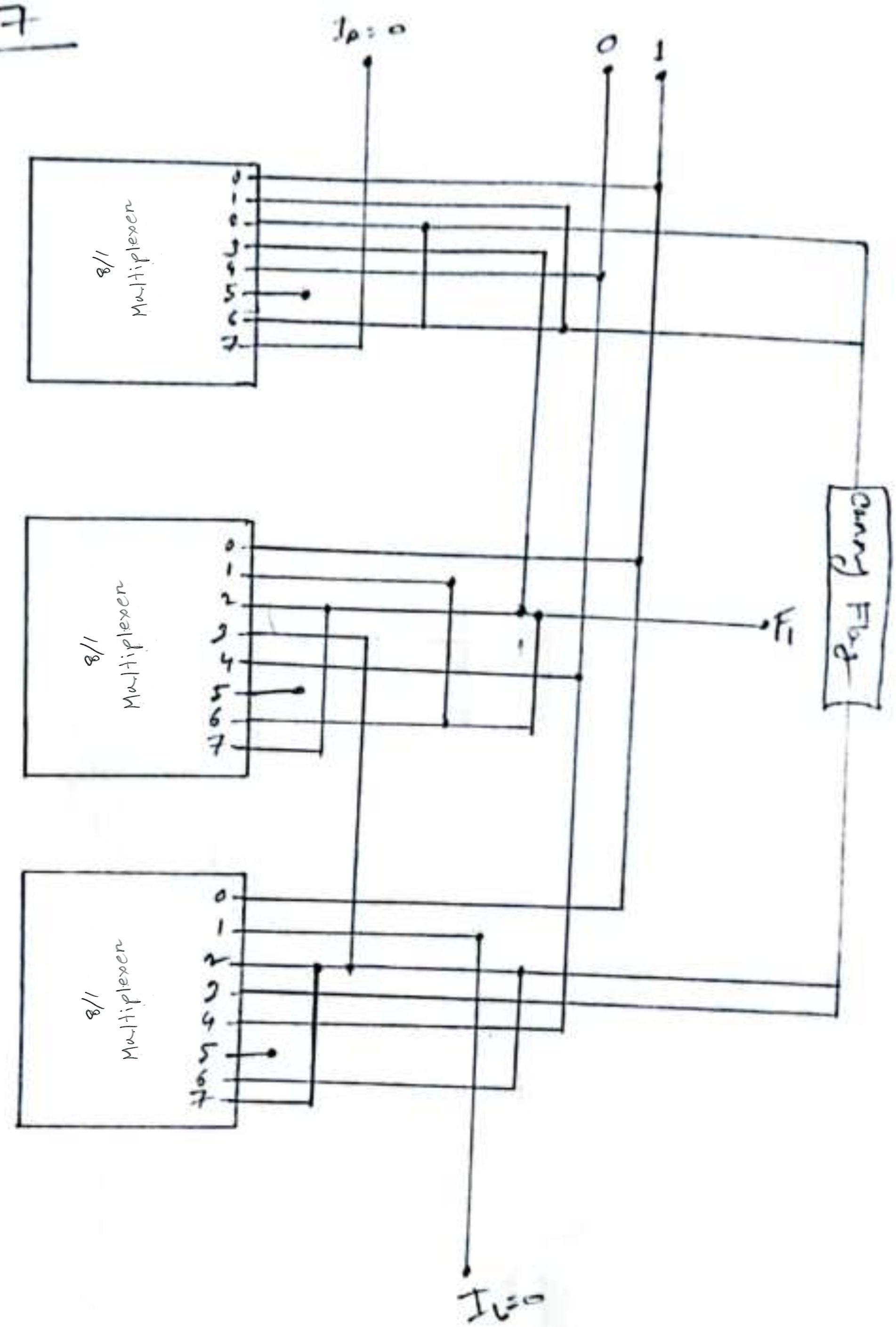
$$Z_i = \bar{S_2} C_{in}$$




ALU Design

6

Q-7


8/1 Multiplexer
8/1 Multiplexer
8/1 Multiplexer
0
1
F1
Carry Flag

Q- 8

(i) $R_7 \longleftarrow R_3 + R_4$

| A | B | D | F | Cin | H | Hex |
|---|---|---|---|---|---|---|
| 010 | 011 | 000 | 000 | 0 | 100 | 4004h |

(ii) $R_3 = SHL\ R_3$

| A | B | D | F | Cin | H | Hex |
|---|---|---|---|---|---|---|
| 011 | 000 | 000 | 001 | 0 | 110 | 6016h |

(iii) $R_5 \longleftarrow R_2$

| A | B | D | F | Cin | H | Hex |
|---|---|---|---|---|---|---|
| 001 | 100 | 000 | 000 | 0 | 100 | 3004h |

(iv) $R_2 \longleftarrow SHR\ R_5$

| A | B | D | F | Cin | H | Hex |
|---|---|---|---|---|---|---|
| 010 | 101 | 000 | 010 | 0 | 110 | 542ch |

(v) $R_3 \longleftarrow CRC\ R_7$

| A | B | D | F | Cin | H | Hex |
|---|---|---|---|---|---|---|
| 110 | 000 | 000 | 001 | 0 | 110 | c003h |

8

Q- 9

| Time State | R2 | | | | | | | | C | R5 |
|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| $T_1$ | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| $T_2$ | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| $T_3$ | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 2 |
| $T_4$ | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 3 |
| $T_5$ | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 3 |
| $T_6$ | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 4 |
| $T_7$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 4 |
| $T_8$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 4 |