EEE 3101: Digital Logic and Circuits

IC & Logic Gates

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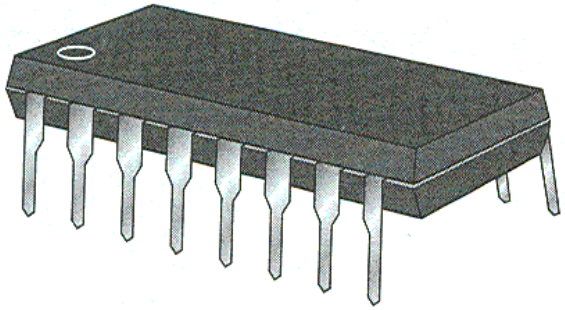
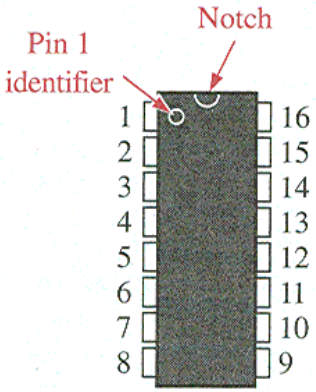
INTEGRATED CIRCUITS

- Digital circuits are constructed with integrated circuits.
- An integrated circuit (abbreviated IC) is a small silicon semiconductor crystal, called a *chip*. containing the electronic components for the digital gates.
- The various gates are interconnected inside the chip to form the required circuit.
- The chip is mounted in a ceramic or plastic container, and connections are welded to external pins to form the integrated circuit.





When working with an IC or Integrated Circuit as an engineer we should be aware of the following factors:

1. The integration level
2. The logic level parameters
3. The logic family or technology
4. The performance parameters

Integration Level

The integration level of an IC or a semiconductor chip gives us an idea about the number of gates that are present in the chip.

Integration Level for Integrated Circuits.

- Small Scale Integration (SSI) (<12 gates/chip).
- Medium Scale Integration (MSI) (<100 gates/chip).
- Large Scale Integration (LSI) (…1K gates/chip).
- Very Large Scale Integration (VLSI) (…10K gates/chip).
- Ultra Large Scale Integration (ULSI) (…100K gates/chip).
- Giga Scale Integration (GSI) (…1M gates/chip).

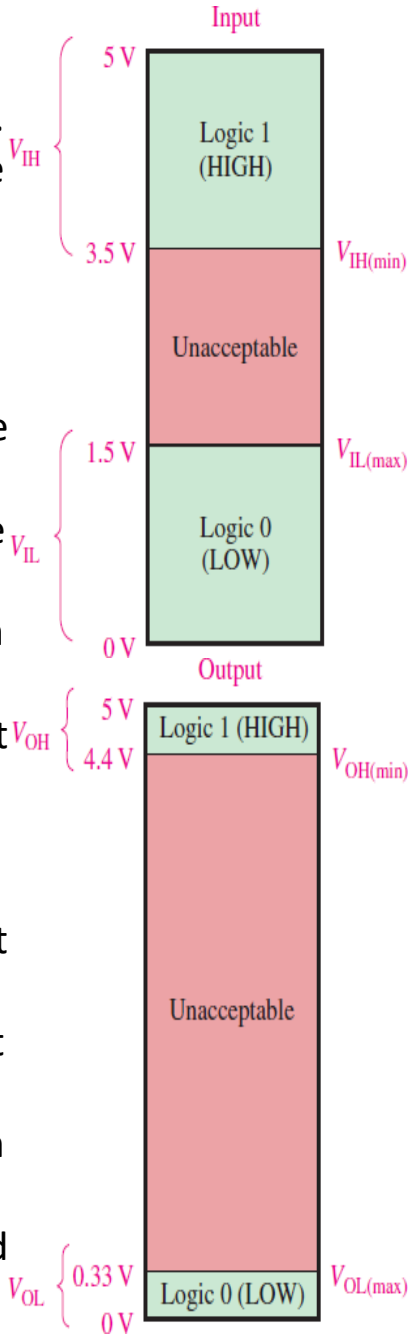
Examples:

- Pentium III Coppermine(32-bit, large cache): 21,000,000 gates
- Pentium 4 Willamette (32-bit, large cache): 42,000,000 gates
- Core 2 Duo Conroe (dual-core 64-bit, large caches): 291,000,000 gates
- ARM Cortex-A9 (32-bit, (optional) SIMD, caches):26,000,000 gates
- Atom (32-bit, large cache): 47,000,000

Logic Level Parameters

Different Logic Families usually operate at different voltage and current levels. Before knowing the particular levels for different families, one should first be acquainted with the logic level parameters and their definitions.

The voltages used to represent a '1' or '0' are called logic levels



Voltage Parameters

High-Level Output Voltage, V_{OH} (MIN): This is the minimum output voltage available at the output under stated loaded condition which corresponds to logic '1'.

Low-Level Output Voltage, V_{OL} (MAX): This is the maximum output voltage available at the output under stated loaded condition which corresponds to logic '0'

High-Level Input Voltage, V_{IH} (MIN): This is the minimum voltage required at an input to be recognized as a logic '1'.

Low-Level Input Voltage, V_{IL} (MAX): This is the maximum voltage at an input which will be recognized as a logic '0'.

Current Parameters

High-Level Output Current, I_{OH} : This is the maximum current at the output under specified loaded condition that a gate can sink at logic level '1'.

Low-Level Output Current, I_{OL}: This is the maximum current a gate can sink at specified load at logic '0',

High-Level Input Current, I_{IH}: This is the minimum current a supply must provide in order to maintain the logic '1'.

Low-Level Input Current, I_{IL}: This is the minimum current that must be provided in order maintain a logic '0'.

Digital Logic Families

Digital integrated circuits are classified not only by their complexity or logical operation, but also by the specific circuit technology to which they belong. The circuit technology is referred to as a digital logic family.

The basic circuit in each technology is a NAND, NOR, or an inverter gate.

The Logic Families are :

- RTL → Resistor-Transistor Logic
- DTL → Diode Transistor Logic
- I^2L → Integrated Injection Logic
- ECL → Emitter Collector Logic
- TTL → Transistor Transistor Logic
- MOS→ Metal Oxide Semiconductor
- CMOS → Complementary MOS

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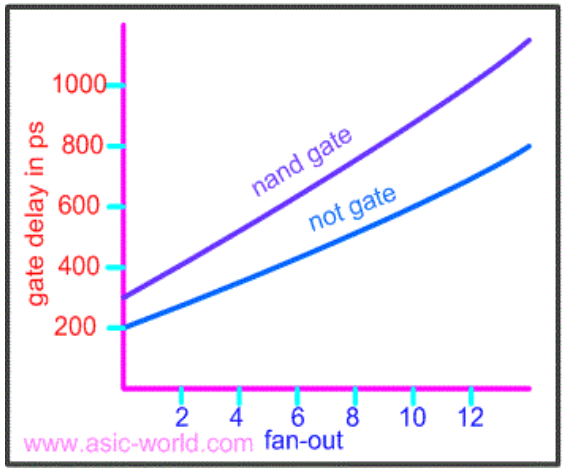
Performance parameters

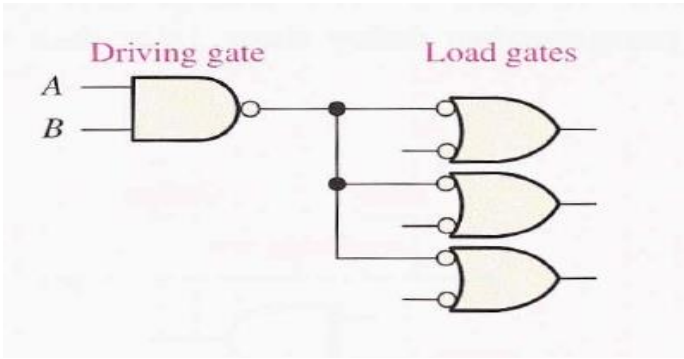
- The characteristics of IC digital logic families are usually compared by analyzing the circuit of the basic gate in each family.
- The most important parameters that are evaluated and compared are

  - ❖ Fan-Out
  - ❖ Fan-In
  - ❖ Power Dissipation
  - ❖ Propagation Delay
  - ❖ Speed-Power Product
  - ❖ Noise Margin

Fan-Out

- The fan-out of a gate specifies the number of standard loads that can be connected to the output of the gate without degrading its normal operation.
- A standard load is usually defined as the amount of current needed by an input of another gate in the same logic family. Sometimes the term *loading* is used instead of fan-out.
- This term is derived because the output of a gate can supply a limited amount of current, above which it ceases to operate properly and is said to be overloaded.
- Each input consumes a certain amount of current from the gate output, so that each additional connection adds to the load of the gate.
- Exceeding the specified maximum load may cause a malfunction because the circuit cannot supply the power demanded from it.
- The fan-out is the maximum number of inputs that can be connected to the output of a gate, and is expressed by a number.





- The fan-out of the gate is calculated from the ratio I_{OH}/I_{IH} or I_{OL} / I_{IL}
- For example, the standard TTL gates have the following values for the currents:

$$I_{OH} = 400\ \mu A$$

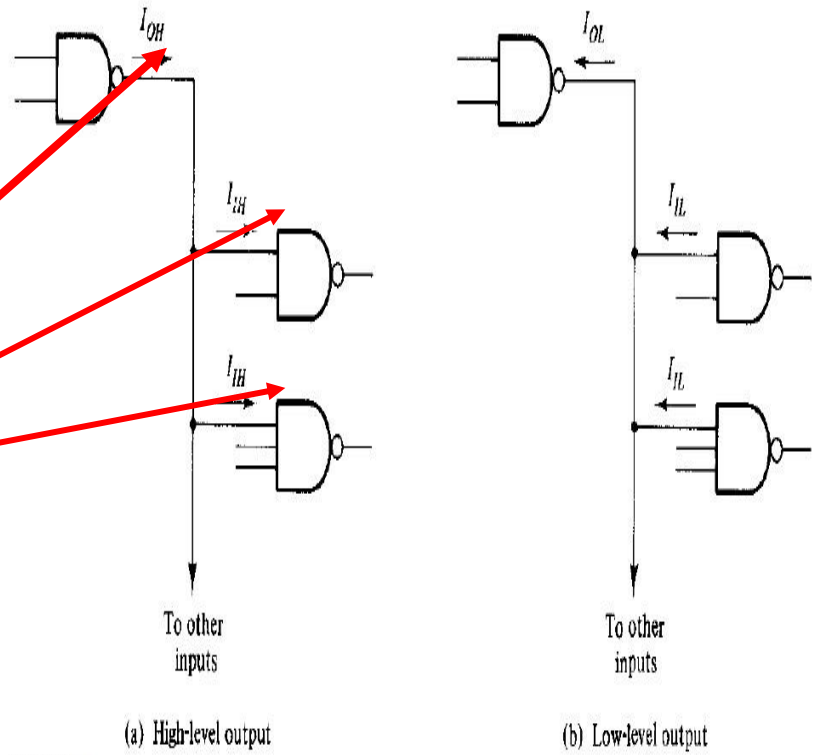
$$I_{IH} = 40\ \mu A$$

$$I_{OL} = 16\ mA$$

$$I_{IL} = 1.6\ mA$$

The two ratios give the same number in this case:

$$\frac{400\ \mu A}{40\ \mu A} = \frac{16\ mA}{1.6\ mA} = 10$$

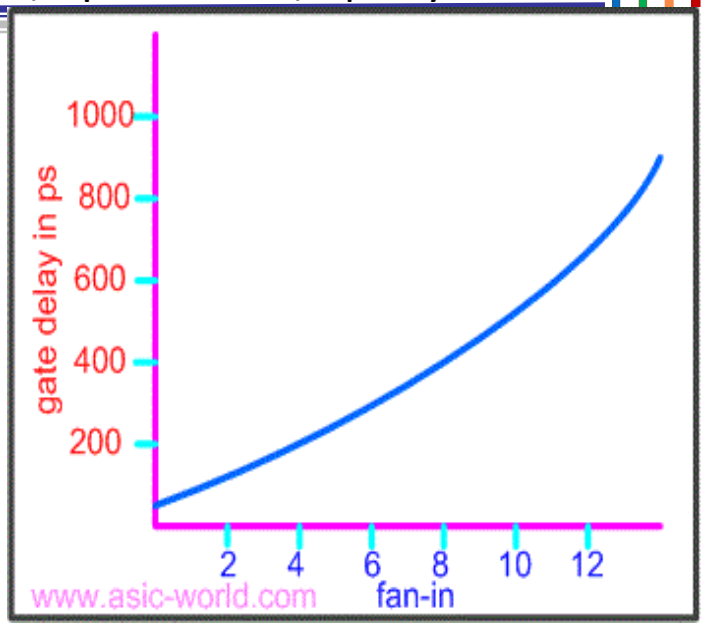


(a) High-level output (b) Low-level output

FIGURE 2
Fan-out computation

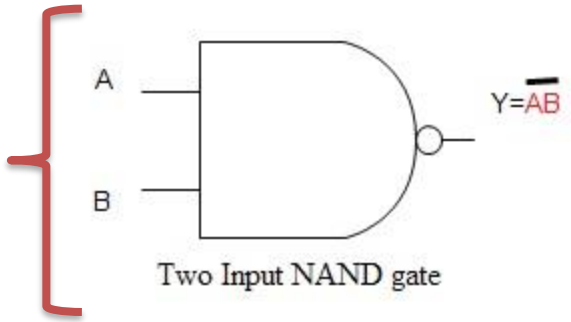
Fan-In:

It is the number of input that can be connected to a particular gate. As more inputs are connected the delay in the input side increases. Delay approximately has a quadratic relationship with Fan-in.



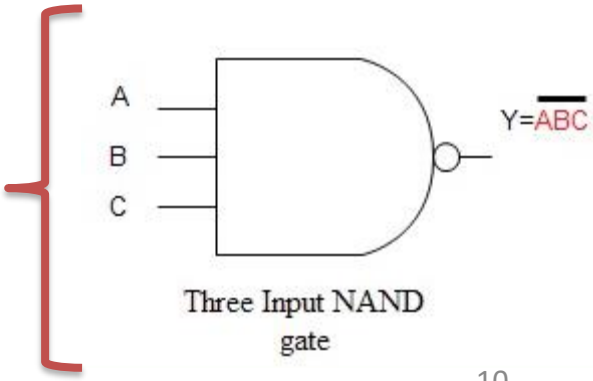
- The fan-in defined as the maximum number of inputs that a logic gate can accept.
- If number of input exceeds, the output will be undefined or incorrect.
- It is specified by manufacturer and is provided in the data sheet.

Fan In = 2



Two Input NAND gate

Fan In = 3



Three Input NAND gate

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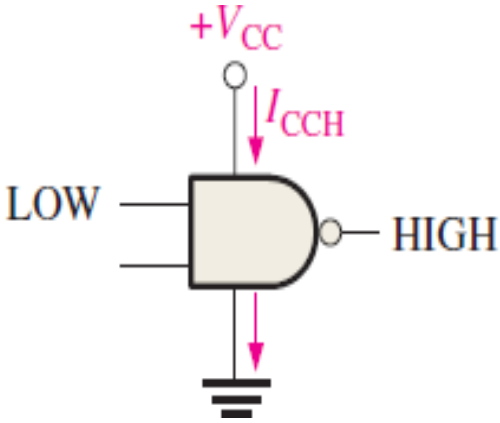
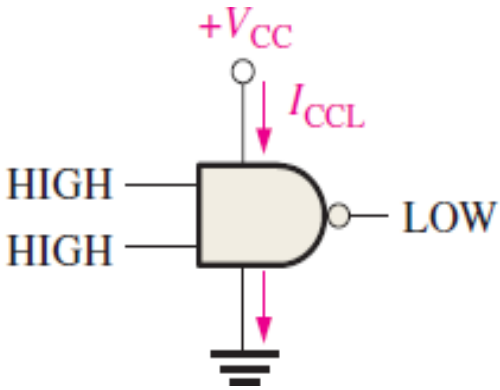
Power Dissipation

A gate draws in current both in HIGH and LOW states. Therefore, in both states a gate dissipates power. The current associated with HIGH state is named I_{CCH} and the current associated with LOW state is named I_{CCL}. Therefore,



Power Dissipation in HIGH state, $P_{DH} = V_{CC}I_{CCH}$
Power Dissipation in LOW state, $P_{DL} = V_{CC}I_{CCL}$

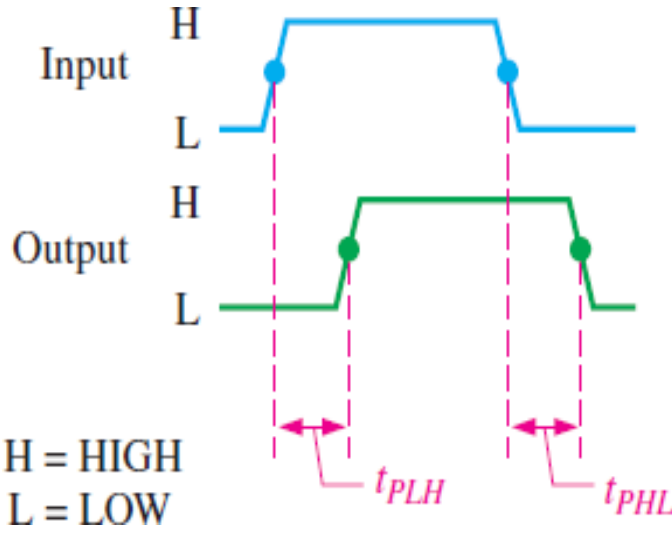
So the average power dissipated in a cycle with duty cycle of X%is,



$$\mathbf{PD} = \frac{(\mathbf{X} \times \mathbf{P_{DH}}) + \left((\mathbf{100} - \mathbf{X})\mathbf{P_{DL}}\right)}{\mathbf{100}}$$

Propagation Delay

When a signal passes through a logic circuit, it always experiences a time delay. The time elapsed between 50% change in input wave-form to the 50% change in output wave-form.



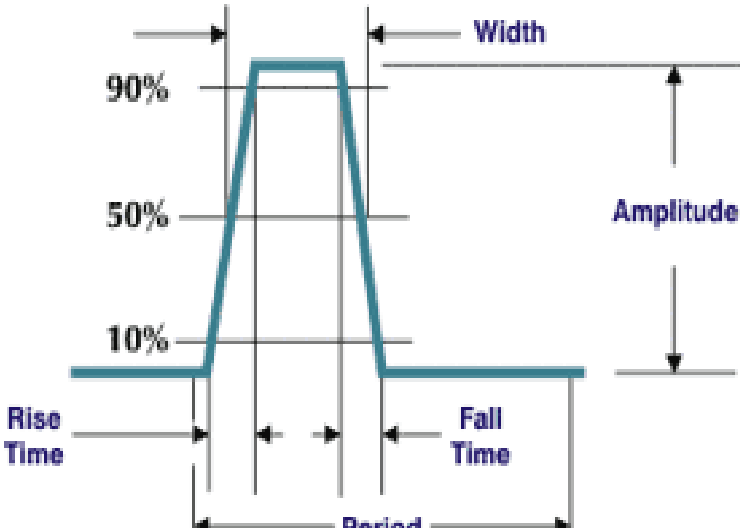
T_{pHL}: Propagation delay for High to Low.

T_{pLH}: Propagation delay for Low to High.

$$t_{PD} = \frac{1}{2}(t_{PHL} + t_{PLH})$$

Time Rise, t_r: The time required for a logic to rise from 10% of its value to 90% of the value.

Time Fall, t_f: The time required for the logic to fall from 90% of its value to 10% of its value.



Speed Power Product

It is a very important parameter of comparison for logic circuit where both power dissipation and propagation delay are together needed to be considered. The speed power product and its significance can be understood from the following equation:

$$P_D = \frac{CV_{CC}V_L}{T_D}$$

where C is the capacitance, V_{CC} is the common collector voltage, V_L is the logic swing of voltage and T_D is the propagation delay. We can rewrite this equation as,

$$P_D T_D = CV_{CC}V_L$$

For a logic family, V_{CC}, C and V_L are all constant. Therefore, if we decrease power dissipation then propagation delay will increase and if we decrease propagation delay power dissipation will increase. Therefore, there will always be a trade-off between the two parameters. However, to decrease both we will need to change construction parameter.

The lower the speed-power the better.

Noise

- **Noise Immunity:** All electrical circuits are susceptible to noise. Noise is the presence of unwanted induced voltage in the electrical circuit. This unwanted induced voltage can disrupt the operation of a digital circuit. In order to not get adversely affected by noise the circuit should have some amount of noise immunity. Noise Immunity is the ability to tolerate unwanted voltage fluctuation.

- There are two types of noise to be considered :
  - **DC noise is** caused by a drift in the voltage levels of a signal.
  - AC noise is a random pulse that may be created by other switching signals.

- Noise margin is the maximum noise voltage added to an input signal of a digital circuit that does not cause an undesirable change in the circuit output.
- Noise margin is expressed in volts and represents the maximum noise signal that can be tolerated by the gate.

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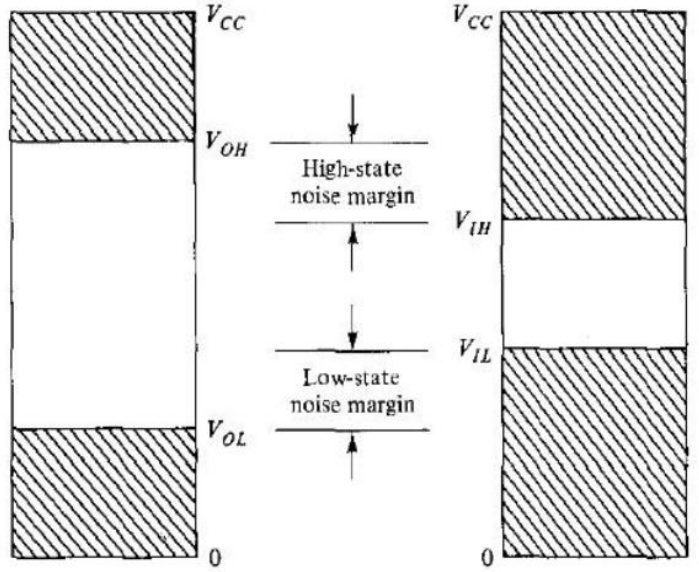
- There are two values of noise margin specified for a given logic circuit:
  - the HIGH level noise margin (V_{NH}) and
  - the LOW level noise margin (V_{NL}).
- There parameters are defined by the following equations:

$$V_{NH} = V_{OH(min)} - V_{IH(min)}$$

$$V_{NL} = V_{IL(max)} - V_{OL(max)}$$



(a) Output voltage range (b) Input voltage range

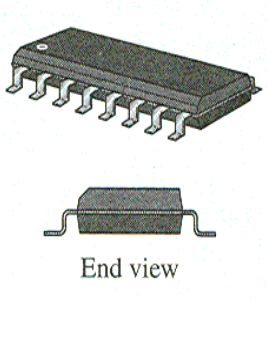
FIGURE

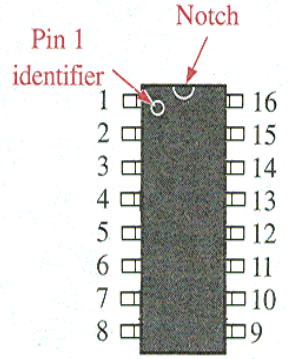
Signals for evaluating noise margin

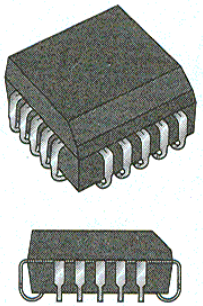
Fixed-Function Integrated Circuits

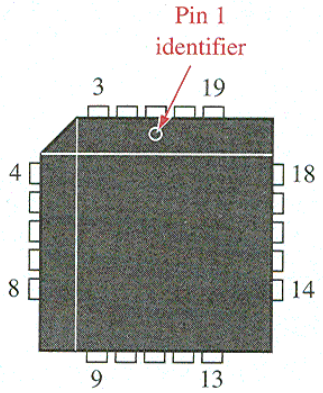
IC package styles

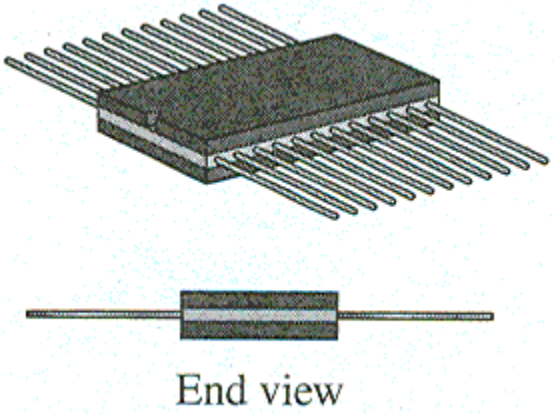
- Dual in-line package (DIP)
- Small-outline IC (SOIC)
- Flat pack (FP)
- Plastic-leaded chip carrier (PLCC)
- Leadless-ceramic chip carrier (LCCC)

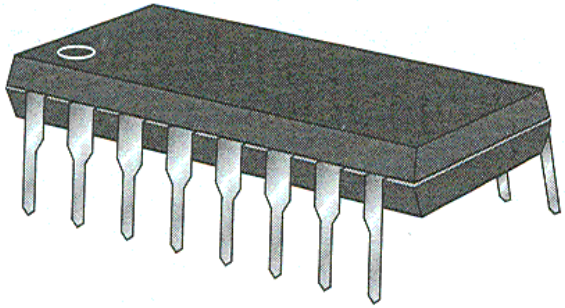


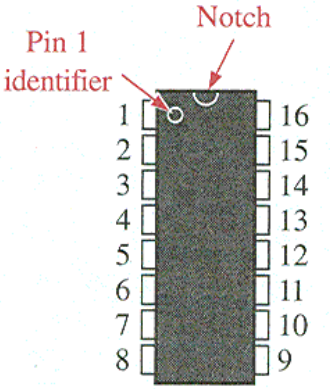












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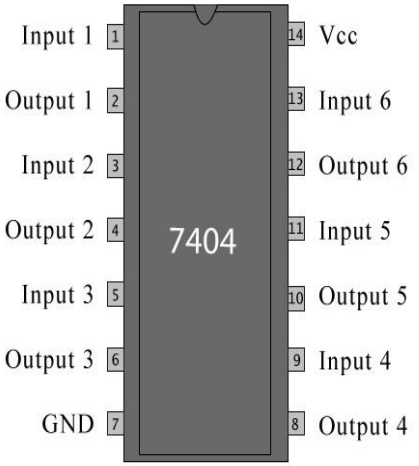

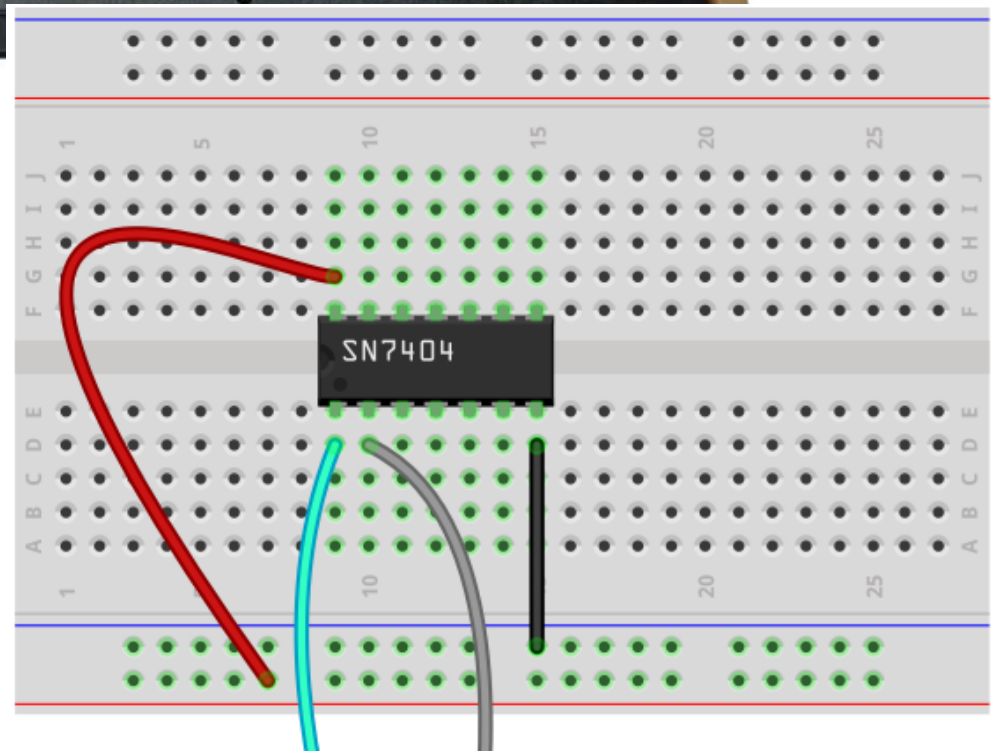

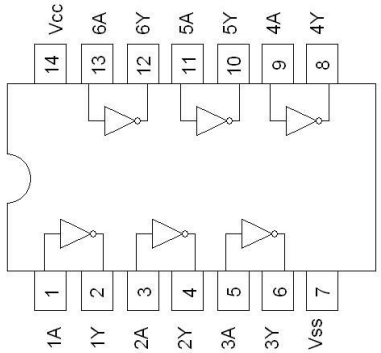

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Logic Circuits:

The manner in which a digital circuit responds to an input is referred to as a circuit logic.

In most basic logic circuits, logic gates are the fundamental building blocks from which all other Logic circuits and digital systems are constructed.

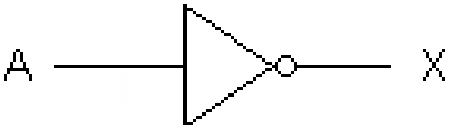
The digital circuit ICs are constructed using the following logic gates:

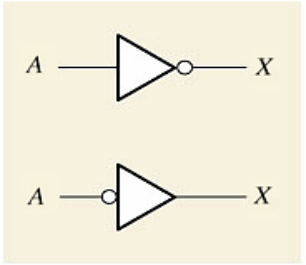
1) Basic Gates:
   - NOT Gate or Inverter
   - AND Gate
   - OR Gate
2) Universal Gates:
   - NAND Gate
   - NOR Gate
3) Exclusive Gates:
   - Exclusive-OR Gate
   - Exclusive-NOR Gate

Each gate can be represented by either:
1) Symbol,
2) Truth Table, or
3) Boolean Expression

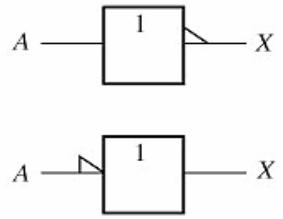
The Inverter

Logic diagram/Symbol:





Distinctive shape symbols



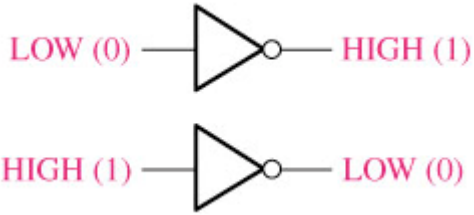
Rectangular outline symbols

The output of an inverter is always the complement (opposite) of the input.

Truth Table:

A	X
0	1
1	0

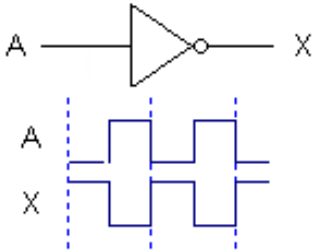
0 = LOW
1 = HIGH



When the input is LOW, the output is HIGH
When the input is HIGH, the output is LOW

Boolean expression:

$$X = \overline{A}$$



Pulsed waveforms

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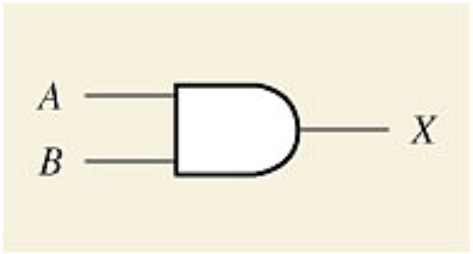
The AND Gate

Logic diagram/Symbol:



Distinctive shape symbol

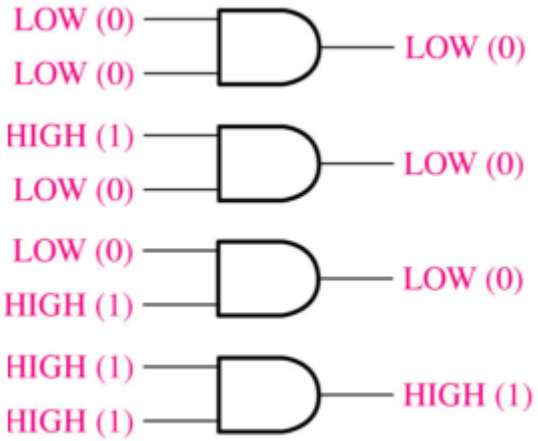
Rectangular outline symbol

The output of an AND gate is HIGH only when all inputs are HIGH.

Truth Table:

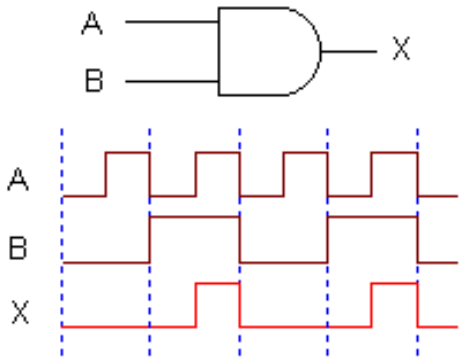
A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

0 = LOW
1 = HIGH



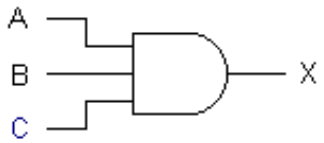
Boolean expression:

$$X = AB$$



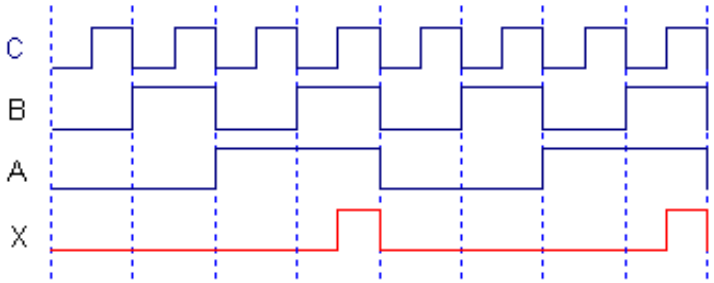
Pulsed waveforms

The AND Gate

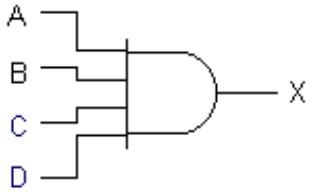


X = ABC

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

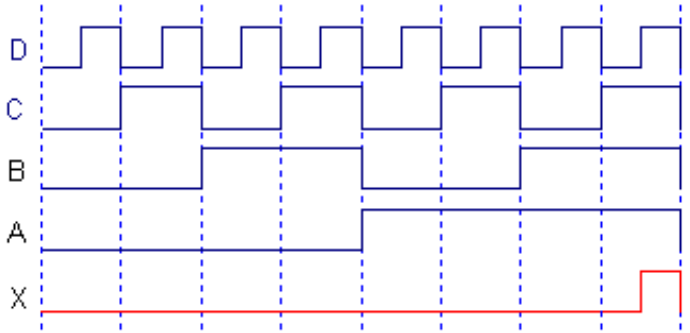


3-Input AND Gate



X = ABCD

A	B	C	D	X
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1



4-Input AND Gate

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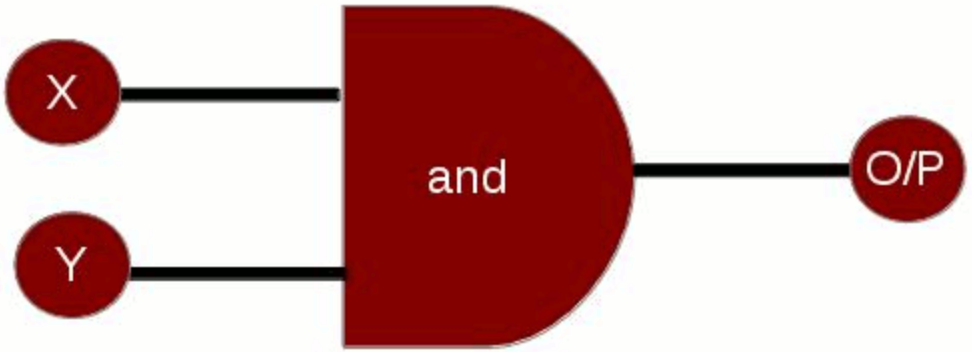
and Gate Animation

X	Y	O/P
0	0	0
0	1	0
1	0	0
1	1	1



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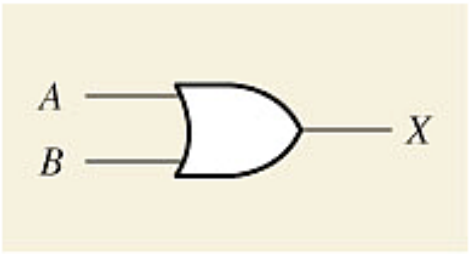
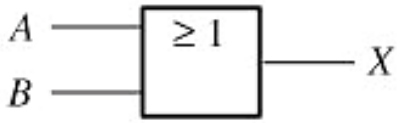
The OR Gate

Logic diagram/Symbol:



Distinctive shape symbol



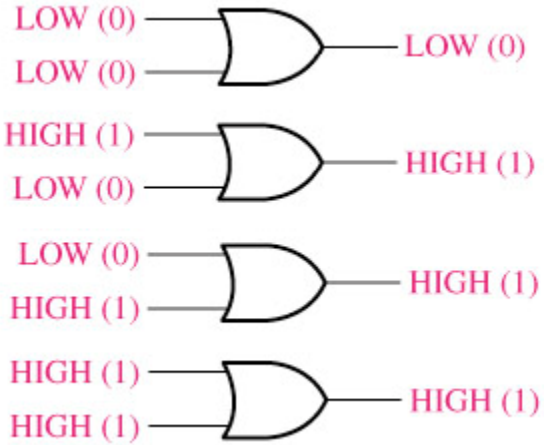
Rectangular outline symbol

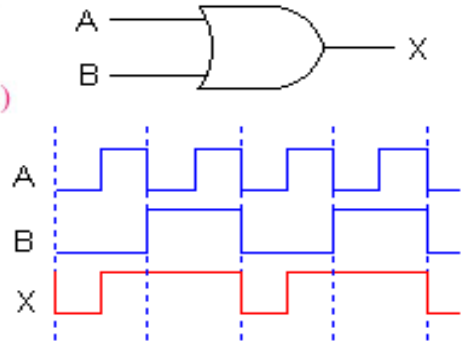
The output of an OR gate is HIGH whenever one or more inputs are HIGH

Truth Table:

A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

0 = LOW
1 = HIGH





Pulsed waveforms

Boolean expression:

$$X = A + B$$

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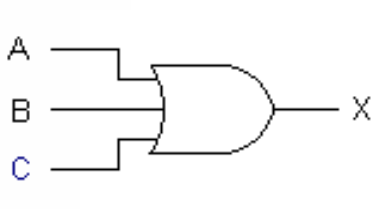
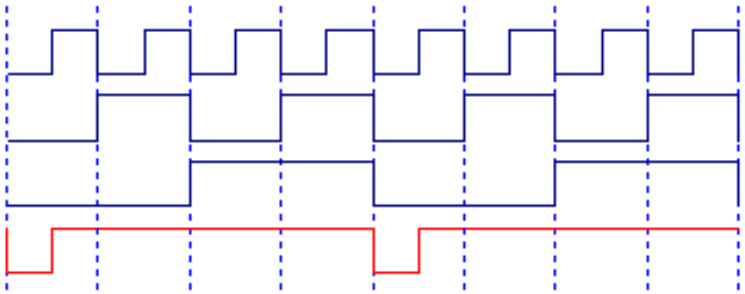
The OR Gate

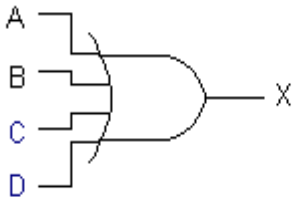


X = A+B+C

A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

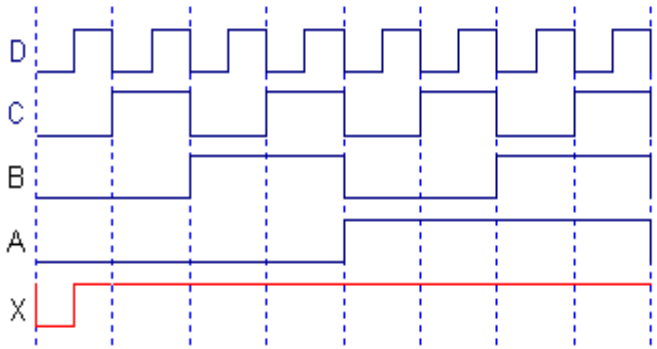


3-Input OR Gate



X = A+B+C+D

A	B	C	D	X
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1



4-Input OR Gate

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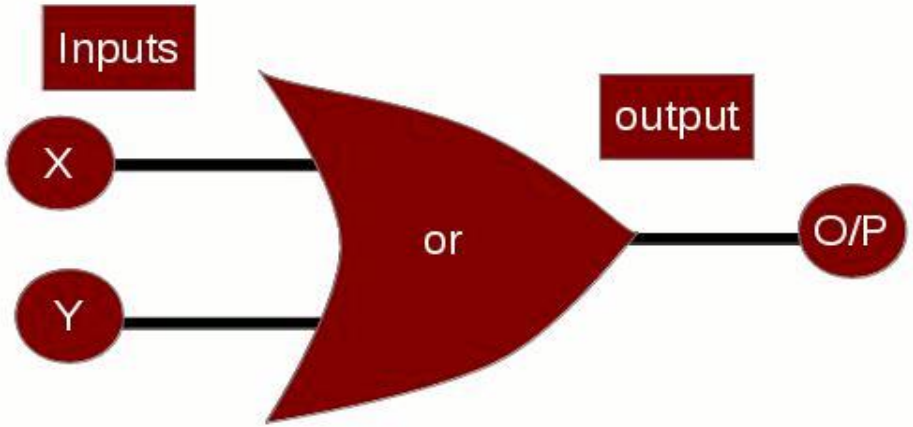
or Gate Animation

X	Y	O/P
0	0	0
0	1	1
1	0	1
1	1	1



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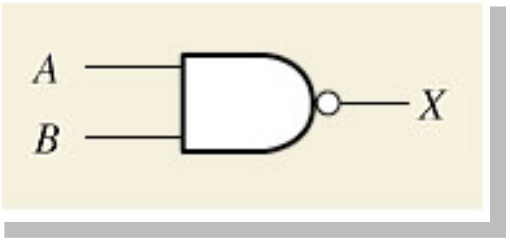
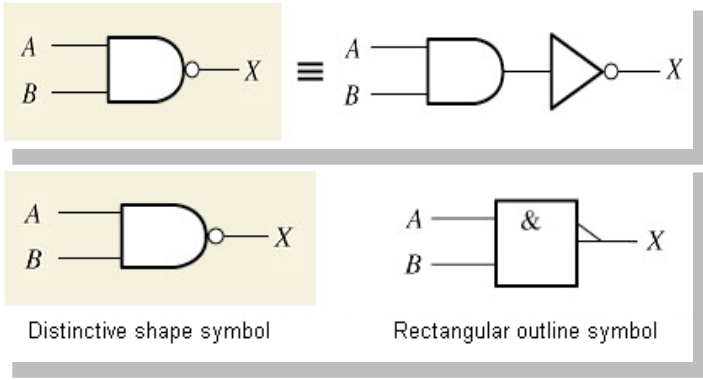
The NAND Gate

Logic diagram/Symbol:



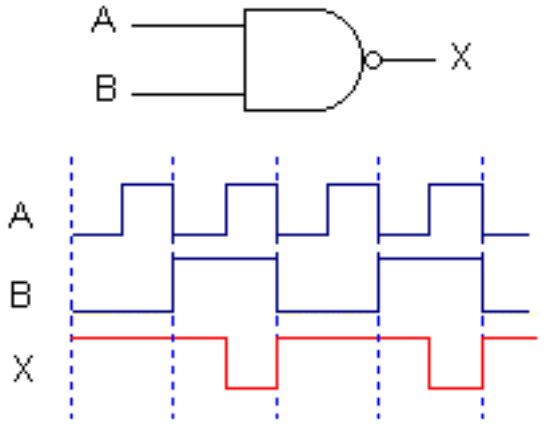


The output of a NAND gate is HIGH whenever one or more inputs are LOW.

Truth Table:

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

0 = LOW
1 = HIGH



Pulsed waveforms

Boolean expression:

$$X = \overline{AB}$$

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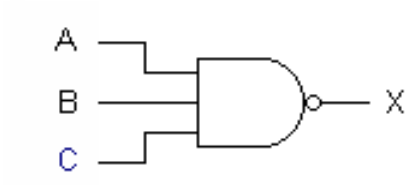
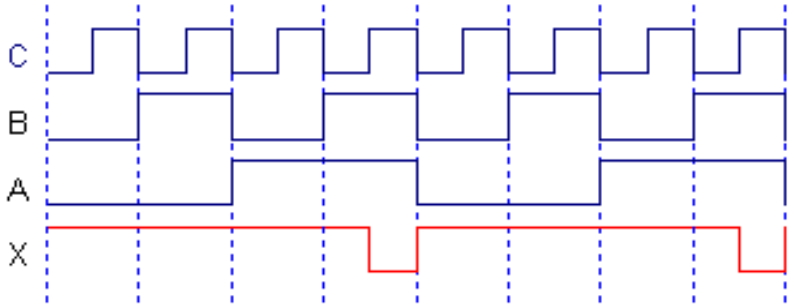
The NAND Gate

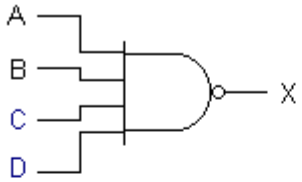


$X = \overline{ABC}$

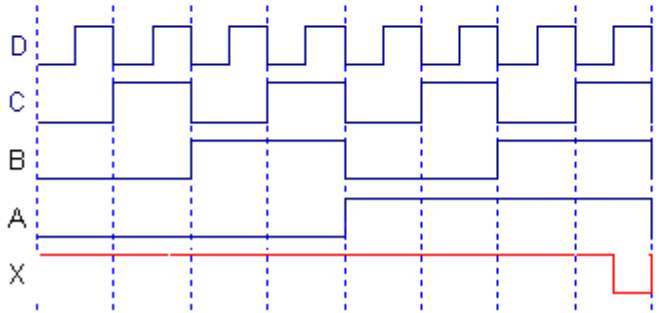
A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



3-Input NAND Gate



$X = \overline{ABCD}$



A	B	C	D	X
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

4-Input NAND Gate

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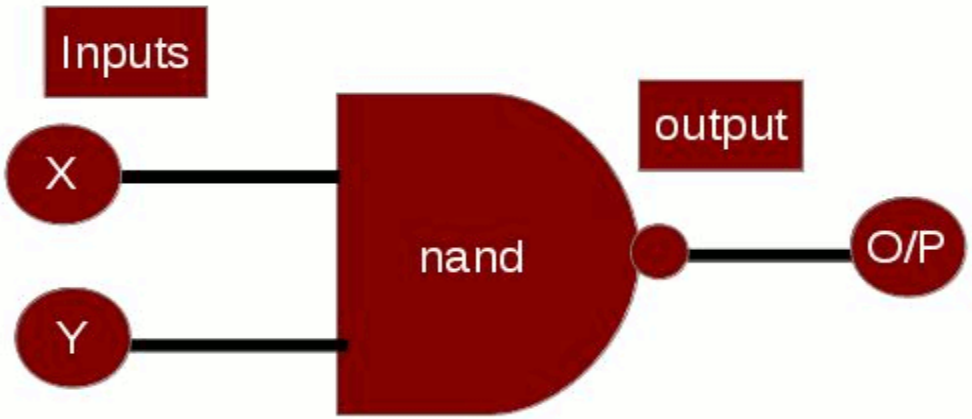
nand Gate Animation

X	Y	O/P
0	0	1
0	1	1
1	0	1
1	1	0



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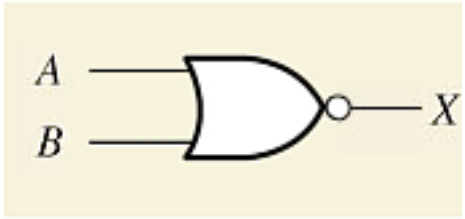
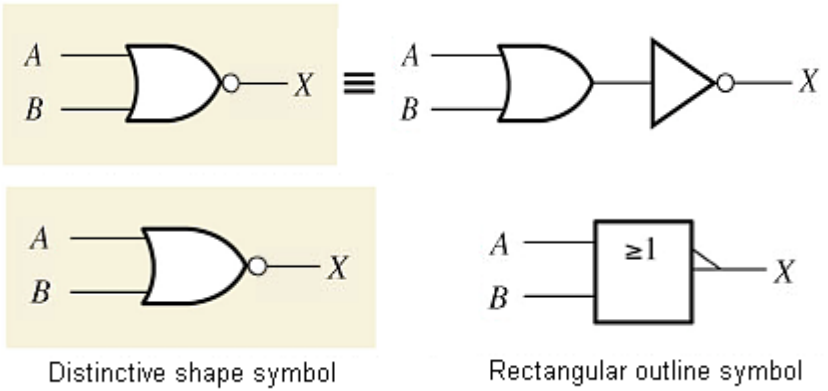
The NOR Gate

Logic diagram/Symbol:



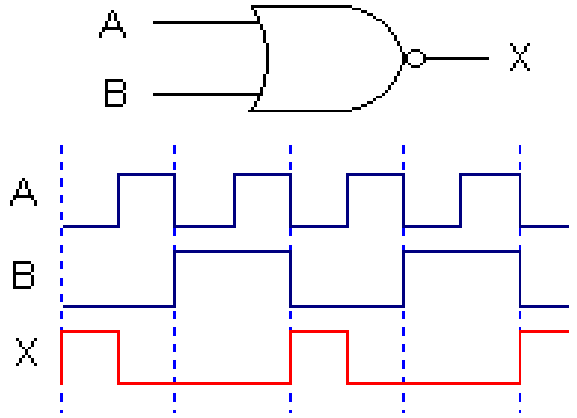


The output of a NOR gate is LOW whenever one or more inputs are HIGH.

Truth Table:

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

0 = LOW
1 = HIGH



Pulsed waveforms

Boolean expression:

$$X = \overline{A + B}$$

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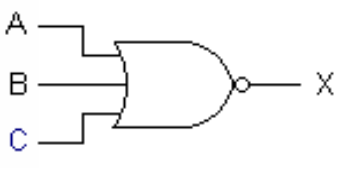
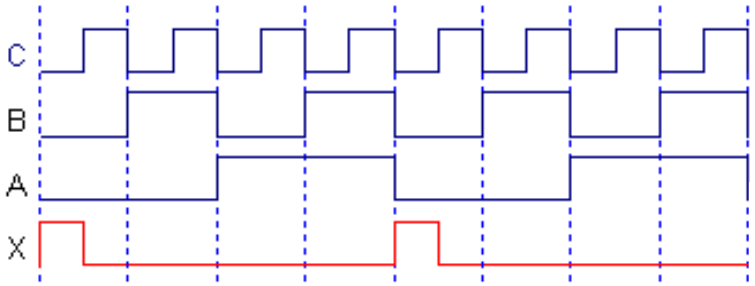
The NOR Gate

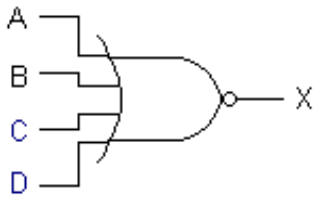


$$X = \overline{A+B+C}$$

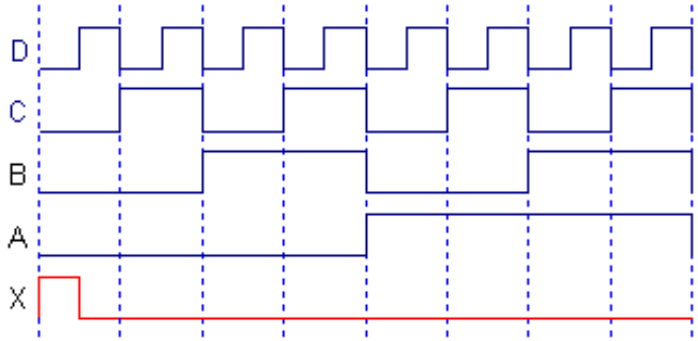
A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0



3-Input NOR Gate



$$X = \overline{A+B+C+D}$$



A	B	C	D	X
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

4-Input NOR Gate

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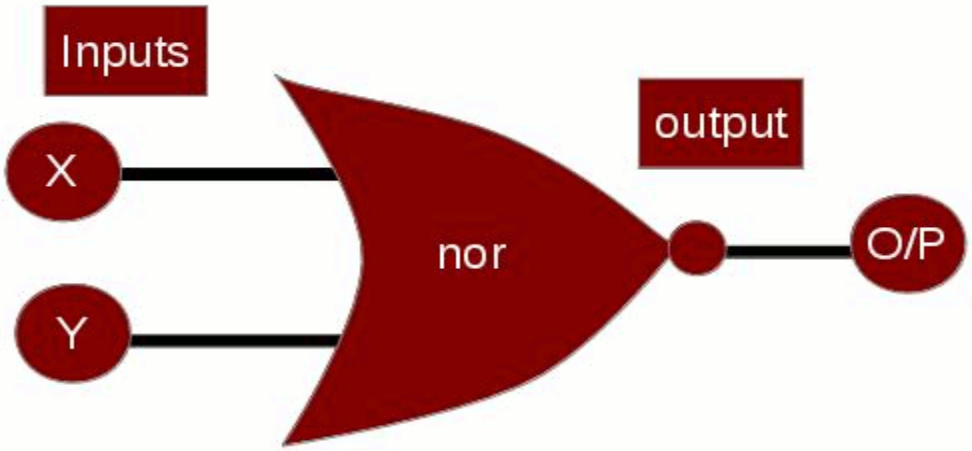
nor Gate Animation

X	Y	O/P
0	0	1
0	1	0
1	0	0
1	1	0



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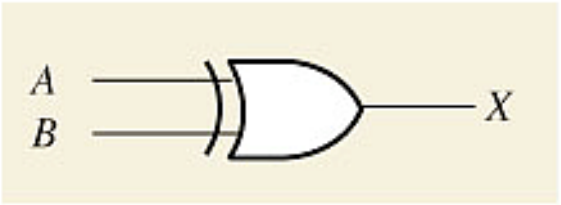
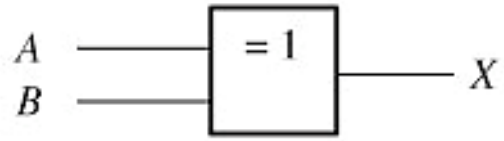
Exclusive-OR Gate

Logic diagram/Symbol:



Distinctive shape symbol



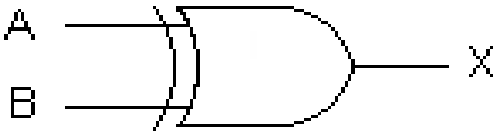
Rectangular outline symbol

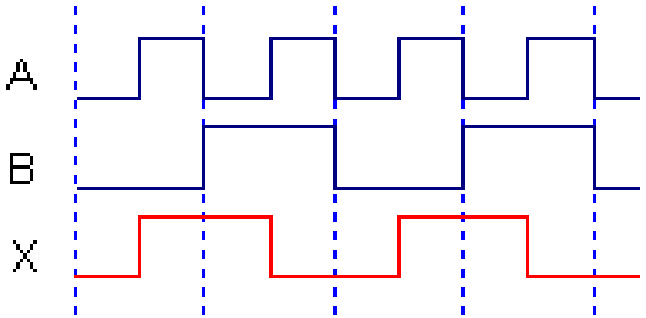
The output of an XOR gate is HIGH whenever the two inputs are different.

Truth Table:

A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

0 = LOW
1 = HIGH





Pulsed waveforms

Boolean expression:

$$X = A \oplus B$$

$$= \bar{A}B + A\bar{B}$$

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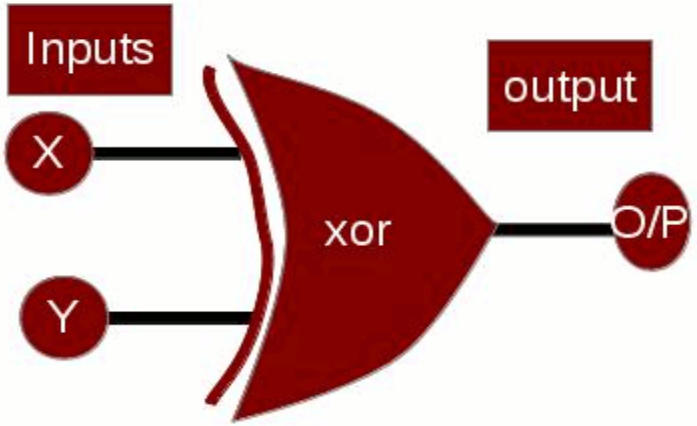
xor Gate Animation

X	Y	O/P
0	0	0
0	1	1
1	0	1
1	1	0



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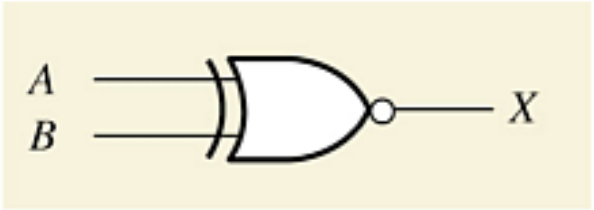
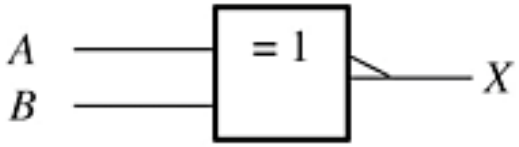
Exclusive-NOR Gate

Logic diagram/Symbol:



Distinctive shape symbol



Rectangular outline symbol

The output of an XNOR gate is HIGH whenever the two inputs are identical.

Truth Table:

A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

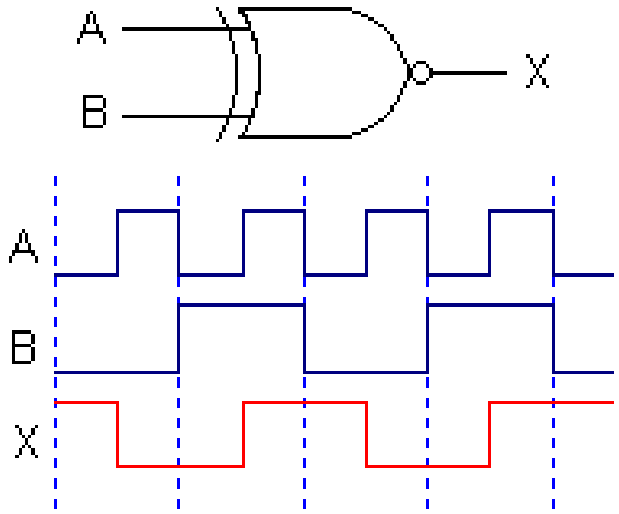
0 = LOW

1 = HIGH

Boolean expression:

$$X = \overline{A \oplus B} = A \odot B$$

$$= \bar{A}B + A\bar{B}$$



Pulsed waveforms

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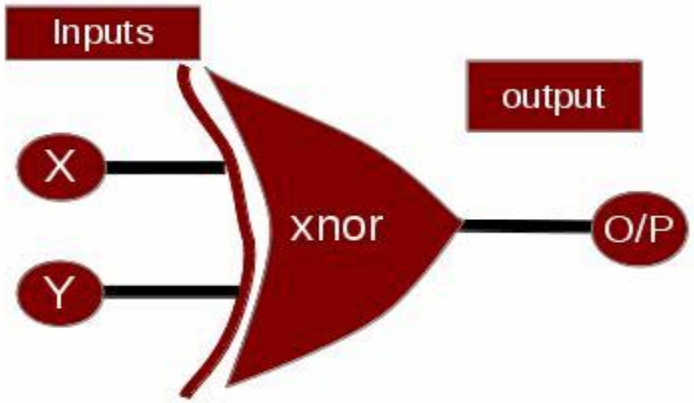
xnor Gate Animation

X	Y	O/P
0	0	1
0	1	0
1	0	0
1	1	1



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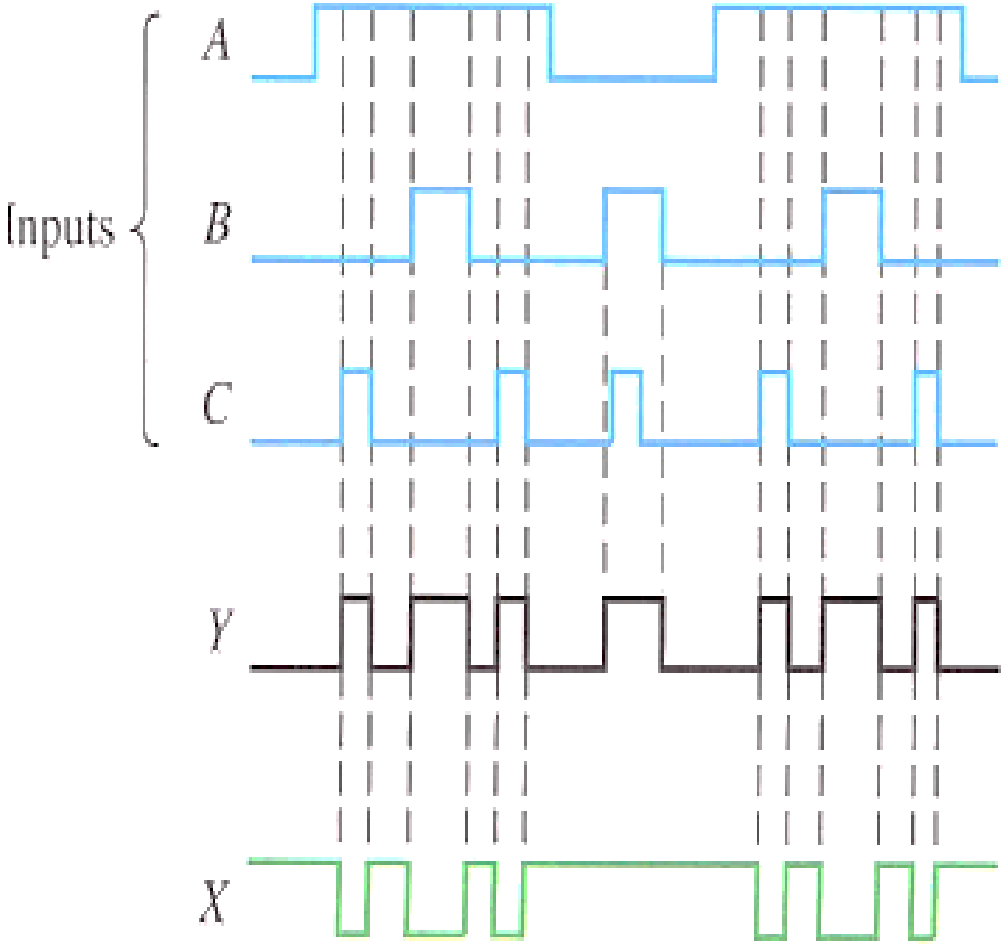
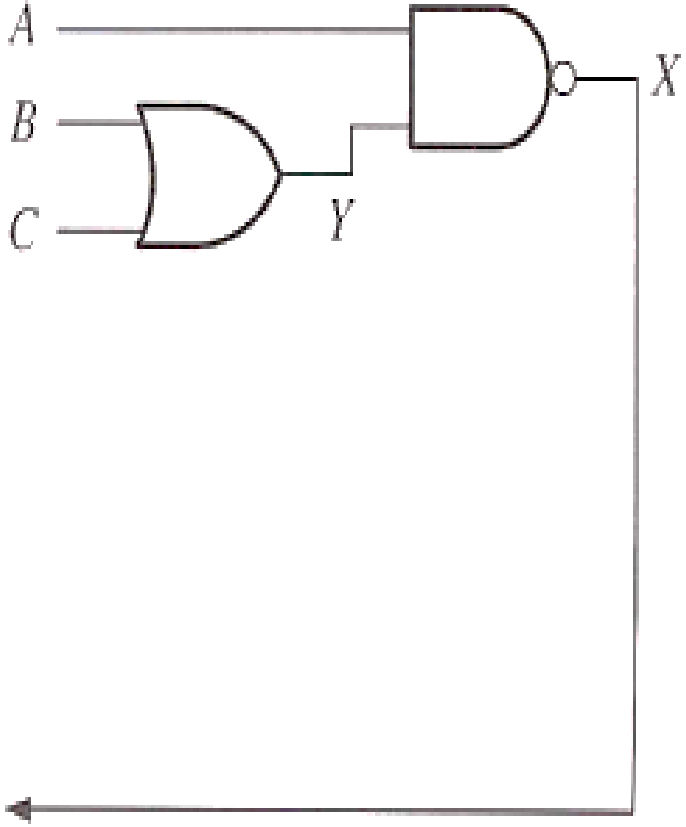
Logic Circuit Operation with Pulse Waveform Inputs:

Example 1:





$$X = \overline{A(B + C)} = \overline{AB + AC}$$

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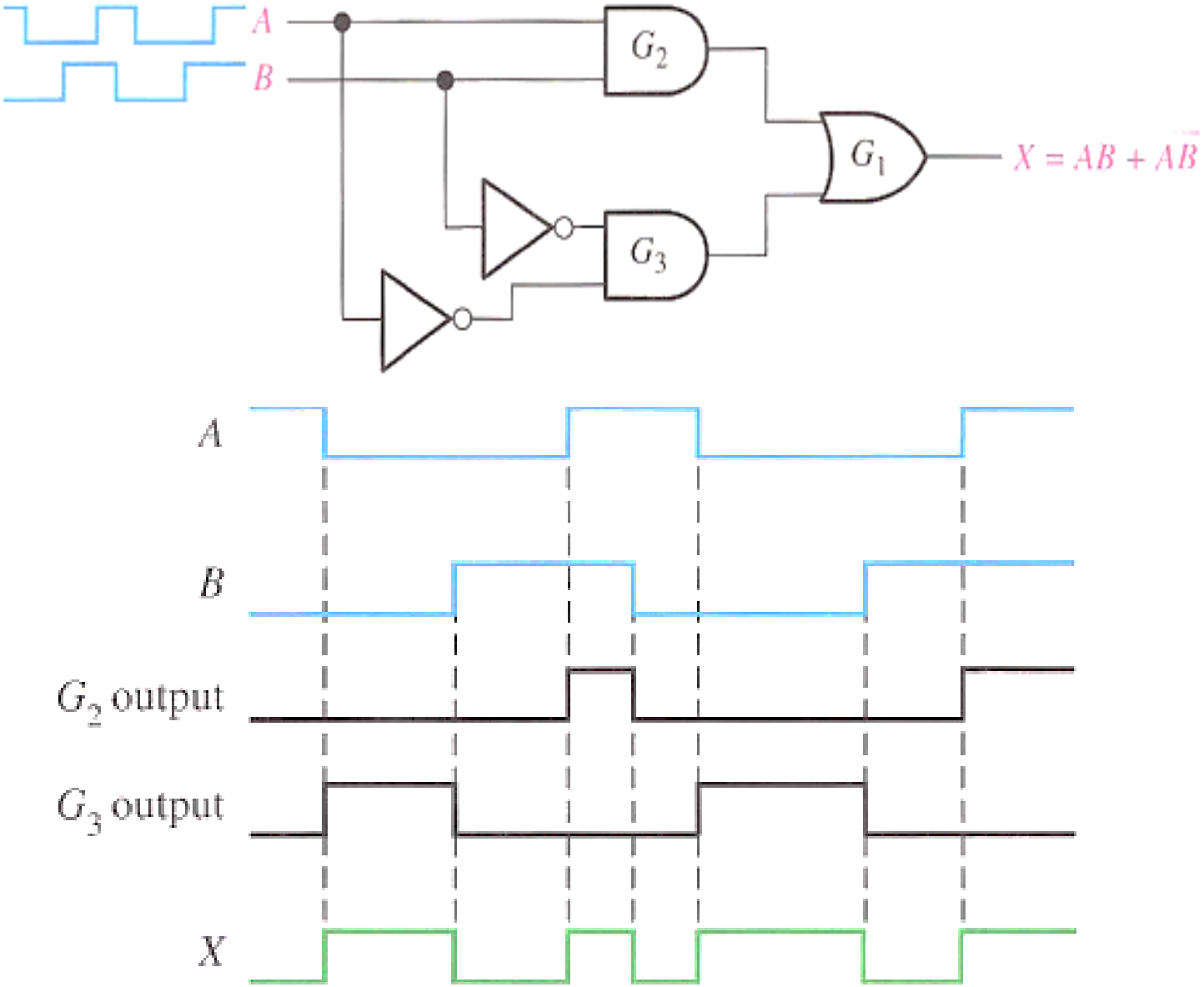
Example 2:



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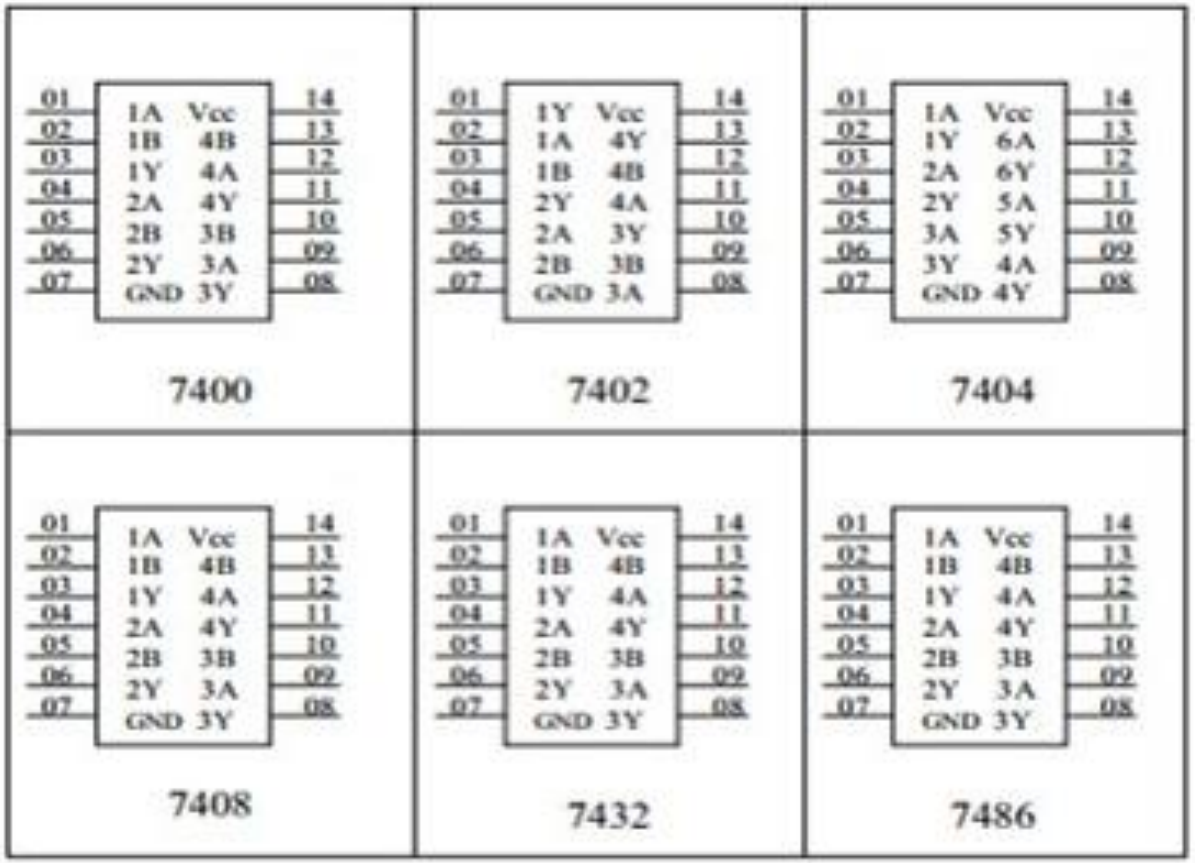
IC configurations:



Integrated Circuits (ICs):

7400 :- Quad 2 I/p NAND.
7402 :- Quad 2 I/p NOR.
7404 :- Hex Inverter.
7408 :- Quad 2 I/p AND.
7432 :- Quad 2 I/p OR.
7486 :- Quad 2 I/p X-OR.

RTL Logic

- The basic circuit of the RTL digital logic family is the NOR gate.
- The voltage levels for the circuit are 0.2 V for the low level and from 1 to 3.6 V for the high level.

Disadvantages of RTL Logic

- It's relatively slow.
- Low noise immunity and noise margin.
- Low Fan-out (Approx. 3~5)
- Expensive due to fabricated resistor.
- It can not be operated above 4MHz.

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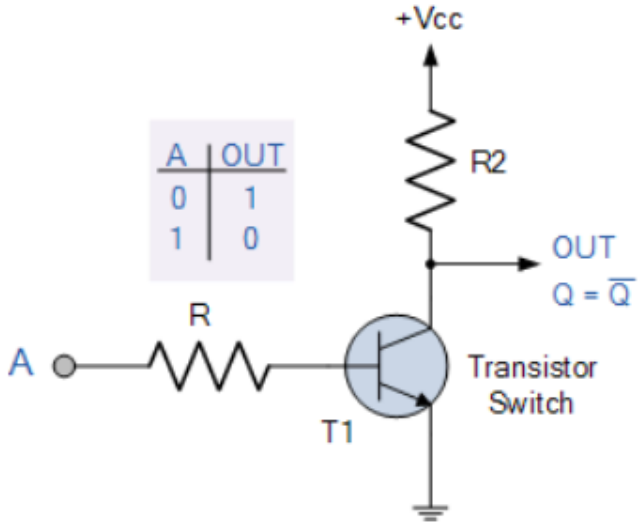
NOT Gate Using RTL Logic

A simple 2-input logic NOT gate can be constructed using a RTL Resistor-transistor switches as shown below with the input connected directly to the transistor base. The transistor must be saturated "ON" for an inverted output "OFF" at Q.



- Operation

Input	Transistor Status	Output
A= Low	T1=OFF , Cutoff Region	Q=+Vcc, High
A= High	T1=ON , Saturation Region	Q= $V_{CE(SAT)}$ =0.2 V, Low

NOR Gate Using RTL Logic

- If any input of the RTL gate is high, the corresponding transistor is driven into saturation. This causes the output to be low, regardless of the states of the other transistors.
- If all inputs are low at 0.2 V, all transistors are cut off because $_{VBE}$ < 0.6 V. This causes the output of the circuit to be high, approaching the value of supply voltage V_{CC}.

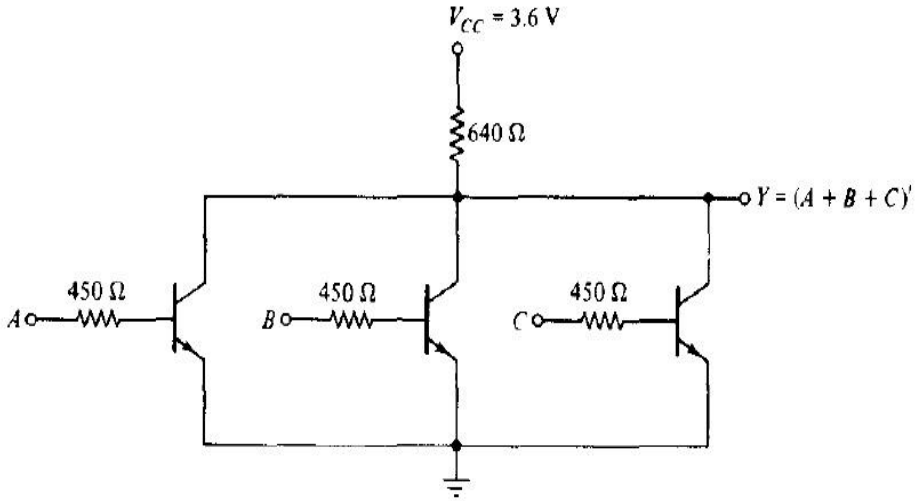


FIGURE
RTL basic NOR gate

- Operation

Input	Transistor Status	Output
All input = low	All transistor OFF, Cutoff Region.	Output = Vcc, High
Any one input/Two input/all input = High	Corresponding transistor turned ON, Saturation Region	Output = $V_{CE(SAT)}$ = 0.2 V. Low

DTL Logic

- The basic circuit in the DTL digital logic family is the NAND gate.
- Each input is associated with one diode.
- The diodes and the 5-kΩ resistor form an AND gate.
- The transistor serves as a current amplifier while inverting the digital signal.
- The two voltage levels are 0.2 V for the low level and between 4 and 5 V for the high level.
- The power

DTL Logic - Disadvantages

- Relatively lower speed.
- Propagation is higher than RTL.

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NAND Gate Using DTL Logic

- Operation

**For Q1 to conduct, $V_P > V_{BE}(Q1) + (2\times0.7)$

$= 0.7\ V + 1.4\ V = 2.1\ V$

Input	Transistor & Diode Status	Output
Any Input = Low(0.2V)	Corresponding input diode forward biased. $V_P = (0.2+0.7)V$	As $V_P < 2.1V$.Q1 is OFF. Cutoff region. Y= Vcc=5V (High)
All input = High (5 V)	All input diode reverse biased. D1 & D2 forward biased. Q1 ON. Saturation region. $V_P = V_{BE}(Q1) + V_{D1} + V_{D2}$ $= 0.7+0.7+0.7 = 2.1\ V$	Q1 is ON. Saturation region. $Y = V_{CE} = 0.2\ V$ (Low)

- Circuit

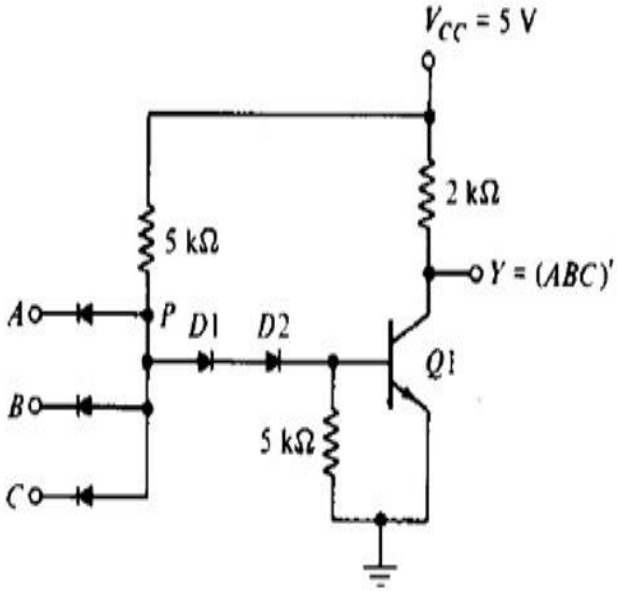

FIGURE
DTL basic NAND gate

NAND Gate Using modified DTL Logic

- The fan-out of the DTL gate is limited by the maximum current that can flow in the collector of the saturated transistor.
- The fan-out of a DTL gate may be increased by replacing one of the diodes in the base circuit with a transistor.

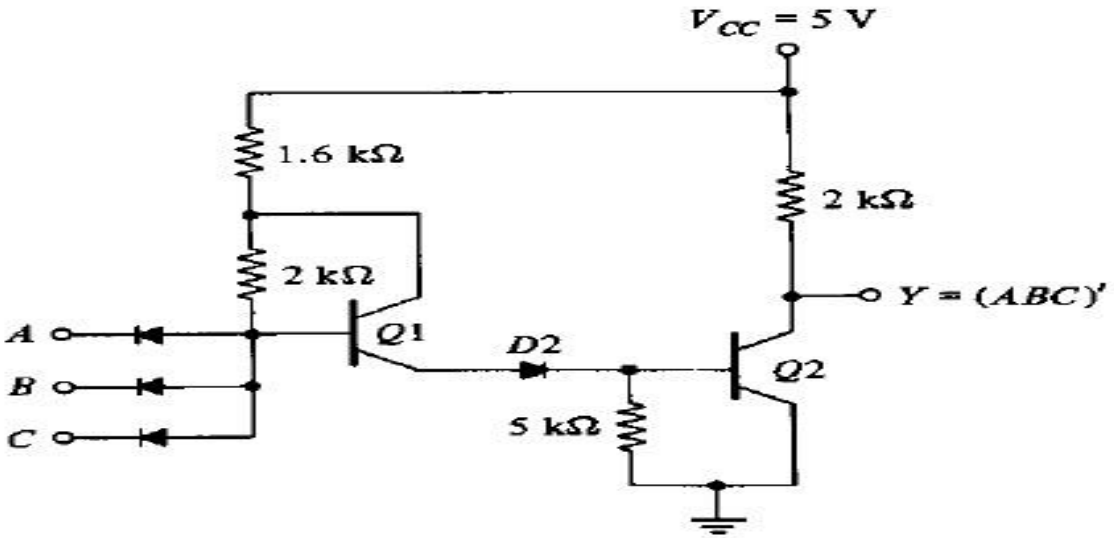

FIGURE
Modified DTL gate

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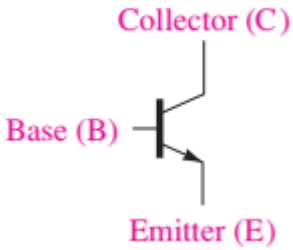
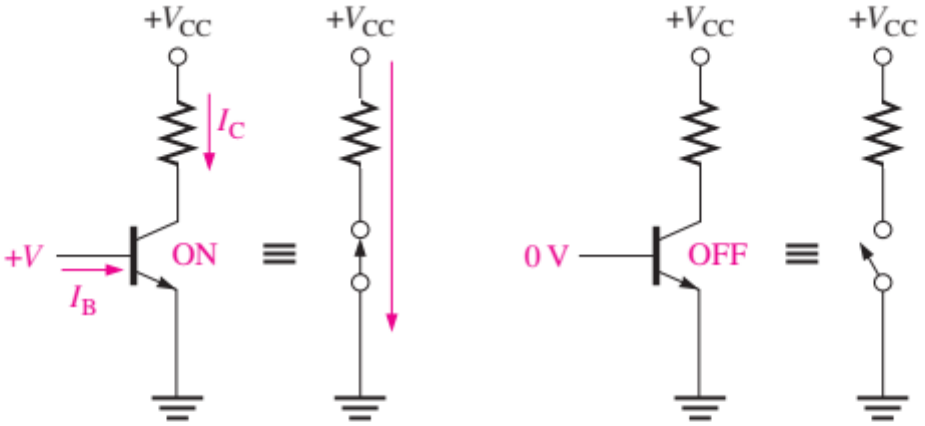
TTL Logic

The bipolar junction transistor (**BJT**) is the active switching element used in all TTL circuits. Figure 15–25 shows the symbol for an *npn* BJT with its three terminals; **base, emitter,** and **collector**. A BJT has two **junctions,** the base-emitter junction and the base-collector junction.





(a) Saturated (ON) transistor and ideal switch equivalent

(b) OFF transistor and ideal switch equivalent

FIGURE 15–26 The ideal switching action of the BJT. Conventional current direction is shown. Electron flow notation is opposite.

TTL Logic

- The Transistor-Transistor Logic (TTL) is a logic family made up of BJTs (bipolar junction transistors). TTL logic includes several transistors that have several emitters as well as several inputs.
- TTLs are available in different types and their classification is done based on the output like the following.
  - Standard TTL
  - Fast TTL
  - Schottky TTL
  - High Power TTL
  - Low Power TTL
  - Advanced Schottky TTL.
- TTL gates in all the available series come in three different types of output configuration:

1. Open -collector output
2. Totem-pole output
3. Three-state (or tristate) output

Open Collector Output (NAND)

- The multiple emitters in transistor *Q1* are connected to the inputs. These emitters behave most of the time like the input diodes in the DTL gate since they form a *pn* junction with their common base.
- The base-collector junction of *Q1* acts as another *pn* junction diode corresponding to *D1* in the DTL gate.
- Transistor *Q2* replaces the second diode, *D*2, in the DTL gate. The output of the TTL gate is taken from the open collector of *Q3.*
- A resistor connected to *Vcc* must be inserted external to the IC package for the output to "pull up" to the high voltage level when *Q*3 is off; otherwise, the output acts as an open circuit.
- For Q3 to start conducting, the path from Q1 to Q3 must overcome.

= One diode drop in B-C junction of Q1 + two V_{BE} drop in Q2 & Q3 = 3 × 0.7 = 2.1 V

Operation:

Input	Transistor & Diode Status	Output
Any Input = Low(0.2V)	Corresponding BE junction of Q1 is forward biased. Voltage at base of Q1 = 0.2V (I/P) + 0.7 V (V_{BE})= 0.9V	V_{BE} (Q1)=0.9 V. So,Q2& Q3 Cutoff. Y = Vcc = 5 V (High)
All input = High (5 V)	All BE junction of Q1 is reversed biased. Q2 & Q3 saturation region.	V_{BE} (Q1)=2.1 V. So,Q2& Q3 Saturates. Y = V_{CE}(Q3) = 0.2V (Low)

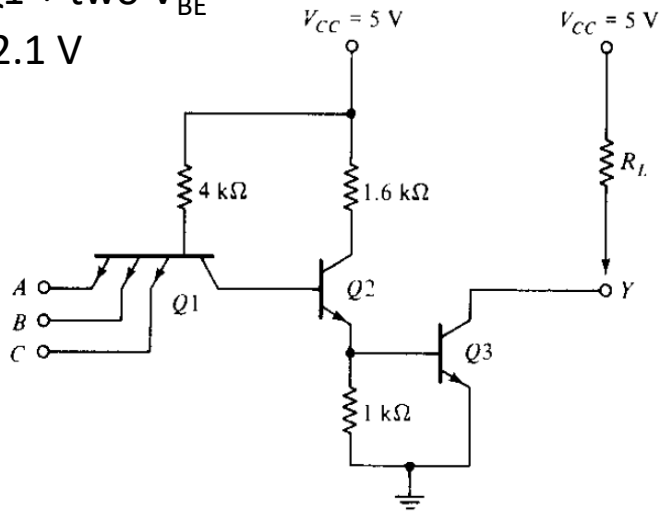
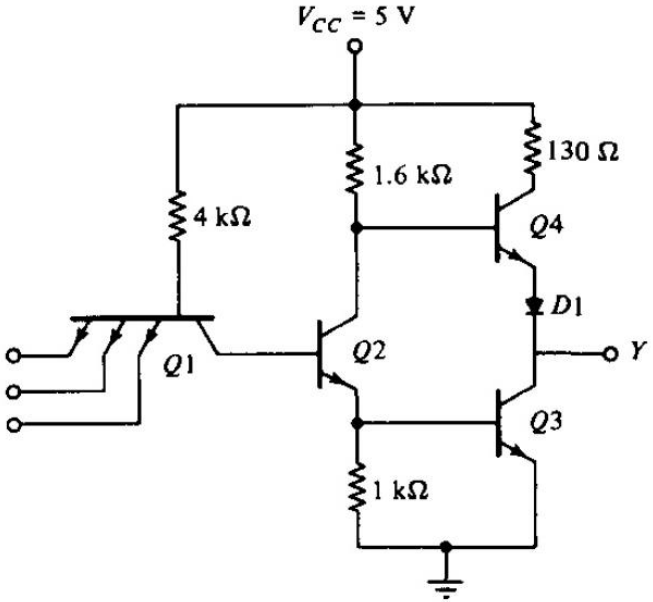


FIGURE
Open-collector TTL gate

Totem pole Output (NAND)

Totem Pole means the addition of an active pull up the circuit in the output of the Gate which results in a reduction of propagation delay. Logic operation is the same as the open collector output. The use of transistors Q4 and diode is to provide quick charging and discharging of parasitic capacitance across Q3. The resistor is used to keep the output current to a safe value.



Operation:

Input	Transistor & Diode Status	Output
Any Input = Low(0.2V)	Corresponding BE junction of Q1 is forward biased. Voltage at base of Q1 = 0.2V (I/P) + 0.7 V (V_{BE})= 0.9V Voltage at base of Q2 = 5V	• Q2& Q3 Cutoff. • Q4 Conducts. D1 Forward biased. • Y = (High)
All input = High (5 V)	All BE junction of Q1 is reversed biased. Q2 & Q3 saturation region. Q4 Cutoff region.	V_{BE} (Q1)=2.1 V. So,Q2& Q3 Saturates. V_B (Q4) = 0.9V . So, Q4 cutoff. Y = V_{CE}(Q3) = 0.2V (Low)

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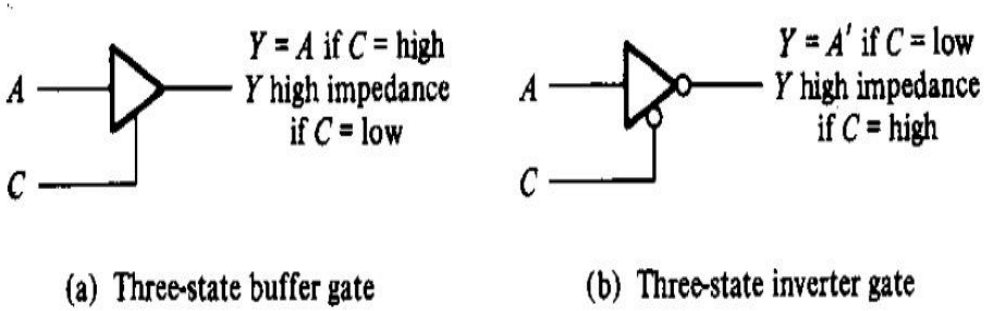
Three-state Gate

- The outputs of two TTL gates with totem-pole structures cannot be connected together as in open-collector outputs.
- However, a special type of totem-pole gate that allows the wired connection of outputs for the purpose of forming a common-bus system. When a totem-pole output TTL gate has this property, it is called a *three-state* (or tristate) gate.



(a) Three-state buffer gate (b) Three-state inverter gate

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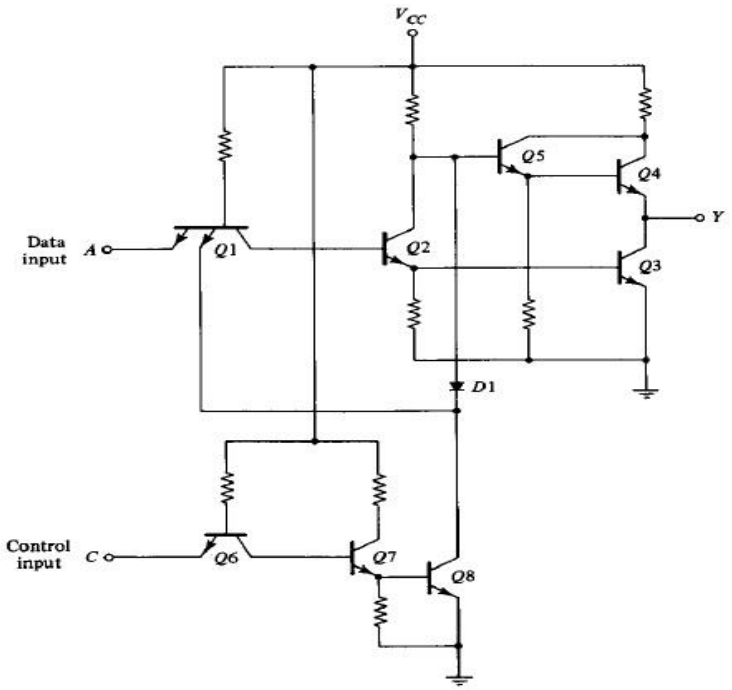
Three-state Gate

- A three-state gate exhibits three output states:

(1) A low-level state when the lower transistor in the totem-pole is on and the upper transistor is off,

(2) A high-level state when the upper transistor in the totem-pole is on and the lower transistor is off, and

(3) A third state when both transistors in the totem-pole are off. The third state provides an open circuit or high-impedance state that allows a direct wire connection of many outputs to a common line. Three-state gates eliminate the need for open-collector gates in bus configurations.



Circuit diagram for the three-state inverter

FIGURE
Three-state TTL gate

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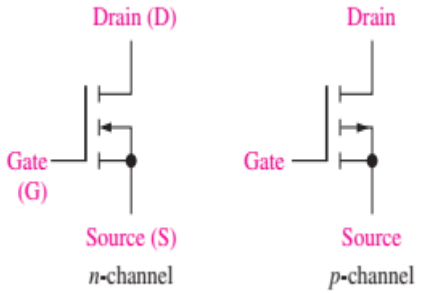
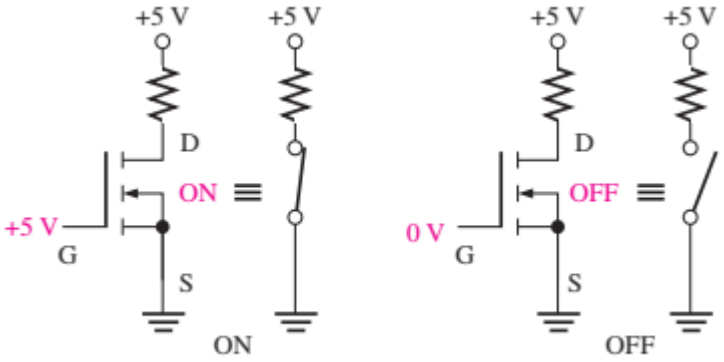
CMOS Logic

Metal-oxide semiconductor field-effect transistors (**MOSFETs**) are the active switching elements in CMOS circuits. These devices differ greatly in construction and internal operation from bipolar junction transistors used in bipolar (TTL) circuits, but the switching action is basically the same: they function ideally as open or closed switches, depending on the input.

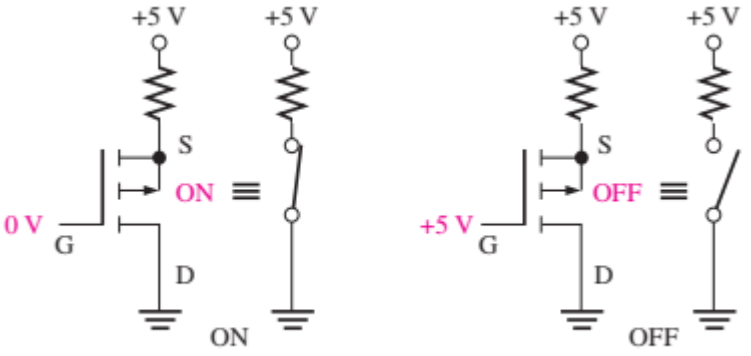
Figure 15–15(a) shows the symbols for both *n*-channel and *p*-channel MOSFETs. As indicated, the three terminals of a MOSFET are **gate, drain,** and **source**. When the gate voltage of an *n*-channel MOSFET is more positive than the source, the MOSFET is on (*saturation*), and there is, ideally, a closed switch between the drain and the source. When the gate-to-source voltage is zero, the MOSFET is off (*cutoff*), and there is, ideally, an open switch between the drain and the source. This operation is illustrated in Figure 15–15(b). The *p*-channel MOSFET operates with opposite voltage polarities, as shown in part (c).



(a) MOSFET symbols



(b) *n*-channel switch



(c) *p*-channel switch

CMOS inverter

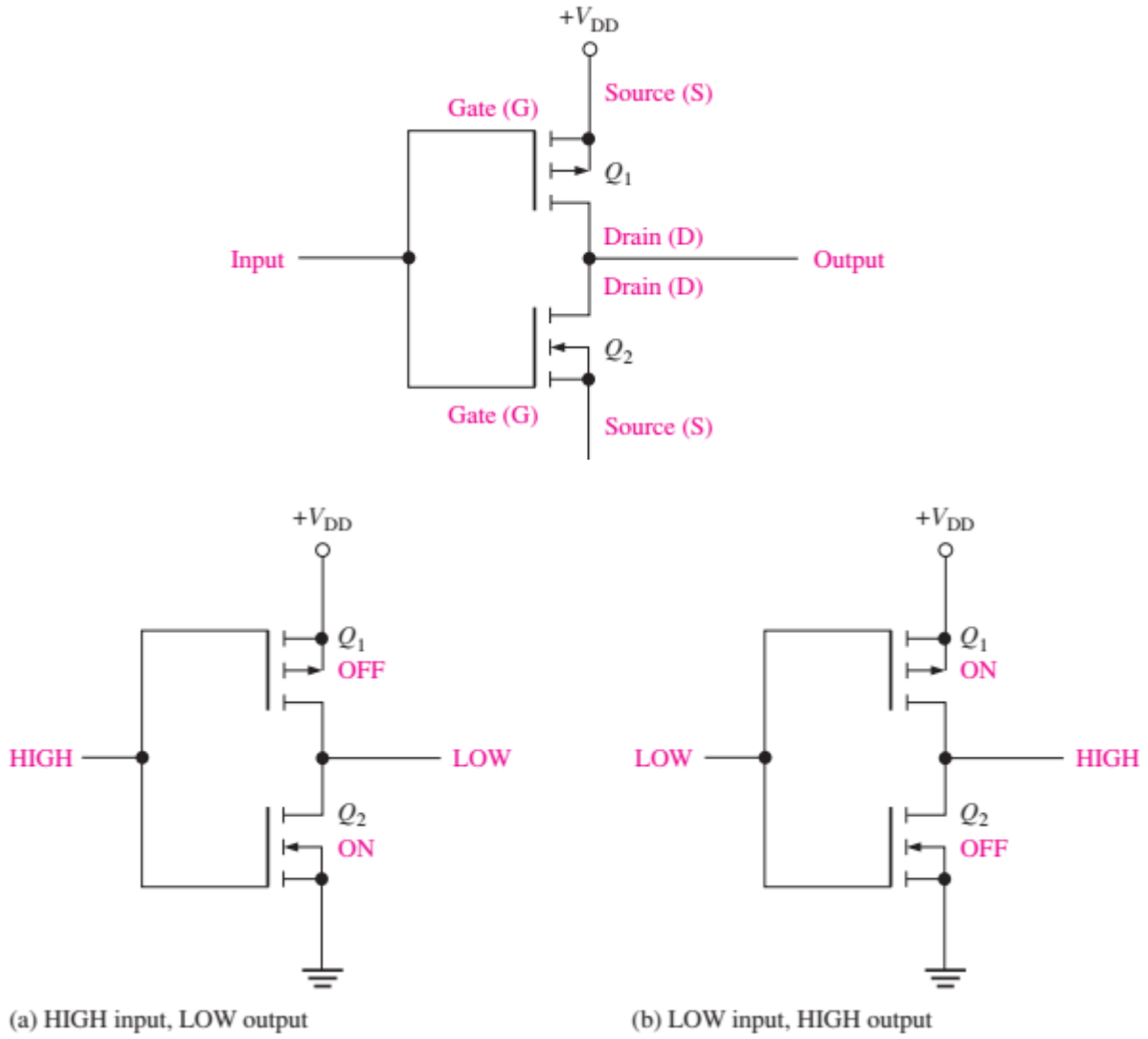


Fig. Operation of a CMOS inverter

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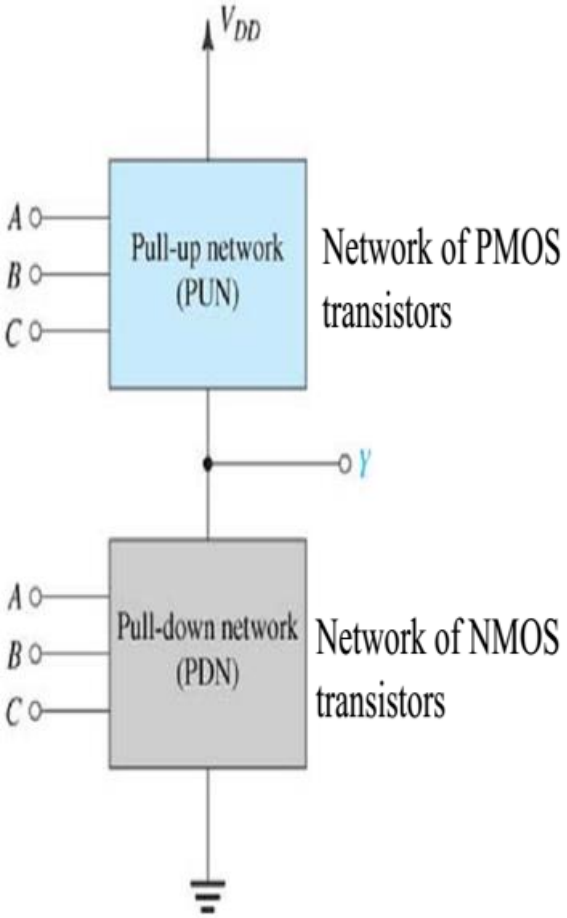
Pull-Up and Pull-Down network



–The pull-up network is made up of only P-MOS.

–P-MOS is responsible for driving the output to logic 1/high/ VDD.

–P-MOS is activated using a logic 0/LOW at its gate terminal.

–The pull-down network is made up of only N-MOS.

–N-MOS is responsible for driving the output to logic 0/LOW/GND.

–N-MOS is activated by logic 1/HIGH at its gate terminal.

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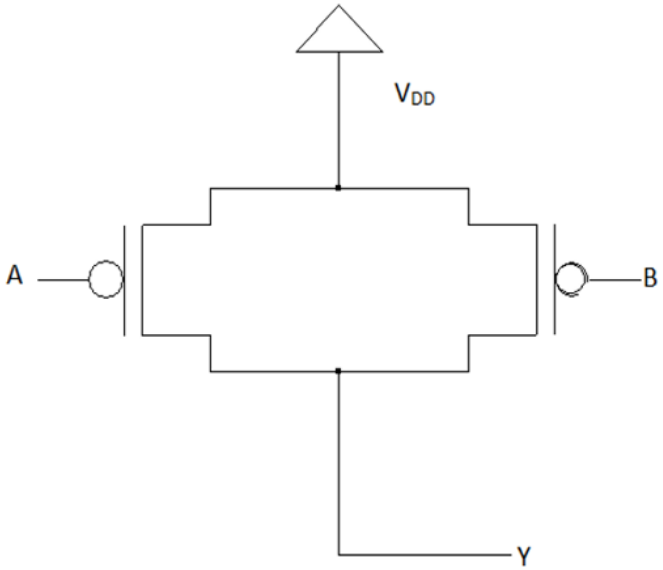
Pull-Up network

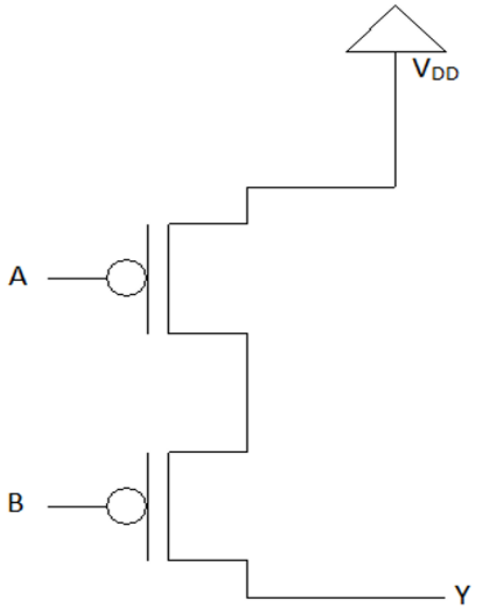
Parallel Combination of P-MOS:



For **Y to be HIGH**, either **Input A** has to be **low/0** **OR** **input B** has to be **low/0**

$$Y = \overline{A} + \overline{B}$$

Series combination of P-MOS



For **Y to be HIGH**, both **Input A** **AND** **Input B** has to be **low/0**.

$$Y = \overline{A}.\overline{B}$$

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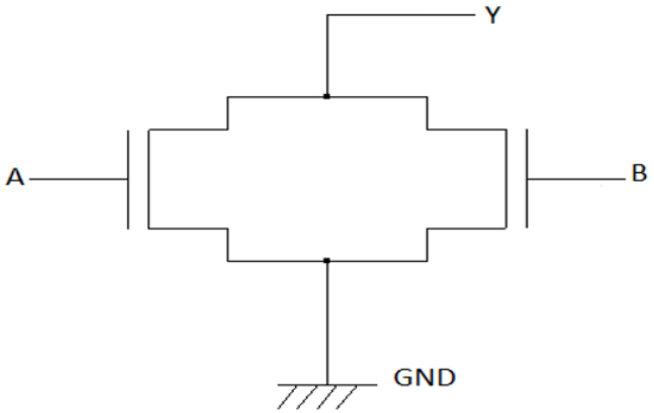
Pull-Down network

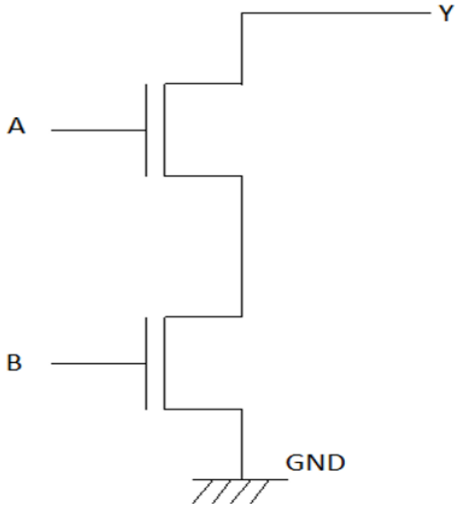
Parallel Combination of N-MOS



For Y to be Low,
either input A **OR** input B has to be high.

$$\overline{Y} = A + B$$

Series combination of N-MOS



For Y to be Low, either input A **AND** input B has to be high.

$$\overline{Y} = A.B$$

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Designing a Complex/Compound gate

For Designing complex gates, the following steps have to be followed, in order to come up with a proper design.

1. Both pull-up and pull-down network designs are required.
2. Design requirements are fulfilled using bottom-up approach.
3. For complementary MOS designs, the pull-down network is designed first.
4. The pull-up network is designed afterwards using De Morgan's Law to break down the equation.

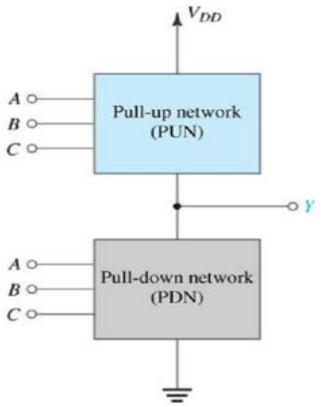
Designing a NAND gate

Expression of NAND:

$$Y = \overline{A.B}$$

Truth Table of NAND:

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

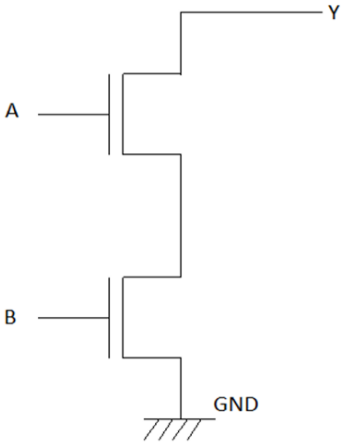


Pull-down network Design:

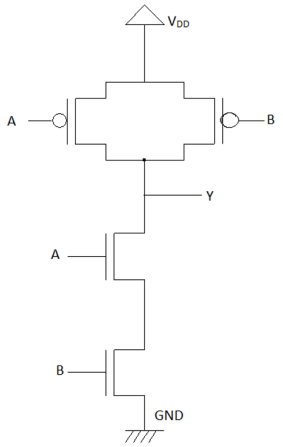
For Designing the Pull-down network, the equation has to be modified so that the output becomes low.

$$\rightarrow \overline{Y} = A.B$$

According to the logic available, it matches with the series combination of N-MOS.



Overall NAND Gate:



Pull-up network Design:

For designing the Pull-up network, the equation has to be modified so that the output becomes high with individual input combination.

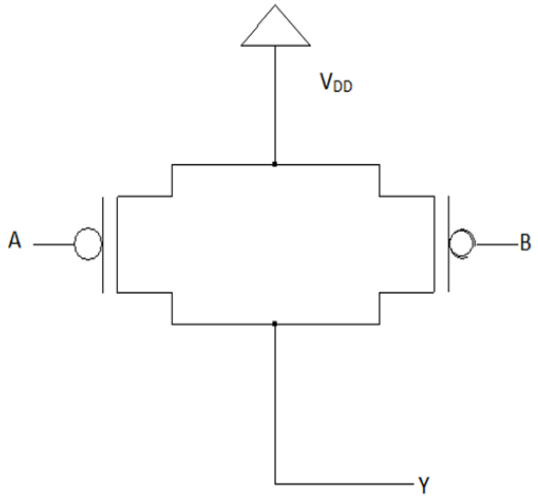
DeMorgan's Laws:

1. $\overline{A+B} = \overline{A}.\overline{B}$
2. $\overline{A.B} = \overline{A}+\overline{B}$

$$\rightarrow Y = \overline{A.B}$$

$$\rightarrow Y = \overline{A} + \overline{B}$$ (break down using De Morgan's Law)

The available logic matches with the parallel combination of P-MOS



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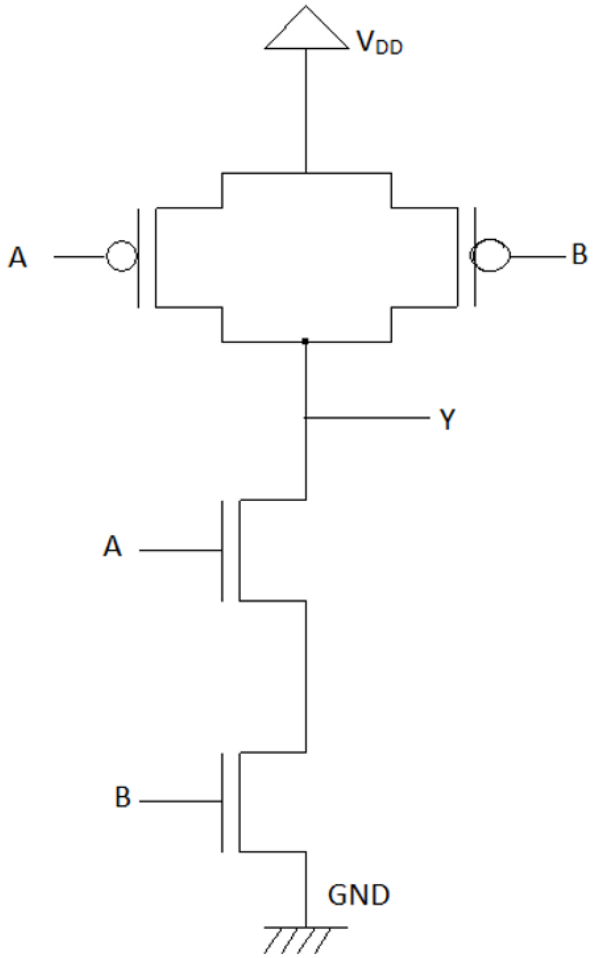
Overall NAND Gate:



Points to Note

- The pull-up inputs do not have any BAR over them.
- The pull-up inputs appear the same way as determined by the pull-down network. In this case just A and B. Not $\overline{A}$ and $\overline{B}$.

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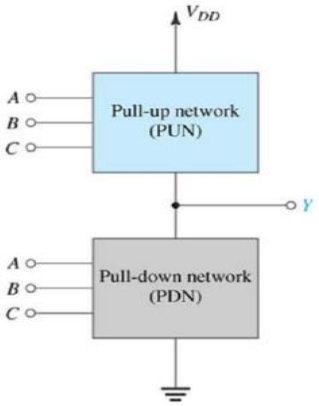
Designing a NOR gate:

SOP Expression:

$$Y = \overline{A + B}$$

Truth Table:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

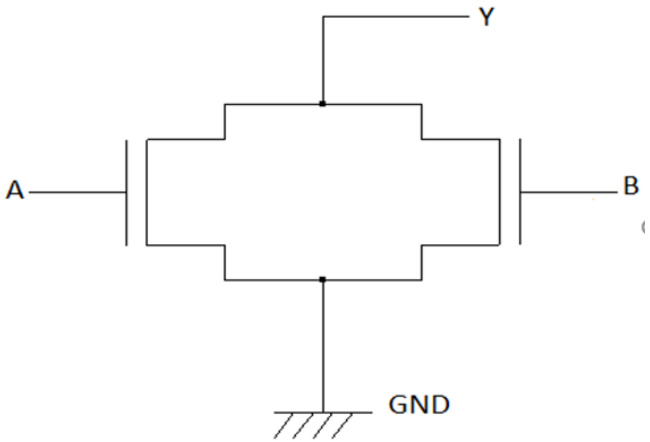


Pull-down network Design:

For Designing the Pull-down network, the equation has to be modified so that the output becomes low.

$$\overline{Y} = A + B$$

According to the logic available, it matches with the parallel combination of N-MOS.



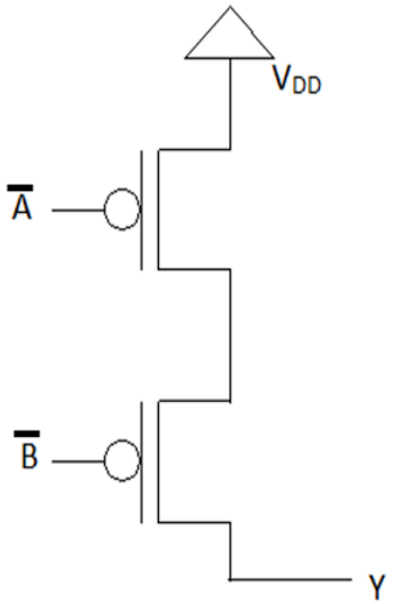
Pull-up network Design:

For designing the Pull-up network, the equation has to be modified so that the output becomes high with individual input combination.

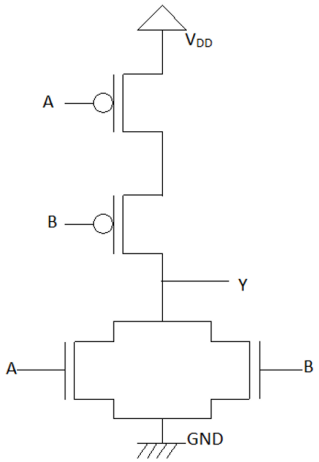
$\rightarrow Y = \overline{A + B}$

$\rightarrow Y = \overline{A}.\overline{B}$ (Break down using De Morgan's Law)

The available logic matches with the Series combination of P-MOS



Overall NOR Gate:



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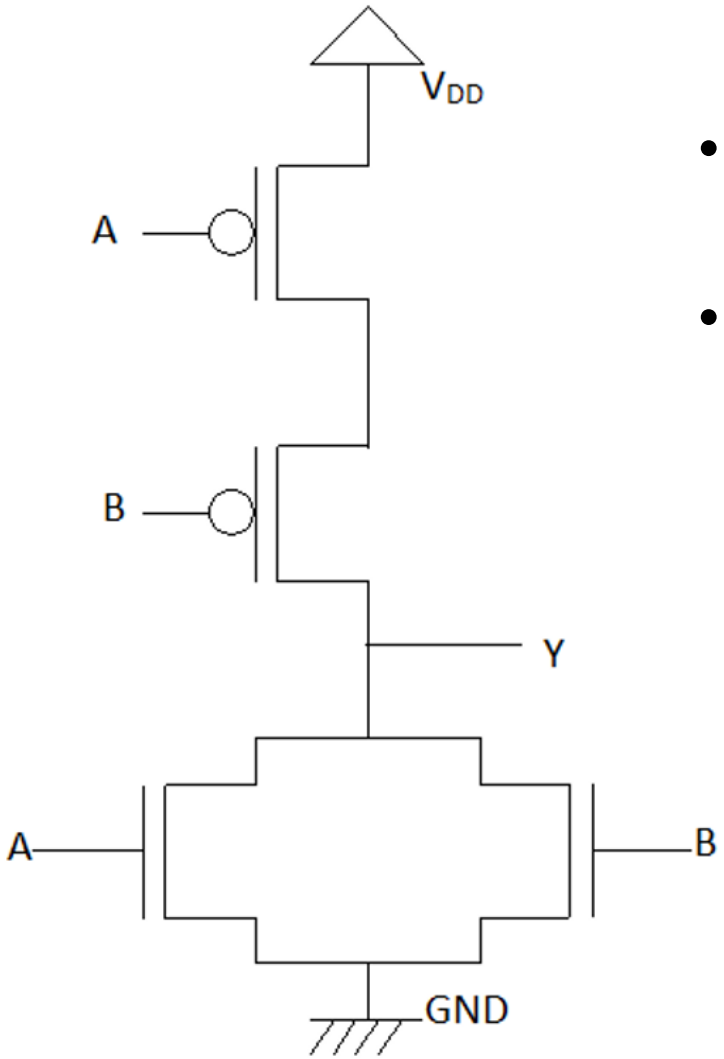
Overall NOR Gate:



Points to Note

- The pull-up inputs do not have any BAR over them.
- The pull-up inputs appear the same way as determined by the pull-down network. In this case just A and B. Not $\overline{A}$ and $\overline{B}$.

Reference:

[1] Thomas L. Floyd, "Digital Fundamentals" 11th edition, Prentice Hall.
[2] M. Morris Mano, "Digital Logic & Computer Design" Prentice Hall.

Thanks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