

# Electronic Devices

## Final Term Lecture - 01

Reference book:

**Electronic Devices and Circuit Theory (Chapter-5)**

Robert L. Boylestad and L. Nashelsky , (11<sup>th</sup> Edition)



**Faculty of Engineering**  
American International University-Bangladesh

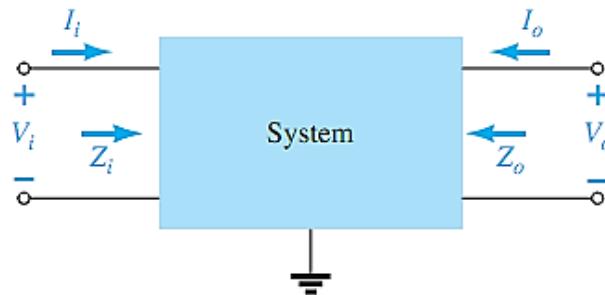
# OBJECTIVES

- Become familiar with there,  $r_e$ , hybrid and hybrid pi models for the BJT transistor.
- Learn to use the equivalent model to find the important ac parameters for an amplifier.
- Understand the effects of a source resistance and load resistor on the overall gain and characteristics of an amplifier.
- Become aware of the general ac characteristics of a variety of important BJT configurations.
- Begin to understand the advantages associated with the two-port systems approach to single- and multistage amplifiers.
- Develop some skill in troubleshooting ac amplifier networks.



# BJT TRANSISTOR MODELING

- A model is an equivalent circuit that represents the AC characteristics of the transistor.
- A model uses circuit elements that approximate the behavior of the transistor.
- There are two models commonly used in small signal AC analysis of a transistor:
  - $r_e$  model
  - Hybrid equivalent model

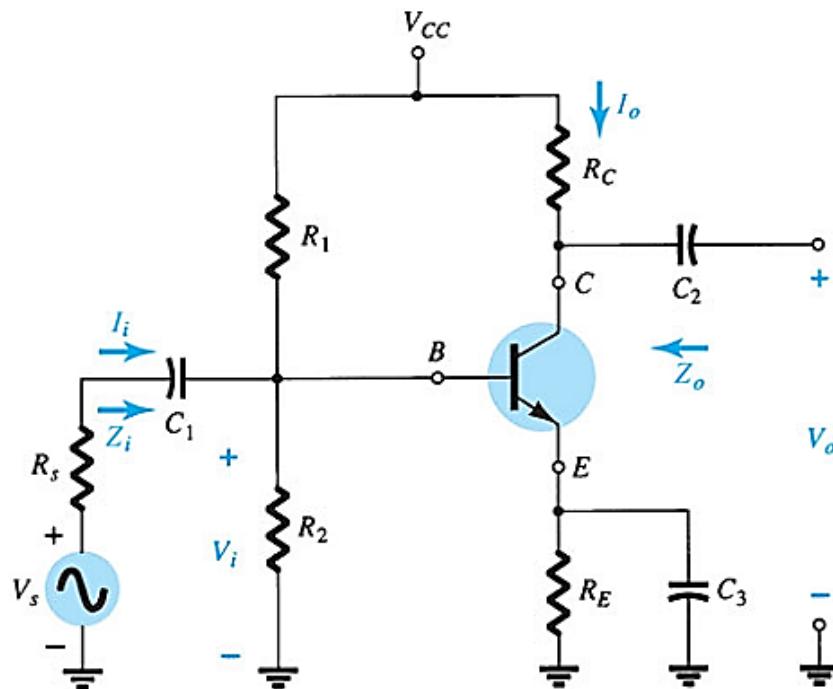


**FIG. 5.5**

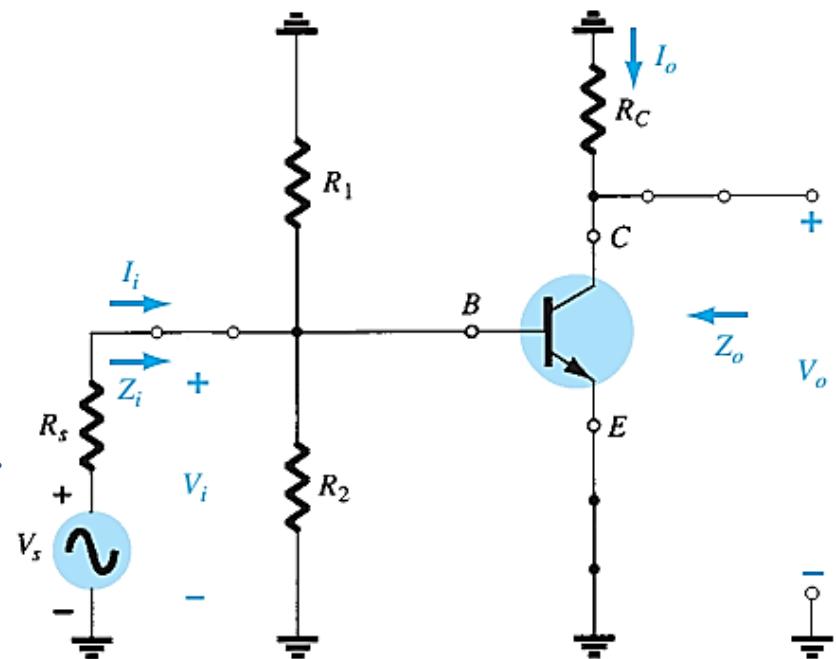
*Defining the important parameters  
of any system.*



# BJT TRANSISTOR MODELING

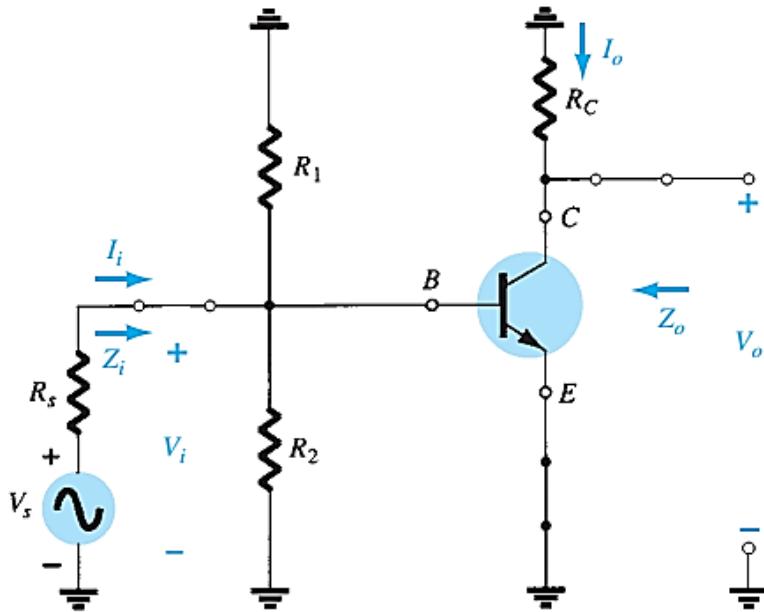


**Capacitors** chosen with **very small reactance** at the frequency of application → **replaced by low-resistance or short circuit.**

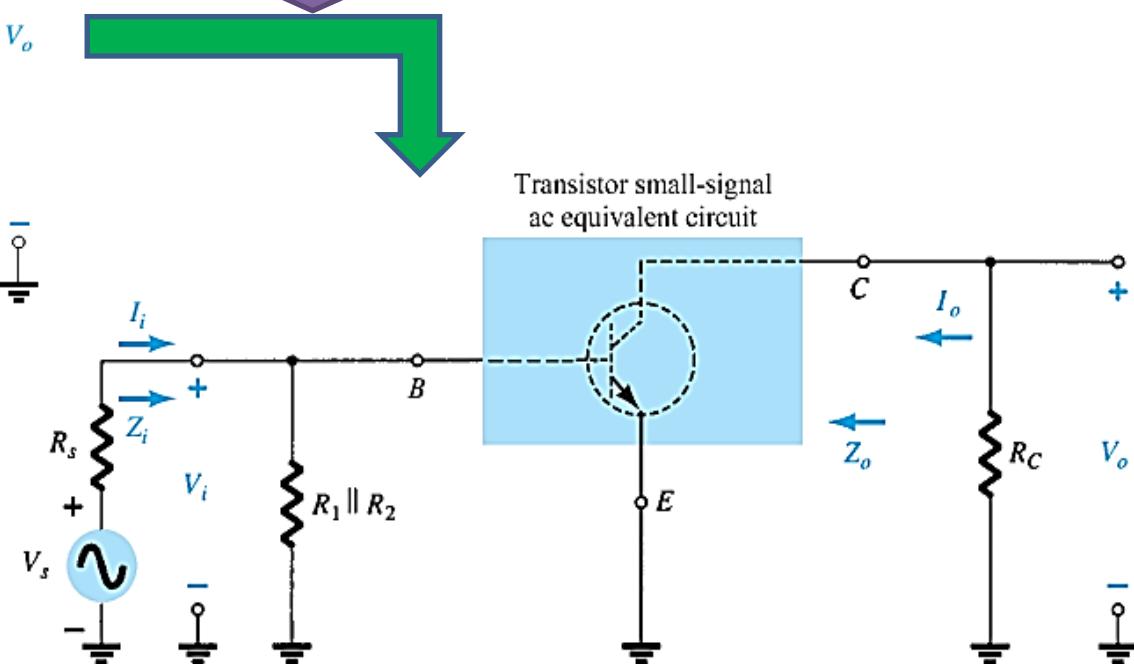


Removal of the dc supply and insertion of the short-circuit equivalent for the capacitors.

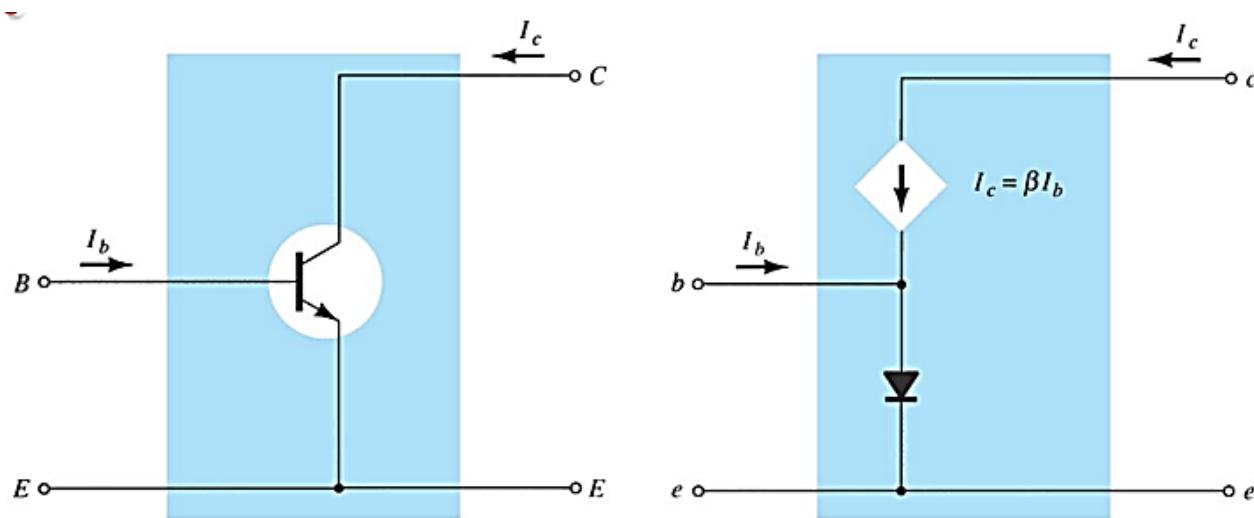
# BJT TRANSISTOR MODELING



Circuit redrawn for small signal ac analysis



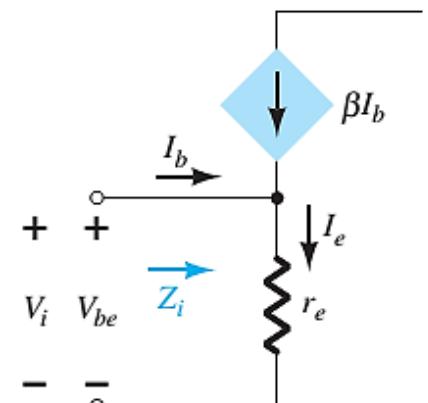
# The $r_e$ Transistor Model (Common Emitter Configuration)



$$Z_i = \frac{V_i}{I_b} = \frac{V_{be}}{I_b}$$

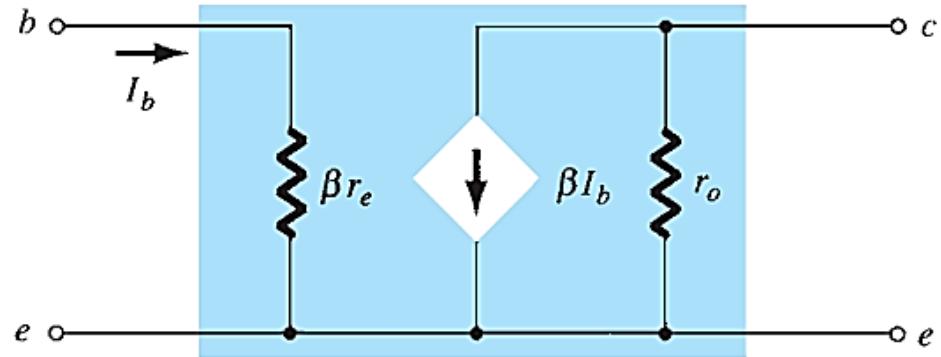
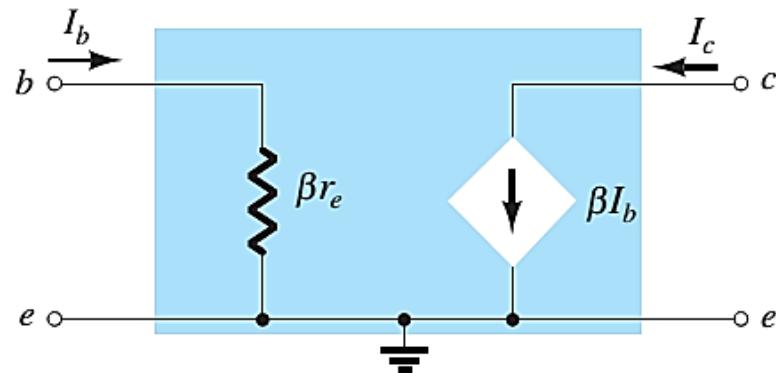
$$\begin{aligned} V_{be} &= I_e r_e = (I_c + I_b) r_e = (\beta I_b + I_b) r_e \\ &= (\beta + 1) I_b r_e \end{aligned}$$

$$Z_i = \frac{V_{be}}{I_b} = \frac{(\beta + 1) I_b r_e}{I_b} = (\beta + 1) r_e \approx \beta r_e$$



# The $r_e$ Transistor Model (Common Emitter Configuration)

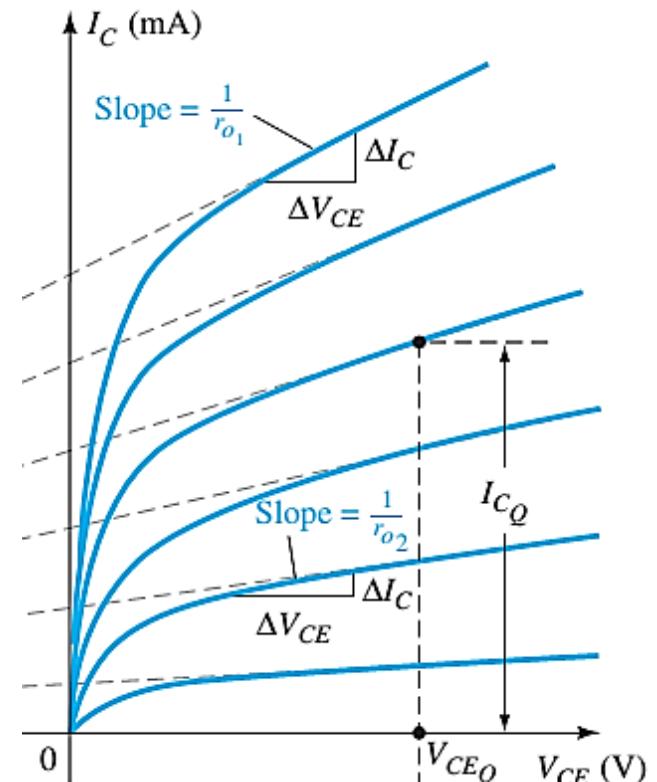
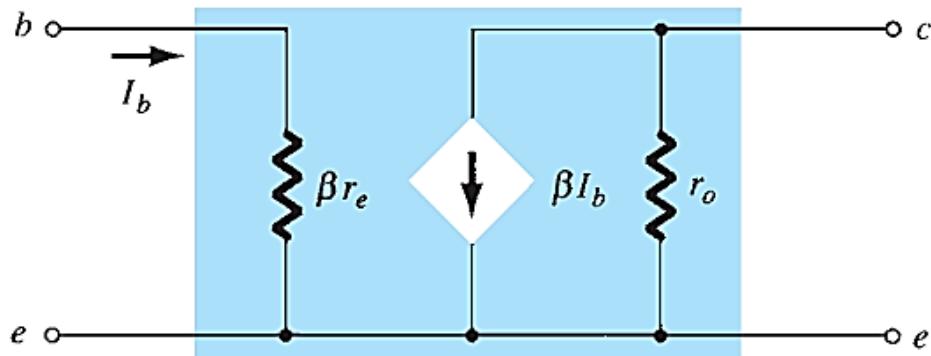
$$r_e = \frac{26 \text{ mV}}{I_E}$$



# The $r_e$ Transistor Model (Common Emitter Configuration)

$$\text{slope} = \frac{\Delta I_C}{\Delta V_{CE}} = \frac{1}{r_0}$$

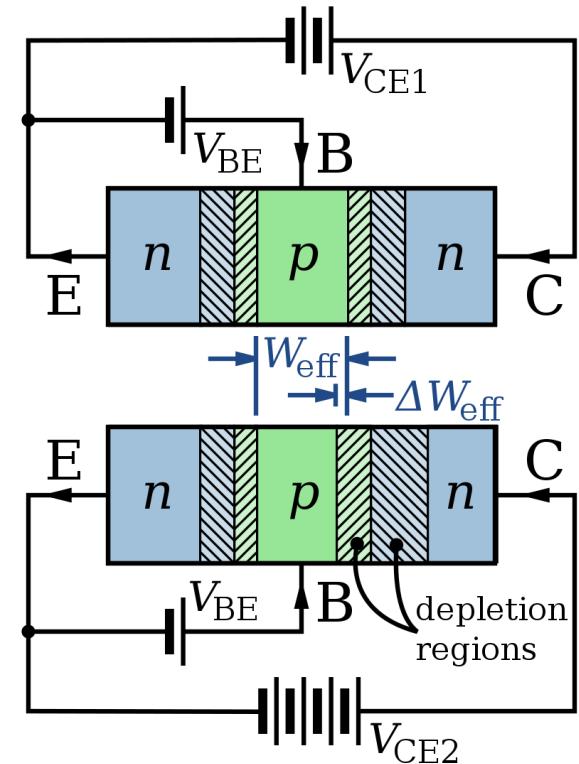
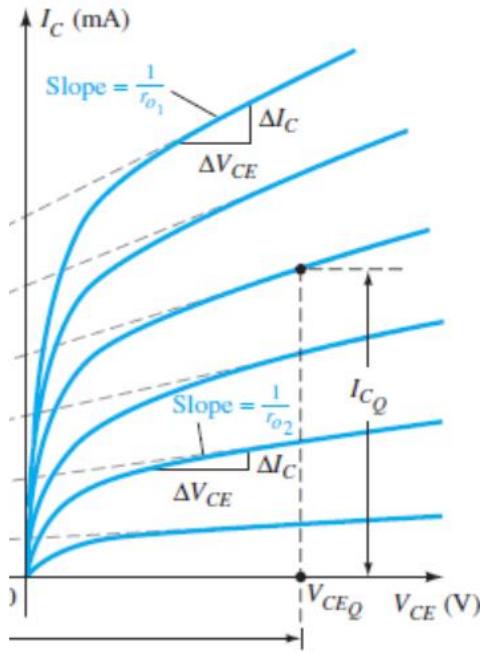
$$r_0 = \frac{\Delta V_{CE}}{\Delta I_C}$$



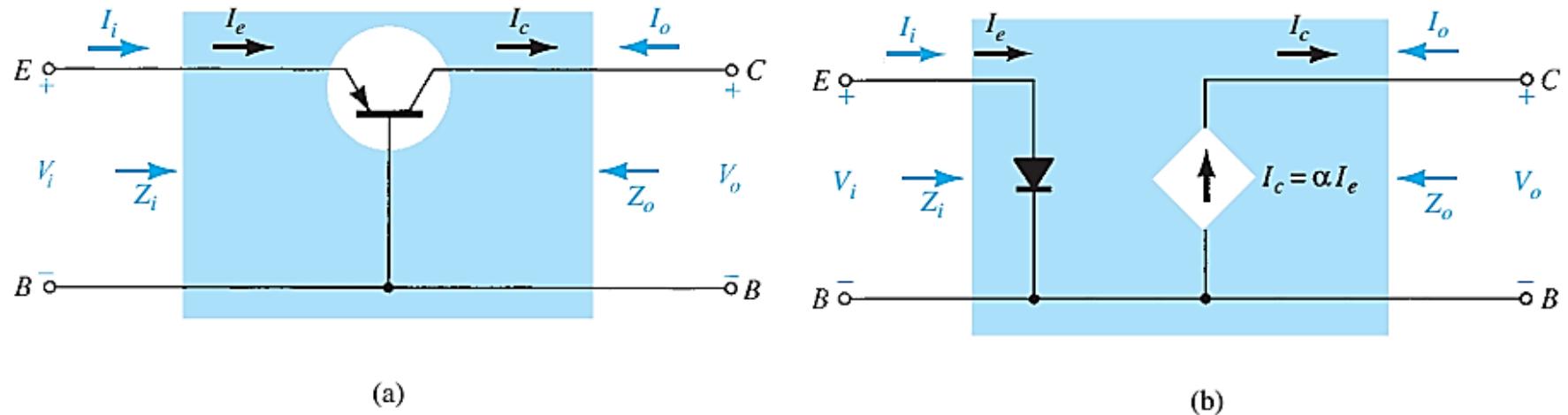
# The $r_e$ Transistor Model (Common Emitter Configuration)

The Early effect, named after its discoverer **James M. Early**, is the variation in the effective width of the base in a bipolar junction transistor (BJT) due to a variation in the applied base-to-collector voltage.

A greater reverse bias across the collector–base junction, for example, increases the collector–base depletion width, thereby decreasing the width of the charge carrier portion of the base.

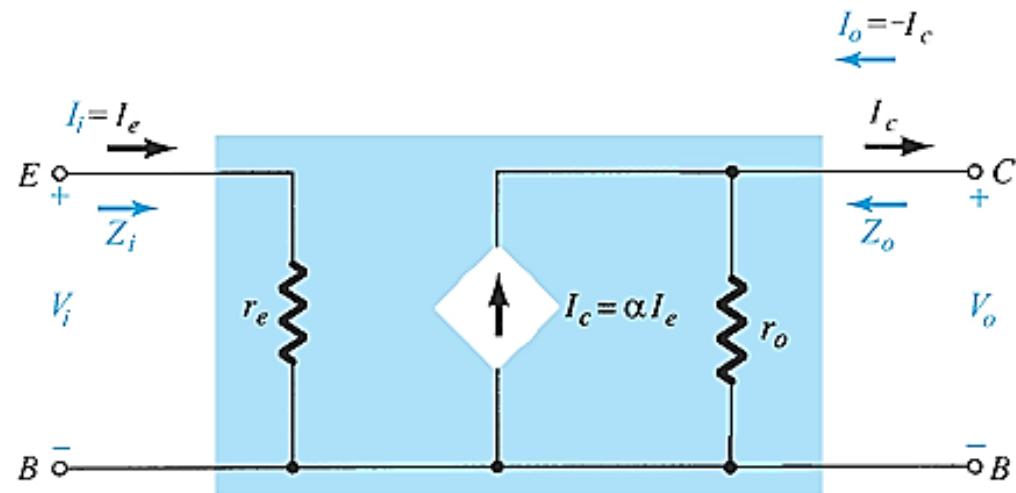
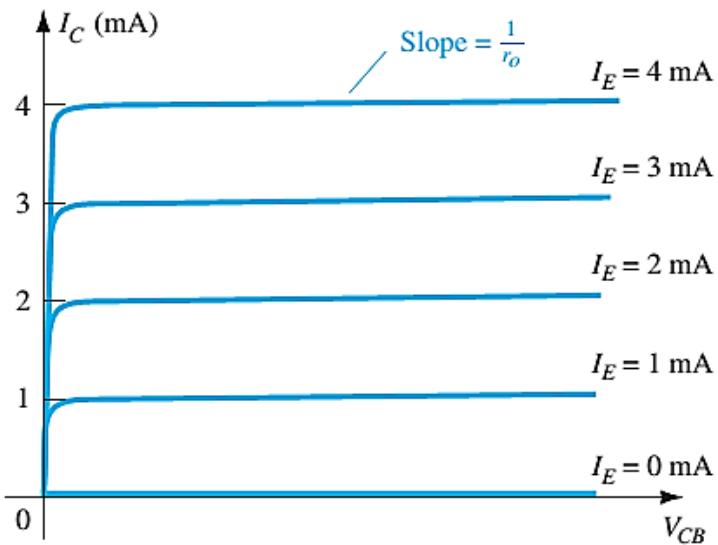


# COMMON-BASE CONFIGURATION



**FIG. 5.17**  
(a) Common-base BJT transistor; (b) equivalent circuit for configuration of (a).

# COMMON-BASE CONFIGURATION

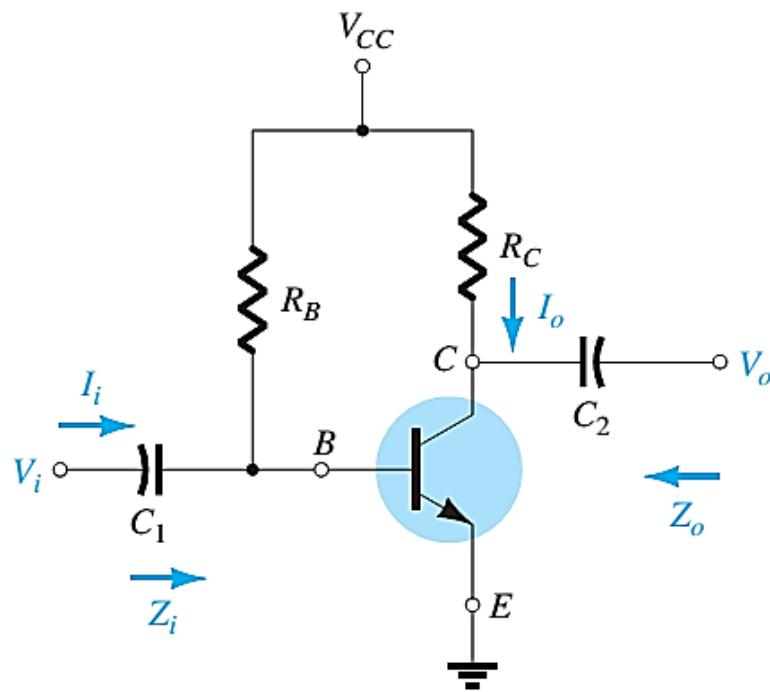


**FIG. 5.19**  
Defining  $Z_o$ .

The output resistance  $r_o$  is quite high, typically extending into the  $M\Omega$  range.

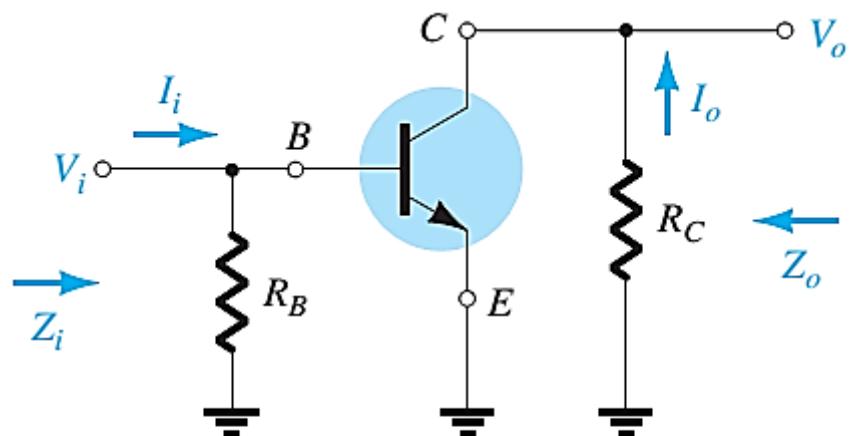
Common Base  $r_e$   
equivalent circuit

# COMMON Emitter FIXED BIAS CONFIGURATION



**FIG. 5.20**

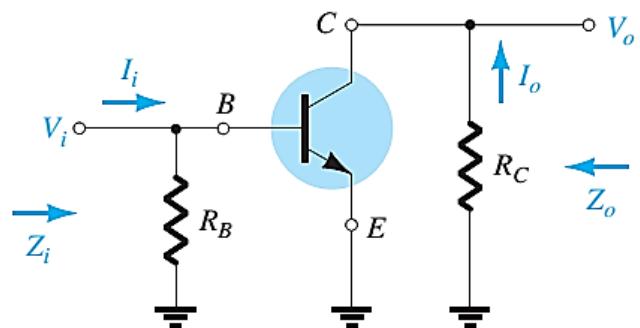
Common-emitter fixed-bias configuration.



**FIG. 5.21**

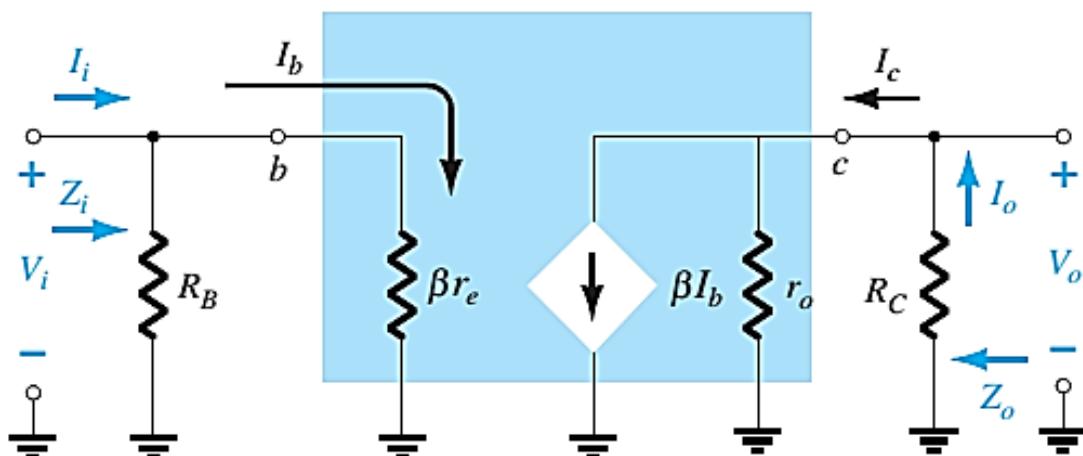
Network of Fig. 5.20 following the removal of the effects of  $V_{CC}$ ,  $C_1$ , and  $C_2$ .

# COMMON Emitter FIXED BIAS CONFIGURATION



**FIG. 5.21**

Network of Fig. 5.20 following the removal of the effects of  $V_{CC}$ ,  $C_1$ , and  $C_2$ .



**FIG. 5.22**

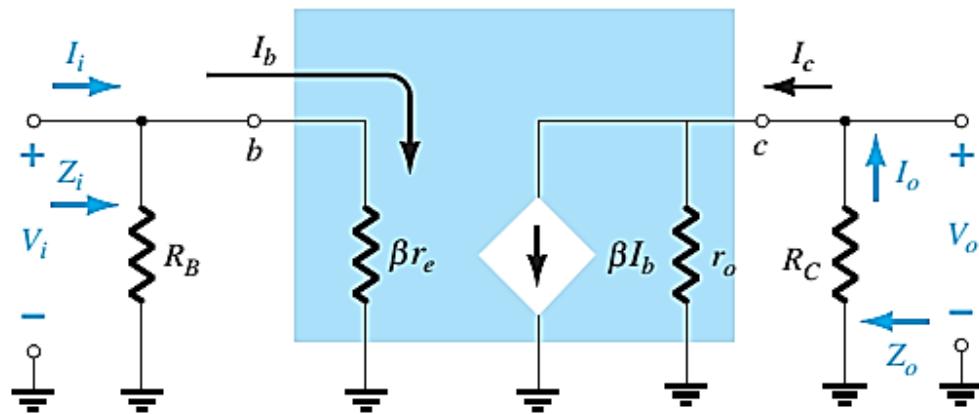
Substituting the  $r_e$  model into the network of Fig. 5.21.

# COMMON Emitter FIXED BIAS CONFIGURATION

**INPUT IMPEDANCE,  $Z_i$**

$$Z_i = R_B \parallel \beta r_e$$

$$Z_i \cong \beta r_e \mid_{R_B} \geq 10\beta r_e$$



**OUTPUT IMPEDANCE,  $Z_o$**

$$Z_o = R_C \parallel r_o$$

$$Z_o \cong R_C \mid_{r_o} \geq 10R_C$$

**VOLTAGE GAIN,  $A_v$**

$$V_o = -\beta I_b (R_C \parallel r_o) = -\beta \left( \frac{V_i}{\beta r_e} \right) (R_C \parallel r_o); \quad I_b = \frac{V_i}{\beta r_e}$$

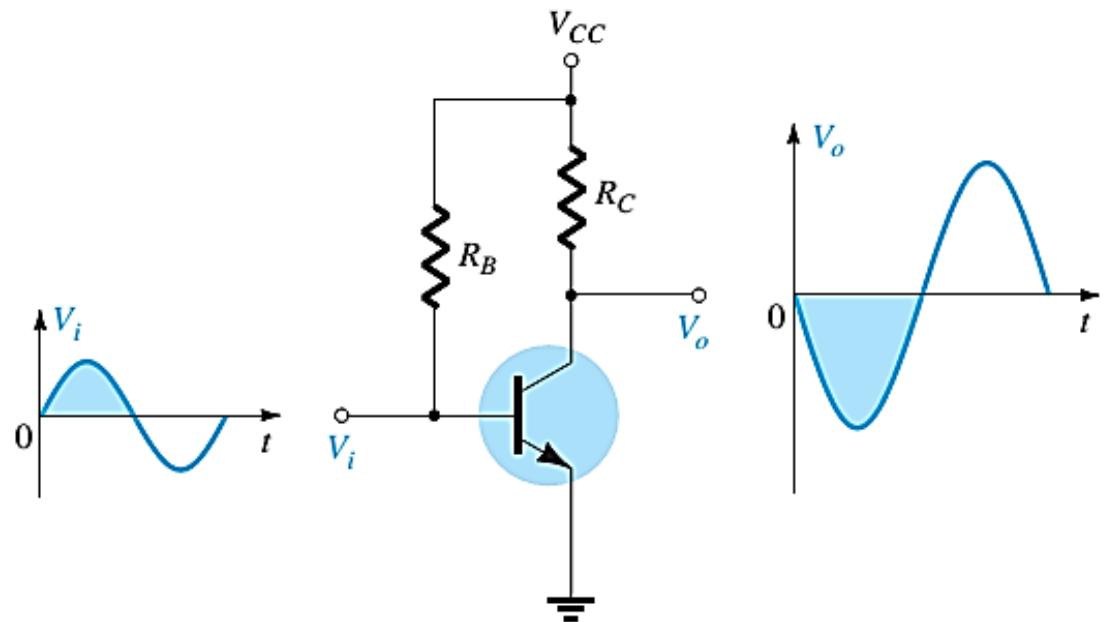
$$A_v = \frac{V_o}{V_i} = -\frac{(R_C \parallel r_o)}{r_e}, \quad A_v = -\frac{R_C}{r_e} \mid_{r_o} \geq 10R_C$$

For the majority of situations  $R_B$  is greater than  $\beta r_e$  by more than a factor of 10

# COMMON Emitter FIXED BIAS PHASE RELATIONSHIP

$$A_v = \frac{V_o}{V_i} = -\frac{(R_C \parallel r_o)}{r_e}$$

Demonstrating the  $180^\circ$  phase shift between input and output waveforms.



**FIG. 5.24**

*Demonstrating the  $180^\circ$  phase shift between input and output waveforms.*

Why is transistor output inverted?

The inversion is **because of the direction of the current source is the reverse of the vbe**, so an increase in vbe results in decrease of vce

# EXAMPLE

- **EXAMPLE 5.1:** For the network of Fig. 5.25 :
- Determine  $r_e$ ,  $Z_i$  (with  $r_o = \infty$ ),  $Z_o$  (with  $r_o = \infty$ ),  $A_v$  (with  $r_o = \infty$ ) and Repeat with  $r_o = 50 \text{ k}\Omega$ .

a. DC analysis:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 \text{ V} - 0.7 \text{ V}}{470 \text{ k}\Omega} = 24.04 \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (101)(24.04 \mu\text{A}) = 2.428 \text{ mA}$$

$$r_e = \frac{26 \text{ mV}}{I_E} = \frac{26 \text{ mV}}{2.428 \text{ mA}} = 10.71 \Omega$$

b.  $\beta r_e = (100)(10.71 \Omega) = 1.071 \text{ k}\Omega$

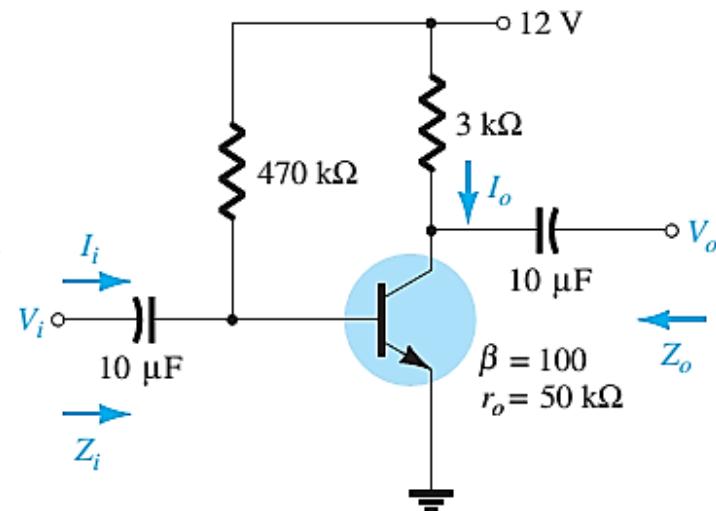
$$Z_i = R_B \parallel \beta r_e = 470 \text{ k}\Omega \parallel 1.071 \text{ k}\Omega = 1.07 \text{ k}\Omega$$

c.  $Z_o = R_C = 3 \text{ k}\Omega$

d.  $A_v = -\frac{R_C}{r_e} = -\frac{3 \text{ k}\Omega}{10.71 \Omega} = -280.11$

e.  $Z_o = r_o \parallel R_C = 50 \text{ k}\Omega \parallel 3 \text{ k}\Omega = 2.83 \text{ k}\Omega$  vs.  $3 \text{ k}\Omega$

$$A_v = -\frac{r_o \parallel R_C}{r_e} = \frac{2.83 \text{ k}\Omega}{10.71 \Omega} = -264.24 \text{ vs. } -280.11$$

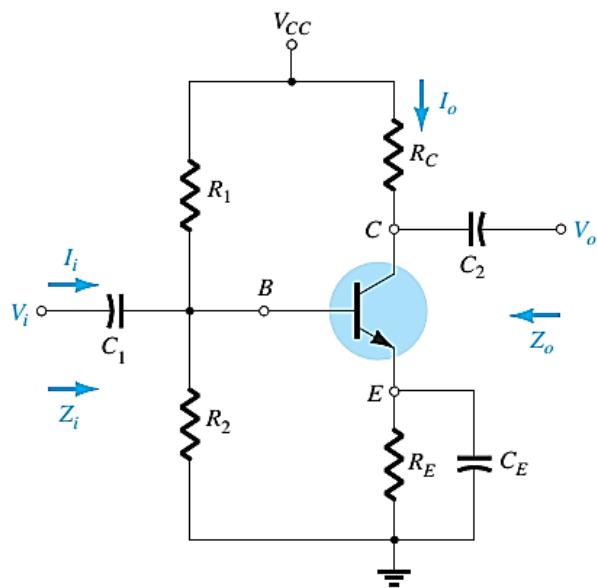


**FIG. 5.25**  
Example 5.1.

# End of Lecture-1

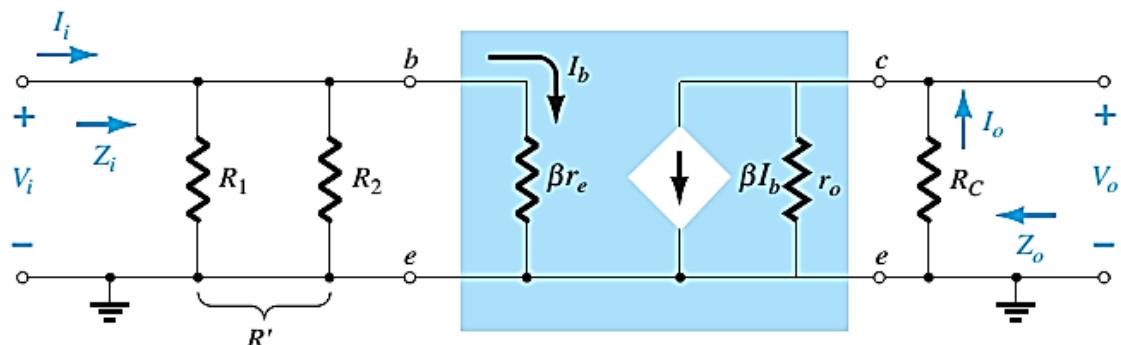


# COMMON-EMITTER VOLTAGE-DIVIDER BIAS



**FIG. 5.26**

Voltage-divider bias configuration.



**FIG. 5.27**

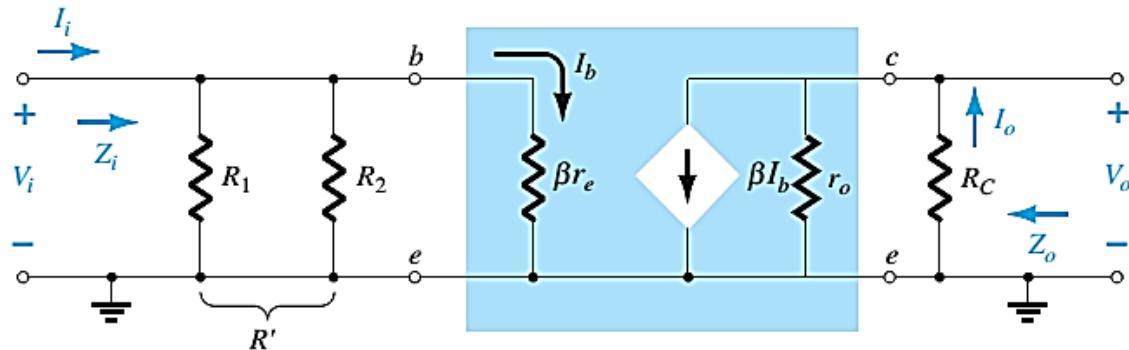
Substituting the  $r_e$  equivalent circuit into the ac equivalent network of Fig. 5.26.

# COMMON-EMITTER VOLTAGE-DIVIDER BIAS

**INPUT IMPEDANCE,  $Z_i$**

$$R' = R_1 \parallel R_2$$

$$Z_i = R' \parallel \beta r_e$$



**OUTPUT IMPEDANCE,  $Z_o$**

$$Z_o = R_C \parallel r_o$$

$$Z_o \cong R_C \mid_{r_o \geq 10R_C}$$

**VOLTAGE GAIN,  $A_v$**

$$V_o = -\beta I_b (R_C \parallel r_o) = -\beta \left( \frac{V_i}{\beta r_e} \right) (R_C \parallel r_o); \quad I_b = \frac{V_i}{\beta r_e}$$

$$A_v = \frac{V_o}{V_i} = -\frac{(R_C \parallel r_o)}{r_e}, \quad A_v = -\frac{R_C}{r_e} \mid_{r_o \geq 10R_C}$$

# EXAMPLE

- **EXAMPLE 5.2:** For the network of Fig. 5.28 :
- Determine  $r_e$ ,  $Z_i$ ,  $Z_o$  (with  $r_o = \infty$ ),  $A_v$  (with  $r_o = \infty$ ) and Repeat with  $r_o = 50 \text{ k}\Omega$ .

a. DC: Testing  $\beta R_E > 10R_2$ ,

$$(90)(1.5 \text{ k}\Omega) > 10(8.2 \text{ k}\Omega)$$
$$135 \text{ k}\Omega > 82 \text{ k}\Omega \text{ (satisfied)}$$

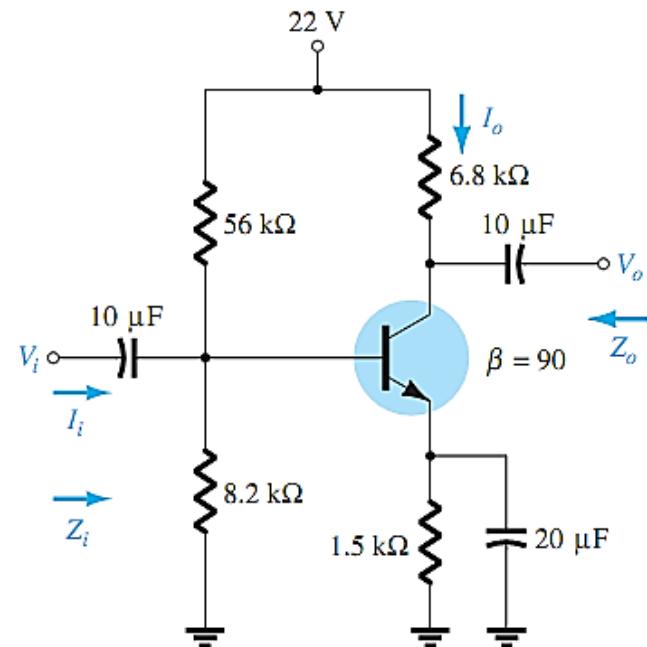
Using the approximate approach, we obtain

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{(8.2 \text{ k}\Omega)(22 \text{ V})}{56 \text{ k}\Omega + 8.2 \text{ k}\Omega} = 2.81 \text{ V}$$

$$V_E = V_B - V_{BE} = 2.81 \text{ V} - 0.7 \text{ V} = 2.11 \text{ V}$$

$$I_E = \frac{V_E}{R_E} = \frac{2.11 \text{ V}}{1.5 \text{ k}\Omega} = 1.41 \text{ mA}$$

$$r_e = \frac{26 \text{ mV}}{I_E} = \frac{26 \text{ mV}}{1.41 \text{ mA}} = 18.44 \Omega$$



**FIG. 5.28**  
Example 5.2.

## EXAMPLE Contd.

b.  $R' = R_1 \parallel R_2 = (56 \text{ k}\Omega) \parallel (8.2 \text{ k}\Omega) = 7.15 \text{ k}\Omega$

$$Z_i = R' \parallel \beta r_e = 7.15 \text{ k}\Omega \parallel (90)(18.44 \Omega) = 7.15 \text{ k}\Omega \parallel 1.66 \text{ k}\Omega$$
$$= 1.35 \text{ k}\Omega$$

c.  $Z_o = R_C = 6.8 \text{ k}\Omega$

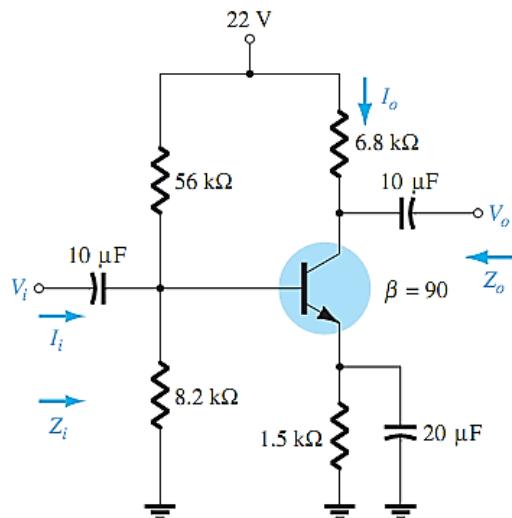
d.  $A_v = -\frac{R_C}{r_e} = -\frac{6.8 \text{ k}\Omega}{18.44 \Omega} = -368.76$

e.  $Z_i = 1.35 \text{ k}\Omega$

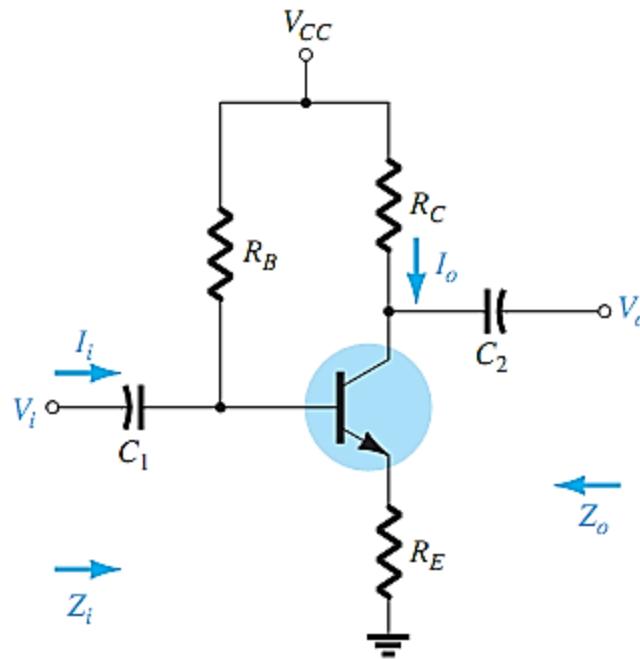
$$Z_o = R_C \parallel r_o = 6.8 \text{ k}\Omega \parallel 50 \text{ k}\Omega = 5.98 \text{ k}\Omega \text{ vs. } 6.8 \text{ k}\Omega$$

$$A_v = -\frac{R_C \parallel r_o}{r_e} = -\frac{5.98 \text{ k}\Omega}{18.44 \Omega} = -324.3 \text{ vs. } -368.76$$

There was a measurable difference in the results for  $Z_o$  and  $A_v$ , because the condition  $r_o \geq 10R_C$  was *not* satisfied.

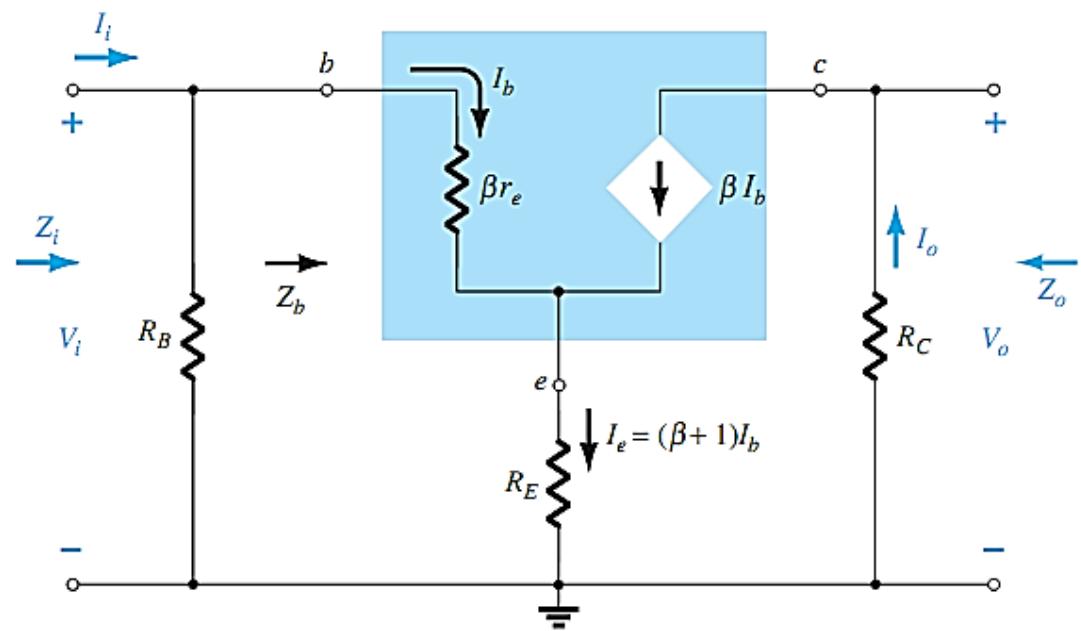


## COMMON-EMITTER EMITTER-BIAS CONFIGURATION: UNBYPASSED $R_E$



**FIG. 5.29**

CE emitter-bias configuration.



**FIG. 5.30**

Substituting the  $r_e$  equivalent circuit into the ac equivalent network of Fig. 5.29.

# IMPEDANCE CALCULATION

## INPUT IMPEDANCE, $Z_i$

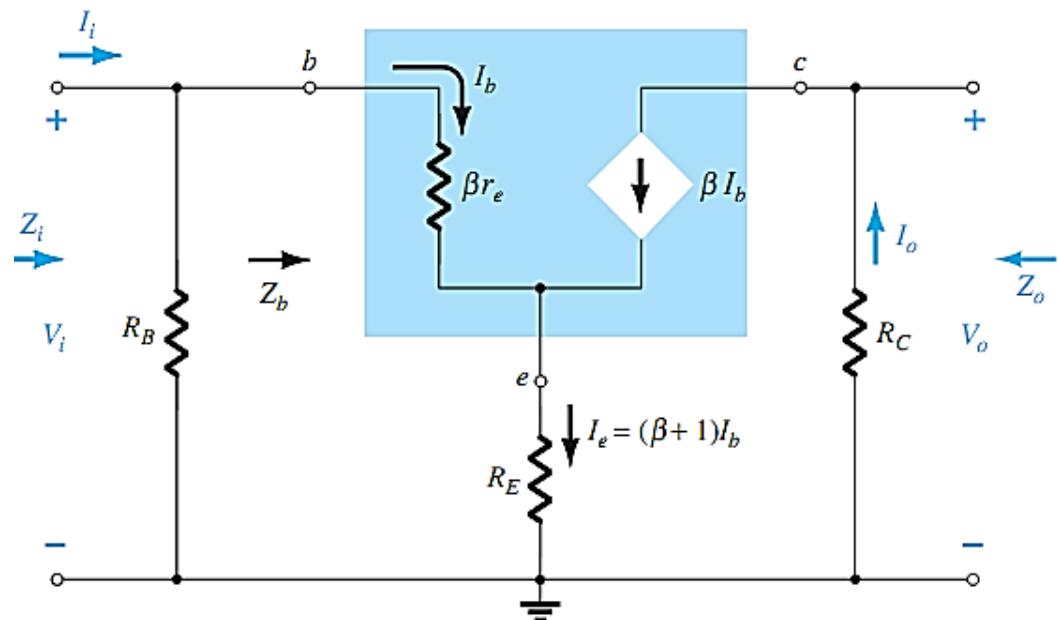
$$V_i = I_b \beta r_e + I_e R_E \\ = I_b \beta r_e + (\beta + 1) I_b R_E$$

$$Z_b = \frac{V_i}{I_b} = \beta r_e + (\beta + 1) R_E$$

$$Z_b \approx \beta r_e + \beta R_E = \beta(r_e + R_E)$$

$$Z_b \approx \beta R_E \quad \text{for } R_E \gg r_e$$

$$Z_i = R_B \parallel Z_b$$



## OUTPUT IMPEDANCE, $Z_o$

$$Z_o = R_C$$

# GAIN CALCULATIONS

## VOLTAGE GAIN, $A_v$

$$V_o = -I_o R_C = -\beta I_b R_C = -\beta \left(\frac{V_i}{Z_b}\right) R_C$$

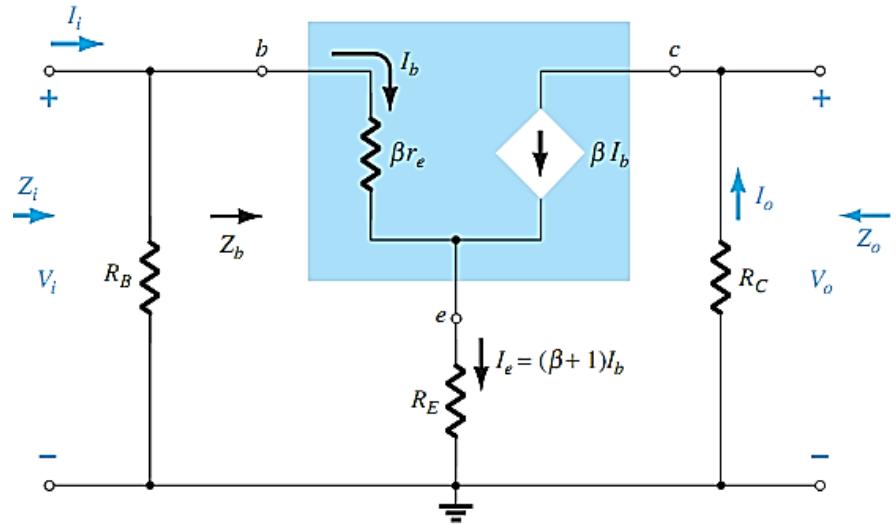
$$A_v = \frac{V_o}{V_i} = -\frac{\beta R_C}{Z_b}$$

*Substituting*  $Z_b \cong \beta(r_e + R_E)$

$$A_v = \frac{V_o}{V_i} = -\frac{R_C}{r_e + R_E}$$

*For the approximation*  $Z_b \cong \beta R_E$

$$A_v = \frac{V_o}{V_i} = -\frac{R_C}{R_E}$$

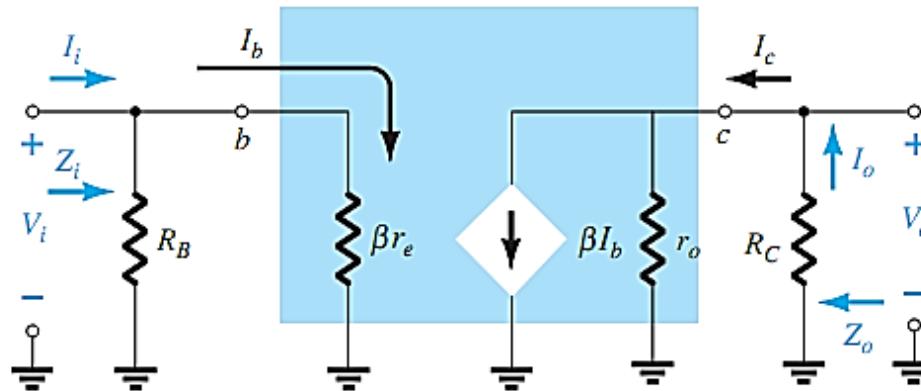


The negative sign in gain equations reveals  $180^\circ$  phase shift between input and output waveforms.

# COMMON-EMITTER Emitter-Bias Configuration: BYPASSED $R_E$

## Bypassed

If  $R_E$  is bypassed by an emitter capacitor  $C_E$ , the complete  $r_e$  equivalent model can be substituted, resulting in the same equivalent network as Fig. 5.22. Equations of slide no. 13 are therefore applicable.



**FIG. 5.22**

Substituting the  $r_e$  model into the network of Fig. 5.21.

# EXAMPLE

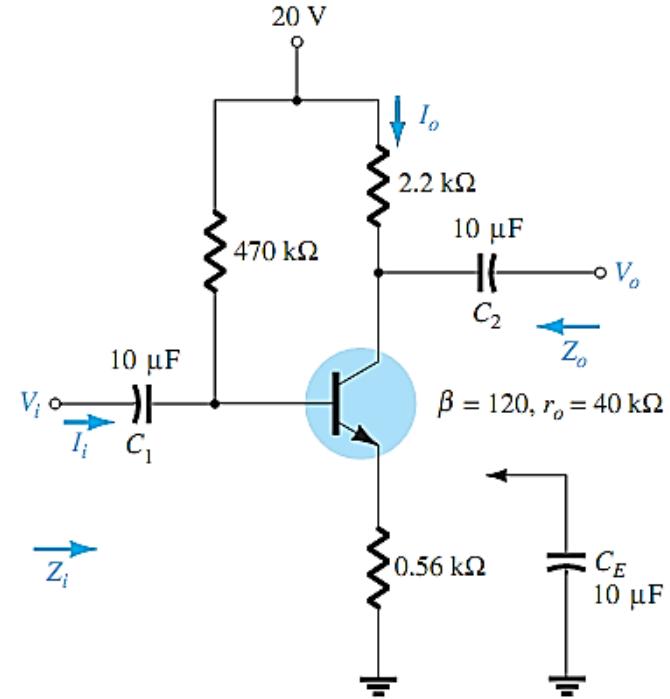
- **EXAMPLE 5.3:** For the network of following Fig, without  $C_E$  (unbypassed), determine:  $r_e$ ,  $Z_i$ ,  $Z_o$  &  $A_v$ .

a. DC:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20 \text{ V} - 0.7 \text{ V}}{470 \text{ k}\Omega + (121)0.56 \text{ k}\Omega} = 35.89 \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (121)(35.89 \mu\text{A}) = 4.34 \text{ mA}$$

and  $r_e = \frac{26 \text{ mV}}{I_E} = \frac{26 \text{ mV}}{4.34 \text{ mA}} = 5.99 \Omega$



**FIG. 5.32**  
Example 5.3.

## EXAMPLE Contd.

b. Testing the condition  $r_o \geq 10(R_C + R_E)$ , we obtain

$$40 \text{ k}\Omega \geq 10(2.2 \text{ k}\Omega + 0.56 \text{ k}\Omega)$$

$$40 \text{ k}\Omega \geq 10(2.76 \text{ k}\Omega) = 27.6 \text{ k}\Omega \text{ (satisfied)}$$

Therefore,

$$\begin{aligned} Z_b &\cong \beta(r_e + R_E) = 120(5.99 \Omega + 560 \Omega) \\ &= 67.92 \text{ k}\Omega \end{aligned}$$

and

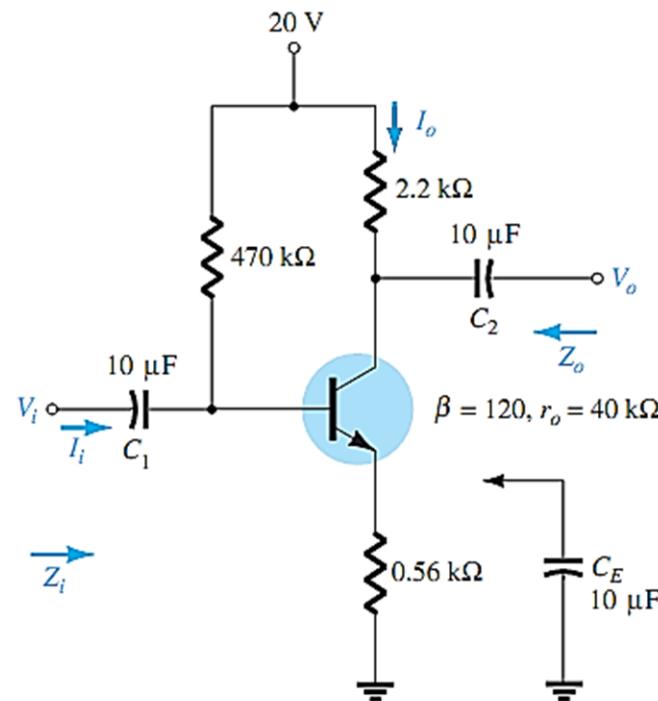
$$\begin{aligned} Z_i &= R_B \| Z_b = 470 \text{ k}\Omega \| 67.92 \text{ k}\Omega \\ &= 59.34 \text{ k}\Omega \end{aligned}$$

c.  $Z_o = R_C = 2.2 \text{ k}\Omega$

d.  $r_o \geq 10R_C$  is satisfied. Therefore,

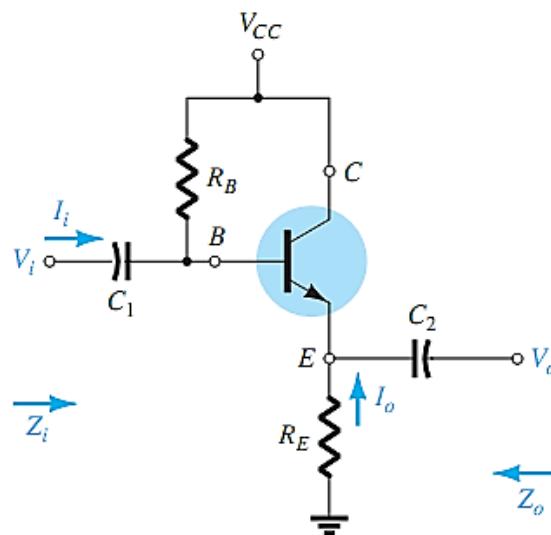
$$\begin{aligned} A_v &= \frac{V_o}{V_i} \cong -\frac{\beta R_C}{Z_b} = -\frac{(120)(2.2 \text{ k}\Omega)}{67.92 \text{ k}\Omega} \\ &= -3.89 \end{aligned}$$

compared to  $-3.93$  using Eq. (5.20):  $A_v \cong -R_C/R_E$ .



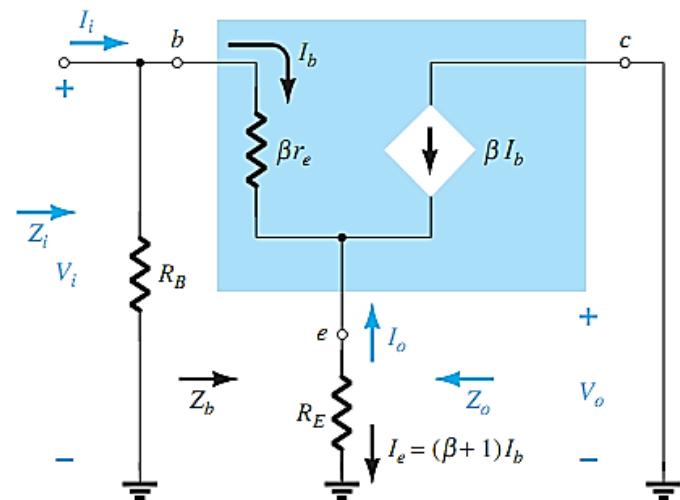
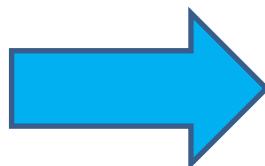
**FIG. 5.32**  
Example 5.3.

# EMITTER-FOLLOWER CONFIGURATION



**FIG. 5.36**

Emitter-follower configuration.



**FIG. 5.37**

Substituting the  $r_e$  equivalent circuit into the ac equivalent network of Fig. 5.36.

- This is also known as the common-collector configuration.
- The input is applied to the base and the output is taken from the emitter.
- There is no phase shift between input and output.

# IMPEDANCE CALCULATIONS

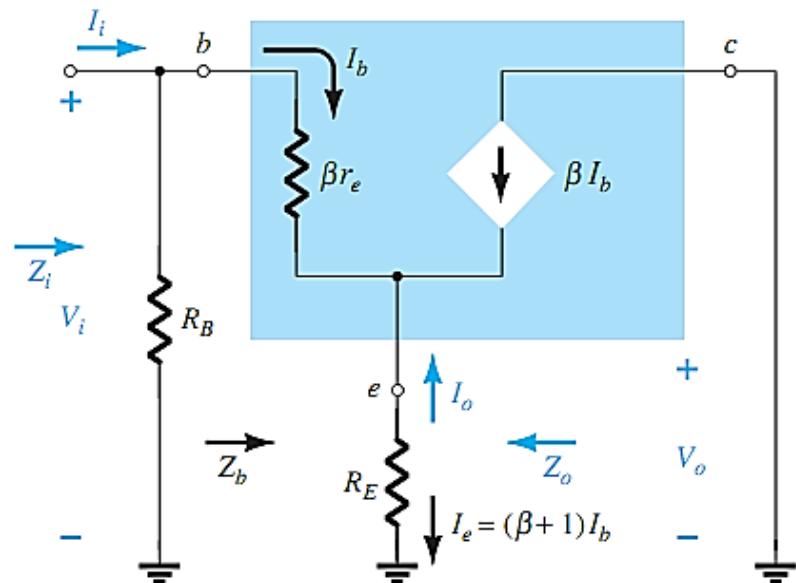
## INPUT IMPEDANCE, $Z_i$

$$Z_i = R_B \parallel Z_b$$

$$Z_b = \beta r_e + (\beta + 1)R_E$$

$$Z_b \cong \beta(r_e + R_E)$$

$$Z_b \cong \beta R_E \quad \text{for } R_E \gg r_e$$



# IMPEDANCE CALCULATIONS

## OUTPUT IMPEDANCE, $Z_o$

$$I_b = \frac{V_i}{Z_b},$$

$$I_E = (\beta + 1)I_b = (\beta + 1) \frac{V_i}{Z_b}$$

$$I_E = \frac{(\beta + 1)V_i}{\beta r_e + (\beta + 1)R_E}$$

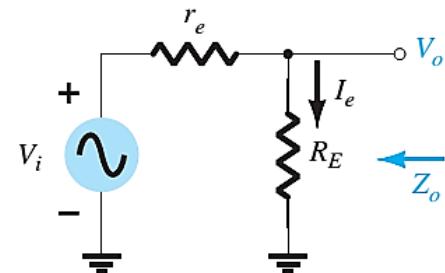
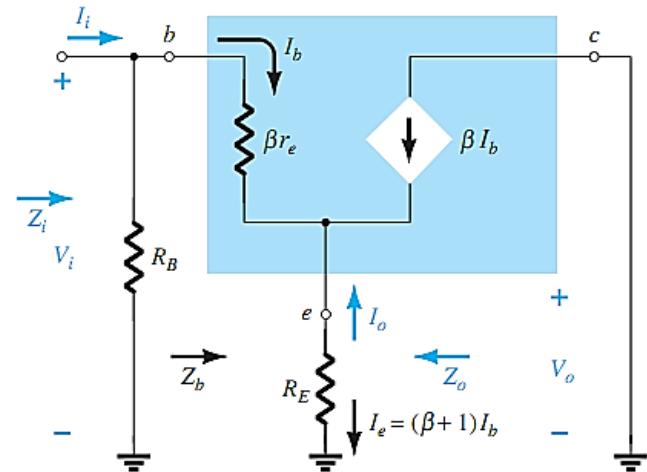
Since  $(\beta + 1) \cong \beta$

$$I_E = \frac{V_i}{r_e + R_E}$$

To determine  $Z_o$ ,  $V_i$  is set to zero

$$Z_o = R_E \parallel r_e$$

$$Z_o = r_e \quad |_{R_E \gg r_e}$$



**FIG. 5.38**

Defining the output impedance for the emitter-follower configuration.

# GAIN CALCULATIONS

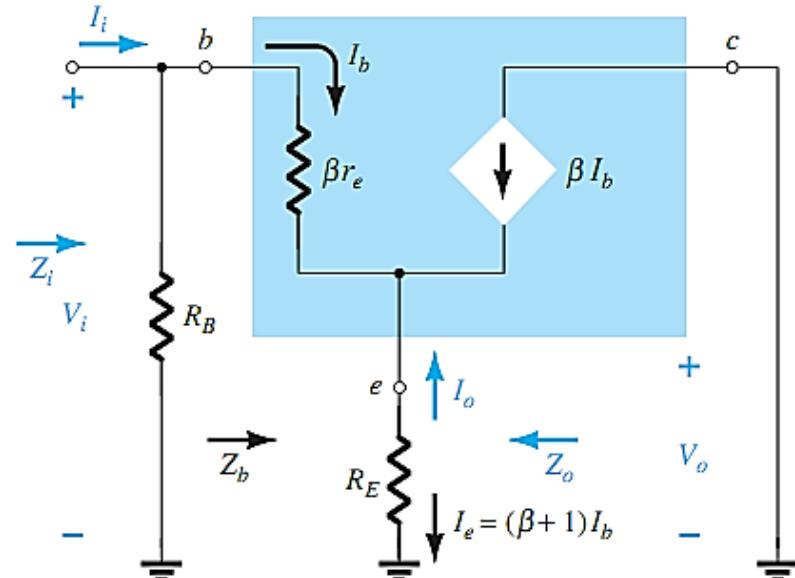
## VOLTAGE GAIN, $A_v$

$$V_o = I_e R_E = (\beta + 1) I_b R_E = \frac{V_i(\beta + 1) R_E}{Z_b}$$

when  $r_o \geq 10R_E$  and  $\beta + 1 \cong \beta$

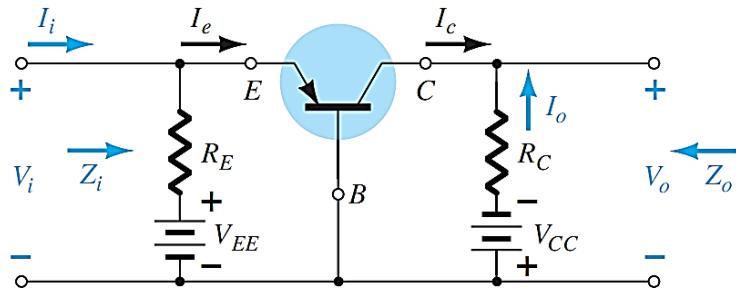
But  $Z_b \cong \beta(r_e + R_E)$

$$A_v = \frac{V_o}{V_i} \cong \frac{\beta R_E}{\beta(r_e + R_E)} \cong \frac{R_E}{(r_e + R_E)}$$



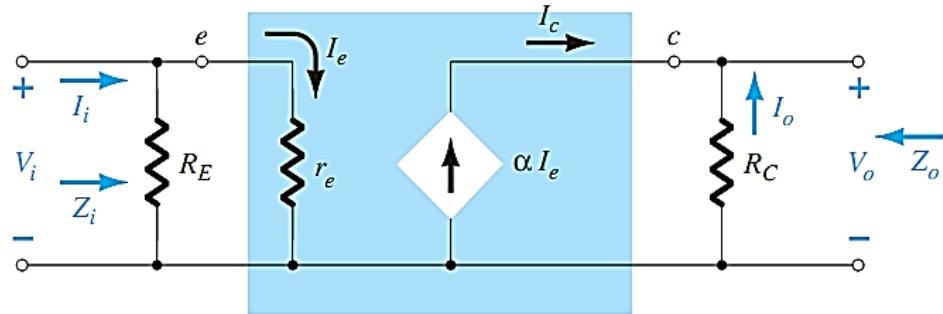
□ See Example 5.7

# COMMON-BASE CONFIGURATION



**FIG. 5.42**

Common-base configuration.



**FIG. 5.43**

Substituting the  $r_e$  equivalent circuit into the ac equivalent network of Fig. 5.44.

- The input is applied to the emitter.
- The output is taken from the collector.
- Low input impedance.
- High output impedance.
- Very high voltage gain.
- No phase shift between input and output.



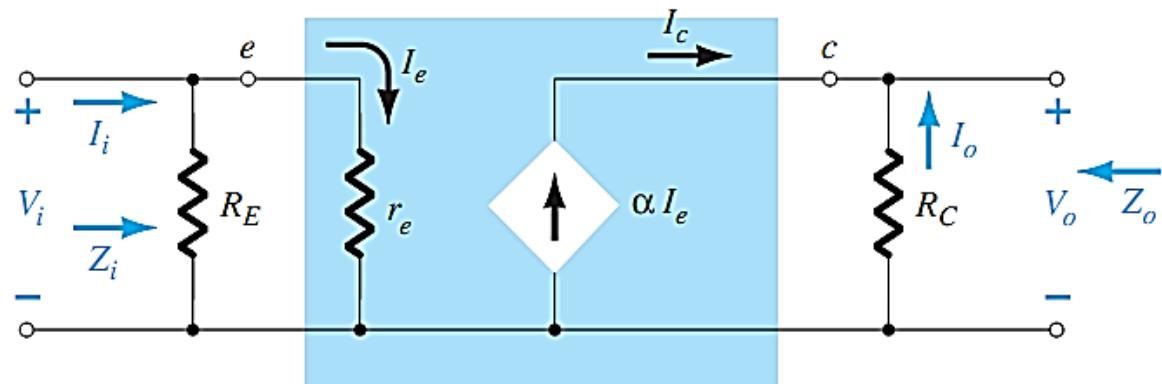
# CALCULATIONS

**INPUT IMPEDANCE,  $Z_i$**

$$Z_i = R_E \parallel r_e$$

**OUTPUT IMPEDANCE,  $Z_o$**

$$Z_o = R_C$$



**VOLTAGE GAIN,  $A_v$**

$$V_o = -I_o R_C = -(I_C) R_C = \alpha I_e R_C ; \quad I_e = \frac{V_i}{r_e}$$

$$V_o = \alpha \left( \frac{V_i}{r_e} \right) R_C ; \quad A_v = \frac{V_o}{V_i} = \frac{\alpha R_C}{r_e} \cong \frac{R_C}{r_e}$$

**CURRENT GAIN,  $A_i$**

*Assuming  $R_E \gg r_e$*

$$I_e = I_i$$

$$I_o = -\alpha I_e = -\alpha I_i$$

$$A_i = \frac{I_o}{I_i} = -\alpha \cong -1$$

# COMMON-BASE CONFIGURATION

- Phase Relationship:

The fact that  $A_v$  is a positive number shows that  $V_o$  and  $V_i$  are in phase for the common-base configuration.

- Effect of  $r_o$ :

For the common-base configuration,  $r_o = 1/h_{ob}$  is typically in the megohm range and sufficiently larger than the parallel resistance  $R_C$  to permit the approximation  $r_o \parallel R_C \cong R_C$ .



# EXAMPLE

- **EXAMPLE 5.8:** For the network of following figure, determine:  $r_e$ ,  $Z_i$ ,  $Z_o$ ,  $A_v$ ,  $A_i$

a.  $I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{2 \text{ V} - 0.7 \text{ V}}{1 \text{ k}\Omega} = \frac{1.3 \text{ V}}{1 \text{ k}\Omega} = 1.3 \text{ mA}$

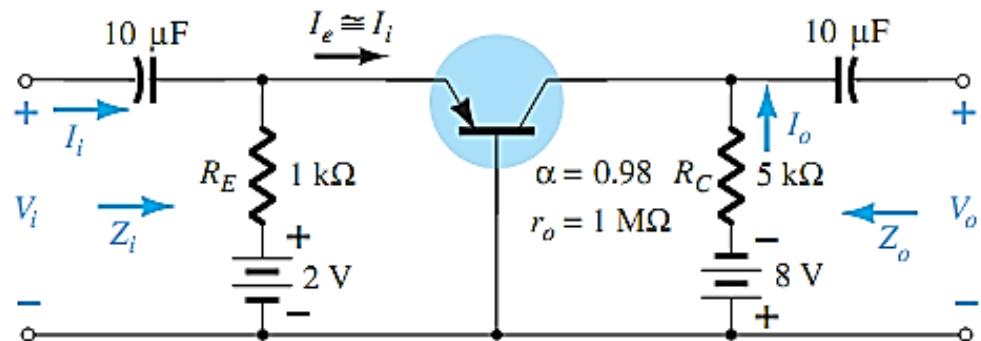
$$r_e = \frac{26 \text{ mV}}{I_E} = \frac{26 \text{ mV}}{1.3 \text{ mA}} = 20 \Omega$$

b.  $Z_i = R_E \parallel r_e = 1 \text{ k}\Omega \parallel 20 \Omega$   
 $= 19.61 \Omega \cong r_e$

c.  $Z_o = R_C = 5 \text{ k}\Omega$

d.  $A_v \cong \frac{R_C}{r_e} = \frac{5 \text{ k}\Omega}{20 \Omega} = 250$

e.  $A_i = -0.98 \cong -1$



**FIG. 5.44**

Example 5.8.

# End of Lecture-2

# FETs vs BJTs

- FET's (Field – Effect Transistors) are much like BJT's (Bipolar Junction Transistors).
- ***Similarities:***
  - Amplifiers
  - Switching devices
  - Impedance matching circuits
- ***Differences:***
  - FET's are voltage controlled devices whereas BJT's are current controlled devices.
  - FET's are unipolar devices whereas BJT's are bipolar devices.
  - FET's also have a higher input impedance, but BJT's have higher gains.
  - FET's are less sensitive to temperature variations and because of their construction they are more easily integrated into IC's.



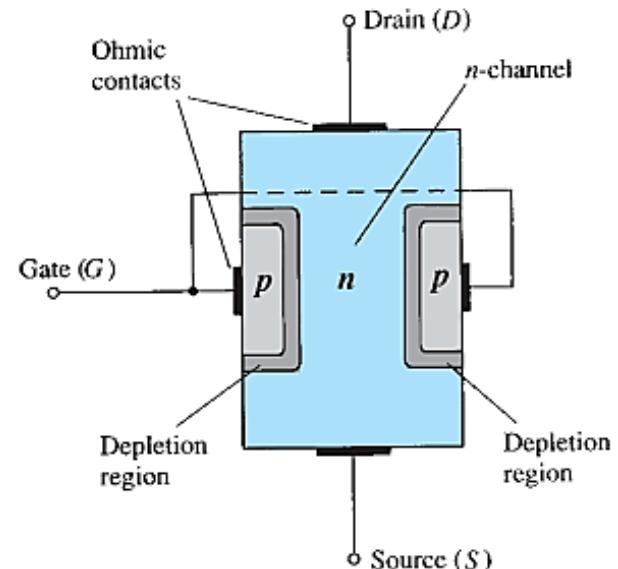
# FET TYPES

- JFET: Junction Field-Effect Transistor
- MOSFET: Metal-Oxide Semiconductor Field-Effect Transistor
  - »D-MOSFET ~ Depletion type MOSFET
  - »E-MOSFET ~ Enhancement type MOSFET



# JFET CONSTRUCTION

- There are two types of JFETs
  - n- channel
  - p- channel
- The n-channel is more widely used.
- There are *three terminals*:
  - **Drain (D)** and **Source (S)** are connected to n-channel
  - **Gate (G)** is connected to the p-type material
- Check this: <http://www-g.eng.cam.ac.uk/mmg/teaching/linearcircuits/jfet.html>



**FIG. 6.3**

Junction field-effect transistor (JFET).

# BASIC OPERATION OF JFET

- JFET operation can be compared to a water spigot.
- The **source of water** pressure is the **accumulation of electrons** at the **negative pole of the drain-source voltage**.
- The **drain of the water** is the **electron deficiency (or holes)** at the **positive pole of the applied voltage**.
- The **control of flow of water** is the **gate voltage** that **controls the width of the n channel** and therefore, the **flow of charges** from source to drain.

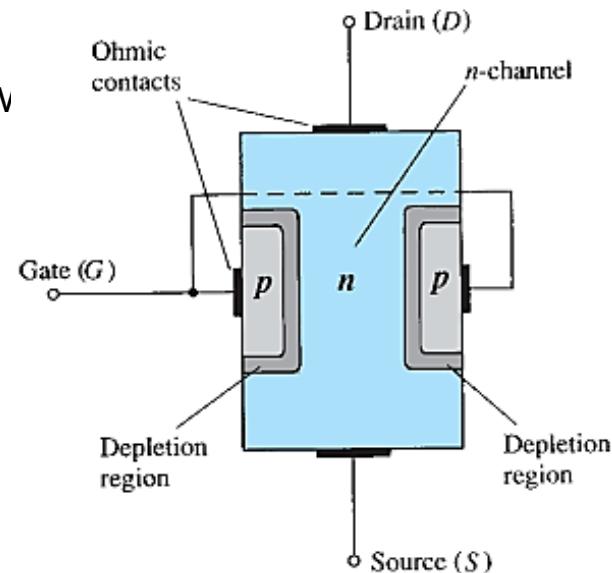


**FIG. 6.4**

*Water analogy for the JFET control mechanism.*

# JFET OPERATING CHARACTERISTICS

- There are three basic operating conditions for a JFET:
  - $V_{GS} = 0$ ,  $V_{DS}$  increasing to some positive value
  - $V_{GS} < 0$ ,  $V_{DS}$  at some positive value
  - Voltage-Controlled Resistor



**FIG. 6.3**  
Junction field-effect transistor (JFET).

## JFET OPERATING CHARACTERISTICS: $V_{GS} = 0 \text{ V}$

- Three things happen when  $V_{GS} = 0$  and  $V_{DS}$  is increased from 0 to a more positive voltage:
  - The depletion region between p-gate and n-channel increases as **electrons from n-channel combine with holes from p-gate**.
  - Increasing the depletion region**, decreases the size of the n-channel which **increases the resistance of the n-channel**.
  - But even **though the n-channel resistance is increasing**, the **current ( $I_D$ ) from Source to Drain** through the n-channel **is increasing**. This is because  **$V_{DS}$  is increasing**.

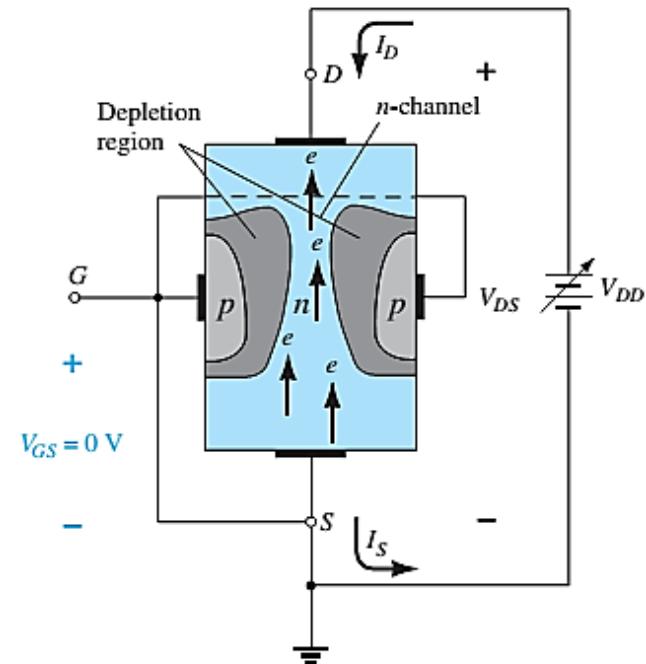
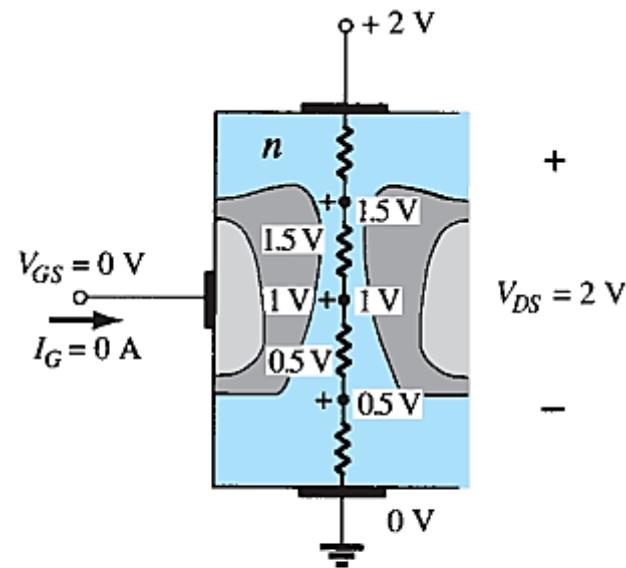


FIG. 6.5

JFET at  $V_{GS} = 0 \text{ V}$  and  $V_{DS} > 0 \text{ V}$ .

## JFET OPERATING CHARACTERISTICS: $V_{GS} = 0 \text{ V}$

- It is important to note that the **depletion region is wider near the top of both p-type Materials**.
- Assuming a uniform resistance in the n-channel, the resistance of the channel can be broken down to the divisions appearing in Figure.
- The current  $I_D$  will establish the voltage levels through the channel** as indicated on the same figure. The result is that the upper region of the p-type material will be reverse biased by about 1.5 V, with the lower region only reverse-biased by 0.5 V.
- The greater the applied reverse bias, the wider the depletion region**—hence the distribution of the depletion region as shown in figure. The fact that the **p-n junction is reverse-biased for the length of the channel results in a gate current of zero amperes**.

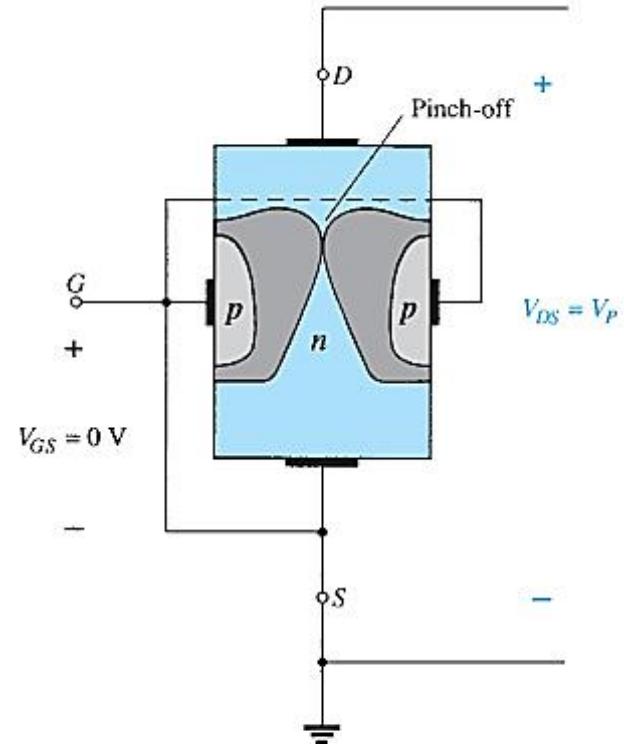


**FIG. 6.6**

Varying reverse-bias potentials across the p-n junction of an n-channel JFET.

## PINCH-OFF

- If  $V_{GS} = 0$  and  $V_{DS}$  is further increased to a more positive voltage, then the depletion zone gets so large that it **pinches off the n-channel**.
- This suggests that **the current in the n-channel ( $I_D$ ) would drop to 0A**, but it does just the opposite: as  $V_{DS}$  increases, so does  $I_D$ .



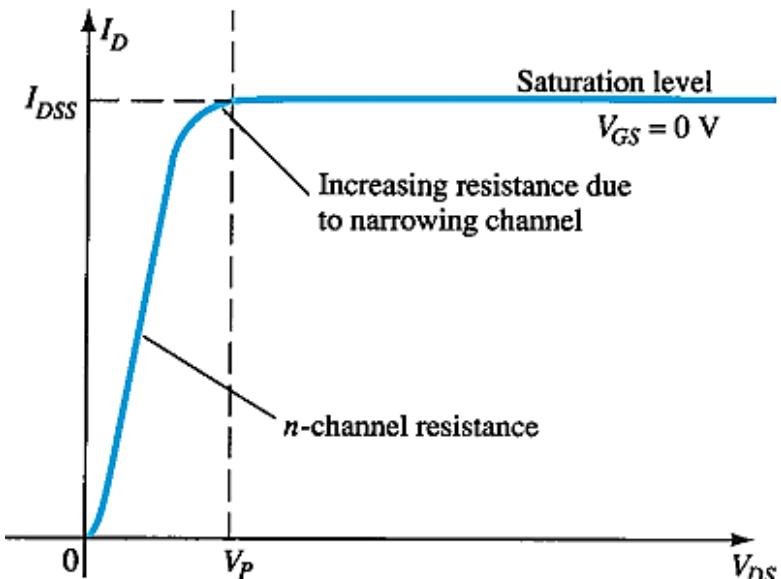
**FIG. 6.8**

Pinch-off ( $V_{GS} = 0 \text{ V}$ ,  $V_{DS} = V_P$ ).

# SATURATION

At the pinch-off point:

- Any further increase in  $V_{DS}$  does not produce any increase in  $I_D$ .  $V_{DS}$  at pinch-off is denoted as  $V_p$ .
- $I_D$  is at saturation or maximum. It is referred to as  $I_{DSS}$ .
- The ohmic value of the channel is at maximum.



**FIG. 6.7**

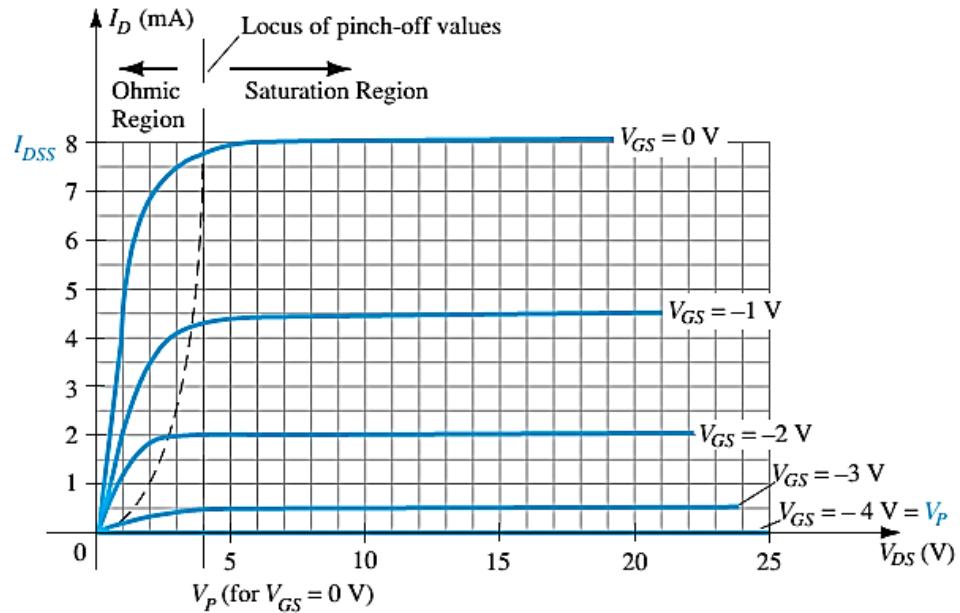
$I_D$  versus  $V_{DS}$  for  $V_{GS} = 0$  V.



$$I_D < I_{DSS}$$

As  $V_{GS}$  becomes more negative:

- The JFET will pinch-off at a lower value of  $V_{DS}$ .
- $I_D$  decreases ( $I_D < I_{DSS}$ ) even though  $V_{DS}$  is increased.
- Eventually  $I_D$  will reach 0A.  $V_{GS}$  at this point is called  $V_p$  or  $V_{GS(off)}$ .
- Also note that at high levels of  $V_{DS}$  the JFET reaches a breakdown situation.  $I_D$  will increases uncontrollably if  $V_{DS} > V_{DS\max}$ .

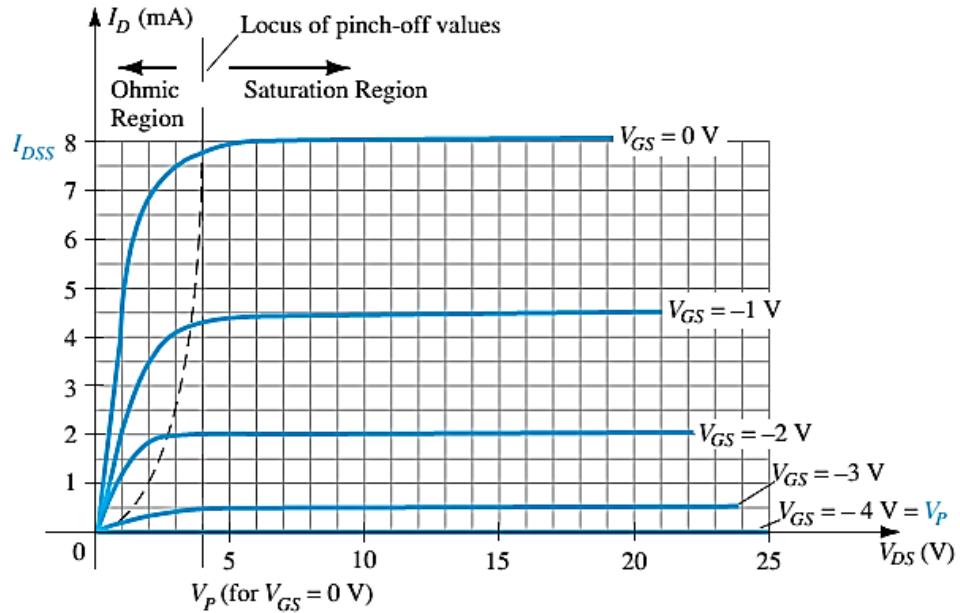


**FIG. 6.11**

*n-Channel JFET characteristics with  $I_{DSS} = 8 \text{ mA}$  and  $V_P = -4 \text{ V}$ .*

## JFET OPERATING CHARACTERISTICS: VOLTAGE CONTROLLED RESISTOR

- The region to the left of the pinch-off point is called the ohmic region.
- The JFET can be used as a variable resistor, where  $V_{GS}$  controls the drain-source resistance ( $r_d$ ).
- The slope of each curve and therefore the resistance of the device between drain and source for  $V_{DS} < V_P$  is a function of the applied voltage  $V_{GS}$ .
- As  $V_{GS}$  becomes more negative, the resistance ( $r_d$ ) increases.



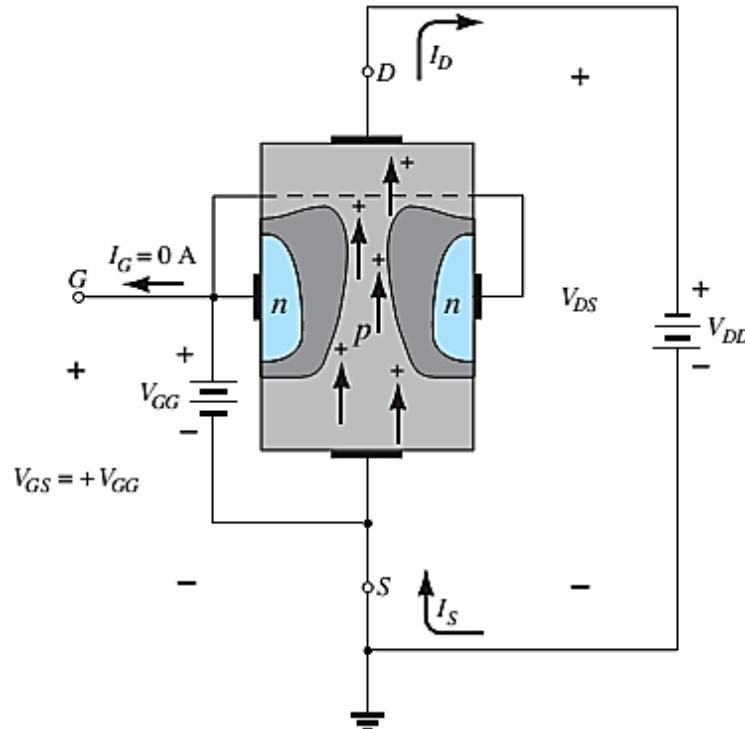
**FIG. 6.11**  
n-Channel JFET characteristics with  $I_{DSS} = 8 \text{ mA}$  and  $V_P = -4 \text{ V}$ .

$$r_d = \frac{r_o}{(1 - V_{GS}/V_P)^2}$$



# P-CHANNEL JFETS

- p-Channel JFET acts the same as the n-channel JFET, except the polarities and currents are reversed.



**FIG. 6.12**  
*p-Channel JFET.*



# Electronic Devices

## Final Term Lecture - 04

Reference book:

**Electronic Devices and Circuit Theory (Chapter-6)**

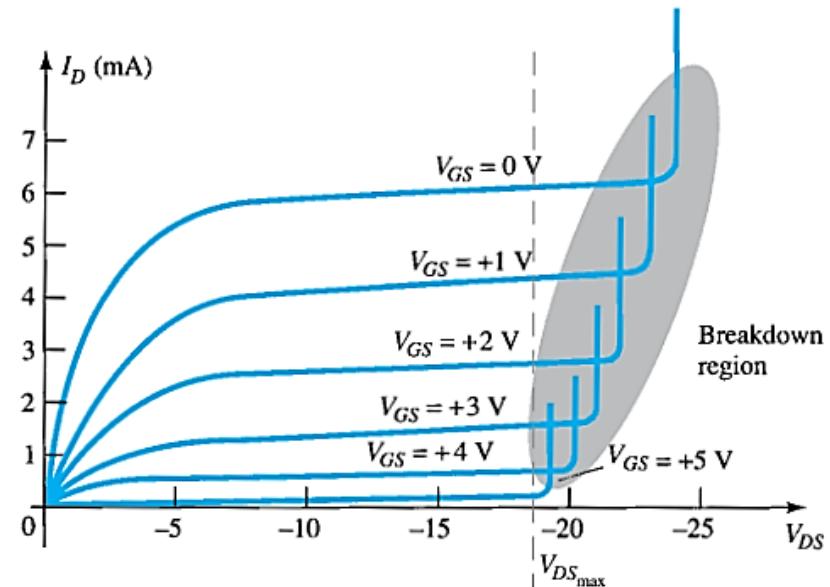
Robert L. Boylestad and L. Nashelsky , (11<sup>th</sup> Edition)



**Faculty of Engineering**  
American International University-Bangladesh

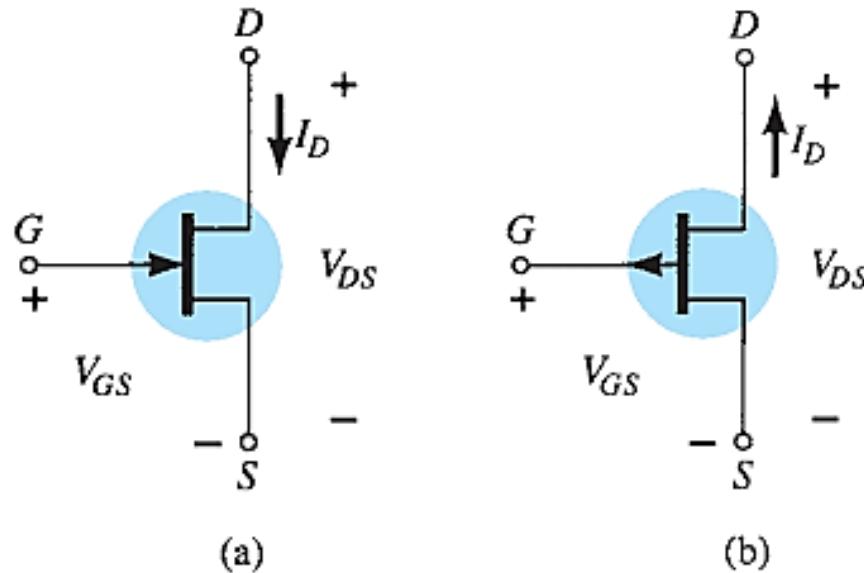
# P-CHANNEL JFET CHARACTERISTICS

- As  $V_{GS}$  increases more positively:
  - The depletion zone increases
  - $I_D$  decreases ( $I_D < I_{DSS}$ )
  - Eventually  $I_D = 0A$
- Also note that at high levels of  $V_{DS}$  the JFET reaches a breakdown situation.  $I_D$  increases uncontrollably if  $V_{DS} > V_{DS\max}$ .



**FIG. 6.13**  
p-Channel JFET characteristics with  $I_{DSS} = 6\text{ mA}$  and  $V_P = +6\text{ V}$ .

## JFET SYMBOLS



**FIG. 6.14**

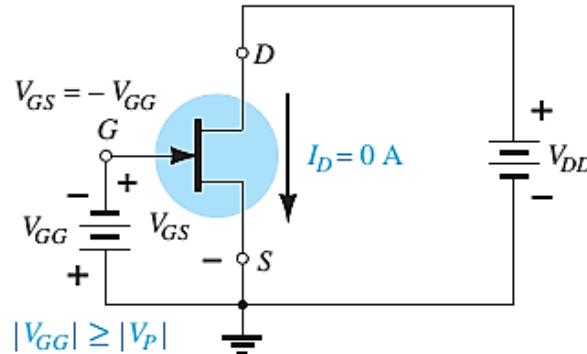
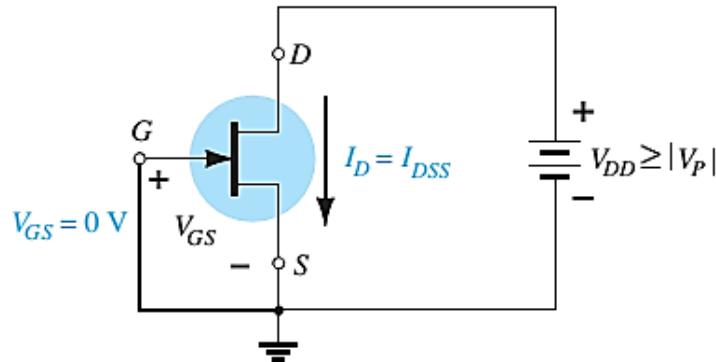
*JFET symbols: (a) n-channel; (b) p-channel.*

## SUMMARY TILL NOW

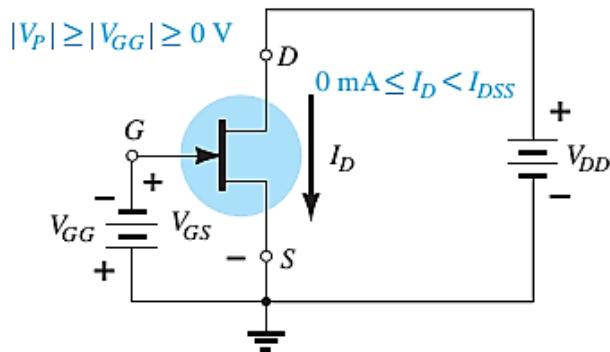
- The maximum current is defined as  $I_{DSS}$  and occurs when  $V_{GS} = 0 \text{ V}$  and  $V_{DS} \geq |V_p|$ , as shown in Fig. 6.15a .
- For gate-to-source voltages  $V_{GS}$  is less than (more negative than) the pinch-off level, the drain current is 0 A ( $I_D = 0 \text{ A}$ ), as in Fig. 6.15b .
- For all levels of  $V_{GS}$  between 0 V and the pinch-off level, the current  $I_D$  will range between  $I_{DSS}$  and 0 A, respectively, as in Fig. 6.15c.
- A similar list can be developed for p-channel JFETs.



# SUMMARY TILL NOW



(b)



(c)

**FIG. 6.15**

(a)  $V_{GS} = 0 \text{ V}, I_D = I_{DSS}$ ; (b) cutoff ( $I_D = 0 \text{ A}$ )  $V_{GS}$  less than the pinch-off level; (c)  $I_D$  is between  $0 \text{ A}$  and  $I_{DSS}$  for  $V_{GS} \leq 0 \text{ V}$  and greater than the pinch-off level.

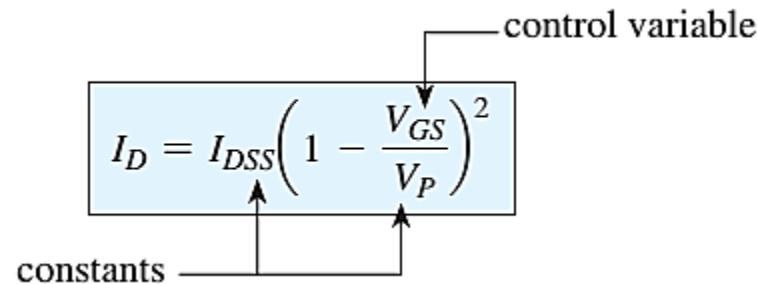
# JFET TRANSFER CHARACTERISTICS

- The transfer characteristic of **input-to-output** is not as straight forward in a JFET as it was in a BJT.
- In a BJT,  $\beta$  indicated the relationship between  $I_B$  (input) and  $I_C$  (output).
- In a JFET, the relationship of  $V_{GS}$  (input) and  $I_D$  (output) is a little more complicated (Shockley's equation):

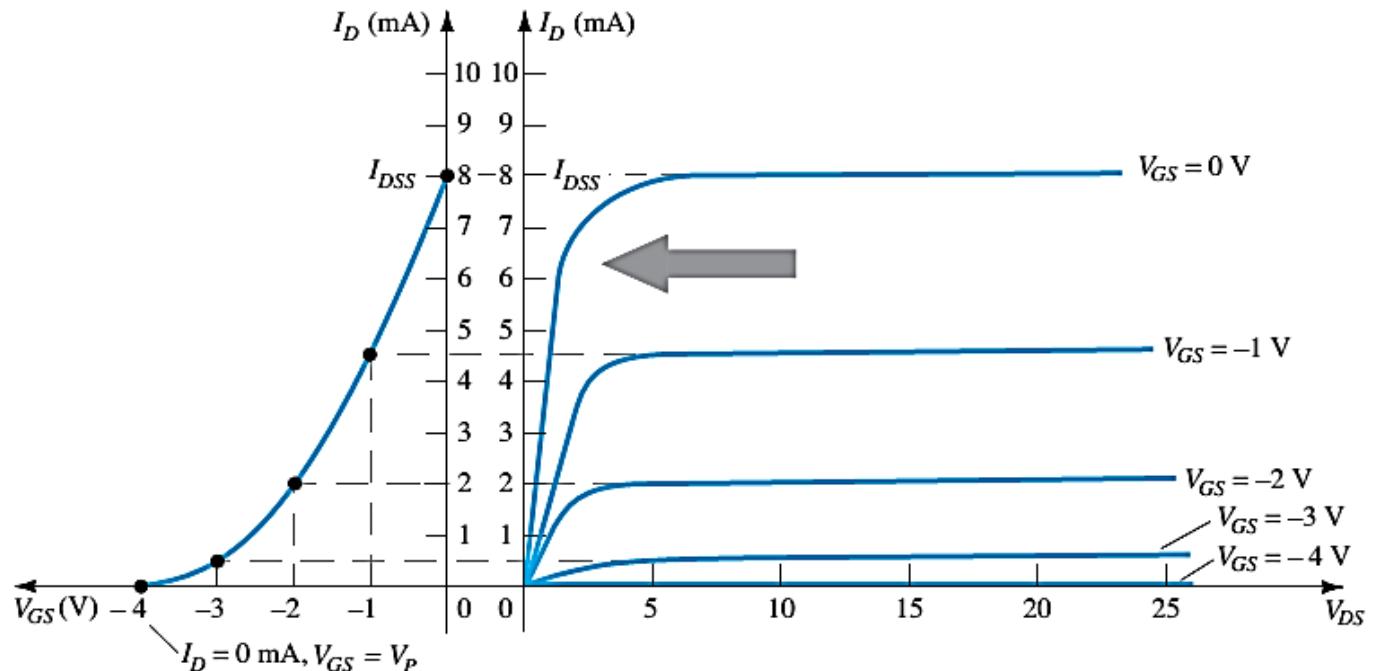
$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

control variable

constants



# TRANSFER CURVE



**FIG. 6.17**  
Obtaining the transfer curve from the drain characteristics.

## PLOTTING THE TRANSFER CURVE

- Using  $I_{DSS}$  and  $V_p$  ( $V_{GS(off)}$ ) values found in a specification sheet, the Transfer Curve can be plotted using these 3 steps:

- Step 1:  $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$

Solving for  $V_{GS} = 0V$ :  $I_D = I_{DSS} \quad \checkmark$   
 $V_{GS} = 0V$

- Step 2:  $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$

Solving for  $V_{GS} = V_p$   $\checkmark$   
 $V_{GS} = V_p$

- Step 3:

Solving for  $V_{GS} = 0V$  to  $V_p$   $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$



# SHORTHAND METHOD

$V_{GS}$	$I_D$
0	$I_{DSS}$
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
$V_P$	0mA

When  $VGS = 0$  V,  $ID =$   
 $IDSS$

When  $VGS = VP$ ,  $ID = 0$   
mA



# EXAMPLE

**EXAMPLE 6.1** Sketch the transfer curve defined by  $I_{DSS} = 12 \text{ mA}$  and  $V_P = -6 \text{ V}$ .

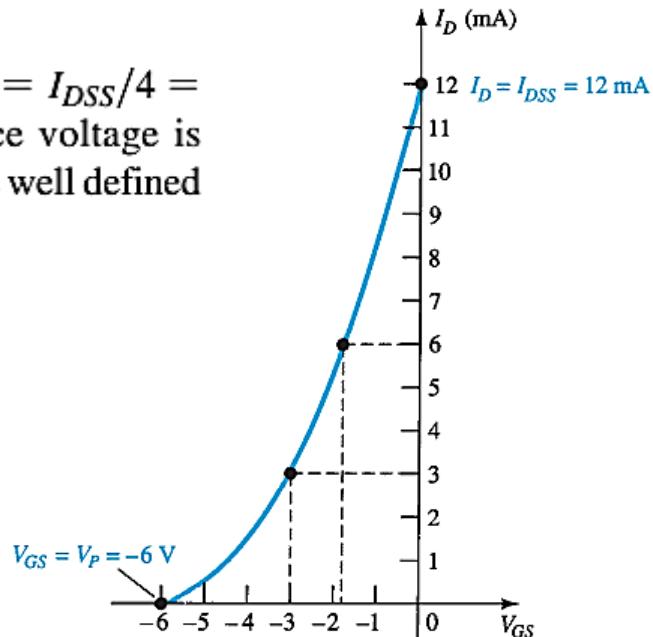
**Solution:** Two plot points are defined by

$$I_{DSS} = 12 \text{ mA} \quad \text{and} \quad V_{GS} = 0 \text{ V}$$

and

$$I_D = 0 \text{ mA} \quad \text{and} \quad V_{GS} = V_P$$

At  $V_{GS} = V_P/2 = -6 \text{ V}/2 = -3 \text{ V}$  the drain current is determined by  $I_D = I_{DSS}/4 = 12 \text{ mA}/4 = 3 \text{ mA}$ . At  $I_D = I_{DSS}/2 = 12 \text{ mA}/2 = 6 \text{ mA}$  the gate-to-source voltage is determined by  $V_{GS} \cong 0.3V_P = 0.3(-6 \text{ V}) = -1.8 \text{ V}$ . All four plot points are well defined on Fig. 6.18 with the complete transfer curve.



**FIG. 6.18**

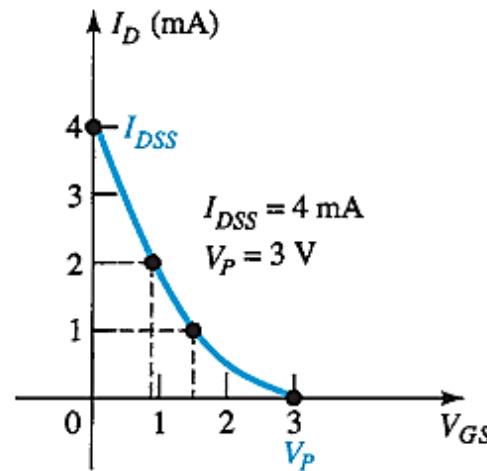
Transfer curve for Example 6.1.



## EXAMPLE

**EXAMPLE 6.2** Sketch the transfer curve for a *p*-channel device with  $I_{DSS} = 4 \text{ mA}$  and  $V_P = 3 \text{ V}$ .

**Solution:** At  $V_{GS} = V_P/2 = 3 \text{ V}/2 = 1.5 \text{ V}$ ,  $I_D = I_{DSS}/4 = 4 \text{ mA}/4 = 1 \text{ mA}$ . At  $I_D = I_{DSS}/2 = 4 \text{ mA}/2 = 2 \text{ mA}$ ,  $V_{GS} = 0.3V_P = 0.3(3 \text{ V}) = 0.9 \text{ V}$ . Both plot points appear in Fig. 6.19 along with the points defined by  $I_{DSS}$  and  $V_P$ .

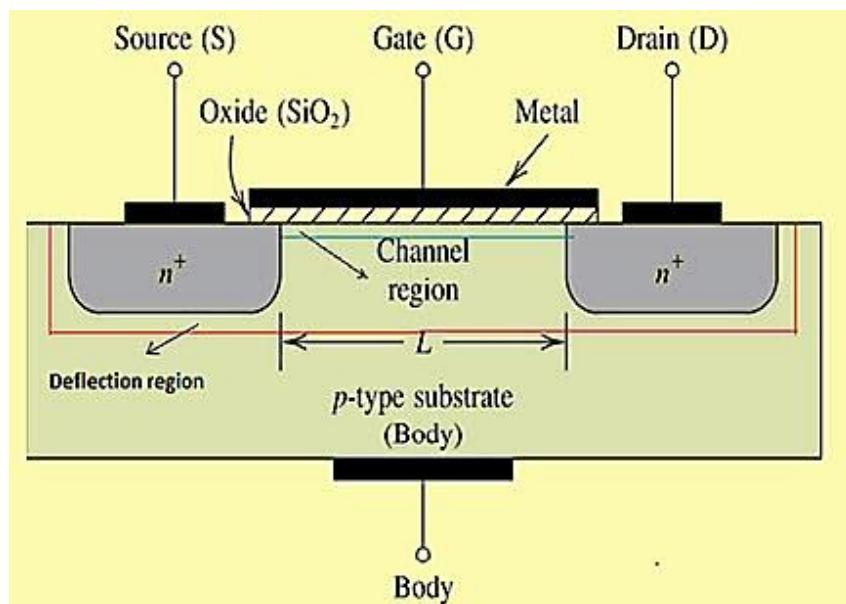


**FIG. 6.19**

Transfer curve for the *p*-channel device of Example 6.2.

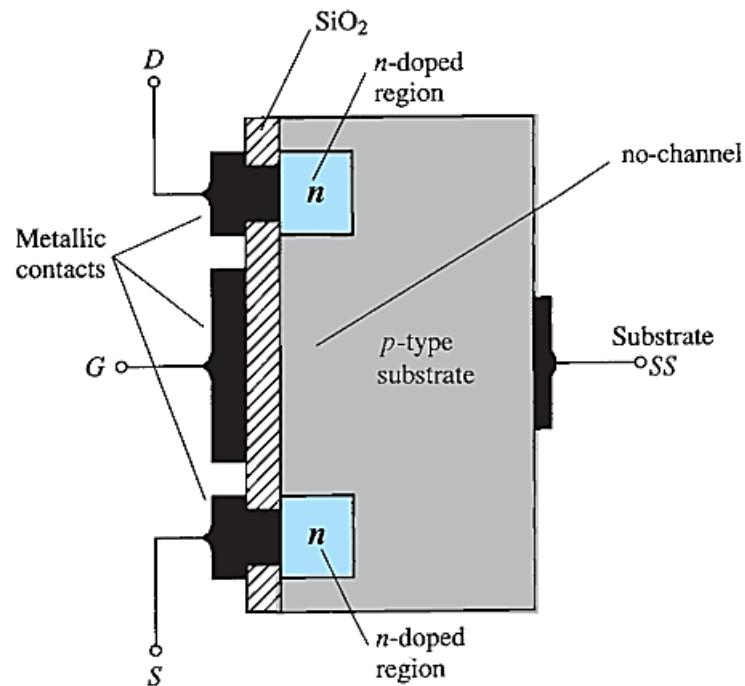
# MOSFETs

- MOSFETs have characteristics similar to JFETs and additional characteristics that make them very useful.
- There are 2 types:
  - Depletion-Type MOSFET
  - Enhancement-Type MOSFET



# ENHANCEMENT-TYPE MOSFET CONSTRUCTION

- The Drain (D) and Source (S) connect to the n-doped regions.
- The Gate (G) connects to the p-doped substrate via a thin insulating layer of  $\text{SiO}_2$ .
- There is no channel. The n-doped material lies on a p-doped substrate that may have an additional terminal connection called SS.
- In summary, therefore, the construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.

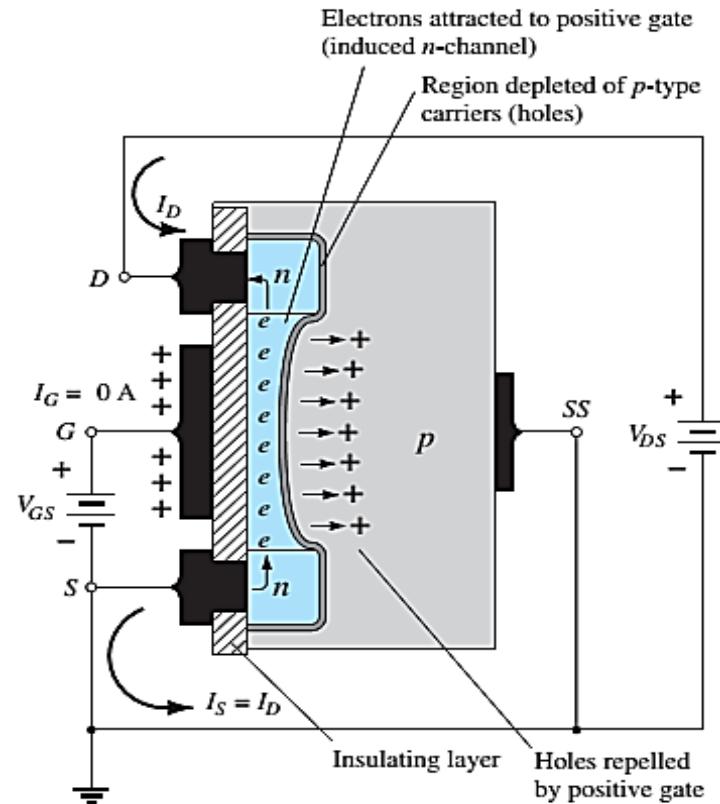


**FIG. 6.32**

*n-Channel enhancement-type MOSFET.*

## CONTINUED...

- As  $V_{GS}$  increases in magnitude, the concentration of electrons near the  $\text{SiO}_2$  surface increases until eventually the induced n-type region can support a measurable flow between drain and source.
- The level of  $V_{GS}$  that results in the significant increase in drain current is called the threshold voltage and is given the symbol  $V_T$ .
- Since the channel is nonexistent with  $V_{GS}=0$  V and “enhanced” by the application of a positive gate-to-source voltage, this type of MOSFET is called an enhancement-type MOSFET.



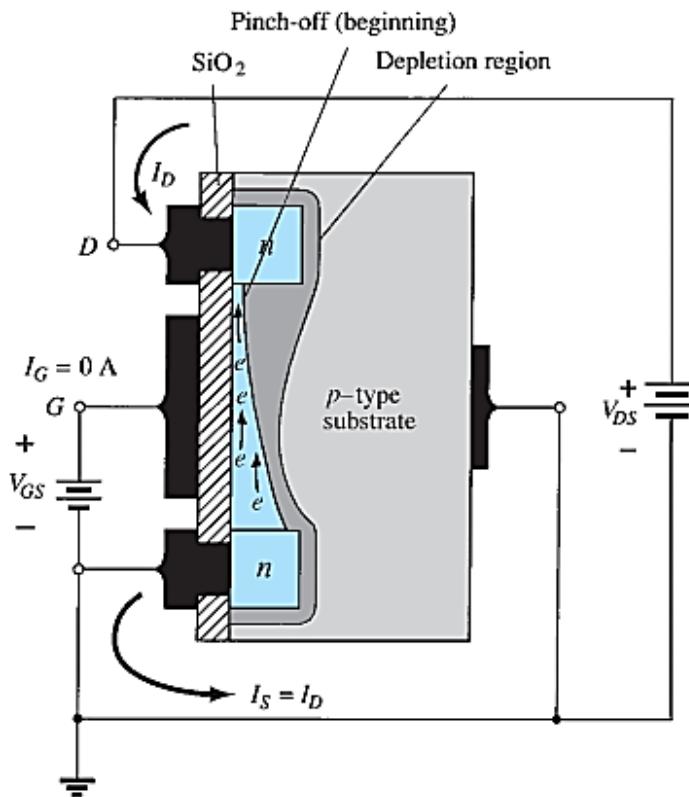
**FIG. 6.33**  
Channel formation in the n-channel enhancement-type MOSFET.

## CONTINUED...

- As  $V_{GS}$  is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current.
- However, if we hold  $V_{GS}$  constant and increase the level of  $V_{DS}$ , the drain current will eventually reach a saturation level. The levelling off of  $I_D$  is due to a pinching-off process depicted by the narrower channel at the drain end of the induced channel.
- By applying KVL we get – 
$$V_{DG} = V_{DS} - V_{GS}$$
- If  $V_{GS}$  is held fixed at some value such as 8 V and  $V_{DS}$  is increased from 2 to 5V, the voltage will drop from -6 to -3 V. This reduction in gate-to-drain voltage will in turn reduce the attractive forces for free carriers (electrons) in this region of the induced channel, causing a reduction in the effective channel width.
- Eventually, the channel will be reduced to the point of pinch-off and a saturation condition will be established.



## CONTINUED...



**FIG. 6.34**

*Change in channel and depletion region with increasing level of  $V_{DS}$  for a fixed value of  $V_{GS}$ .*

# BASIC OPERATION

- The Enhancement-type MOSFET only operates in the enhancement mode.

- $V_{GS}$  is always positive.**
- As  $V_{GS}$  increases,  $I_D$  increases.**
- But if  $V_{GS}$  is kept constant and  $V_{DS}$  is increased, then  $I_D$  saturates ( $I_{DSS}$ ).**
- The saturation level,  $V_{DSSat}$  is reached.**

$$V_{DSSat} = V_{GS} - V_T$$

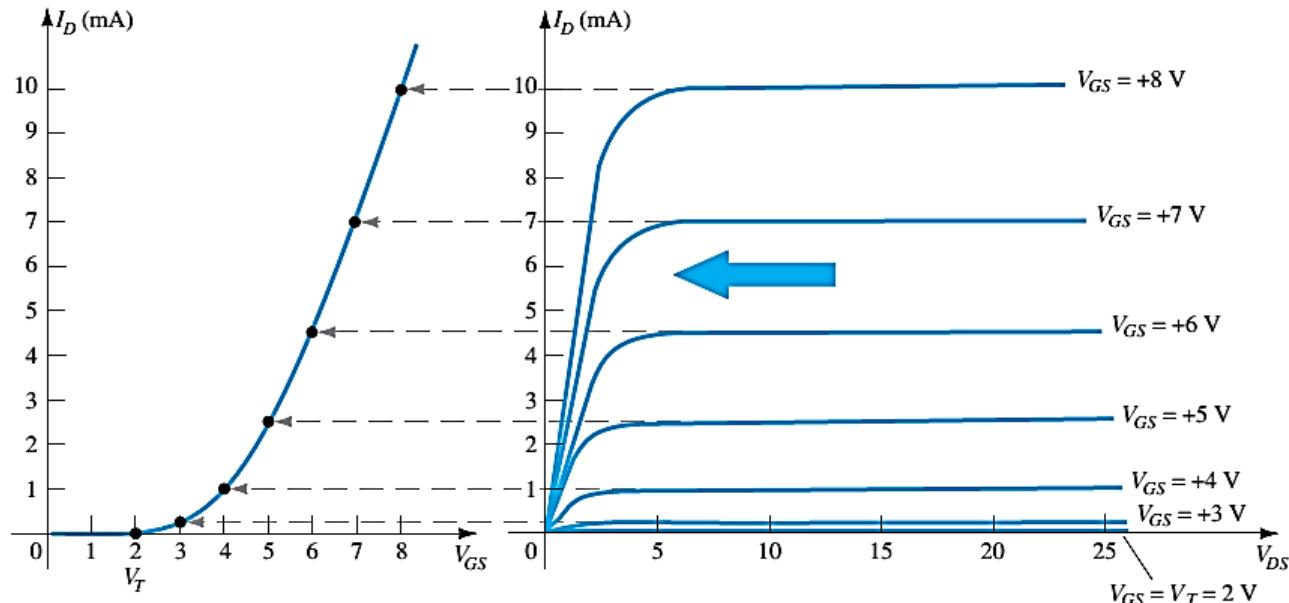


FIG. 6.36

Sketching the transfer characteristics for an n-channel enhancement-type MOSFET from the drain characteristics.

Check this: <http://www-g.eng.cam.ac.uk/mmg/teaching/linearcircuits/jfet.html>

# End of Lecture-4

# TRANSFER CURVE

- To determine  $I_D$  given  $V_{GS}$ :

$$I_D = k(V_{GS} - V_T)^2$$

- where  $V_T$  = threshold voltage or voltage at which the MOSFET turns on.
- $k$  = constant found in the specification sheet
- $k$  can also be determined by using values at a specific point and the formula:

$$k = \frac{I_{D(on)}}{(V_{GS(ON)} - V_T)^2}$$

- $V_{DSsat}$  can also be calculated:

$$V_{DSsat} = V_{GS} - V_T$$

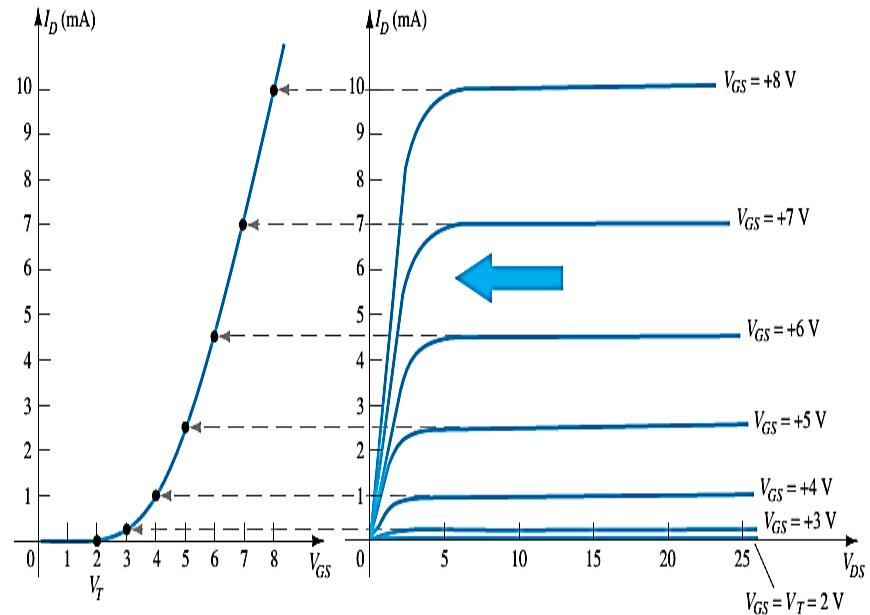
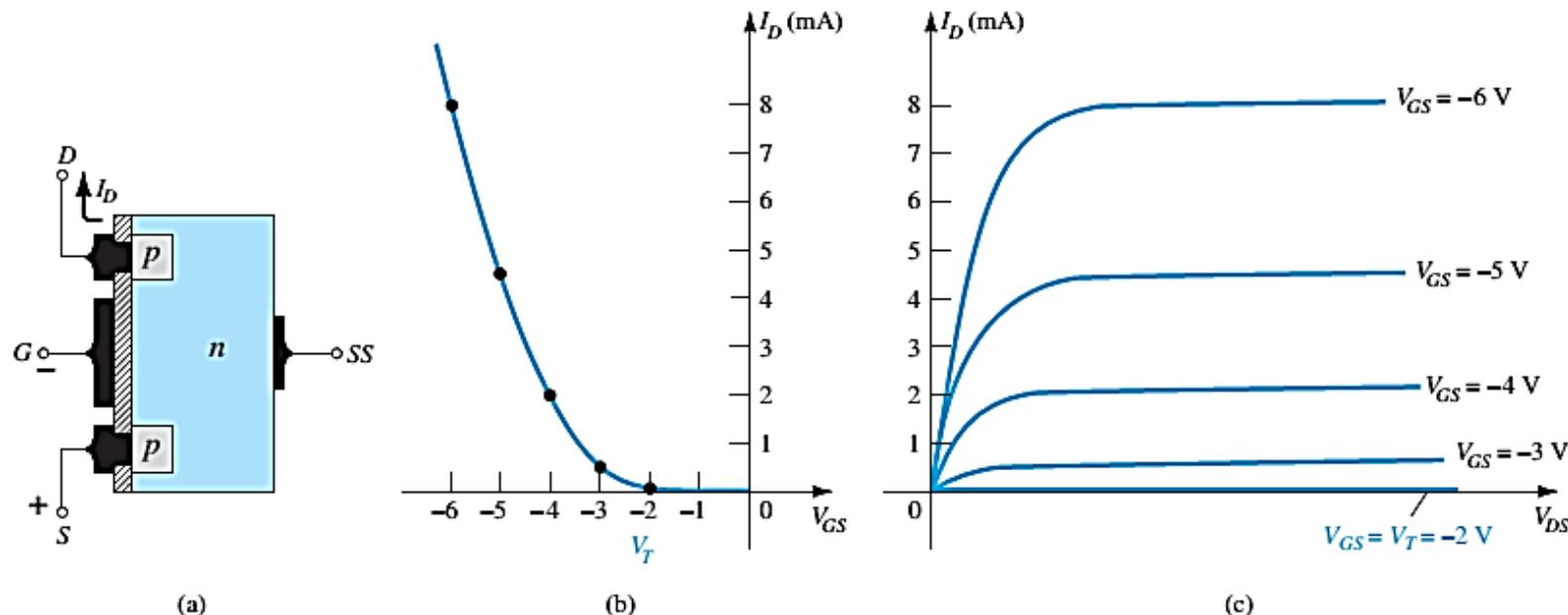


FIG. 6.36

Sketching the transfer characteristics for an n-channel enhancement-type MOSFET from the drain characteristics.

## P -CHANNEL ENHANCEMENT-TYPE MOSFETS

- The p-channel Enhancement-type MOSFET is similar to the n-channel except that the voltage polarities and current directions are reversed.

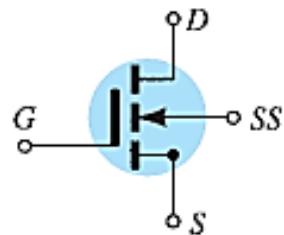


**FIG. 6.38**

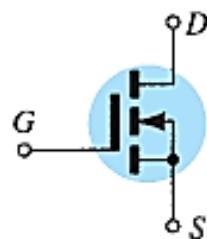
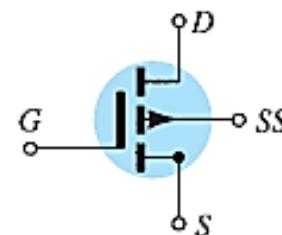
*p-Channel enhancement-type MOSFET with  $V_T = 2$  V and  $k = 0.5 \times 10^{-3}$  A/V<sup>2</sup>.*

# SYMBOLS

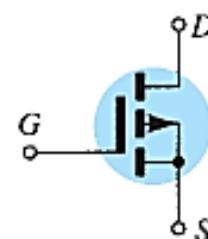
*n*-channel



*p*-channel



(a)



(b)

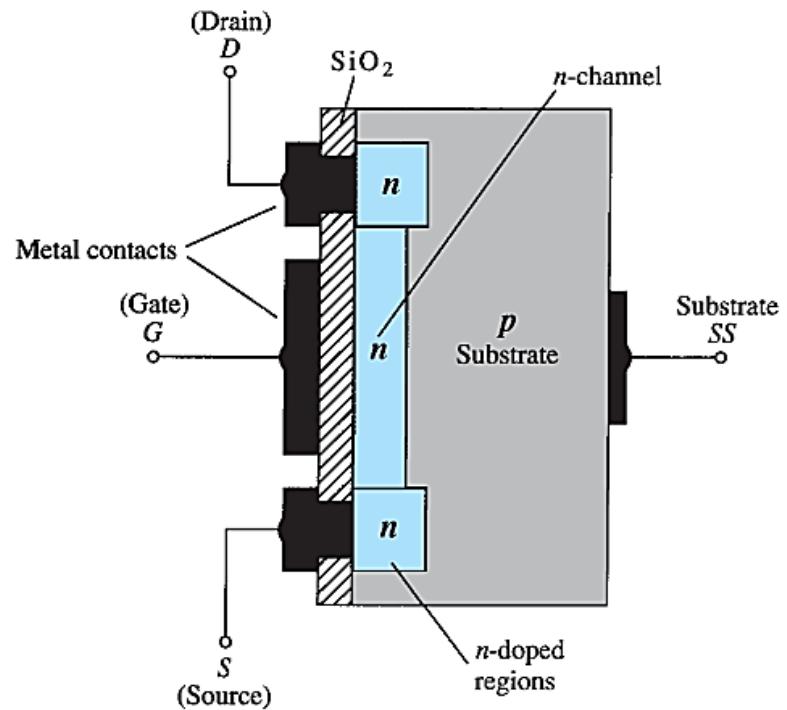
**FIG. 6.39**

*Symbols for: (a) n-channel enhancement-type MOSFETs and (b) p-channel enhancement-type MOSFETs.*



# DEPLETION-TYPE MOSFET CONSTRUCTION

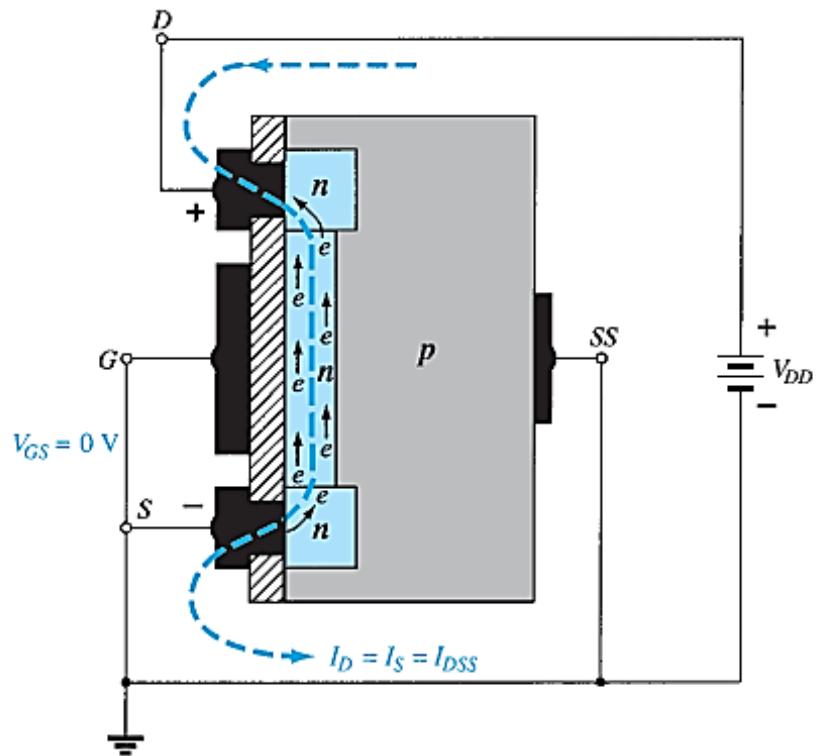
- The Drain (D) and Source (S) connect to the n-doped regions.
- These N-doped regions are connected via an n-channel. This n-channel is connected to the Gate (G) via a thin insulating layer of SiO<sub>2</sub>.
- The n-doped material lies on a p-doped substrate that may have an additional terminal connection called SS.



**FIG. 6.24**  
*n-Channel depletion-type MOSFET.*

# BASIC OPERATION

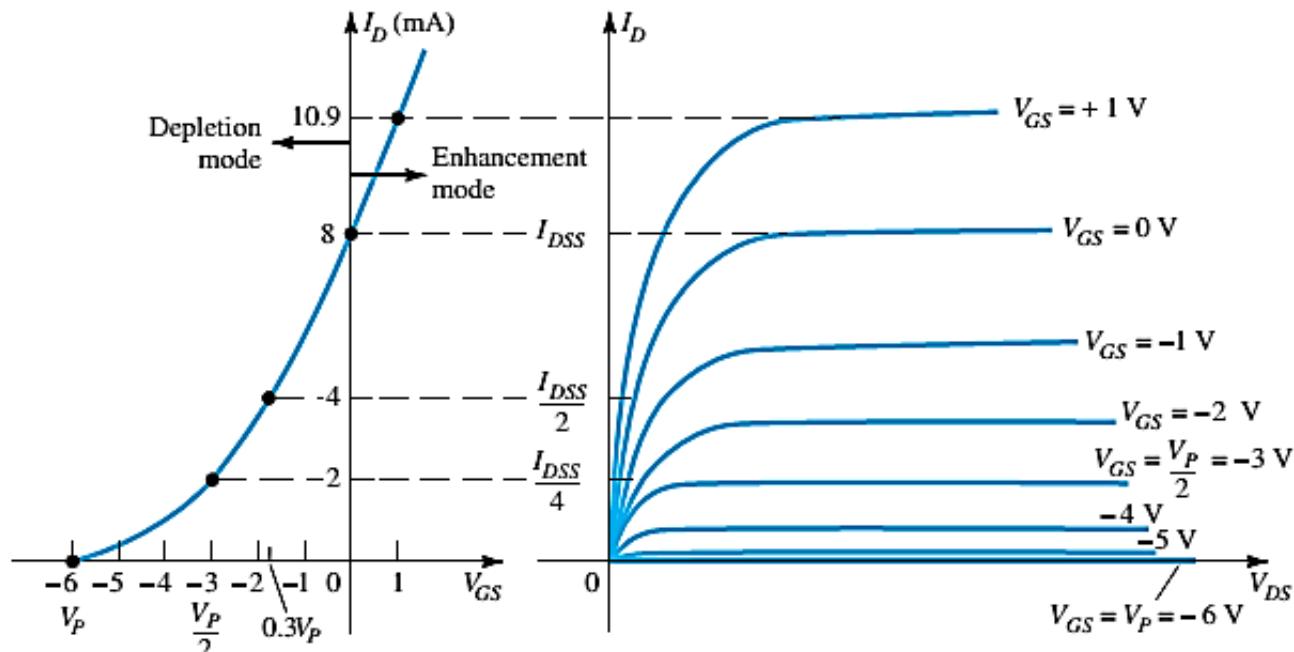
- In Fig. 6.25 the gate-to-source voltage is set to 0 V by the direct connection from one terminal to the other, and a voltage  $V_{DD}$  is applied across the drain-to-source terminals.
- The result is an attraction of the free electrons of the n-channel for the positive voltage at the drain.
- The result is a current similar to that flowing in the channel of the JFET. In fact, the resulting current with  $V_{GS} = 0$  V continues to be labeled  $I_{DSS}$ .



**FIG. 6.25**  
n-Channel depletion-type MOSFET with  $V_{GS} = 0$  V and applied voltage  $V_{DD}$ .

# BASIC OPERATION

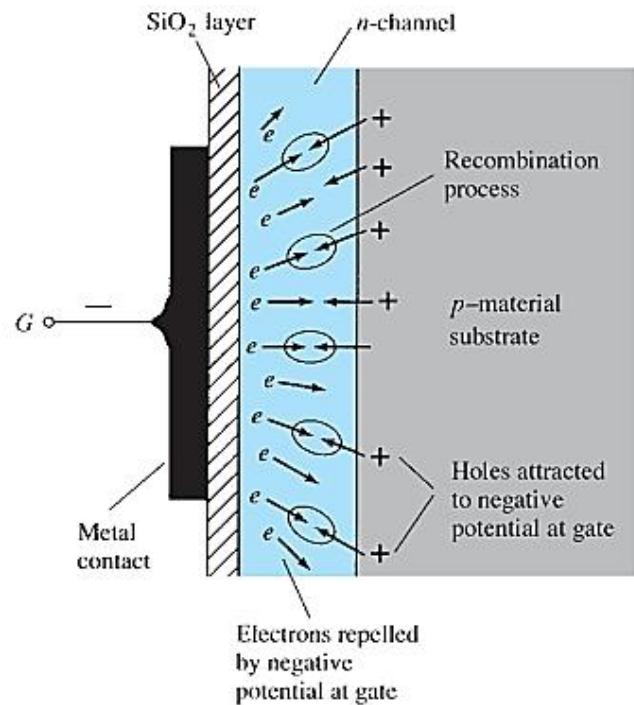
- A Depletion MOSFET can operate in two modes: Depletion or Enhancement mode.



**FIG. 6.26**  
Drain and transfer characteristics for an n-channel depletion-type MOSFET.

# BASIC OPERATION CONTD.

- In this figure  $V_{GS}$  has been set at a negative voltage such as 1 V. The negative potential at the gate will tend to pressure electrons toward the p-type substrate (like charges repel) and attract holes from the p-type substrate (opposite charges attract).
- Depending on the magnitude of the negative bias established by  $V_{GS}$ , a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the n-channel available for conduction. The more negative the bias, the higher the rate of recombination.
- The resulting level of drain current is therefore reduced with increasing negative bias for  $V_{GS}$  for  $V_{GS} = 1$  V, 2 V, and so on, to the pinch-off level of 6 V. The resulting levels of drain current and the plotting of the transfer curve proceeds exactly as described for the JFET.



**FIG. 6.27**  
Reduction in free carriers in a channel due to a negative potential at the gate terminal.

# DEPLETION-TYPE MOSFET IN *DEPLETION MODE*

- **Depletion mode:**

- The characteristics are similar to the JFET.
- When  $V_{GS} = 0V$ ,  $I_D = I_{DSS}$
- When  $V_{GS} < 0V$ ,  $I_D < I_{DSS}$
- The formula used to plot the Transfer Curve still applies:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

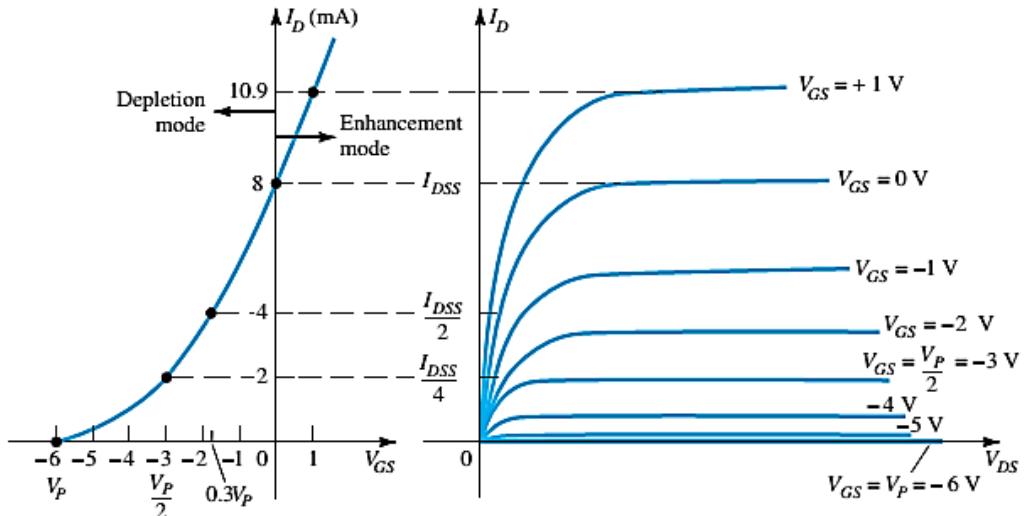


FIG. 6.26

Drain and transfer characteristics for an n-channel depletion-type MOSFET.

# ENHANCEMENT MODE

- For positive values of  $V_{GS}$ , the positive gate will draw additional electrons (free carriers) from the p-type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles.
- As the gate-to-source voltage continues to increase in the positive direction, the drain current will increase at a rapid rate.
- The application of a positive gate-to-source voltage has “enhanced” the level of free carriers in the channel compared to that encountered with  $V_{GS} = 0$  V. For this reason the region of positive gate voltages on the drain or transfer characteristics is often referred to as the enhancement region,
- The region between cutoff and the saturation level of  $I_{DSS}$  referred to as the depletion region.

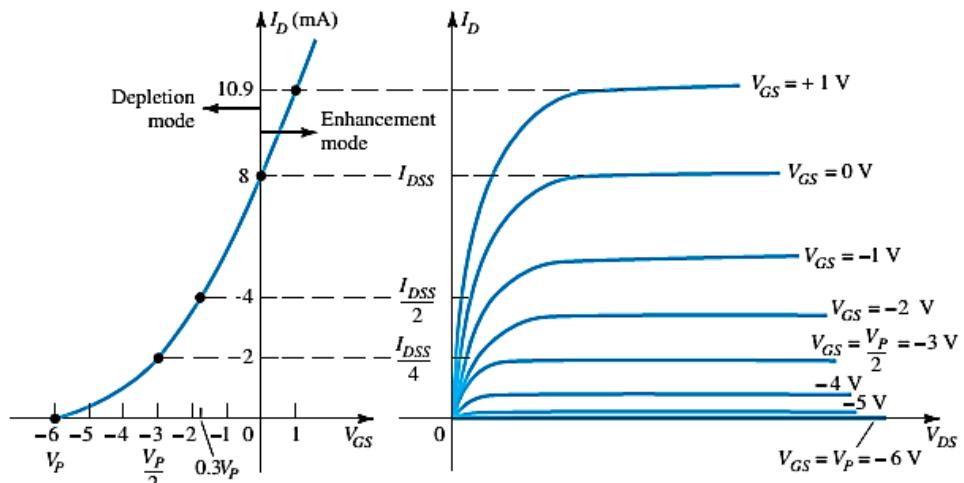


# DEPLETION-TYPE MOSFET IN ENHANCEMENT MODE

- Enhancement mode:

- $V_{GS} > 0V$ ,  $I_D$  increases above  $I_{DSS}$ .
- The formula used to plot the Transfer Curve still applies:  
(note that  $V_{GS}$  is now a positive polarity)

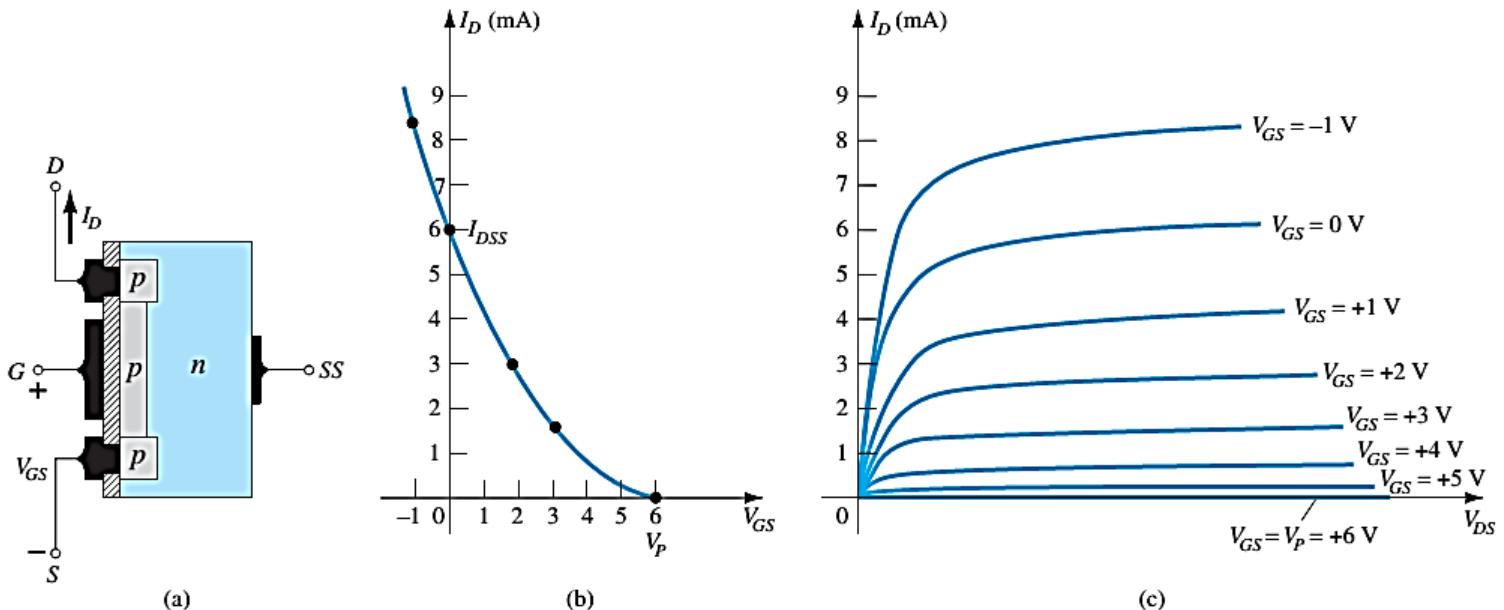
$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$



**FIG. 6.26**  
Drain and transfer characteristics for an n-channel depletion-type MOSFET.

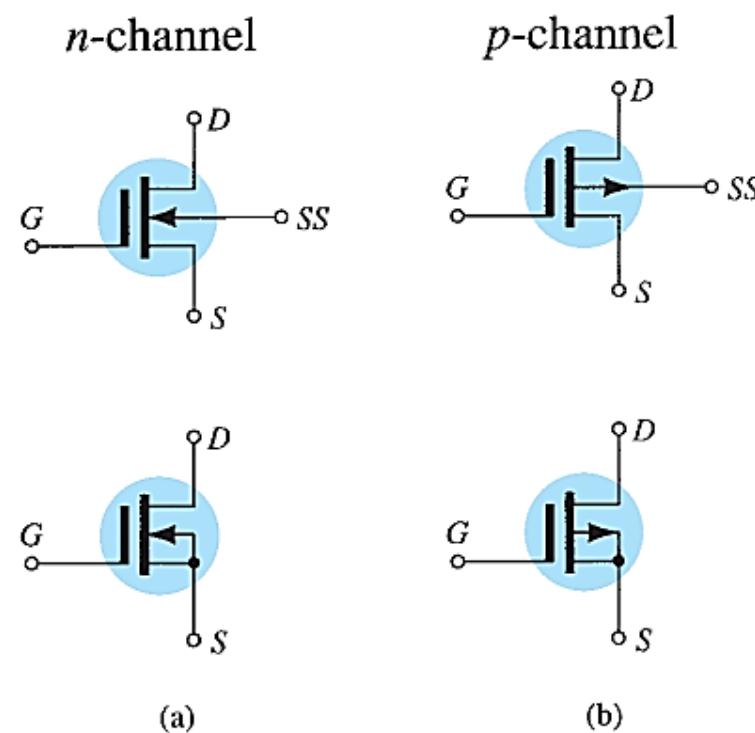
# P-CHANNEL DEPLETION-TYPE MOSFET

- The p-channel Depletion-type MOSFET is similar to the n-channel except that the voltage polarities and current directions are reversed.



**FIG. 6.29**  
p-Channel depletion-type MOSFET with  $I_{DSS} = 6$  mA and  $V_P = +6$  V.

# SYMBOLS

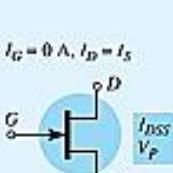
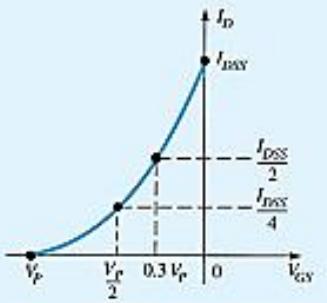
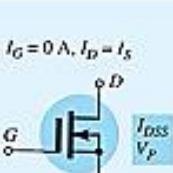
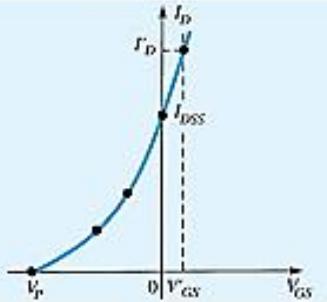
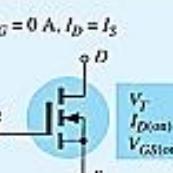
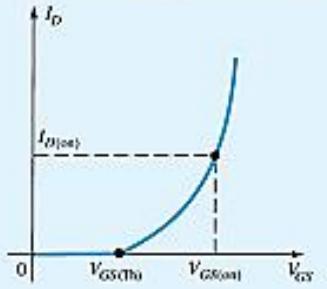


**FIG. 6.30**

*Graphic symbols for: (a) n-channel depletion-type MOSFETs and (b) p-channel depletion-type MOSFETs.*

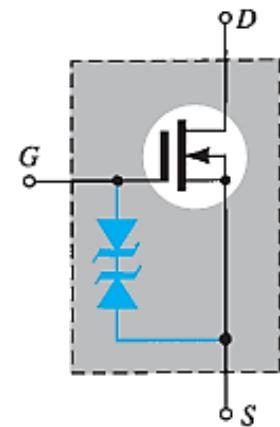


# SUMMARY TABLE

<b>JFET (n-channel)</b>	 $I_G = 0 \text{ A}, I_D = I_S$ $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$	
<b>MOSFET depletion type (n-channel)</b>	 $I_G = 0 \text{ A}, I_D = I_S$ $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$	
<b>MOSFET enhancement type (n-channel)</b>	 $I_G = 0 \text{ A}, I_D = I_S$ $I_D = k (V_{GS} - V_{GSOE})^2$ $k = \frac{I_{Dmax}}{(V_{GSOE} - V_{GSOmin})^2}$	

# MOSFET HANDLING

- MOSFETs are **very static sensitive**. Because of the very thin SiO<sub>2</sub> layer between the external terminals and the layers of the device, any small electrical discharge can establish an unwanted conduction.
- Protection:
  - Always transport in a static sensitive bag.
  - Always wear a static strap when handling MOSFETS.
  - Apply voltage limiting devices between the Gate and Source, such as back-to-back Zeners to limit any transient voltage.

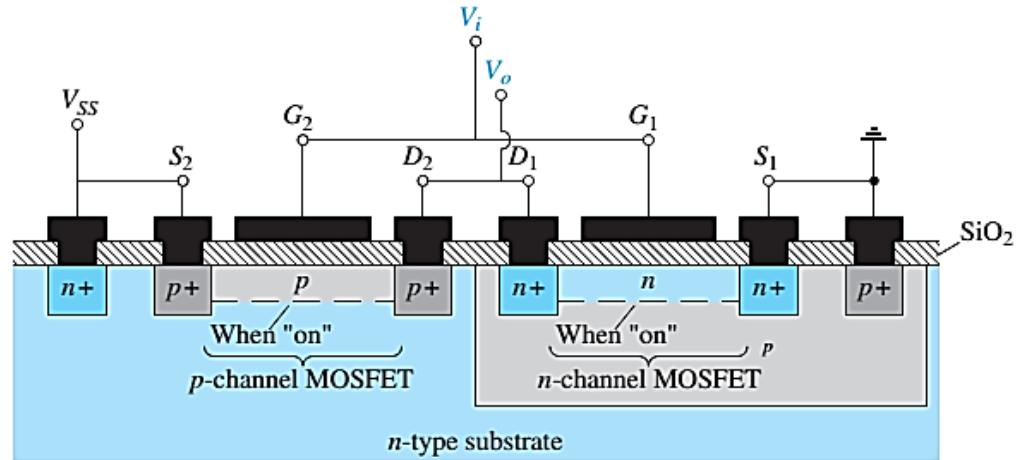


**FIG. 6.42**  
Zener-protected MOSFET.



# CMOS

- CMOS – Complementary MOSFET p-channel and n-channel MOSFET on the same substrate.
- Advantage:
  - Useful in logic circuit designs
  - Higher input impedance
  - Faster switching speeds
  - Lower operating power levels
- Application:
  - CMOS Inverter

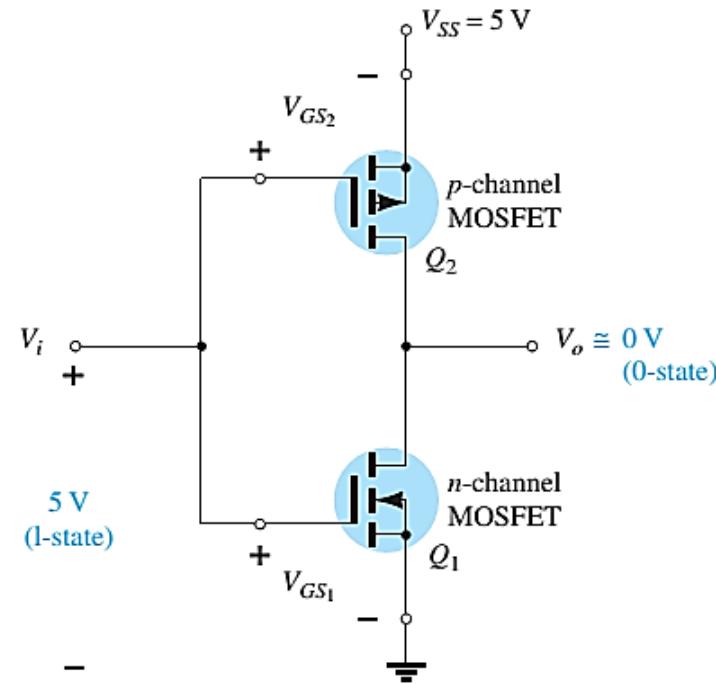


**FIG. 6.44**

*CMOS with the connections indicated in Fig. 6.45.*

# CMOS INVERTER

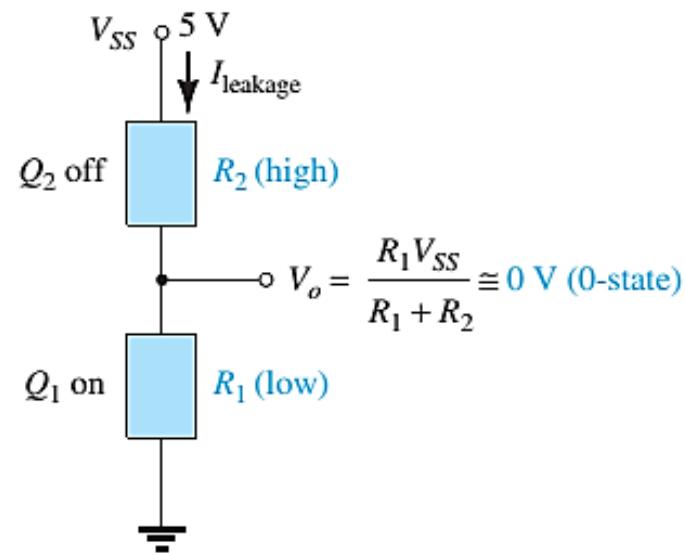
- An inverter is a logic element that “inverts” the applied signal. That is, if the logic levels of operation are 0V (0-state) and 5V (1-state), an input level of 0V will result in an output level of 5V, and vice versa.
- Here, **both gates are connected to the applied signal** and **both drain to the output  $V_o$** . The **source of the p-channel MOSFET ( $Q_2$ ) is connected directly to the applied voltage  $V_{SS}$** , while the **source of the n-channel MOSFET ( $Q_1$ ) is connected to ground**.
- Here, the application of 5V at the input should result in approximately 0 V at the output. **With 5V at  $V_i$**  (with respect to ground),  $V_{GS1} = V_i$  and  $Q_1$  is “on,” resulting in a relatively **low resistance between drain and source**.
- Since  $V_i$  and  $V_{SS}$  are at 5 V,  $V_{GS2} = 0$  V, which is **less than the required  $V_T$**  for the device, resulting in an “off” state. The resulting resistance level between drain and source is **quite high for  $Q_2$** .



**FIG. 6.45**  
CMOS inverter.

# CMOS INVERTER

- A simple application of the voltage-divider rule will reveal that  $V_o$  is very close to 0 V or the 0-state, establishing the desired inversion process.
- For an applied voltage  $V_i$  of 0V (0-state),  $V_{GS1} = 0V$  and  $Q_1$  will be off with  $V_{SS2} = -5V$ , turning on the p-channel MOSFET. The result is that  $Q_2$  will present a small resistance level,  $Q_1$  a high resistance, and  $V_o = V_{SS} = 5V$  (the 1-state).



**FIG. 6.46**

Relative resistance levels for  $V_i = 5\text{ V}$  (1-state).



# End of Lecture-5

# OBJECTIVES

- Be able to perform a dc analysis of JFET, MOSFET, and MESFET networks.
- Become proficient in the use of load-line analysis to examine FET networks.
- Develop confidence in the dc analysis of networks with both FETs and BJTs.
- Understand how to use the Universal JFET Bias Curve to analyze the various FET configurations.



# GENERAL RELATIONSHIPS

- For all FETs:  $I_G \approx 0A$   $I_D = I_S$
- For JFETs and Depletion-Type MOSFETs:  $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$
- For Enhancement-Type MOSFETs:  $I_D = k(V_{GS} - V_T)^2$
- BJT: **Linear Relationship** between  $I_B$  and  $I_C$
- FET: **Non-linear Relationship** between  $V_{GS}$  and  $I_D$ .



# COMMON FET BIASING CIRCUITS

- JFET
  - Fixed – Bias
  - Self-Bias
  - Voltage-Divider Bias
- Depletion-Type MOSFET
  - Self-Bias
  - Voltage-Divider Bias
- Enhancement-Type MOSFET
  - Feedback Configuration
  - Voltage-Divider Bias



# FIXED-BIAS JFET

- The simplest biasing arrangements:

$$I_G \approx 0A$$

$$I_D = I_S$$

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

- For the DC analysis,
  - Capacitors are open circuits

$$I_G \approx 0A \quad V_{RG} = I_G R_G = (0A)R_G = 0V$$

- The **zero-volt drop across  $R_G$**  permits **replacing  $R_G$  by a short-circuit.**

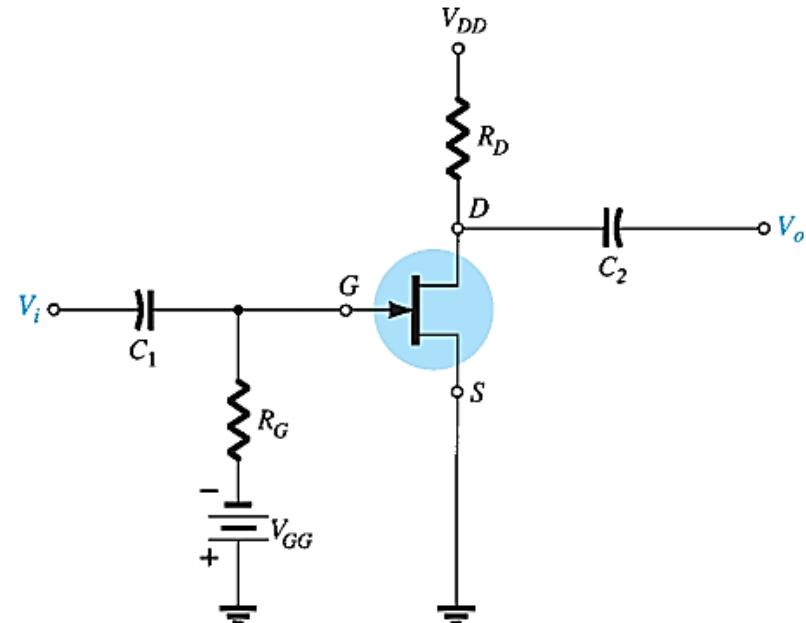
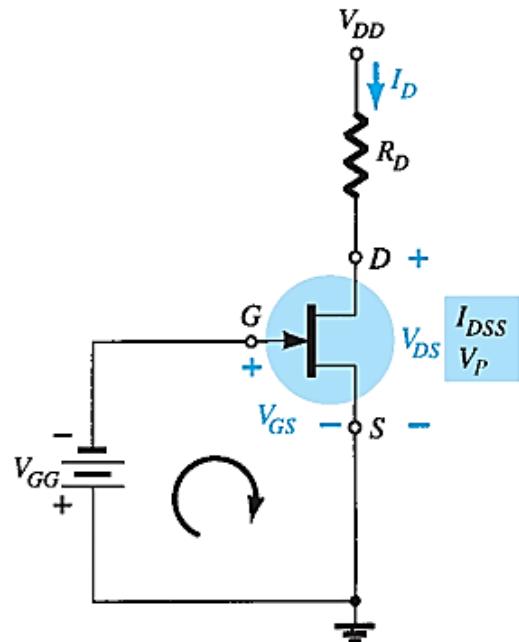


FIG. 7.1

Fixed-bias configuration.

# FIXED-BIAS JFET

- Can be solved using either Mathematical Approach or Graphical Approach:



**FIG. 7.2**  
Network for dc analysis.

## Mathematical Approach

$$V_{GS} = -V_{GG}$$

$$V_{DS} = V_{DD} - I_D R_D$$

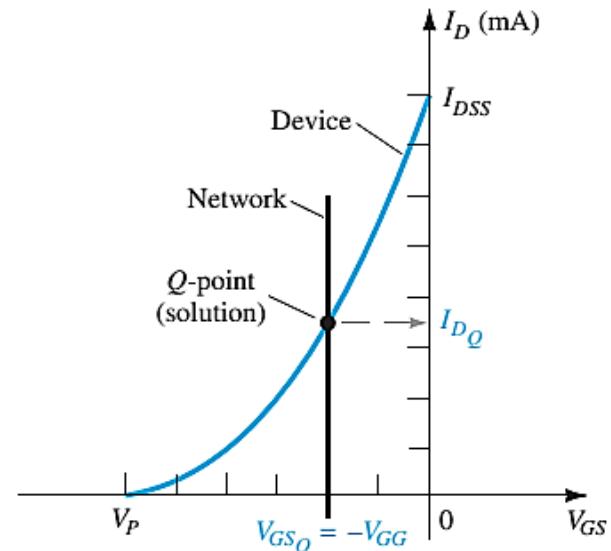
$$V_S = 0$$

$$V_D = V_{DS}$$

$$V_G = V_{GS}$$

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

## Graphical Approach



**FIG. 7.4**  
Finding the solution for the fixed-bias configuration.

# FIXED-BIAS JFET EXAMPLE

- Determine  $V_{GSQ}$ ,  $I_{DQ}$ ,  $V_{DS}$ ,  $V_D$ ,  $V_G$ ,  $V_S$ .

## Mathematical Approach

a.  $V_{GSQ} = -V_{GG} = -2 \text{ V}$

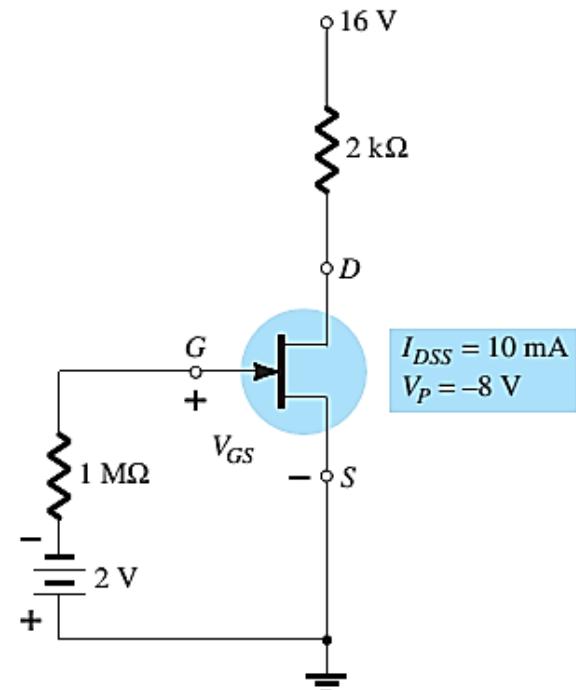
b.  $I_{DQ} = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10 \text{ mA} \left(1 - \frac{-2 \text{ V}}{-8 \text{ V}}\right)^2$   
 $= 10 \text{ mA}(1 - 0.25)^2 = 10 \text{ mA}(0.75)^2 = 10 \text{ mA}(0.5625)$   
**5.625 mA**

c.  $V_{DS} = V_{DD} - I_D R_D = 16 \text{ V} - (5.625 \text{ mA})(2 \text{ k}\Omega)$   
 $= 16 \text{ V} - 11.25 \text{ V} = 4.75 \text{ V}$

d.  $V_D = V_{DS} = 4.75 \text{ V}$

e.  $V_G = V_{GS} = -2 \text{ V}$

f.  $V_S = 0 \text{ V}$



**FIG. 7.6**  
Example 7.1.

# FIXED-BIAS JFET EXAMPLE

## Graphical Approach

$$V_{GSQ} = -V_{GG} = -2 \text{ V}$$

$$I_{DQ} = 5.6 \text{ mA}$$

$$\begin{aligned} V_{DS} &= V_{DD} - I_D R_D = 16 \text{ V} - (5.6 \text{ mA})(2 \text{ k}\Omega) \\ &= 16 \text{ V} - 11.2 \text{ V} = 4.8 \text{ V} \end{aligned}$$

$$V_D = V_{DS} = 4.8 \text{ V}$$

$$V_G = V_{GS} = -2 \text{ V}$$

$$V_S = 0 \text{ V}$$

$V_{GS}$	$I_D$
0	$I_{DSS}$
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
$V_P$	0mA

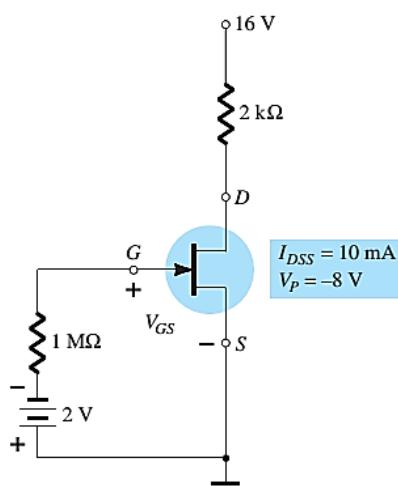


FIG. 7.6  
Example 7.1.

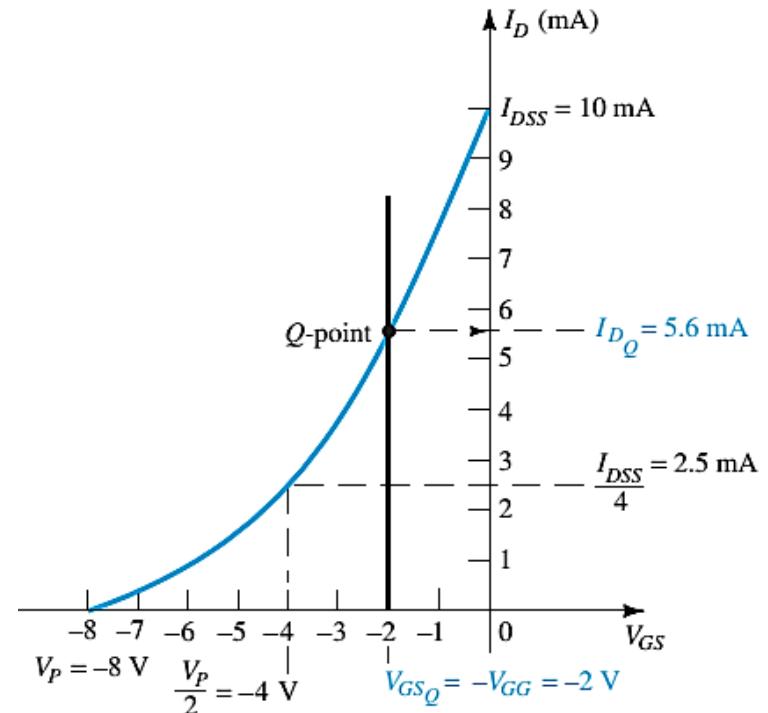


FIG. 7.7

Graphical solution for the network of Fig. 7.6.

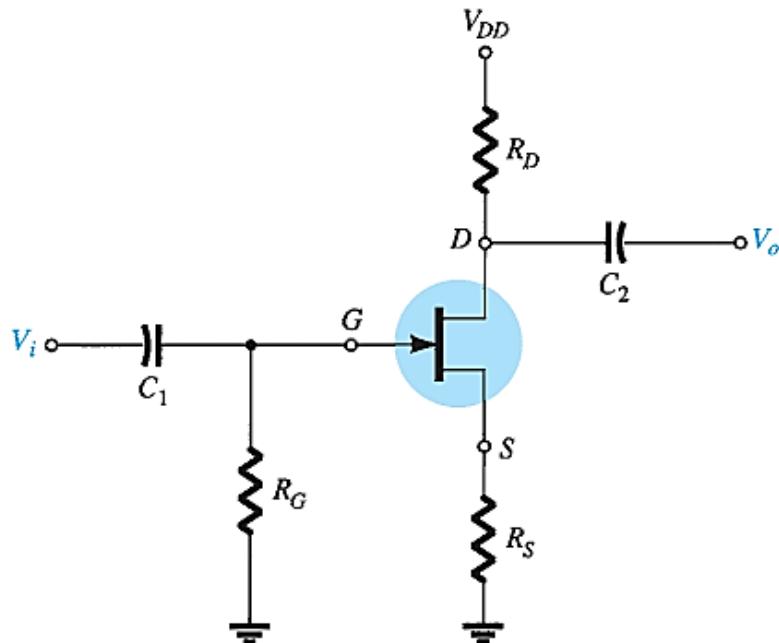
# JFET: SELF-BIAS CONFIGURATION

- The self-bias configuration **eliminates the need for two dc supplies.**

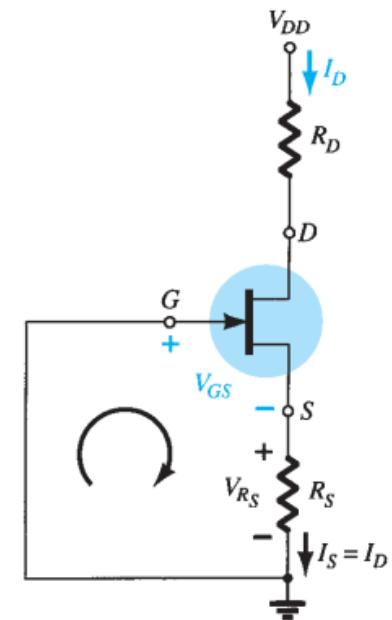
$$I_G \approx 0A$$

$$I_D = I_S$$

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$



**FIG. 7.8**  
JFET self-bias configuration.



**FIG. 7.9**  
DC analysis of the self-bias configuration.

# SELF-BIAS CONFIGURATION

- Can be solved using either Mathematical Approach or Graphical Approach:

## Mathematical Approach

$$V_{GS} = -I_D R_S$$

$$V_{DS} = V_{DD} - I_D (R_S + R_D)$$

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

$$I_D = I_{DSS} \left( 1 + \frac{I_D R_S}{V_P} \right)^2$$

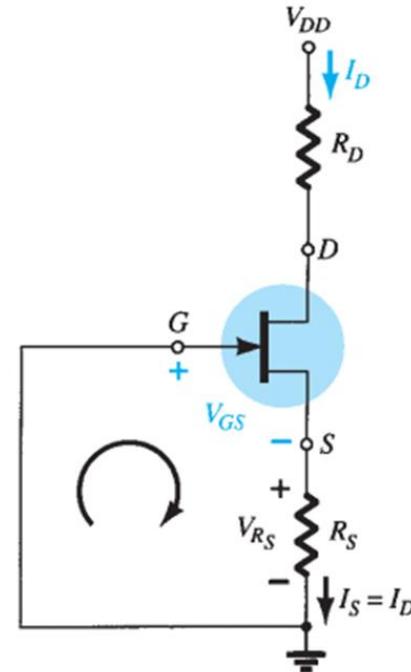


FIG. 7.9

DC analysis of the self-bias configuration.



# SELF-BIAS CONFIGURATION

## Graphical Approach

- Draw the device transfer characteristic using shorthand method.
- Draw the network load line
  - Use  $V_{GS} = -I_D R_S$  to draw straight line.
  - First point,  $I_D = 0, V_{GS} = 0$
  - Second point, any point from  $I_D = 0$  to  $I_D = I_{DSS}$ . Choose

$$I_D = \frac{I_{DSS}}{2} \text{ then}$$

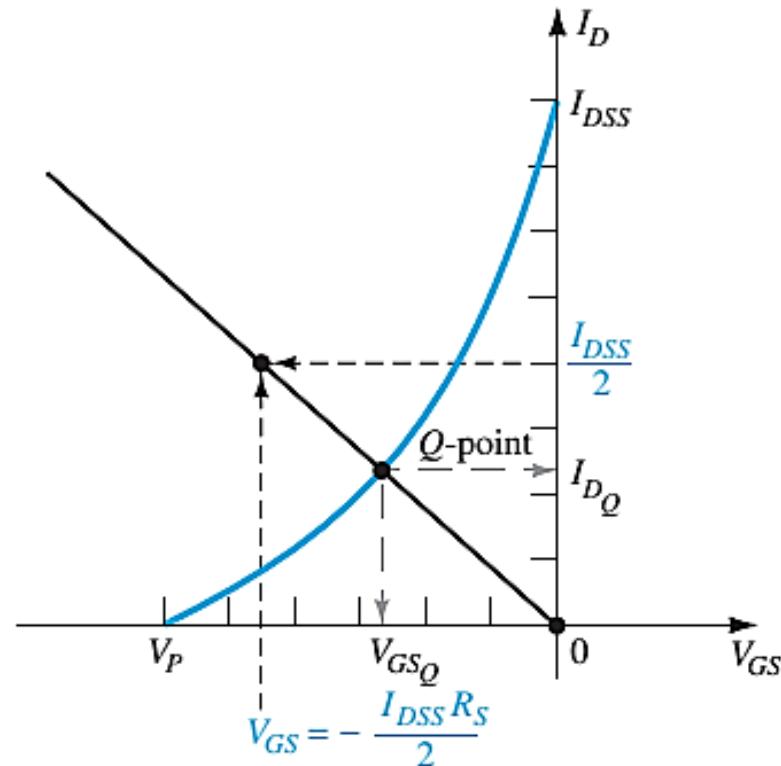
$$V_{GS} = -\frac{I_{DSS} R_S}{2}$$

- The Q-point obtained at the intersection of the straight line plot and the device characteristic curve.
- The quiescent value for  $I_D$  and  $V_{GS}$  can then be determined and used to find the other quantities of interest.



# SELF-BIAS CONFIGURATION

## Graphical Approach



**FIG. 7.11**  
Sketching the self-bias line.



# SELF-BIAS EXAMPLE

- Determine  $V_{GSQ}$ ,  $I_{DQ}$ ,  $V_{DS}$ ,  $V_S$ ,  $V_G$  and  $V_D$ .

$$V_{GS} = -I_D R_S$$

$$V_{DS} = V_{DD} - I_D (R_S + R_D)$$

$$V_{GSQ} = -2.6 \text{ V}$$

$$\begin{aligned} V_{DS} &= V_{DD} - I_D(R_S + R_D) \\ &= 20 \text{ V} - (2.6 \text{ mA})(1 \text{ k}\Omega + 3.3 \text{ k}\Omega) \end{aligned}$$

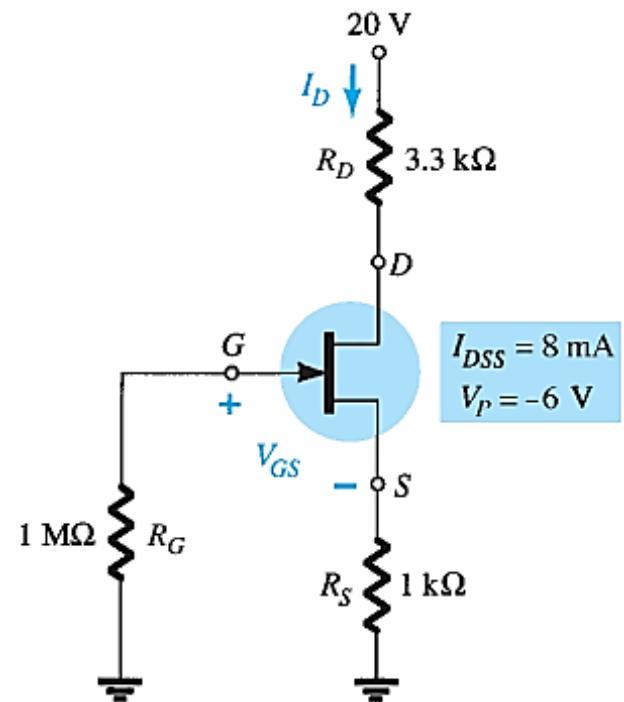
$$V_S = I_D R_S$$

$$\begin{aligned} &= (2.6 \text{ mA})(1 \text{ k}\Omega) \\ &= 2.6 \text{ V} \end{aligned}$$

$$V_G = 0 \text{ V}$$

$$V_D = V_{DS} + V_S = 8.82 \text{ V} + 2.6 \text{ V} = 11.42 \text{ V}$$

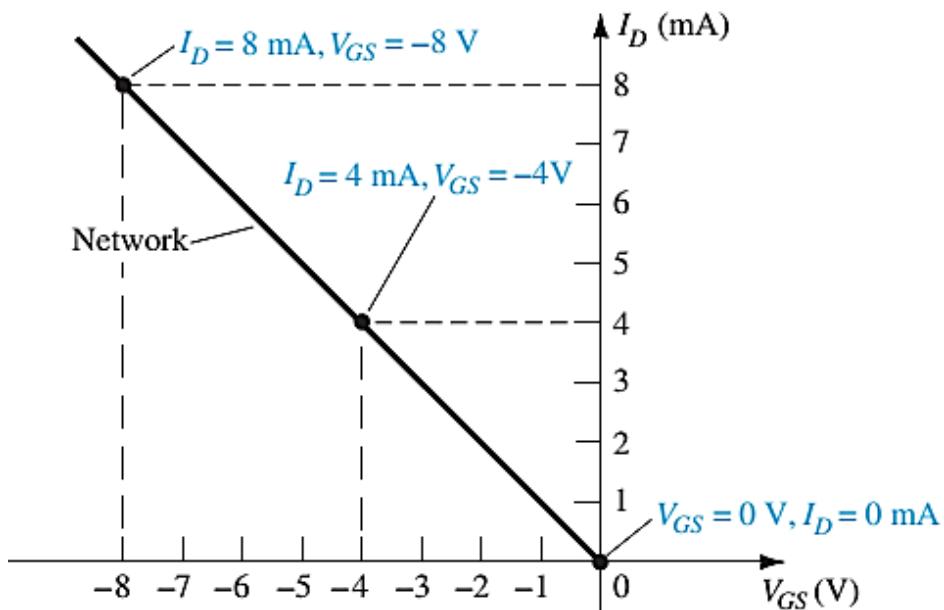
$$V_D = V_{DD} - I_D R_D = 20 \text{ V} - (2.6 \text{ mA})(3.3 \text{ k}\Omega) = 11.42 \text{ V}$$



**FIG. 7.12**  
Example 7.2.

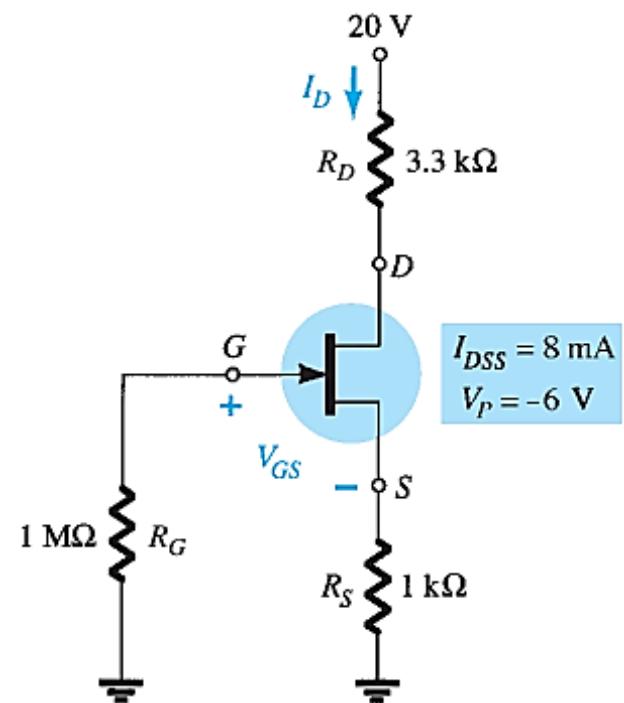
# SELF-BIAS EXAMPLE Contd.

- Plot  $I_D$  vs  $V_{GS}$  and draw a line from the origin of the axis.



**FIG. 7.13**

Sketching the self-bias line for the network of Fig. 7.12.



**FIG. 7.12**

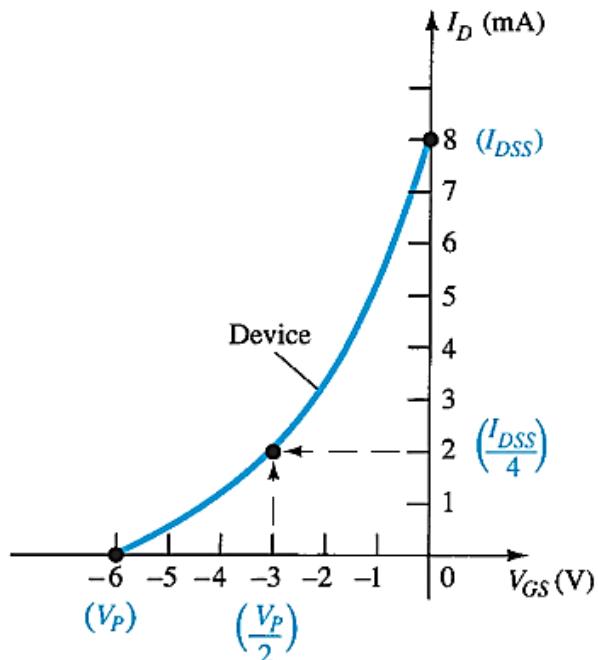
Example 7.2.

# End of Lecture-6

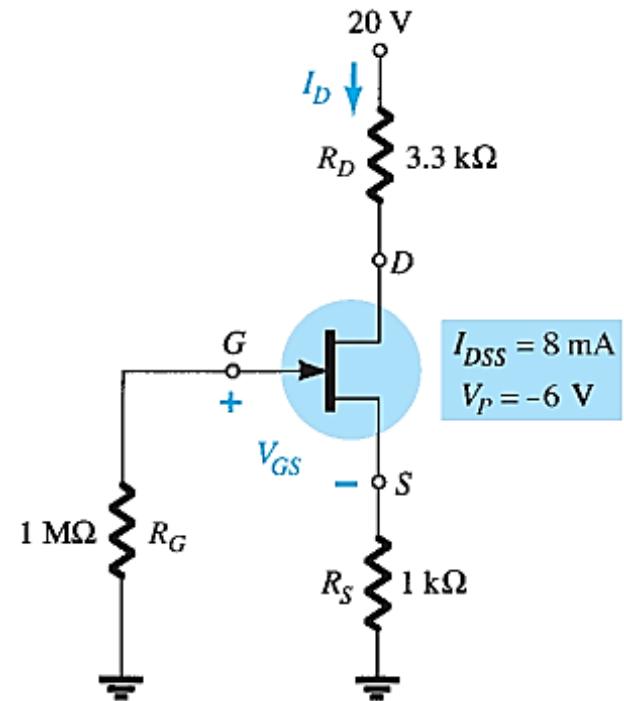
# SELF-BIAS EXAMPLE Contd.

- Plot the transfer curve using  $I_{DSS}$  and  $V_P$  using shorthand method:

$V_{GS}$	$I_D$
0	$I_{DSS}$
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
$V_P$	0mA



**FIG. 7.14**  
Sketching the device characteristics for the JFET of Fig. 7.12.



**FIG. 7.12**  
Example 7.2.

# SELF-BIAS EXAMPLE Contd.

- Superimpose the load line on top of the transfer curve:

$$V_{GSQ} = -2.6 \text{ V}$$

$$I_{DQ} = 2.6 \text{ mA}$$

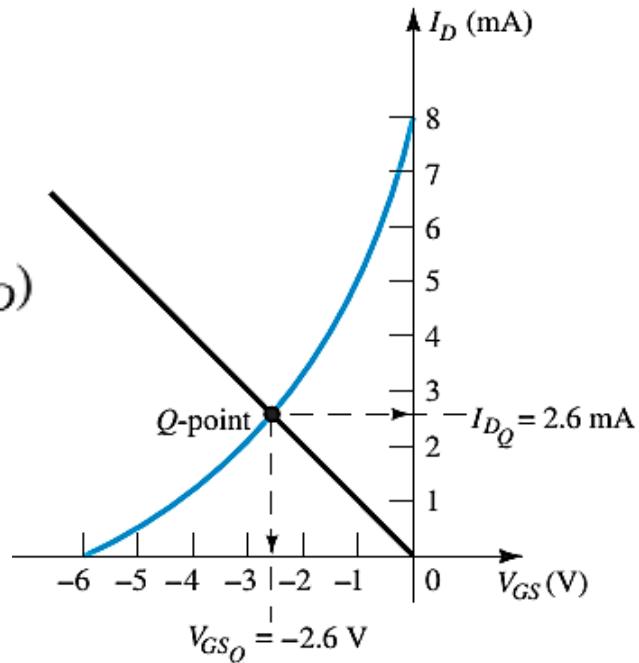
$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

$$V_S = I_D R_S$$

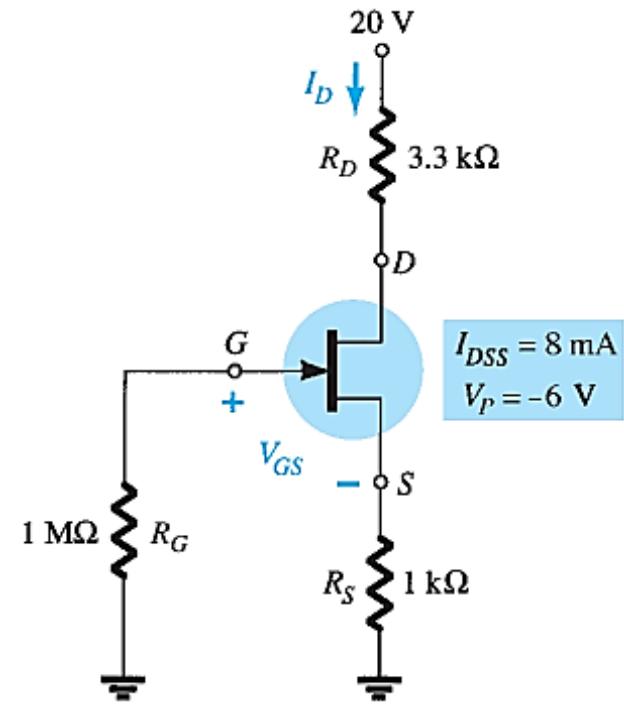
$$V_G = 0 \text{ V}$$

$$V_D = V_{DS} + V_S$$

$$V_D = V_{DD} - I_D R_D$$



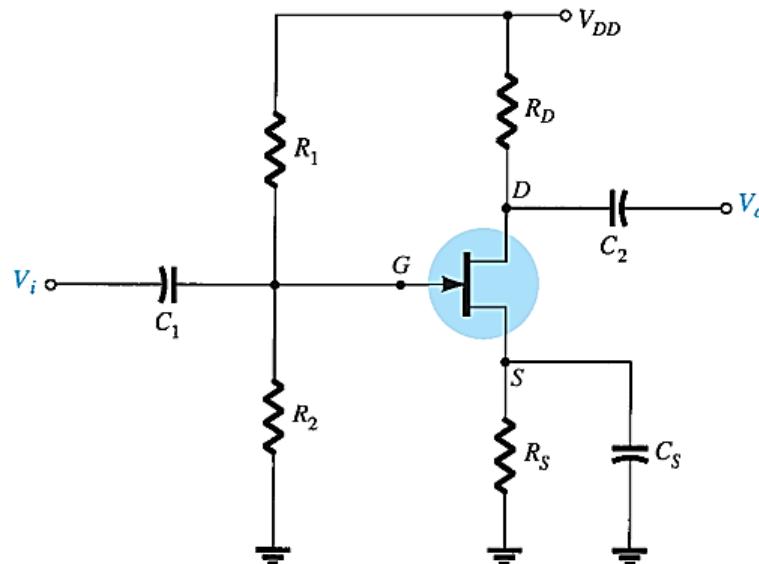
**FIG. 7.15**  
Determining the *Q*-point for the network of Fig. 7.12.



**FIG. 7.12**  
Example 7.2.

# JFET: VOLTAGE-DIVIDER BIAS

- The source  $V_{DD}$  was separated into two equivalent sources to permit a further separation of the input and output regions of the network.
- Since  $I_G = 0A$ , Kirchoff's current law requires that  $I_{R1} = I_{R2}$  and the series equivalent circuit appearing to the left of the figure can be used to find the level of  $V_G$ .



**FIG. 7.17**  
Voltage-divider bias arrangement.

# VOLTAGE-DIVIDER BIAS

- $V_G$  can be found using the voltage divider rule:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

- Using Kirchoff's Law on the input loop:

$$V_D = V_{DD} - I_D R_D$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

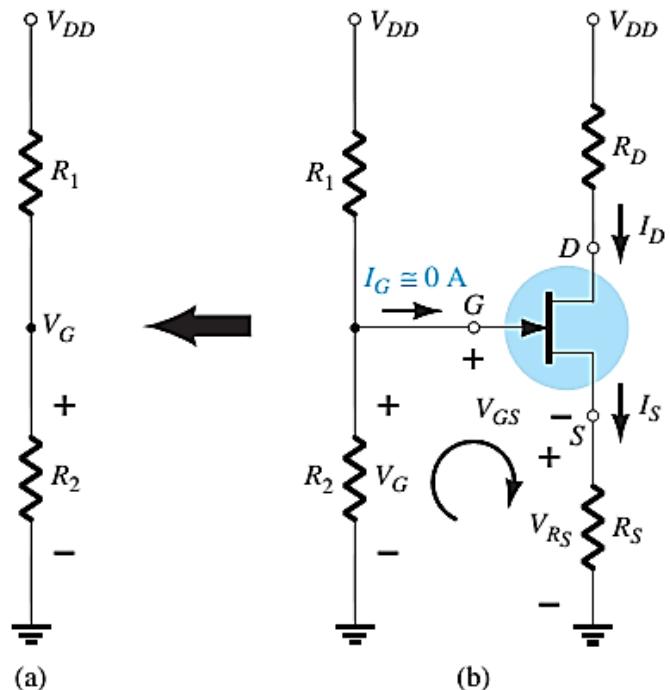
$$V_S = I_D R_S$$

$$V_{GS} = V_G - I_D R_S$$

- Rearranging and using  $I_D = I_S$ :

$$I_{R1} = I_{R2} = \frac{V_{DD}}{R_1 + R_2}$$

- Again the Q point needs to be established by plotting a line that intersects the transfer curve.



**FIG. 7.18**

Redrawn network of Fig. 7.17 for dc analysis.

# VOLTAGE-DIVIDER BIAS

- Graphical Approach (to find  $V_{GSQ}$  and  $I_{DQ}$ ):

- Plot a line for:

»  $V_{GS} = V_G$  when  $I_D = 0A$

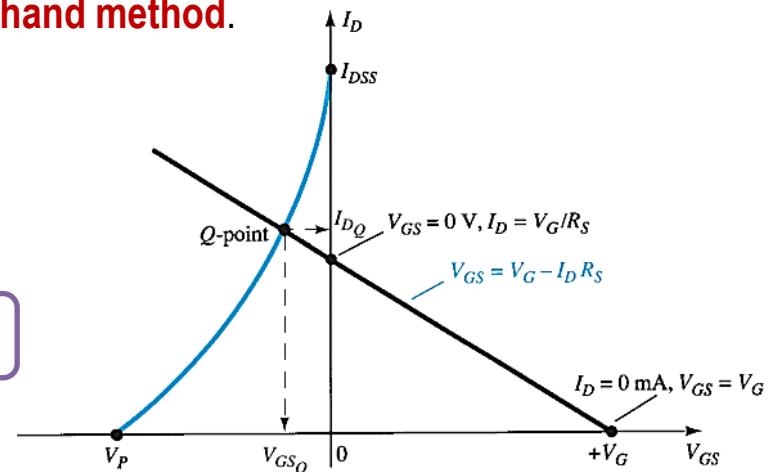
»  $V_{GS} = 0V$  when  $I_D = V_G/R_S$ .

- Plot the transfer curve using  $I_{DSS}$  and  $V_P$  using shorthand method.

- The Q-point is located at the intersection.

$V_{GS}$	$I_D$
0	$I_{DSS}$
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
$V_P$	0mA

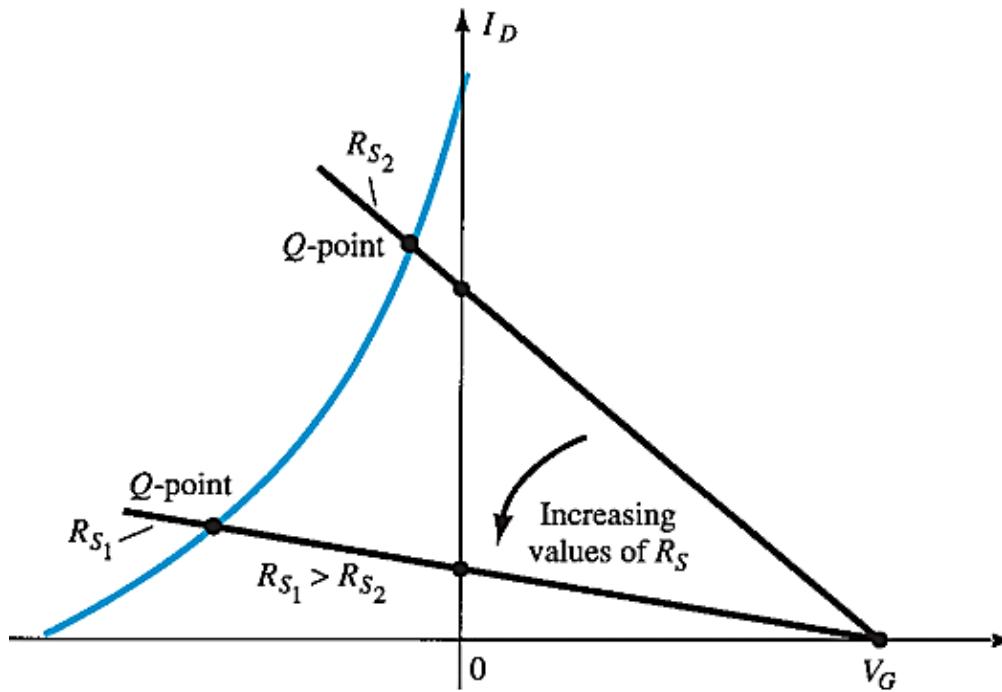
$$V_{GS} = V_G - I_D R_S$$



**FIG. 7.19**

Sketching the network equation for the voltage-divider configuration.

# EFFECT OF INCREASING VALUES OF $R_S$



**FIG. 7.20**  
Effect of  $R_S$  on the resulting Q-point.



# JFET: VOLTAGE-DIVIDER BIAS EXAMPLE

- Determine  $I_{DQ}$ ,  $V_{GSQ}$ ,  $V_D$ ,  $V_S$ ,  $V_{DS}$  and  $V_{DG}$ .

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_{GS} = V_G - I_D R_S$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

$$V_{GSQ} = -1.8V$$

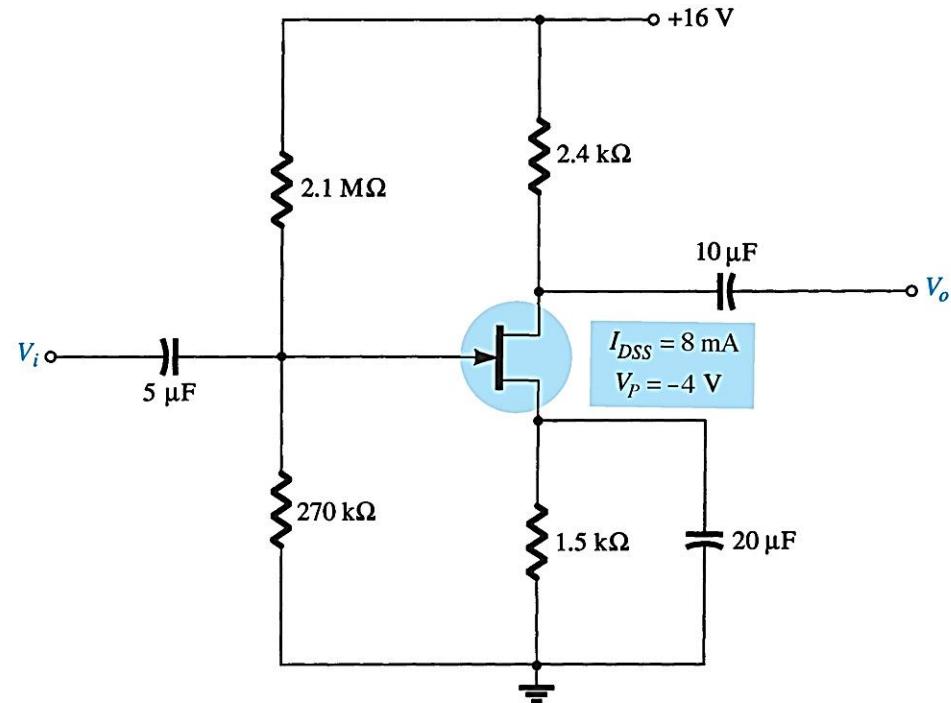
$$I_{DQ} = 2.4mA$$

$$V_D = 10.24V$$

$$V_S = 3.6V$$

$$V_{DS} = 6.64V$$

$$V_{DG} = 8.24V$$



# VOLTAGE-DIVIDER BIAS EXAMPLE Contd.

- Graphical Approach ( to find  $V_{GSQ}$  and  $I_{DQ}$ ):

- Plot a line for:

»  $V_{GS} = V_G$  when  $I_D = 0A$

»  $V_{GS} = 0V$  when  $I_D = V_G/R_S$ .

- Plot the **transfer curve** using  $I_{DSS}$  and  $V_P$  using **shorthand method**.
- Identify the Q-point.

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_S = I_D R_S$$

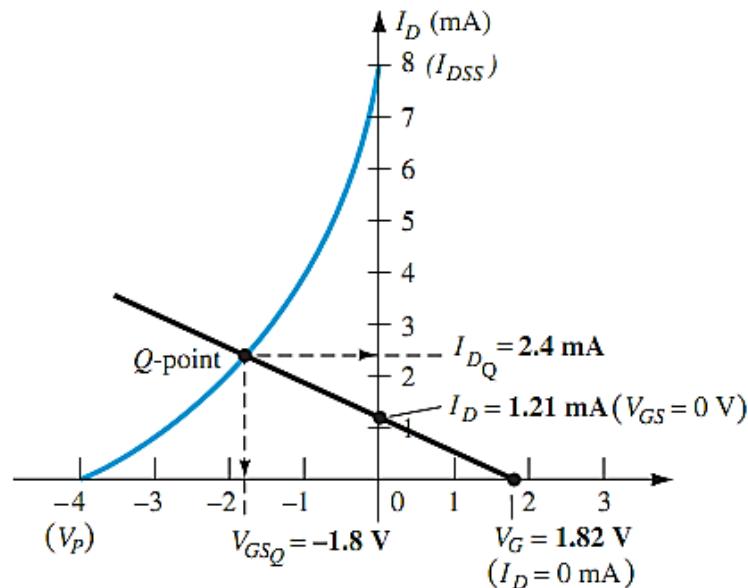
$$V_{GS} = V_G - I_D R_S$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

$$V_{DS} = V_D - V_S$$

$$V_D = V_{DD} - I_D R_D$$

$$V_{DG} = V_D - V_G$$



**FIG. 7.22**

Determining the Q-point for the network of Fig. 7.21.

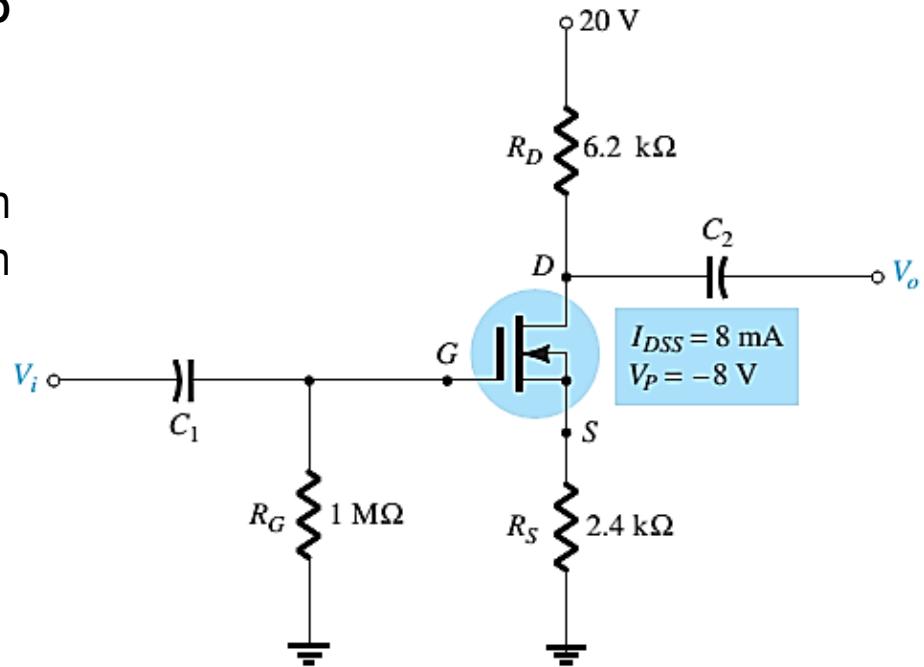
# D-MOSFET SELF-BIAS

- D-MOSFET bias circuits are **similar** to JFETs.
- The only **difference** is that D-MOSFETs can operate with **positive** values of  $V_{GS}$  and with  $I_D$  values that exceed  $I_{DSS}$ .

$$I_G \approx 0A$$

$$I_D = I_S$$

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$



**FIG. 7.33**  
Example 7.8.

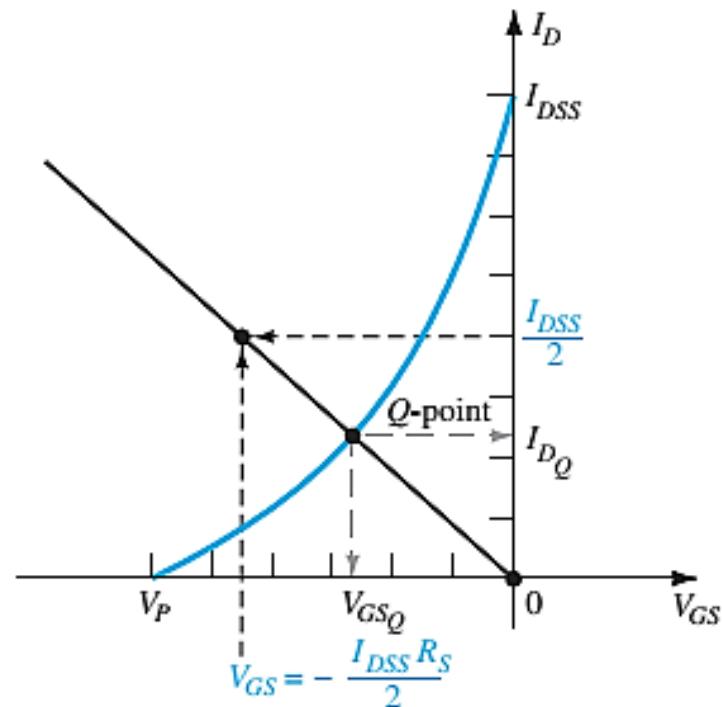
# D-MOSFET SELF-BIAS

- **Graphical Approach** (to find  $V_{GSQ}$  and  $I_{DQ}$ ):

- Plot the *transfer curve* using  $I_{DSS}$  and  $V_P$  using *shorthand method*.
- Plot  $I_D$  vs  $V_{GS}$  using  $V_{GS} = -I_D R_S$ .
- Take a positive value of  $V_{GS}$  and find the  $I_D$  value using

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

- The Q-point is located at the intersection.



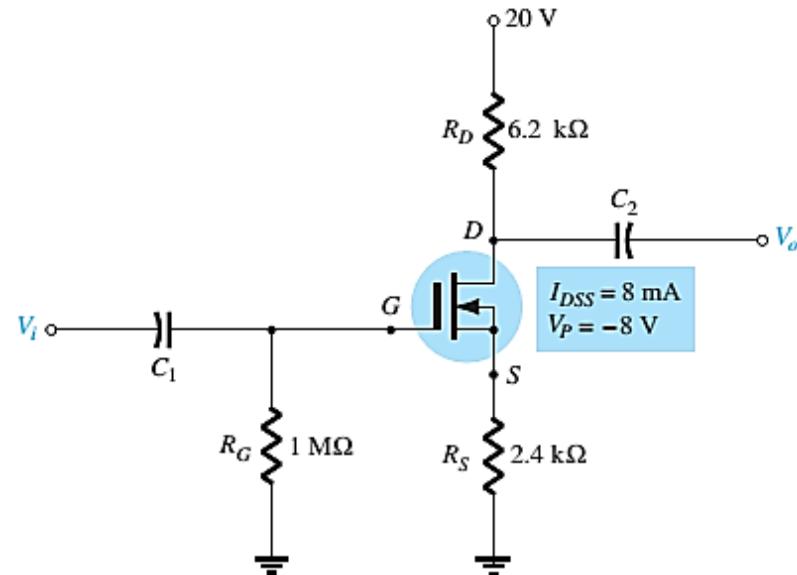
# D-MOSFET SELF-BIAS EXAMPLE

- Determine the  $I_{DQ}$ ,  $V_{GSQ}$  and  $V_D$ .
- **Graphical Approach** (to find  $V_{GSQ}$  and  $I_{DQ}$ ):

- Plot the *transfer curve* using  $I_{DSS}$  and  $V_P$  using *shorthand method*.
- Take a positive value of  $V_{GS}$  and find the  $I_D$  value using

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

- Plot  $I_D$  vs  $V_{GS}$  using  $V_{GS} = -I_D R_S$ .
- Identify the intersection Q-point.



**FIG. 7.33**  
Example 7.8.

# D-MOSFET SELF-BIAS EXAMPLE

$$V_D = V_{DD} - I_D R_D$$

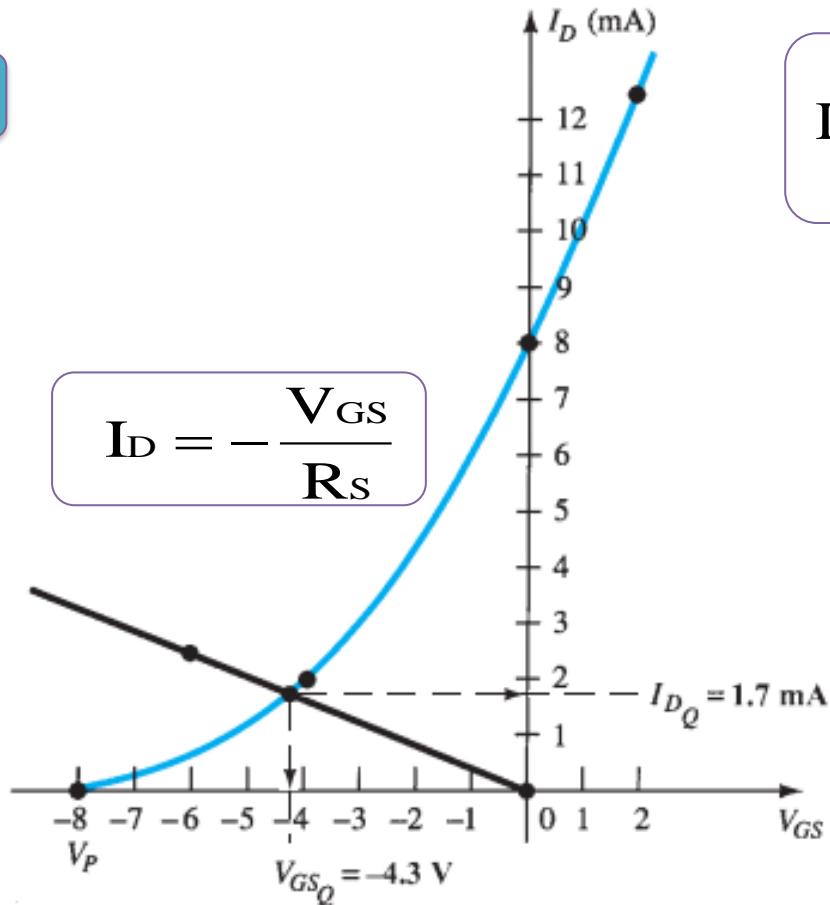
$$V_{GSQ} = -4.3 \text{ V}$$

$$I_{DQ} = 1.7 \text{ mA}$$

$$V_D = 9.46 \text{ V}$$

$$I_D = -\frac{V_{GS}}{R_S}$$

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$



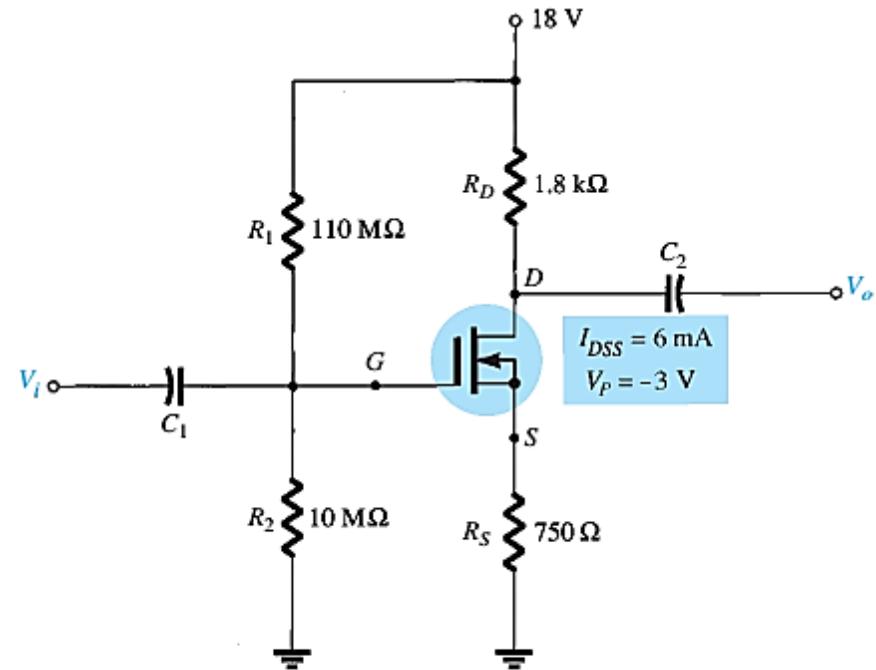
# D-MOSFET VOLTAGE-DIVIDER BIAS

- D-MOSFET bias circuits are similar to **JFETs**.

$$I_G \approx 0A$$

$$I_D = I_S$$

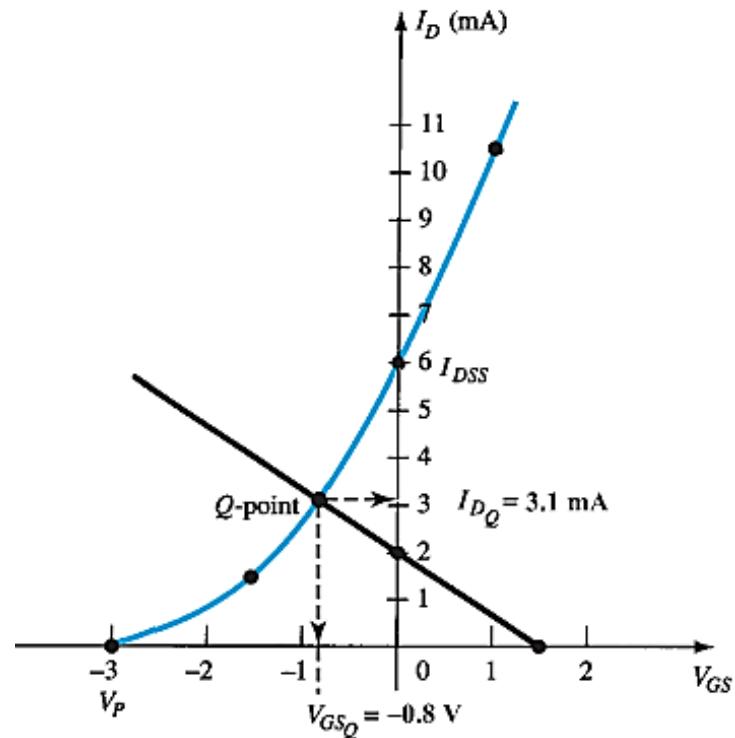
$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$



**FIG. 7.30**  
Example 7.6.

# D-MOSFET VOLTAGE-DIVIDER BIAS

- **Graphical Approach (to find  $V_{GSQ}$  and  $I_{DQ}$ ):**
  - Plot the *transfer curve* using  $I_{DSS}$  and  $V_P$  using *shorthand method*.
  - Take a positive value of  $V_{GS}$  and find the  $I_D$  value using
- Plot  $I_D$  vs  $V_{GS}$  using  $V_{GS} = V_G - I_D R_S$ .
- The Q-point is located at the intersection.



**FIG. 7.31**

Determining the Q-point for the network of Fig. 7.30.

# End of Lecture-7

# E-MOSFET VOLTAGE-DIVIDER BIAS

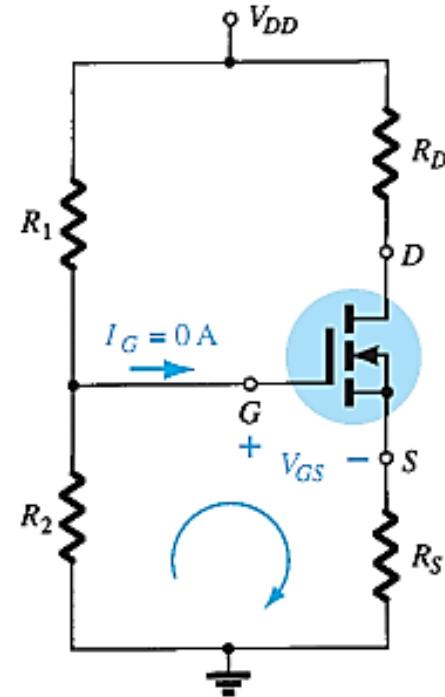
- E-MOSFETs use the **same procedure** to JFETs and D-MOSFETs.

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_{GS} = V_G - I_D R_S$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

$$I_D = k(V_{GS} - V_T)^2$$



**FIG. 7.43**

*Voltage-divider biasing arrangement for an n-channel enhancement MOSFET.*

# E-MOSFET VOLTAGE-DIVIDER BIAS

- **Graphical Approach:**

- Calculate the value for

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$$

- Plot  $V_{GS}$  vs  $I_D$  using

$$I_D = k(V_{GS} - V_T)^2$$

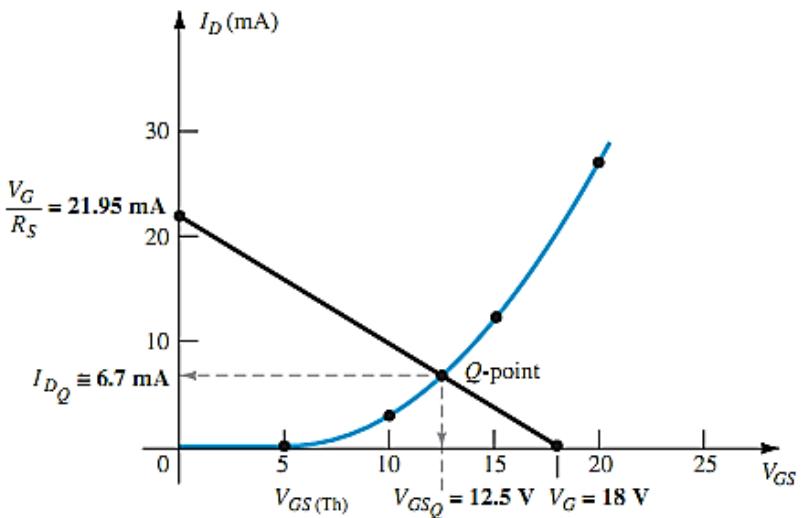
- Plot for:

- »  $V_{GS} = V_G$  at  $I_D = 0A$

- »  $V_{GS} = 0V$  at  $I_D = V_G/R_S$

$$V_{GS} = V_G - I_D R_S$$

- Identify the Q-point.



# E-MOSFET VOLTAGE-DIVIDER BIAS EXAMPLE

- Determine  $I_D$ ,  $V_{GS}$ , and  $V_{DS}$  for the following network:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(18 \text{ M}\Omega)(40 \text{ V})}{22 \text{ M}\Omega + 18 \text{ M}\Omega} = 18 \text{ V}$$

$$V_{GS} = V_G - I_D R_S = 18 \text{ V} - I_D(0.82 \text{ k}\Omega)$$

When  $I_D = 0 \text{ mA}$ ,

$$V_{GS} = 18 \text{ V} - (0 \text{ mA})(0.82 \text{ k}\Omega) = 18 \text{ V}$$

When  $I_D = 0 \text{ mA}$ ,

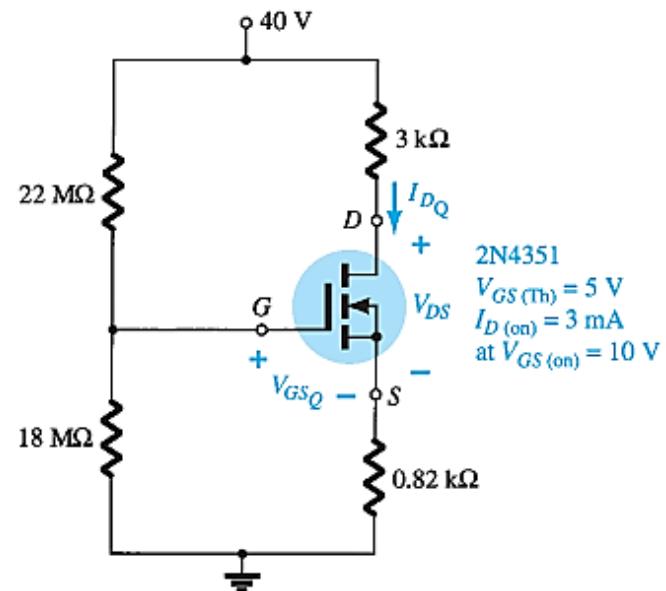
$$V_{GS} = 18 \text{ V} - (0 \text{ mA})(0.82 \text{ k}\Omega) = 18 \text{ V}$$

as appearing on Fig. 7.45. When  $V_{GS} = 0 \text{ V}$ ,

$$V_{GS} = 18 \text{ V} - I_D(0.82 \text{ k}\Omega)$$

$$0 = 18 \text{ V} - I_D(0.82 \text{ k}\Omega)$$

$$I_D = \frac{18 \text{ V}}{0.82 \text{ k}\Omega} = 21.95 \text{ mA}$$



**FIG. 7.44**  
Example 7.11.

# E-MOSFET VOLTAGE-DIVIDER BIAS EXAMPLE

## Device

$$V_{GS(\text{Th})} = 5 \text{ V}, \quad I_{D(\text{on})} = 3 \text{ mA} \text{ with } V_{GS(\text{on})} = 10 \text{ V}$$

$$\begin{aligned}\text{Eq. (7.34): } k &= \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2} \\ &= \frac{3 \text{ mA}}{(10 \text{ V} - 5 \text{ V})^2} = 0.12 \times 10^{-3} \text{ A/V}^2\end{aligned}$$

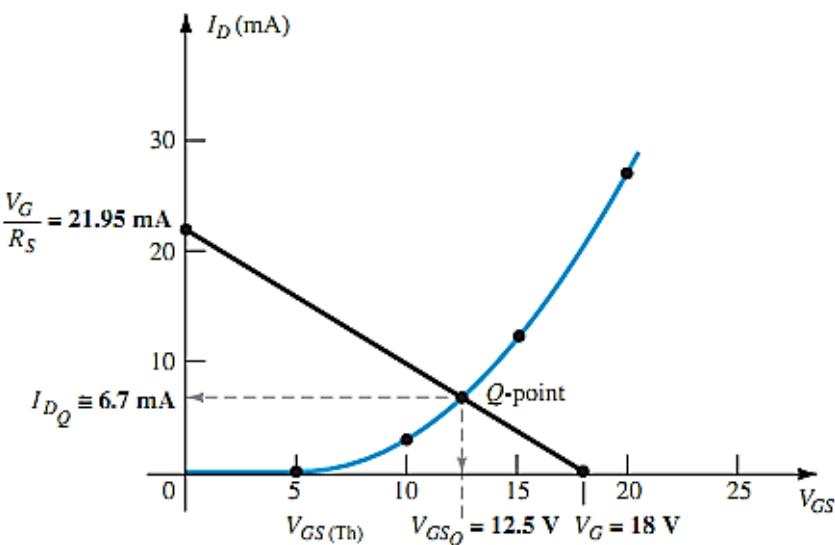
and

$$\begin{aligned}I_D &= k(V_{GS} - V_{GS(\text{Th})})^2 \\ &= 0.12 \times 10^{-3}(V_{GS} - 5)^2\end{aligned}$$

$$I_{D_Q} \cong 6.7 \text{ mA}$$

$$V_{GSQ} = 12.5 \text{ V}$$

$$\begin{aligned}V_{DS} &= V_{DD} - I_D(R_S + R_D) \\ &= 40 \text{ V} - (6.7 \text{ mA})(0.82 \text{ k}\Omega + 3.0 \text{ k}\Omega) \\ &= 40 \text{ V} - 25.6 \text{ V} \\ &= 14.4 \text{ V}\end{aligned}$$



**FIG. 7.45**

Determining the  $Q$ -point for the network of Example 7.11.



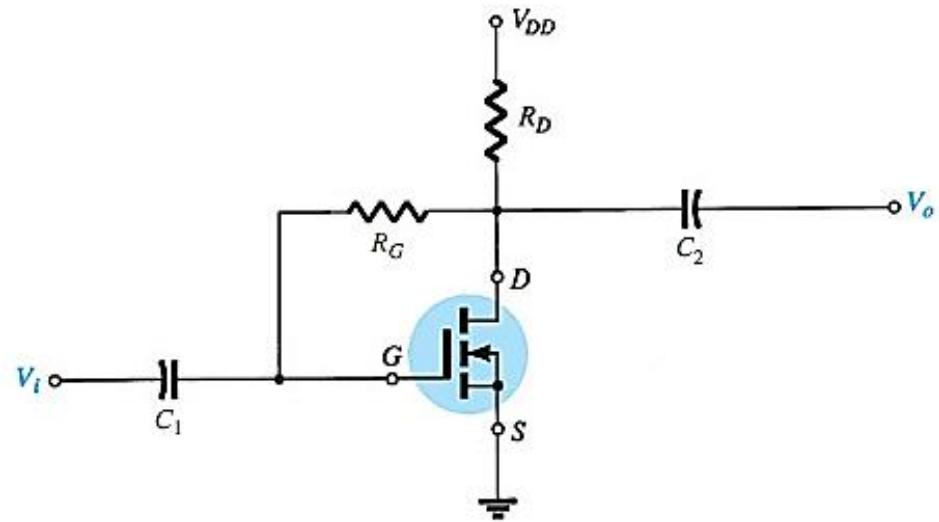
# E-MOSFET FEEDBACK BIAS

$$I_G \approx 0A$$

$$V_{RG} = 0V$$

$$V_{GS} = V_{DS}$$

$$V_{GS} = V_{DD} - I_D R_D$$



**FIG. 7.37**

*Feedback biasing arrangement.*

# E-MOSFET FEEDBACK BIAS

- **Graphical Approach** (to find  $V_{GSQ}$  and  $I_{DQ}$ ):

- Calculate the value for

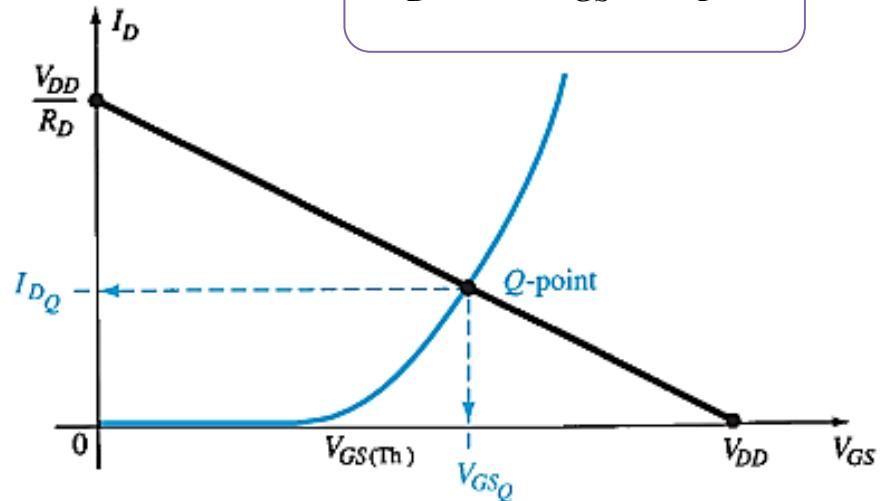
- Plot  $V_{GS}$  vs  $I_D$  for the range of interest.

$$V_{GS} = V_{DD} - I_D R_D$$

- Identify the Q-point.

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$$

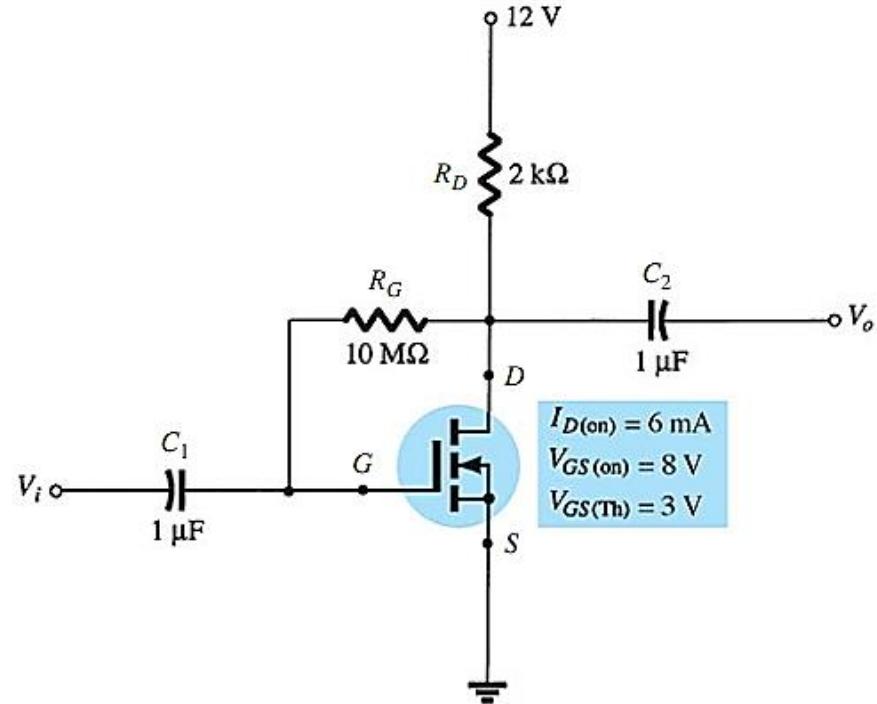
$$I_D = k(V_{GS} - V_T)^2$$



# E-MOSFET FEEDBACK BIAS EXAMPLE

- **Example 7.10:** Determine  $I_{DQ}$  and  $V_{DSQ}$  for the following circuit:

$$\begin{aligned}k &= \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2} \\&= \frac{6 \text{ mA}}{(8 \text{ V} - 3 \text{ V})^2} = \frac{6 \times 10^{-3}}{25} \text{ A/V}^2 \\&= 0.24 \times 10^{-3} \text{ A/V}^2\end{aligned}$$



**FIG. 7.40**  
Example 7.10.

# E-MOSFET FEEDBACK BIAS EXAMPLE CONTD.

For  $V_{GS} = 6$  V (between 3 and 8 V):

$$\begin{aligned}I_D &= 0.24 \times 10^{-3}(6\text{ V} - 3\text{ V})^2 = 0.24 \times 10^{-3}(9) \\&= 2.16 \text{ mA}\end{aligned}$$

as shown on Fig. 7.41. For  $V_{GS} = 10$  V (slightly greater than  $V_{GS(\text{Th})}$ ),

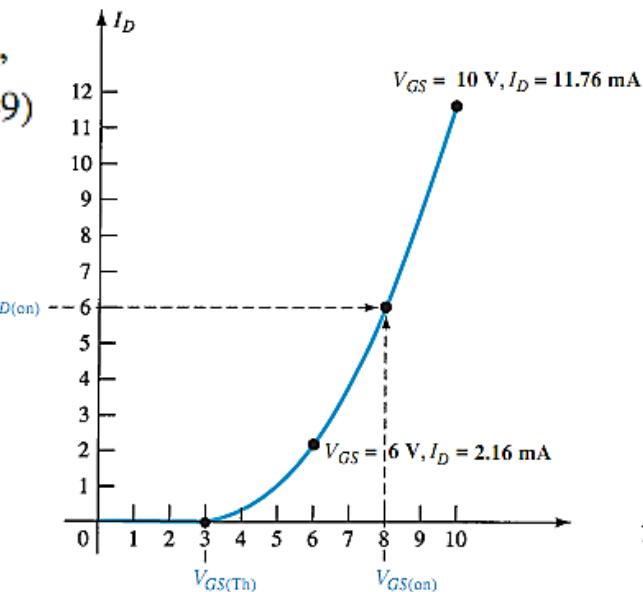
$$\begin{aligned}I_D &= 0.24 \times 10^{-3}(10\text{ V} - 3\text{ V})^2 = 0.24 \times 10^{-3}(49) \\&= 11.76 \text{ mA}\end{aligned}$$

## For the Network Bias Line

$$\begin{aligned}V_{GS} &= V_{DD} - I_D R_D \\&= 12\text{ V} - I_D(2\text{ k}\Omega)\end{aligned}$$

$$\text{Eq. (7.37): } V_{GS} = V_{DD} = 12\text{ V} \Big|_{I_D=0\text{ mA}}$$

$$\text{Eq. (7.38): } I_D = \frac{V_{DD}}{R_D} = \frac{12\text{ V}}{2\text{ k}\Omega} = 6\text{ mA} \Big|_{V_{GS}=0\text{ V}}$$



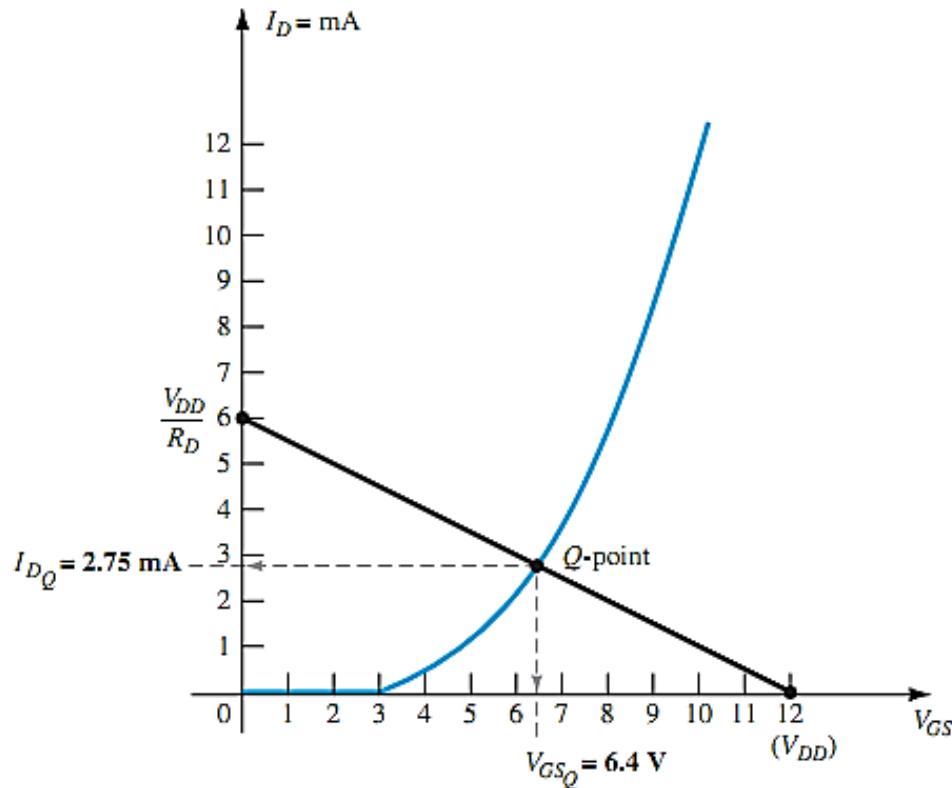
**FIG. 7.41**  
Plotting the transfer curve for the MOSFET of Fig. 7.40.

## E-MOSFET FEEDBACK BIAS EXAMPLE CONTD.

$$I_{DQ} = 2.75 \text{ mA}$$

$$V_{GSQ} = 6.4 \text{ V}$$

$$V_{DSQ} = V_{GSQ} = 6.4 \text{ V}$$



**FIG. 7.42**  
Determining the *Q*-point for the network of Fig. 7.40.



# p-CHANNEL FETs

- For p-channel FETs the same calculations and graphs are used, except that the voltage polarities and current directions are the opposite.
- The graphs will be mirrors of the n-channel graphs.



# End of Lecture-8



# OBJECTIVES

- Become acquainted with the small-signal ac model for a JFET and MOSFET.
- Be able to perform a small-signal ac analysis of a variety of JFET and MOSFET configurations.
- Begin to appreciate the design sequence applied to FET configurations.
- Understand the effects of a source resistor and load resistor on the input impedance, output impedance and overall gain.
- Be able to analyze cascaded configurations with FETs and/or BJT amplifiers.



# Introduction

- Field-effect transistor amplifiers provide an excellent voltage gain with the added feature of a high input impedance.

## JFET Small-Signal Model

- The ac analysis of a JFET Configuration requires that a small-signal ac model for the JFET be developed.
- *The gate-to-source voltage controls the drain-to-source (channel) current of a JFET.*
- The *change* in drain current that will result from a *change* in gate-to-source voltage can be determined using the transconductance factor  $g_m$  in the following manner:

$$\Delta I_D = g_m \Delta V_{GS}$$

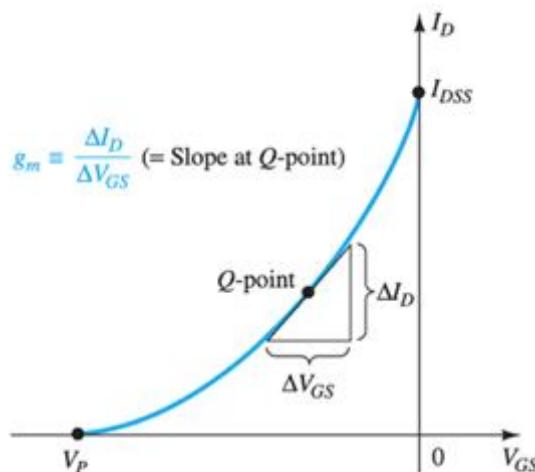
$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$



# Graphical Determination of $g_m$

If we now examine the transfer characteristics of Fig. 8.1, we find that  $g_m$  is actually the slope of the characteristics at the point of operation. That is,

$$g_m = m = \frac{\Delta y}{\Delta x} = \frac{\Delta I_D}{\Delta V_{GS}} \quad (8.3)$$



**FIG. 8.1**  
Definition of  $g_m$  using transfer characteristic.

# Example:

**EXAMPLE 8.1** Determine the magnitude of  $g_m$  for a JFET with  $I_{DSS} = 8 \text{ mA}$  and  $V_P = -4 \text{ V}$  at the following dc bias points:

- $V_{GS} = -0.5 \text{ V}$ .
- $V_{GS} = -1.5 \text{ V}$ .
- $V_{GS} = -2.5 \text{ V}$ .

**Solution:** The transfer characteristics are generated as Fig. 8.2 using the procedure defined in Chapter 7. Each operating point is then identified and a tangent line is drawn at each point to best reflect the slope of the transfer curve in this region. An appropriate increment is then chosen for  $V_{GS}$  to reflect a variation to either side of each  $Q$ -point. Equation (8.2) is then applied to determine  $g_m$ .

- $$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \cong \frac{2.1 \text{ mA}}{0.6 \text{ V}} = 3.5 \text{ mS}$$
- $$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \cong \frac{1.8 \text{ mA}}{0.7 \text{ V}} \cong 2.57 \text{ mS}$$
- $$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{1.5 \text{ mA}}{1.0 \text{ V}} = 1.5 \text{ mS}$$

Note the decrease in  $g_m$  as  $V_{GS}$  approaches  $V_P$ .

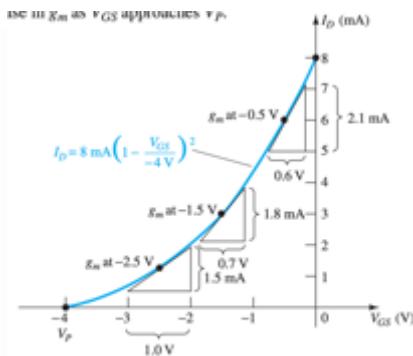


FIG. 8.2  
Calculating  $g_m$  at various bias points.

# Mathematical Definition of $g_m$

*The derivative of a function at a point is equal to the slope of the tangent line drawn at that point.*

If we therefore take the derivative of  $I_D$  with respect to  $V_{GS}$  (differential calculus) using Shockley's equation, we can derive an equation for  $g_m$  as follows:

$$\begin{aligned} g_m &= \frac{dI_D}{dV_{GS}} \Big|_{Q\text{-pt.}} = \frac{d}{dV_{GS}} \left[ I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 \right] \\ &= I_{DSS} \frac{d}{dV_{GS}} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 = 2I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right] \frac{d}{dV_{GS}} \left( 1 - \frac{V_{GS}}{V_P} \right) \\ &= 2I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right] \left[ \frac{d}{dV_{GS}} (1) - \frac{1}{V_P} \frac{dV_{GS}}{dV_{GS}} \right] = 2I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right] \left[ 0 - \frac{1}{V_P} \right] \end{aligned}$$

and

$$g_m = \frac{2I_{DSS}}{|V_P|} \left[ 1 - \frac{V_{GS}}{V_P} \right] \quad (8.4)$$

the slope of the transfer curve is a maximum at  $V_{GS} = 0$  V.

$$g_m = \frac{2I_{DSS}}{|V_P|} \left[ 1 - \frac{0}{V_P} \right]$$

$$g_{m0} = \frac{2I_{DSS}}{|V_P|}$$

$$g_m = g_{m0} \left[ 1 - \frac{V_{GS}}{V_P} \right]$$



## Example

**EXAMPLE 8.2** For the JFET having the transfer characteristics of Example 8.1:

- Find the maximum value of  $g_m$ .
- Find the value of  $g_m$  at each operating point of Example 8.1 using Eq. (8.6) and compare with the graphical results.

**Solution:**

a. 
$$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(8 \text{ mA})}{4 \text{ V}} = 4 \text{ mS}$$
 (maximum possible value of  $g_m$ )

b. At  $V_{GS} = -0.5 \text{ V}$ ,

$$g_m = g_{m0} \left[ 1 - \frac{V_{GS}}{V_P} \right] = 4 \text{ mS} \left[ 1 - \frac{-0.5 \text{ V}}{-4 \text{ V}} \right] = 3.5 \text{ mS}$$
 (vs. 3.5 mS graphically)

At  $V_{GS} = -1.5 \text{ V}$ ,

$$g_m = g_{m0} \left[ 1 - \frac{V_{GS}}{V_P} \right] = 4 \text{ mS} \left[ 1 - \frac{-1.5 \text{ V}}{-4 \text{ V}} \right] = 2.5 \text{ mS}$$
 (vs. 2.57 mS graphically)

At  $V_{GS} = -2.5 \text{ V}$ ,

$$g_m = g_{m0} \left[ 1 - \frac{V_{GS}}{V_P} \right] = 4 \text{ mS} \left[ 1 - \frac{-2.5 \text{ V}}{-4 \text{ V}} \right] = 1.5 \text{ mS}$$
 (vs. 1.5 mS graphically)



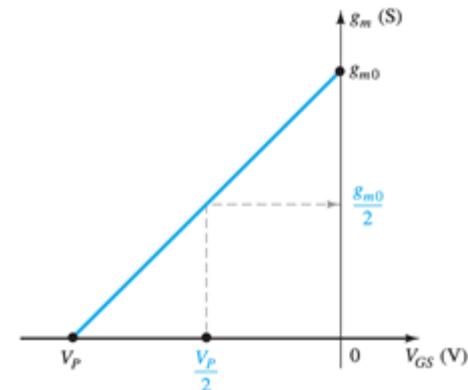
## Plotting $g_m$ versus $V_{GS}$

Since the factor  $\left(1 - \frac{V_{GS}}{V_P}\right)$  of Eq. (8.6) is less than 1 for any value of  $V_{GS}$  other than 0 V, the magnitude of  $g_m$  will decrease as  $V_{GS}$  approaches  $V_P$  and the ratio  $\frac{V_{GS}}{V_P}$  increases in magnitude. At  $V_{GS} = V_P$ ,  $g_m = g_{m0}(1 - 1) = 0$ . Equation (8.6) defines a straight line with a minimum value of 0 and a maximum value of  $g_{m0}$ , as shown by the plot of Fig. 8.3.

In general, therefore

*the maximum value of  $g_m$  occurs where  $V_{GS} = 0$  V and the minimum value at  $V_{GS} = V_P$ . The more negative the value of  $V_{GS}$  the less the value of  $g_m$ .*

Figure 8.3 also shows that when  $V_{GS}$  is one-half the pinch-off value,  $g_m$  is one-half the maximum value.



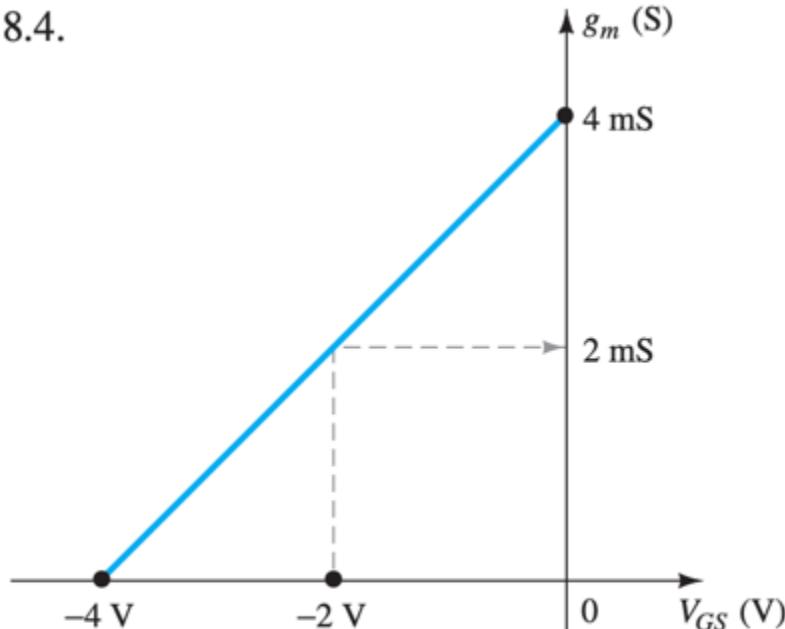
**FIG. 8.3**  
Plot of  $g_m$  versus  $V_{GS}$ .



## Example

**EXAMPLE 8.3** Plot  $g_m$  versus  $V_{GS}$  for the JFET of Examples 8.1 and 8.2.

**Solution:** Note Fig. 8.4.



**FIG. 8.4**

Plot of  $g_m$  versus  $V_{GS}$  for a JFET with  $I_{DSS} = 8 \text{ mA}$  and  $V_P = -4 \text{ V}$ .



## Effect of $I_D$ on $g_m$

A mathematical relationship between  $g_m$  and the dc bias current  $I_D$  can be derived by noting that Shockley's equation can be written in the following form:

$$1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}} \quad (8.8)$$

Substituting Eq. (8.8) into Eq. (8.6) results in

$$g_m = g_{m0} \left( 1 - \frac{V_{GS}}{V_P} \right) = g_{m0} \sqrt{\frac{I_D}{I_{DSS}}} \quad (8.9)$$

Using Eq. (8.9) to determine  $g_m$  for a few specific values of  $I_D$ , we obtain the following results:

a. If  $I_D = I_{DSS}$ ,

$$g_m = g_{m0} \sqrt{\frac{I_{DSS}}{I_{DSS}}} = g_{m0}$$

b. If  $I_D = I_{DSS}/2$ ,

$$g_m = g_{m0} \sqrt{\frac{I_{DSS}/2}{I_{DSS}}} = 0.707g_{m0}$$

c. If  $I_D = I_{DSS}/4$ ,

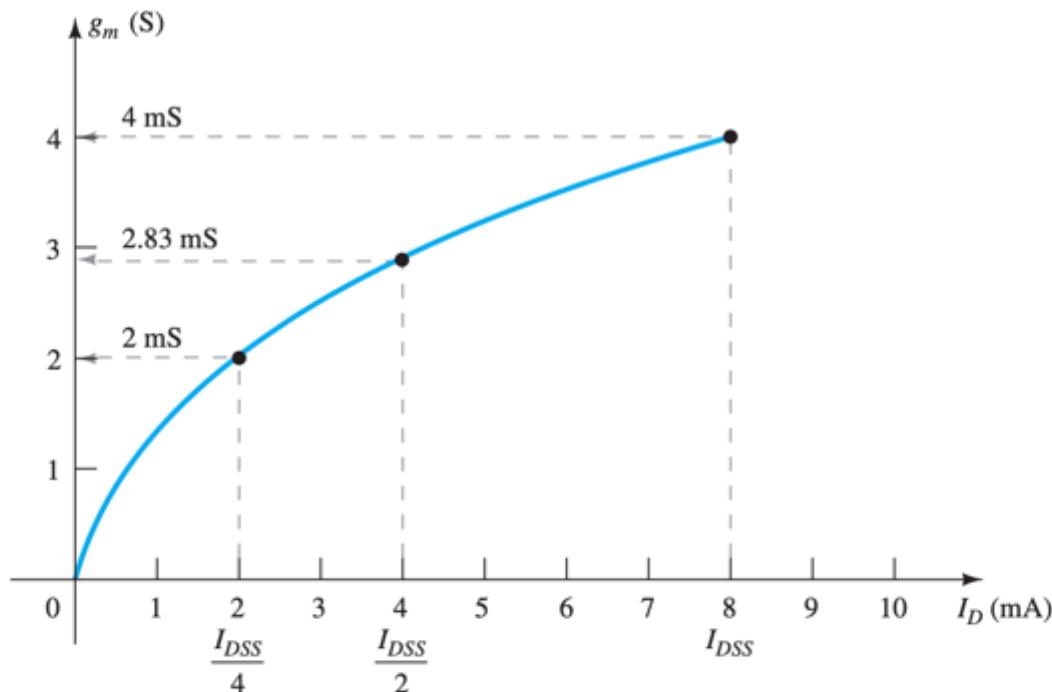
$$g_m = g_{m0} \sqrt{\frac{I_{DSS}/4}{I_{DSS}}} = \frac{g_{m0}}{2} = 0.5g_{m0}$$



## Example

**EXAMPLE 8.4** Plot  $g_m$  versus  $I_D$  for the JFET of Examples 8.1 through 8.3.

**Solution:** See Fig. 8.5.



**FIG. 8.5**

Plot of  $g_m$  versus  $I_D$  for a JFET with  $I_{DSS} = 8 \text{ mA}$  and  $V_{GS} = -4 \text{ V}$ .



# End of Lecture-9

# JFET Small Signal Model

## JFET Input Impedance $Z_i$

The input impedance of all commercially available JFETs is sufficiently large to assume that the input terminals approximate an open circuit. In equation form,

$$Z_i (\text{JFET}) = \infty \Omega \quad (8.10)$$

For a JFET a practical value of  $10^9 \Omega$  ( $1000 \text{ M}\Omega$ ) is typical, whereas a value of  $10^{12} \Omega$  to  $10^{15} \Omega$  is typical for MOSFETs and MESFETs.

## JFET Output Impedance $Z_o$

The output impedance of JFETs is similar in magnitude to that of conventional BJTs. On JFET specification sheets, the output impedance will typically appear as  $g_{os}$  or  $y_{os}$  with the units of  $\mu\text{S}$ . The parameter  $y_{os}$  is a component of an *admittance equivalent circuit*, with the subscript  $o$  signifying an *output* network parameter and  $s$  the terminal (source) to which it is attached in the model. For the JFET of Fig. 6.20,  $g_{os}$  has a range of  $10 \mu\text{S}$  to  $50 \mu\text{S}$  or  $20 \text{ k}\Omega$  ( $R = 1/G = 1/50 \mu\text{S}$ ) to  $100 \text{ k}\Omega$  ( $R = 1/G = 1/10 \mu\text{S}$ ).

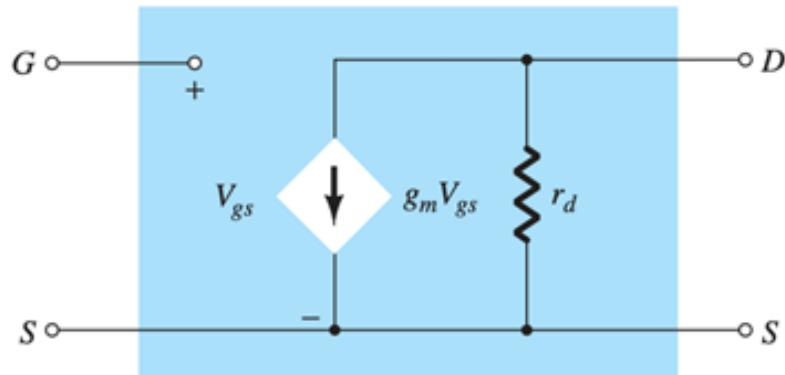
In equation form,

$$Z_o (\text{JFET}) = r_d = \frac{1}{g_{os}} = \frac{1}{y_{os}} \quad (8.11)$$



# JFET AC Equivalent Circuit

Now that the important parameters of an ac equivalent circuit have been introduced and discussed, a model for the JFET transistor in the ac domain can be constructed. The control of  $I_d$  by  $V_{gs}$  is included as a current source  $g_m V_{gs}$  connected from drain to source as shown in Fig. 8.8. The current source has its arrow pointing from drain to source to establish a  $180^\circ$  phase shift between output and input voltages as will occur in actual operation.



**FIG. 8.8**  
*JFET ac equivalent circuit.*

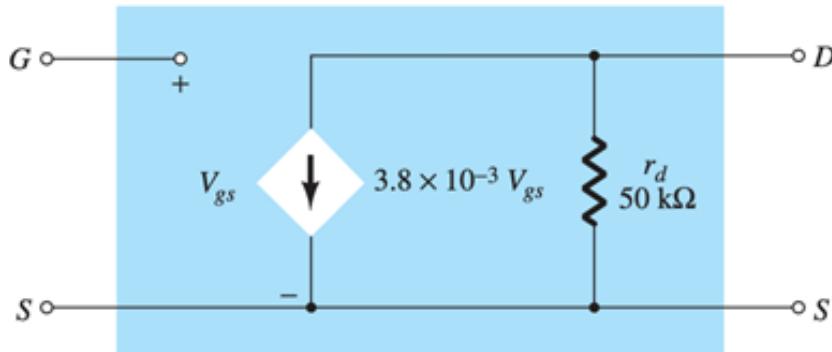
# Example

**EXAMPLE 8.6** Given  $g_{fs} = 3.8 \text{ mS}$  and  $g_{os} = 20 \mu\text{S}$ , sketch the FET ac equivalent model.

**Solution:**

$$g_m = g_{fs} = 3.8 \text{ mS} \quad \text{and} \quad r_d = \frac{1}{g_{os}} = \frac{1}{20 \mu\text{S}} = 50 \text{ k}\Omega$$

resulting in the ac equivalent model of Fig. 8.9.



**FIG. 8.9**

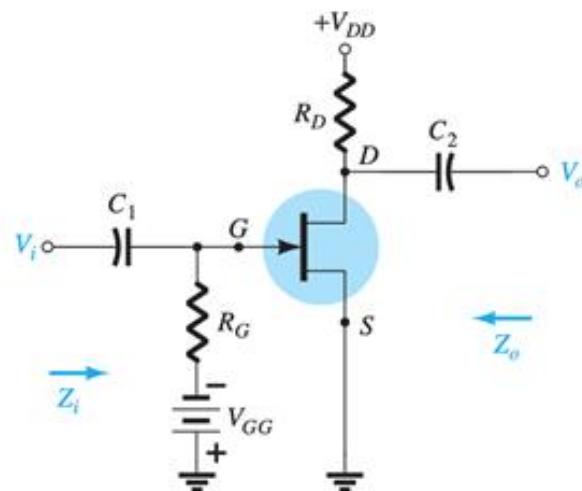
*JFET ac equivalent model for Example 8.6.*



# FIXED-BIAS CONFIGURATION

Now that the JFET equivalent circuit has been defined, a number of fundamental JFET small-signal configurations are investigated. The approach parallels the ac analysis of BJT amplifiers with a determination of the important parameters of  $Z_i$ ,  $Z_o$ , and  $A_v$  for each configuration.

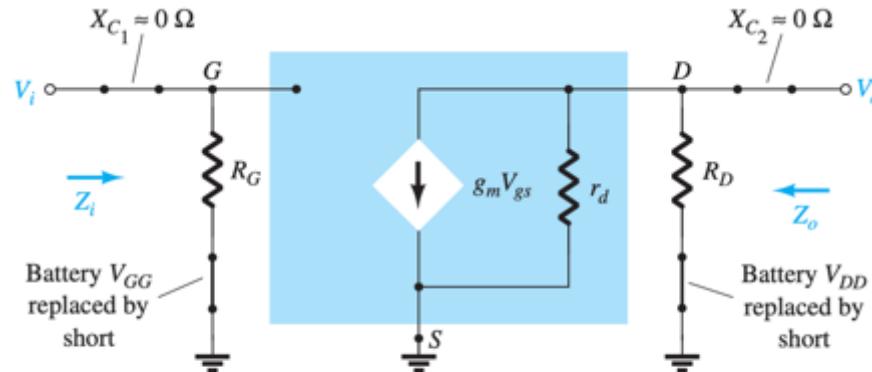
The *fixed-bias* configuration of Fig. 8.10 includes the coupling capacitors  $C_1$  and  $C_2$ , which isolate the dc biasing arrangement from the applied signal and load; they act as short-circuit equivalents for the ac analysis.



**FIG. 8.10**  
JFET fixed-bias configuration.

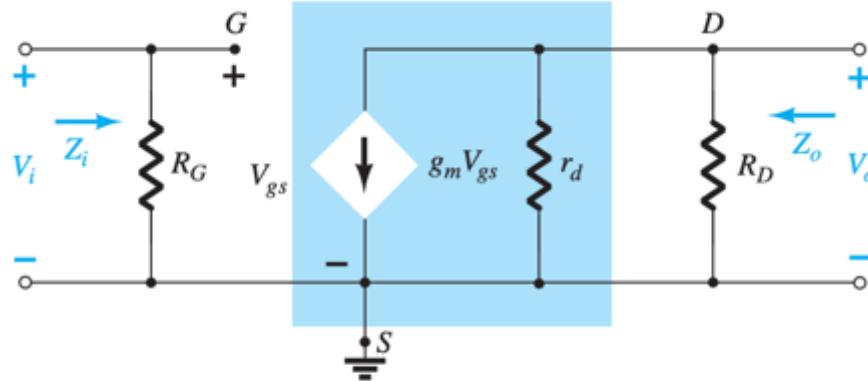


# Continued.



**FIG. 8.11**

Substituting the JFET ac equivalent circuit unit into the network of Fig. 8.10.



**FIG. 8.12**

Redrawn network of Fig. 8.11.



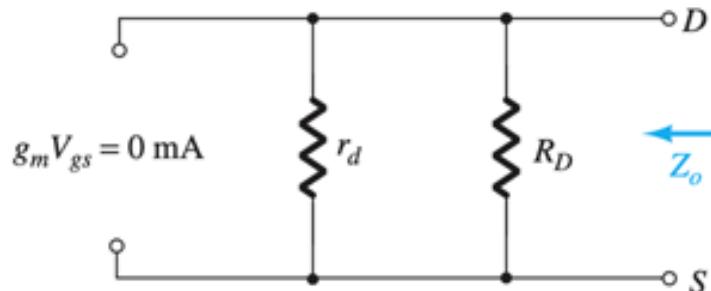
**Z<sub>i</sub>** Figure 8.12 clearly reveals that

$$Z_i = R_G \quad (8.13)$$

because of the infinite input impedance at the input terminals of the JFET.

**Z<sub>o</sub>** Setting  $V_i = 0$  V as required by the definition of  $Z_o$  will establish  $V_{gs}$  as 0 V also. The result is  $g_m V_{gs} = 0$  mA, and the current source can be replaced by an open-circuit equivalent as shown in Fig. 8.13. The output impedance is

$$Z_o = R_D \| r_d \quad (8.14)$$



**FIG. 8.13**  
Determining  $Z_o$ .



$$Z_o \cong R_D \quad r_d \geq 10R_D$$

**A<sub>v</sub>** Solving for  $V_o$  in Fig. 8.12, we find

$$V_o = -g_m V_{gs} (r_d \| R_D)$$

but

$$V_{gs} = V_i$$

and

$$V_o = -g_m V_i (r_d \| R_D)$$

so that

$$A_v = \frac{V_o}{V_i} = -g_m (r_d \| R_D)$$

If  $r_d \geq 10R_D$ ,

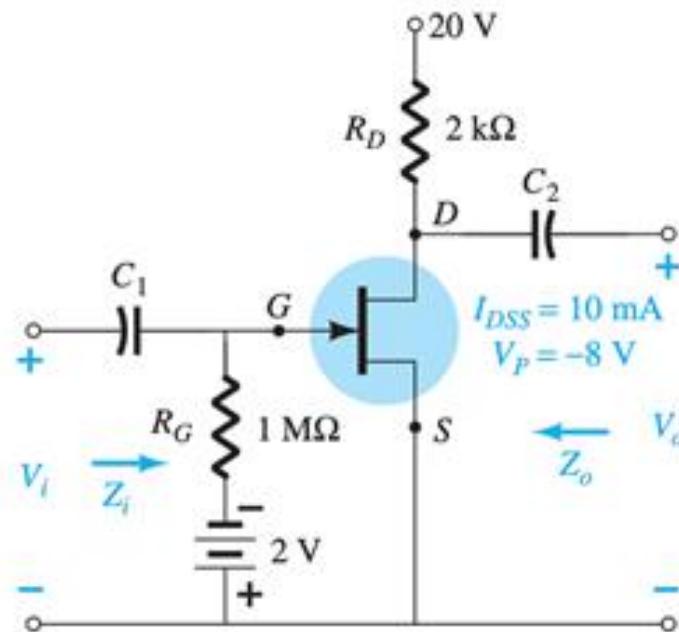
$$A_v = \frac{V_o}{V_i} = -g_m R_D \quad r_d \geq 10R_D$$

**Phase Relationship** The negative sign in the resulting equation for  $A_v$  clearly reveals a phase shift of  $180^\circ$  between input and output voltages.



**EXAMPLE 8.7** The fixed-bias configuration of Example 7.1 had an operating point defined by  $V_{GSQ} = -2$  V and  $I_{DQ} = 5.625$  mA, with  $I_{DSS} = 10$  mA and  $V_P = -8$  V. The network is redrawn as Fig. 8.14 with an applied signal  $V_i$ . The value of  $y_{os}$  is provided as  $40 \mu\text{S}$ .

- Determine  $g_m$ .
- Find  $r_d$ .
- Determine  $Z_i$ .
- Calculate  $Z_o$ .
- Determine the voltage gain  $A_v$ .
- Determine  $A_v$  ignoring the effects of  $r_d$ .



**FIG. 8.14**  
JFET configuration for Example 8.7.



**Solution:**

a.  $g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10 \text{ mA})}{8 \text{ V}} = 2.5 \text{ mS}$

$$g_m = g_{m0} \left( 1 - \frac{V_{GSQ}}{V_P} \right) = 2.5 \text{ mS} \left( 1 - \frac{(-2 \text{ V})}{(-8 \text{ V})} \right) = \mathbf{1.88 \text{ mS}}$$

b.  $r_d = \frac{1}{y_{os}} = \frac{1}{40 \mu\text{S}} = \mathbf{25 \text{ k}\Omega}$

c.  $Z_i = R_G = \mathbf{1 \text{ M}\Omega}$

d.  $Z_o = R_D \| r_d = 2 \text{ k}\Omega \| 25 \text{ k}\Omega = \mathbf{1.85 \text{ k}\Omega}$

e.  $A_v = -g_m(R_D \| r_d) = -(1.88 \text{ mS})(1.85 \text{ k}\Omega)$   
 $= \mathbf{-3.48}$

f.  $A_v = -g_m R_D = -(1.88 \text{ mS})(2 \text{ k}\Omega) = \mathbf{-3.76}$

As demonstrated in part (f), a ratio of  $25 \text{ k}\Omega : 2 \text{ k}\Omega = 12.5:1$  between  $r_d$  and  $R_D$  results in a difference of 8% in the solution.



# End of Lecture- 10

