AMERICAN INTERNATIONAL UNIVERSITY–BANGLADESH (AIUB)

FACULTY OF SCIENCE & TECHNOLOGY

DIGITAL LOGIC AND CIRCUITS LAB

Summer 2022-2023

Section: F
Group Number: 02

EXPERIMENT NO. 6

NAME OF THE EXPERIMENT

Study of Different Flip-Flops

Supervised By

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Submitted By:

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Introduction:

The basic building blocks of combinational logic circuits are gates. In particular, AND, OR, and NOT gates (however, there are also XOR, NAND, NOR, and XNOR gates).

The basic building blocks of sequential logic circuits are flip flops. Flip-flops are devices that use a clock. Each flip-flop can store one bit. There are different types of flip-flops. D flip-flop, T flip-flop, J-K flip-flop, etc.

Theory and Methodology:

A flip-flop has two/three inputs. One input is a control input. For a D flip flop, the control input is labeled D. For a T flip-flop; the control input is labeled T. For the J-K flip-flop, the control inputs are J and K. The other input is the clock.

The clock input is usually drawn with a triangular input. These flip-flops are *positive edge-triggered flip-flops*. This means the flip-flops can only change output values when the clock is at a positive edge. There are also negative edge-triggered flip flops, which vary on a negative edge. In this theory section, we consider only positive edge-triggered flip flops.

When the clock is not at a positive edge, then the output value is held. That is, it does not change.

A flip flop also has two outputs, **Q** and **Q'**. The output is really the bit that's stored. Thus, the flip-flop is always outputting one bit of information.

But one might wonder "Doesn't it have two bits of information? **Q** and **Q'**?" If we have two bits, we have four possible values. However, **Q'** is the negation of **Q** which means you only have two possible outputs: **Q = 0, Q' = 1** or **Q = 1, Q' = 0**. Since the second output is always negated from the first, you don't get any additional storage. But what is the necessity of the negated output? Actually, the design of flip-flop gives **Q'** basically for free, so that's why flip-flops have both the regular output and the negated output.

D Flip-Flop:

In a positive edge triggered D flip-flop, the output **Q** samples the input **D** and becomes **Q = D** only at the positive edge of the clock and it does not change during the whole clock cycle even if the input changes.

Sometimes flip flops often have two additional inputs called *clear* and *preset*. Conventionally they are drawn at the top and bottom of the flip flop respectively. 'Preset' and 'Clear' can be either active low or active high. If the preset is active, the output will be 1 no matter what are the conditions of D or clock. But 'clear' has two types. Asynchronous clear and synchronous clear. If the asynchronous clear is activated, it causes **Q** to be automatically set to 0. It does this, even if the clock has not reached a positive edge. That is, it sets Q to zero as fast as it can. The asynchronous clear is often used to reset flip flops to some initial value. But for synchronous clear, **Q** will be 0 if the clear is active when the clock is in a positive edge.

There are different ways to design a D flip-flop. In this lab sheet, only one way is shown. Students will be familiar about other ways in their theory class.

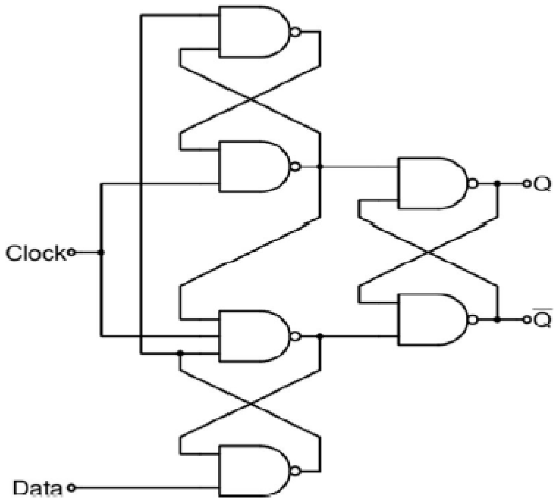


Figure1: Logic circuit a positive edge triggered D flip-flop without preset and clear capability.

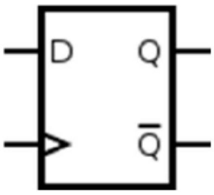


Figure 2: Graphical Symbol of a positive edge triggered D flip-flop without preset and clear capability.

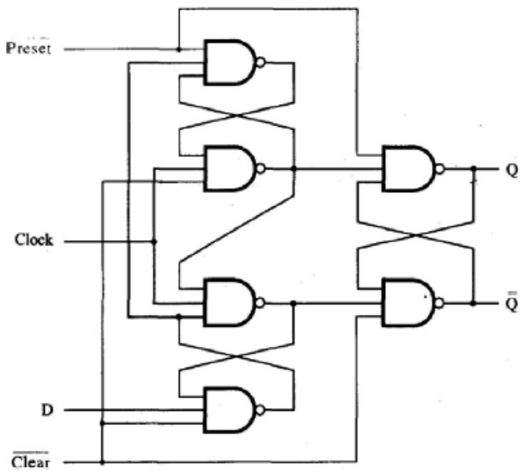


Figure3: Logic circuit a positive edge triggered D flip-flop with preset (active low) and asynchronous clear (active low) capability.

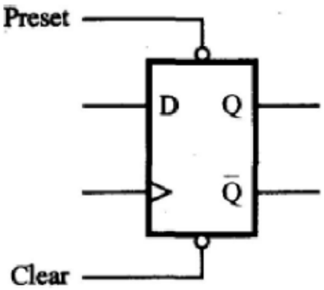


Figure4: Graphical symbol of a positive edge triggered D flip-flop with preset (active low) and asynchronous clear (active low) capability.

Timing Diagram of a positive edge trigged D flip-flop without 'Preset' and 'Clear' capability:

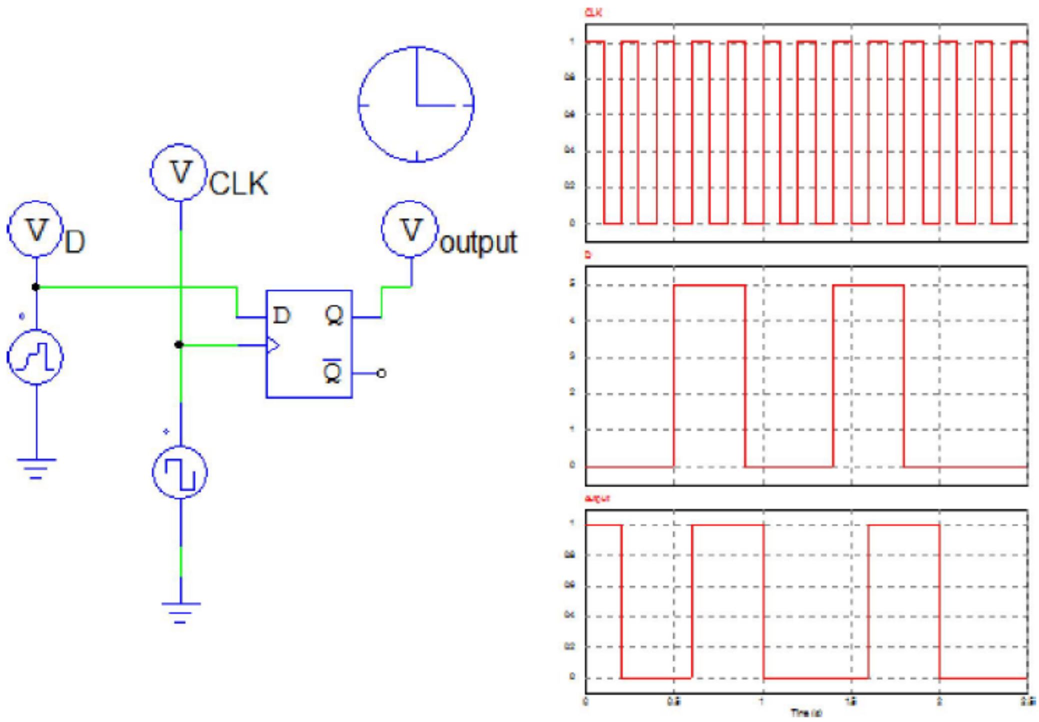


Figure11: Timing Diagram of a positive edge triggered D Flip-Flop without preset and clear capability. Output only samples the input when the clock has a positive edge and remains unchanged for the next positive edge.

J-K Flip Flop:

In a J-K flip-flop, there are two control input labeled as J and K and a clock input. It has two outputs Q and Q' as usual. In a positive edge triggered J-K flip-flop, output only changes at the positive edge of the clock depending on the values of J and K. If J=1 and K=0, Q is set to 1. If J = 0, K=1 then Q is set to 0. If J = 0 and K = 0 then Q remains unchanged. If J = 1 and K = 1 then Q changes from its former value, which we can say the output toggles.

We can show the characteristics of a J-K in a table given below.

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	~ Q(t)

J-K flip-flop can be designed easily using D flip-flops.

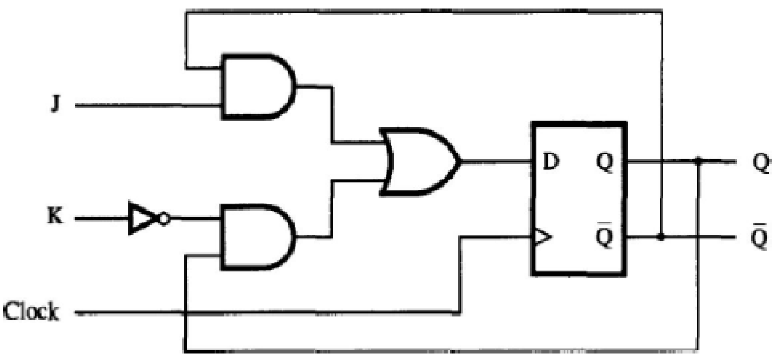


Figure 5: J-K flip-flop using D flip-flop

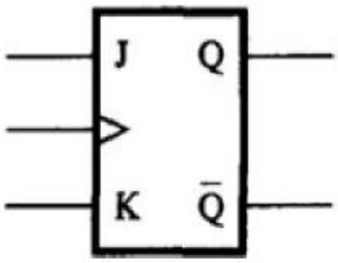


Figure 6: Graphical Symbol of J-K flip-flop.

T Flip-Flop:

A T flip-flop has a control input labeled as T and a clock. The characteristic of a T flip-flop is such that the output toggles at the positive edge of the clock if T is 1. But if T is 0, the output remains unchanged even at the positive edge of the clock.

A T flip-flop can be designed easily by making J and K short of a J-K flip flop.

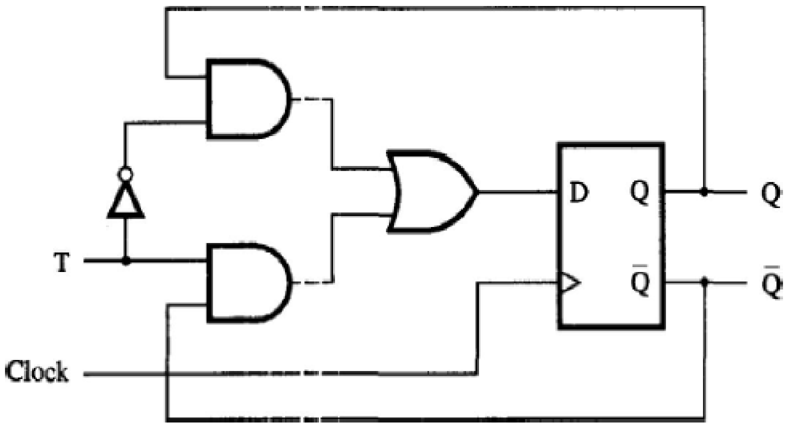


Figure 7: J-K flip-flop using D flip-flop

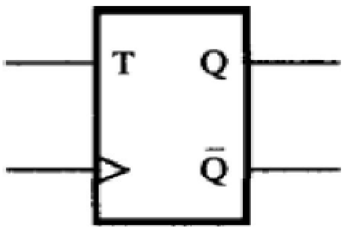


Figure 8: Graphical Symbol of T flip-flop.

There are built-in ICs for D flip-flop and J-K flip-flop. IC-7474 contains 2 D flip-flops and IC-7476 contains 2 J-K flip-flops. The pin configuration of IC-7474 and IC 7476 are given below.

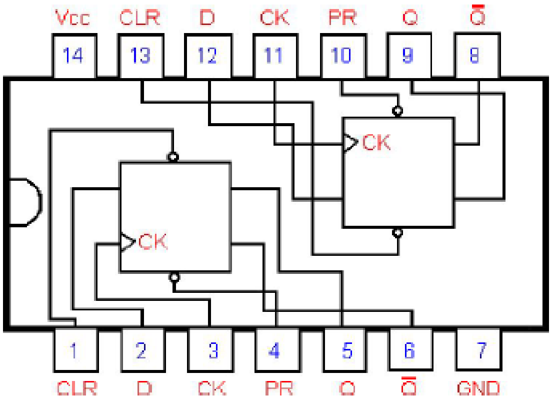


Figure 9: IC-7474

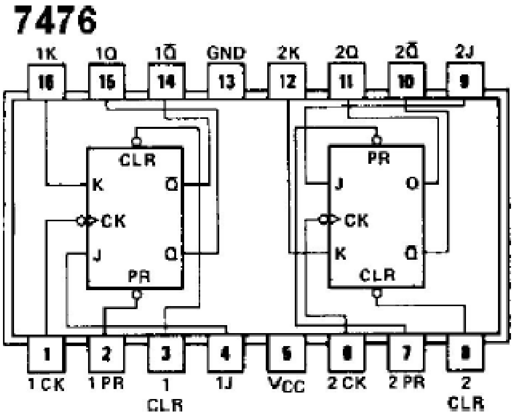


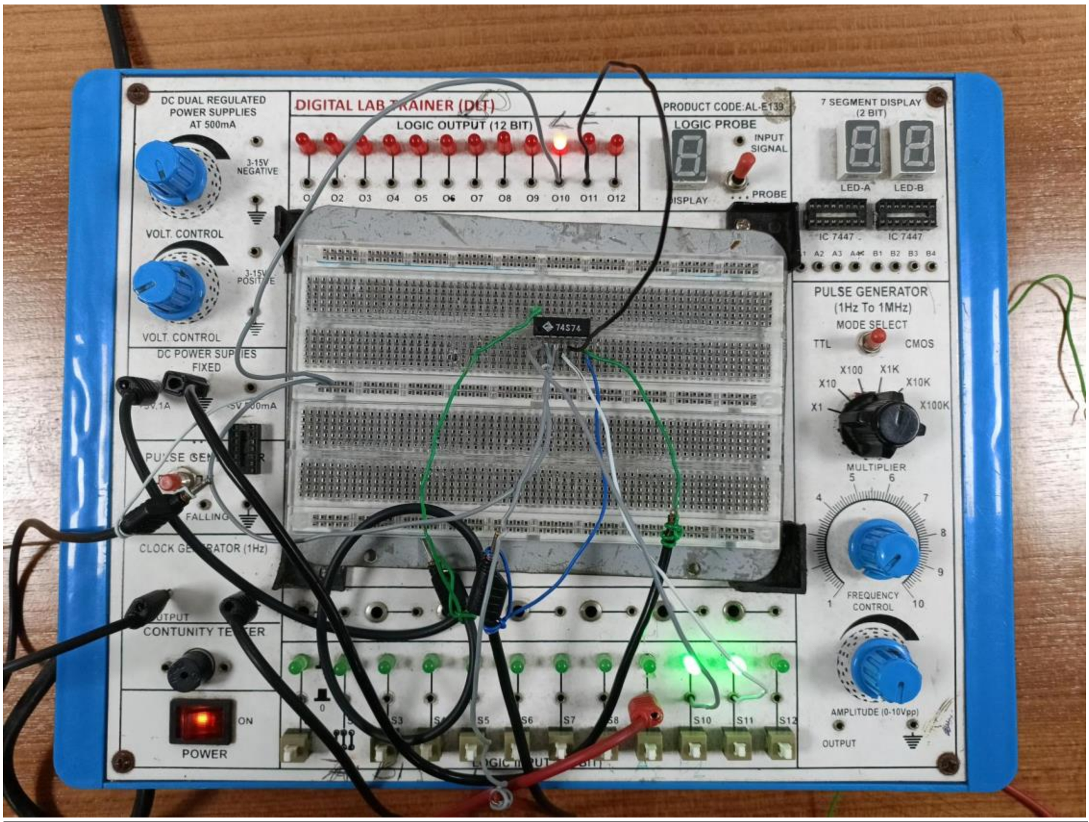
Figure10: IC-7476

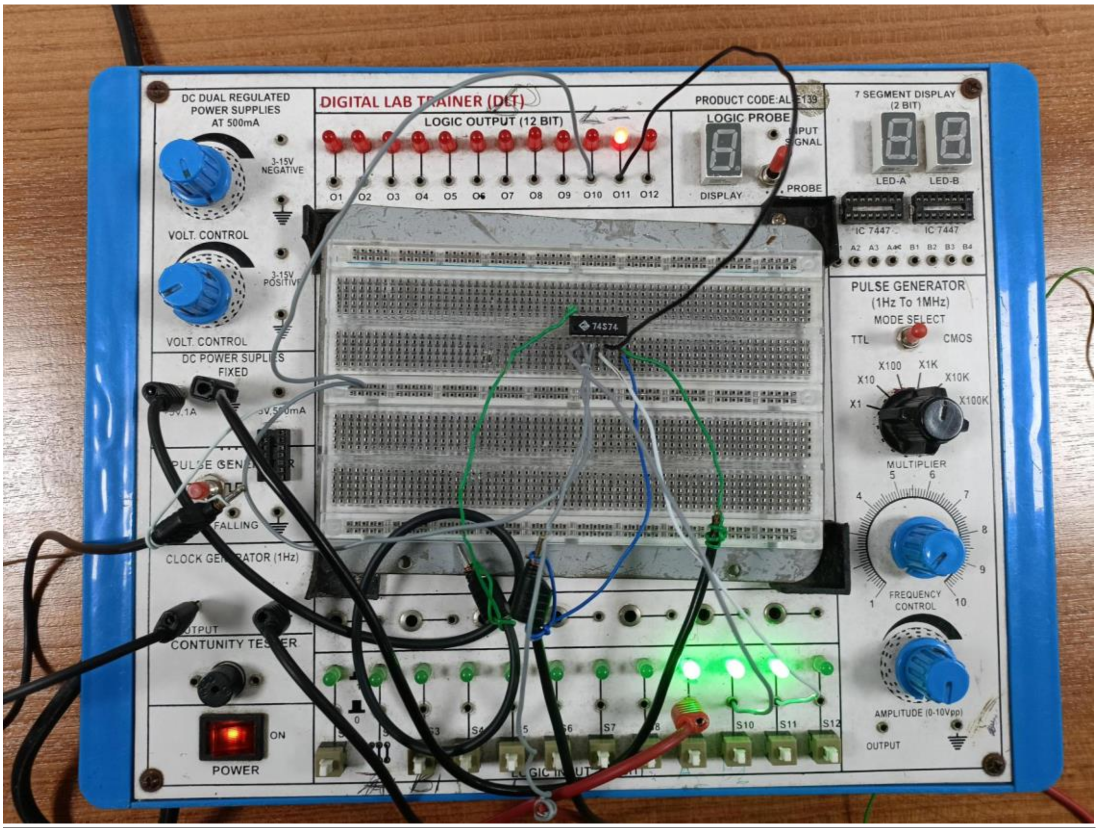
Apparatus:

IC: 7404 (NOT Gate) 1[pcs]
7408 (AND Gate), 2[pcs]
7432 (OR Gate) 1[pcs]
7400 (NAND Gate) 6[pcs]
7474 (D flip-flop) 1[pcs]
7476 (J-K flip-flop) 1[pcs]

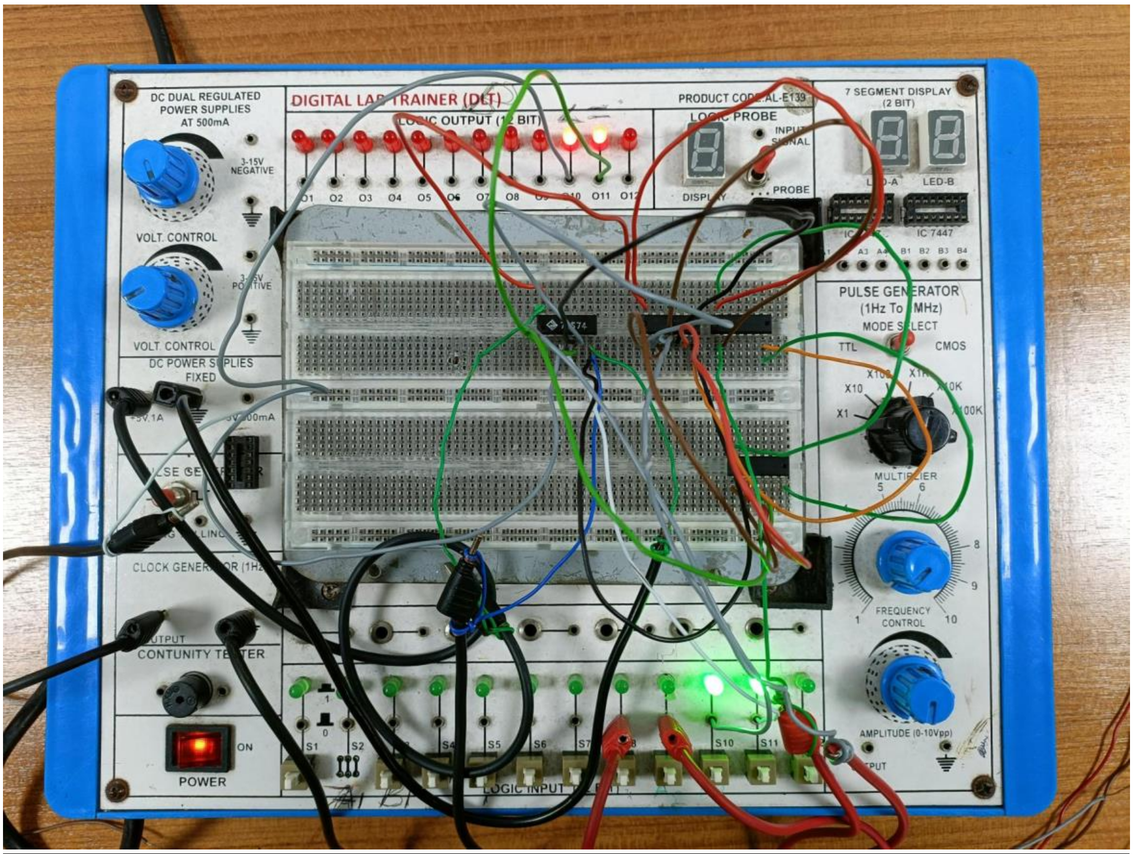
Hardware Implementation:

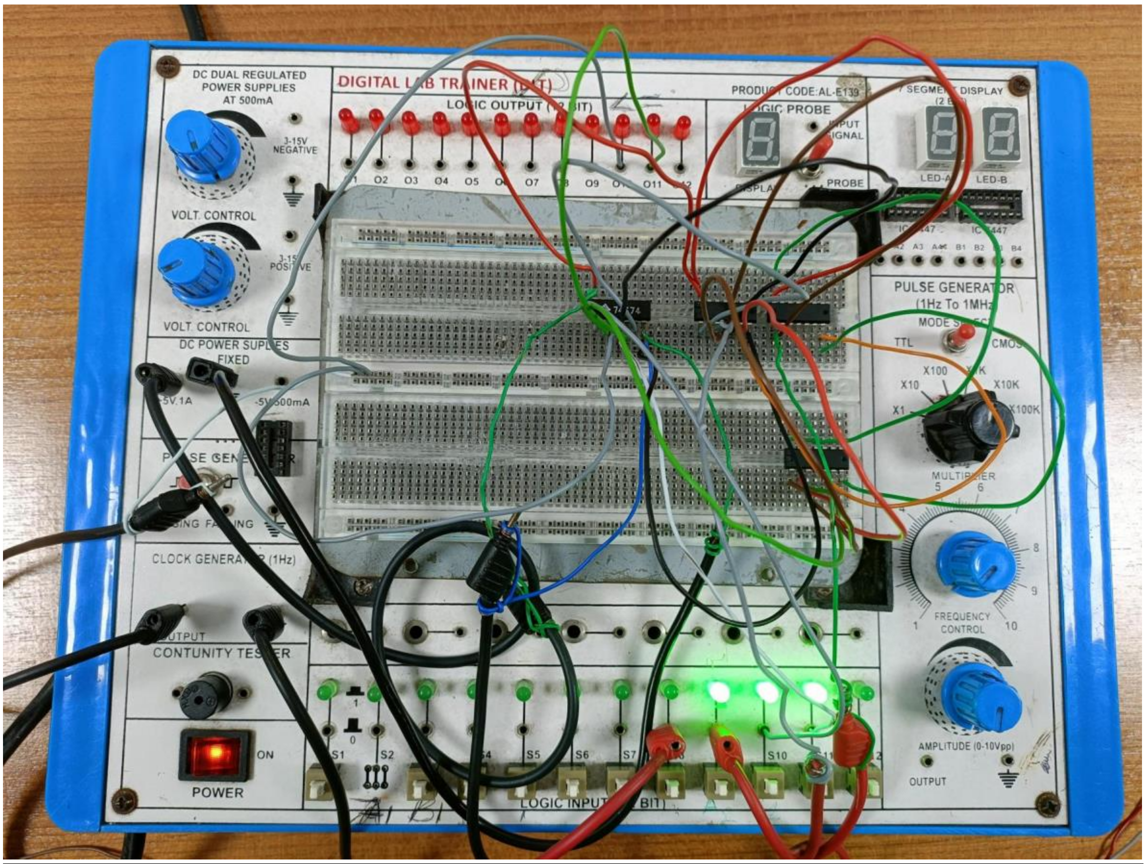
D flip-flop

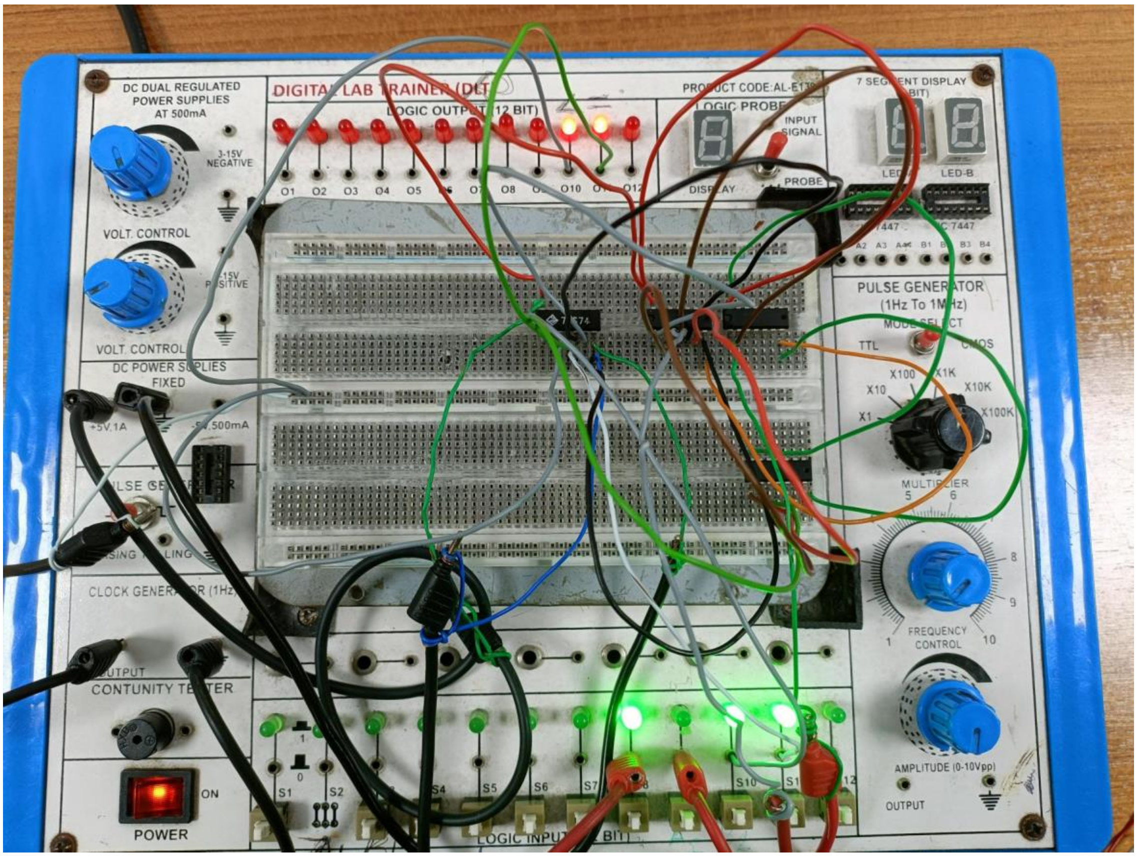


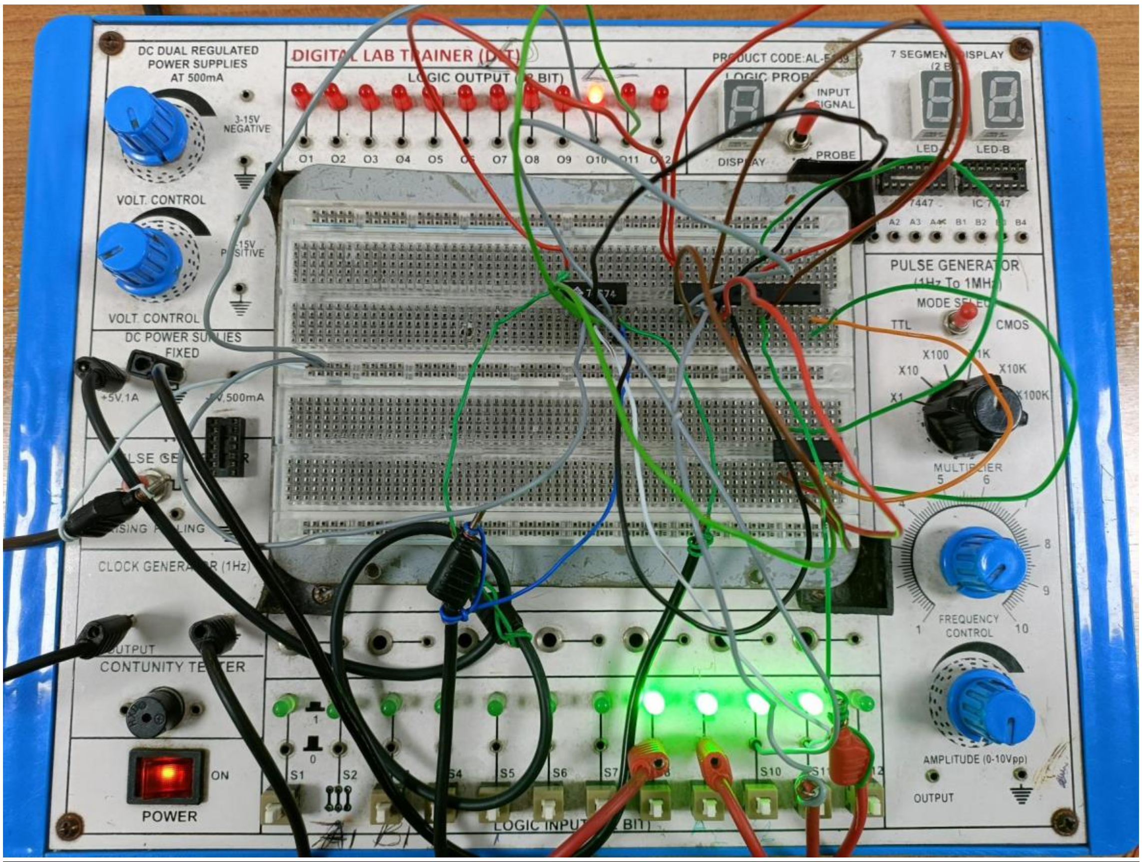


J-k flip-flop

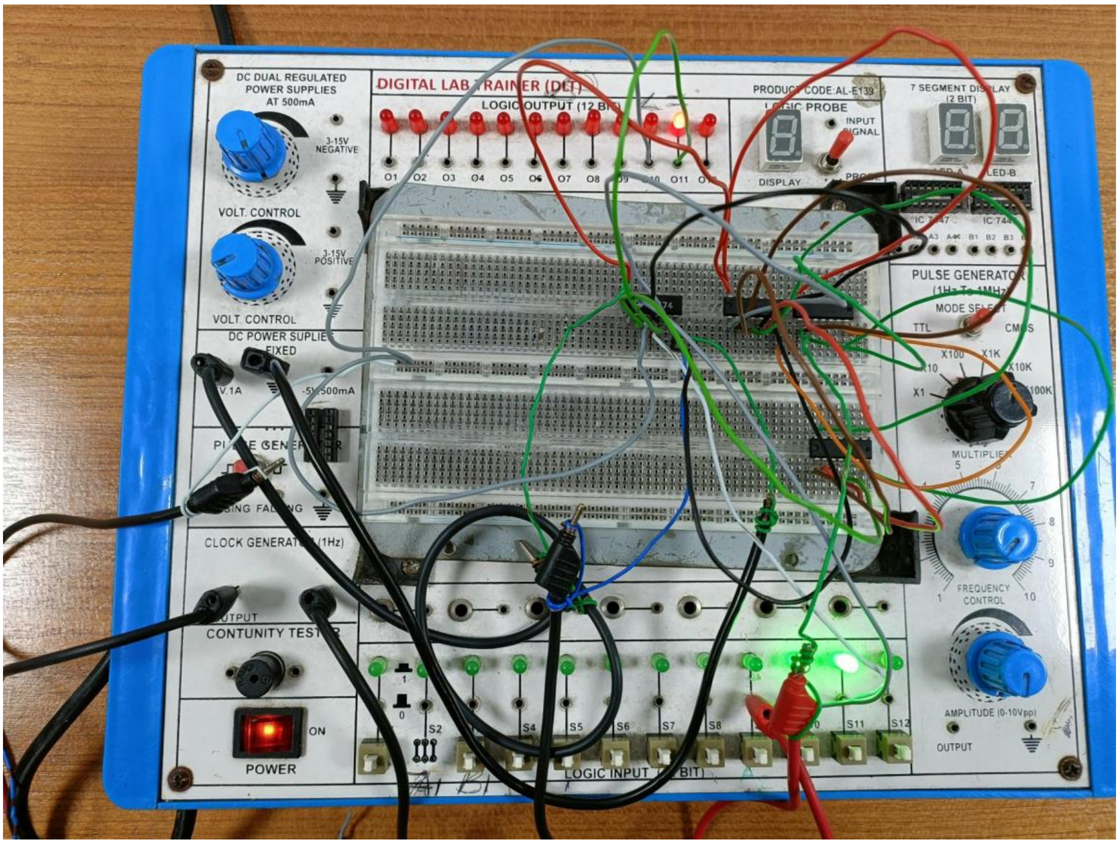

DC DUAL REGULATED
POWER SUPPLIES
AT 500mA
DIGITAL LAB TRAINER (DLT)
PRODUCT CODE:AL-E133
7 SEGMENT DISPLAY
(2 BIT)
3-15V
NEGATIVE
VOLT. CONTROL
INPUT
SIGNAL
PROBE
LED-A
LED-B
IC 7447
PULSE GENERATOR
(1Hz To 1MHz)
MODE SELECT
TTL
CMOS
X10
X1
X10K
X100K
MULTIPLIER
FREQUENCY
CONTROL
AMPLITUDE (0-10Vpp)
CONTUNITY TESTER
POWER
ON
S1
S2
S4
S5
S6
S7
S10
S11


DC DUAL REGULATED
POWER SUPPLIES
AT 500mA
3-15V
NEGATIVE
VOLT. CONTROL
LOGIC PROBE
LED-A
LED-B
PULSE GENERATOR
TTL
X100
X10
X1
X10K
X100K
MULTIPLIER
FREQUENCY
CONTROL
AMPLITUDE (0-10Vpp)
OUTPUT
CLOCK GENERATOR (1Hz)
POWER
ON
S1
S2
S4
S5
S6
S7
S10


DC DUAL REGULATED POWER SUPPLIES AT 500mA
VOLT. CONTROL
VOLT. CONTROL
DC POWER SUPPLIES FIXED
+5V,1A
CLOCK GENERATOR (1Hz)
CONTUNITY TESTER
POWER
ON
LOGIC OUTPUT (12 BIT)
O1 O2 O3 O4 O5 O6 O7 O8 O9 O10 O11 O12
LOGIC PROBE
DISPLAY
INPUT SIGNAL
PROBE
7 SEGMENT DISPLAY
LED-B
PULSE GENERATOR
(1Hz To 1MHz)
TTL
CMOS
X10
X100
X1K
X10K
X100K
X1
MULTIPLIER
FREQUENCY CONTROL
AMPLITUDE (0-10Vpp)
OUTPUT
S1 S2 S5 S6 S7 S10


DC DUAL REGULATED POWER SUPPLIES AT 500mA
3-15V NEGATIVE
VOLT. CONTROL
VOLT. CONTROL
DC POWER SUPPLIES FIXED
+5V,1A
CONTUNITY TESTER
POWER
ON
LOGIC OUTPUT
O1 O2 O3 O4 O5 O6 O7 O8 O9 O10 O11 O12
DISPLAY
INPUT SIGNAL
PROBE
LED-B
PULSE GENERATOR
TTL
CMOS
X10
X100
X10K
X100K
X1
FREQUENCY CONTROL
AMPLITUDE (0-10Vpp)
OUTPUT
S1 S2 S4 S5 S6 S7 S10

T flip-flop


DC DUAL REGULATED
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VOLT. CONTROL
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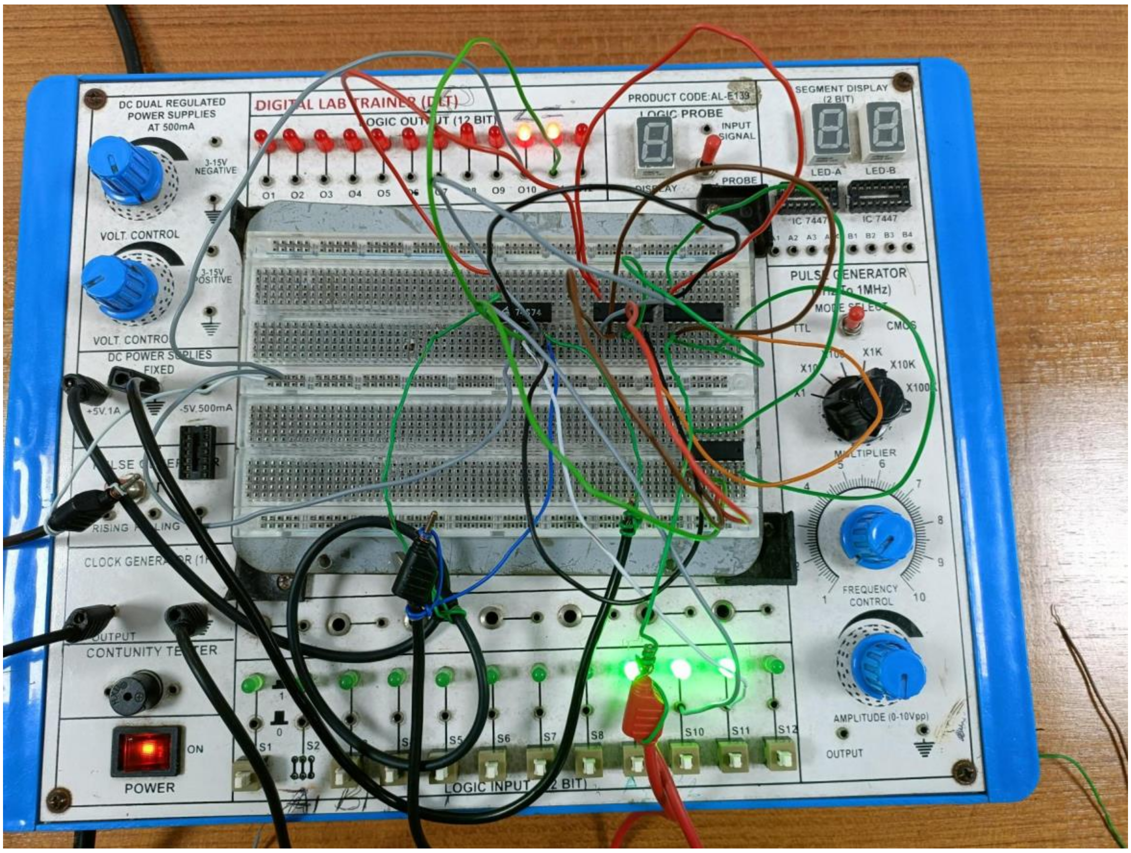
FREQUENCY
CONTROL
AMPLITUDE (0-10Vpp)
OUTPUT
CLOCK GENERATOR (1Hz)
CONTUNITY TESTER
POWER
ON
LOGIC INPUT (12 BIT)


DC DUAL REGULATED
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LED-B
IC 7447
IC 7447
VOLT. CONTROL
DC POWER SUPPLIES
FIXED
+5V.1A
-5V.500mA
PULSE GENERATOR
(1Hz To 1MHz)
MULTIPLIER
FREQUENCY
CONTROL
AMPLITUDE (0-10Vpp)
OUTPUT
CONTUNITY TESTER
POWER
ON
LOGIC INPUT (12 BIT)

<u>D Flip-Flop from NAND:</u>

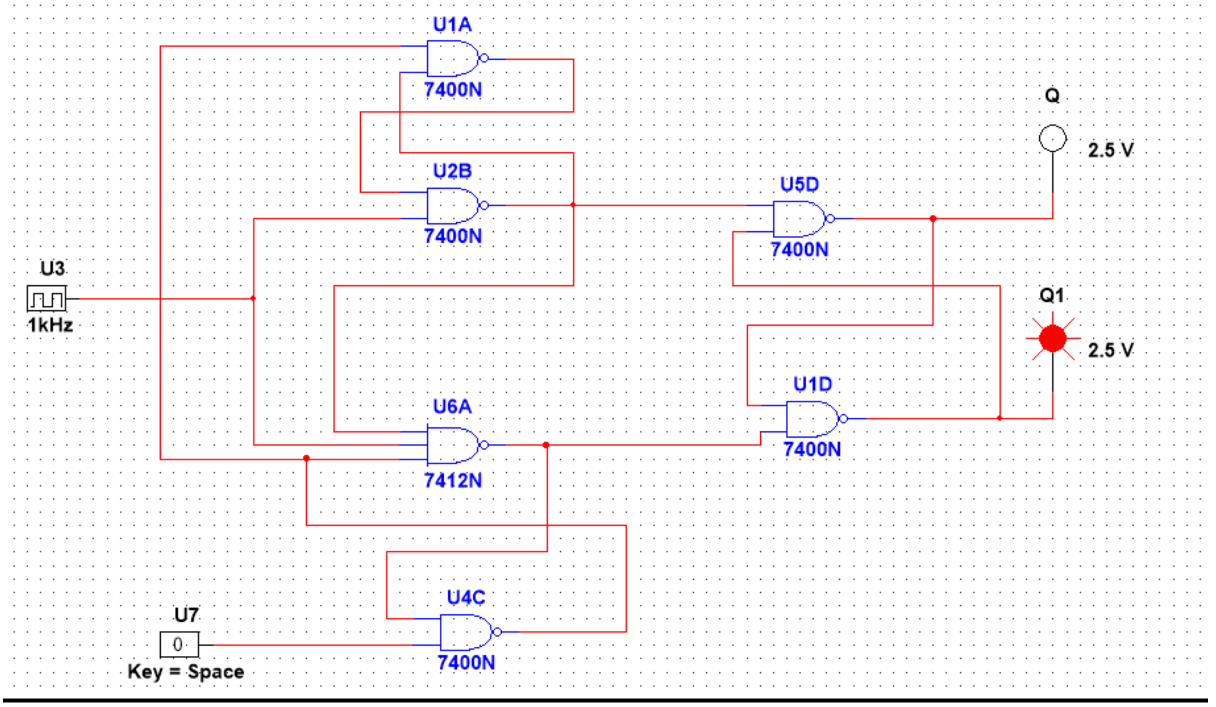


Fig: input – 0; output (Q) – 0

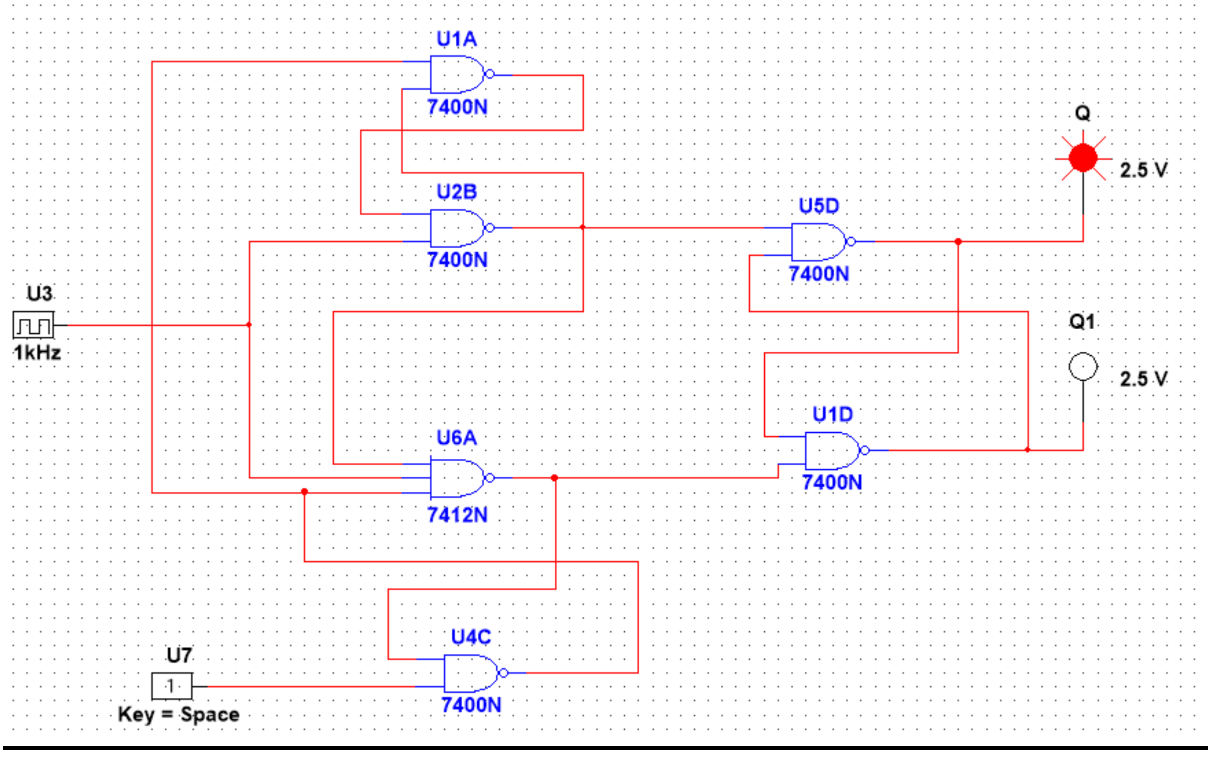


Fig: input – 1; output (Q) – 1

J-K flip-flop

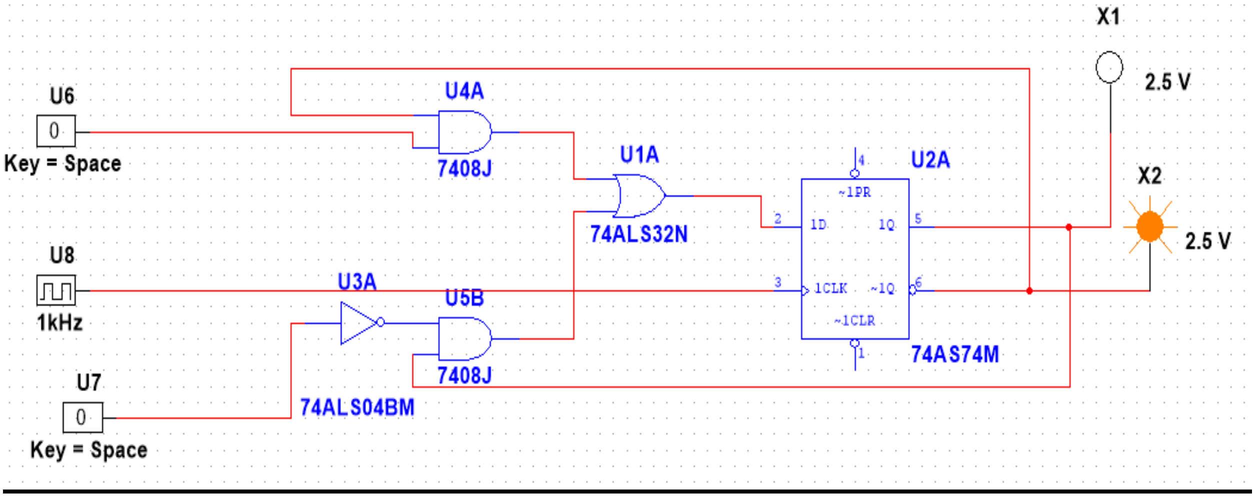


Fig: input – 0 0; output (Q) – 0 (No change)

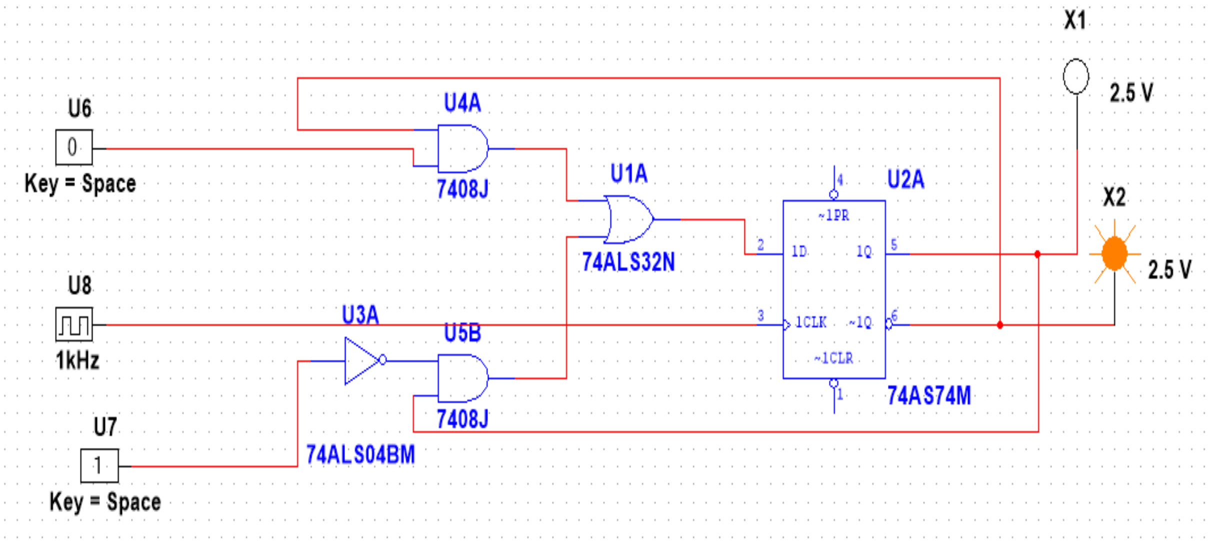


Fig: input – 0 1; output (Q) – 0 (Reset)

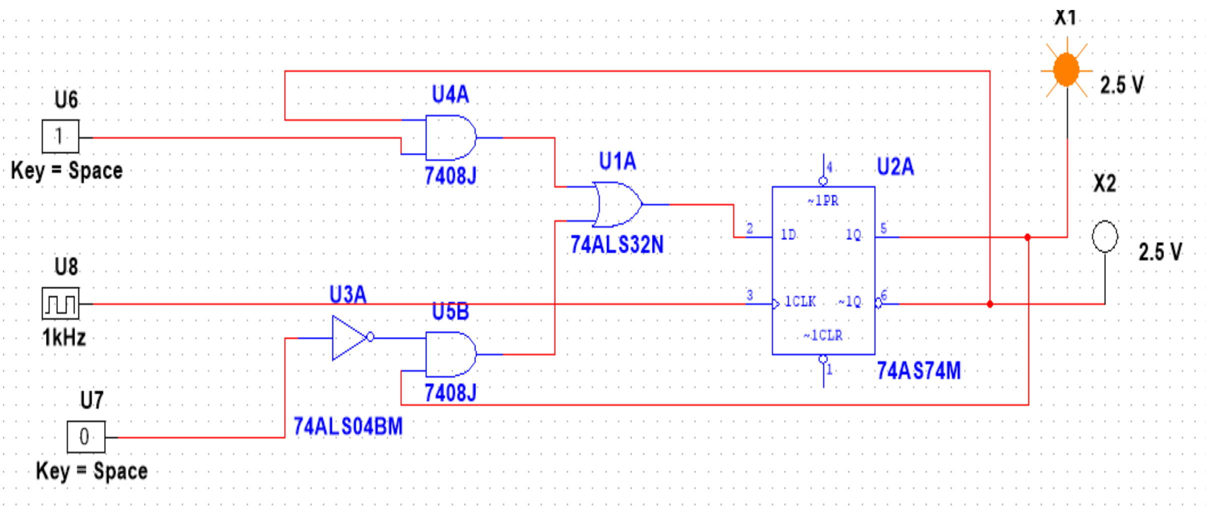


Fig: input – 1 0; output (Q) – 1 (Set)

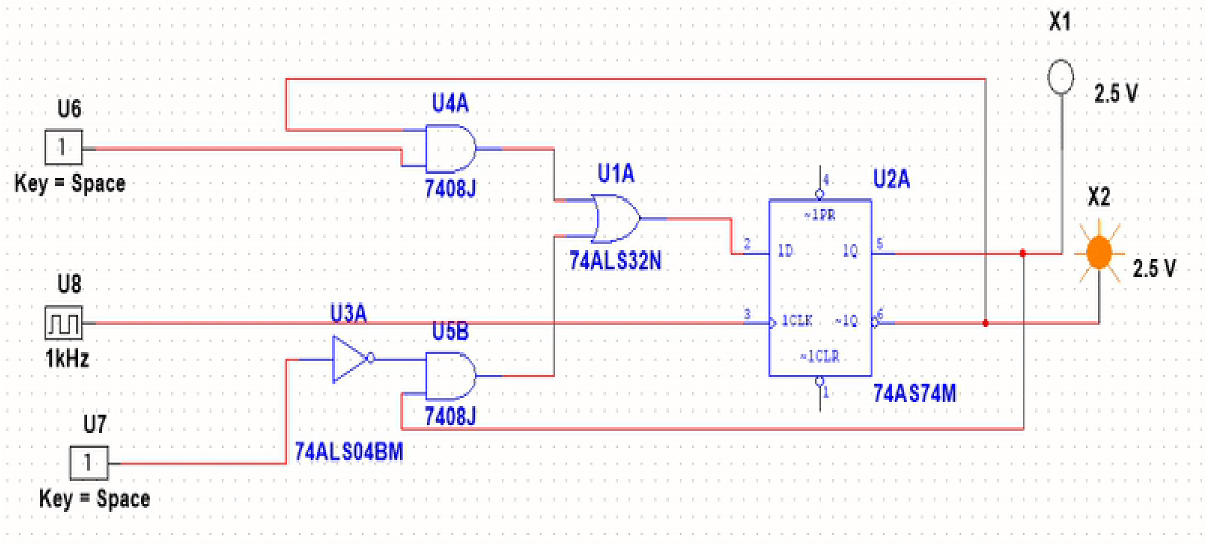


Fig: input – 1 1; output (Q) – 0 (Toggle)

T flip-flop

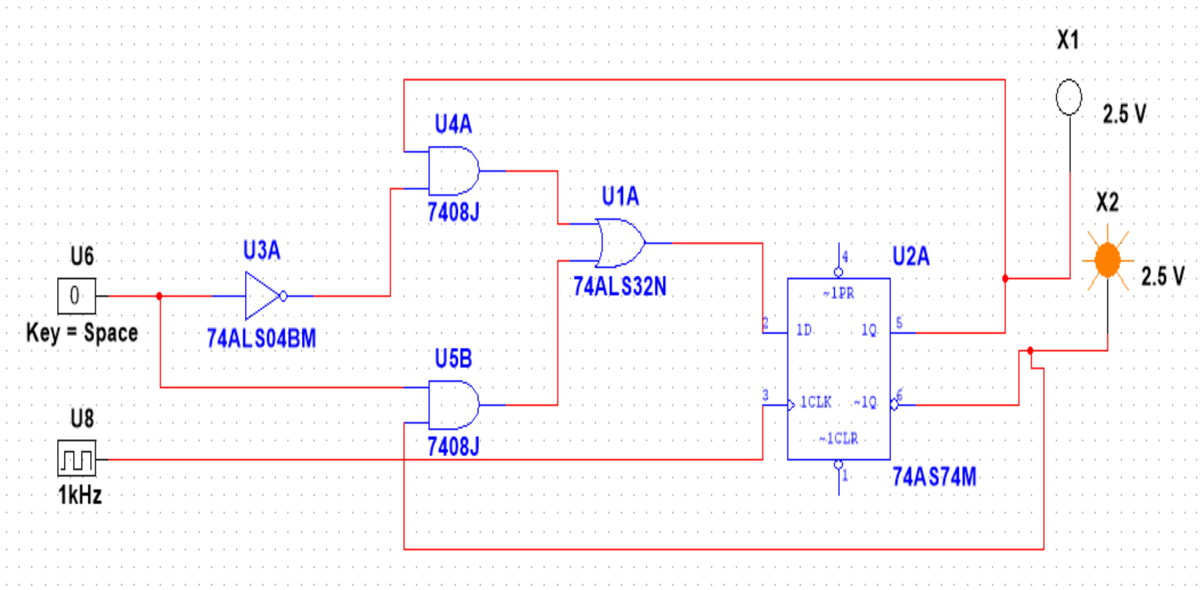


Fig: input – 0 ; output (Q) – 0

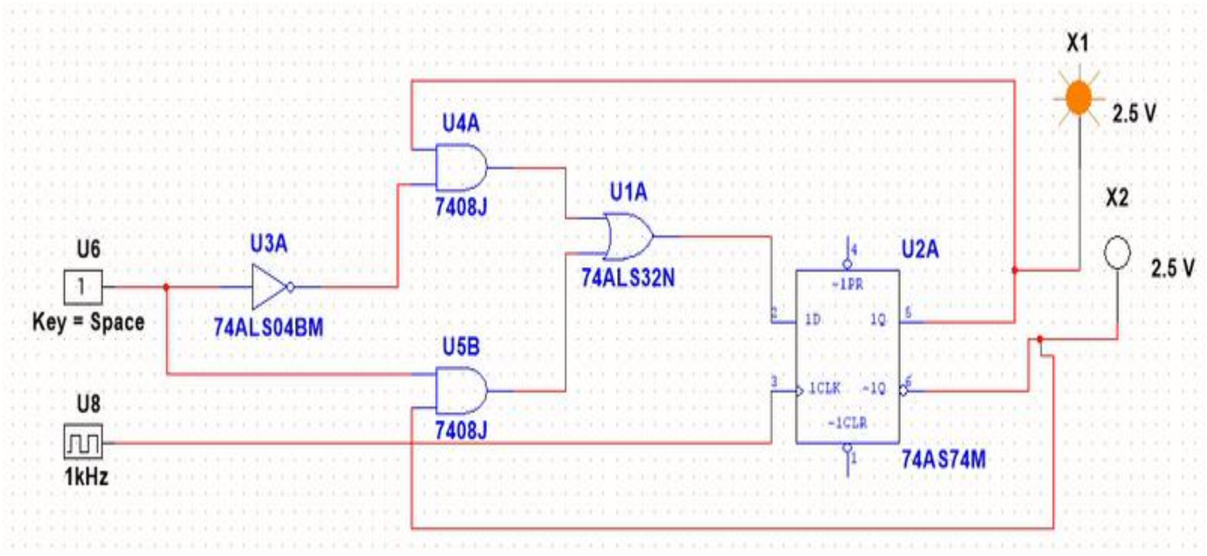
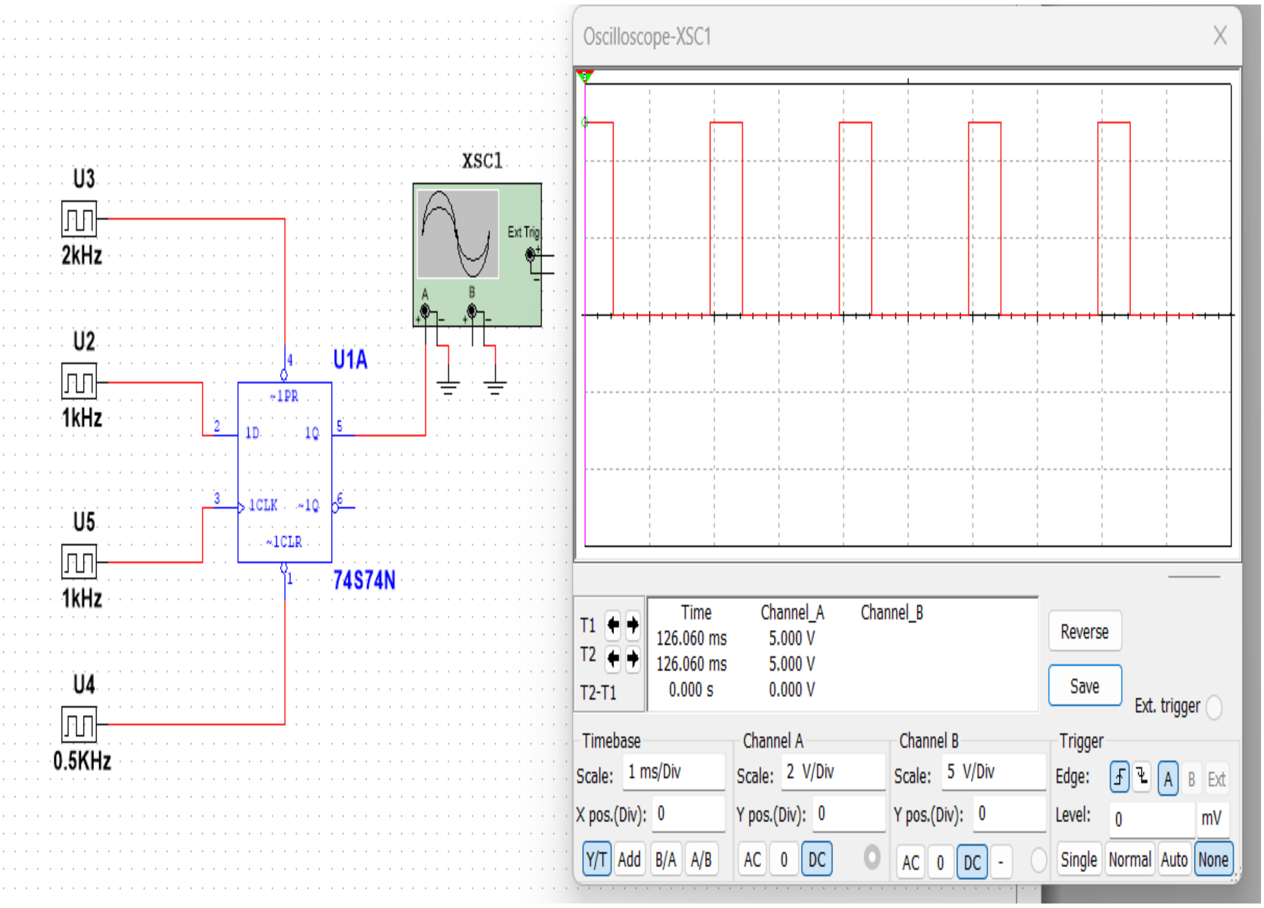


Fig: input – 1 ; output (Q) – 0 (Toggle)

D Flip-Flop



Results: The Simulation results matched the hardware implementation.

Discussion:

After performing this experiment, we became familiar with the design of positive edge triggered D flip-flop with and without 'Preset' and 'Clear' capabilities, J-K flip-flop, and T-flip-flop. After the experiment, our job was to design negative edge-triggered flip-flops and draw the timing diagrams for them. We have also designed and drawn a timing diagram for a D flip-flop having active high 'Preset' and 'Clear' pins.

Reference:

1. "Fundamentals of Digital Logic with verilog design" by – Brown &Vranesic
2. www.wikipedia.org
3. http://www.cs.umd.edu/class/spring2003/cmsc311/Notes/Seq/flip.html