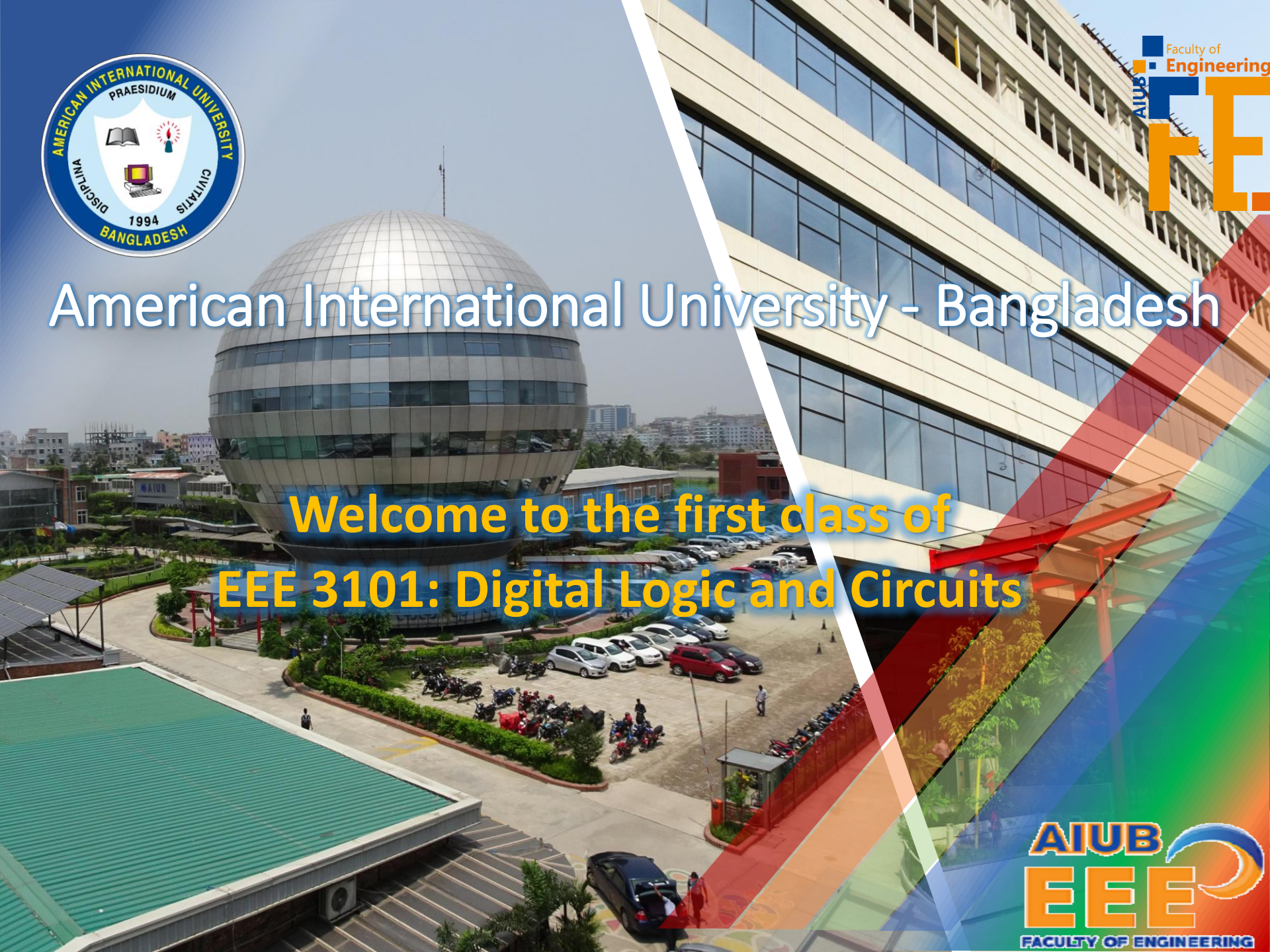
American International University - Bangladesh
Welcome to the first class of
EEE 3101: Digital Logic and Circuits
AIUB
EEE
FACULTY OF ENGINEERING

EEE 3101: Digital Logic and Circuits

Course Teacher: Nafiz Ahmed Chisty

Associate Professor, Department of EEE & CoE
Head (UG), Department of EEE
Faculty of Engineering
Room# DNG03, Ground Floor, D Building
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Teaching and Consulting Schedule

Nafiz A. Chisty| Head (UG), Dept of EEE; Associate Professor, Dept. of EEE & CoE

AMERICAN INTERNATIONAL UNIVERSITY-BANGLADESH (AIUB)
Ka 66/a, Kuratuli Road, Kuril, Dhaka-1229, Bangladesh

TEACHER'S SCHEDULE FORM
Spring Semester, 2022-2023

Day	Sunday	Monday	Tuesday	Wednesday	Thursday
Starting Time	10:00	10:00	10:00	10:00	10:00
Ending Time	18:00	18:00	18:00	18:00	18:00
10:00-10:30	Consulting & Office Hours	Consulting & Office Hours	Consulting & Office Hours	Consulting & Office Hours	Consulting & Office Hours
10:30-11:45	Digital Logic and Circuits Section: M Room# 1116	Digital Logic and Circuits Section: D Room# 1116	Digital Logic and Circuits Section: M Room# 1116	Digital Logic and Circuits Section: D Room# 1116	
11:45-13:00	Digital Logic and Circuits Section: E Room# 1116	Digital Logic and Circuits Section: F Room# 1113	Digital Logic and Circuits Section: E Room# 1116	Digital Logic and Circuits Section: F Room# 1113	
13:00-18:00	Consulting & Office Hours	Consulting & Office Hours	Consulting & Office Hours	Consulting & Office Hours	

Teacher's Name: Nafiz Ahmed Chisty

Designation: Associate Professor, Dept. of EEE & CoE
Head In-Charge (UG), Dept. of EEE

E-mail: chisty@aiub.edu

Consulting Hours:

Sunday	Monday	Tuesday	Wednesday	Thursday
10:00 - 10:30 13:00 - 18:00	10:00 - 10:30 13:00 - 18:00	10:00 - 10:30 13:00 - 18:00	10:00 - 10:30 13:00 - 18:00	10:00 - 18:00

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Academic Calendar*

Spring 2022-2023

2023		
Jan	22	First day of regular classes
	26 & 29	Adding/ Dropping
	26	Automatic conversion of UW, I, blank grades of Fall 2022-23 Semester to F
Feb	16 (Thursday)	Makeup of Sunday Classes
	18 (Saturday)	Makeup of Monday Classes
	7th Week 26 – Mar 2	Laboratory midterm exams
Mar	8th Week 4 – 11	Midterm Exam
	16 (Thursday)	Makeup of Tuesday Classes
	18 (Saturday)	Makeup of Wednesday Classes
	18	Submission of midterm grades
	19 – 23	TPE
	23	Midterm Grades Locked
	25 – 30	Pre-registration for Summer 2022-23 Semester
	*26/ 27	Ramadan Class Timing starts
Apr	*23 / 24	Eid Ul Fitr
	16th Week 30 – May 4	Laboratory Final exams
May	17th Week 6 – 13	Final Exam
	20	Submission of Final Grades
	27	Final Grades Locked
	May 14 -May 27	Semester break Release of grades Registration for Summer 2022-23
	June 22	Automatic conversion of UW, I grades of this semester to F

*AIUB reserves the right to change the academic calendar.

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COURSE OUTLINE

I. Course Core and Title: EEE 3101: Digital Logic and Circuits
II. Credit: 3 credit hours (3 hours of theory per week)
III. Nature: Core Course for EEE
IV. Prerequisite: EEE 2103: Electronic Devices

Objectives:

The objectives of the course can be grouped into two categories.

The first one relates to understanding the basics of Boolean algebra and the operation of logic components, combinational, and sequential circuits.
The second set of objectives relates to the design of digital circuits and systems.

Course Description:

This is core course of Electrical and Electronic Engineering & Computer Engineering program that presents basic tools for the design of digital circuits. It serves as a building block in many disciplines that utilize data of digital nature like digital control, data communication, digital computers etc.

This course is designed to:
Manipulate Boolean algebraic structures, Implement the Boolean Functions using NAND and NOR gates, Simplify the Boolean expressions using Karnaugh Map, Analyze and design various combinational logic circuits, Study of Storage Elements: Introduction to the behavior and structure of latches, flip-flops, and registers, Understand the importance of state diagram representation of sequential circuits, Study Sequential Circuits: Analyze and design clocked sequential circuits, Perform Timing Analysis: Introduction to timing analysis of combinational and sequential circuits. Special characteristics of Digital logic families and their comparative discussion. Definition and Problem solving on Fan out, Noise Margin, Propagation Delay, Power Dissipation, Duty Cycle and Speed Power Product. Diode Logic Gates. Basic Diode Transistor Logic Gates: RTL, DTL, Modified DTL and HTL with operational detail.

MOS and CMOS Logic with operational detail. Basic memory units and operations. Memory system: RAM Family. Memory System: ROM Family. Memory System: Flash Memory, Magnetic storage, USB Flash Drive, SSD hard drive. DSP basics: Sample and Hold circuits. Digital to Analog Conversion with application. Analog to Digital Conversion with application. Operation and Mathematical operation of 555 integrated timer circuit: Monostable, Astable multi-vibrator. Charge Coupled Device (CCD)and LCD. Introduction to Programmable Logic Devices (PLDs): Advantages & disadvantages over discrete logic gates, Implementation of digital circuits using PLDs (using PAL and PLA).

Course Outcomes

COs/CLOs	Details	K	P	A	Assessed Program Outcome Indicator	BNQF Indicator	Assessment Techniques
CO1	Construct digital combinational logic circuits (adder, magnitude comparator, encoder, decoder, multiplexer, demultiplexer) applying appropriate techniques at gate level and transistor level (RTL, DTL, TTL, CMOS) for conflicting requirements of complex engineering problem.	3	P1 P2 P6		P.a.3.C3	FS.1	Quiz
CO2	**Develop a system with 555 timer and transistors for conflicting requirements of complex engineering problem.**	**3**	**P1 P2 P6**		**P.a.3.C3**	**FS.1**	**In Class Assignment**
CO3	Construct sequential logic circuits (latches, flipflops) applying appropriate techniques for conflicting requirements of complex engineering problem..	3	P1 P2 P6		P.a.3.C3	FS.1	Quiz
CO4	Apply information and concepts of conversion of signals for a complex engineering problem.	4	P1, P3, P7		P.a.4.C3	N/A	Quiz

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Topics to be covered*:

Week	Topics
1	• Objective of DLC course. • Introduction to Integrated Circuit (IC). • Special Characteristics of digital logic families. • Binary Logic, Logic gates and their truth table. • Logic Gates using: DL, RTL, DTL, HTL, MOS and CMOS • Logic family mathematical problems
2	• Boolean algebra, Simplification using Boolean Algebra. • Implementing circuit from Boolean expressions • De-Morgan's law. • Universal gates and their applications.
3	• Canonical forms-maxterms and minterms. Sum of Product (SOP) and Product of Sum (POS) form. • Boolean expression in Simplifying using K – map.
4	• Adders • Magnitude Comparators.
5	• Decoders, • Encoders, Priority Encoders, • Cascading of Decoders, Encoders
6	• Multiplexers, De-Multiplexer • Boolean Function implementation using Multiplexers, • Cascading of Multiplexers, De-Multiplexers
7	**MID-TERM WEEK**

* The faculty reserves the right to change, amend, add or delete any of the contents.

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Week	Topics
8	• Sequential Logic circuit: Latches, Flip – flops • Timing Diagram.
9	• Counters: Asynchronous and Synchronous counters. • Modulus Counters, Binary Up-Down counter, Ripple Counter
10	• Designing Irregular Counters using State Diagram and State Equation. • Shift registers • Shift register Counters: Johnson counter, Ring counter
11	• Memory Systems: read, write operations • RAM family, ROM family • Flash memory programming, read & erase operation. Magnetic Storage: Hard Disk Drive (HDD), SSD R-L transient: Storage cycle; Related Problems.
12	• Operation of 555 integrated timer circuit: Monostable, Astable multivibrator • Introduction to Programmable Logic Devices (PLDs): Advantages and disadvantages of PLDs over discreet logic gates. • Classification of PLDs
13	• Digital Signal Processing Basics, Sample and Hold Circuits. Different types of A/D Converter with application • Different types of D/A converter with application.
14	**FINAL-TERM WEEK**

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Textbooks/ References

Textbooks:

[1] Thomas L. Floyd, “Digital Fundamentals” 9th edition, Prentice Hall.
[2] M. Morris Mano, “Digital Logic & Computer Design” Prentice Hall.

References:

[1] Ronald J. Tocci & Neal S. Widmer, “Digital Systems” 7th edition, Prentice Hall.
[2] Digital design – Karim and Johnson
[3] Brian Holdsworth and Clive Woods, “Digital Logic Design”-Fourth Edition.
[4] Stephen Brown and Zvonko Vranesic, “Fundamentals of Digital Logic with VHDL Design with CD-ROM”
[5] William J. Dally and R. Curtis Harting, “Digital Design: A Systems Approach”
[6] Victor P. Nelson, H. Troy Nagle, Bill D. Carroll and David Irwin, “Digital Logic Circuit Analysis and Design”
[7] John P. Hayes, “Introduction to Digital Logic Design”
[8] Norman Balabanian and Bradley Carlson, “Digital Logic Design Principles”
[9] Enoch O. Hwang, “Digital Logic and Microprocessor Design with VHDL”
[10] Joseph Cavanagh, “Digital Computer Arithmetic: Design and Implementation (Computer Science)”

Course Requirements

At least **80%** class attendance and submission of ALL assignment/homework **within** the deadline decided by the course teacher is necessary.

Evaluation

Marking system For Theory Classes (Midterm)	
Attendance	10%
Midterm: Assignment (Not OBE)	10%
Quiz (Best 2 out of 3)	40%
Midterm: Written	40%
Total	100%

Marking system For Theory Classes (Final term)	
Attendance	10%
Final term: OBE assessed assignment	30%
Quiz (Best 1 out of 2)	10%
Final term: Written	30%
Project presentation + Viva (max. 5 members)	20%
Total	100%

Final Grade/ Grand Total: - - - - - - - 40% of Midterm + 60% of Final Term

COs and POs Assessment

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COs Assessment Tools for Mid-Term

Assessment Tools	CO/CLO 1 Marks	CO/CLO 2 Marks	CO/CLO 3 Marks	Marks for Grading
Attendance	N/A	N/A	N/A	10
Quiz	N/A	N/A	N/A	40
Assignment	N/A	N/A	N/A	10
Midterm Exam	N/A	N/A	N/A	40
Total				**100**

COs Assessment Tools for Final-Term

Assessment Tools	CO/CLO 1 Marks	CO/CLO 2 Marks	CO/CLO 3 Marks	Marks for Grading
Attendance	N/A	N/A	N/A	10
Quiz	N/A	N/A	N/A	10
Assignment	N/A	N/A	**30**	**30**
Presentation	N/A	N/A	N/A	20
Final Exam	N/A	N/A	N/A	30
Total				**100**

Total P.a.3.C3 Marks from midterm and final term: 30

Assessment rationale:

The examinations will consist of questions regarding topics mentioned in the class schedule.

Quiz

- Each quiz mark is 20.
- No makeup quiz will be taken. (You have to be serious from first to last)
- Quiz script will be cancelled, if students do any cheating and if students do not write his/her name and ID on the top of quiz paper.

Attendance

- At least 80% presence is necessary.
- Late in Class:10 minutes from the time of start of the class, full attendance. Otherwise late marking. (2 late is equal to one absent).
- Students must inform the course teacher regarding his/her absence **before** class through e-mail, MS Teams, or via guardian/friend/family to the course teacher.
- **If your attendance is very poor**, it will be informed to **OSA** and they **will contact with your guardian**.

Assignment and VIVA

- There might be 2/3 assignments (OBE/non-OBE) and Viva.

Teaching Method

- Maximum topics will be covered from the textbook. For the rest of the topics, reference books will be followed. Some Class notes will be uploaded on the web.
- Students must study up to the last lecture before coming to the class and it is suggested that they should go through the relevant chapter before coming to the class. Just being present in the class is not enough- students must participate in classroom discussions.
- Formal lectures will provide the theoretical base for the subject as well as covering its practical application.
- A set of lecture notes, tutorial examples, with subsequent discussion and explanation, together with suggested reading will support and direct the students in their own personal study.
- Few assignments will be given to the students based on that class to test their class performance.

Teaching Materials

- Teacher would post the syllabus and the lecture notes on the course webpage in VUES.
- Students must store the teaching materials and the course outline/syllabus, as these might be required in future, especially for admission for higher studies.

Missing Evaluations

- Makeup for missing Quiz/Assignment/ etc… will be considered only through valid application procedures with pure evidence of reasoning.
- Student missing less than 40% of the total evaluation for each term (mid/final) will be given 'I' (incomplete) grade along with a strict deadline to complete the missing evaluations by the course teacher.
- Student missing more than 40% of the total evaluation for each term (mid/final), will be given 'UW' (Unofficial Withdraw) grade. Students must go through valid application procedures with pure evidence of reasoning to change 'UW' to 'I'.
- Except extreme cases (accident/hospitalized etc.), marks for attendance will not be considered. On extreme cases, partial/full marks (*judged by the course teacher*) may be given to the student.

During Class

- Students are encouraged to ask question at any moment during the lecture,
- The teacher might ask question to students,
- Students must have active headphone or mic/speaker,
- Teachers will randomly ask the students to share the desktop for checking student activity/ question's answer.

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Consultation

- Students are Encouraged to use e-mail/ MS Teams to communicate with the teacher for Consultation.
- You may communicate during the consulting hours of the teacher or at any time you feel comfortable. The teacher will revert back at his earliest possible time.
- Group/one-to-one consultation both are allowed.

Important Dates: Midterm

For Sections: M & E (Sunday-Tuesday class)

Quiz No.*	Date*	Syllabus*	
		Uploaded Slide No.	Book Chapter (Floyd 9th Edition)
Quiz 1	February 19, 2023	4a_Boolean Algebra	Chapter 4
Quiz 2	February 26, 2023	5_Universal Gates, 6_Adders_subtractors, & 7_Magnitude Comparator	Chapter 3, 5, 6
Quiz 3	February 28, 2023	8_Decoder_Encoder	Chapter 6
Assignment	March 02, 2023	All	Chapters 2,3,4,5 & 6

For Sections: D & F (Monday-Wednesday class)

Quiz No.*	Date*	Syllabus*	
		Uploaded Slide No.	Book Chapter (Floyd 9th Edition)
Quiz 1	February 20, 2023	4a_Boolean Algebra	Chapter 4
Quiz 2	February 27, 2023	5_Universal Gates, 6_Adders_subtractors, & 7_Magnitude Comparator	Chapter 3, 5, 6
Quiz 3	March 01, 2023	8_Decoder_Encoder	Chapter 6
Assignment	March 02, 2023	All	Chapters 2,3,4,5 & 6

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Important Dates: Final term

For Sections: M & E (Sunday-Tuesday class)

Quiz No.*	Date*	Syllabus*		Details
		Uploaded Slide No.	Book Chapter (Floyd 11th Edition)	
Quiz 1	April 11, 2023	2_Counters	Chapter 7 & 9	Offline mode
Quiz 2	April 16, 2023	3_Shift Registers	Chapter 8, 10 & 11	Offline mode
OBE Assignment	April 30, 2023	4_555Timer	Chapter 7	VUES (valid till 11:45PM)
Project Presentation Slide submission	April 30, 2023	All	Chapter 7, 8, 9, 10, 11 & 12	Link: https://forms.office.com/r/BaW0FWeWdi (valid till 11:45PM)
Project Presentation & VIVA	May 02, 2023			Offline mode

For Sections: D & F (Monday-Wednesday class)

Quiz No.*	Date*	Syllabus*		Details
		Uploaded Slide No.	Book Chapter (Floyd 11th Edition)	
Quiz 1	April 12, 2023	2_Counters	Chapter 7 & 9	Offline mode
Quiz 2	April 17, 2023	3_Shift Registers	Chapter 8, 10 & 11	Offline mode
OBE Assignment	April 30, 2023	4_555Timer	Chapter 7	VUES (valid till 11:45PM)
Project Presentation Slide submission	April 30, 2023	All	Chapter 7, 8, 9, 10, 11 & 12	Link: https://forms.office.com/r/BaW0FWeWdi (valid till 11:45PM)
Project Presentation & VIVA	May 02, 2023			Offline mode

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Thanks


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