AMERICAN INTERNATIONAL UNIVERSITY–BANGLADESH (AIUB)

FACULTY OF SCIENCE & TECHNOLOGY

DIGITAL LOGIC AND CIRCUITS LAB

Summer 2022-2023

Section: F
Group Number: 02

EXPERIMENT NO. 2

NAME OF THE EXPERIMENT

Deriving logic equations and truth tables from a given statement or expression and construction of combinational circuits

Supervised By

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Submitted By:

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Abstract:

This experiment aims to learn how to implement the logic circuits in the breadboard from a given statement. Familiar with Boolean algebra and De Morgan's law. Finally, how to simplify a logic expression using K-Map and verify accuracy in the breadboard.

Introduction:

We can construct a digital logic circuit using the given logical statement. This involves creating a truth table and determining whether it follows the typical SOP (sum of products) or POS (product of sums) form. By examining the individual logic operations and matching them with their respective logic gates, we can extract a logic expression from the combinational circuit design. These expressions can be simplified using techniques such as Boolean algebra, De Morgan's law, or K-Map, which help minimize the number of required gates. The circuit can then be implemented on a breadboard using gate ICs, and the output can be observed to verify if it matches the truth table of the provided statement.

Theory:

Boolean algebra: In Boolean algebra, a variable is a symbol that represents an action, circumstance, or information. It can take on only two possible values: 1 and 0.

Sum of Products (SOP): When two or more product terms are summed by Boolean addition, the resulting expression is a sum of product. Ex. Implementing an SOP expression simply requires ORing the outputs of two or more AND gates. A product term is produced by an AND operation, and the sum (addition) of two or more product terms is produced by an OR operation. Therefore, an SOP expression can be implemented by AND-OR logic in which the outputs of a number (equal to the number of product terms in the expression) of AND gates connect to the inputs of an OR gate. A standard SOP expression is one in which all the variables in the domain appear in each product term. Ex. Standard SOP expressions are important in constructing truth-tables and in Karnaugh map simplification method. The SOP expression is equal to 1 only if one or more of the product terms in the expression is equal to 1.

Product of Sums (POS): When two or more sum terms are multiplied, the resulting expression is a product of sums (POS). Ex. Implementing a POS expression simply requires ANDing the outputs of two or more OR gates. A sum term is produced by an OR operation, and the product of two or more sum terms is produced by an AND operation. Therefore, a POS expression can be implemented by logic in which the outputs of a number (equal to the number of sum terms in the expression) of OR gates connect to the inputs of an AND gate. A standard POS expression is one in which all the variables in the domain appear in each sum term in the expression. Ex. A POS expression is equal to 0 only if one or more of the sum terms in the expression is equal to 0.

Karnaugh Map: A Karnaugh map provides a systematic method for simplifying Boolean expressions and, if properly used, will produce the simplest SOP or POS expression possible le, known as the minimum expression. A Karnaugh map is similar to a truth table because it presents all of the possible values of input variables and the resulting output of each valued. Instead of

being organized into columns and rows like truth table, the Karnaugh map is an array of cells in which each cell presents binary value of the input variables. The cells are arranged in a way so that the simplification of a given expression is simply a matter of properly grouping the cells. Karnaugh maps can be used for expressions with two, three, four and five variables. The number of cells in a Karnaugh map is equal to the total number of possible input variable combinations as is the number of rows in a truth table.

Apparatus:

1. Digital trainer board.
2. IC 7432:1 pcs
3. IC 7408:1 pcs
4. IC 7404:2 pcs
5. IC 7402:1 pcs
6. IC 7400:1 pcs
7. IC 7486:1 pcs
8. Connecting wires.

Calculation:

Problem 1:

Truth Table

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Standard SOP expression:

Y = A’B’C’D + A’B’CD + A’BC’D + A’BCD’ + A’BCD + AB’C’D + AB’CD’ + AB’CD + ABC’D + ABCD’ + ABCD

Y = (A+B) C + D

Problem 2:

Y = (AB+AC)'+A'B'C

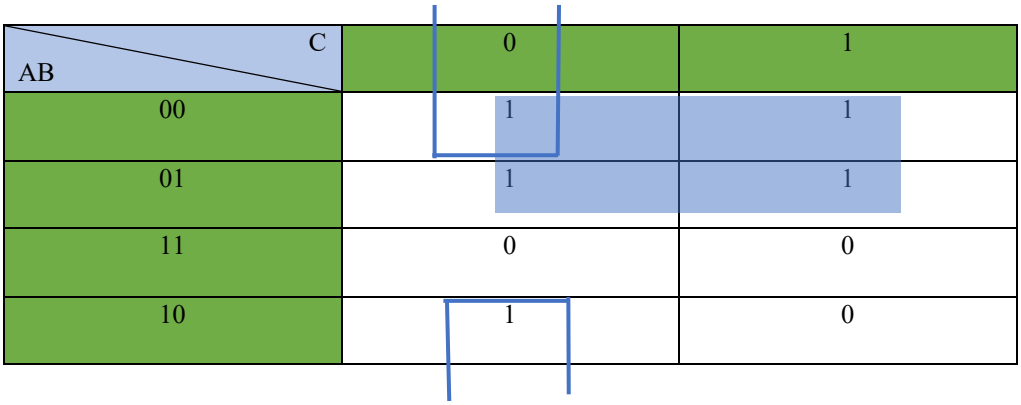
= A'+B'C'+A'B'C

= A'B'C' + A'B'C + A'BC' + A'BC + AB'C' **[standard SOP Expression]**

Truth Table

A	**B**	**C**	**Y**
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

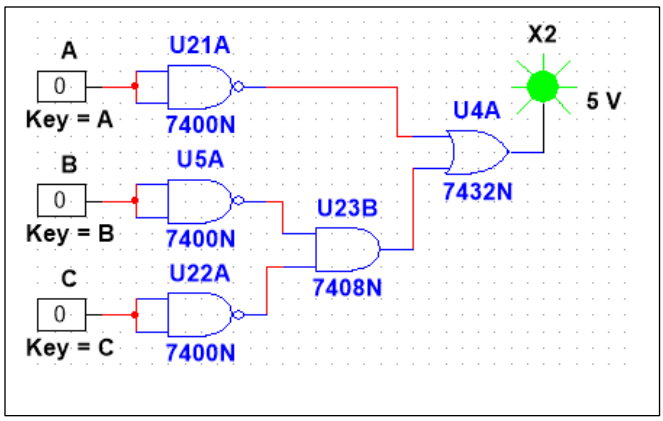
K-Map:

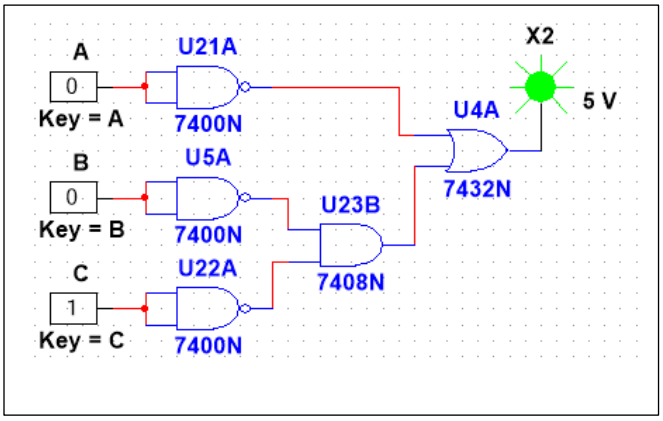


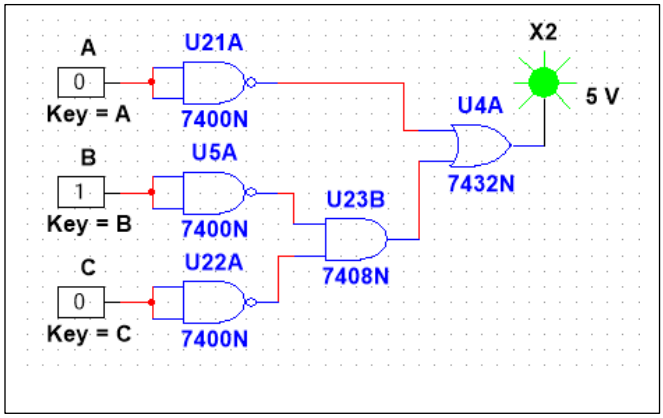
Y = A' + B'C'

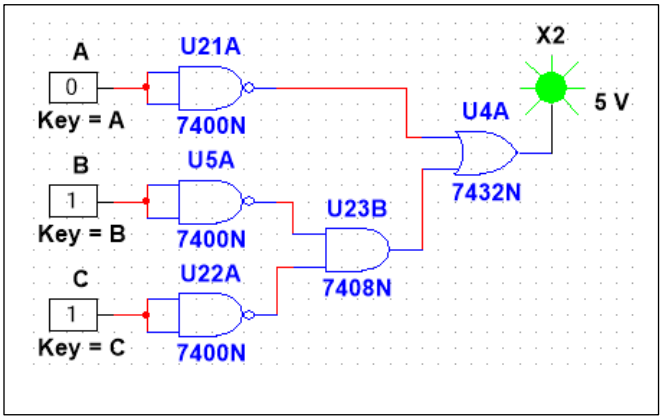
Simulation:

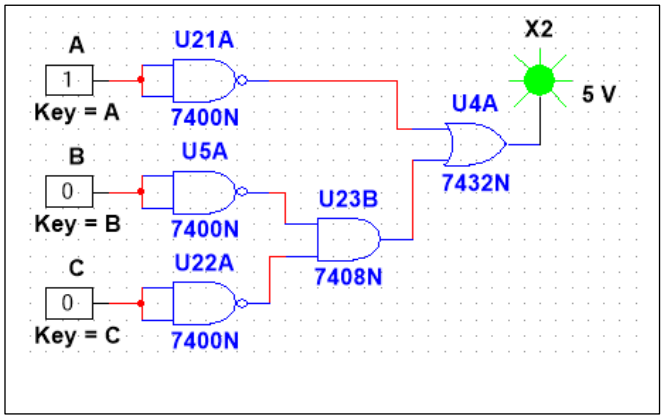
Problem 2





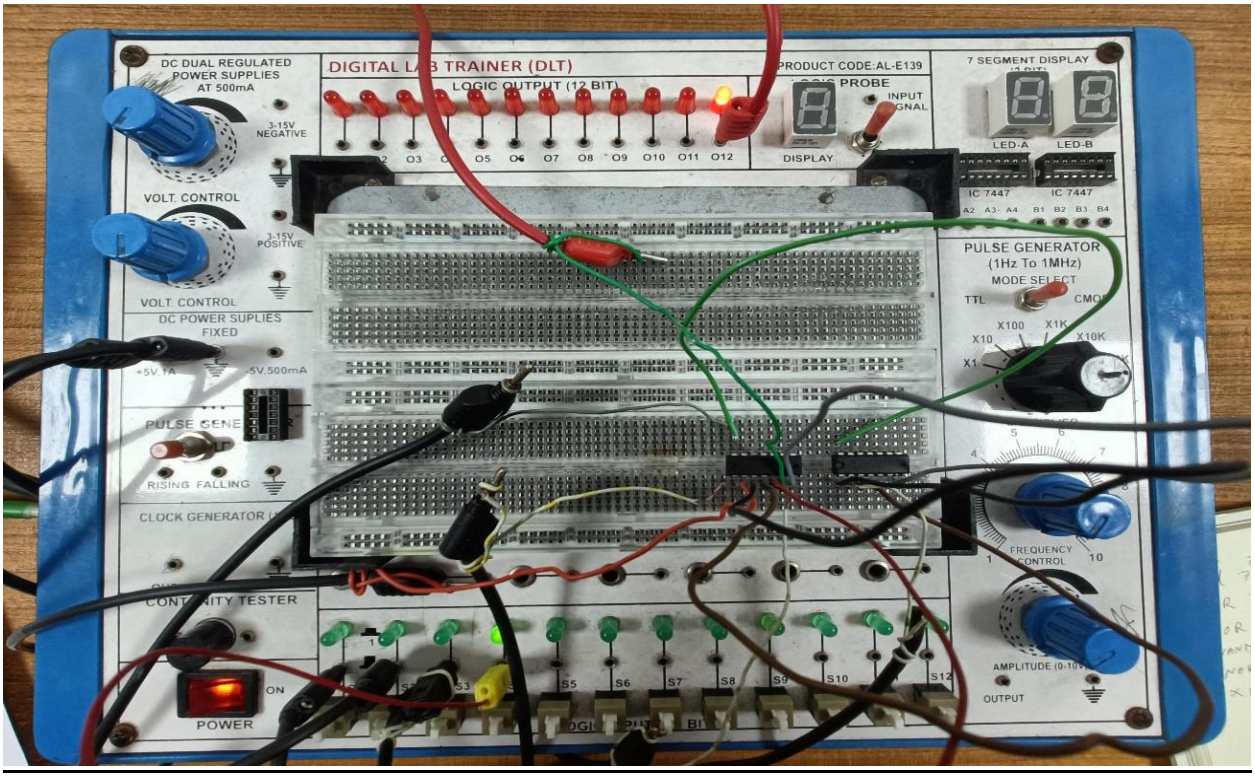


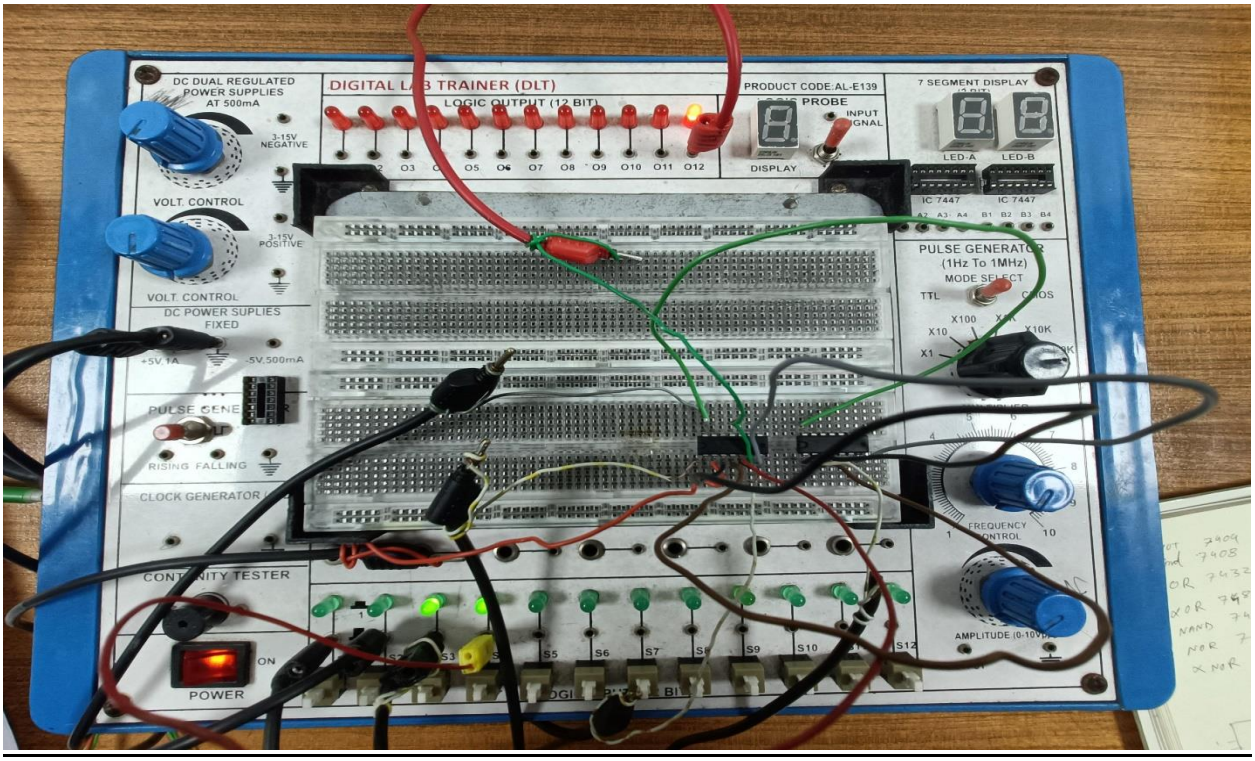


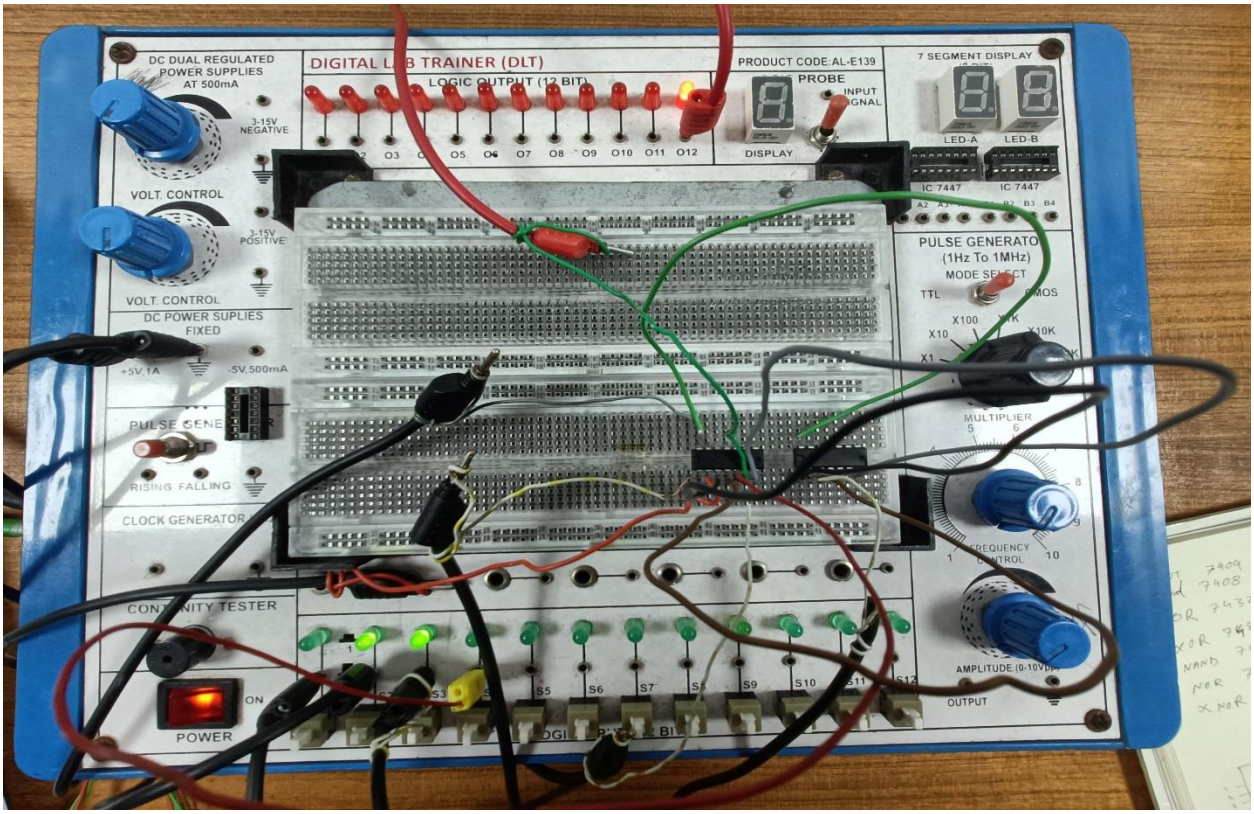


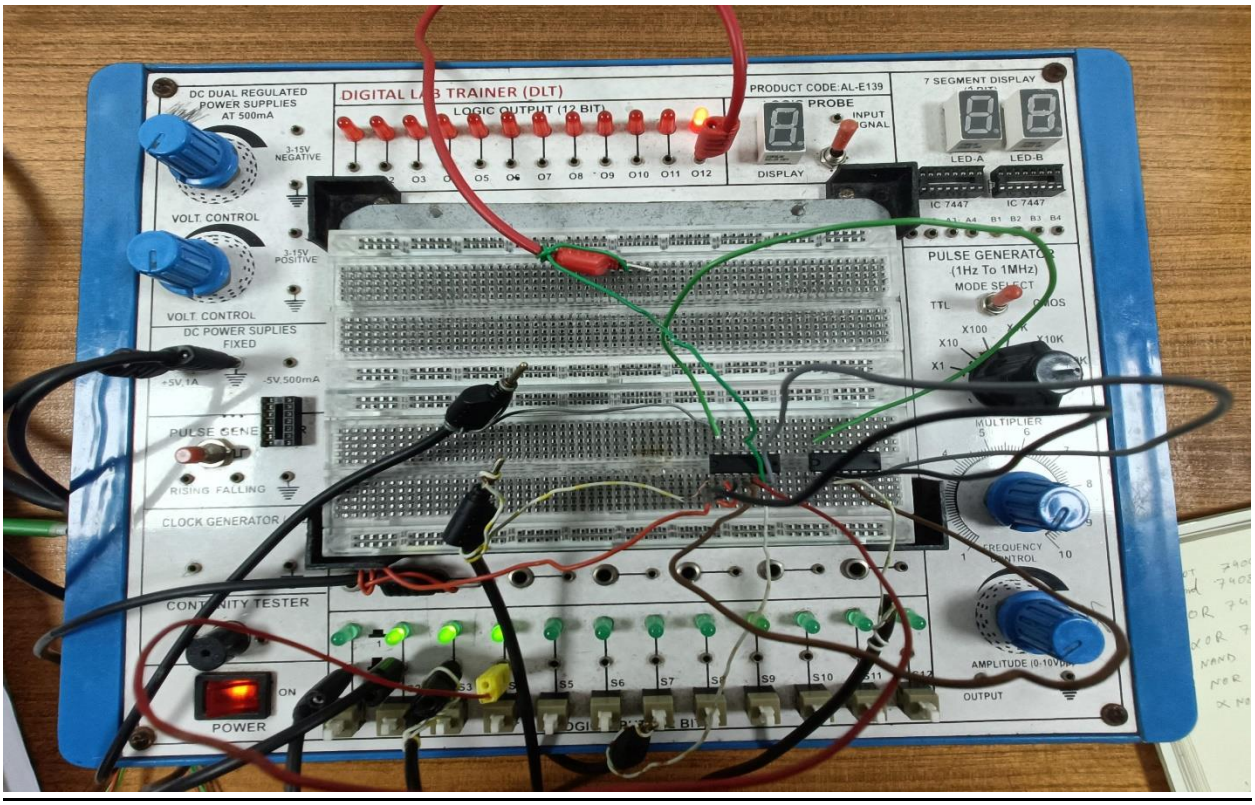
Hardware Implementation:

Problem-1






DC DUAL REGULATED POWER SUPPLIES AT 500mA
3-15V NEGATIVE
VOLT. CONTROL
3-15V POSITIVE
VOLT. CONTROL
DC POWER SUPLIES FIXED
+5V,1A
-5V,500mA
RISING FALLING
CLOCK GENERATOR
POWER
ON
DIGITAL LAB TRAINER (DLT)
LOGIC OUTPUT (12 BIT)
PRODUCT CODE:AL-E139
PROBE
INPUT SIGNAL
DISPLAY
7 SEGMENT DISPLAY
LED-A
LED-B
IC 7447
IC 7447
PULSE GENERATOR
(1Hz To 1MHz)
MODE SELECT
TTL
CMOS
X100
X10
X1
X10K
MULTIPLIER
FREQUENCY CONTROL
AMPLITUDE (0-10VDC)
OUTPUT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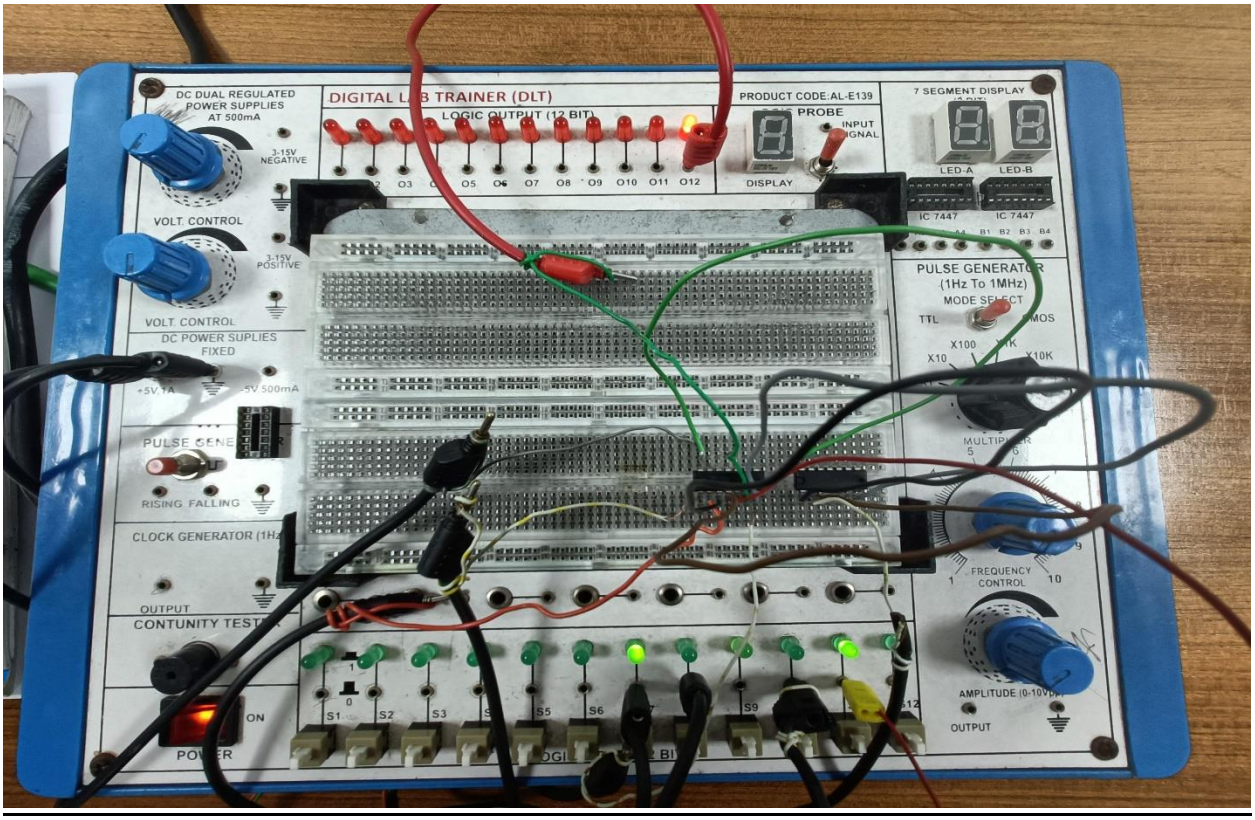
3-15V NEGATIVE
VOLT. CONTROL
3-15V POSITIVE
VOLT. CONTROL
DC POWER SUPLIES FIXED
+5V,1A
-5V,500mA
RISING FALLING
CLOCK GENERATOR
POWER
ON
LOGIC OUTPUT (12 BIT)
PRODUCT CODE:AL-E139
PROBE
INPUT SIGNAL
DISPLAY
LED-A
LED-B
IC 7447
IC 7447
(1Hz To 1MHz)
MODE SELECT
TTL
CMOS
X100
X10
X1
X10K
MULTIPLIER
FREQUENCY CONTROL
OUTPUT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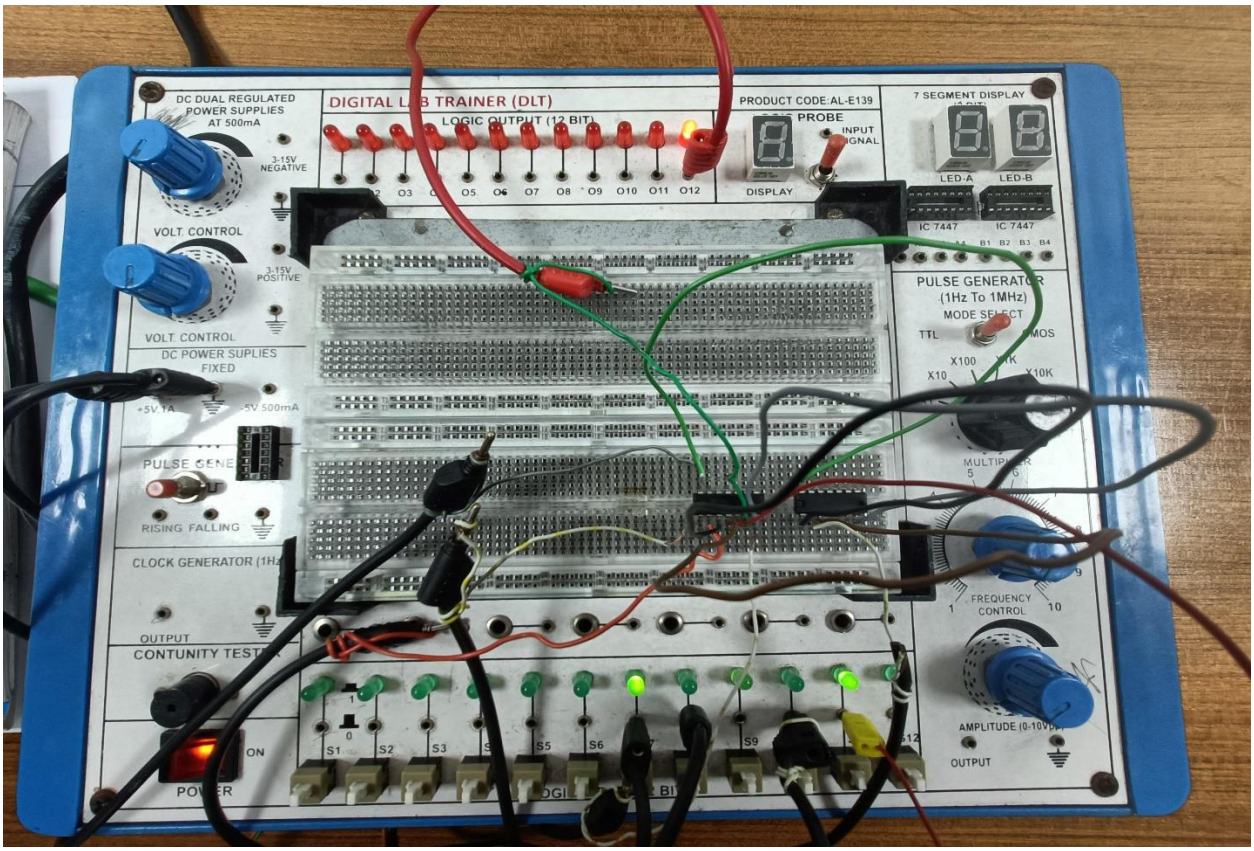
DIGITAL LAB TRAINER (DLT)
LOGIC OUTPUT (12 BIT)
PRODUCT CODE:AL-E139
PROBE
DISPLAY
7 SEGMENT DISPLAY
LED-A
LED-B
IC 7447
IC 7447
VOLT. CONTROL
VOLT. CONTROL
DC POWER SUPLIES FIXED
PULSE GENERATOR (1Hz To 1MHz)
MODE SELECT
TTL
CMOS
RISING FALLING
CLOCK GENERATOR
OUTPUT
CONTUNITY TEST
FREQUENCY CONTROL
AMPLITUDE (0-10Vpp)
OUTPUT
ON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VOLT. CONTROL
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MODE SELECT
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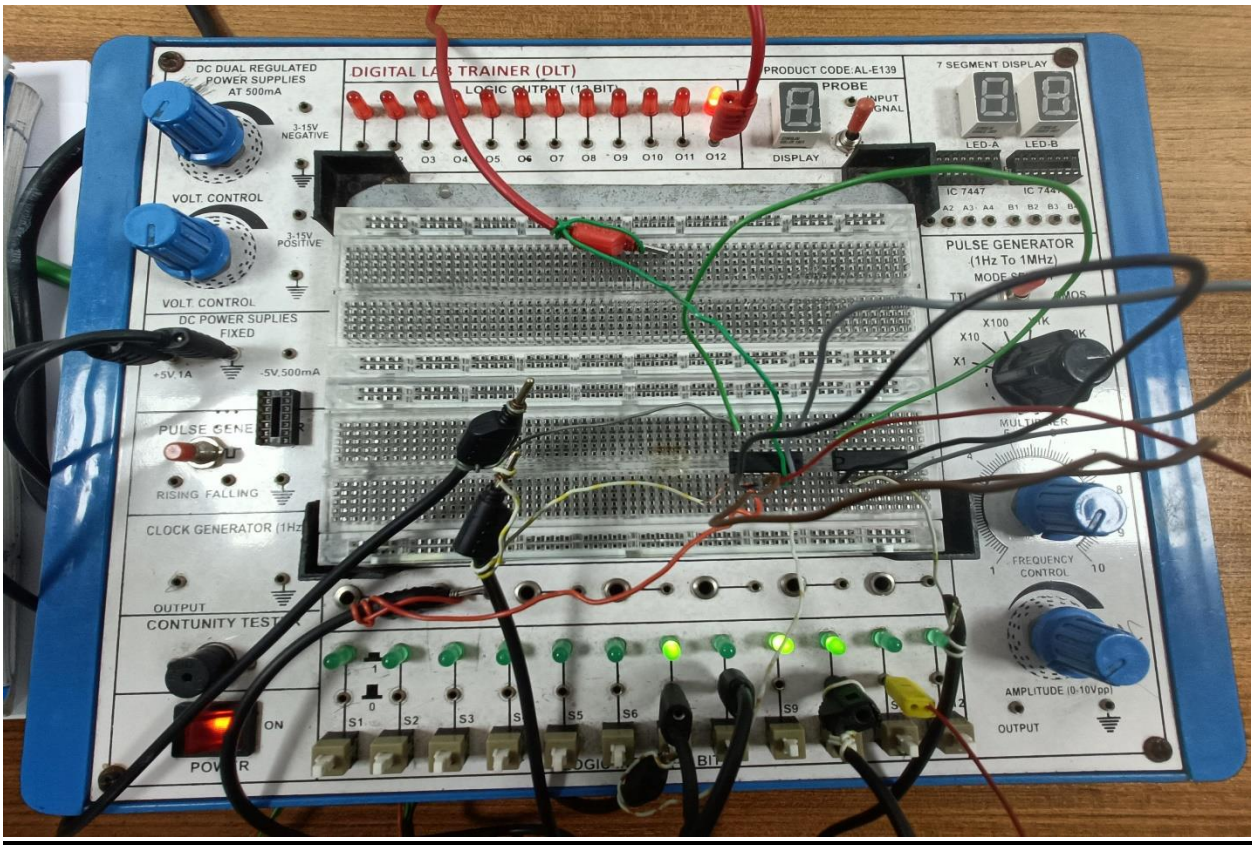
RISING FALLING
CLOCK GENERATOR
OUTPUT
CONTUNITY TEST
FREQUENCY CONTROL
AMPLITUDE (0-10Vpp)
OUTPUT
ON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3-15V NEGATIVE
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VOLT. CONTROL
DC POWER SUPLIES FIXED
+5V 1A
-5V,500mA
PULSE GENE
RISING FALLING
CLOCK GENERATOR (1Hz
OUTPUT
CONTUNITY TEST
ON
POWER
DIGITAL LAB TRAINER (DLT)
LOGIC OUTPUT (12 BIT)
O3 O4 O5 O6 O7 O8 O9 O10 O11 O12
PRODUCT CODE:AL-E139
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PULSE GENERATOR
(1Hz To 1MHz)
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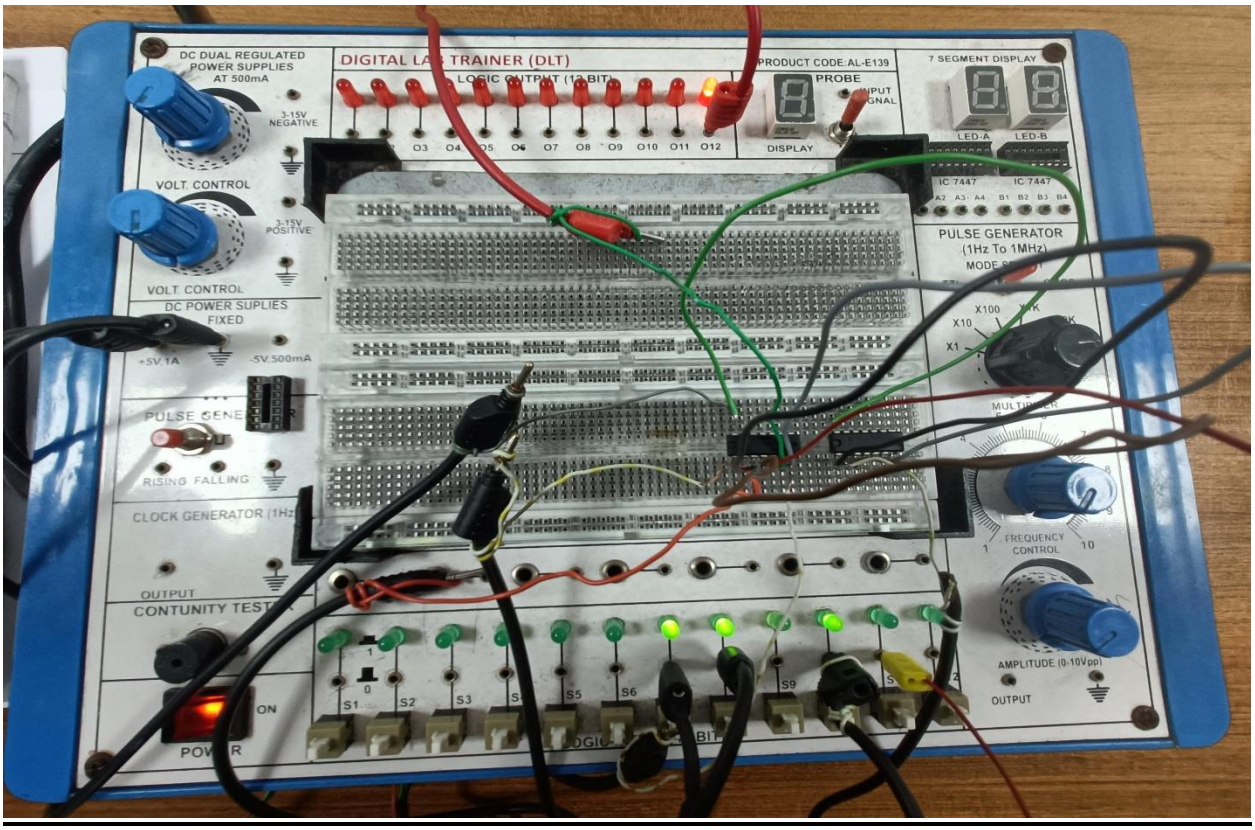
X10
X1
FREQUENCY CONTROL
AMPLITUDE (0-10Vpp)
OUTPUT
S1
S2
S3
S5
S6
S9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VOLT. CONTROL
DC POWER SUPLIES FIXED
+5V 1A
-5V 500mA
PULSE GENE
RISING FALLING
CLOCK GENERATOR (1Hz
OUTPUT
CONTUNITY TEST
ON
POWER
DIGITAL LAB TRAINER (DLT)
LOGIC OUTPUT (12 BIT)
O3 O4 O5 O6 O7 O8 O9 O10 O11 O12
PRODUCT CODE:AL-E139
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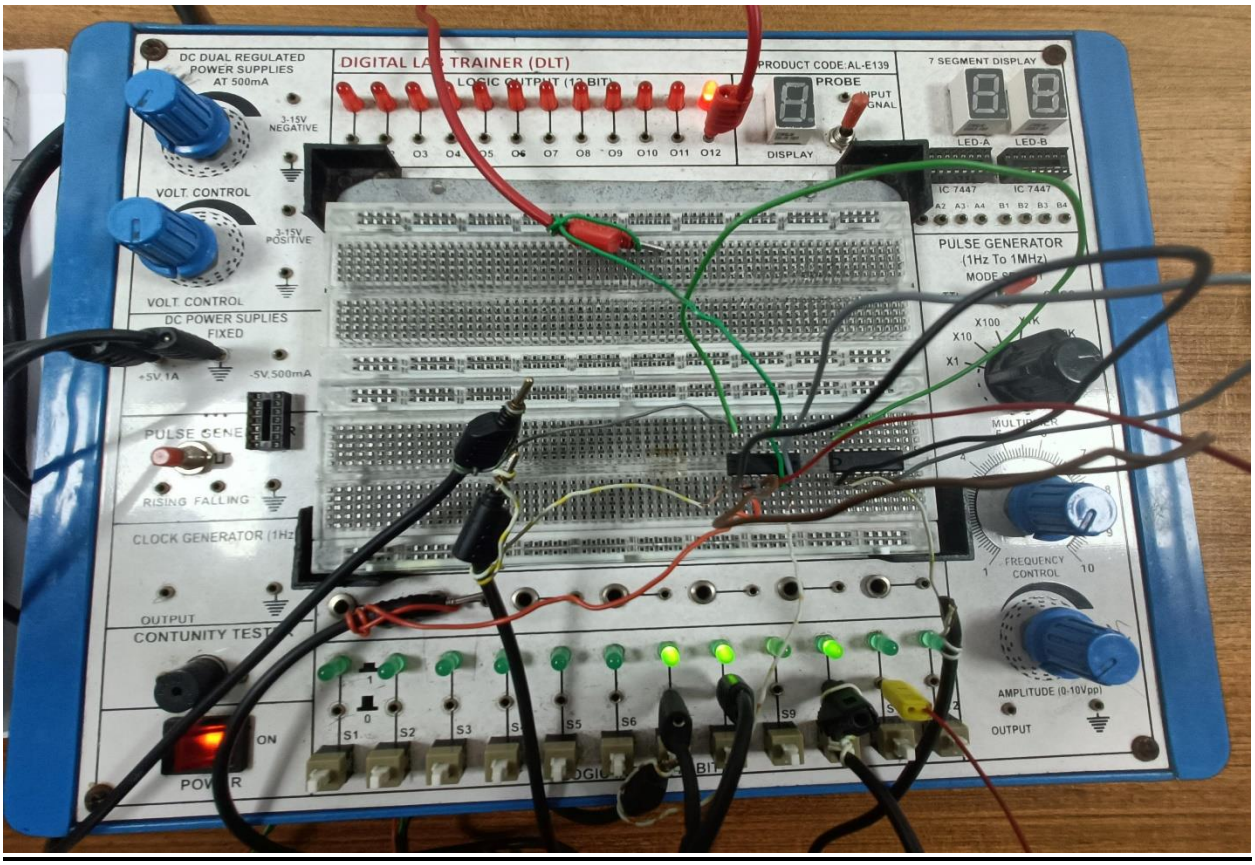
X100
X10
X1
FREQUENCY CONTROL
AMPLITUDE (0-10Vpp)
OUTPUT
S1
S2
S3
S5
S6
S9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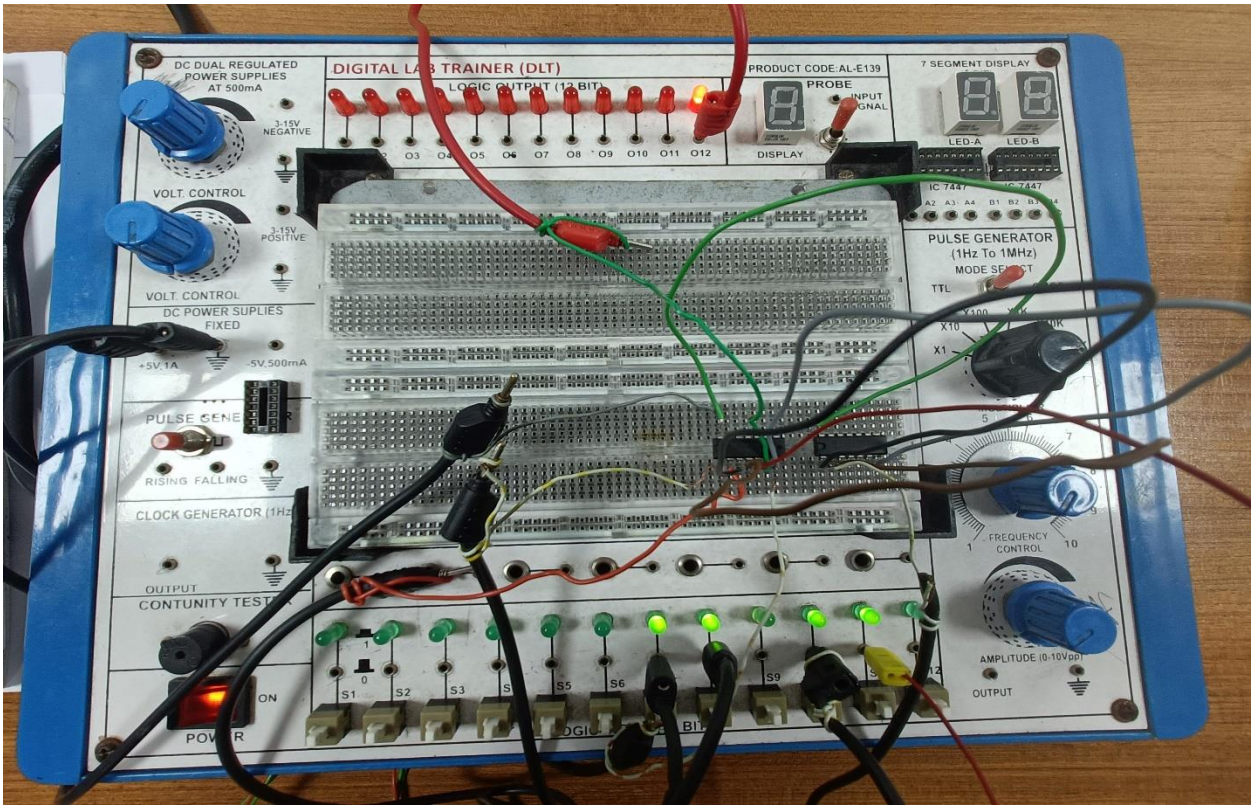
CLOCK GENERATOR (1Hz
OUTPUT
CONTUNITY TEST
ON
FREQUENCY CONTROL
AMPLITUDE (0-10Vpp)
S1
S2
S3
S5
S6
S9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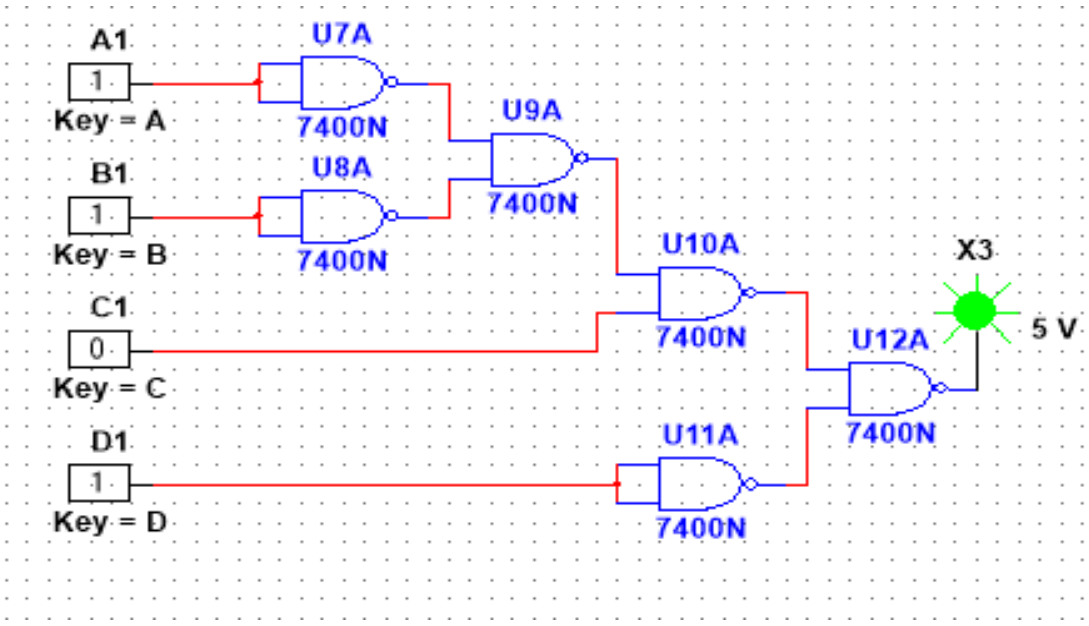
VOLT. CONTROL
DC POWER SUPLIES FIXED
+5V,1A
-5V,500mA
RISING FALLING
CLOCK GENERATOR (1Hz
OUTPUT
CONTUNITY TEST
ON
FREQUENCY CONTROL
AMPLITUDE (0-10Vpp)
S1
S2
S3
S5
S6
S9

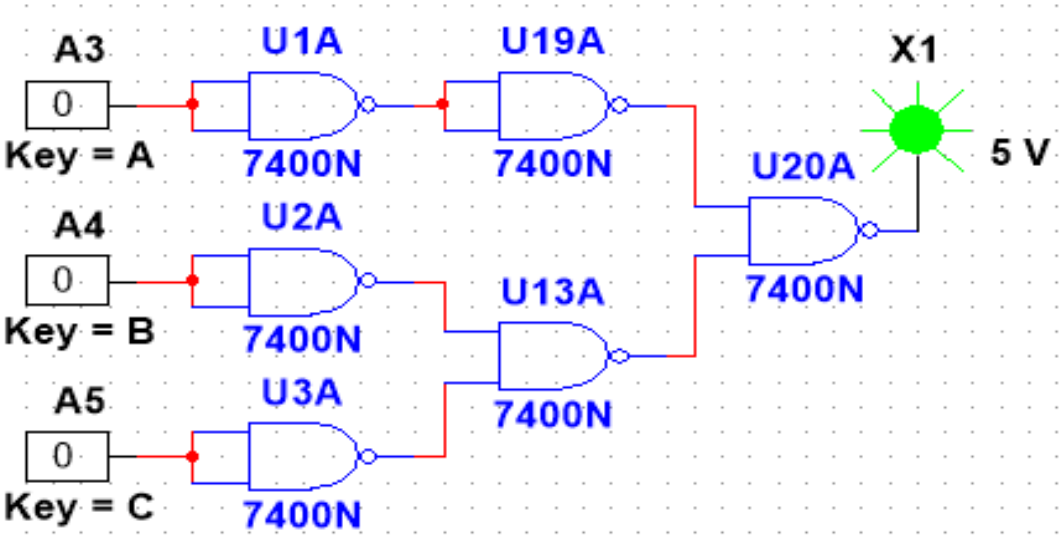
Report Questions:

1. Construct the derived equations (i) and (ii), using Universal gates (both NAND and NOR).

Equation (i) Y = (A+B) C + D



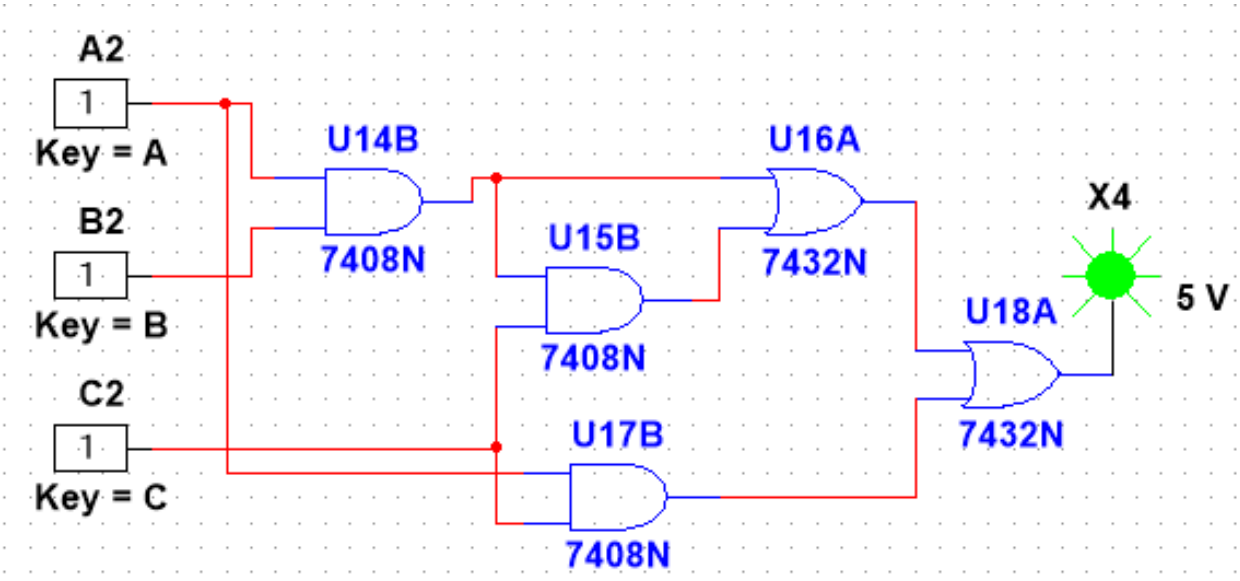
Equation (ii) Y = A' + B'C'



2. Develop the truth table for a certain three-input logic circuit with the output expression Y=ABC+(AB)'C+A'BC+AB'C+A(B'+C).

A	B	C	A'	B'	AB	(AB)'	(B'+C)	ABC	(AB)'C	A'BC	AB'C	A(B'+C)	Y
0	0	0	1	1	0	1	1	0	0	0	0	0	0
0	0	1	1	1	0	1	1	0	1	0	0	0	1
0	1	0	1	0	0	1	0	0	0	0	0	0	0
0	1	1	1	0	0	1	1	0	1	1	0	0	1
1	0	0	0	1	0	1	1	0	0	0	0	1	1
1	0	1	0	1	0	1	1	0	1	0	1	1	1
1	1	0	0	0	1	0	0	0	0	0	0	0	0
1	1	1	0	0	1	0	1	1	0	0	0	1	1

3. Implement the following logic expressions with logic gates Y=ABC+AB+AC



Conclusion:

Through this experiment, we acquired fundamental knowledge of learning and implementing logical expressions based on the given statement. By comparing the results of our simulations with the truth table, we confirmed that our system performed flawlessly during the simulation phase. The K-Map was utilized to simplify the logic expressions. Using only the AND and NAND gates, we were able to construct any other type of gate. In our experiment, we successfully built the system and circuits using AND, NAND, and OR gates.

Reference:

1. Thomas L. Floyd, “Digital Fundamentals,” available Edition, Prentice Hall International Inc.