AMERICAN INTERNATIONAL UNIVERSITY–BANGLADESH (AIUB)

FACULTY OF SCIENCE & TECHNOLOGY

DIGITAL LOGIC AND CIRCUITS LAB

Summer 2022-2023

Section: F
Group Number: 02

EXPERIMENT NO. 7

NAME OF THE EXPERIMENT

Implementation of Asynchronous and Synchronous counters using flip-flops

Supervised By

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Faculty of Engineering, AIUB

Submitted By:

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Introduction:

The purpose of this experiment is to learn about the counters and their characteristic against interval pulses using flip-flops. Also, we will learn two types of counters Asynchronous and Synchronous counters using the J-K flip flop. If the flip-flops do not receive the same clock signal, then that counter is called as Asynchronous counter. The output of system clock is applied as clock signal only to first flip-flop. The remaining flip-flops receive the clock signal from output of its previous stage flip-flop. If all the flip-flops receive the same clock signal, then that counter is called as Synchronous counter.

Theory and Methodology:

Asynchronous Counter: In a three-bit asynchronous counter, the external counter is connected to the clock input of the first flip-flop (FF0) only. By getting the Q output of FF0, then FF1 will be triggered. Because of the propagation delay through the flip-flop, the transition between the input clock pulse and the transition of the Q output of FF0 can never occur at the same time.

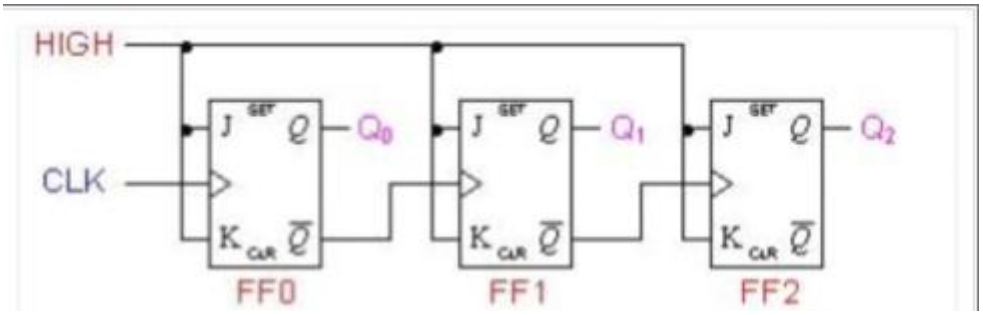


Figure-2: 3-bit Asynchronous Counter

Synchronous Counter: In a three-bit synchronous counter, the clock inputs of all the flip-flops are connected with each other. By this, all the flip-flops change their state parallelly. The advantage of this counter is that there is no cumulative time delay because all flip-flops are triggered in parallel.

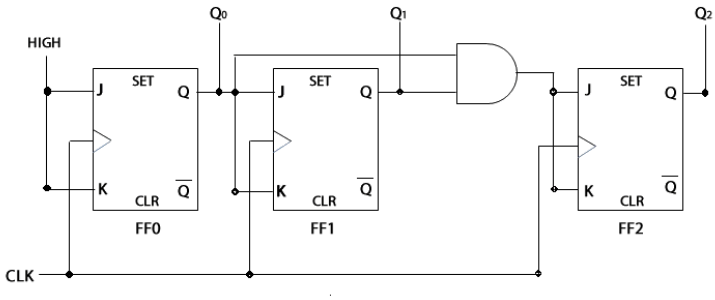


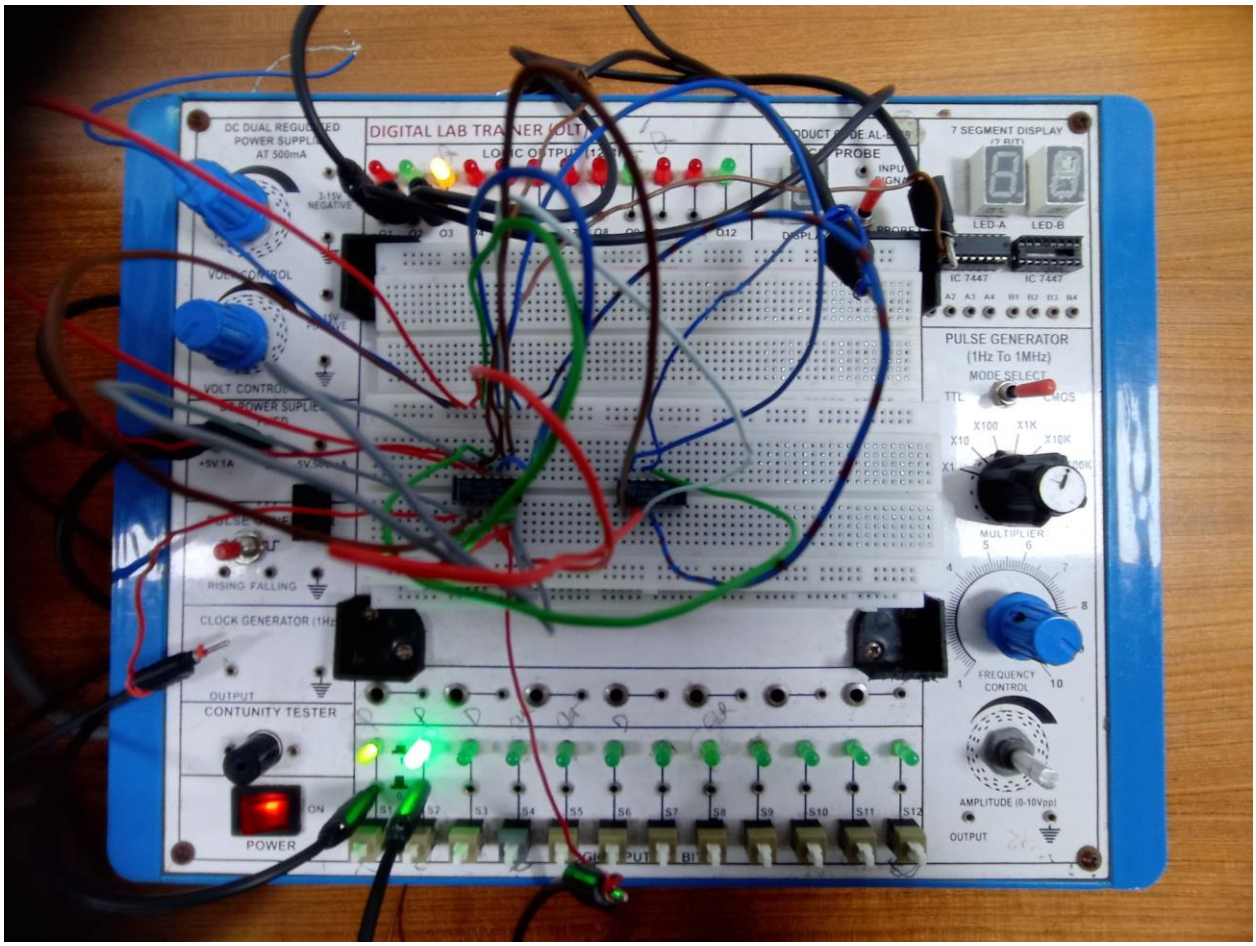
Figure-3: 3-bit Synchronous Counter

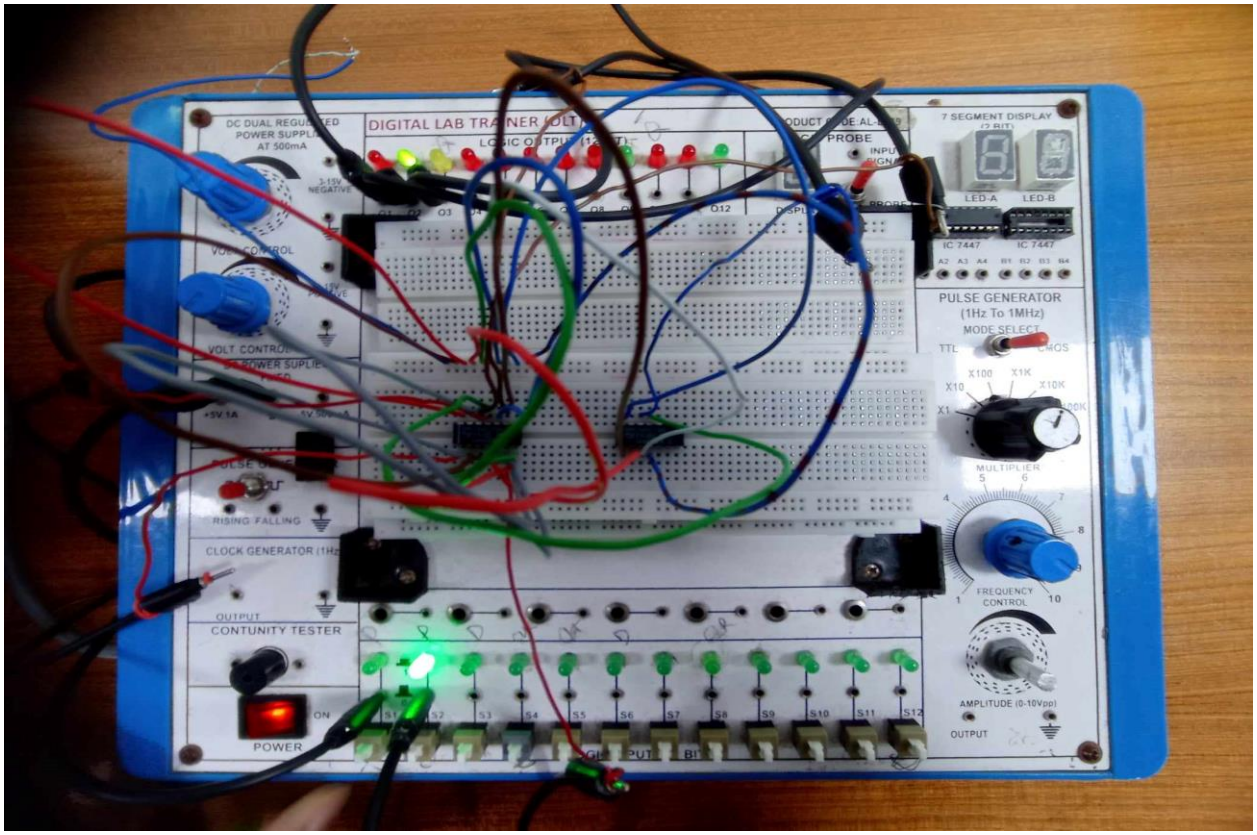
Apparatus:

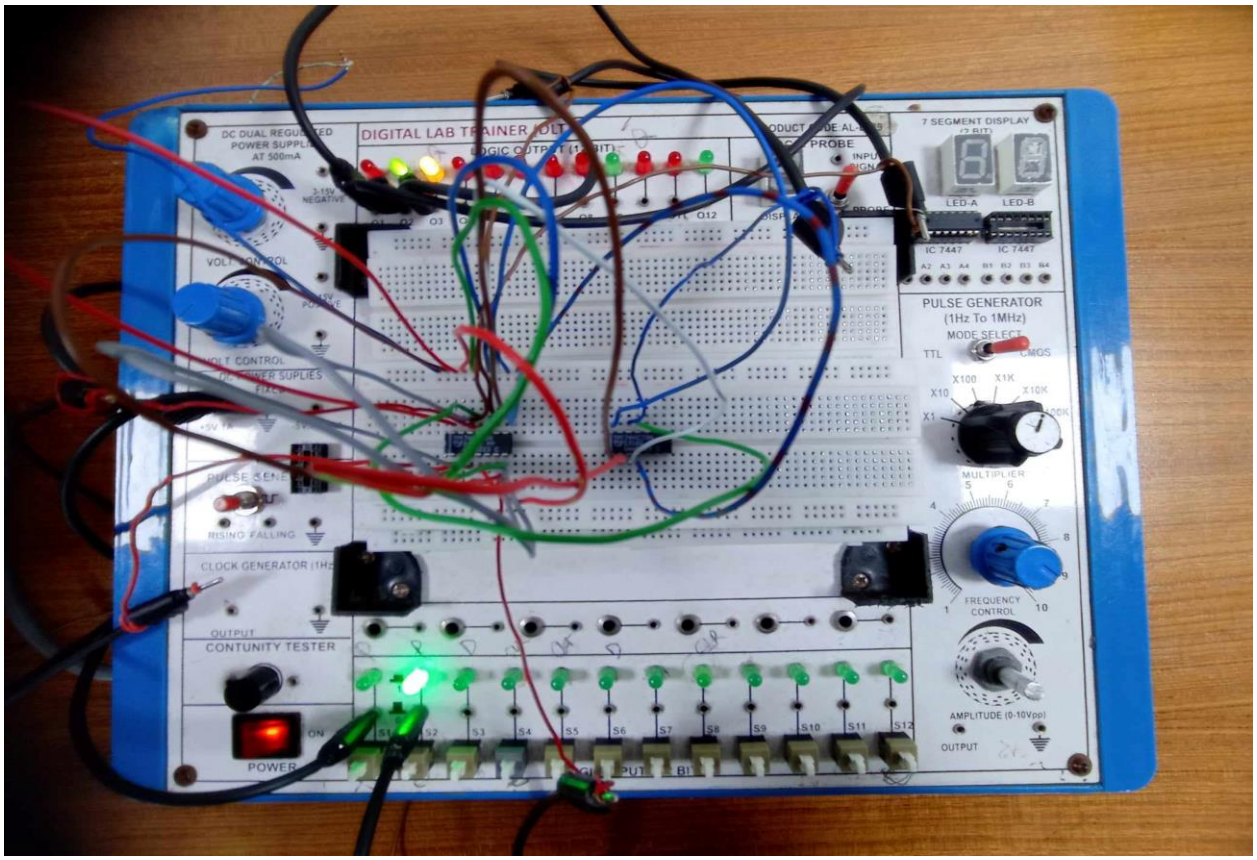
- IC 74LS76 (JK Flip Flop)
- IC 7408 (AND Gate)
- LED Lamps or Display
- Trainer Board
- Oscilloscope
- Connecting Wires

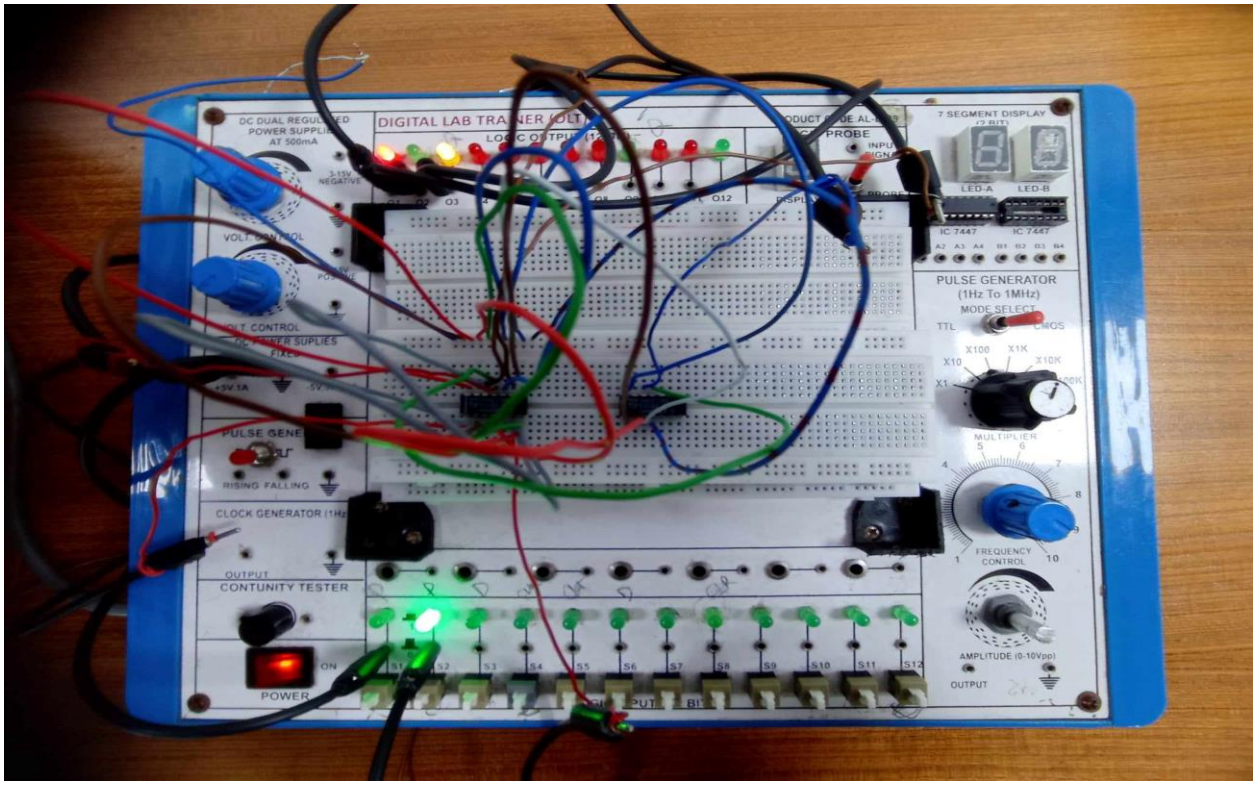
Hardware implementation

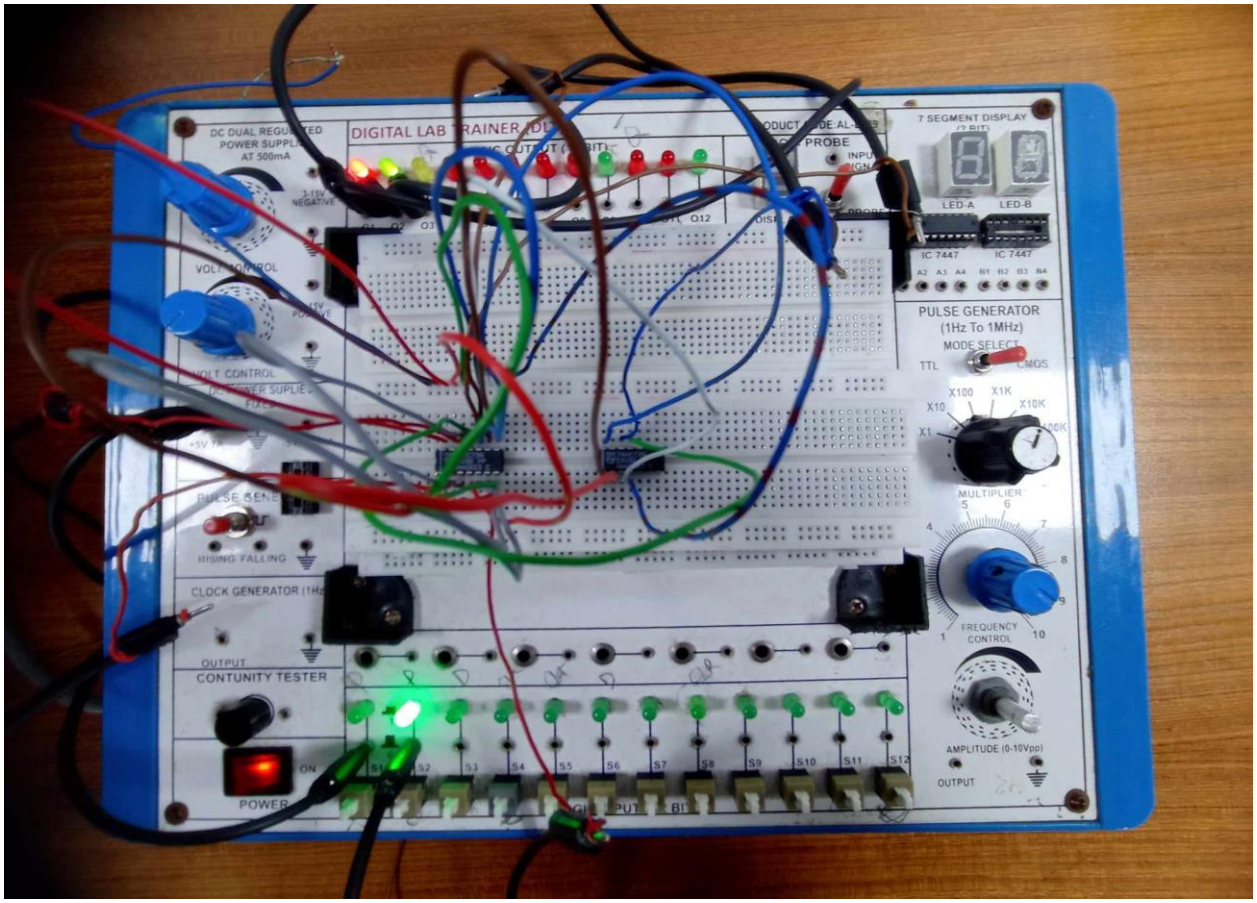
Asynchronous Counter:

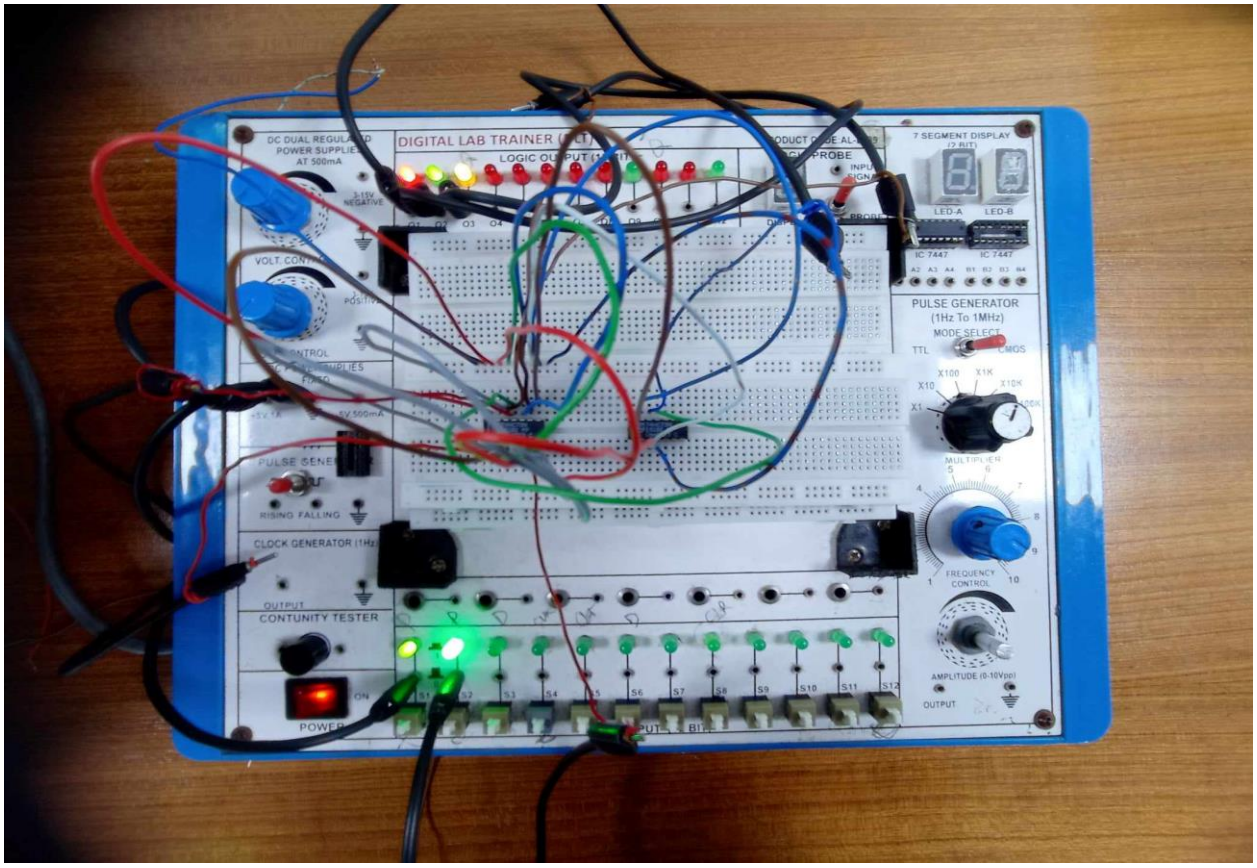



DIGITAL LAB TRAINER
PROBE
7 SEGMENT DISPLAY
LED-A
LED-B
IC 7447
IC 7447
PULSE GENERATOR
(1Hz To 1MHz)
MODE SELECT
TTL
CMOS
MULTIPLIER
FREQUENCY CONTROL
AMPLITUDE (0-10Vpp)
OUTPUT
CONTUNITY TESTER
POWER
ON

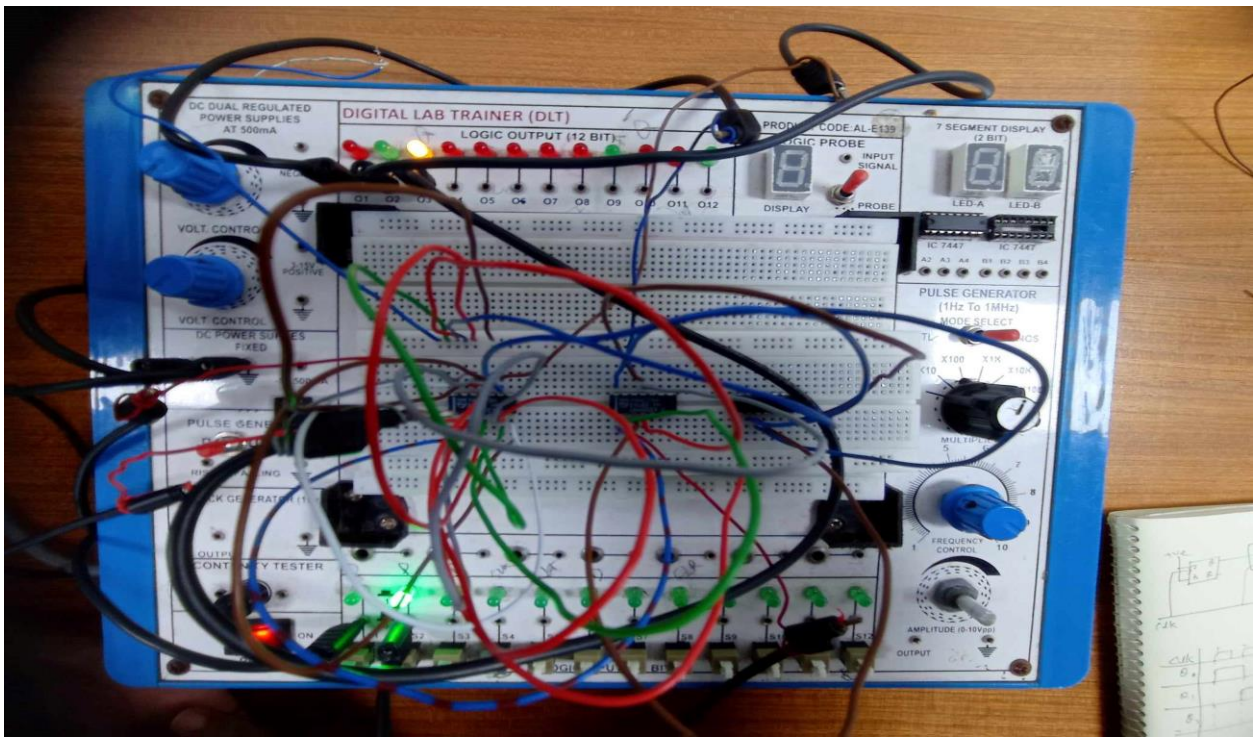

DIGITAL LAB TRAINER
PROBE
7 SEGMENT DISPLAY
LED-A
LED-B
IC 7447
IC 7447
PULSE GENERATOR
(1Hz To 1MHz)
MODE SELECT
TTL
CMOS
MULTIPLIER
FREQUENCY CONTROL
AMPLITUDE (0-10Vpp)
OUTPUT
CONTUNITY TESTER
POWER
ON

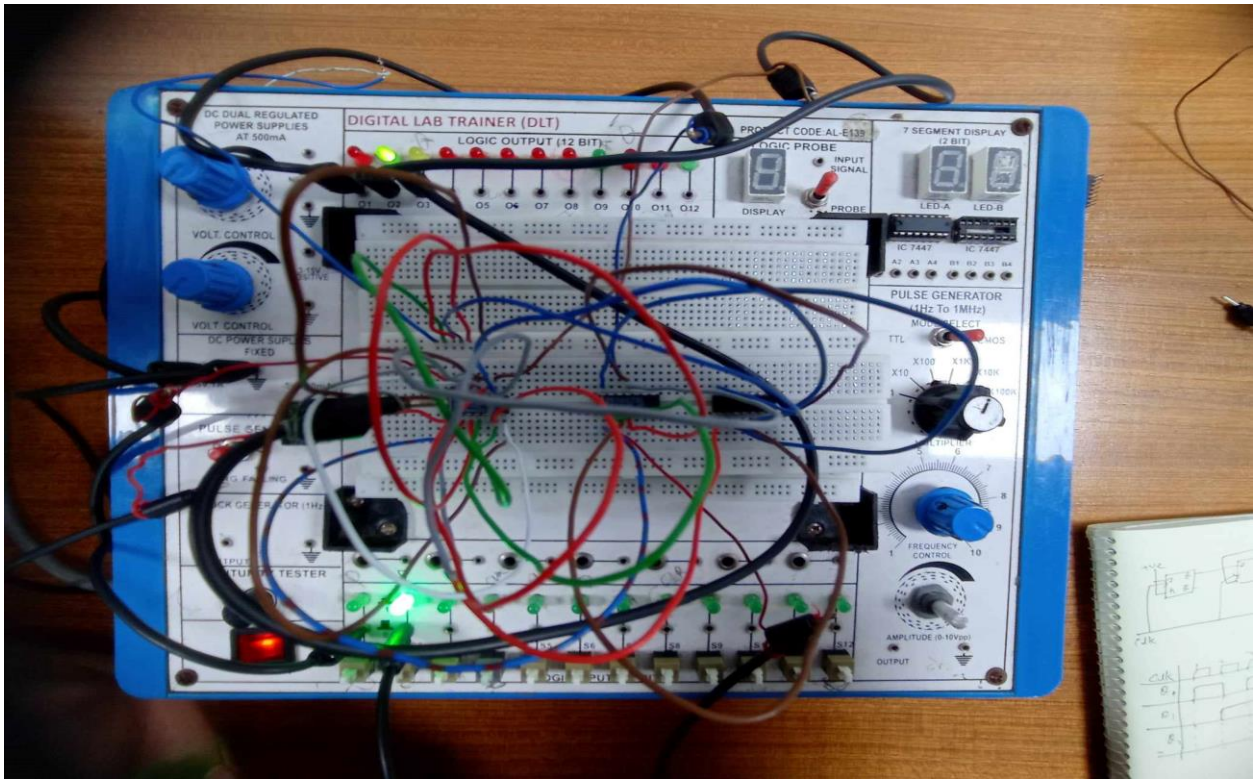

DIGITAL LAB TRAINER
7 SEGMENT DISPLAY
LED-A
LED-B
IC 7447
PULSE GENERATOR
(1Hz To 1MHz)
MODE SELECT
TTL
CMOS
MULTIPLIER
FREQUENCY CONTROL
AMPLITUDE (0-10Vpp)
OUTPUT
CONTUNITY TESTER
POWER
PROBE

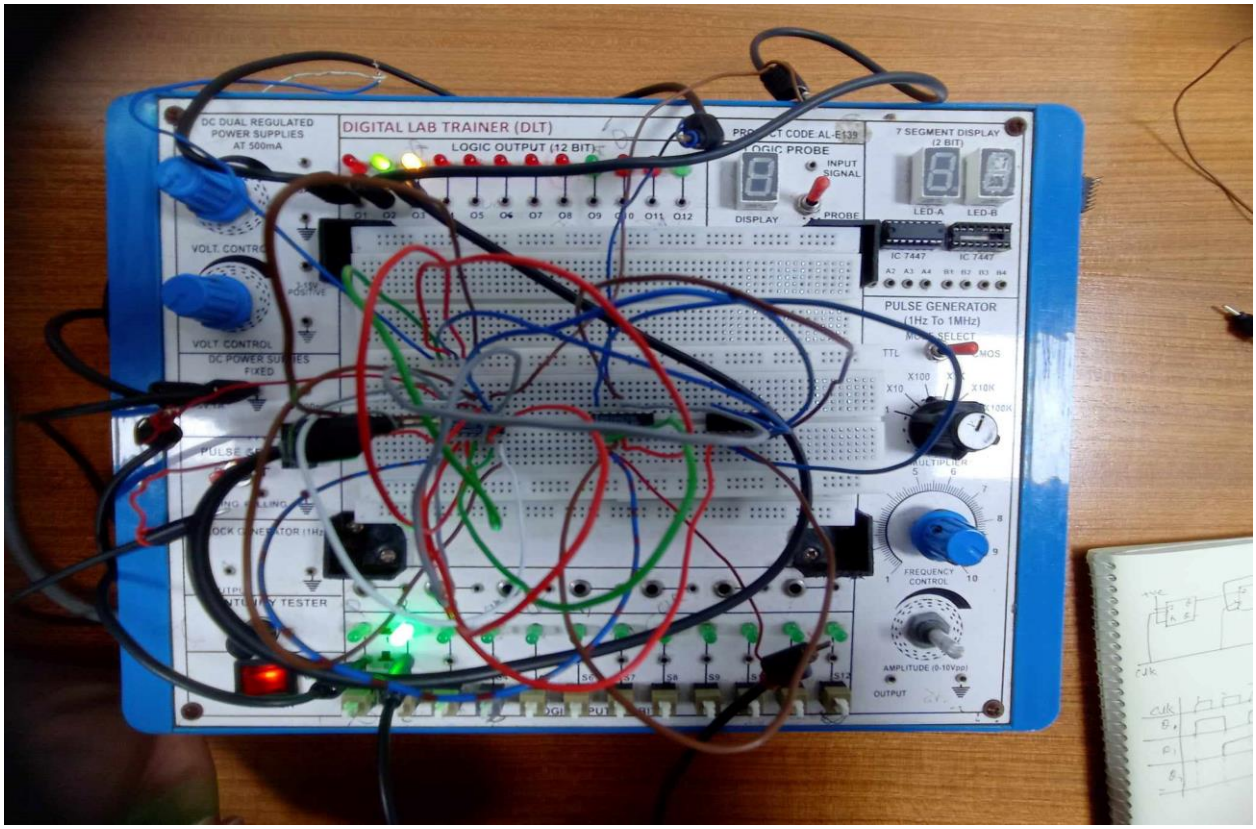

DIGITAL LAB TRAINER
7 SEGMENT DISPLAY
LED-A
LED-B
IC 7447
PULSE GENERATOR
(1Hz To 1MHz)
MODE SELECT
TTL
CMOS
MULTIPLIER
FREQUENCY CONTROL
AMPLITUDE (0-10Vpp)
OUTPUT
CONTUNITY TESTER
POWER
PROBE

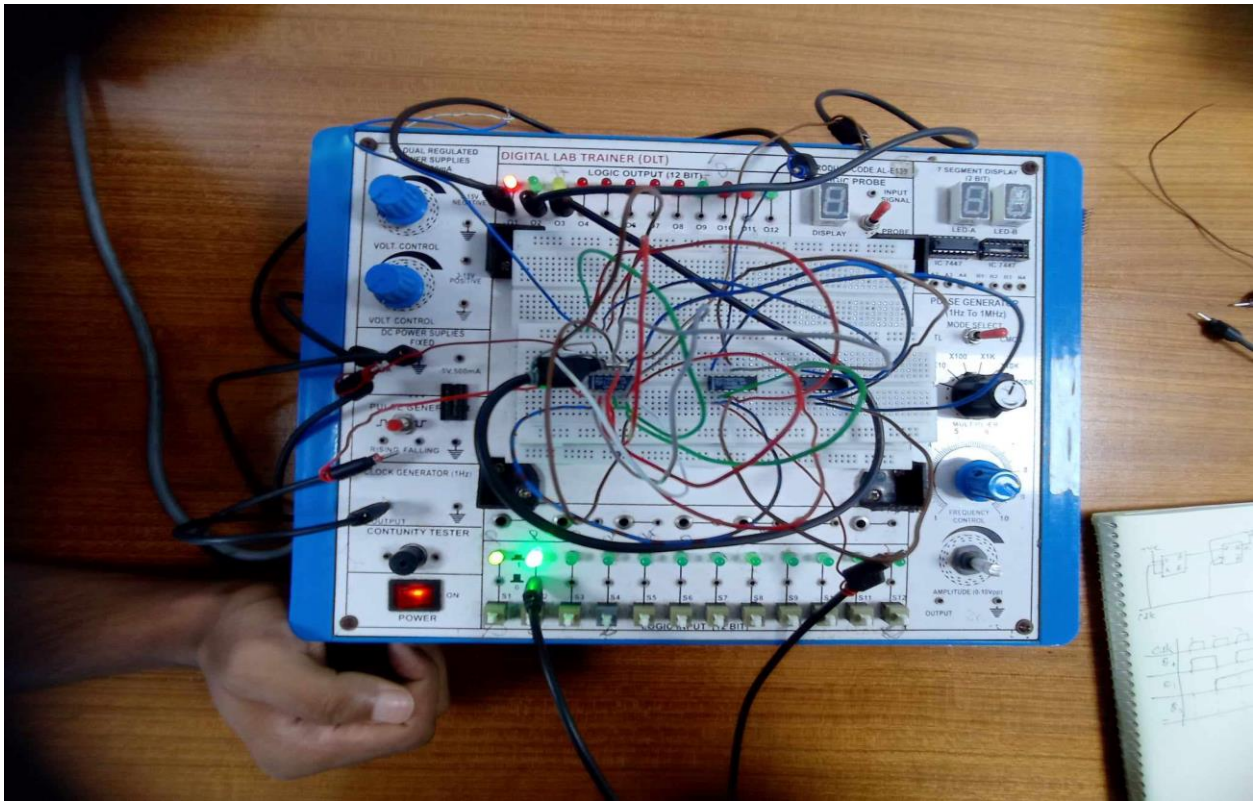


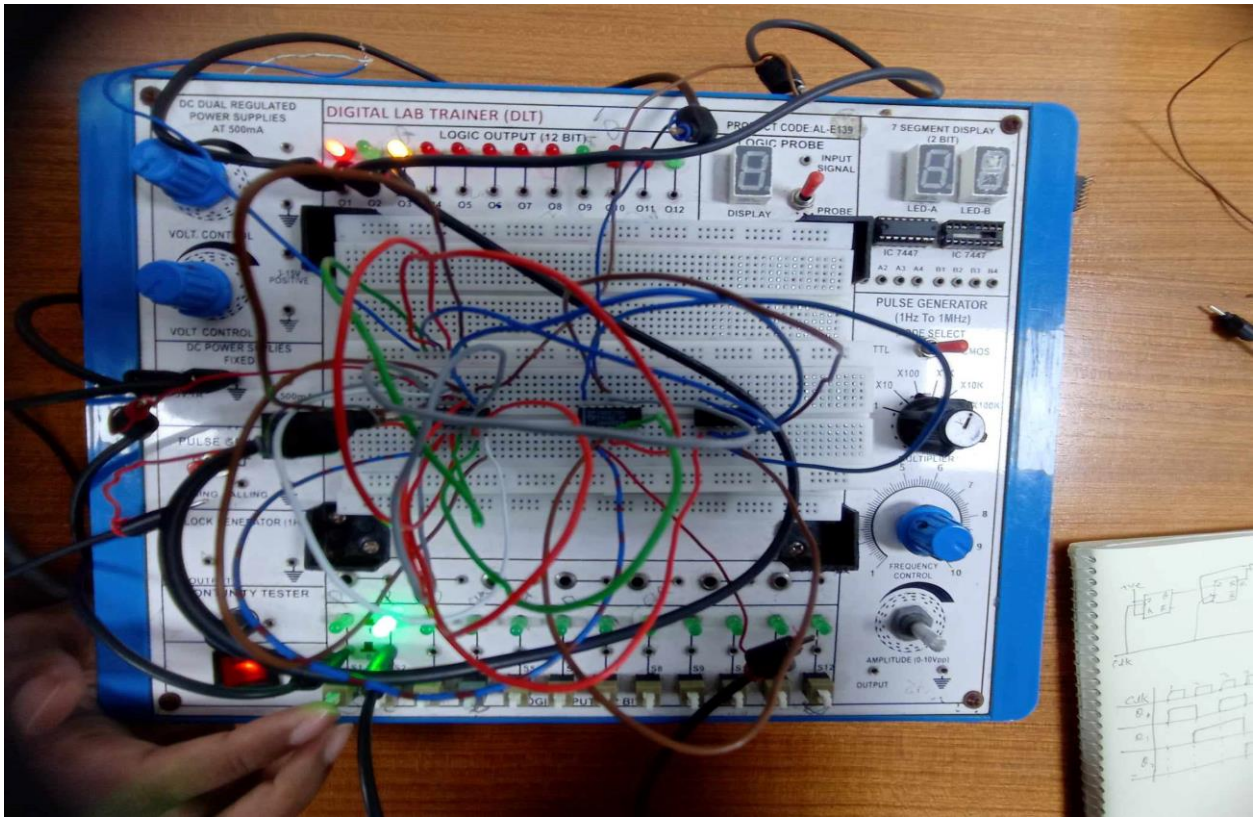
Synchronous Counter:

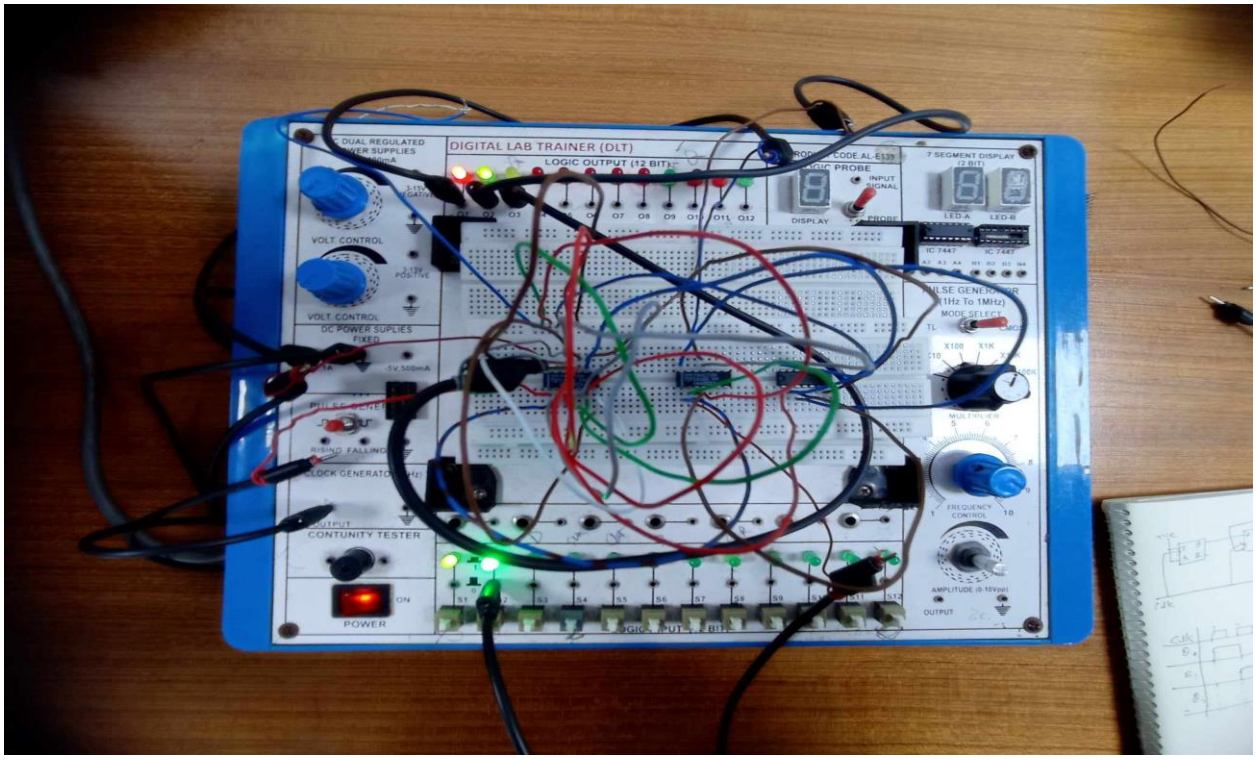


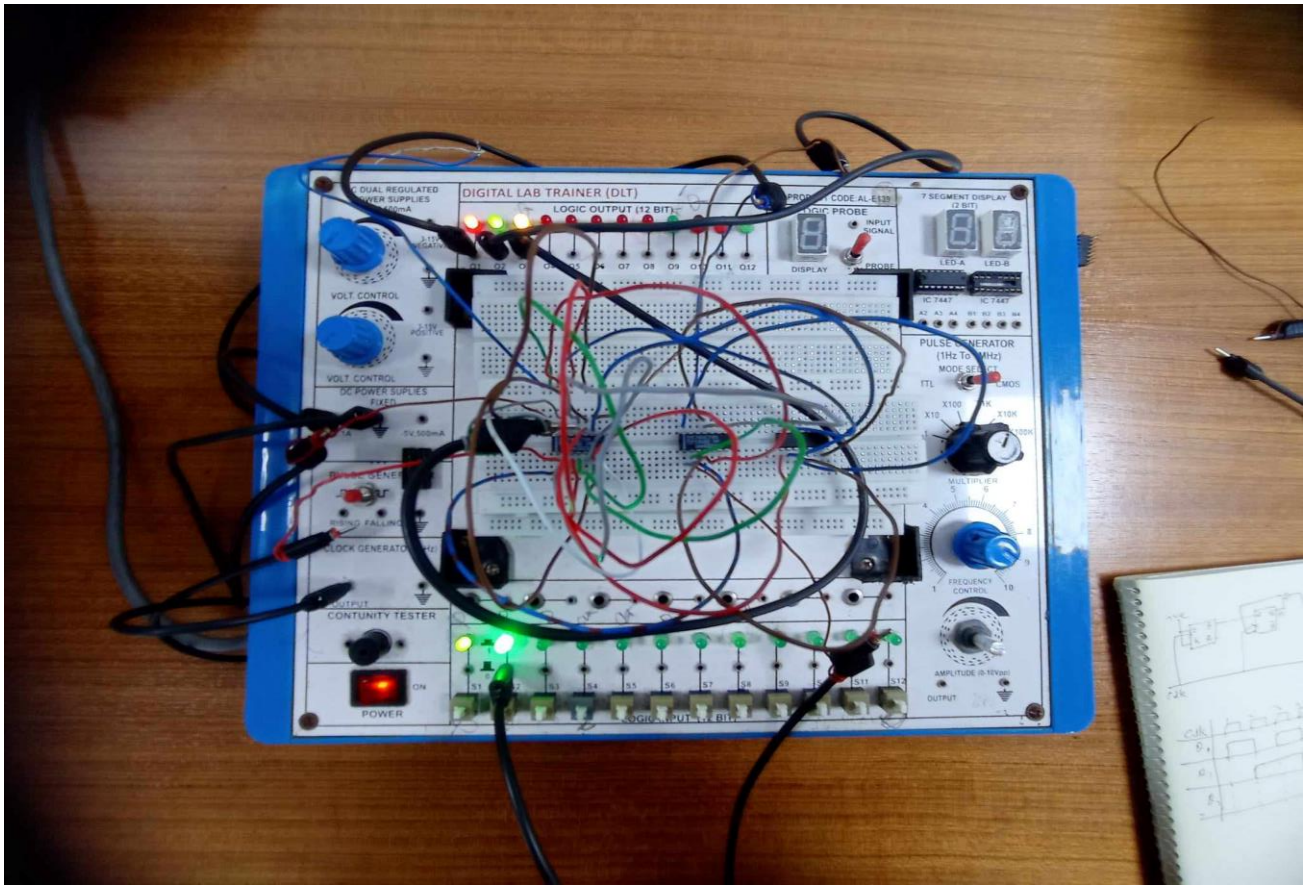

DC DUAL REGULATED
POWER SUPPLIES
AT 500mA
DIGITAL LAB TRAINER (DLT)
LOGIC OUTPUT (12 BIT)
LOGIC PROBE
INPUT
SIGNAL
DISPLAY
PROBE
7 SEGMENT DISPLAY
(2 BIT)
LED-A
LED-B
IC 7447
IC 7447
PULSE GENERATOR
(1Hz To 1MHz)
TTL
MOS
X100
X10
X1K
X10K
FREQUENCY
CONTROL
AMPLITUDE (0-10Vpp)
OUTPUT
VOLT. CONTROL
VOLT. CONTROL
FIXED


DC DUAL REGULATED
POWER SUPPLIES
AT 500mA
DIGITAL LAB TRAINER (DLT)
LOGIC OUTPUT (12 BIT)
LOGIC PROBE
INPUT
SIGNAL
DISPLAY
PROBE
7 SEGMENT DISPLAY
(2 BIT)
LED-A
LED-B
IC 7447
IC 7447
PULSE GENERATOR
(1Hz To 1MHz)
TTL
MOS
X100
X10
X1K
X10K
FREQUENCY
CONTROL
AMPLITUDE (0-10Vpp)
OUTPUT
VOLT. CONTROL
VOLT. CONTROL
FIXED


DIGITAL LAB TRAINER (DLT)
LOGIC OUTPUT (12 BIT)
VOLT CONTROL
VOLT CONTROL
DC POWER SUPLIES FIXED
CONTUNITY TESTER
POWER
7 SEGMENT DISPLAY (2 BIT)
LED-A
LED-B
IC 7447
IC 7447
PULSE GENERATOR (1Hz To 1MHz)
MODE SELECT
FREQUENCY CONTROL
AMPLITUDE (0-10Vpp)
OUTPUT

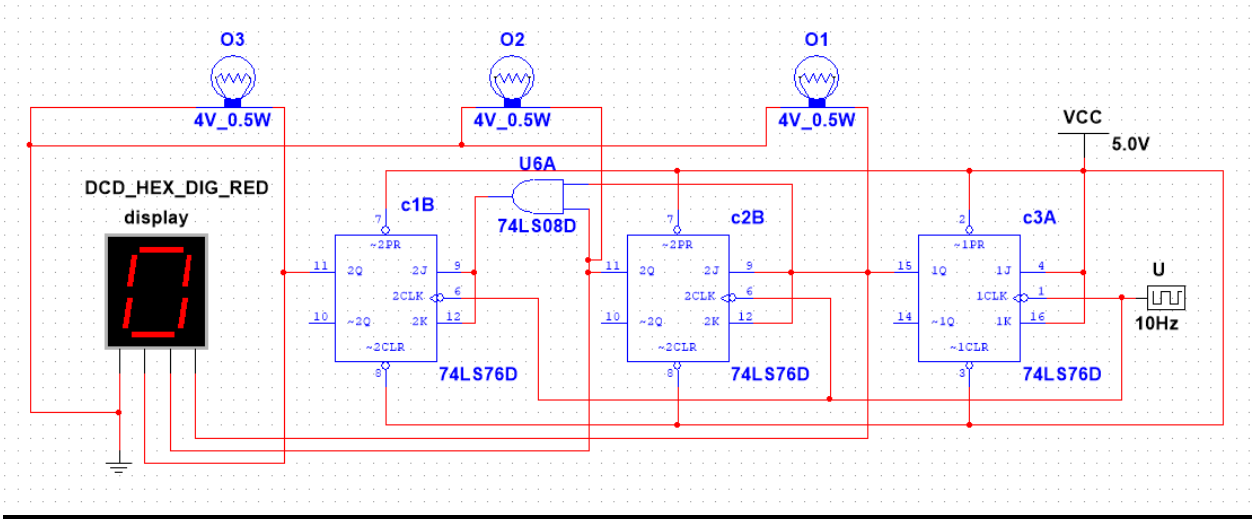

DC DUAL REGULATED POWER SUPPLIES AT 500mA
DIGITAL LAB TRAINER (DLT)
LOGIC OUTPUT (12 BIT)
LOGIC PROBE
INPUT SIGNAL
DISPLAY
PROBE
7 SEGMENT DISPLAY (2 BIT)
LED-A
LED-B
IC 7447
IC 7447
PULSE GENERATOR (1Hz To 1MHz)
TTL
MOS
X100
X10
X10K
FREQUENCY CONTROL
AMPLITUDE (0-10Vpp)
OUTPUT

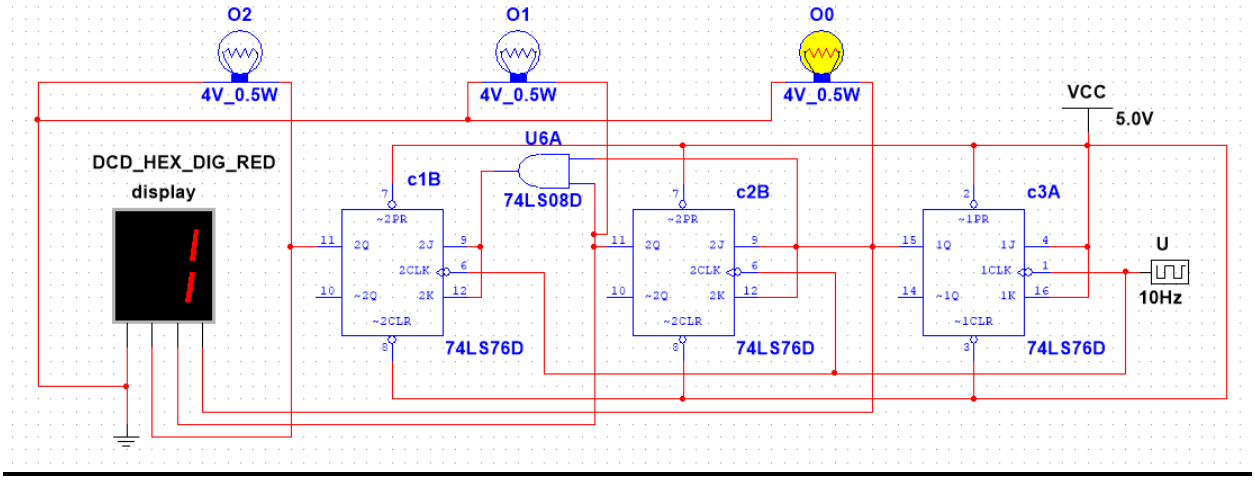

DIGITAL LAB TRAINER (DLT)
LOGIC OUTPUT (12 BIT)
LOGIC PROBE
7 SEGMENT DISPLAY
VOLT CONTROL
DC POWER SUPPLIES FIXED
CONTUNITY TESTER
POWER
FREQUENCY CONTROL
AMPLITUDE
OUTPUT

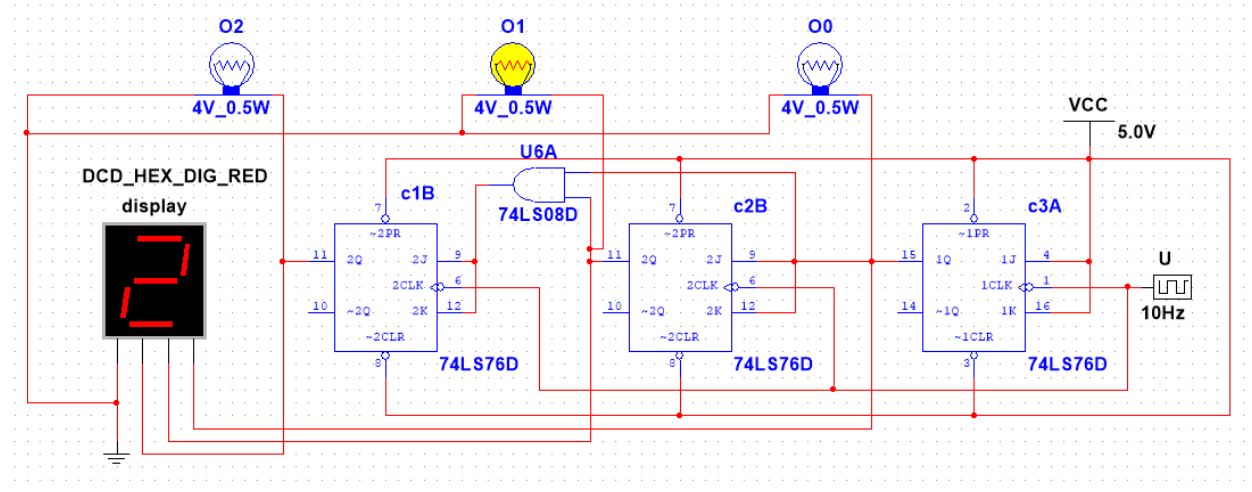

DIGITAL LAB TRAINER (DLT)
LOGIC OUTPUT (12 BIT)
LOGIC PROBE
7 SEGMENT DISPLAY
VOLT CONTROL
DC POWER SUPPLIES FIXED
CONTUNITY TESTER
POWER
FREQUENCY CONTROL
OUTPUT

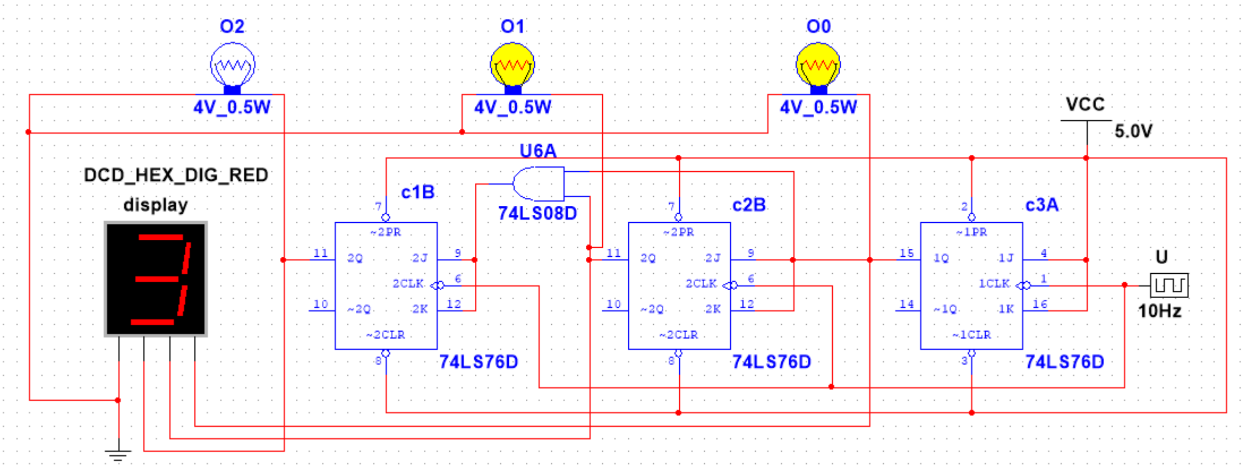
Simulation

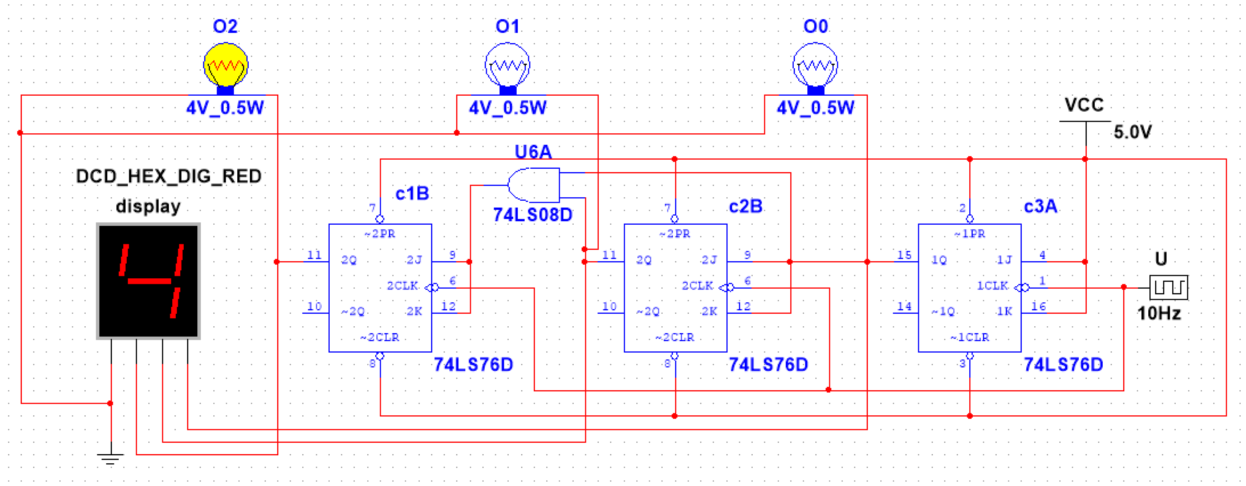
3- bit synchronous up counter:

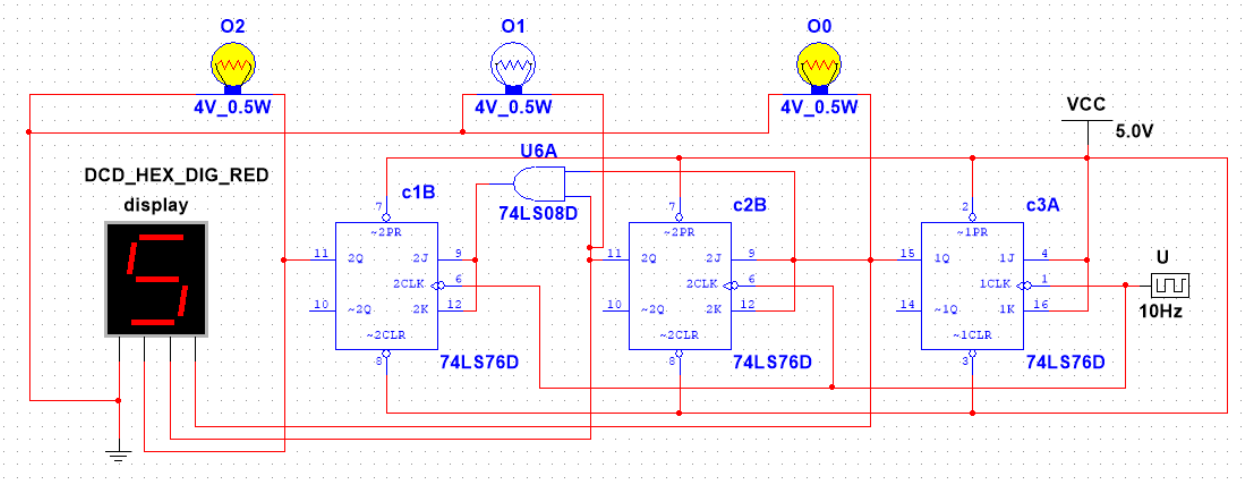


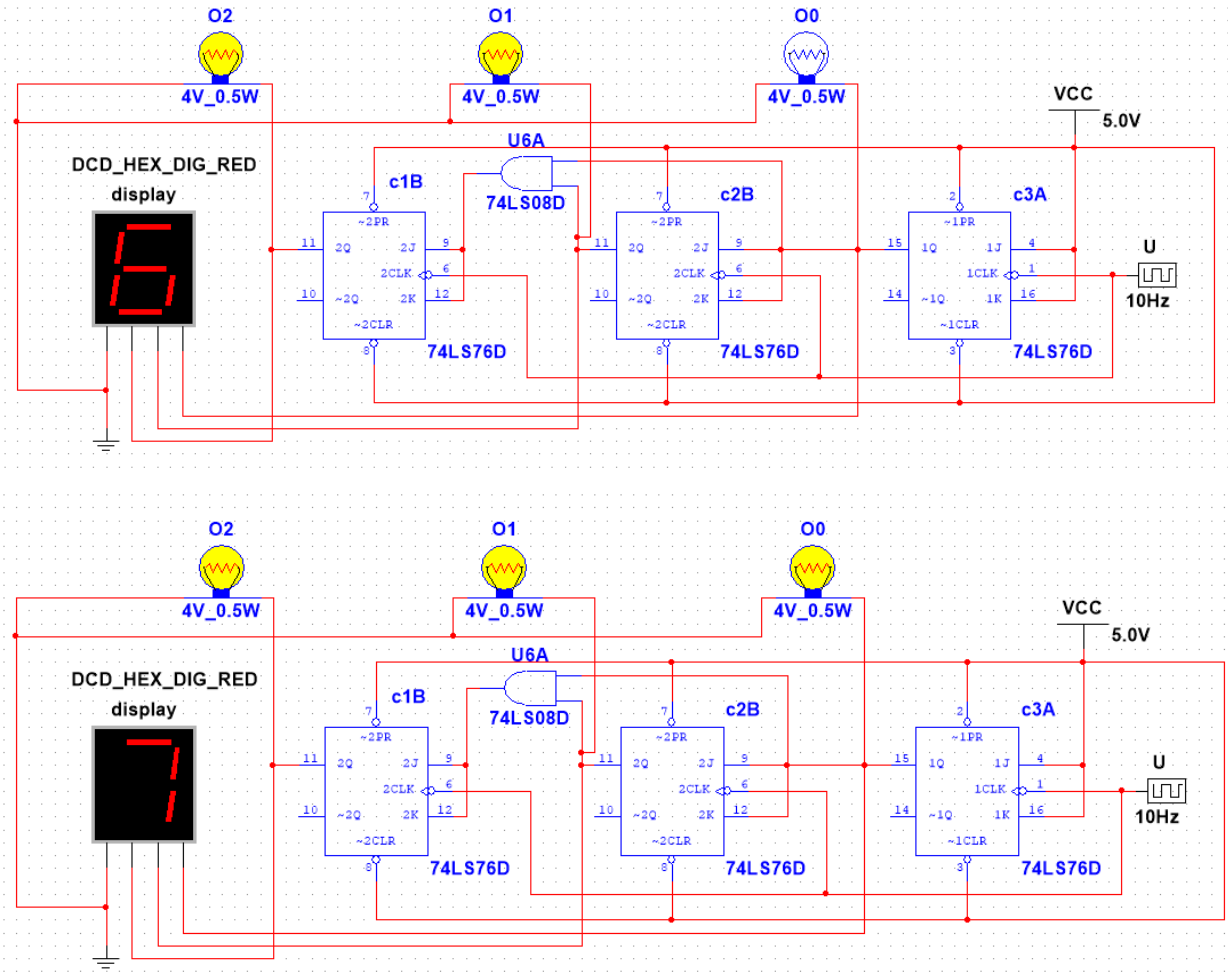




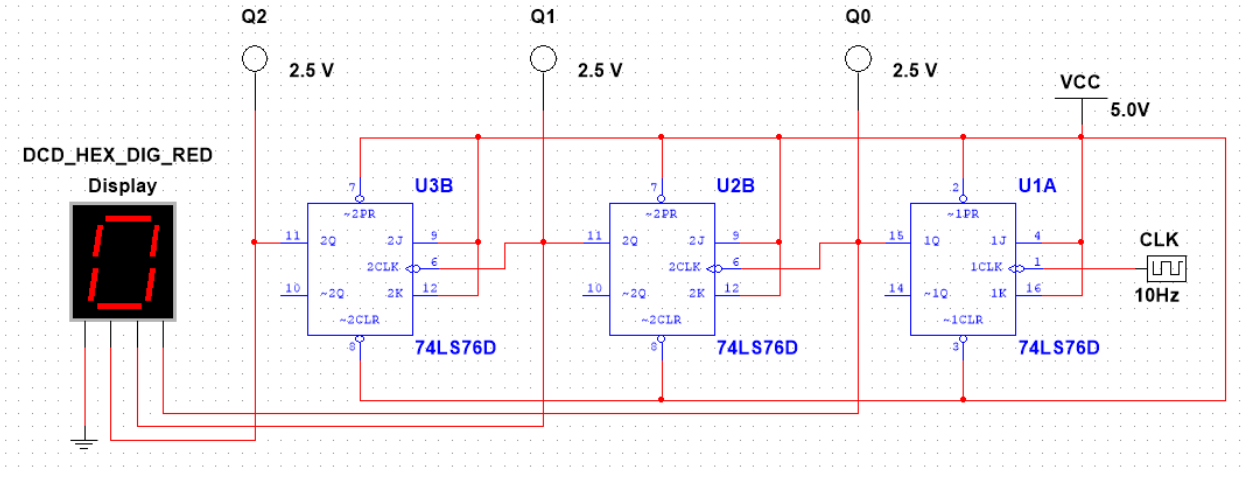

O2
O1
O0
4V_0.5W
4V_0.5W
4V_0.5W
VCC
5.0V
U6A
DCD_HEX_DIG_RED
display
c1B
74LS08D
c2B
c3A
U
10Hz
74LS76D
74LS76D
74LS76D

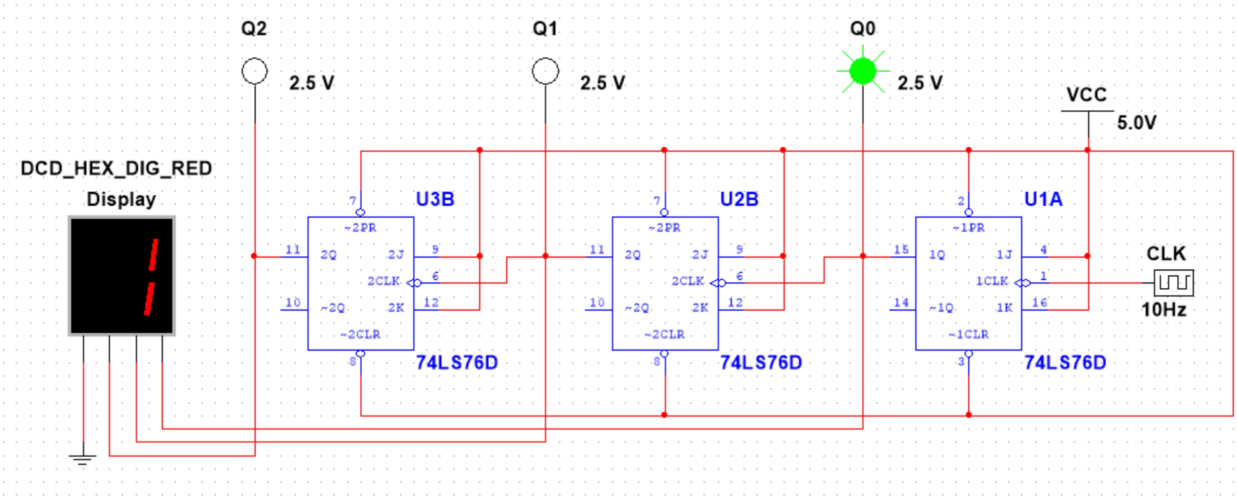

O2
O1
O0
4V_0.5W
4V_0.5W
4V_0.5W
VCC
5.0V
U6A
DCD_HEX_DIG_RED
display
c1B
74LS08D
c2B
c3A
U
10Hz
74LS76D
74LS76D
74LS76D

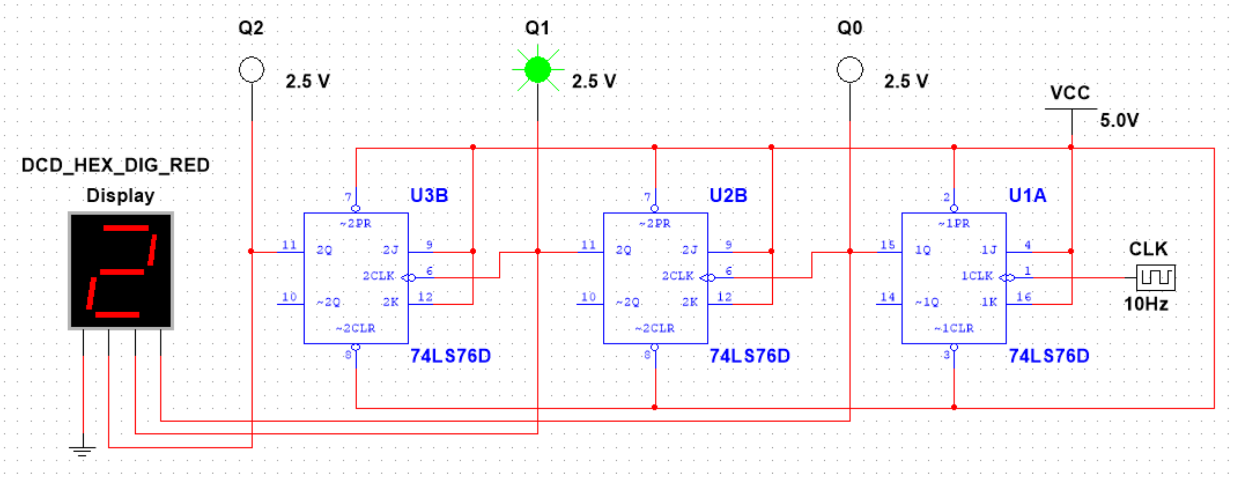

O2
O1
O0
4V_0.5W
4V_0.5W
4V_0.5W
VCC
5.0V
U6A
DCD_HEX_DIG_RED
display
c1B
74LS08D
c2B
c3A
U
10Hz
74LS76D
74LS76D
74LS76D

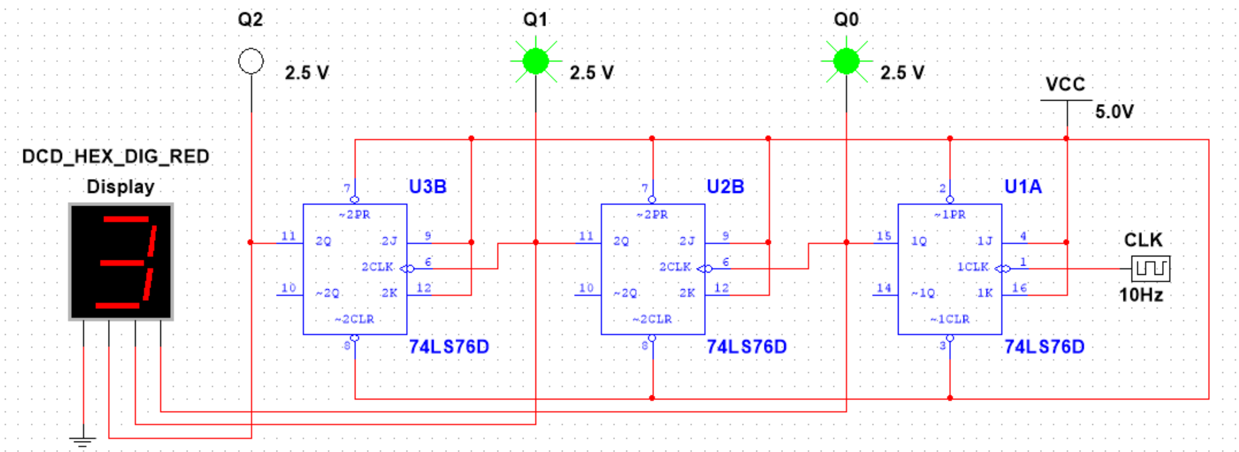


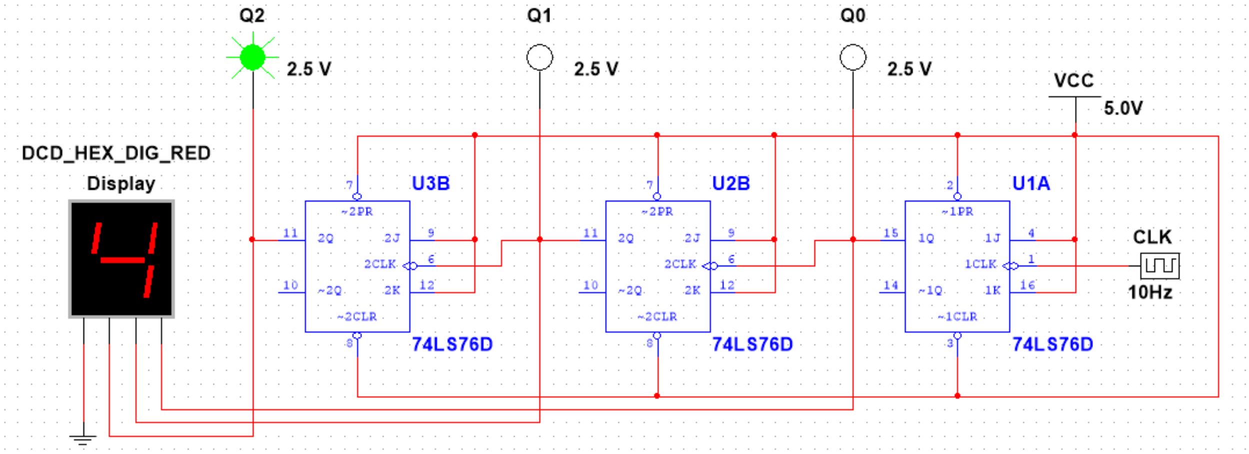
3- bit asynchronous up counter:

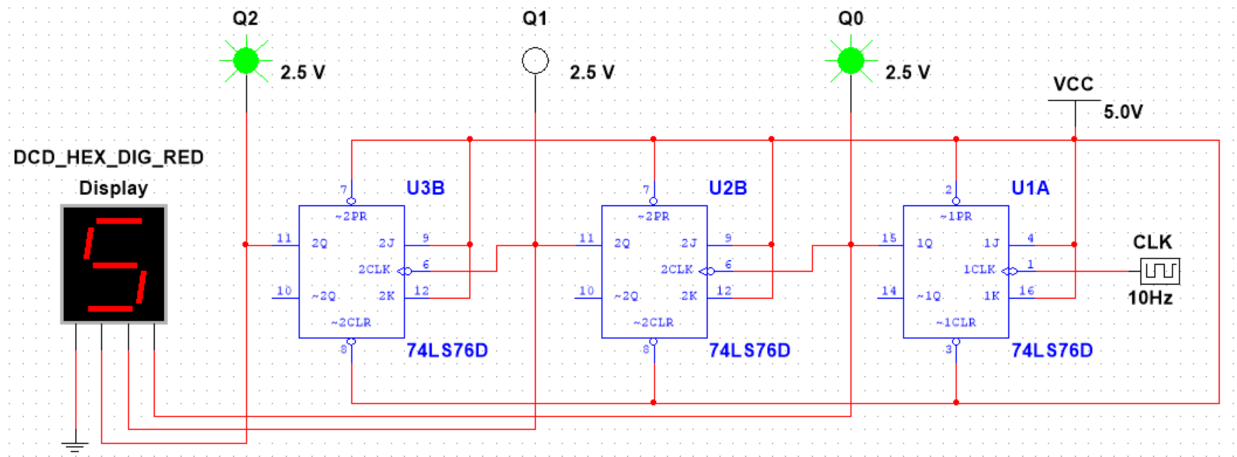


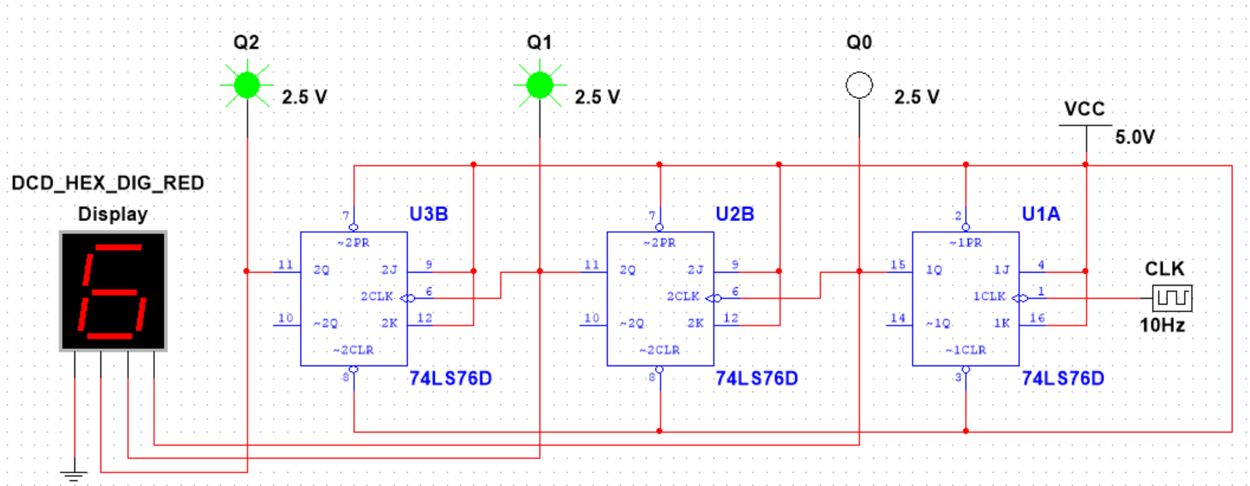

Q2
Q1
Q0
2.5 V
2.5 V
2.5 V
VCC
5.0V
DCD_HEX_DIG_RED
Display
U3B
U2B
U1A
74LS76D
74LS76D
74LS76D
CLK
10Hz

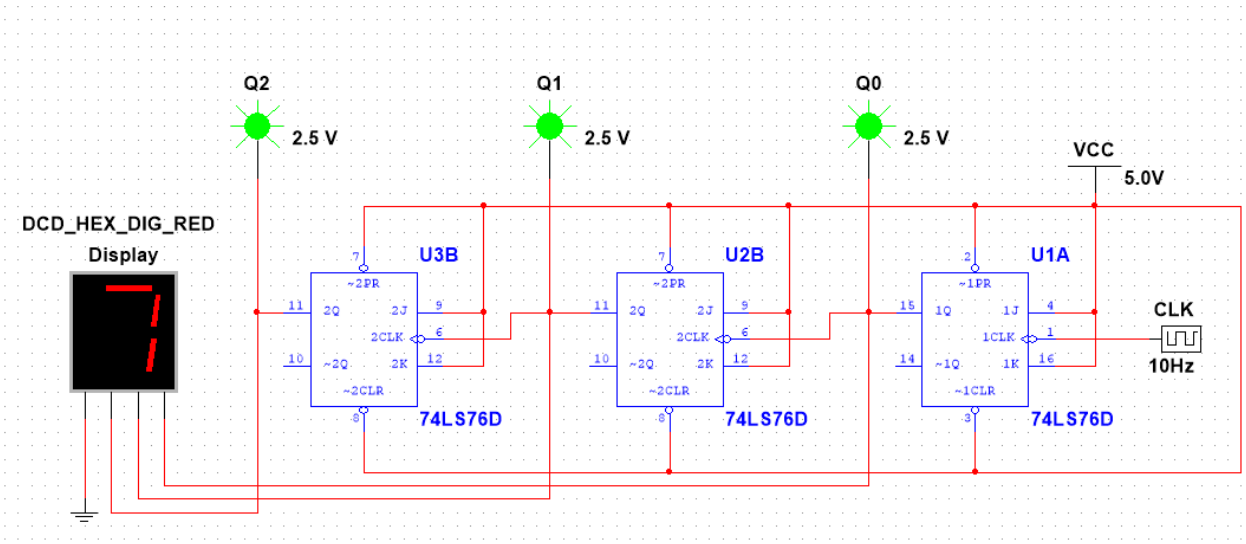

Q2
Q1
Q0
2.5 V
2.5 V
2.5 V
VCC
5.0V
DCD_HEX_DIG_RED
Display
U3B
U2B
U1A
74LS76D
74LS76D
74LS76D
CLK
10Hz


Q2
Q1
Q0
2.5 V
2.5 V
2.5 V
VCC
5.0V
DCD_HEX_DIG_RED
Display
U3B
U2B
U1A
74LS76D
74LS76D
74LS76D
CLK
10Hz

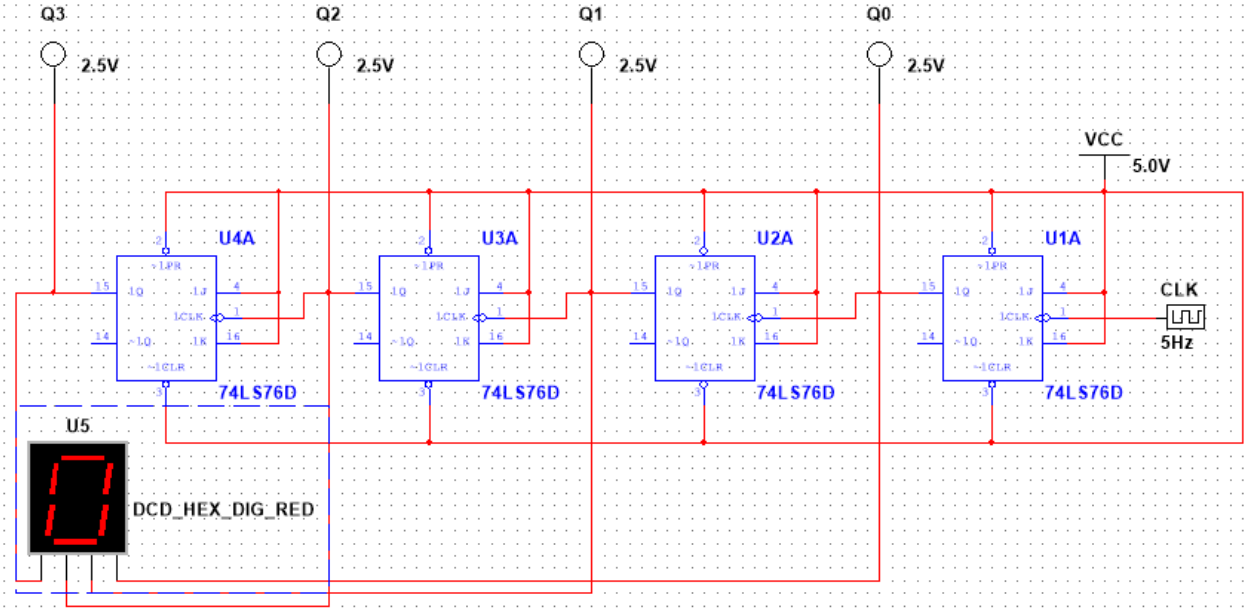

Q2
2.5 V
Q1
2.5 V
Q0
2.5 V
VCC
5.0V
DCD_HEX_DIG_RED
Display
U3B
74LS76D
U2B
74LS76D
U1A
74LS76D
CLK
10Hz

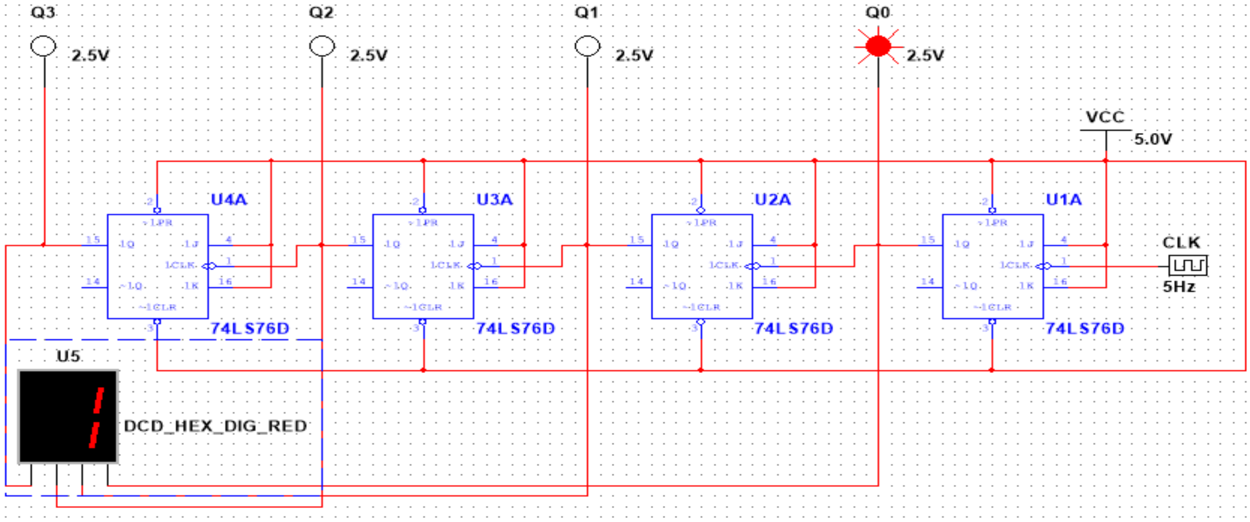

Q2
2.5 V
Q1
2.5 V
Q0
2.5 V
VCC
5.0V
DCD_HEX_DIG_RED
Display
U3B
74LS76D
U2B
74LS76D
U1A
74LS76D
CLK
10Hz

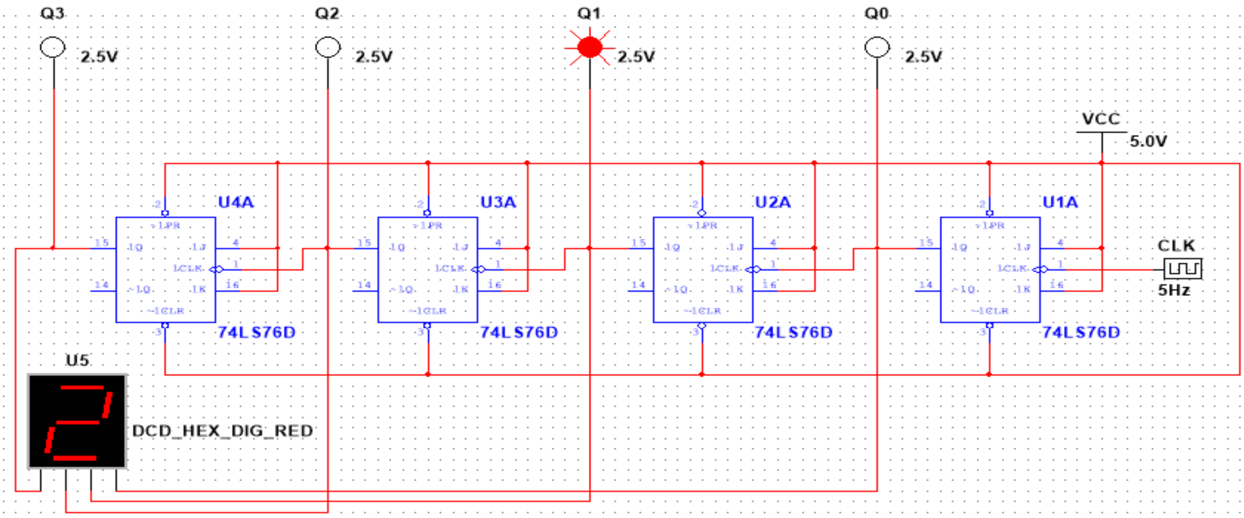

Q2
2.5 V
Q1
2.5 V
Q0
2.5 V
VCC
5.0V
DCD_HEX_DIG_RED
Display
U3B
74LS76D
U2B
74LS76D
U1A
74LS76D
CLK
10Hz

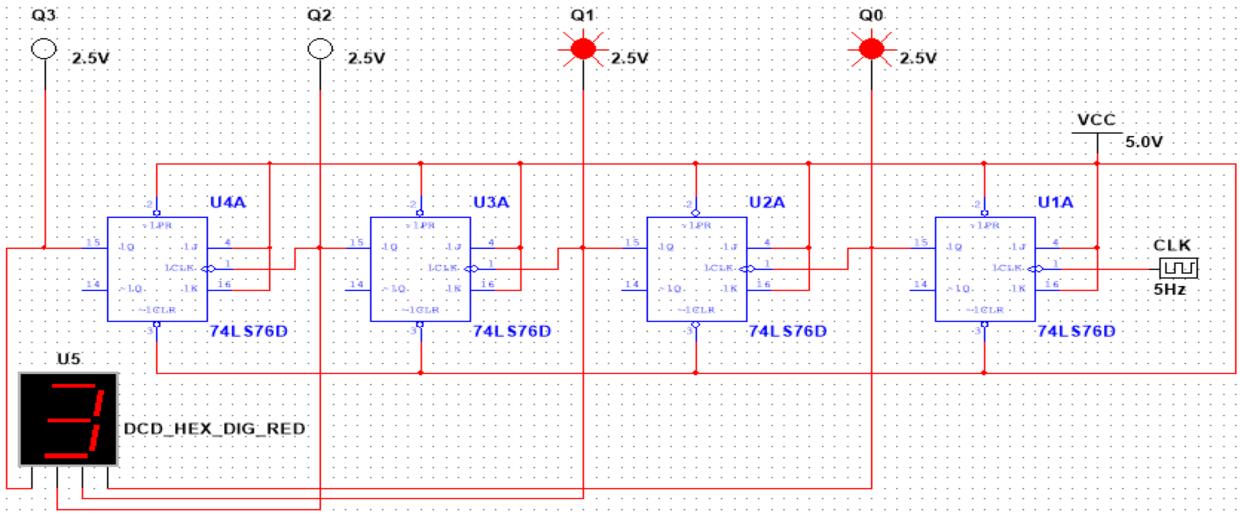


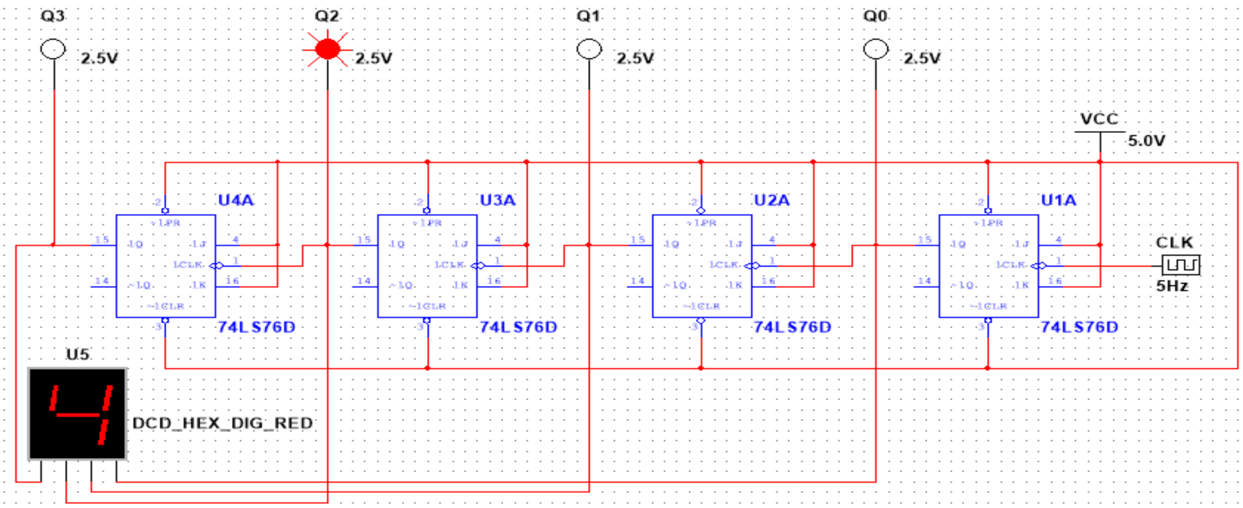
4-bit Asynchronous Up Counter:

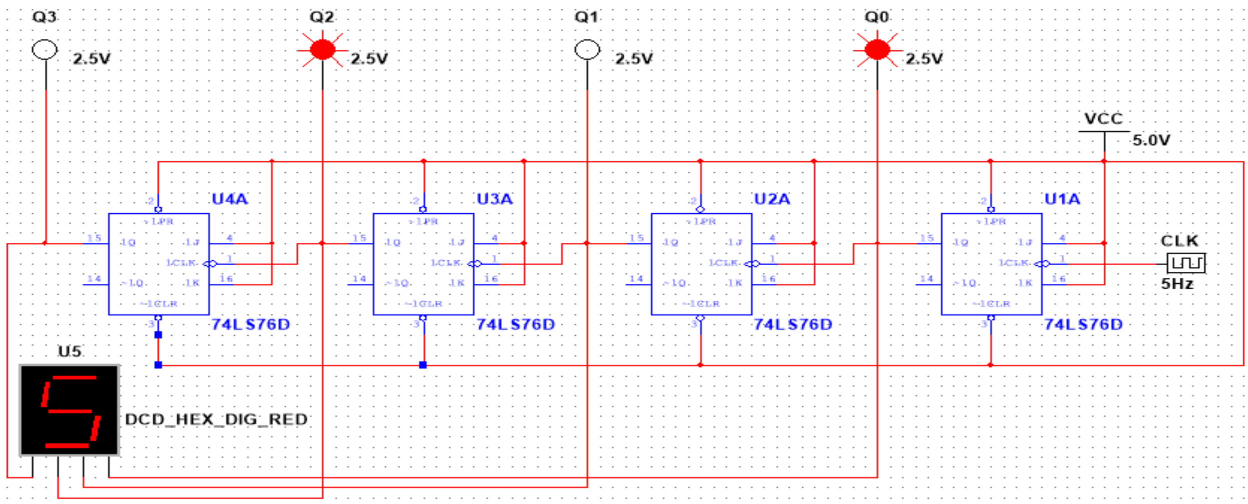


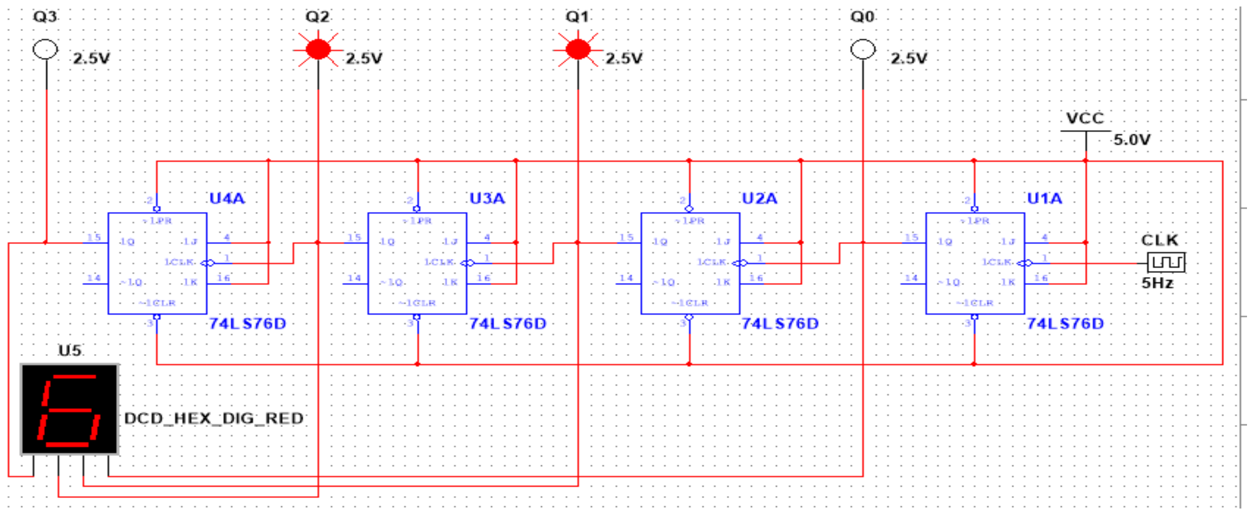

Q3
2.5V
Q2
2.5V
Q1
2.5V
Q0
2.5V
VCC
5.0V
U4A
U3A
U2A
U1A
74LS76D
74LS76D
74LS76D
74LS76D
CLK
5Hz
U5
DCD_HEX_DIG_RED

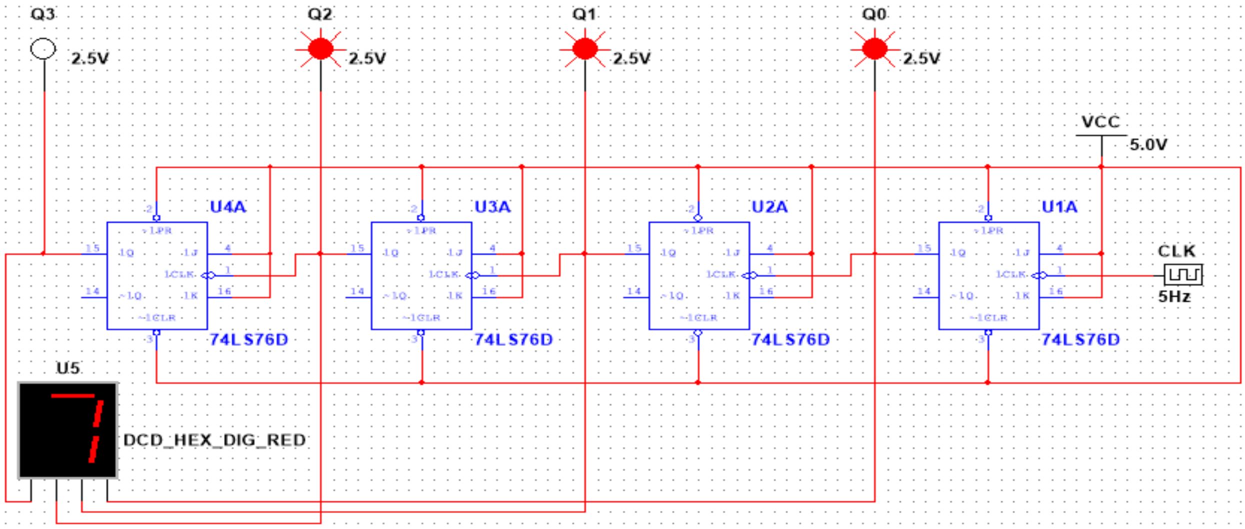

Q3
2.5V
Q2
2.5V
Q1
2.5V
Q0
2.5V
VCC
5.0V
U4A
U3A
U2A
U1A
74LS76D
74LS76D
74LS76D
74LS76D
CLK
5Hz
U5
DCD_HEX_DIG_RED

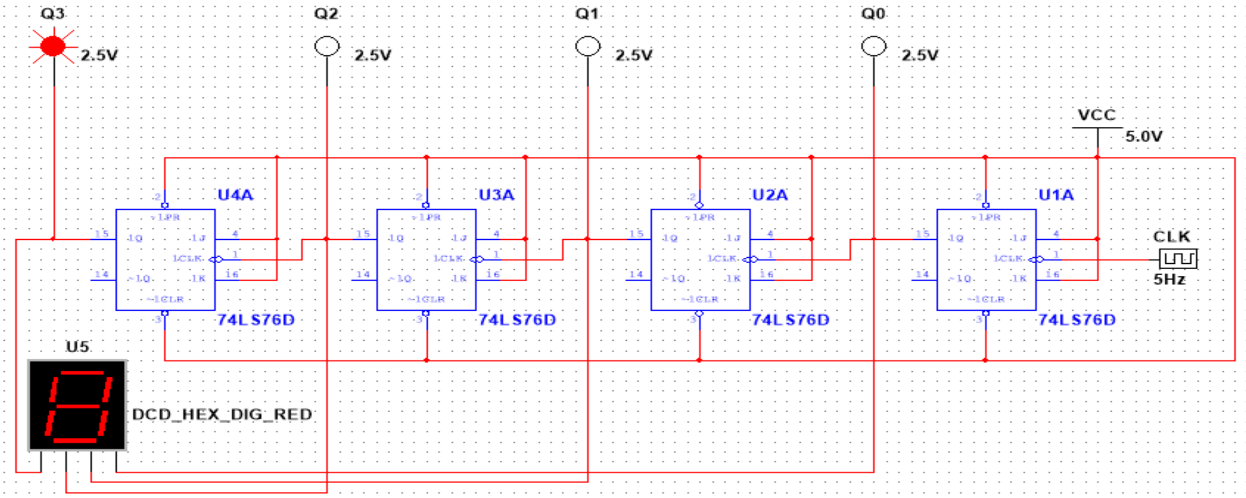

Q3
2.5V
Q2
2.5V
Q1
2.5V
Q0
2.5V
VCC
5.0V
U4A
U3A
U2A
U1A
74LS76D
74LS76D
74LS76D
74LS76D
CLK
5Hz
U5
DCD_HEX_DIG_RED


Q3
Q2
Q1
Q0
2.5V
2.5V
2.5V
2.5V
VCC
5.0V
U4A
U3A
U2A
U1A
74LS76D
74LS76D
74LS76D
74LS76D
CLK
5Hz
U5
DCD_HEX_DIG_RED


Q3
Q2
Q1
Q0
2.5V
2.5V
2.5V
2.5V
VCC
5.0V
U4A
U3A
U2A
U1A
74LS76D
74LS76D
74LS76D
74LS76D
CLK
5Hz
U5
DCD_HEX_DIG_RED


Q3
Q2
Q1
Q0
2.5V
2.5V
2.5V
2.5V
VCC
5.0V
U4A
U3A
U2A
U1A
74LS76D
74LS76D
74LS76D
74LS76D
CLK
5Hz
U5
DCD_HEX_DIG_RED


Q3
2.5V
Q2
2.5V
Q1
2.5V
Q0
2.5V
VCC
5.0V
U4A
U3A
U2A
U1A
CLK
5Hz
74LS76D
74LS76D
74LS76D
74LS76D
U5
DCD_HEX_DIG_RED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Q2
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Q0
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VCC
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CLK
5Hz
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74LS76D
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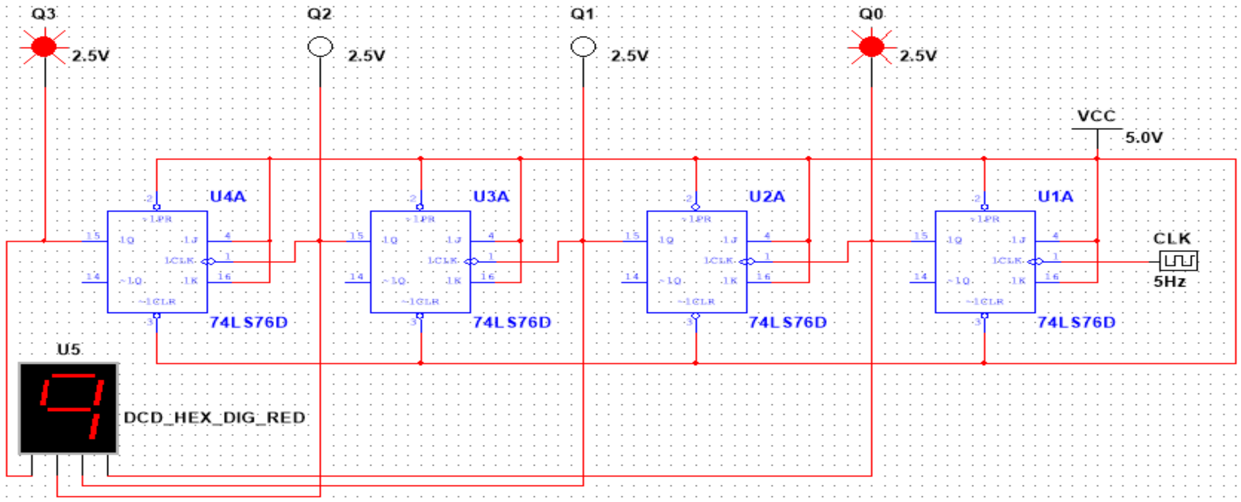
DCD_HEX_DIG_RED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Q0
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VCC
5.0V
U4A
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U2A
U1A
CLK
5Hz
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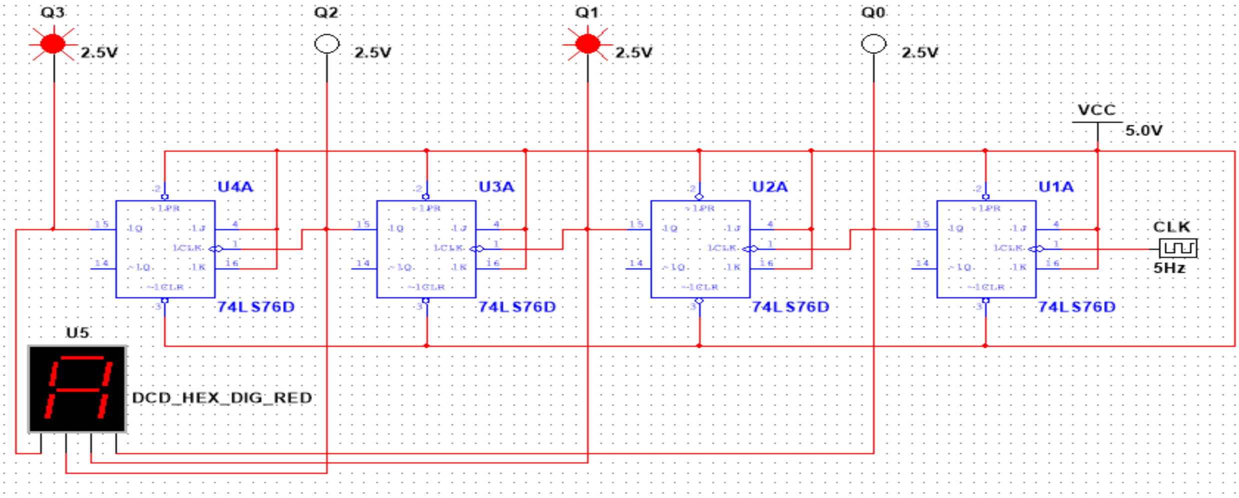
74LS76D
74LS76D
U5
DCD_HEX_DIG_RED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Q2
2.5V
Q1
2.5V
Q0
2.5V
VCC
5.0V
U4A
U3A
U2A
U1A
74LS76D
74LS76D
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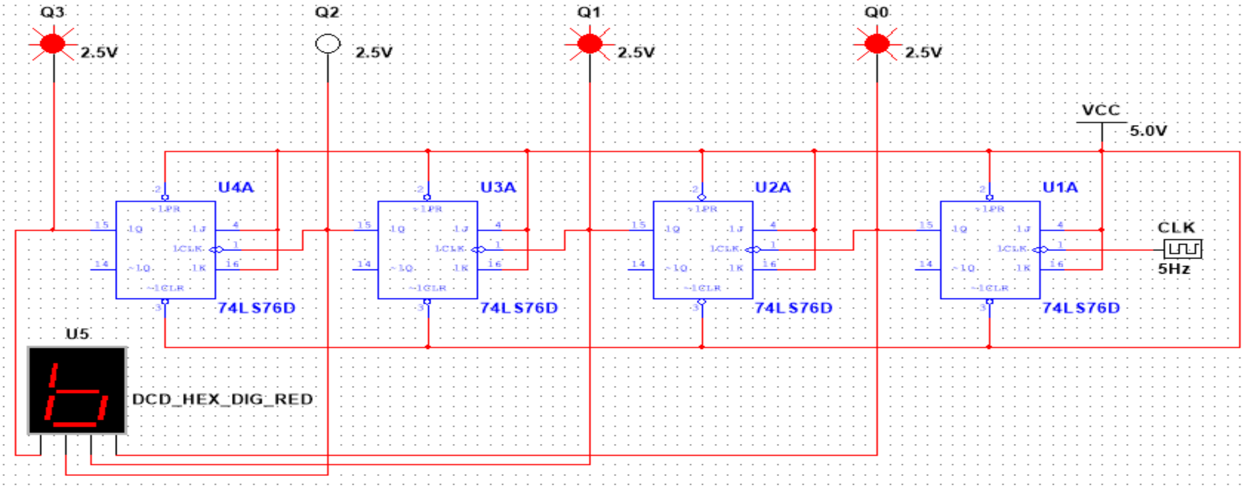
74LS76D
CLK
5Hz
U5
DCD_HEX_DIG_RED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Q2
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Q1
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Q0
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VCC
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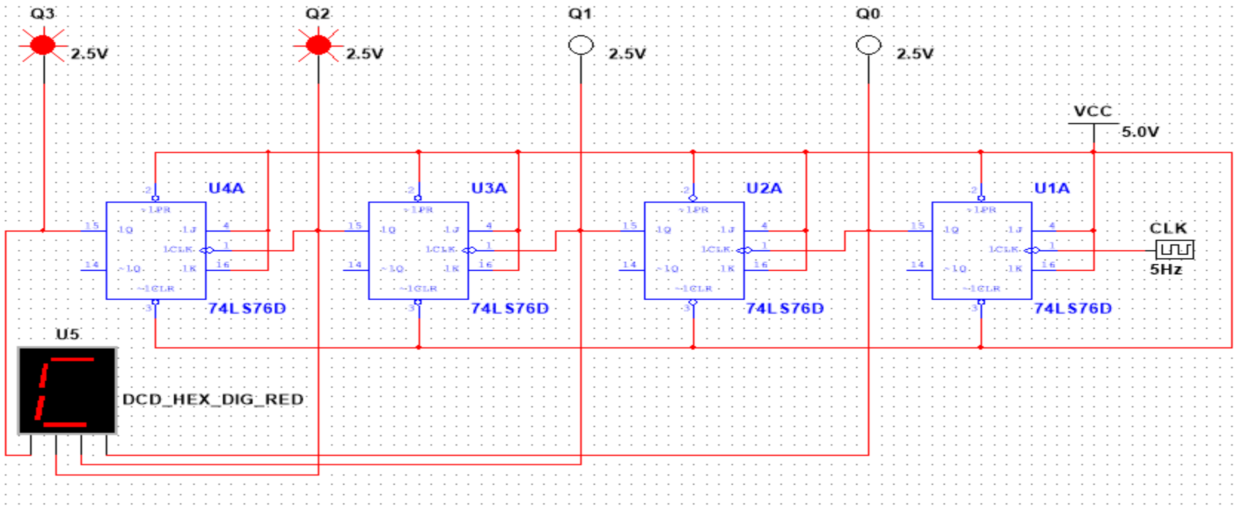
U2A
U1A
74LS76D
74LS76D
74LS76D
74LS76D
CLK
5Hz
U5
DCD_HEX_DIG_RED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Q0
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VCC
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U4A
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74LS76D
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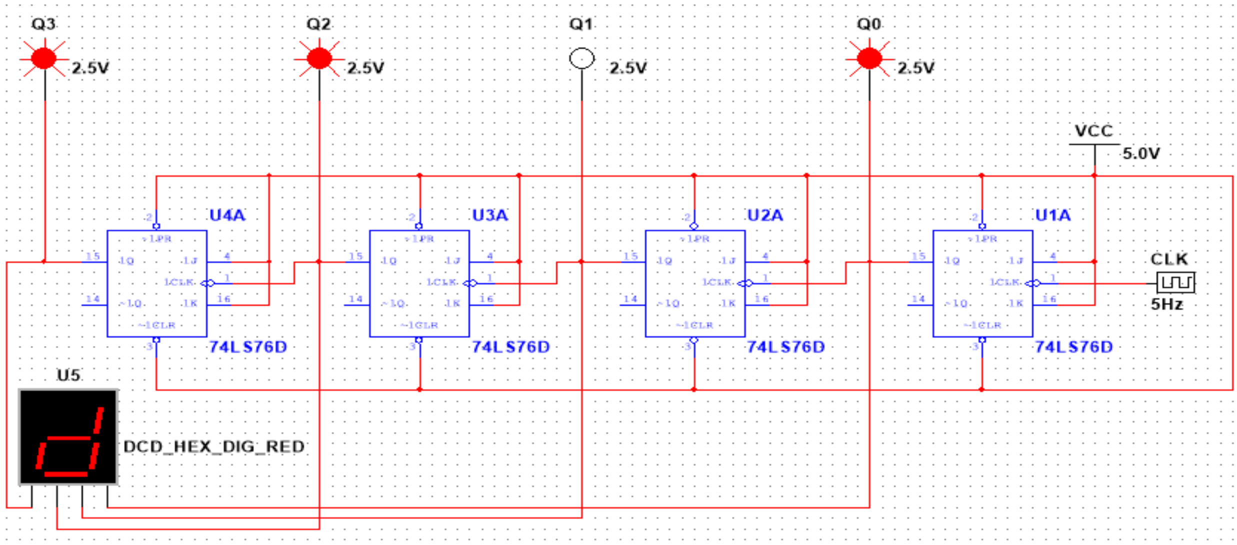
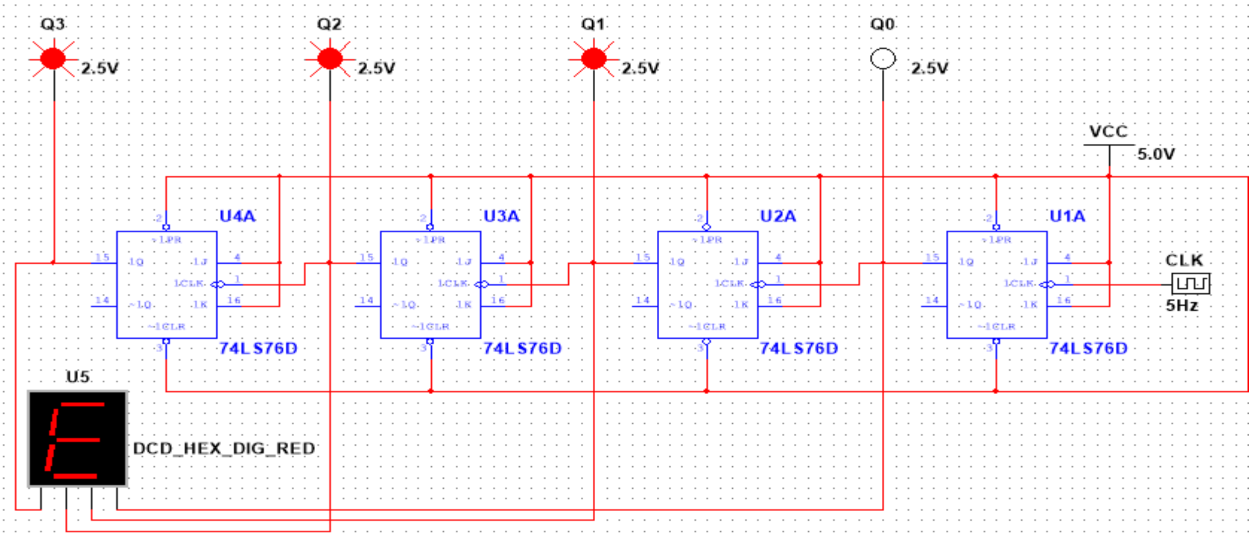
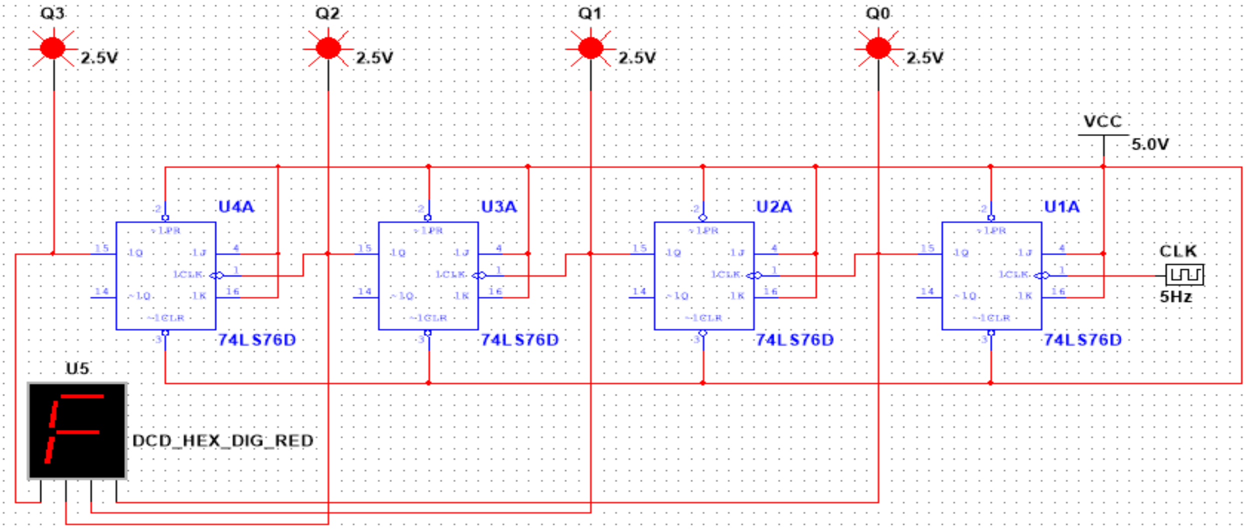
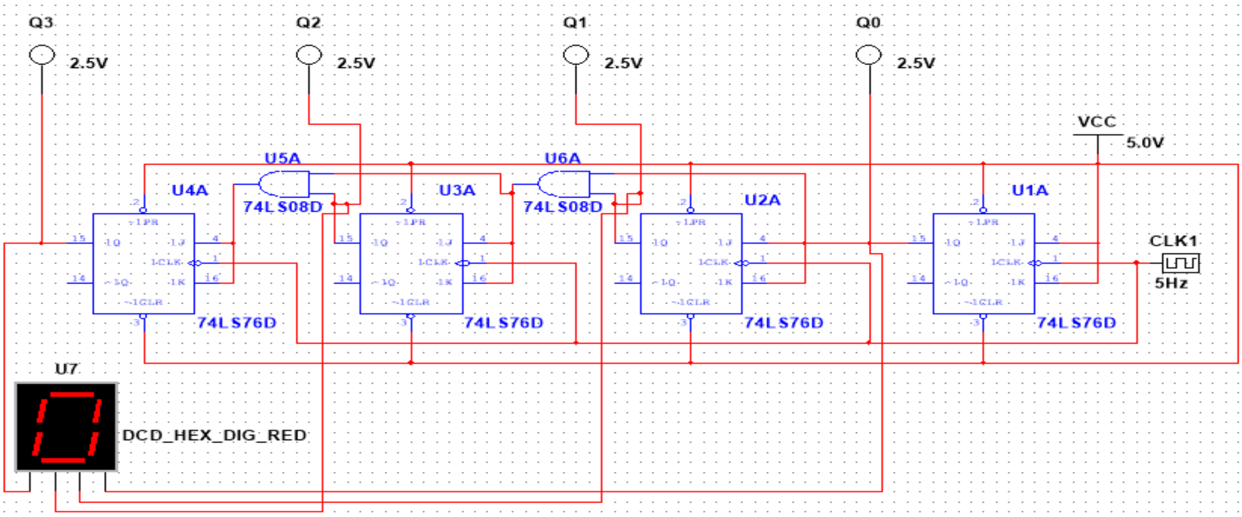
74LS76D
CLK
5Hz
U5
DCD_HEX_DIG_RED







4-bit Synchronous Up Counter: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Q2
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Q1
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Q0
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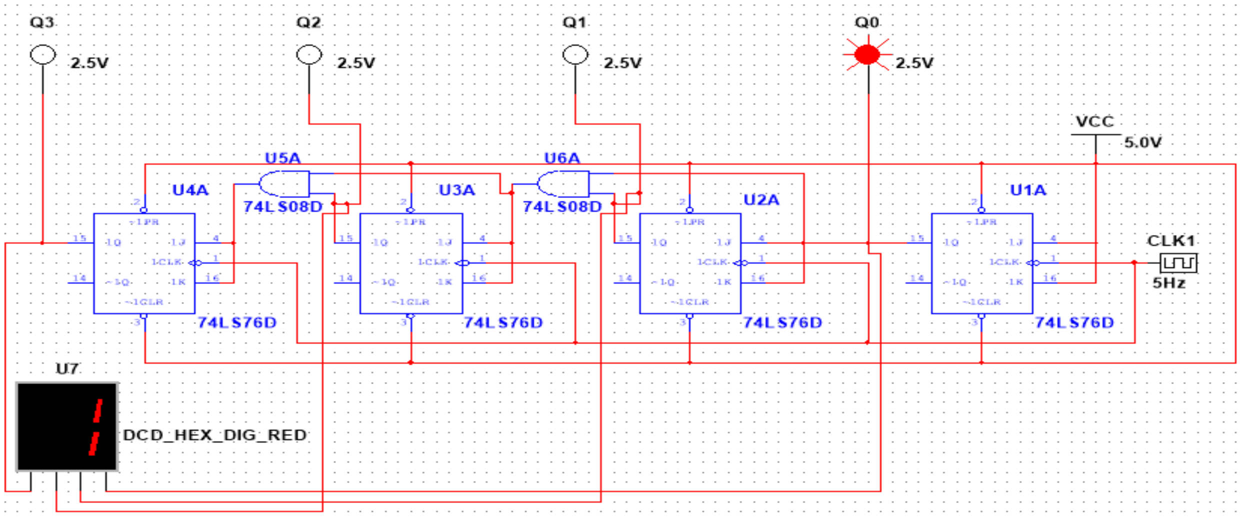
VCC
5.0V
U5A
74LS08D
U6A
74LS08D
U4A
U3A
U2A
U1A
74LS76D
74LS76D
74LS76D
74LS76D
CLK1
5Hz
U7
DCD_HEX_DIG_RED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Q0
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VCC
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U5A
74LS08D
U6A
74LS08D
U4A
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U2A
U1A
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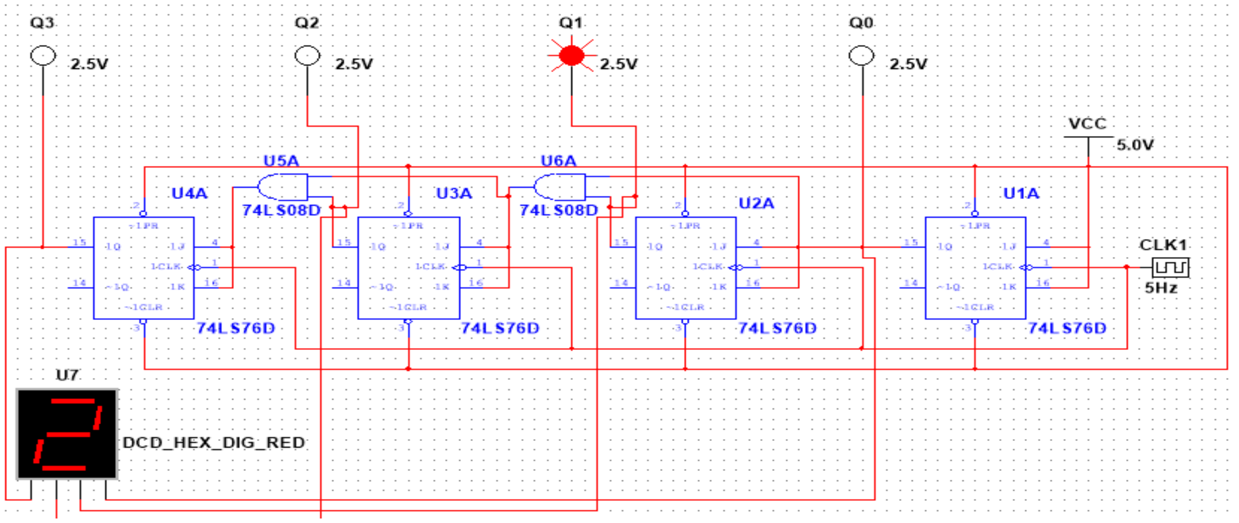
74LS76D
CLK1
5Hz
U7
DCD_HEX_DIG_RED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Q1
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Q0
2.5V
VCC
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U5A
74LS08D
U6A
74LS08D
U4A
U3A
U2A
U1A
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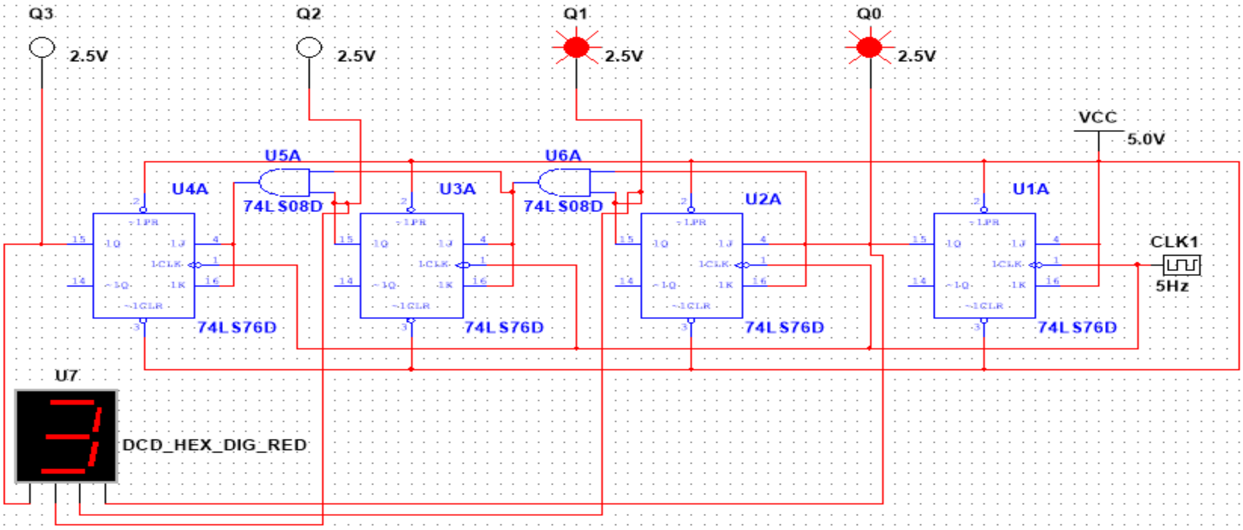
74LS76D
74LS76D
74LS76D
CLK1
5Hz
U7
DCD_HEX_DIG_RED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Q2
2.5V
Q1
2.5V
Q0
2.5V
VCC
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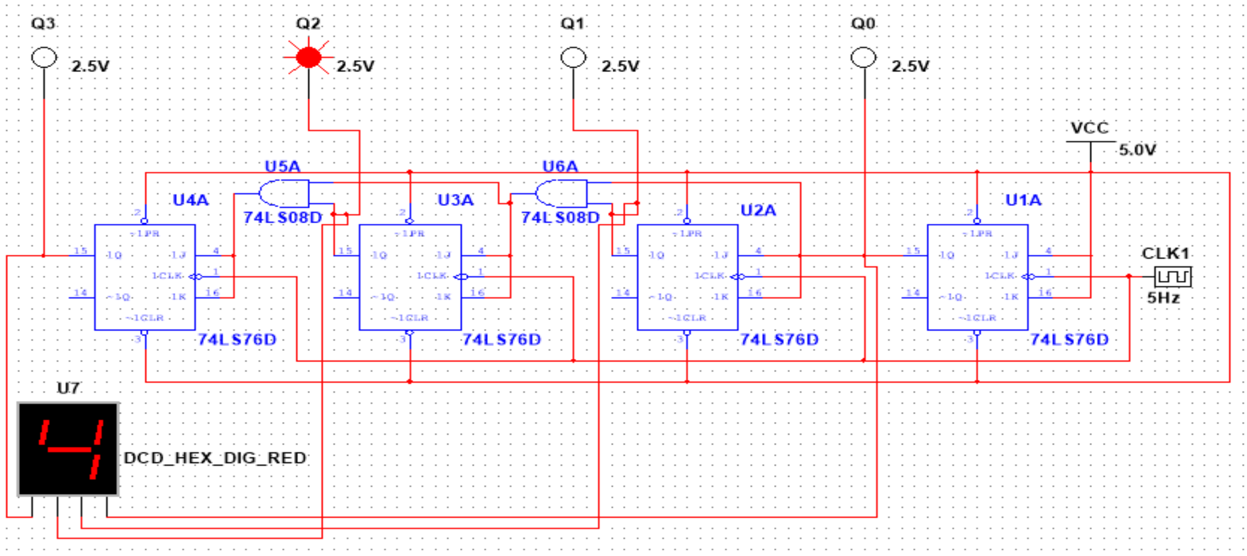
U5A
74LS08D
U6A
74LS08D
U4A
U3A
U2A
U1A
74LS76D
74LS76D
74LS76D
74LS76D
CLK1
5Hz
U7
DCD_HEX_DIG_RED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Q2
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Q1
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Q0
2.5V
VCC
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U5A
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U6A
74LS08D
U4A
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U2A
U1A
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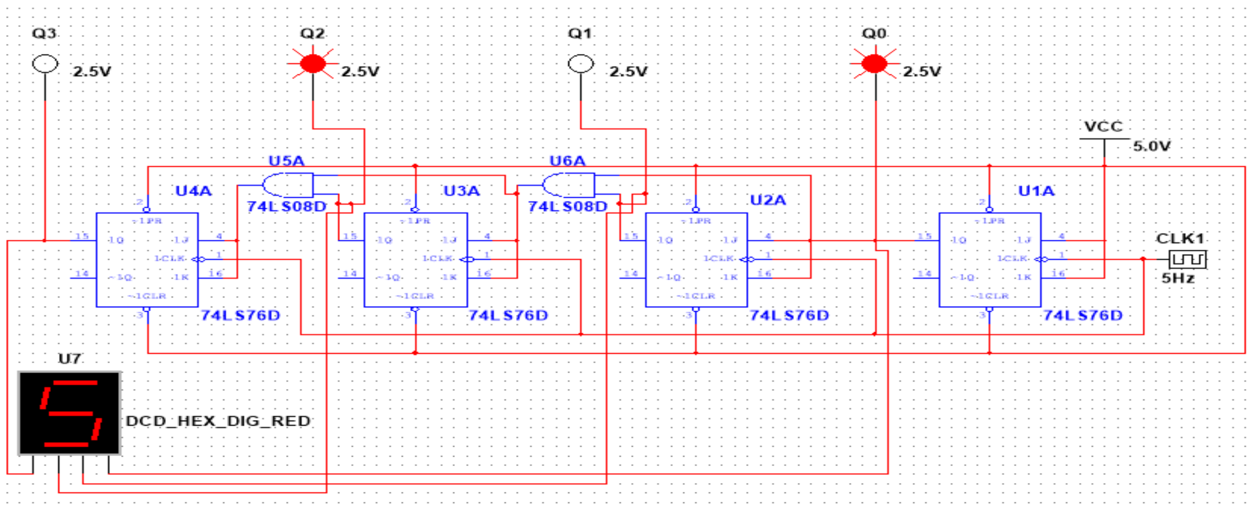
74LS76D
CLK1
5Hz
U7
DCD_HEX_DIG_RED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Q2
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Q1
2.5V
Q0
2.5V
VCC
5.0V
U5A
74LS08D
U6A
74LS08D
U4A
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U2A
U1A
74LS76D
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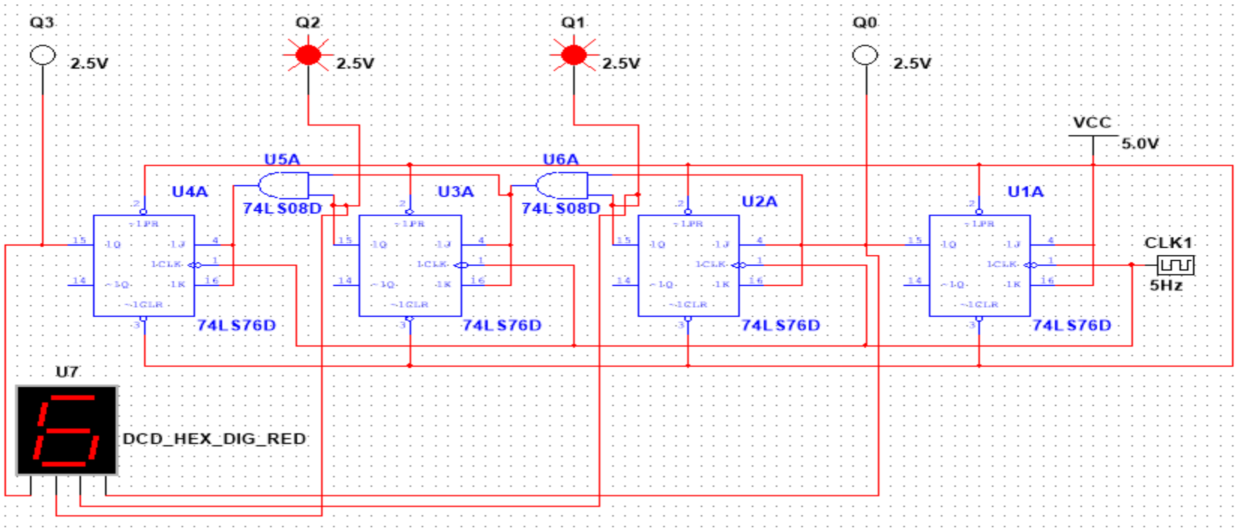
CLK1
5Hz
U7
DCD_HEX_DIG_RED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Q2
2.5V
Q1
2.5V
Q0
2.5V
VCC
5.0V
U5A
74LS08D
U6A
74LS08D
U4A
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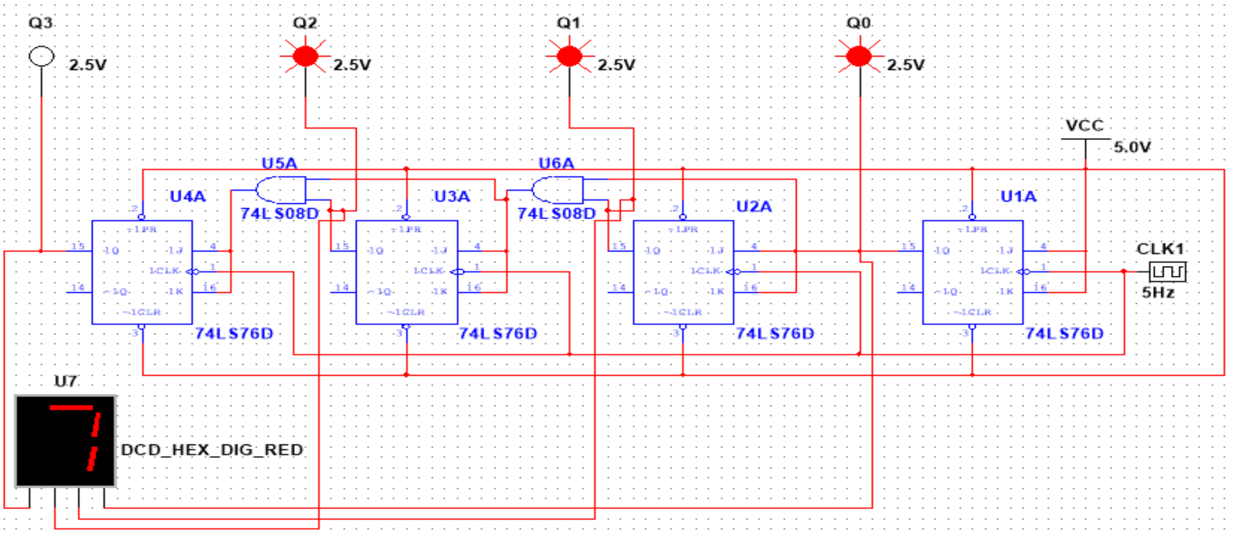
U2A
U1A
74LS76D
74LS76D
74LS76D
74LS76D
CLK1
5Hz
U7
DCD_HEX_DIG_RED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Q2
2.5V
Q1
2.5V
Q0
2.5V
VCC
5.0V
U5A
74LS08D
U6A
74LS08D
U4A
U3A
U2A
U1A
74LS76D
74LS76D
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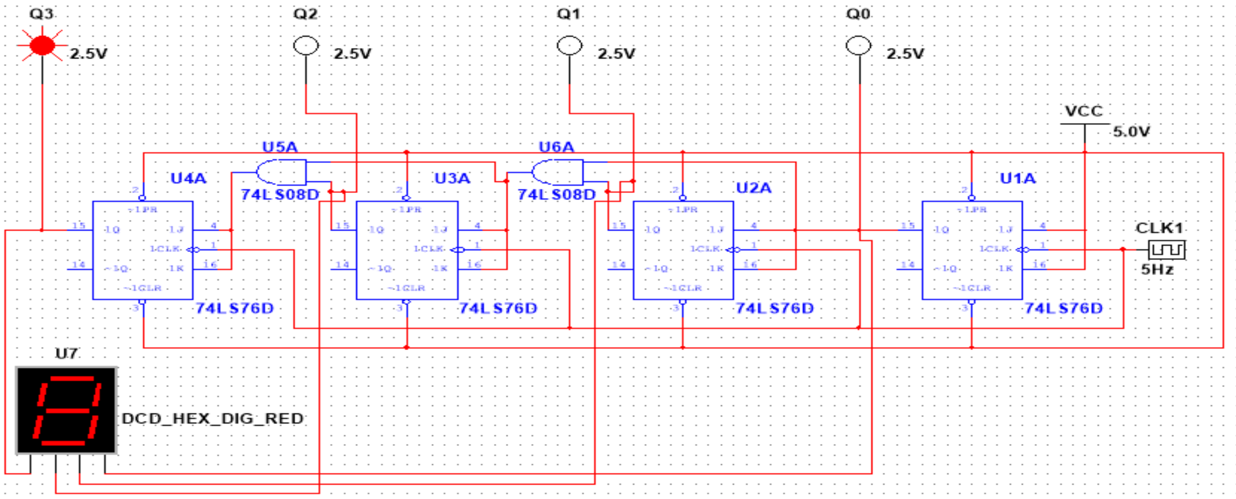
CLK1
5Hz
U7
DCD_HEX_DIG_RED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Q2
2.5V
Q1
2.5V
Q0
2.5V
VCC
5.0V
U5A
74LS08D
U6A
74LS08D
U4A
U3A
U2A
U1A
74LS76D
74LS76D
74LS76D
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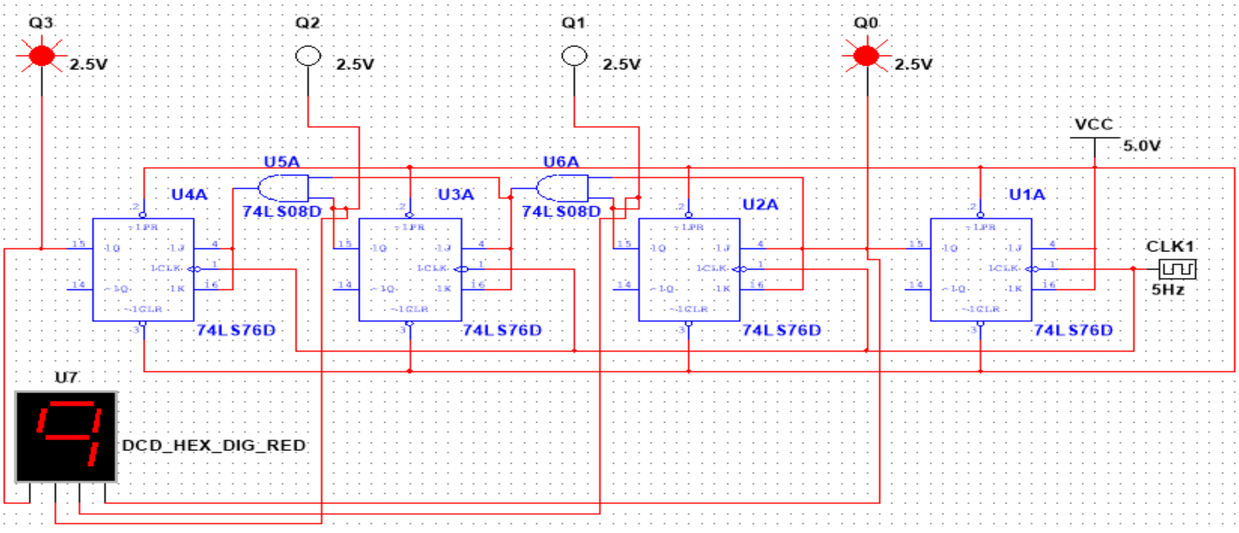
CLK1
5Hz
U7
DCD_HEX_DIG_RED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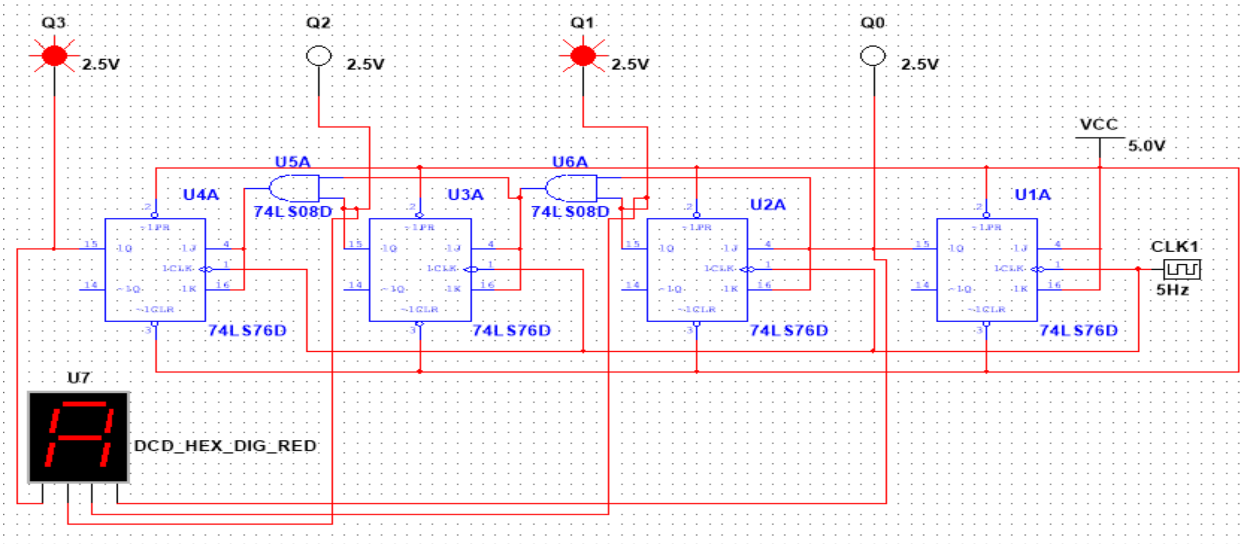
Q2
2.5V
Q1
2.5V
Q0
2.5V
VCC
5.0V
U5A
74LS08D
U6A
74LS08D
U4A
U3A
U2A
U1A
74LS76D
74LS76D
74LS76D
74LS76D
CLK1
5Hz
U7
DCD_HEX_DIG_RED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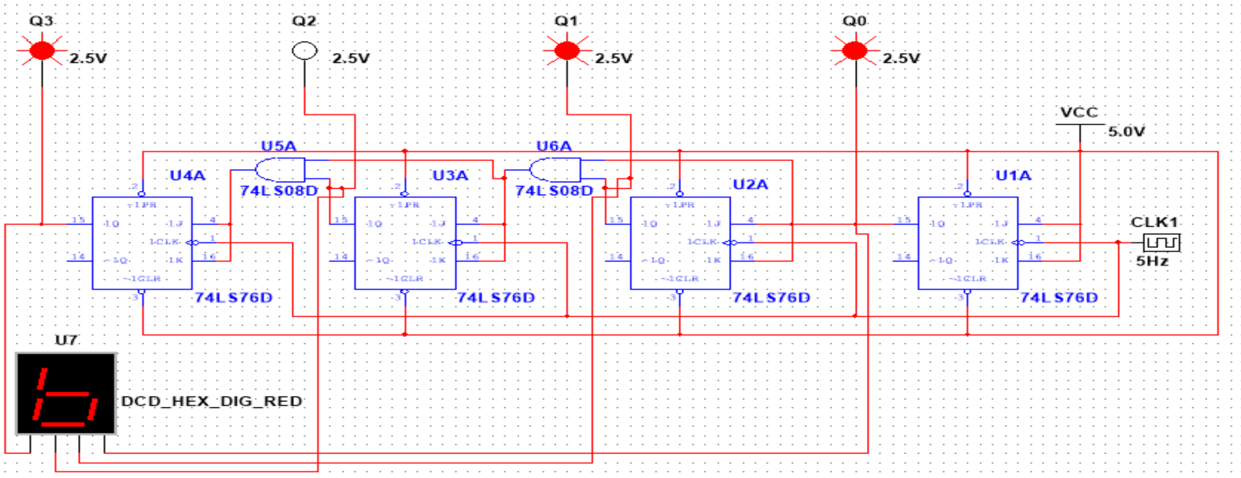
Q2
2.5V
Q1
2.5V
Q0
2.5V
VCC
5.0V
U5A
74LS08D
U6A
74LS08D
U4A
U3A
U2A
U1A
74LS76D
74LS76D
74LS76D
74LS76D
CLK1
5Hz
U7
DCD_HEX_DIG_RED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Q2
2.5V
Q1
2.5V
Q0
2.5V
VCC
5.0V
U5A
74LS08D
U6A
74LS08D
U4A
U3A
U2A
U1A
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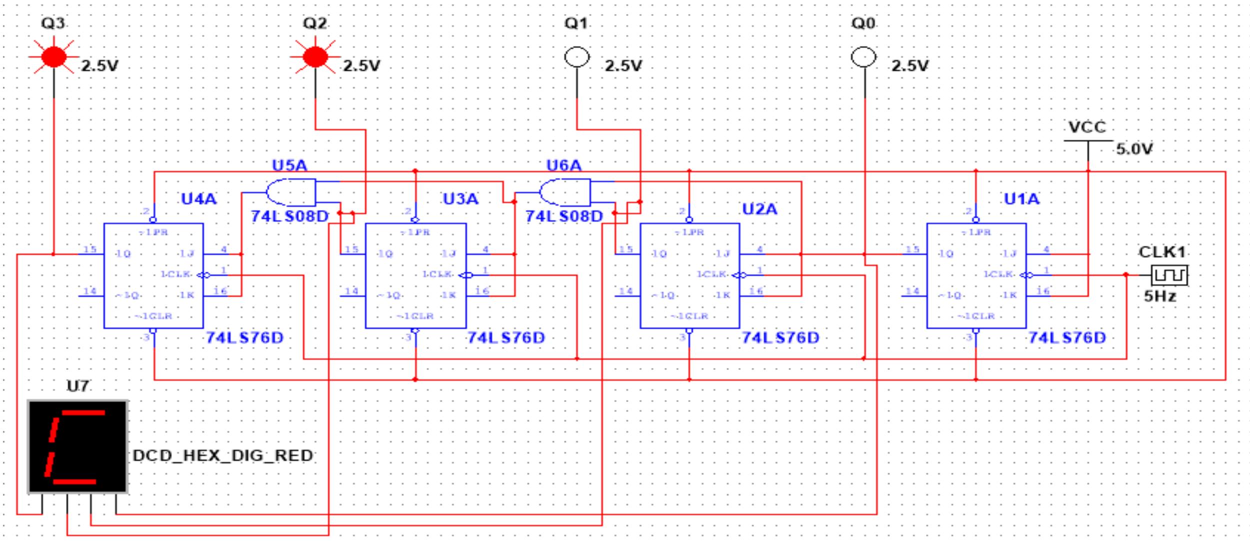
74LS76D
74LS76D
74LS76D
CLK1
5Hz
U7
DCD_HEX_DIG_RED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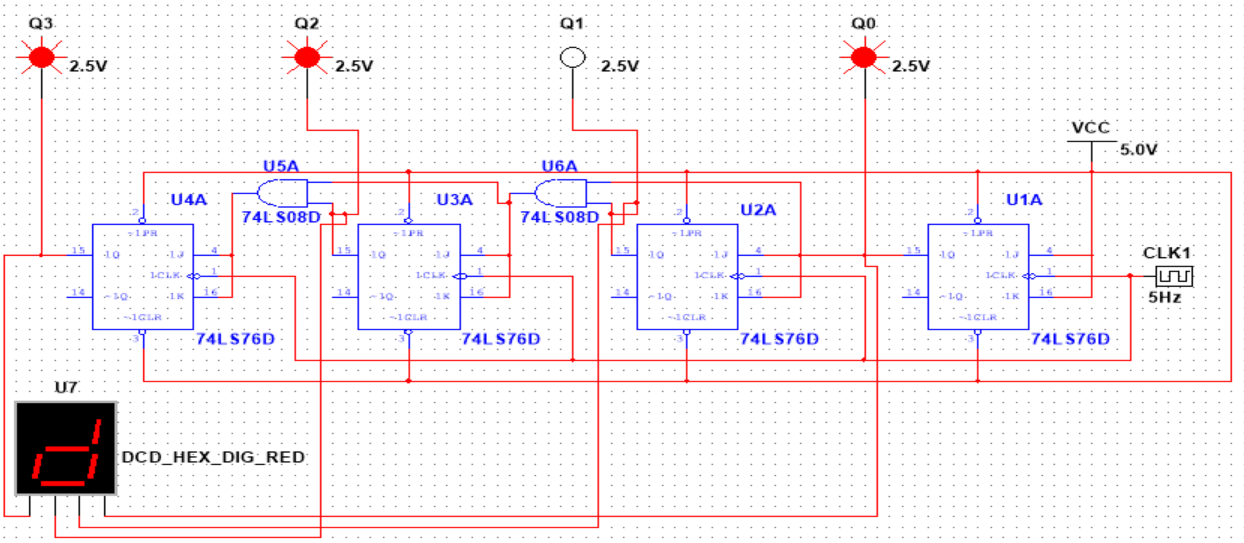
Q2
2.5V
Q1
2.5V
Q0
2.5V
VCC
5.0V
U5A
74LS08D
U6A
74LS08D
U4A
U3A
U2A
U1A
74LS76D
74LS76D
74LS76D
74LS76D
CLK1
5Hz
U7
DCD_HEX_DIG_RED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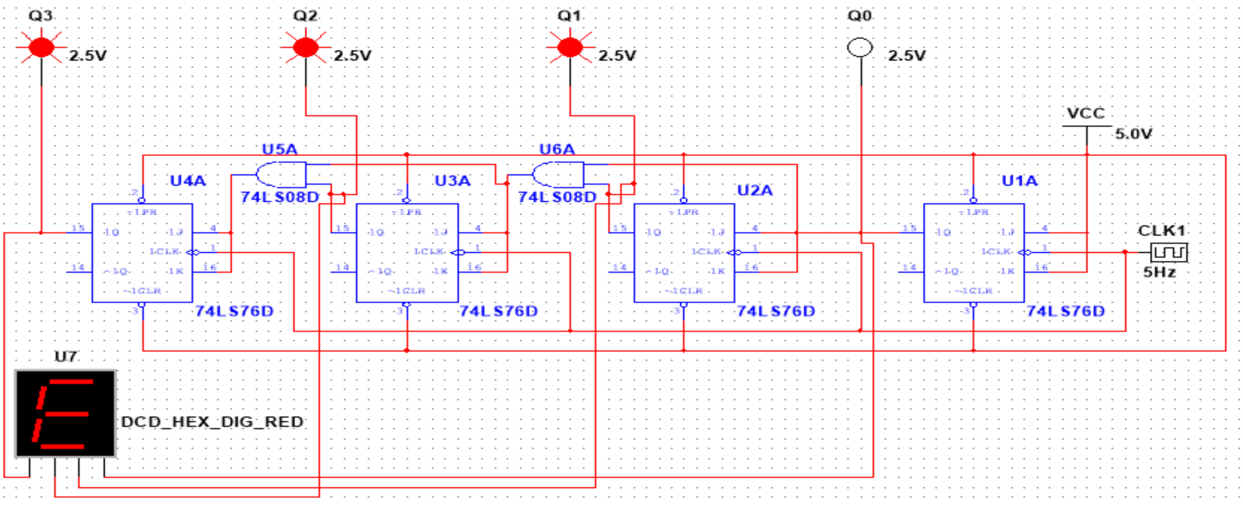
Q2
2.5V
Q1
2.5V
Q0
2.5V
VCC
5.0V
U5A
74LS08D
U6A
74LS08D
U4A
U3A
U2A
U1A
74LS76D
74LS76D
74LS76D
74LS76D
CLK1
5Hz
U7
DCD_HEX_DIG_RED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Q1
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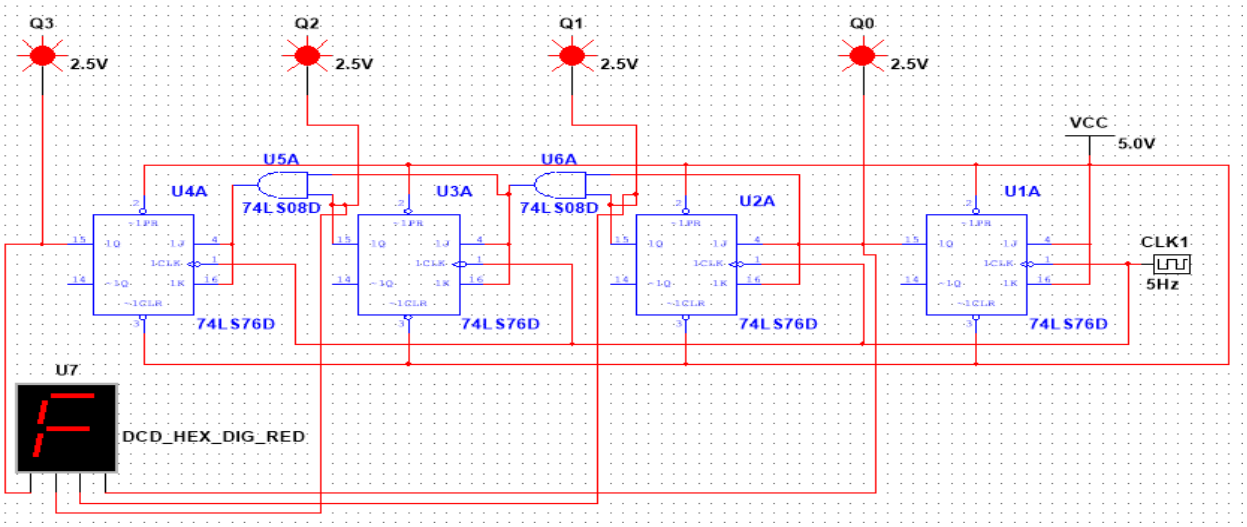
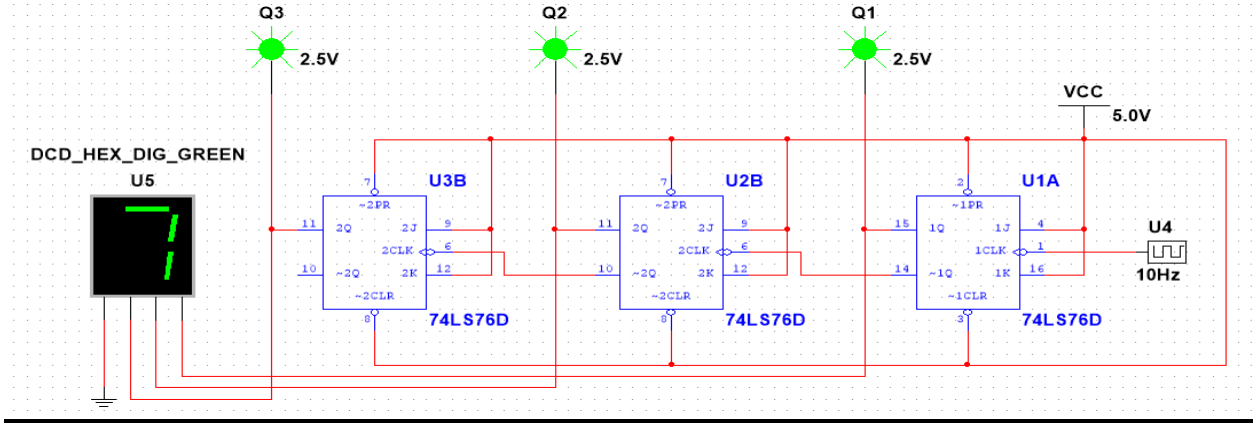
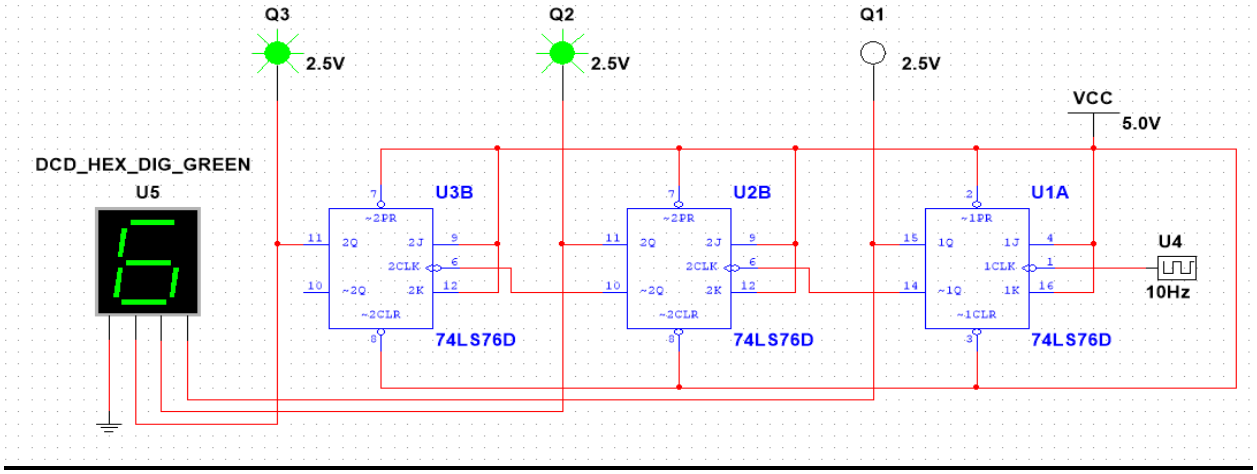
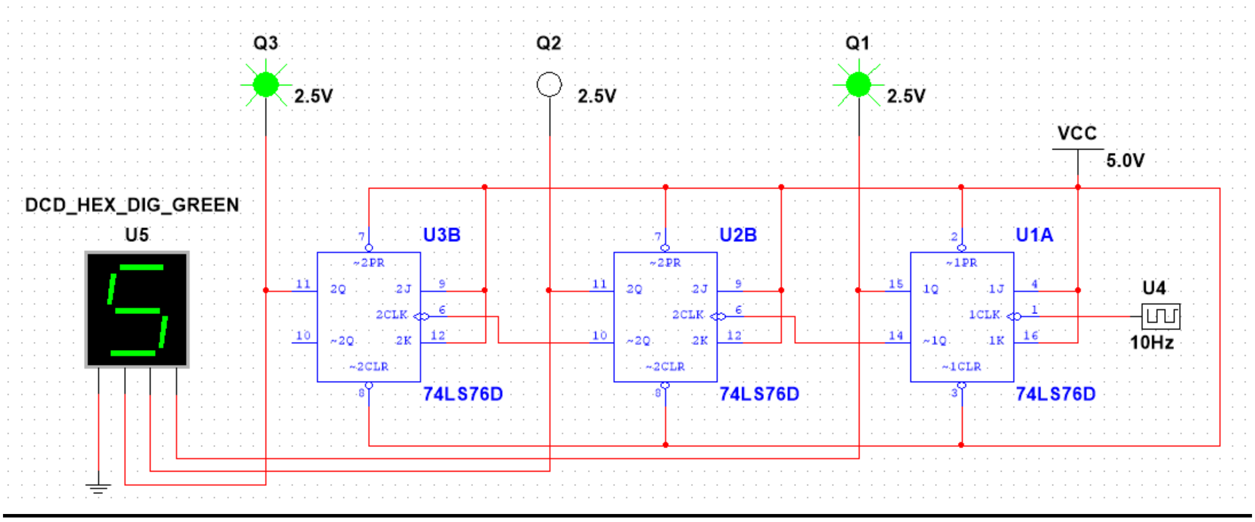
Q0
2.5V
VCC
5.0V
U5A
74LS08D
U6A
74LS08D
U4A
U3A
U2A
U1A
74LS76D
74LS76D
74LS76D
74LS76D
CLK1
5Hz
U7
DCD_HEX_DIG_RED



3-bit Asynchronous down counter



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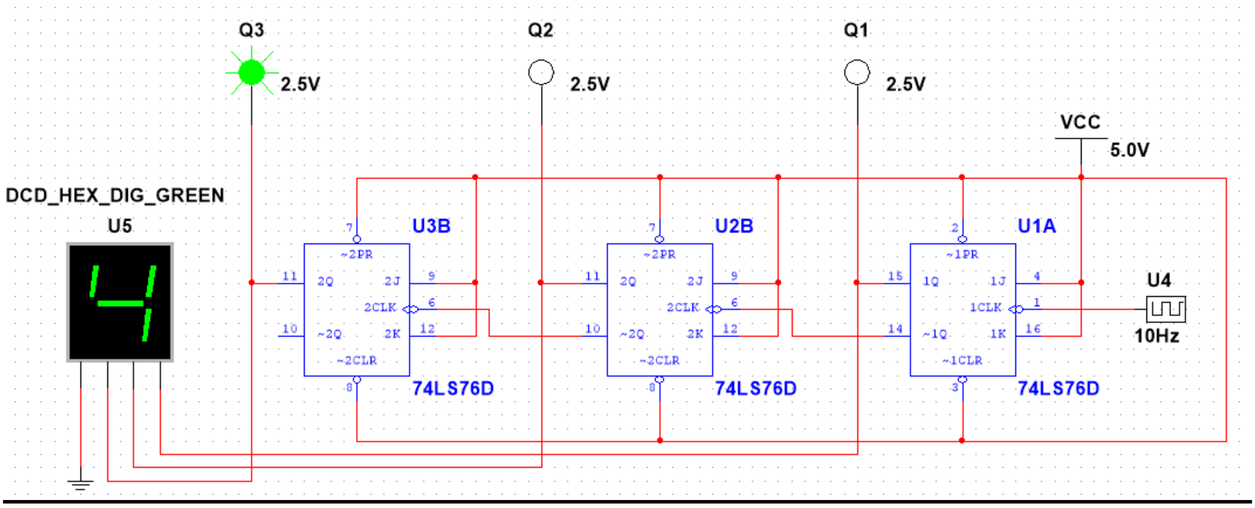
Q2
2.5V
Q1
2.5V
VCC
5.0V
DCD_HEX_DIG_GREEN
U5
U3B
U2B
U1A
74LS76D
74LS76D
74LS76D
U4
10Hz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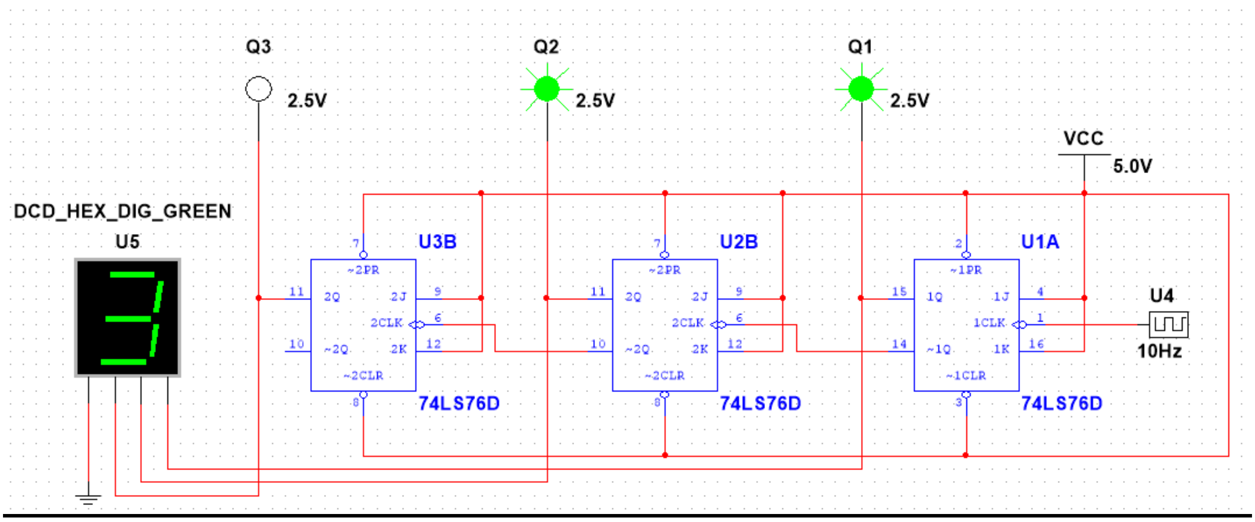
2.5V
Q2
2.5V
Q1
2.5V
VCC
5.0V
DCD_HEX_DIG_GREEN
U5
U3B
U2B
U1A
74LS76D
74LS76D
74LS76D
U4
10Hz


Q3
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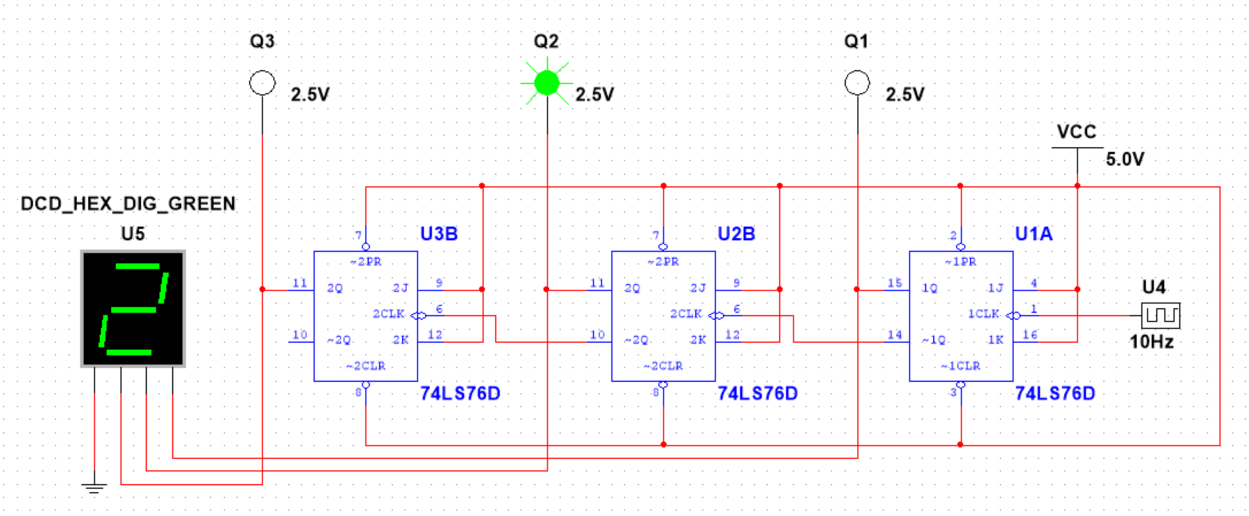
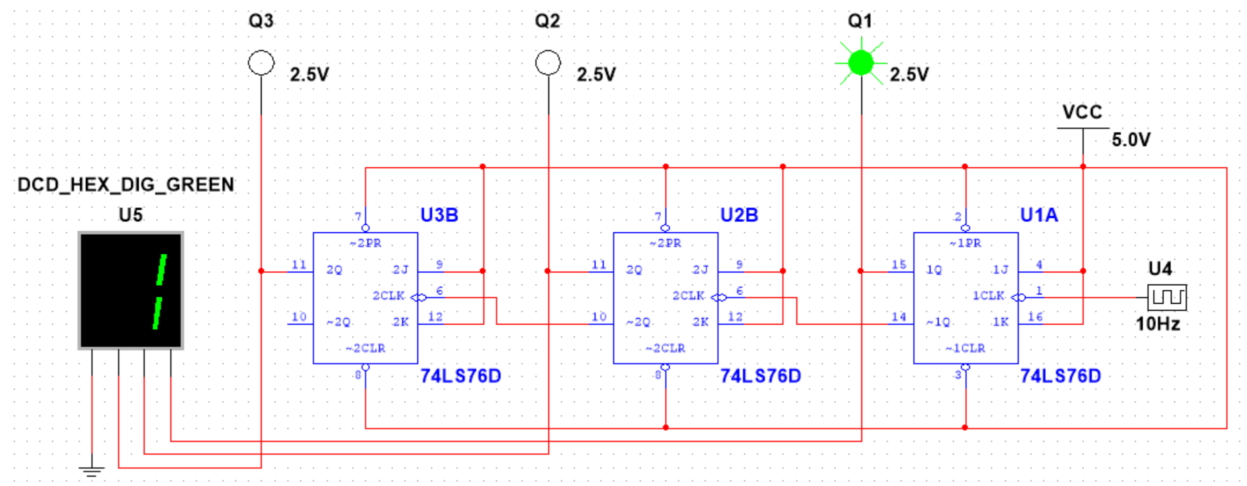
Q2
2.5V
Q1
2.5V
VCC
5.0V
DCD_HEX_DIG_GREEN
U5
U3B
U2B
U1A
74LS76D
74LS76D
74LS76D
U4
10Hz



Q3
2.5V
Q2
2.5V
Q1
2.5V
VCC
5.0V
DCD_HEX_DIG_GREEN
U5
U3B
U2B
U1A
U4
10Hz
74LS76D
74LS76D
74LS76D



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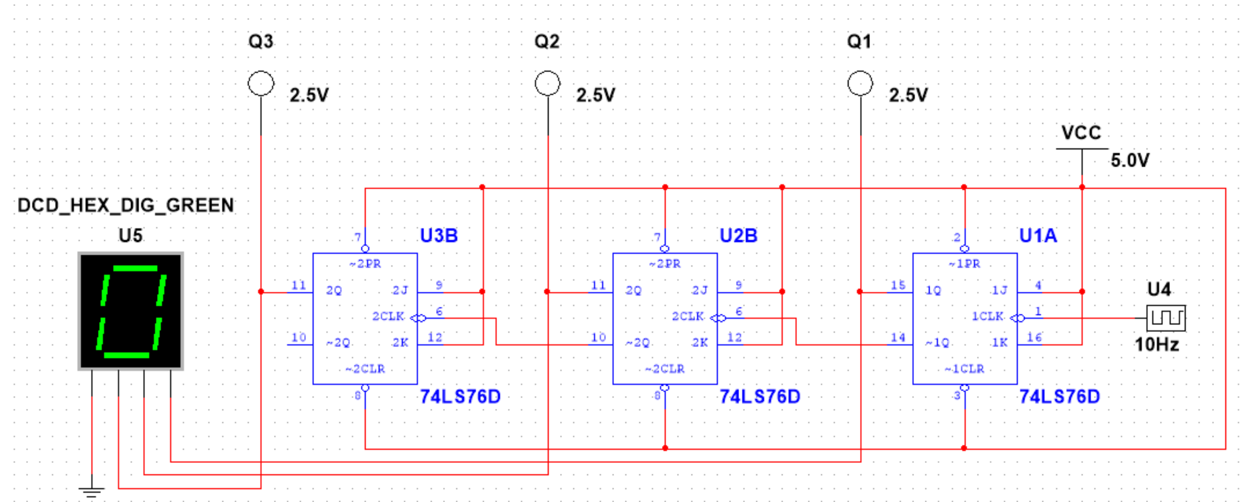
2.5V
Q2
2.5V
Q1
2.5V
VCC
5.0V
DCD_HEX_DIG_GREEN
U5
U3B
U2B
U1A
U4
10Hz
74LS76D
74LS76D
74LS76D



Q3
2.5V
Q2
2.5V
Q1
2.5V
VCC
5.0V
DCD_HEX_DIG_GREEN
U5
U3B
U2B
U1A
U4
10Hz
74LS76D
74LS76D
74LS76D

Results: The Simulation results matched the hardware implementation.

Discussion:

The experiment involved two parts: Asynchronous and Synchronous counters using a trainer board and JK Flip Flop IC. Initially, the Asynchronous counter used an external clock for the first flip-flop and cascaded outputs for subsequent ones, making it slower but simple. In contrast, the Synchronous counter employed a universal clock, allowing simultaneous flip-flop operation for higher speed, albeit with a more complex circuit. Designing and implementing 3-bit versions of both counters provided valuable insights into their processes and circuits.

Reference:

1. Thomas L. Floyd, "Digital Fundamentals," available Edition, Prentice Hall International Inc.