Yuchuan Li
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EDUCATION

University of California San Diego **San Diego, CA**
Master of Science in Electrical and Computer Engineering | GPA 3.7 Expected 12/2024

- Relevant Courses: Digital System Algorithms and Architecture, Computer Architecture, VLSI Implementation for machine learning, System Design for Deep Learning, VLSI Advanced Topics, Programming for Data Analysis.

The University of Edinburgh **Edinburgh, UK**
Bachelor of Engineering in Electrical and Electronic Engineering (Honors) | GPA 3.5 06/2019

TECHNICAL SKILLS

Skills: Logic Synthesis, Static-Timing Analysis (STA), Physical Design (PnR), Verilog Design and Verification, Machine Learning Accelerator, Low Power Implementation, Formal Verification, Functional and Timing ECO.
Programming Language: Tcl, Python, Verilog, System Verilog, UVM, UPF, Shell, Perl.
EDA Tool: Design Compiler, Prime Time, Formality, Innovus, VCLP, Virtuoso.

PROFESSIONAL EXPERIENCE

Hisilicon, HUAWEI **Shanghai, China**
Physical Design and Timing Engineer - Kirin SoC Team 03/2020 – 03/2023

Logic Synthesis and Physical Design

- Led floorplanning and physical synthesis for the 5nm SoC subsystems (CPU/Media), focusing on PPA optimization and congestion prediction.
- Conducted data-flow driven floorplanning, macro/pin placement for the media display module, achieving a 6% reduction in Low-Vth cell usage and mitigating congestion risks.
- Reduced the leakage power of CPU little core by 5% by utilizing MCMM synthesis and the Multi-Vth cell strategy.
- Executed partition level PnR flow including floorplanning, placement, CTS, routing, and DRC fixing.
- Led formal verification and ECO implementation for functional, DFT, and timing aspects.

Static-Timing Analysis

- Owned SoC subsystems timing closure and sign-off. Experienced with STA considering PVT corner, timing margins, process variations, signal integrity, and multi power domains.
- Developed timing constraints for clock domain crossing, exception, block I/O timing, and multi-voltage design, achieving timing closure for a complex SoC submodule.
- Recognized as the top contributor for improving EDA workflow efficiency by developing Tcl and Python scripts.
- Developed a performance prediction model across different technology nodes, voltages and Low-Vth cell percentages.

Low Power Implementation and Verification

- Implemented SoC Power Structure, including more than 20 power domains, complicated power-off strategy and multi-voltage design on netlist, proficient in UPF and VCLP low power verification.
- Led full-chip low-power design verification and sign-off check, including critical aspects like power connections for memory, isolation and level shifter cells, physical IP and always-on special signals.

RESEARCH EXPERIENCE

University of California San Diego **San Diego, CA**
Graduate Student Researcher – VVIP Lab 03/2024 – Present

Deep Learning Accelerator ASIC Tape-Out

- Implemented an AI accelerator tailored for Convolutional Neural Networks (CNNs) and Transformer models.
- Mapped deep learning algorithms to datapath, including systolic array, softmax function, special function unit.
- Developed a novel dataflow ISA for the accelerator, optimizing performance for systolic array based architectures.
- Programmed an FSM micro-controller and asynchronous I/O interface for the AI accelerator to manage control signals and data flow.
- Managed the entire RTL to GDS flow, including RTL design and verification, physical design and timing closure.

RISC-V AI Accelerator for Mamba

- Accelerated Mamba model by RISC-V Accelerator to optimize both linear operation and element-wise operation.
- Implemented PE array, instruction processing unit, nonlinear function unit, normalization unit and on-chip buffer to accelerate matrix operation in Mamba.