NONA **RAJABI**

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PROFILE

I have recently graduated from Sharif university of technology, Tehran, Iran in the field of electrical engineering. Currently I am working as a research intern at National University of Singapore (NUS), school of computing in the field of networking and field programmable gate arrays (FPGA).

EDUCATION

Undergraduate student of Electrical Engineering | Sharif University of Technology

2015 – 2019

Selected Courses:

- Artificial Neural Networks (18.6/20)
- Electroencephalogram (EEG) signal processing (19.2/20)
- Data Communication Networks (18/20)
- Introduction to Machine Learning (18.5/20)
- System Dynamics (17.7/20)
- Parallel Programming and Architecture (20/20)
- Microprocessor Systems Design (19.5/20)
- ASIC/FPGA Systems Design (15.4/20)
- Communication Systems (19.6/20)
- Linear Control Systems (17/20)
- Computer Structure and Microprocessors (19.8/20)
- Probability and Statistics (18.8/20)
- Signals and Systems (16.4/20)

GPA 18.57/20 (3.93/4)

Mathematics & Physics Diploma | Farzanegan High school

2011 – 2015

GPA 19.9/20

Tehran's branch of National Organization for Development of Exceptional Talents (NODET)

HONORS & AWARDS

Iran's National Elites Foundation: Being a member due to standing among top students of university

National University Entrance Exam: Rank 29th among 300,000 students in university entrance exam

HIGHSCHOOL OLYMPIADS: being accepted at the first stage of national Mathematics Olympiad (2012 & 2013) and Literature Olympiad (2013)

SKILLS

Software Simulators:	MATLAB
Network Simulators/Analyzers:	NS3, GNS3, Mininet, Wireshark, Scapy, Moongen, Pcap++
Hardware Simulators:	PSPICE, PROTEUS, MODELSIM, ISE DESIGN, QUARTUS
Programming Languages:	C, C++, JAVA, ANDROID, PYTHON, Assembly (MIPS), P4 (Networking)
HDL:	VERILOG
OS:	WINDOWS, ANDROID, LINUX
Microcontrollers :	AVR, PIC-32, ARDUINO
FPGA boards :	DE2, DE270, ATLYS
Parallel Programming:	PTHREADS, GPU
Version Control:	GIT

RESEARCH INTEREST

- Systems & Networking
- Programmable Hardware (FPGA)
- Biomedical Signal Processing
- Machine Learning (mostly practical)

SELECTED ACADEMIC PROJECTS

Fair Queue Management & Time-Driven Execution Using NetFPGA | Networking

10.2019 – PRESENT

P4 programming language is a fairly new programming language introduced to enable us to program our new networking protocols on programmable switches. We are to implement a P4 object called TimerTask on NetFPGA board in this project.

P4-TrafficTool | Networking

08.2019 – 10.2019

P4-TrafficTool is an automated code generator for P4 traffic generators and analyzers. The main project was done by Deepanshu Jindal, Raj Joshi and Professor Ben Leon from national university of Singapore. My job was to work on the limitations of the tool and also provide some documentations for it.

EEG Signal Processing Projects| EEG Signal Processing

02.2019 – 06.2019

Course projects in order to get familiar with different aspects of EEG signal processing like denoising, source separation, brain source localization and etc.

Critical Object Detection in THz Image Sequences | Computer Vision

09.2018 – 07.2019

Unlike X-ray, THz radiation is not detrimental to human body. THz scanners allow remote detection of metallic, plastic, ceramic and other objects concealed under clothes at a distance of several meters, so it is a good choice for security systems. Sometimes it is hard to distinguish critical objects from body organs in a single THz image. So our goal is to detect objects in a sequence of THz images using machine learning.

A Chat Application| Data Communication Networks

01.2019 – 01.2019

In The project a chat application capable of transferring texts and files was developed. MAC Layer issues should be considered in this project. To simulate TCP behavior, protocols like stop and wait and windowing were implemented. Also some features were added for congestion control (TCP Tahoe).

Machine Learning Projects| Introduction to Machine Learning

10.2018 – 01.2019

Course projects in order to get familiar with machine learning algorithms like KNN, Decision trees, SVM and neural networks and also to learn how to analyze raw data and extract features from it.

A System Dynamics Model for Chabahar Port Solar Power Plant Development| System Dynamics

12.2018 – 01.2019

In a group of three we tried to develop a system dynamics model for the economic cycle of a solar power plant project which is in progress in Chabahar port.

JPEG COMPRESSOR | ASIC/FPGA

04.2018 – 05.2018

JPEG compression is a way of compressing pictures. The process consists of RGB to YCbCr conversion, taking the DCT transform, quantization, zigzag buffer and entropy coding. The Hardware is designed with Verilog language and verification for each part is done with several test benches. The simulations are done with Quartus and Modelsim design tools.

IMPLEMENTATION OF A NEURAL NETWORK ON FPGA| ASIC/FPGA

04.2016 – 05.2016

An artificial neural network is an interconnected group of nodes, similar to the vast network of neurons in a brain. Our task was to implement the hardware needed for a given network (the network structure is given as an input to the hardware) using Verilog.

STRATEGY GAME | Advanced Programming Lab

04.2016 – 05.2016

Using Java programing language in a groups of two, we developed a graphical strategy game, and implemented various objects like enemies, soldiers, guns and etc. the graphic part was designed with javafx.

AM TRANSMITTER | Principles of Electronics

01.2017 – 01.2017

AM transmitter is widely used in communication systems such as radio stations. We Designed a AM transmitter with a specific modulation frequency based on BJT transistors. The design was implemented on test boards and also we simulated it with Hspice. The PCB was also designed by Altium Designer.

BRAIN COMPUTER INTERFACE (BCI) | Signals & Systems

02.2017 – 05.2017

A Brain–computer interface (BCI), is a direct communication pathway between an enhanced or wired brain and an external device. Our purpose was to determine a specific letter that the person under experiment concentrates on, among 36 different characters, from his brain EEG (Electroencephalography) signals. We used MATLAB to implement the project.

TEACHING EXPERIENCE

Teaching Assistant | Sharif university of technology

02.2019 – 06.2019

Python programming laboratory teacher assistant.

Teaching Assistant | Sharif university of technology

09.2018 – 12.2018

Teaching Verilog to the students of Logic circuits course under supervision of Dr. Hoda Mohammadzadeh.

Teaching Assistant | Sharif university of technology

02.2018 – 05.2018

Working as the Analog Circuits Laboratory teaching assistant under supervision of Dr. Mahdi Shabany.

WORK EXPERIENCE

Engineering Intern | FANAP Payment

07.2018 – 09.2018

Android and C Developer

FANAP Payment is one of FANAP holding companies working on bank POS devices (programming and related issues using C programming language). I worked on an android application trying to find POS device as a UPNP device (UPNP is a set of networking protocols). I also worked with flat buffers, in order to let different devices (e.g. PC and POS) communicate with each other despite their source code programming language.

Engineering Intern | Raanas

01.2017 – 02.2017

Android Developer

Web Developer and A Member of the Organizing Committee | Makeathon

09.2016 – 01.2017

"Makeathon" or "Making Marathon" is an event held for the first time in Iran by Resana _ the Scientific & Cultural Society of the Electrical Engineering department of Sharif university of technology. I was the web developer and content manager in this event.

Private Educational Consultant

2015 – 2017

Giving educational advices to high school students.

High school Book Editor

08.2015 – 09.2015

mathematics for 9th grade students, basic mathematics for entrance university exam