CÔNG THỨC BJT DC

TABLE 4.1

BJT Bias Configurations

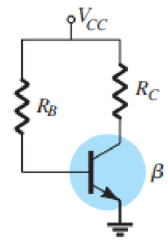
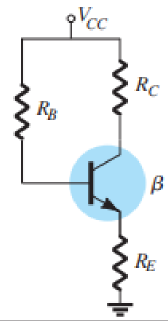
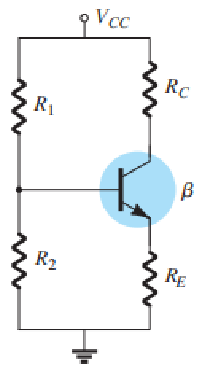
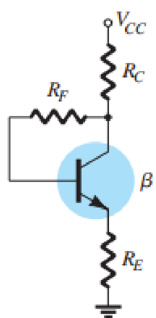
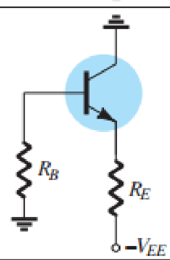
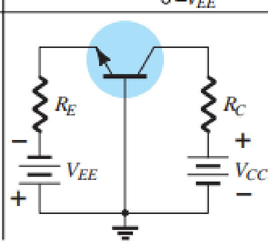
Type	Configuration	Pertinent Equations
Fixed-bias		$I_B = \dfrac{V_{CC} - V_{BE}}{R_B}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{CC} - I_C R_C$
Emitter-bias		$I_B = \dfrac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $R_i = (\beta + 1)R_E$ $V_{CE} = V_{CC} - I_C(R_C + R_E)$
Voltage-divider bias		EXACT: $R_{Th} = R_1 \Vert R_2, E_{Th} = \dfrac{R_2 V_{CC}}{R_1 + R_2}$ $I_B = \dfrac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{CC} - I_C(R_C + R_E)$ APPROXIMATE: $\beta R_E \geq 10R_2$ $V_B = \dfrac{R_2 V_{CC}}{R_1 + R_2}, V_E = V_B - V_{BE}$ $I_E = \dfrac{V_E}{R_E}, I_B = \dfrac{I_E}{\beta + 1}$ $V_{CE} = V_{CC} - I_C(R_C + R_E)$
Collector-feedback		$I_B = \dfrac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{CC} - I_C(R_C + R_E)$
Emitter-follower		$I_B = \dfrac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{EE} - I_E R_E$
Common-base		$I_E = \dfrac{V_{EE} - V_{BE}}{R_E}$ $I_B = \dfrac{I_E}{\beta + 1}, I_C = \beta I_B$ $V_{CE} = V_{EE} + V_{CC} - I_E(R_C + R_E)$ $V_{CB} = V_{CC} - I_C R_C$

TABLE 5.1

Unloaded BJT Transistor Amplifiers

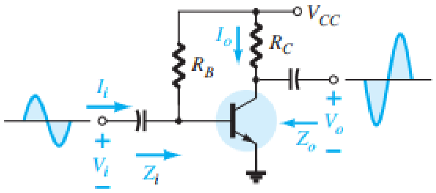
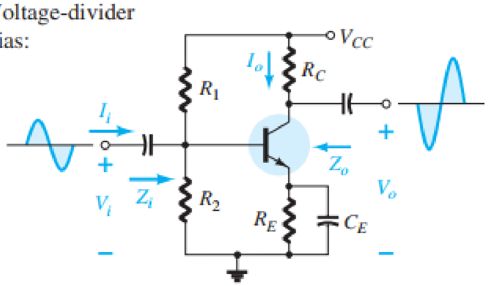
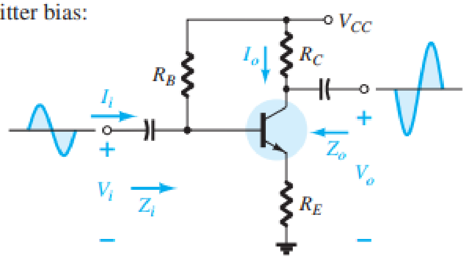
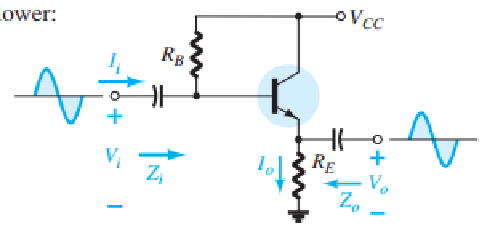
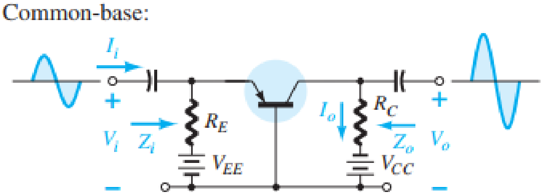
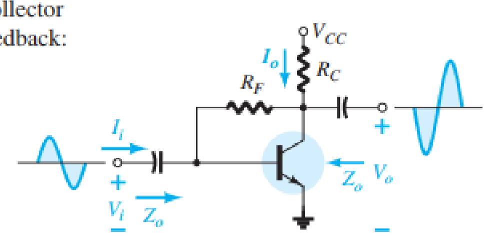
Configuration	Z_i	Z_o	A_v	A_i
Fixed-bias: 	Medium (1 kΩ) $= \boxed{R_B \| \beta r_e}$ $\cong \boxed{\beta r_e}$ $(R_B \geq 10\beta r_e)$	Medium (2 kΩ) $= \boxed{R_C \| r_o}$ $\cong \boxed{R_C}$ $(r_o \geq 10R_C)$	High (−200) $= \boxed{-\frac{(R_C \| r_o)}{r_e}}$ $\cong \boxed{-\frac{R_C}{r_e}}$ $(r_o \geq 10R_C)$	High (100) $= \boxed{\frac{\beta R_B r_o}{(r_o + R_C)(R_B + \beta r_e)}}$ $\cong \boxed{\beta}$ $(r_o \geq 10R_C,$ $R_B \geq 10\beta r_e)$
Voltage-divider bias: 	Medium (1 kΩ) $= \boxed{R_1 \| R_2 \| \beta r_e}$	Medium (2 kΩ) $= \boxed{R_C \| r_o}$ $\cong \boxed{R_C}$ $(r_o \geq 10R_C)$	High (−200) $= \boxed{-\frac{R_C \| r_o}{r_e}}$ $\cong \boxed{-\frac{R_C}{r_e}}$ $(r_o \geq 10R_C)$	High (50) $= \boxed{\frac{\beta(R_1 \| R_2) r_o}{(r_o + R_C)(R_1 \| R_2 + \beta r_e)}}$ $\cong \boxed{\frac{\beta(R_1 \| R_2)}{R_1 \| R_2 + \beta r_e}}$ $(r_o \geq 10R_C)$
Unbypassed emitter bias: 	High (100 kΩ) $= \boxed{R_B \| Z_b}$ $Z_b \cong \beta(r_e + R_E)$ $\cong \boxed{R_B \| \beta R_E}$ $(R_E \gg r_e)$	Medium (2 kΩ) $= \boxed{R_C}$ (any level of r_o)	Low (−5) $= \boxed{-\frac{R_C}{r_e + R_E}}$ $\cong \boxed{-\frac{R_C}{R_E}}$ $(R_E \gg r_e)$	High (50) $\cong \boxed{-\frac{\beta R_B}{R_B + Z_b}}$
Emitter-follower: 	High (100 kΩ) $= \boxed{R_B \| Z_b}$ $Z_b \cong \beta(r_e + R_E)$ $\cong \boxed{R_B \| \beta R_E}$ $(R_E \gg r_e)$	Low (20 Ω) $= \boxed{R_E \| r_e}$ $\cong \boxed{r_e}$ $(R_E \gg r_e)$	Low (≅1) $= \boxed{\frac{R_E}{R_E + r_e}}$ $\cong \boxed{1}$	High (−50) $\cong \boxed{-\frac{\beta R_B}{R_B + Z_b}}$
Common-base: 	Low (20 Ω) $= \boxed{R_E \| r_e}$ $\cong \boxed{r_e}$ $(R_E \gg r_e)$	Medium (2 kΩ) $= \boxed{R_C}$	High (200) $\cong \boxed{\frac{R_C}{r_e}}$	Low (−1) $\cong \boxed{-1}$
Collector feedback: 	Medium (1 kΩ) $= \boxed{\frac{r_e}{\frac{1}{\beta} + \frac{R_C}{R_F}}}$ $(r_o \geq 10R_C)$	Medium (2 kΩ) $\cong \boxed{R_C \| R_F}$ $(r_o \geq 10R_C)$	High (−200) $\cong \boxed{-\frac{R_C}{r_e}}$ $(r_o \geq 10R_C)$ $(R_F \gg R_C)$	High (50) $= \boxed{\frac{\beta R_F}{R_F + \beta R_C}}$ $\cong \boxed{\frac{R_F}{R_C}}$

TABLE 5.2

BJT Transistor Amplifiers Including the Effect of R_s and R_L

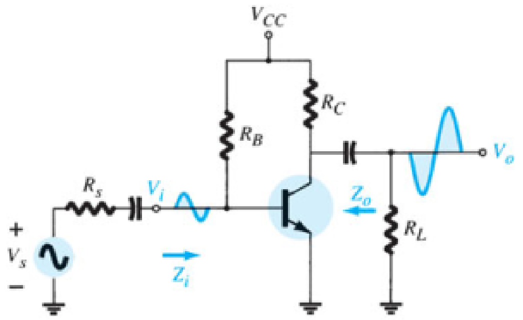
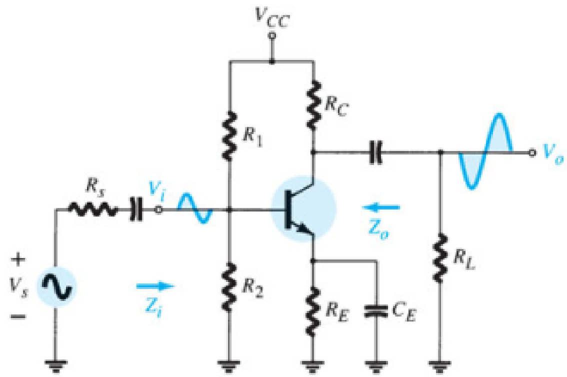
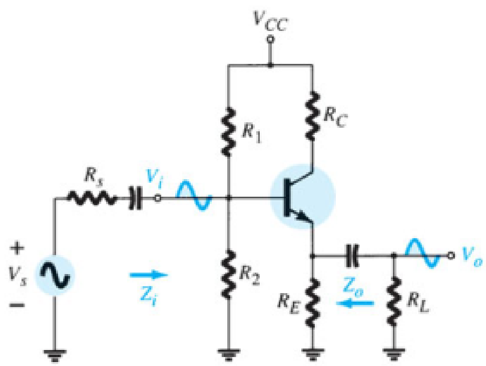
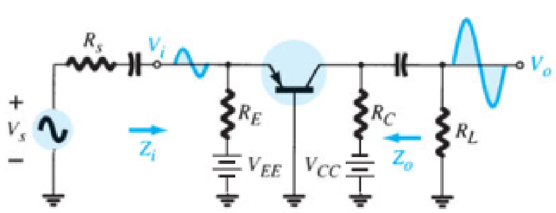
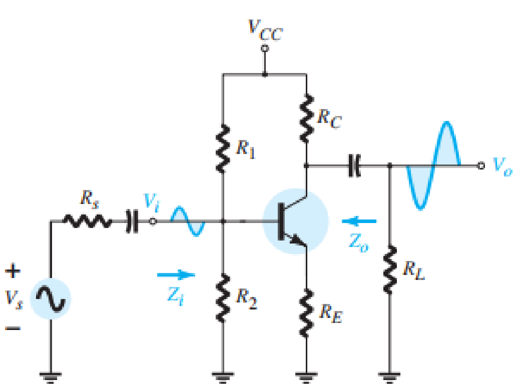
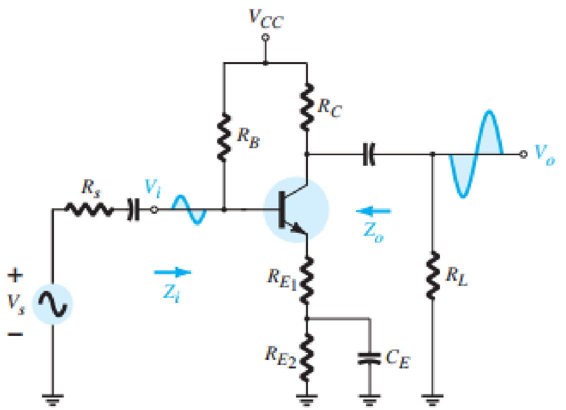
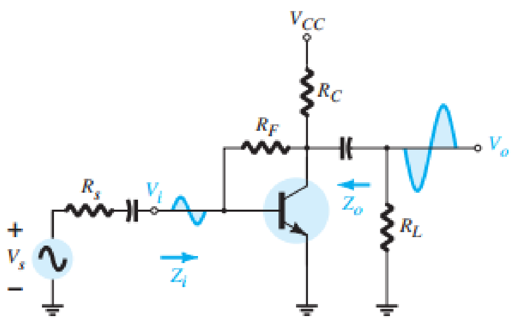
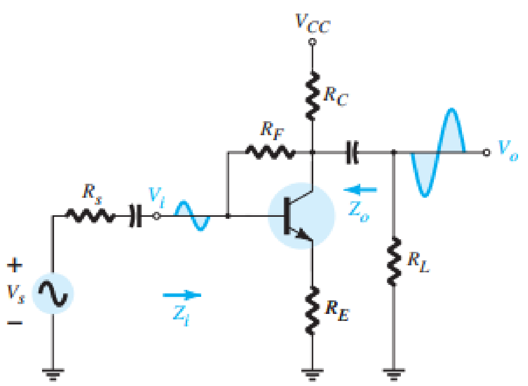
Configuration	$A_{v_L} = V_o/V_i$	Z_i	Z_o
	$\dfrac{-(R_L \Vert R_C)}{r_e}$	$R_B \Vert \beta r_e$	R_C
	Including r_o: $-\dfrac{(R_L \Vert R_C \Vert r_o)}{r_e}$	$R_B \Vert \beta r_e$	$R_C \Vert r_o$
	$\dfrac{-(R_L \Vert R_C)}{r_e}$	$R_1 \Vert R_2 \Vert \beta r_e$	R_C
	Including r_o: $\dfrac{-(R_L \Vert R_C \Vert r_o)}{r_e}$	$R_1 \Vert R_2 \Vert \beta r_e$	$R_C \Vert r_o$
	$\cong 1$	$R_E' = R_L \Vert R_E$ $R_1 \Vert R_2 \Vert \beta(r_e + R_E')$	$R_s' = R_s \Vert R_1 \Vert R_2$ $R_E \Vert \left(\dfrac{R_s'}{\beta} + r_e\right)$
	Including r_o: $\cong 1$	$R_1 \Vert R_2 \Vert \beta(r_e + R_E')$	$R_E \Vert \left(\dfrac{R_s'}{\beta} + r_e\right)$
	$\cong \dfrac{-(R_L \Vert R_C)}{r_e}$	$R_E \Vert r_e$	R_C
	Including r_o: $\cong \dfrac{-(R_L \Vert R_C \Vert r_o)}{r_e}$	$R_E \Vert r_e$	$R_C \Vert r_o$
	$\dfrac{-(R_L \Vert R_C)}{R_E}$	$R_1 \Vert R_2 \Vert \beta(r_e + R_E)$	R_C
	Including r_o: $\dfrac{-(R_L \Vert R_C)}{R_E}$	$R_1 \Vert R_2 \Vert \beta(r_e + R_e)$	$\cong R_C$

TABLE 5.2 *(Continued)*

BJT Transistor Amplifiers Including the Effect of R_s and R_L

Configuration	$A_{v_L} = V_o/V_i$	Z_i	Z_o
	$\dfrac{-(R_L \parallel R_C)}{R_{E_1}}$	$R_B \parallel \beta(r_e + R_{E_1})$	R_C
	Including r_o: $\dfrac{-(R_L \parallel R_C)}{R_{E_1}}$	$R_B \parallel \beta(r_e + R_E)$	$\cong R_C$
	$\dfrac{-(R_L \parallel R_C)}{r_e}$	$\beta r_e \parallel \dfrac{R_F}{\lvert A_v \rvert}$	R_C
	Including r_o: $\dfrac{-(R_L \parallel R_C \parallel r_o)}{r_e}$	$\beta r_e \parallel \dfrac{R_F}{\lvert A_v \rvert}$	$R_C \parallel R_F \parallel r_o$
	$\dfrac{-(R_L \parallel R_C)}{R_E}$	$\beta R_E \parallel \dfrac{R_F}{\lvert A_v \rvert}$	$\cong R_C \parallel R_F$
	Including r_o: $\cong \dfrac{-(R_L \parallel R_C)}{R_E}$	$\cong \beta R_E \parallel \dfrac{R_F}{\lvert A_v \rvert}$	$\cong R_C \parallel R_F$

$V_{BE} \cong 0.7\ \text{V}, \quad I_E = (\beta + 1)I_B \cong I_C, \quad I_C = \beta I_B$

Fixed bias:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}, \quad I_C = \beta I_B$$

Emitter stabilized:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}, \quad R_i = (\beta + 1)R_E$$

Voltage-divider bias:

Exact: $R_{Th} = R_1 \| R_2, \quad E_{Th} = V_{R_2} = \dfrac{R_2 V_{CC}}{R_1 + R_2}, \quad I_B = \dfrac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$

Approximate: Test $\beta R_E \geq 10R_2$

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}, \quad V_E = V_B - V_{BE}, \quad I_E = \frac{V_E}{R_E} \cong I_C$$

DC bias with voltage feedback:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}, \quad I_C' \cong I_C \cong I_E$$

Common base:

$$I_E = \frac{V_{EE} - V_{BE}}{R_E}, \quad I_C \cong I_E$$

Transistor switching networks:

$$I_{C_{sat}} = \frac{V_{CC}}{R_C}, \quad I_B > \frac{I_{C_{sat}}}{\beta_{dc}}, \quad R_{sat} = \frac{V_{CE_{sat}}}{I_{C_{sat}}},$$

$$t_{on} = t_r + t_d, \quad t_{off} = t_s + t_f$$

TABLE 6.3

Field Effect Transistors

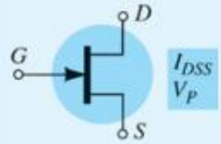
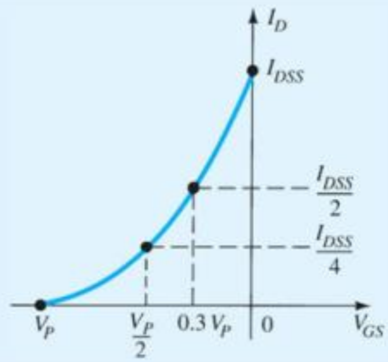
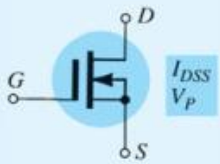
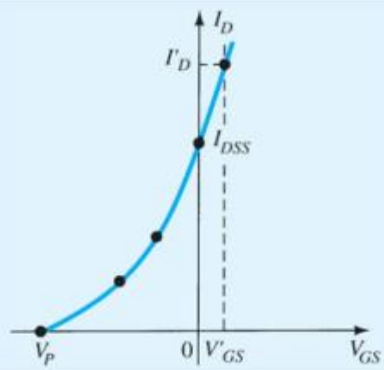
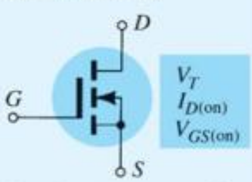
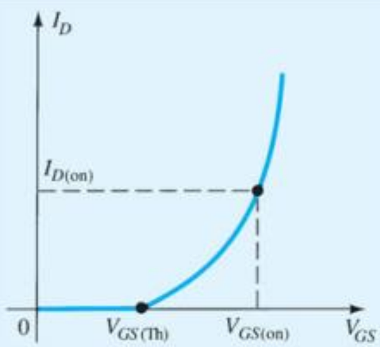
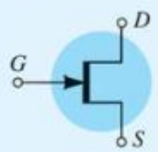
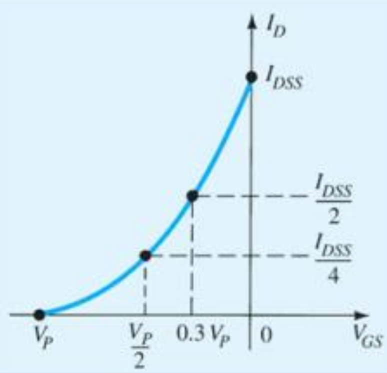
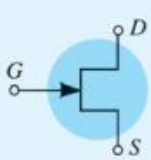
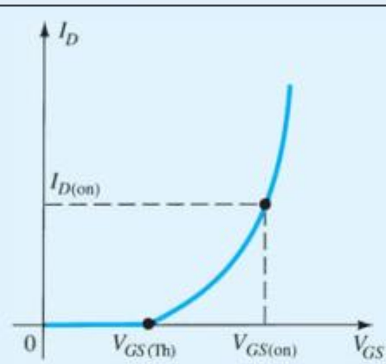
Type	Symbol and Basic Relationships	Transfer Curve	Input Resistance and Capacitance
JFET (*n*-channel)	$I_G = 0\text{ A}, I_D = I_S$  $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$		$R_i > 100\text{ M}\Omega$ C_i: $(1 - 10)$ pF
MOSFET depletion type (*n*-channel)	$I_G = 0\text{ A}, I_D = I_S$  $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$		$R_i > 10^{10}\ \Omega$ C_i: $(1 - 10)$ pF
MOSFET enhancement type (*n*-channel)	$I_G = 0\text{ A}, I_D = I_S$  $I_D = k\,(V_{GS} - V_{GS\,(\text{Th})})^2$ $k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS\,(\text{Th})})^2}$		$R_i > 10^{10}\ \Omega$ C_i: $(1 - 10)$ pF
MESFET depletion type (*n*-channel)	$I_G = 0\text{ A}, I_D = I_S$  $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ $I_G = 0\text{ A}, I_D = I_S$		$R_i > 10^{12}\ \Omega$ C_i: $(1 - 5)$ pF
MESFET enhancement type (*n*-channel)	 $I_D = k\,(V_{GS} - V_{GS\,(\text{Th})})^2$ $k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS\,(\text{Th})})^2}$		$R_i > 10^{12}\ \Omega$ C_i: $(1 - 5)$ pF

TABLE 7.1

FET Bias Configurations

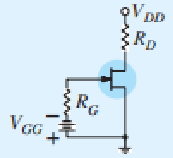
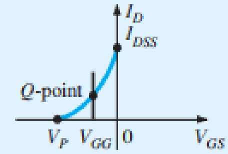
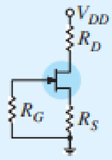
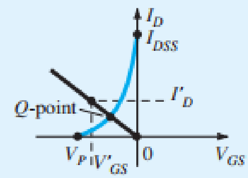
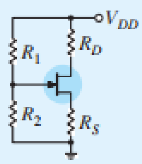
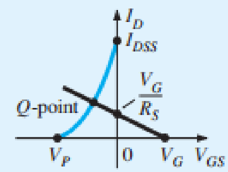
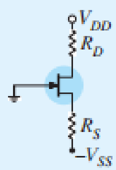
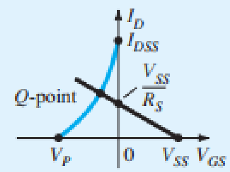
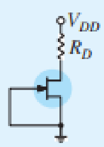
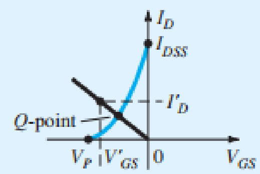
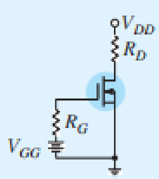
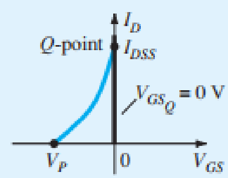
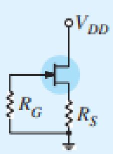
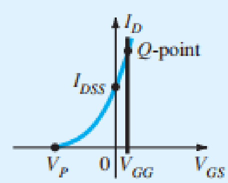
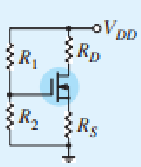
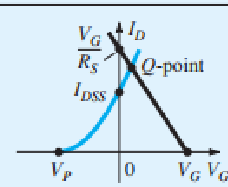
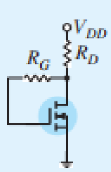
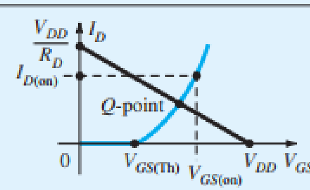
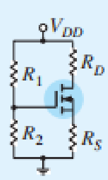
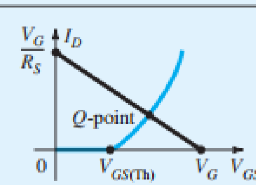
Type	Configuration	Pertinent Equations	Graphical Solution
JFET Fixed-bias		$V_{GS_Q} = -V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
JFET Self-bias		$V_{GS} = -I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Voltage-divider bias		$V_G = \dfrac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Common-gate		$V_{GS} = V_{SS} - I_D R_S$ $V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)$	
JFET ($R_D = 0\ \Omega$)		$V_{GS} = -I_D R_S$ $V_D = V_{DD}$ $V_S = I_D R_S$ $V_{DS} = V_{DD} - I_S R_S$	
JFET Special case ($V_{GS_Q} = 0$ V)		$V_{GS_Q} = 0$ V $I_{D_Q} = I_{DSS}$	
Depletion-type MOSFET Fixed-bias (and MESFETs)		$V_{GS_Q} = +V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
Depletion-type MOSFET Voltage-divider bias (and MESFETs)		$V_G = \dfrac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_S R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
Enhancement type MOSFET Feedback configuration (and MESFETs)		$V_{GS} = V_{DS}$ $V_{GS} = V_{DD} - I_D R_D$	
Enhancement type MOSFET Voltage-divider bias (and MESFETs)		$V_G = \dfrac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$	

TABLE 8.1

Z_i, Z_o, and A_v for various FET configurations

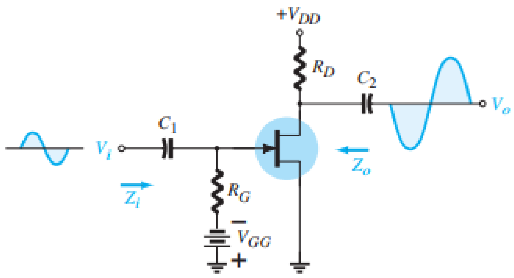
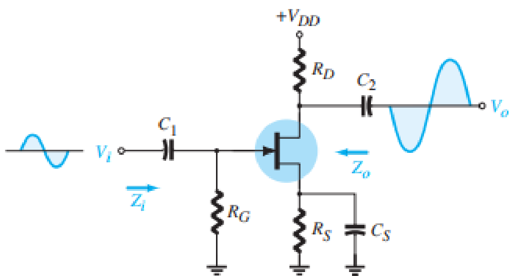
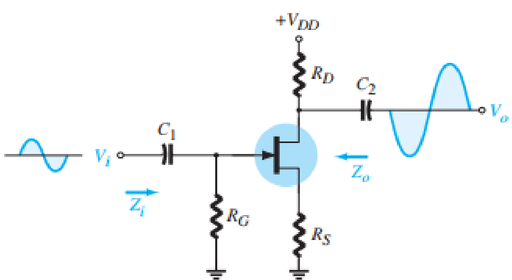
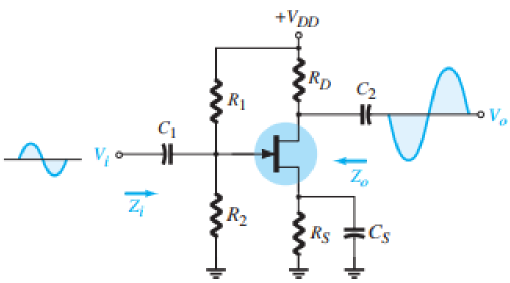
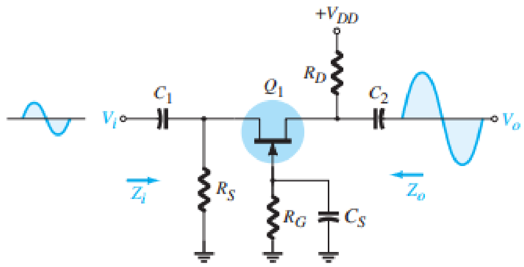
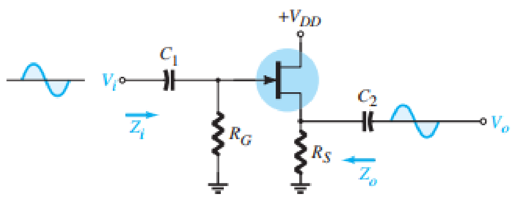
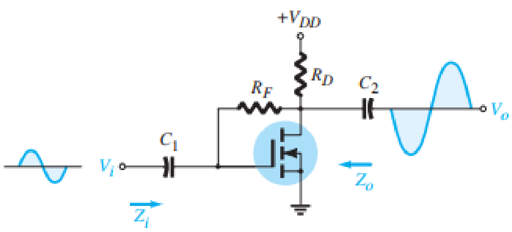
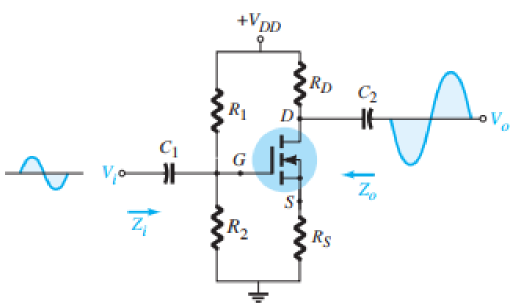
Configuration	Z_i	Z_o	$A_v = \dfrac{V_o}{V_i}$
Fixed-bias [JFET or D-MOSFET]  	High (10 MΩ) $= \boxed{R_G}$	Medium (2 kΩ) $= \boxed{R_D \Vert r_d}$ $\cong \boxed{R_D}$ $_{(r_d \geq 10 R_D)}$	Medium (−10) $= \boxed{-g_m(r_d \Vert R_D)}$ $\cong \boxed{-g_m R_D}$ $_{(r_d \geq 10 R_D)}$
Self-bias bypassed R_S [JFET or D-MOSFET]  	High (10 MΩ) $= \boxed{R_G}$	Medium (2 kΩ) $= \boxed{R_D \Vert r_d}$ $\cong \boxed{R_D}$ $_{(r_d \geq 10 R_D)}$	Medium (−10) $= \boxed{-g_m(r_d \Vert R_D)}$ $\cong \boxed{-g_m R_D}$ $_{(r_d \geq 10 R_D)}$
Self-bias unbypassed R_S [JFET or D-MOSFET]  	High (10 MΩ) $= \boxed{R_G}$	$= \boxed{\dfrac{\left[1 + g_m R_S + \dfrac{R_S}{r_d}\right] R_D}{\left[1 + g_m R_S + \dfrac{R_S}{r_d} + \dfrac{R_D}{r_d}\right]}}$ $= \boxed{R_D}$ $_{r_d \geq 10 R_D \text{ or } r_d = \infty\,\Omega}$	Low (−2) $= \boxed{\dfrac{g_m R_D}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}}}$ $\cong \boxed{-\dfrac{g_m R_D}{1 + g_m R_S}}$ $_{[r_d \geq 10 (R_D + R_S)]}$
Voltage-divider bias [JFET or D-MOSFET]  	High (10 MΩ) $= \boxed{R_1 \Vert R_2}$	Medium (2 kΩ) $= \boxed{R_D \Vert r_d}$ $\cong \boxed{R_D}$ $_{(r_d \geq 10 R_D)}$	Medium (−10) $= \boxed{-g_m(r_d \Vert R_D)}$ $\cong \boxed{-g_m R_D}$ $_{(r_d \geq 10 R_D)}$

TABLE 8.1

(Continued)

Configuration	Z_i	Z_o	$A_v = \frac{V_o}{V_i}$
Common-gate [JFET or D-MOSFET] 	Low (1 kΩ) $= R_S \Big\| \left[\frac{r_d + R_D}{1 + g_m r_d}\right]$ $\cong R_S \Big\| \frac{1}{g_m}$ $(r_d \geq 10\, R_D)$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(R_d \geq 10\, R_D)$	Medium (+10) $= \frac{g_m R_D + \frac{R_D}{r_d}}{1 + \frac{R_D}{r_d}}$ $\cong g_m R_D$ $(r_d \geq 10\, RD)$
Source-follower [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	Low (100 kΩ) $= r_d \| R_S \| 1/g_m$ $\cong R_S \| 1/g_m$ $(r_d \geq 10\, R_S)$	Low (<1) $= \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)}$ $\cong \frac{g_m R_S}{1 + g_m R_S}$ $(r_d \geq 10\, R_S)$
Drain-feedback bias E-MOSFET 	Medium (1 MΩ) $= \frac{R_F + r_d \| R_D}{1 + g_m(r_d \| R_D)}$ $\cong \frac{R_F}{1 + g_m R_D}$ $(r_d \geq 10\, R_D)$	Medium (2 kΩ) $= R_F \| r_d \| R_D$ $\cong R_D$ $(R_F, r_d \geq 10 R_D)$	Medium (−10) $= -g_m(R_F \| r_d \| R_D)$ $\cong -g_m R_D$ $(R_F, r_d \geq 10 R_D)$
Voltage-divider bias E-MOSFET 	Medium (1 MΩ) $= R_1 \| R_2$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(r_d \geq 10\, R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10\, R_D)$

Equations

$$g_m = y_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}$$

$$g_{m0} = \frac{2I_{DSS}}{|V_P|}$$

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]$$

$$g_m = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}$$

$$r_d = \frac{1}{y_{os}} = \frac{\Delta V_{DS}}{\Delta I_D}\bigg|_{V_{GS}=\text{constant}}$$

Effect of load impedance:

$$A_{v_L} = \frac{V_o}{V_i} = \frac{R_L}{R_L + R_o} A_{v_{NL}}, \qquad A_{i_L} = \frac{I_o}{I_i} = -A_{v_L}\frac{Z_i}{R_L}$$

Effect of source impedance:

$$V_i = \frac{R_i V_s}{R_i + R_s}, \qquad A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} A_{v_{NL}}$$

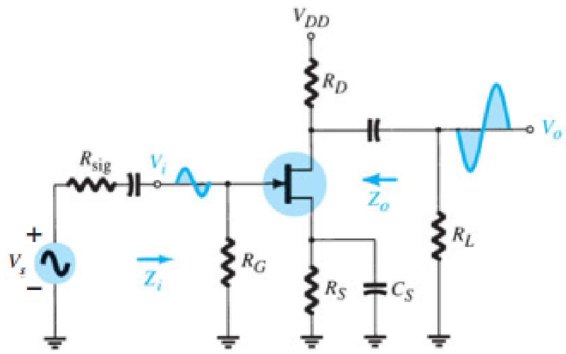
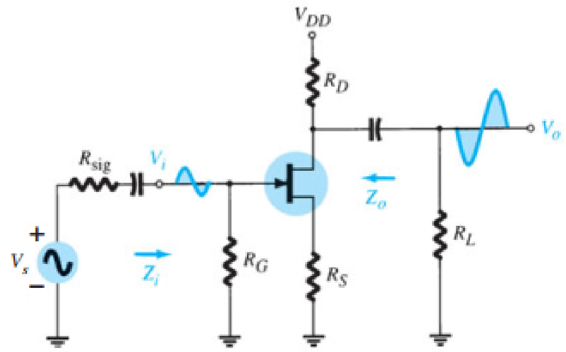
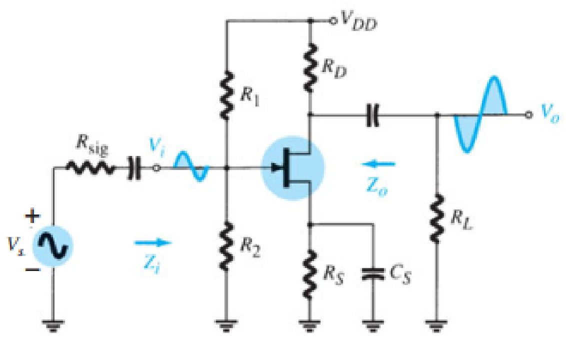
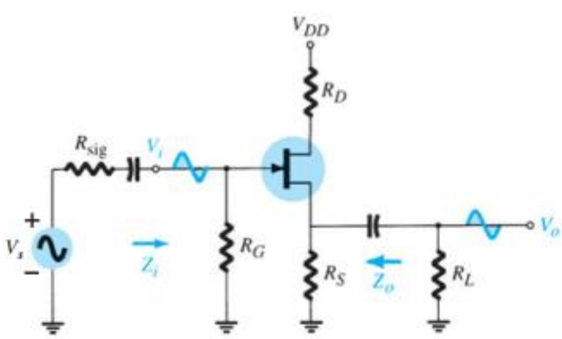
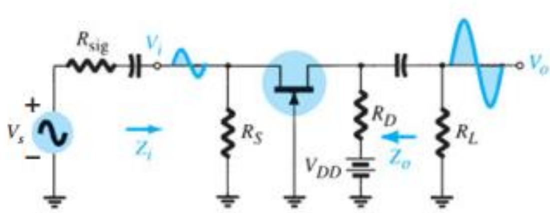
$$I_s = \frac{V_s}{R_s + R_i}$$

Combined effect of load and source impedance:

$$A_{v_L} = \frac{V_o}{V_i} = \frac{R_L}{R_L + R_o} A_{v_{NL}}, \qquad A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} \cdot \frac{R_L}{R_L + R_o} A_{v_{NL}}$$

$$A_{i_L} = \frac{I_o}{I_i} = -A_{v_L}\frac{R_i}{R_L}, \qquad A_{i_s} = \frac{I_o}{I_s} = -A_{v_s}\frac{R_s + R_i}{R_L}$$

TABLE 8.2

Configuration	$A_{v_L} = V_o / V_i$	Z_i	Z_o
	$-g_m(R_D \| R_L)$ Including r_d: $-g_m(R_D \| R_L \| r_d)$	R_G R_G	R_D $R_D \| r_d$
	$\dfrac{-g_m(R_D \| R_L)}{1 + g_m R_S}$ Including r_d: $\dfrac{-g_m(R_D \| R_L)}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}}$	R_G R_G	$\dfrac{R_D}{1 + g_m R_S}$ $\cong \dfrac{R_D}{1 + g_m R_S}$
	$-g_m(R_D \| R_L)$ Including r_d: $-g_m(R_D \| R_L \| r_d)$	$R_1 \| R_2$ $R_1 \| R_2$	R_D $R_D \| r_d$;
	$\dfrac{g_m(R_S \| R_L)}{1 + g_m(R_S \| R_L)}$ Including r_d: $= \dfrac{g_m r_d (R_S \| R_L)}{r_d + R_D + g_m r_d (R_S \| R_L)}$	R_G R_G	$R_S \| 1/g_m$ $\dfrac{R_S}{1 + \dfrac{g_m r_d R_S}{r_d + R_D}}$
	$g_m(R_D \| R_L)$ Including r_d: $\cong g_m(R_D \| R_L)$	$\dfrac{R_S}{1 + g_m R_S}$ $Z_i = \dfrac{R_S}{1 + \dfrac{g_m r_d R_S}{r_d + R_D \| R_L}}$	R_D $R_D \| r_d$