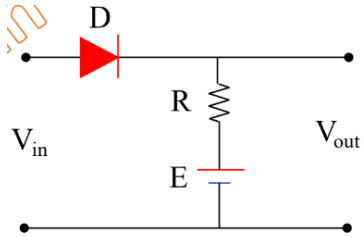
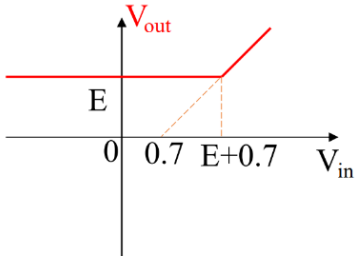
A. DIODE

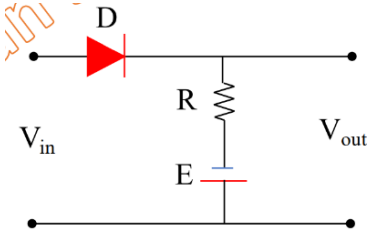
1. Mạch hạn chế nối tiếp

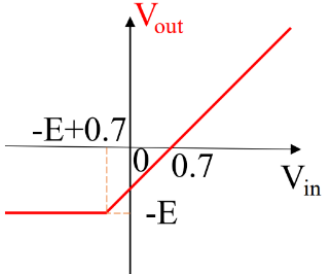
a. Hạn chế mức dưới dương



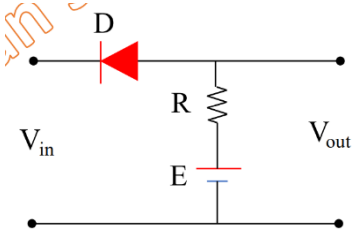


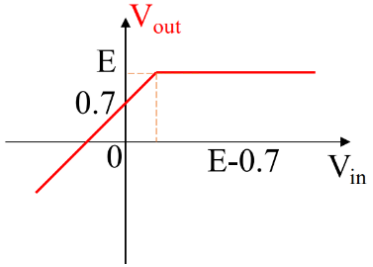
b. Hạn chế mức dưới âm



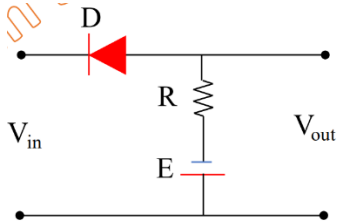


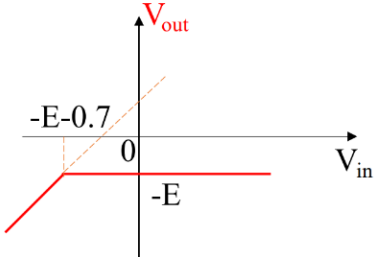
c. Hạn chế mức trên dương





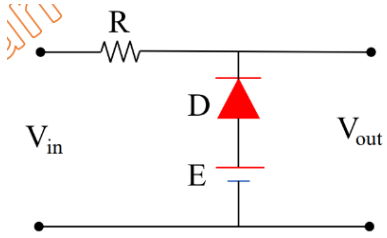
d. Hạn chế mức trên âm

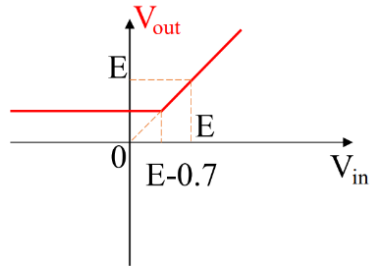




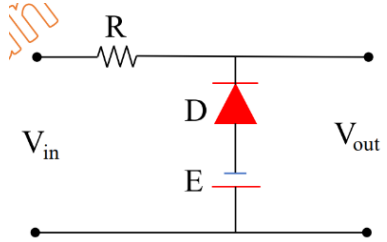
2. Mạch hạn chế song song

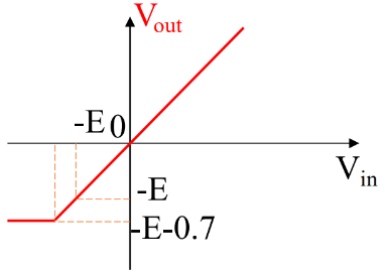
a. Hạn chế mức dưới dương



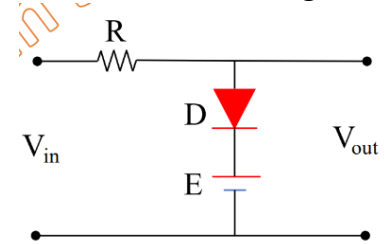


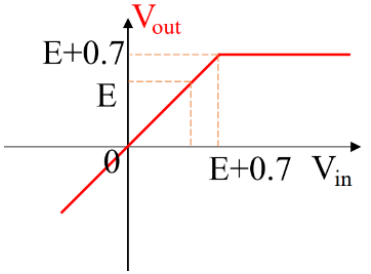
b. Hạn chế mức dưới âm



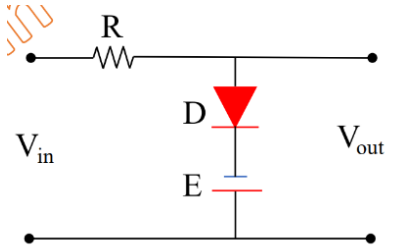


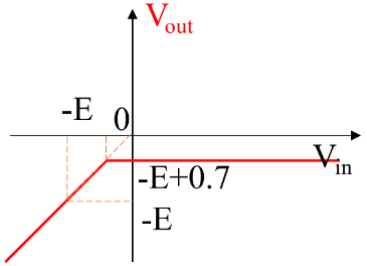
c. Hạn chế mức trên dương



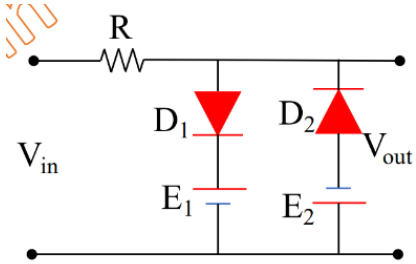


d. Hạn chế mức trên âm



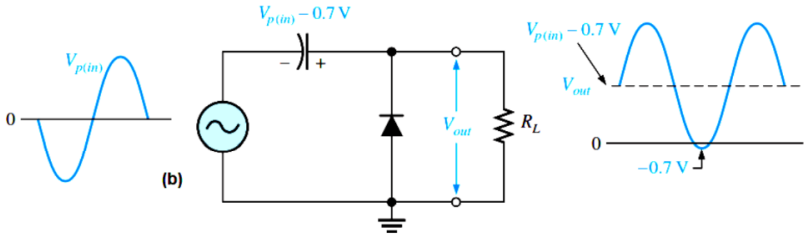


e. Hạn chế trên – dưới

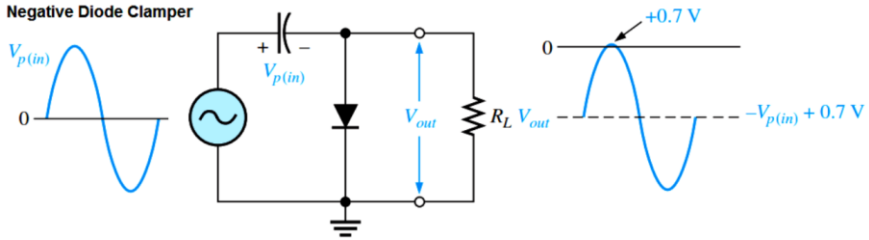


3. Mạch dịch mức

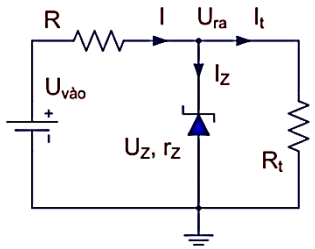
a. Mạch dịch mức dương



b. Mạch dịch mức âm



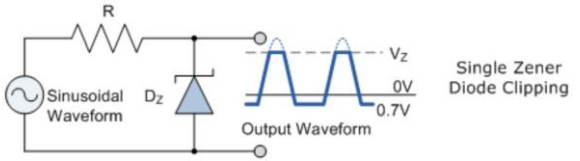
4. Diode Zener

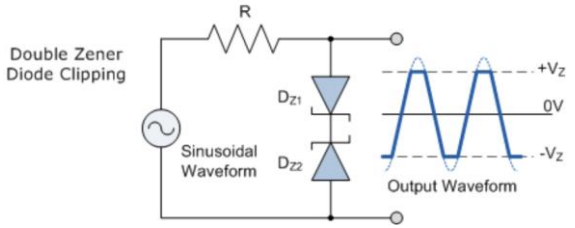


Công thức tổng quát cho mạch:

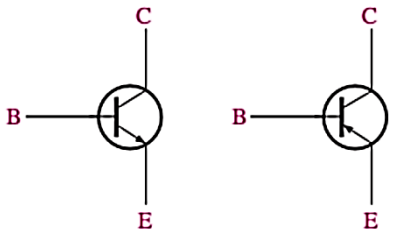
$$I_Z = \frac{U_{vào} - U_Z\left(1 + \frac{R}{R_t}\right)}{R + r_Z + \frac{R.r_Z}{R_t}}$$

Mạch hạn chế dùng diode Zener



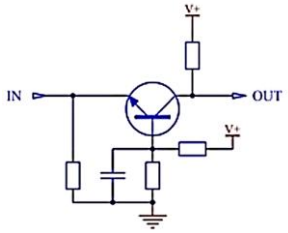
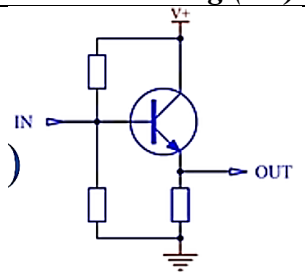
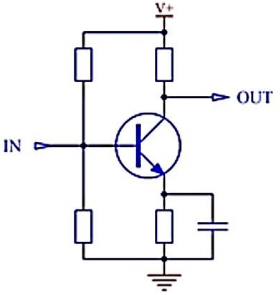


B. BJT



$$I_E = I_B + I_C$$
$$I_C = \beta\, I_B$$
$$I_E = (\beta + 1)\, I_B$$
$$I_C = \alpha\, I_E$$
$$\alpha = \frac{\beta}{\beta + 1} \qquad \beta = \frac{\alpha}{1 - \alpha}$$

1. Mắc BJT

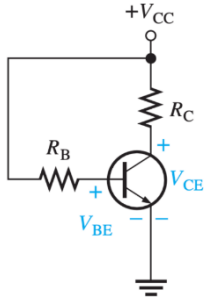
Base chung (BC)	*Collector chung (CC)*	*Emittor chung (EC)*
		
- Tín hiệu ra cùng pha tín hiệu vào - Ku khá lớn, Ki < 1	- Tín hiệu ra cùng pha tín hiệu vào - Ku xấp xỉ 1, Ki > 1	- Tín hiệu ra ngược pha tín hiệu vào - Ku lớn, Ki lớn

2. Phân cực BJT

Đường tải một chiều: $E_C = I_C R_C + U_{CE}$

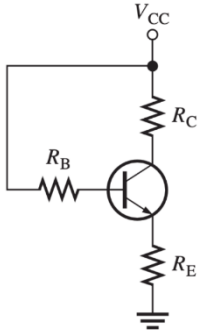
a. Phân cực base

$$V_{CC} = V_{R_B} + V_{BE} = I_B R_B + V_{BE}$$
$$I_B = \frac{V_{CC} - V_{BE}}{R_B}, I_C = \beta I_B = \beta \frac{V_{CC} - V_{BE}}{R_B}$$
$$U_{CE} = V_{CC} - I_C R_C$$



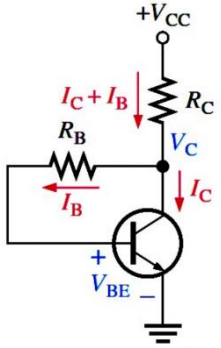
b. Phân cực hồi tiếp Emitter

$$V_{CC} = V_{R_B} + V_{BE} + V_{R_E} = I_B R_B + V_{BE} + I_E R_E$$
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}, I_C = \beta I_B = \beta \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$
$$U_{CE} = V_{CC} - I_C R_C - I_E R_E \approx V_{CC} - I_C(R_C + R_E)$$

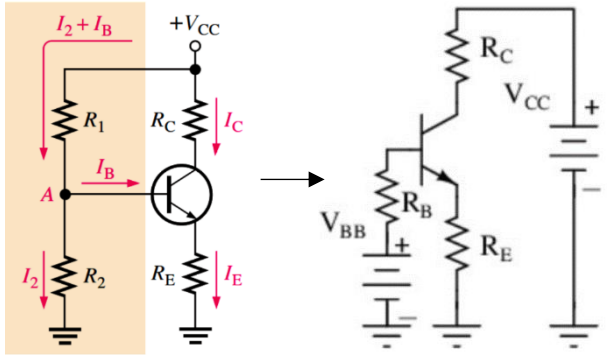


c. Phân cực hồi tiếp Collector

$$V_{CC} = V_{R_B} + V_{R_C} + V_{BE} = I_B R_B + I_C R_C + V_{BE}$$
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_C}, I_C = \beta I_B = \beta \frac{V_{CC} - V_{BE}}{R_B + \beta R_C}$$
$$U_{CE} = V_{CC} - I_C R_C \approx V_{CC} - \beta \frac{V_{CC} - V_{BE}}{R_B + \beta R_C} R_C$$



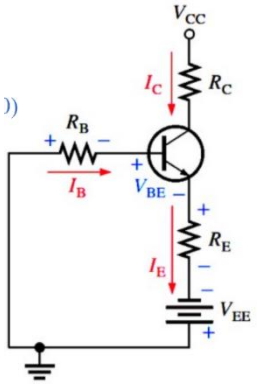
d. Phân cực bằng phân áp



$$V_{BB} = V_{CC} \frac{R_2}{R_1 + R_2}, R_B = \frac{R_1 R_2}{R_1 + R_2}$$
$$V_{BB} = V_{R_B} + V_{R_E} + V_{BE} = I_B R_B + I_E R_E + V_{BE}$$
$$I_B = \frac{V_{BB} - V_{BE}}{R_B + (\beta + 1)R_E}, I_C = \beta I_B = \beta \frac{V_{BB} - V_{BE}}{R_B + (\beta + 1)R_E}$$
$$U_{CE} = V_{CC} - I_C R_C - I_E R_E \approx V_{CC} - I_C(R_C + R_E)$$

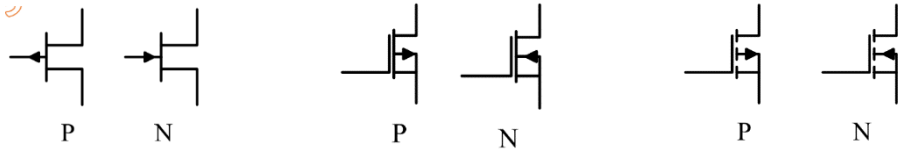
e. Phân cực Emitter

$$V_{EE} = V_{R_B} + V_{R_E} + V_{BE} = I_B R_B + I_E R_E + V_{BE}$$
$$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E}, I_C = \beta I_B = \beta \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E}$$
$$U_{CE} = V_{CC} + V_{EE} - I_C R_C - I_E R_E \approx V_{CC} + V_{EE} - I_C(R_C + R_E)$$



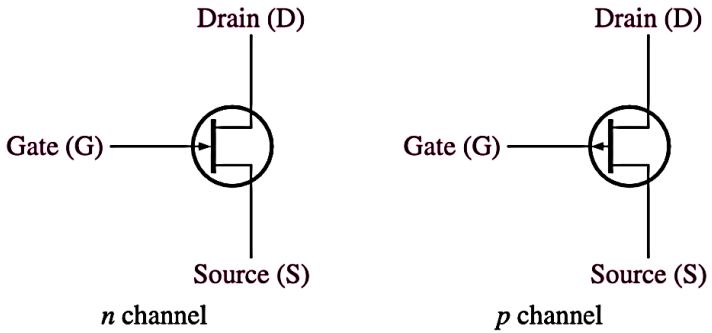
Bazơ	Hồi tiếp Emitơ	Hồi tiếp Colectơ	Phân áp	Emitơ
Kém ổn định, chỉ dùng cho mạch đóng cắt	Ổn định tốt	Ổn định tốt	Ổn định rất tốt, độ đồng đều cao, thông dụng nhất	Ổn định tốt, cần thêm nguồn âm

C. FET



JFET | MOSFET kênh sẵn | MOSFET kênh cảm ứng

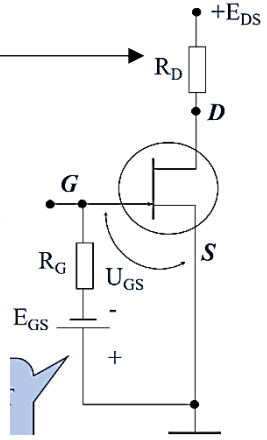
1. JFET



Phân cực cho JFET

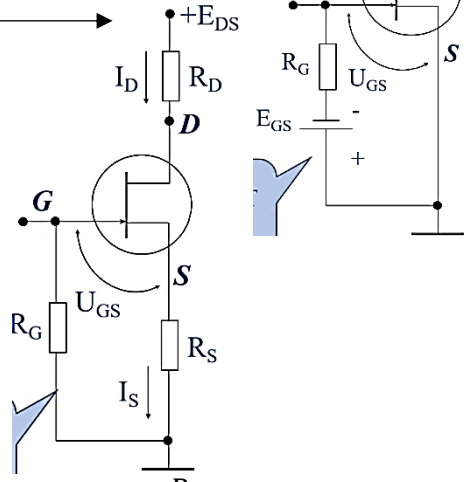
a. Phân cực bằng điện áp cố định

$$U_{GSQ} = -E_{GS}, U_{DSQ} = E_{DS} - I_D R_D$$

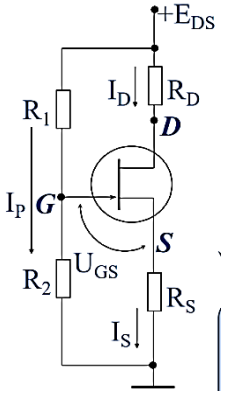


b. Tự phân cực

$$U_{GS} = -I_D R_S,$$
$$U_{DSQ} = E_{DS} - I_{DQ}(R_D + R_S)$$



c. Phân cực bằng phân áp

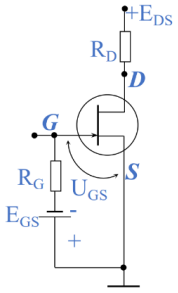
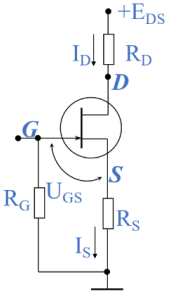
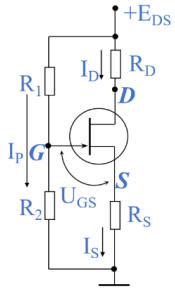


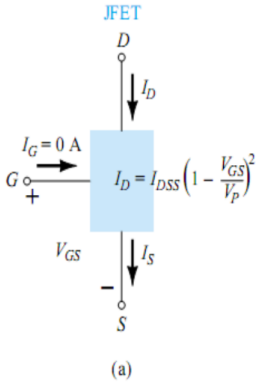
$$U_{GS} = E_{DS}\frac{R_2}{R_1 + R_2} - I_D R_S$$

$$U_{DSQ} = E_{DS} - I_{DQ}(R_D + R_S)$$

=> Phương trình: $aU_{GS}^2 + bU_{GS} + c = 0$

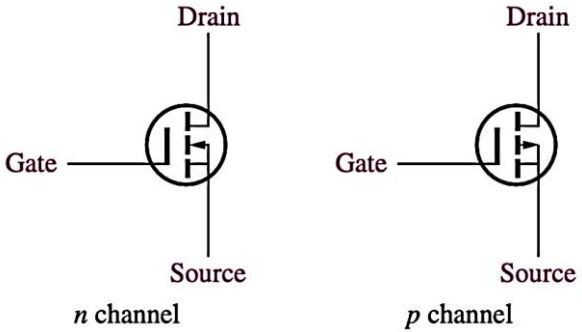
$$\begin{cases} a = \dfrac{R_S I_{DSS}}{U_P^2} \\ b = \left(1 - \dfrac{2R_S I_{DSS}}{U_P}\right) \\ c = R_S I_{DSS} \end{cases}$$

Điện áp cố định	Tự phân cực	Phân áp
Kém ổn định	Ổn định khá	Ổn định tốt
		



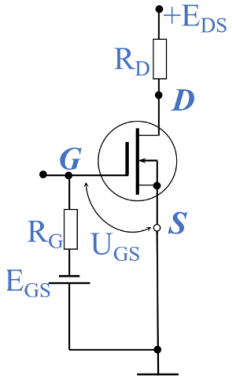
JFET		*BJT*
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	⇔	$I_C = \beta I_B$
$I_D = I_S$	⇔	$I_C \cong I_E$
$I_G \cong 0$ A	⇔	$V_{BE} \cong 0.7$ V

2. MOSFET

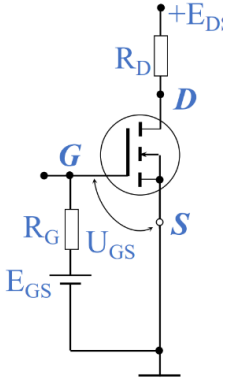


Phân cực cho MOSFET

a. Phân cực bằng điện áp cố định

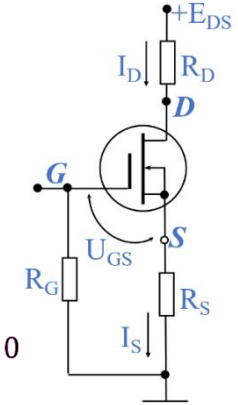


D-MOSFET kênh N



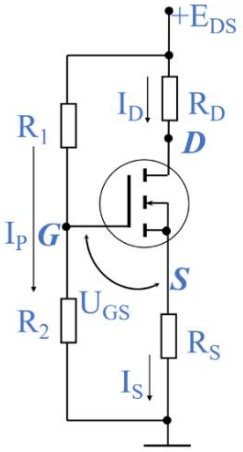
E-MOSFET kênh N

*b. Tự phân cực (**Không áp dụng cho E-MOSFET**)*



c. Phân cực bằng phân áp (D-MOSFET như JFET)

Với E-MOSFET:



$$U_{DSQ} = E_{DS} - I_{DQ}(R_D + R_S)$$

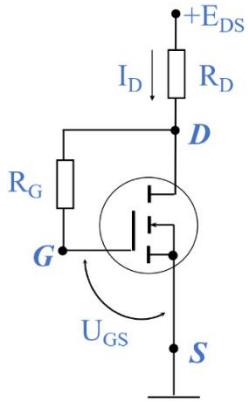
Phương trình: $aU_{GS}^2 + bU_{GS} + c = 0$

$$\begin{cases} a = kR_S \\ b = (1 - 2kR_S U_T) \\ c = \left(kR_S U_T^2 - U_G\right) \end{cases}$$

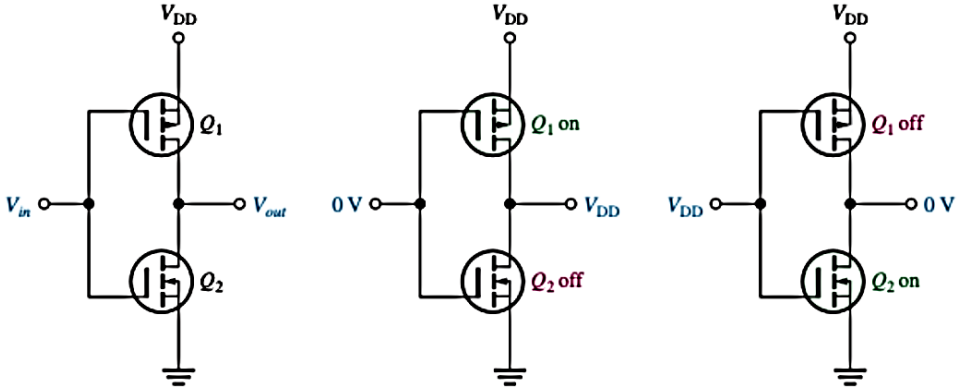
d. Phân cực bằng hồi tiếp điện áp

Phương trình: $aU_{GS}^2 + bU_{GS} + c = 0$

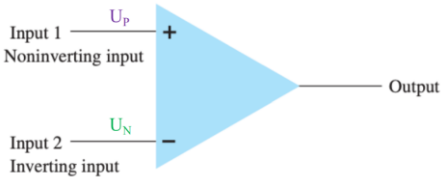
$$\begin{cases} a = k \\ b = \left(\dfrac{1}{R_D} - 2k.U_T\right) \\ c = \left(kU_T^2 - \dfrac{E_{DS}}{R_D}\right) \end{cases}$$

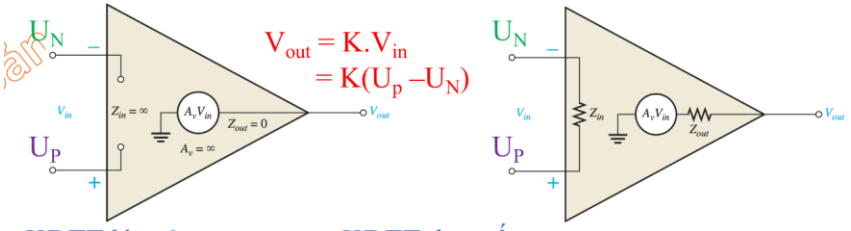


C-MOSFET



D. OP – AMP

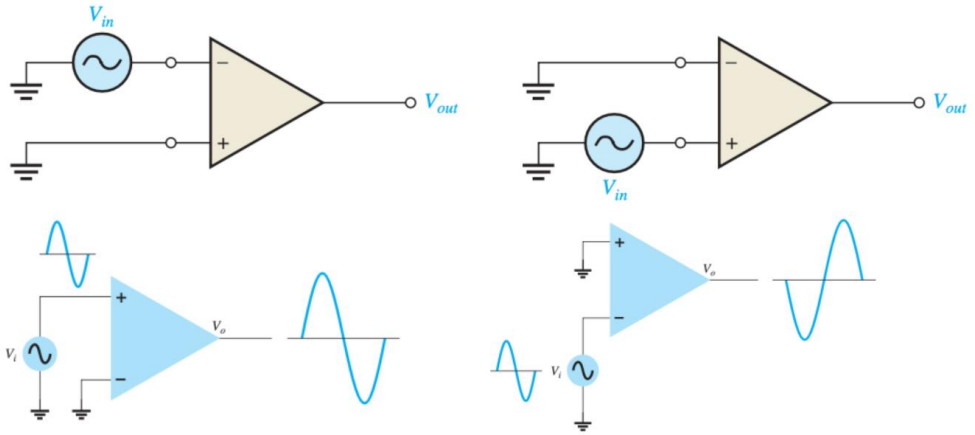




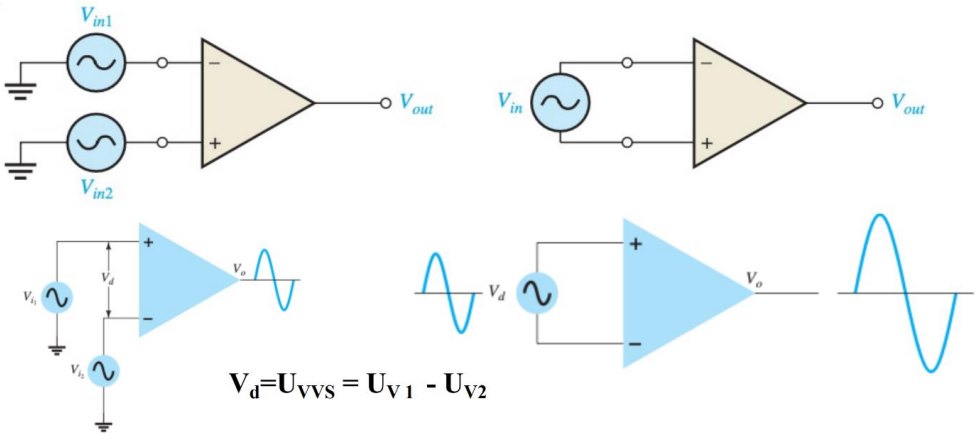
• KĐTT lý tưởng: • KĐTT thực tế:

1. Mắc tín hiệu vào

a. Single – ended



b. Double – ended



$\mathbf{V_d = U_{VVS} = U_{V1} - U_{V2}}$

Tỉ số nén mode chung: $CMRR = \frac{K_{VS}}{K_C} = 20 \log \frac{K_{VS}}{K_C} (dB)$

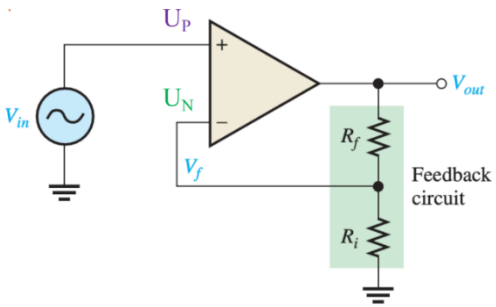
2. KDTT có vòng hồi tiếp

a. Mạch khuếch đại thuận

$$V_{out} = V_{in} \frac{R_i + R_f}{R_i}$$

$$A_{cl} = K_u = \frac{V_{out}}{V_{in}} = \frac{R_i + R_f}{R_i}$$

Tín hiệu ra cùng pha tín hiệu vào

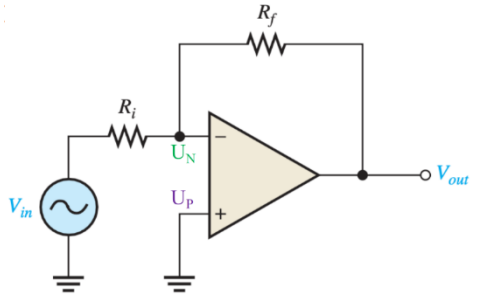


b. Mạch khuếch đại đảo

$$V_{out} = -V_{in} \frac{R_f}{R_i}$$

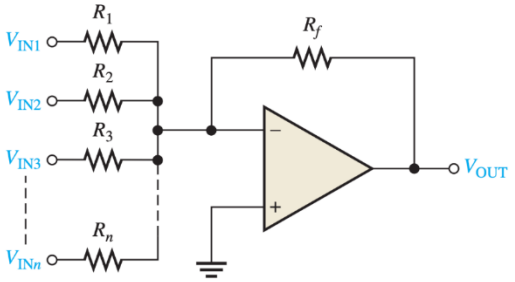
$$A_{cl} = K_u = \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_i}$$

Tín hiệu ra ngược pha tín hiệu vào



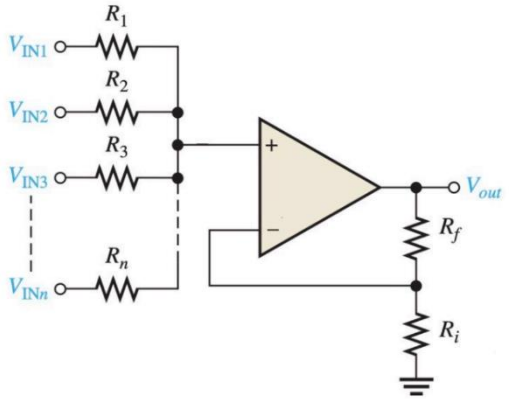
c. Mạch khuếch đại cộng đảo

$$V_{out} = -R_f \sum_{i=1}^{n} \frac{V_{IN(i)}}{R_i}$$



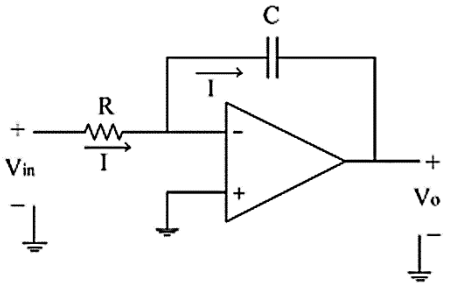
d. Mạch khuếch đại cộng không đảo

$$V_{out} = \frac{R_i + R_f}{R_i} \sum_{i=1}^{n} \frac{V_{IN(i)}}{n}$$



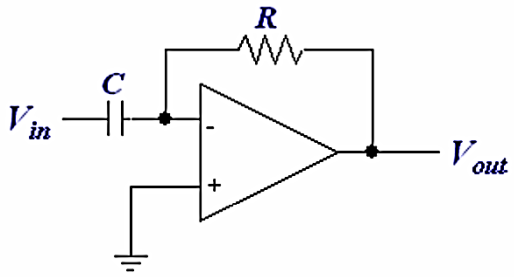
e. Mạch tích phân

$$V_{out} = -\frac{1}{RC} \int_0^t V_{in} dt$$



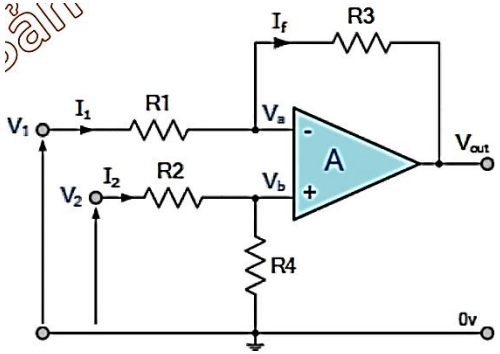
f. Mạch vi phân

$$V_{out} = -RC\frac{dV_{in}}{dt}$$

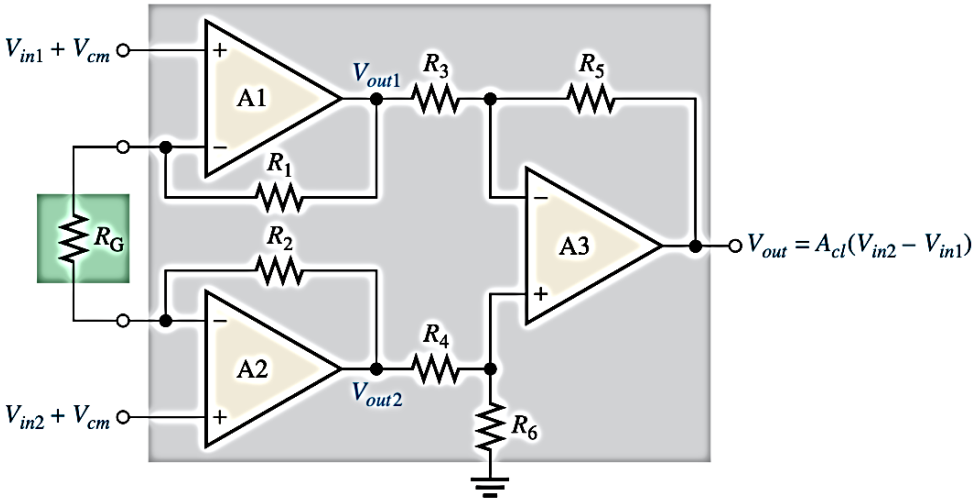


3. Mạch khuếch đại vi sai

$$V_{out} = \frac{V_2 R_4}{R_4 + R_2}\left(1 + \frac{R_3}{R_1}\right) - \frac{V_1 R_3}{R_1}$$



4. Mạch khuếch đại đo

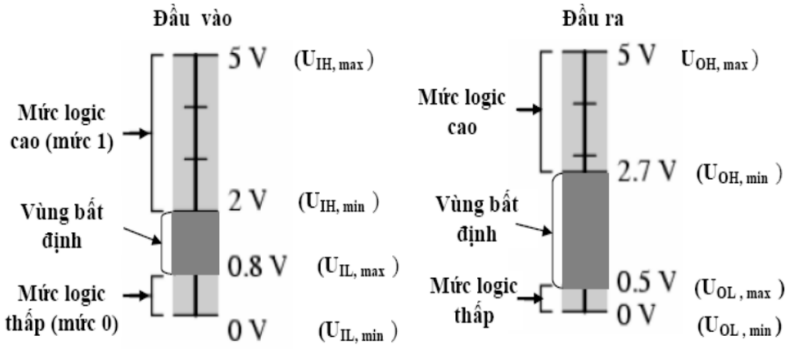


$$K_u = \left(1 + \frac{2R_1}{R_G}\right)\frac{R_5}{R_3}$$

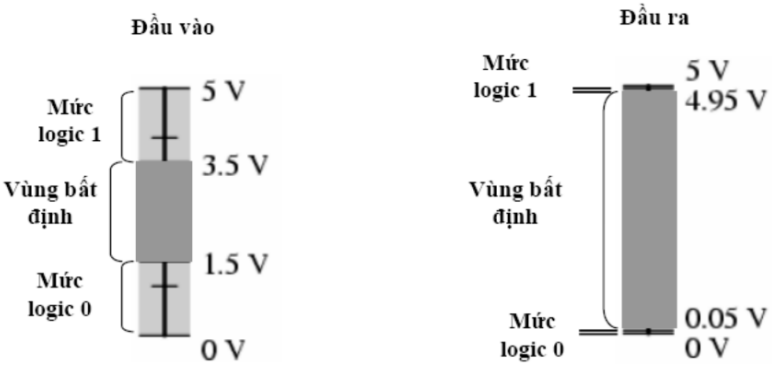
5. VI MẠCH SỐ

1. Mức logic vào/ra của IC số

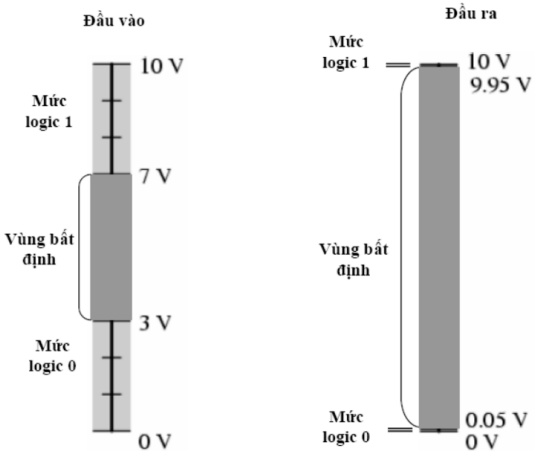
a. Họ TTL



b. Họ CMOS (5V)



c. Họ CMOS (10V)



Khả năng chống nhiễu:

- Nhiễu mức cao: $U_{noise} \geq U_{IHmin} - U_{OHmin}$
- Nhiễu mức thấp: $U_{noise} \leq U_{ILmax} - U_{OLmax}$

Mức logic điện áp của các vi mạch số điển hình

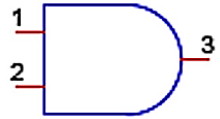
Tham số	4000/14000	74C/HC	74HCT	74AC	74ACT	74AHC	74AHC
$U_{IH(min)}$	3.5V	3.5V	2V	3.5V	2V	3.85V	2V
$U_{IL(max)}$	1.5V	1.0V	0.8V	1.5V	0.8V	1.65V	0.8V
$U_{OH(min)}$	4.95V	4.9V	4.9V	4.9V	4.9V	4.4V	3.15V
$U_{OL(max)}$	0.05V	0.1V	0.1V	0.1V	0.1V	0.44V	0.1V
U_{NH}	1.45V	1.4V	2.9V	1.4V	2.9V	0.55V	1.15V
U_{NL}	1.45V	0.9V	0.7V	1.4V	0.7V	1.21V	0.7V

Mức logic dòng của một số vi mạch số điển hình

Parameter	CMOS				TTL				
	4000B	74HC/HCT	74AC/ACT	74AHC/AHCT	74	74LS	74AS	74ALS	74F
$I_{IH(max)}$	1µA	1µA	1µA	1µA	40µA	20µA	20µA	20µA	20µA
$I_{IL(max)}$	1µA	1µA	1µA	1µA	1.6mA	0.4mA	0.5mA	100µA	0.6mA
$I_{OH(max)}$	0.4mA	4mA	24mA	8mA	0.4mA	0.4mA	2mA	400mA	1mA
$I_{OL(max)}$	0.4mA	4mA	24mA	8mA	16mA	8mA	20mA	8mA	20mA

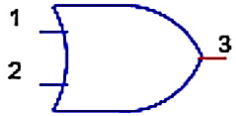
2. Các cổng logic cơ bản

a. Cổng AND



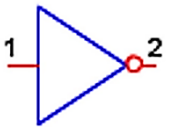
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

b. Cổng OR



A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

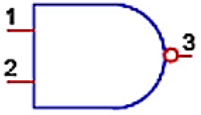
c. Cổng NOT



A	F
1	0
0	1

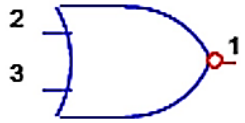
3. Các cổng logic thông dụng

a. Cổng NAND = NOT + AND



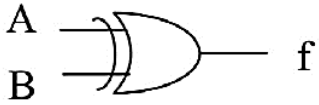
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

b. Cổng NOR = NOT + OR



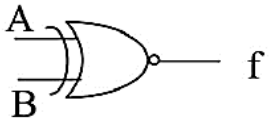
A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

c. Cổng XOR



A	B	f
0	0	0
0	1	1
1	0	1
1	1	0

d. Cổng XNOR



A	B	f
0	0	1
0	1	0
1	0	0
1	1	1