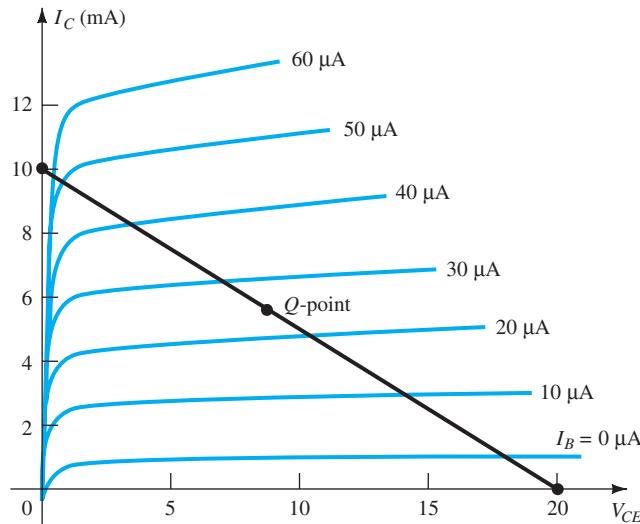


**EXAMPLE 4.3** Given the load line of Fig. 4.16 and the defined *Q*-point, determine the required values of  $V_{CC}$ ,  $R_C$ , and  $R_B$  for a fixed-bias configuration.



**FIG. 4.16**  
Example 4.3.

**Solution:** From Fig. 4.16,

$$V_{CE} = V_{CC} = 20 \text{ V} \text{ at } I_C = 0 \text{ mA}$$

$$I_C = \frac{V_{CC}}{R_C} \text{ at } V_{CE} = 0 \text{ V}$$

and

$$R_C = \frac{V_{CC}}{I_C} = \frac{20 \text{ V}}{10 \text{ mA}} = 2 \text{ k}\Omega$$

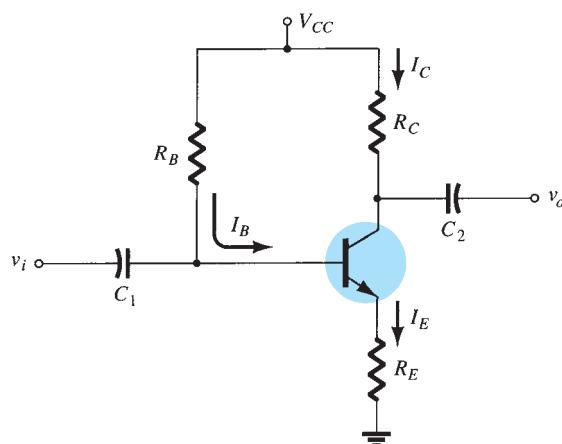
$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

and

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20 \text{ V} - 0.7 \text{ V}}{25 \mu\text{A}} = 772 \text{ k}\Omega$$

#### 4.4 Emitter-Bias Configuration

The dc bias network of Fig. 4.17 contains an emitter resistor to improve the stability level over that of the fixed-bias configuration. The more stable a configuration, the less its response will change due to undesirable changes in temperature and parameter



**FIG. 4.17**  
BJT bias circuit with emitter resistor.

Now the BJT collector current increases by about 81% due to the 100% increase in  $\beta$ . Notice that  $I_B$  decreased, helping maintain the value of  $I_C$ —or at least reducing the overall change in  $I_C$  due to the change in  $\beta$ . The change in  $V_{CE}$  has dropped to about 35%. The network of Fig. 4.23 is therefore more stable than that of Fig. 4.7 for the same change in  $\beta$ .

## Saturation Level

The collector saturation level or maximum collector current for an emitter-bias design can be determined using the same approach applied to the fixed-bias configuration: Apply a short circuit between the collector–emitter terminals as shown in Fig. 4.24 and calculate the resulting collector current. For Fig. 4.24

$$I_{C_{\text{sat}}} = \frac{V_{CC}}{R_C + R_E} \quad (4.25)$$

The addition of the emitter resistor reduces the collector saturation level below that obtained with a fixed-bias configuration using the same collector resistor.

**EXAMPLE 4.6** Determine the saturation current for the network of Example 4.4.

**Solution:**

$$\begin{aligned} I_{C_{\text{sat}}} &= \frac{V_{CC}}{R_C + R_E} \\ &= \frac{20 \text{ V}}{2 \text{ k}\Omega + 1 \text{ k}\Omega} = \frac{20 \text{ V}}{3 \text{ k}\Omega} \\ &= 6.67 \text{ mA} \end{aligned}$$

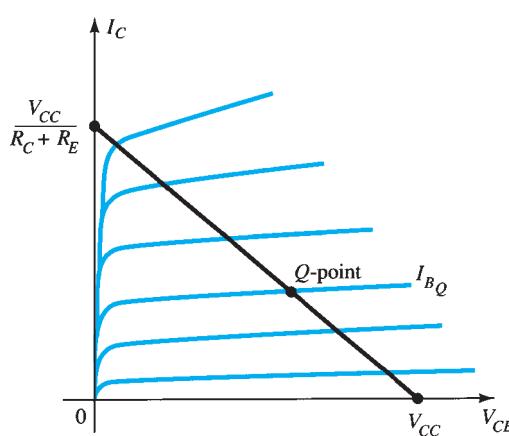
which is about three times the level of  $I_{C_Q}$  for Example 4.4.

## Load-Line Analysis

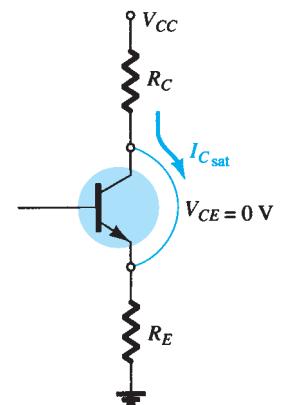
The load-line analysis of the emitter-bias network is only slightly different from that encountered for the fixed-bias configuration. The level of  $I_B$  as determined by Eq. (4.17) defines the level of  $I_B$  on the characteristics of Fig. 4.25 (denoted  $I_{B_Q}$ ).

The collector–emitter loop equation that defines the load line is

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$



**FIG. 4.25**  
Load line for the emitter-bias configuration.



**FIG. 4.24**  
Determining  $I_{C_{\text{sat}}}$  for the emitter-stabilized bias circuit.

Choosing  $I_C = 0 \text{ mA}$  gives

$$V_{CE} = V_{CC} \Big|_{I_C=0 \text{ mA}} \quad (4.26)$$

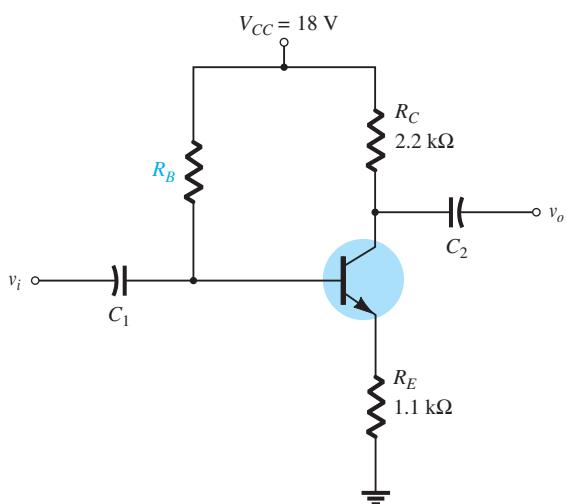
as obtained for the fixed-bias configuration. Choosing  $V_{CE} = 0 \text{ V}$  gives

$$I_C = \frac{V_{CC}}{R_C + R_E} \Big|_{V_{CE}=0 \text{ V}} \quad (4.27)$$

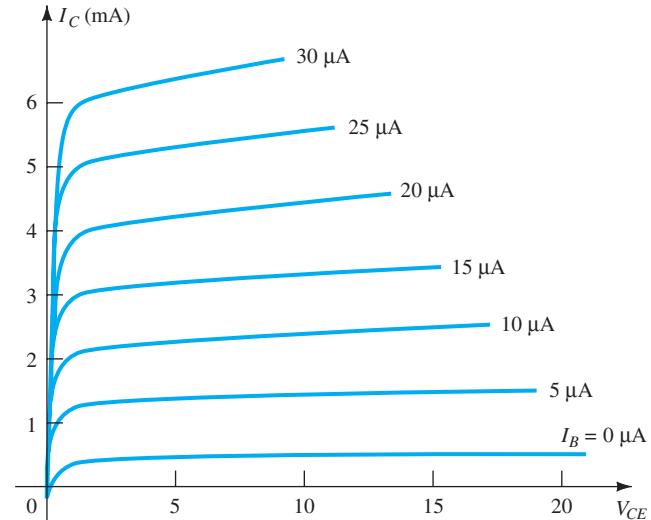
as shown in Fig. 4.25. Different levels of  $I_{B_Q}$  will, of course, move the  $Q$ -point up or down the load line.

### EXAMPLE 4.7

- Draw the load line for the network of Fig. 4.26a on the characteristics for the transistor appearing in Fig. 4.26b.
- For a  $Q$ -point at the intersection of the load line with a base current of  $15 \mu\text{A}$ , find the values of  $I_{C_Q}$  and  $V_{CE_Q}$ .
- Determine the dc beta at the  $Q$ -point.
- Using the beta for the network determined in part c, calculate the required value of  $R_B$  and suggest a possible standard value.



**FIG. 4.26a**  
Network for Example 4.7.



**FIG. 4.26b**  
Example 4.7.

### Solution:

- Two points on the characteristics are required to draw the load line.

$$\text{At } V_{CE} = 0 \text{ V: } I_C = \frac{V_{CC}}{R_C + R_E} = \frac{18 \text{ V}}{2.2 \text{ k}\Omega + 1.1 \text{ k}\Omega} = \frac{18 \text{ V}}{3.3 \text{ k}\Omega} = 5.45 \text{ mA}$$

$$\text{At } I_C = 0 \text{ mA: } V_{CE} = V_{CC} = 18 \text{ V}$$

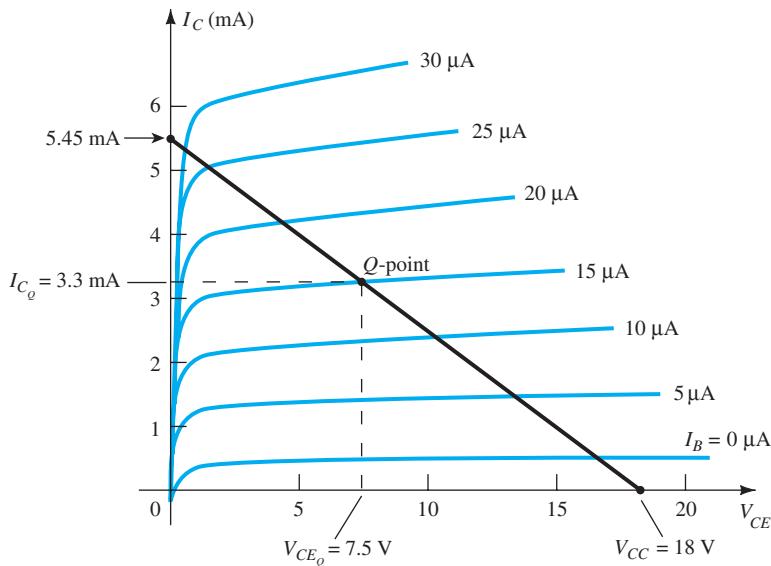
The resulting load line appears in Fig. 4.27.

- From the characteristics of Fig. 4.27 we find

$$V_{CE_Q} \approx 7.5 \text{ V}, I_{C_Q} \approx 3.3 \text{ mA}$$

- The resulting dc beta is:

$$\beta = \frac{I_{C_Q}}{I_{B_Q}} = \frac{3.3 \text{ mA}}{15 \mu\text{A}} = 220$$



**FIG. 4.27**  
Example 4.7.

d. Applying Eq. 4.17:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{18 \text{ V} - 0.7 \text{ V}}{R_B + (220 + 1)(1.1 \text{ k}\Omega)}$$

$$\text{and } 15 \mu\text{A} = \frac{17.3 \text{ V}}{R_B + (221)(1.1 \text{ k}\Omega)} = \frac{17.3 \text{ V}}{R_B + 243.1 \text{ k}\Omega}$$

$$\text{so that } (15 \mu\text{A})(R_B) + (15 \mu\text{A})(243.1 \text{ k}\Omega) = 17.3 \text{ V}$$

$$\text{and } (15 \mu\text{A})(R_B) = 17.3 \text{ V} - 3.65 \text{ V} = 13.65 \text{ V}$$

$$\text{resulting in } R_B + \frac{13.65 \text{ V}}{15 \mu\text{A}} = 910 \text{ k}\Omega$$

## 4.5 VOLTAGE-DIVIDER BIAS CONFIGURATION

In the previous bias configurations the bias current  $I_{C_Q}$  and voltage  $V_{CE_Q}$  were a function of the current gain  $\beta$  of the transistor. However, because  $\beta$  is temperature sensitive, especially for silicon transistors, and the actual value of beta is usually not well defined, it would be desirable to develop a bias circuit that is less dependent on, or in fact is independent of, the transistor beta. The voltage-divider bias configuration of Fig. 4.28 is such a network. If analyzed on an exact basis, the sensitivity to changes in beta is quite small. If the circuit parameters are properly chosen, the resulting levels of  $I_{C_Q}$  and  $V_{CE_Q}$  can be almost totally independent of beta. Recall from previous discussions that a *Q*-point is defined by a fixed level of  $I_{C_Q}$  and  $V_{CE_Q}$  as shown in Fig. 4.29. The level of  $I_{B_Q}$  will change with the change in beta, but the operating point on the characteristics defined by  $I_{C_Q}$  and  $V_{CE_Q}$  can remain fixed if the proper circuit parameters are employed.

As noted earlier, there are two methods that can be applied to analyze the voltage-divider configuration. The reason for the choice of names for this configuration will become obvious in the analysis to follow. The first to be demonstrated is the *exact method*, which can be applied to *any* voltage-divider configuration. The second is referred to as the *approximate method* and can be applied only if specific conditions are satisfied. The approximate approach permits a more direct analysis with a savings in time and energy. It is also particularly helpful in the design mode to be described in a later section. All in all, the approximate approach can be applied to the majority of situations and therefore should be examined with the same interest as the exact method.

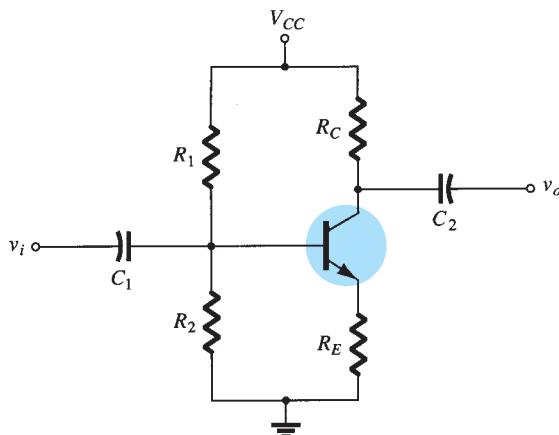


FIG. 4.28

Voltage-divider bias configuration.

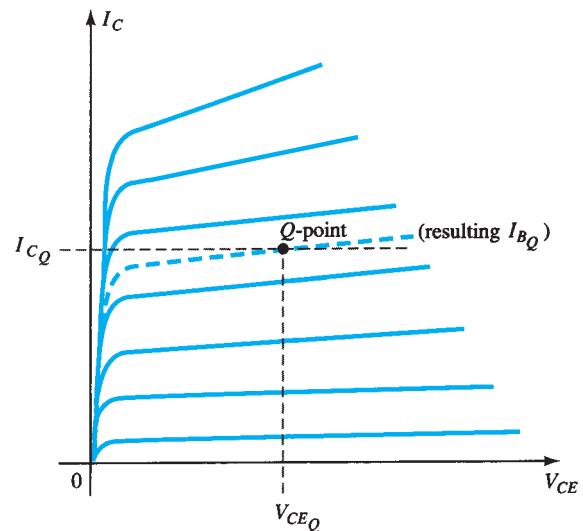
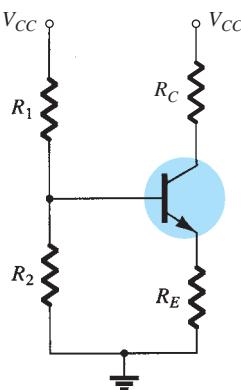


FIG. 4.29

Defining the Q-point for the voltage-divider bias configuration.

**Exact Analysis**

For the dc analysis the network of Fig. 4.28 can be redrawn as shown in Fig. 4.30. The input side of the network can then be redrawn as shown in Fig. 4.31 for the dc analysis. The Thévenin equivalent network for the network to the left of the base terminal can then be found in the following manner:

**R<sub>Th</sub>** The voltage source is replaced by a short-circuit equivalent as shown in Fig. 4.32:

$$R_{Th} = R_1 \parallel R_2 \quad (4.28)$$

**E<sub>Th</sub>** The voltage source  $V_{CC}$  is returned to the network and the open-circuit Thévenin voltage of Fig. 4.33 determined as follows:

Applying the voltage-divider rule gives

$$E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2} \quad (4.29)$$

The Thévenin network is then redrawn as shown in Fig. 4.34, and  $I_{BQ}$  can be determined by first applying Kirchhoff's voltage law in the clockwise direction for the loop indicated:

$$E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

Substituting  $I_E = (\beta + 1)I_B$  and solving for  $I_B$  yields

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} \quad (4.30)$$

Although Eq. (4.30) initially appears to be different from those developed earlier, note that the numerator is again a difference of two voltage levels and the denominator is the base resistance plus the emitter resistor reflected by  $(\beta + 1)$ —certainly very similar to Eq. (4.17).

Once  $I_B$  is known, the remaining quantities of the network can be found in the same manner as developed for the emitter-bias configuration. That is,

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \quad (4.31)$$

Redrawing the input side of the network of Fig. 4.28.

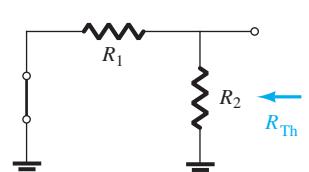


FIG. 4.32  
Determining  $R_{Th}$ .

which is exactly the same as Eq. (4.19). The remaining equations for  $V_E$ ,  $V_C$ , and  $V_B$  are also the same as obtained for the emitter-bias configuration.

**EXAMPLE 4.8** Determine the dc bias voltage  $V_{CE}$  and the current  $I_C$  for the voltage-divider configuration of Fig. 4.35.

**Solution:** Eq. (4.28):  $R_{Th} = R_1 \parallel R_2$

$$= \frac{(39 \text{ k}\Omega)(3.9 \text{ k}\Omega)}{39 \text{ k}\Omega + 3.9 \text{ k}\Omega} = 3.55 \text{ k}\Omega$$

Eq. (4.29):  $E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2}$

$$= \frac{(3.9 \text{ k}\Omega)(22 \text{ V})}{39 \text{ k}\Omega + 3.9 \text{ k}\Omega} = 2 \text{ V}$$

Eq. (4.30):  $I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$

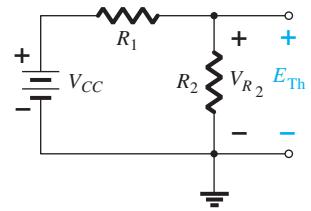
$$= \frac{2 \text{ V} - 0.7 \text{ V}}{3.55 \text{ k}\Omega + (101)(1.5 \text{ k}\Omega)} = \frac{1.3 \text{ V}}{3.55 \text{ k}\Omega + 151.5 \text{ k}\Omega}$$

$$= 8.38 \mu\text{A}$$

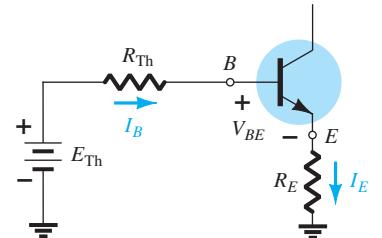
$$I_C = \beta I_B$$

$$= (100)(8.38 \mu\text{A})$$

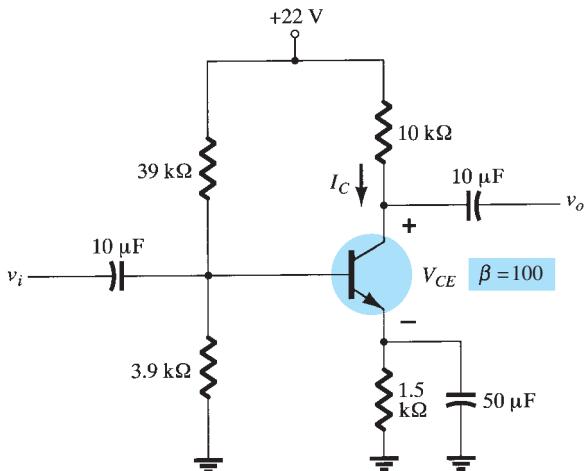
$$= \mathbf{0.84 \text{ mA}}$$



**FIG. 4.33**  
Determining  $E_{Th}$ .



**FIG. 4.34**  
Inserting the Thévenin equivalent circuit.



**FIG. 4.35**  
Beta-stabilized circuit for Example 4.8.

Eq. (4.31):  $V_{CE} = V_{CC} - I_C(R_C + R_E)$

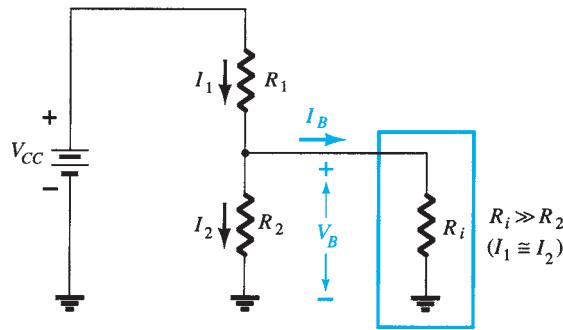
$$= 22 \text{ V} - (0.84 \text{ mA})(10 \text{ k}\Omega + 1.5 \text{ k}\Omega)$$

$$= 22 \text{ V} - 9.66 \text{ V}$$

$$= \mathbf{12.34 \text{ V}}$$

## Approximate Analysis

The input section of the voltage-divider configuration can be represented by the network of Fig. 4.36. The resistance  $R_i$  is the equivalent resistance between base and ground for the transistor with an emitter resistor  $R_E$ . Recall from Section 4.4 [Eq. (4.18)] that the reflected resistance between base and emitter is defined by  $R_i = (\beta + 1)R_E$ . If  $R_i$  is much larger than the resistance  $R_2$ , the current  $I_B$  will be much smaller than  $I_2$  (current always seeks the path of least resistance) and  $I_2$  will be approximately equal to  $I_1$ . If we accept the approximation that  $I_B$  is essentially 0 A compared to  $I_1$  or  $I_2$ , then  $I_1 = I_2$ , and  $R_1$  and  $R_2$  can be considered series elements. The voltage across  $R_2$ , which is actually the base voltage, can be



**FIG. 4.36**  
Partial-bias circuit for calculating the approximate base voltage  $V_B$ .

determined using the voltage-divider rule (hence the name for the configuration). That is,

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} \quad (4.32)$$

Because  $R_i = (\beta + 1)R_E \cong \beta R_E$  the condition that will define whether the approximate approach can be applied is

$$\beta R_E \geq 10R_2 \quad (4.33)$$

In other words, if  $\beta$  times the value of  $R_E$  is at least 10 times the value of  $R_2$ , the approximate approach can be applied with a high degree of accuracy.

Once  $V_B$  is determined, the level of  $V_E$  can be calculated from

$$V_E = V_B - V_{BE} \quad (4.34)$$

and the emitter current can be determined from

$$I_E = \frac{V_E}{R_E} \quad (4.35)$$

and

$$I_{CQ} \cong I_E \quad (4.36)$$

The collector-to-emitter voltage is determined by

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

but because  $I_E \cong I_C$ ,

$$V_{CEQ} = V_{CC} - I_C (R_C + R_E) \quad (4.37)$$

Note in the sequence of calculations from Eq. (4.33) through Eq. (4.37) that  $\beta$  does not appear and  $I_B$  was not calculated. The  $Q$ -point (as determined by  $I_{CQ}$  and  $V_{CEQ}$ ) is therefore independent of the value of  $\beta$ .

**EXAMPLE 4.9** Repeat the analysis of Fig. 4.35 using the approximate technique, and compare solutions for  $I_{CQ}$  and  $V_{CEQ}$ .

**Solution:** Testing:

$$\begin{aligned} \beta R_E &\geq 10R_2 \\ (100)(1.5 \text{ k}\Omega) &\geq 10(3.9 \text{ k}\Omega) \\ 150 \text{ k}\Omega &\geq 39 \text{ k}\Omega \text{ (satisfied)} \end{aligned}$$

$$\begin{aligned}\text{Eq. (4.32): } V_B &= \frac{R_2 V_{CC}}{R_1 + R_2} \\ &= \frac{(3.9 \text{ k}\Omega)(22 \text{ V})}{39 \text{ k}\Omega + 3.9 \text{ k}\Omega} \\ &= 2 \text{ V}\end{aligned}$$

Note that the level of  $V_B$  is the same as  $E_{Th}$  determined in Example 4.7. Essentially, therefore, the primary difference between the exact and approximate techniques is the effect of  $R_{Th}$  in the exact analysis that separates  $E_{Th}$  and  $V_B$ .

$$\begin{aligned}\text{Eq. (4.34): } V_E &= V_B - V_{BE} \\ &= 2 \text{ V} - 0.7 \text{ V} \\ &= 1.3 \text{ V} \\ I_{CQ} \cong I_E &= \frac{V_E}{R_E} = \frac{1.3 \text{ V}}{1.5 \text{ k}\Omega} = 0.867 \text{ mA}\end{aligned}$$

compared to 0.84 mA with the exact analysis. Finally,

$$\begin{aligned}V_{CEQ} &= V_{CC} - I_C(R_C + R_E) \\ &= 22 \text{ V} - (0.867 \text{ mA})(10 \text{ k}\Omega + 1.5 \text{ k}\Omega) \\ &= 22 \text{ V} - 9.97 \text{ V} \\ &= 12.03 \text{ V}\end{aligned}$$

versus 12.34 V obtained in Example 4.8.

The results for  $I_{CQ}$  and  $V_{CEQ}$  are certainly close, and considering the actual variation in parameter values, one can certainly be considered as accurate as the other. The larger the level of  $R_i$  compared to  $R_2$ , the closer is the approximate to the exact solution. Example 4.11 will compare solutions at a level well below the condition established by Eq. (4.33).

**EXAMPLE 4.10** Repeat the exact analysis of Example 4.8 if  $\beta$  is reduced to 50, and compare solutions for  $I_{CQ}$  and  $V_{CEQ}$ .

**Solution:** This example is not a comparison of exact versus approximate methods, but a testing of how much the  $Q$ -point will move if the level of  $\beta$  is cut in half.  $R_{Th}$  and  $E_{Th}$  are the same:

$$\begin{aligned}R_{Th} &= 3.55 \text{ k}\Omega, \quad E_{Th} = 2 \text{ V} \\ I_B &= \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} \\ &= \frac{2 \text{ V} - 0.7 \text{ V}}{3.55 \text{ k}\Omega + (51)(1.5 \text{ k}\Omega)} = \frac{1.3 \text{ V}}{3.55 \text{ k}\Omega + 76.5 \text{ k}\Omega} \\ &= 16.24 \mu\text{A} \\ I_{CQ} &= \beta I_B \\ &= (50)(16.24 \mu\text{A}) \\ &= 0.81 \text{ mA} \\ V_{CEQ} &= V_{CC} - I_C(R_C + R_E) \\ &= 22 \text{ V} - (0.81 \text{ mA})(10 \text{ k}\Omega + 1.5 \text{ k}\Omega) \\ &= 12.69 \text{ V}\end{aligned}$$

Tabulating the results, we have:

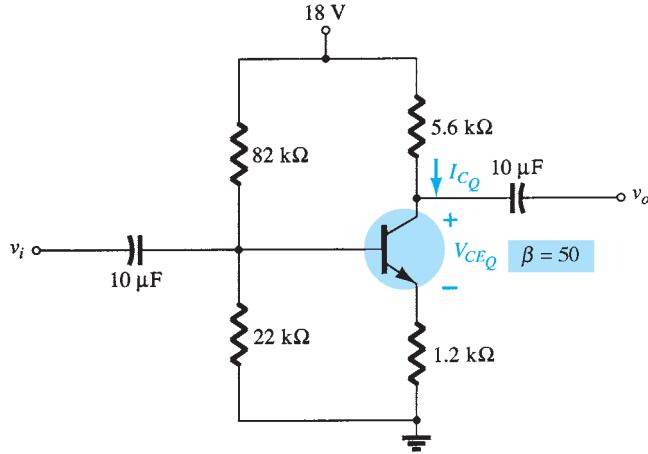
*Effect of  $\beta$  variation on the response of the voltage-divider configuration of Fig. 4.35.*

$\beta$	$I_{CQ}$ (mA)	$V_{CEQ}$ (V)
100	0.84 mA	12.34 V
50	0.81 mA	12.69 V

The results clearly show the relative insensitivity of the circuit to the change in  $\beta$ . Even though  $\beta$  is drastically cut in half, from 100 to 50, the levels of  $I_{CQ}$  and  $V_{CEQ}$  are essentially the same.

**Important Note:** Looking back on the results for the fixed-bias configuration, we find the current decreased from 4.71 mA to 2.35 mA when beta dropped from 100 to 50. For the voltage-divider configuration, the same change in beta only resulted in a change in current from 0.84 mA to 0.81 mA. Even more noticeable is the change in  $V_{CEQ}$  for the fixed-bias configuration. Dropping beta from 100 to 50 resulted in an increase in voltage from 1.64 to 6.83 V (a change of over 300%). For the voltage-divider configuration, the increase in voltage was only from 12.34 V to 12.69 V, which is a change of less than 3%. In summary, therefore, changing beta by 50% resulted in a change in an important network parameter of over 300% for the fixed-bias configuration and less than 3% for the voltage-divider configuration—a significant difference.

**EXAMPLE 4.11** Determine the levels of  $I_{CQ}$  and  $V_{CEQ}$  for the voltage-divider configuration of Fig. 4.37 using the exact and approximate techniques and compare solutions. In this case, the conditions of Eq. (4.33) will not be satisfied and the results will reveal the difference in solution if the criterion of Eq. (4.33) is ignored.



**FIG. 4.37**  
Voltage-divider configuration for Example 4.11.

**Solution:** Exact analysis:

Eq. (4.33):

$$\beta R_E \geq 10R_2$$

$$(50)(1.2 \text{ k}\Omega) \geq 10(22 \text{ k}\Omega)$$

$$60 \text{ k}\Omega \neq 220 \text{ k}\Omega \text{ (not satisfied)}$$

$$R_{\text{Th}} = R_1 \parallel R_2 = 82 \text{ k}\Omega \parallel 22 \text{ k}\Omega = 17.35 \text{ k}\Omega$$

$$E_{\text{Th}} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{22 \text{ k}\Omega (18 \text{ V})}{82 \text{ k}\Omega + 22 \text{ k}\Omega} = 3.81 \text{ V}$$

$$I_B = \frac{E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_E} = \frac{3.81 \text{ V} - 0.7 \text{ V}}{17.35 \text{ k}\Omega + (51)(1.2 \text{ k}\Omega)} = \frac{3.11 \text{ V}}{78.55 \text{ k}\Omega} = 39.6 \mu\text{A}$$

$$I_{CQ} = \beta I_B = (50)(39.6 \mu\text{A}) = 1.98 \text{ mA}$$

$$\begin{aligned} V_{CEQ} &= V_{CC} - I_C(R_C + R_E) \\ &= 18 \text{ V} - (1.98 \text{ mA})(5.6 \text{ k}\Omega + 1.2 \text{ k}\Omega) \\ &= 4.54 \text{ V} \end{aligned}$$

Approximate analysis:

$$V_B = E_{\text{Th}} = 3.81 \text{ V}$$

$$V_E = V_B - V_{BE} = 3.81 \text{ V} - 0.7 \text{ V} = 3.11 \text{ V}$$

$$I_{CQ} \cong I_E = \frac{V_E}{R_E} = \frac{3.11 \text{ V}}{1.2 \text{ k}\Omega} = 2.59 \text{ mA}$$

$$\begin{aligned} V_{CEQ} &= V_{CC} - I_C(R_C + R_E) \\ &= 18 \text{ V} - (2.59 \text{ mA})(5.6 \text{ k}\Omega + 1.2 \text{ k}\Omega) \\ &= 3.88 \text{ V} \end{aligned}$$

*Comparing the exact and approximate approaches.*

	$I_{C_Q}$ (mA)	$V_{CE_Q}$ (V)
Exact	1.98	4.54
Approximate	2.59	3.88

The results reveal the difference between exact and approximate solutions.  $I_{C_Q}$  is about 30% greater with the approximate solution, whereas  $V_{CE_Q}$  is about 10% less. The results are notably different in magnitude, but even though  $\beta R_E$  is only about three times larger than  $R_2$ , the results are still relatively close to each other. For the future, however, our analysis will be dictated by Eq. (4.33) to ensure a close similarity between exact and approximate solutions.

## Transistor Saturation

The output collector-emitter circuit for the voltage-divider configuration has the same appearance as the emitter-biased circuit analyzed in Section 4.4. The resulting equation for the saturation current (when  $V_{CE}$  is set to 0 V on the schematic) is therefore the same as obtained for the emitter-biased configuration. That is,

$$I_{C_{\text{sat}}} = I_{C_{\text{max}}} = \frac{V_{CC}}{R_C + R_E} \quad (4.38)$$

## Load-Line Analysis

The similarities with the output circuit of the emitter-biased configuration result in the same intersections for the load line of the voltage-divider configuration. The load line will therefore have the same appearance as that of Fig. 4.25, with

$$I_C = \frac{V_{CC}}{R_C + R_E} \Big|_{V_{CE}=0 \text{ V}} \quad (4.39)$$

and

$$V_{CE} = V_{CC} \Big|_{I_C=0 \text{ mA}} \quad (4.40)$$

The level of  $I_B$  is of course determined by a different equation for the voltage-divider bias and the emitter-bias configurations.

## 4.6 COLLECTOR FEEDBACK CONFIGURATION

An improved level of stability can also be obtained by introducing a feedback path from collector to base as shown in Fig. 4.38. Although the  $Q$ -point is not totally independent of beta (even under approximate conditions), the sensitivity to changes in beta or temperature variations is normally less than encountered for the fixed-bias or emitter-biased configurations. The analysis will again be performed by first analyzing the base-emitter loop, with the results then applied to the collector-emitter loop.

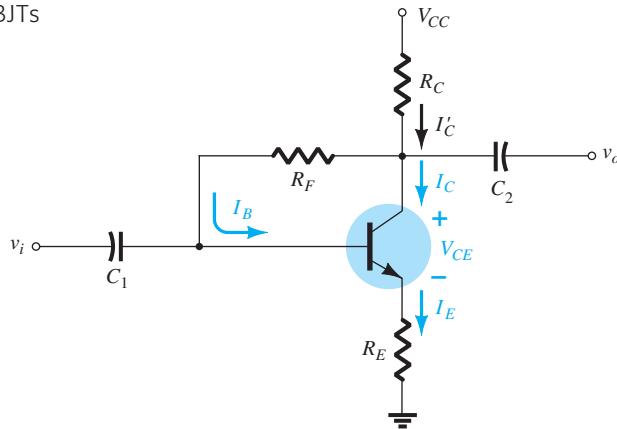
### Base-Emitter Loop

Figure 4.39 shows the base-emitter loop for the voltage feedback configuration. Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction will result in

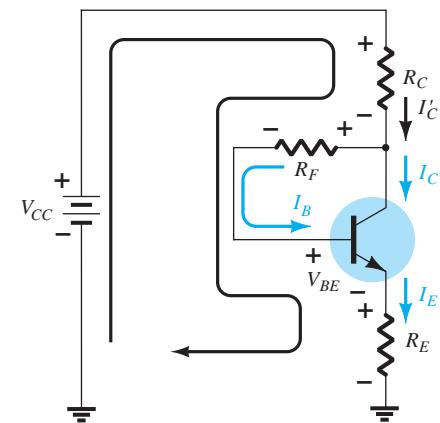
$$V_{CC} - I'_C R_C - I_B R_F - V_{BE} - I_E R_E = 0$$

It is important to note that the current through  $R_C$  is not  $I_C$ , but  $I'_C$  (where  $I'_C = I_C + I_B$ ). However, the level of  $I_C$  and  $I'_C$  far exceeds the usual level of  $I_B$ , and the approximation  $I'_C \approx I_C$  is normally employed. Substituting  $I'_C \approx I_C = \beta I_B$  and  $I_E \approx I_C$  results in

$$V_{CC} - \beta I_B R_C - I_B R_F - V_{BE} - \beta I_B R_E = 0$$



**FIG. 4.38**  
DC bias circuit with voltage feedback.



**FIG. 4.39**  
Base-emitter loop for the network of Fig. 4.38.

Gathering terms, we have

$$V_{CC} - V_{BE} - \beta I_B (R_C + R_E) - I_B R_F = 0$$

and solving for  $I_B$  yields

$$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)} \quad (4.41)$$

The result is quite interesting in that the format is very similar to equations for  $I_B$  obtained for earlier configurations. The numerator is again the difference of available voltage levels, whereas the denominator is the base resistance plus the collector and emitter resistors reflected by beta. In general, therefore, the feedback path results in a reflection of the resistance  $R_C$  back to the input circuit, much like the reflection of  $R_E$ .

In general, the equation for  $I_B$  has the following format, which can be compared with the result for the fixed-bias and emitter-bias configurations.

$$I_B = \frac{V'}{R_F + \beta R'}$$

For the fixed-bias configuration  $\beta R'$  does not exist. For the emitter-bias setup (with  $\beta + 1 \approx \beta$ ),  $R' = R_E$ .

Because  $I_C = \beta I_B$ ,

$$I_{CQ} = \frac{\beta V'}{R_F + \beta R'} = \frac{V'}{\frac{R_F}{\beta} + R'}$$

In general, the larger  $R'$  is compared with  $\frac{R_F}{\beta}$ , the more accurate the approximation that

$$I_{CQ} \approx \frac{V'}{R'}$$

The result is an equation absent of  $\beta$ , which would be very stable for variations in  $\beta$ . Because  $R'$  is typically larger for the voltage-feedback configuration than for the emitter-bias configuration, the sensitivity to variations in beta is less. Of course,  $R'$  is  $0 \Omega$  for the fixed-bias configuration and is therefore quite sensitive to variations in beta.

### Collector-Emitter Loop

The collector-emitter loop for the network of Fig. 4.38 is provided in Fig. 4.40. Applying Kirchhoff's voltage law around the indicated loop in the clockwise direction results in

$$I_E R_E + V_{CE} + I'_C R_C - V_{CC} = 0$$

**FIG. 4.40**  
Collector-emitter loop for the network of Fig. 4.38.

Because  $I_C' \cong I_C$  and  $I_E \cong I_C$ , we have

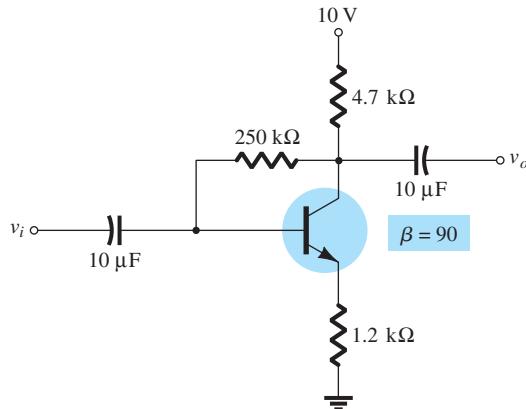
$$I_C(R_C + R_E) + V_{CE} - V_{CC} = 0$$

and

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \quad (4.42)$$

which is exactly as obtained for the emitter-bias and voltage-divider bias configurations.

**EXAMPLE 4.12** Determine the quiescent levels of  $I_{CQ}$  and  $V_{CEQ}$  for the network of Fig. 4.41.



**FIG. 4.41**  
Network for Example 4.12.

**Solution:** Eq. (4.41):  $I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)}$

$$= \frac{10 \text{ V} - 0.7 \text{ V}}{250 \text{ k}\Omega + (90)(4.7 \text{ k}\Omega + 1.2 \text{ k}\Omega)}$$

$$= \frac{9.3 \text{ V}}{250 \text{ k}\Omega + 531 \text{ k}\Omega} = \frac{9.3 \text{ V}}{781 \text{ k}\Omega}$$

$$= 11.91 \mu\text{A}$$

$$I_{CQ} = \beta I_B = (90)(11.91 \mu\text{A})$$

$$= 1.07 \text{ mA}$$

$$V_{CEQ} = V_{CC} - I_C(R_C + R_E)$$

$$= 10 \text{ V} - (1.07 \text{ mA})(4.7 \text{ k}\Omega + 1.2 \text{ k}\Omega)$$

$$= 10 \text{ V} - 6.31 \text{ V}$$

$$= 3.69 \text{ V}$$

**EXAMPLE 4.13** Repeat Example 4.12 using a beta of 135 (50% greater than in Example 4.12).

**Solution:** It is important to note in the solution for  $I_B$  in Example 4.12 that the second term in the denominator of the equation is much larger than the first. Recall in a recent discussion that the larger this second term is compared to the first, the less is the sensitivity to changes in beta. In this example, the level of beta is increased by 50%, which will increase the magnitude of this second term even more compared to the first. It is more important to note in these examples, however, that once the second term is relatively large compared to the first, the sensitivity to changes in beta is significantly less.

Solving for  $I_B$  gives

$$\begin{aligned} I_B &= \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} \\ &= \frac{10 \text{ V} - 0.7 \text{ V}}{250 \text{ k}\Omega + (135)(4.7 \text{ k}\Omega + 1.2 \text{ k}\Omega)} \\ &= \frac{9.3 \text{ V}}{250 \text{ k}\Omega + 796.5 \text{ k}\Omega} = \frac{9.3 \text{ V}}{1046.5 \text{ k}\Omega} \\ &= 8.89 \mu\text{A} \end{aligned}$$

and

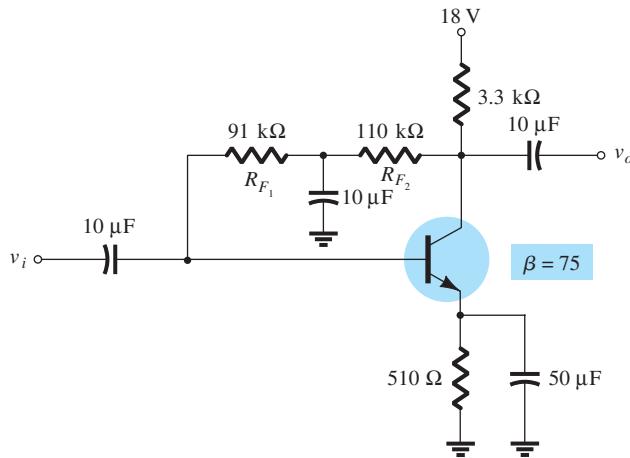
$$\begin{aligned} I_{CQ} &= \beta I_B \\ &= (135)(8.89 \mu\text{A}) \\ &= 1.2 \text{ mA} \end{aligned}$$

and

$$\begin{aligned} V_{CEQ} &= V_{CC} - I_C(R_C + R_E) \\ &= 10 \text{ V} - (1.2 \text{ mA})(4.7 \text{ k}\Omega + 1.2 \text{ k}\Omega) \\ &= 10 \text{ V} - 7.08 \text{ V} \\ &= 2.92 \text{ V} \end{aligned}$$

Even though the level of  $\beta$  increased 50%, the level of  $I_{CQ}$  only increased 12.1%, whereas the level of  $V_{CEQ}$  decreased about 20.9%. If the network were a fixed-bias design, a 50% increase in  $\beta$  would have resulted in a 50% increase in  $I_{CQ}$  and a dramatic change in the location of the  $Q$ -point.

**EXAMPLE 4.14** Determine the dc level of  $I_B$  and  $V_C$  for the network of Fig. 4.42.



**FIG. 4.42**

Network for Example 4.14.

**Solution:** In this case, the base resistance for the dc analysis is composed of two resistors with a capacitor connected from their junction to ground. For the dc mode, the capacitor assumes the open-circuit equivalence, and  $R_B = R_{F1} + R_{F2}$ .

Solving for  $I_B$  gives

$$\begin{aligned} I_B &= \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} \\ &= \frac{18 \text{ V} - 0.7 \text{ V}}{(91 \text{ k}\Omega + 110 \text{ k}\Omega) + (75)(3.3 \text{ k}\Omega + 0.51 \text{ k}\Omega)} \\ &= \frac{17.3 \text{ V}}{201 \text{ k}\Omega + 285.75 \text{ k}\Omega} = \frac{17.3 \text{ V}}{486.75 \text{ k}\Omega} \\ &= 35.5 \mu\text{A} \end{aligned}$$

$$\begin{aligned}
 I_C &= \beta I_B \\
 &= (75)(35.5 \mu\text{A}) \\
 &= 2.66 \text{ mA} \\
 V_C &= V_{CC} - I'_C R_C \approx V_{CC} - I_C R_C \\
 &= 18 \text{ V} - (2.66 \text{ mA})(3.3 \text{ k}\Omega) \\
 &= 18 \text{ V} - 8.78 \text{ V} \\
 &= \mathbf{9.22 \text{ V}}
 \end{aligned}$$

### Saturation Conditions

Using the approximation  $I'_C = I_C$ , we find that the equation for the saturation current is the same as obtained for the voltage-divider and emitter-bias configurations. That is,

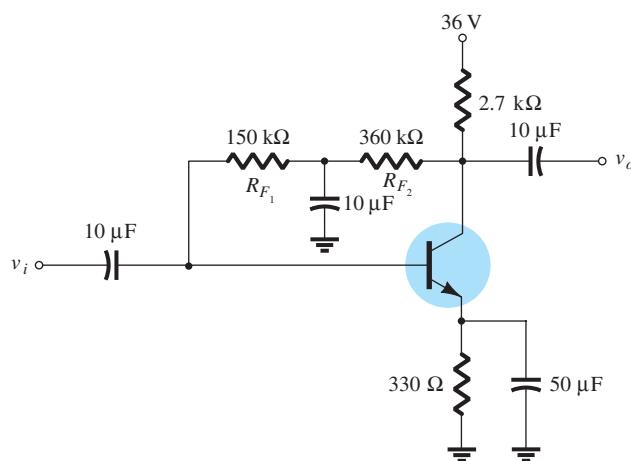
$$I_{C_{\text{sat}}} = I_{C_{\text{max}}} = \frac{V_{CC}}{R_C + R_E} \quad (4.43)$$

### Load-Line Analysis

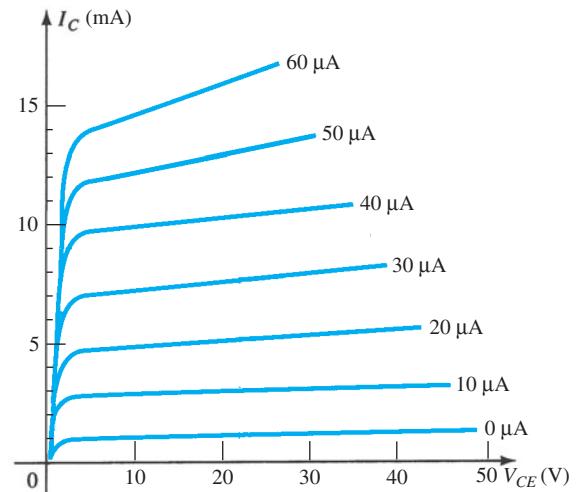
Continuing with the approximation  $I'_C = I_C$  results in the same load line defined for the voltage-divider and emitter-biased configurations. The level of  $I_{B_Q}$  is defined by the chosen bias configuration.

**EXAMPLE 4.15** Given the network of Fig. 4.43 and the BJT characteristics of Fig. 4.44.

- Draw the load line for the network on the characteristics.
- Determine the dc beta in the center region of the characteristics. Define the chosen point as the  $Q$ -point.
- Using the dc beta calculated in part b, find the dc value of  $I_B$ .
- Find  $I_{C_Q}$  and  $I_{CEQ}$ .



**FIG. 4.43**  
Network for Example 4.15.



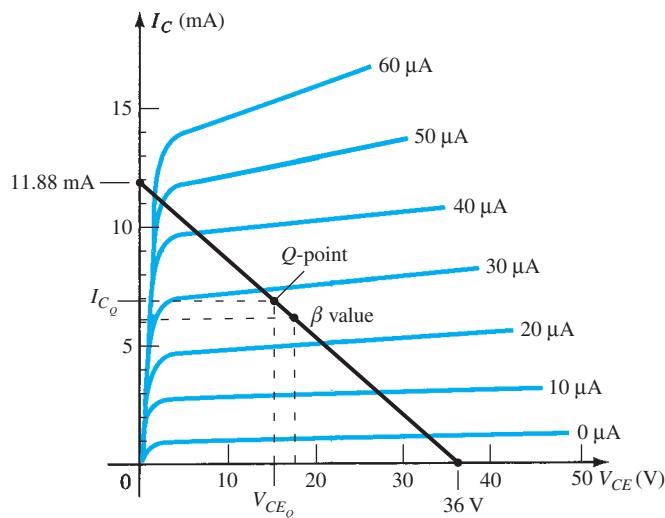
**FIG. 4.44**  
BJT characteristics.

### Solution:

- The load line is drawn on Fig. 4.45 as determined by the following intersections:

$$V_{CE} = 0 \text{ V}: I_C = \frac{V_{CC}}{R_C + R_E} = \frac{36 \text{ V}}{2.7 \text{ k}\Omega + 330 \Omega} = \mathbf{11.88 \text{ mA}}$$

$$I_C = 0 \text{ mA}: V_{CE} = V_{CC} = \mathbf{36 \text{ V}}$$



**FIG. 4.45**  
Defining the  $Q$ -point for the voltage-divider bias configuration of Fig. 4.43.

- b. The dc beta was determined using  $I_B = 25 \mu\text{A}$  and  $V_{CE}$  about 17 V.

$$\beta \cong \frac{I_{C_Q}}{I_{B_Q}} = \frac{6.2 \text{ mA}}{25 \mu\text{A}} = 248$$

- c. Using Eq. 4.41:

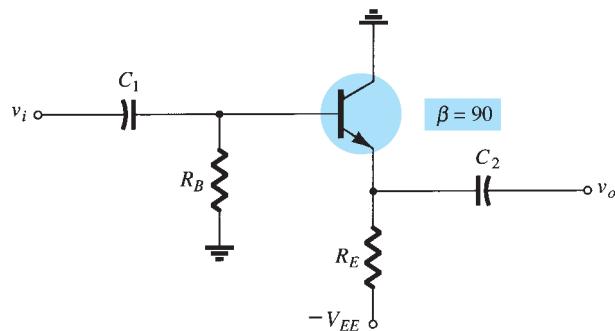
$$\begin{aligned} I_B &= \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} = \frac{36 \text{ V} - 0.7 \text{ V}}{510 \text{ k}\Omega + 248(2.7 \text{ k}\Omega + 330 \Omega)} \\ &= \frac{35.3 \text{ V}}{510 \text{ k}\Omega + 751.44 \text{ k}\Omega} \\ \text{and } I_B &= \frac{35.3 \text{ V}}{1.261 \text{ M}\Omega} = 28 \mu\text{A} \end{aligned}$$

- d. From Fig. 4.45 the quiescent values are

$$I_{C_Q} \cong 6.9 \text{ mA} \text{ and } V_{CE_Q} \cong 15 \text{ V}$$

## 4.7 Emitter-Follower Configuration

The previous sections introduced configurations in which the output voltage is typically taken off the collector terminal of the BJT. This section will examine a configuration where the output is taken off the emitter terminal as shown in Fig. 4.46. The configuration of Fig. 4.46 is not the only one where the output can be taken off the emitter terminal. In fact, any of the configurations just described can be used so long as there is a resistor in the emitter leg.



**FIG. 4.46**  
Common-collector (emitter-follower) configuration.

The dc equivalent of the network of Fig. 4.46 appears in Fig. 4.47.

Applying Kirchhoff's voltage rule to the input circuit will result in

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

and using  $I_E = (\beta + 1)I_B$

$$I_B R_B + (\beta + 1)I_B R_E = V_{EE} - V_{BE}$$

so that

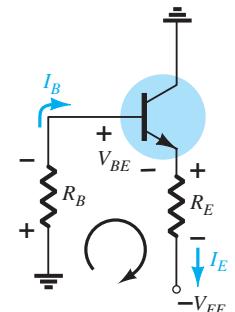
$$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E} \quad (4.44)$$

For the output network, an application of Kirchhoff's voltage law will result in

$$-V_{CE} - I_E R_E + V_{EE} = 0$$

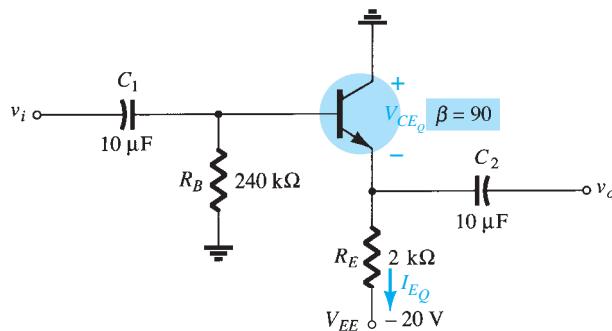
and

$$V_{CE} = V_{EE} - I_E R_E \quad (4.45)$$



**FIG. 4.47**  
dc equivalent of  
Fig. 4.46.

**EXAMPLE 4.16** Determine  $V_{CEQ}$  and  $I_{EQ}$  for the network of Fig. 4.48.



**FIG. 4.48**  
Example 4.16.

### Solution:

$$\begin{aligned} \text{Eq. 4.44: } I_B &= \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E} \\ &= \frac{20 \text{ V} - 0.7 \text{ V}}{240 \text{ k}\Omega + (90 + 1)2 \text{ k}\Omega} = \frac{19.3 \text{ V}}{240 \text{ k}\Omega + 182 \text{ k}\Omega} \\ &= \frac{19.3 \text{ V}}{422 \text{ k}\Omega} = 45.73 \mu\text{A} \end{aligned}$$

and Eq. 4.45:

$$\begin{aligned} V_{CEQ} &= V_{EE} - I_E R_E \\ &= V_{EE} - (\beta + 1)I_B R_E \\ &= 20 \text{ V} - (90 + 1)(45.73 \mu\text{A})(2 \text{ k}\Omega) \\ &= 20 \text{ V} - 8.32 \text{ V} \\ &= \mathbf{11.68 \text{ V}} \end{aligned}$$

$$\begin{aligned} I_{EQ} &= (\beta + 1)I_B = (91)(45.73 \mu\text{A}) \\ &= 4.16 \text{ mA} \end{aligned}$$

## 4.8 COMMON-BASE CONFIGURATION

The common-base configuration is unique in that the applied signal is connected to the emitter terminal and the base is at, or just above, ground potential. It is a fairly popular configuration because in the ac domain it has a very low input impedance, high output impedance, and good gain.

A typical common-base configuration appears in Fig. 4.49. Note that two supplies are used in this configuration and the base is the common terminal between the input emitter terminal and output collector terminal.

The dc equivalent of the input side of Fig. 4.49 appears in Fig. 4.50.

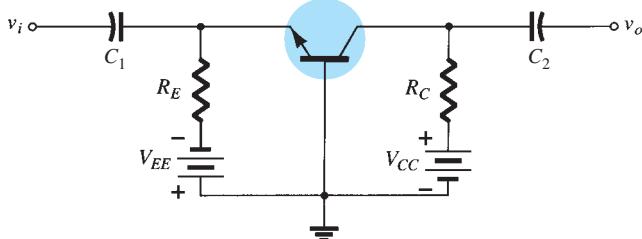


FIG. 4.49

Common-base configuration.

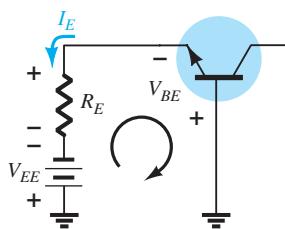


FIG. 4.50

Input dc equivalent of Fig. 4.49.

Applying Kirchhoff's voltage law will result in

$$-V_{EE} + I_E R_E + V_{BE} = 0$$

$$I_E = \frac{V_{EE} - V_{BE}}{R_E} \quad (4.46)$$

Applying Kirchhoff's voltage law to the entire outside perimeter of the network of Fig. 4.51 will result in

$$-V_{EE} + I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

and solving for  $V_{CE}$ :  $V_{CE} = V_{EE} + V_{CC} - I_E R_E - I_C R_C$

Because  $I_E \cong I_C$

$$V_{CE} = V_{EE} + V_{CC} - I_E (R_C + R_E) \quad (4.47)$$

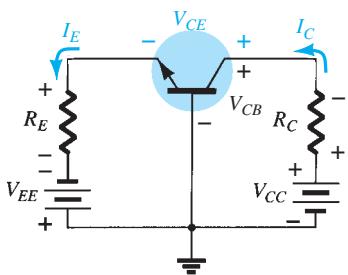


FIG. 4.51

Determining  $V_{CE}$  and  $V_{CB}$ .

The voltage  $V_{CB}$  of Fig. 4.51 can be found by applying Kirchhoff's voltage law to the output loop of Fig. 4.51 to obtain:

$$V_{CB} + I_C R_C - V_{CC} = 0$$

or

$$V_{CB} = V_{CC} - I_C R_C$$

Using

$$I_C \cong I_E$$

we have

$$V_{CB} = V_{CC} - I_C R_C \quad (4.48)$$

**EXAMPLE 4.17** Determine the currents  $I_E$  and  $I_B$  and the voltages  $V_{CE}$  and  $V_{CB}$  for the common-base configuration of Fig. 4.52.

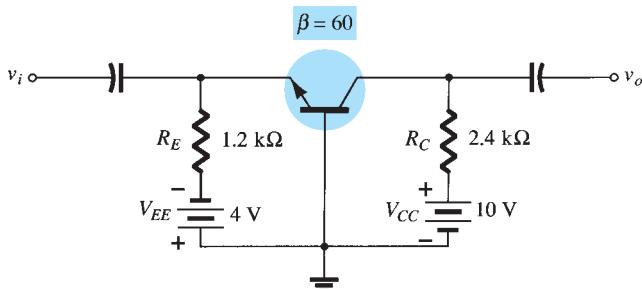


FIG. 4.52

Example 4.17.

**Solution:** Eq. 4.46:

$$I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

$$= \frac{4 \text{ V} - 0.7 \text{ V}}{1.2 \text{ k}\Omega} = 2.75 \text{ mA}$$

$$I_B = \frac{I_E}{\beta + 1} = \frac{2.75 \text{ mA}}{60 + 1} = \frac{2.75 \text{ mA}}{61}$$

$$= 45.08 \mu\text{A}$$

Eq. 4.47:

$$V_{CE} = V_{EE} + V_{CC} - I_E(R_C + R_E)$$

$$= 4 \text{ V} + 10 \text{ V} - (2.75 \text{ mA})(2.4 \text{ k}\Omega + 1.2 \text{ k}\Omega)$$

$$= 14 \text{ V} - (2.75 \text{ mA})(3.6 \text{ k}\Omega)$$

$$= 14 \text{ V} - 9.9 \text{ V}$$

$$= 4.1 \text{ V}$$

Eq. 4.48:

$$V_{CB} = V_{CC} - I_C R_C = V_{CC} - \beta I_B R_C$$

$$= 10 \text{ V} - (60)(45.08 \mu\text{A})(24 \text{ k}\Omega)$$

$$= 10 \text{ V} - 6.49 \text{ V}$$

$$= 3.51 \text{ V}$$

## 4.9 MISCELLANEOUS BIAS CONFIGURATIONS

There are a number of BJT bias configurations that do not match the basic mold of those analyzed in the previous sections. In fact, there are variations in design that would require many more pages than is possible in a single publication. However, the primary purpose here is to emphasize those characteristics of the device that permit a dc analysis of the configuration and to establish a general procedure toward the desired solution. For each configuration discussed thus far, the first step has been the derivation of an expression for the base current. Once the base current is known, the collector current and voltage levels of the output circuit can be determined quite directly. This is not to imply that all solutions will take this path, but it does suggest a possible route to follow if a new configuration is encountered.

The first example is simply one where the emitter resistor has been dropped from the voltage-feedback configuration of Fig. 4.38. The analysis is quite similar, but does require dropping  $R_E$  from the applied equation.

**EXAMPLE 4.18** For the network of Fig. 4.53:

- Determine  $I_{CQ}$  and  $V_{CEQ}$ .
- Find  $V_B$ ,  $V_C$ ,  $V_E$ , and  $V_{BC}$ .

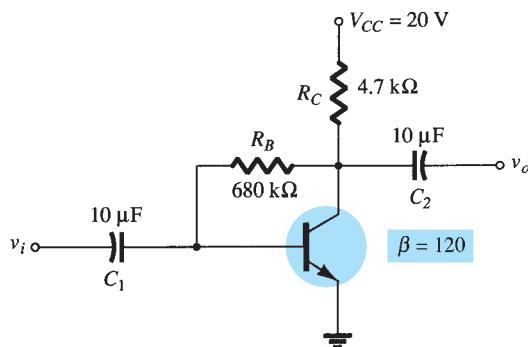


FIG. 4.53

Collector feedback with  $R_E = 0 \Omega$ .

**Solution:**

- a. The absence of  $R_E$  reduces the reflection of resistive levels to simply that of  $R_C$ , and the equation for  $I_B$  reduces to

$$\begin{aligned} I_B &= \frac{V_{CC} - V_{BE}}{R_B + \beta R_C} \\ &= \frac{20 \text{ V} - 0.7 \text{ V}}{680 \text{ k}\Omega + (120)(4.7 \text{ k}\Omega)} = \frac{19.3 \text{ V}}{1.244 \text{ M}\Omega} \\ &= 15.51 \mu\text{A} \end{aligned}$$

$$\begin{aligned} I_{CQ} &= \beta I_B = (120)(15.51 \mu\text{A}) \\ &= 1.86 \text{ mA} \end{aligned}$$

$$\begin{aligned} V_{CEQ} &= V_{CC} - I_C R_C \\ &= 20 \text{ V} - (1.86 \text{ mA})(4.7 \text{ k}\Omega) \\ &= 11.26 \text{ V} \end{aligned}$$

b.  $V_B = V_{BE} = 0.7 \text{ V}$

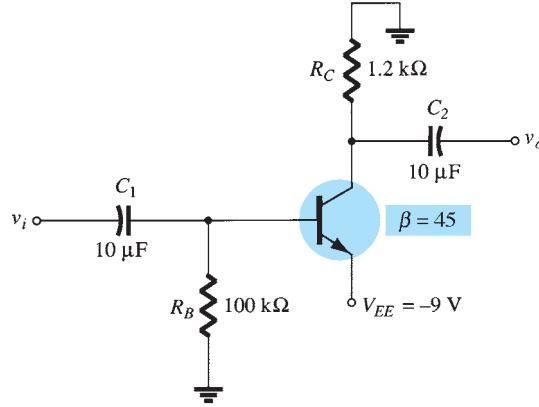
$$V_C = V_{CE} = 11.26 \text{ V}$$

$$V_E = 0 \text{ V}$$

$$\begin{aligned} V_{BC} &= V_B - V_C = 0.7 \text{ V} - 11.26 \text{ V} \\ &= -10.56 \text{ V} \end{aligned}$$

In the next example, the applied voltage is connected to the emitter leg and  $R_C$  is connected directly to ground. Initially, it appears somewhat unorthodox and quite different from those encountered thus far, but one application of Kirchhoff's voltage law to the base circuit will result in the desired base current.

**EXAMPLE 4.19** Determine  $V_C$  and  $V_B$  for the network of Fig. 4.54.



**FIG. 4.54**

Example 4.19.

**Solution:** Applying Kirchhoff's voltage law in the clockwise direction for the base–emitter loop results in

$$-I_B R_B - V_{BE} + V_{EE} = 0$$

and

$$I_B = \frac{V_{EE} - V_{BE}}{R_B}$$

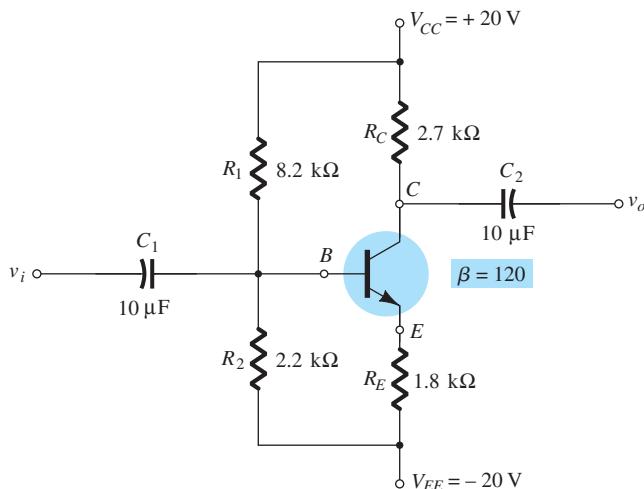
Substitution yields

$$\begin{aligned} I_B &= \frac{9 \text{ V} - 0.7 \text{ V}}{100 \text{ k}\Omega} \\ &= \frac{8.3 \text{ V}}{100 \text{ k}\Omega} \\ &= 83 \mu\text{A} \end{aligned}$$

$$\begin{aligned}
 I_C &= \beta I_B \\
 &= (45)(83 \mu\text{A}) \\
 &= 3.735 \text{ mA} \\
 V_C &= -I_C R_C \\
 &= -(3.735 \text{ mA})(1.2 \text{ k}\Omega) \\
 &= \mathbf{-4.48 \text{ V}} \\
 V_B &= -I_B R_B \\
 &= -(83 \mu\text{A})(100 \text{ k}\Omega) \\
 &= \mathbf{-8.3 \text{ V}}
 \end{aligned}$$

Example 4.20 employs a split supply and will require the application of Thévenin's theorem to determine the desired unknowns.

**EXAMPLE 4.20** Determine  $V_C$  and  $V_B$  for the network of Fig. 4.55.

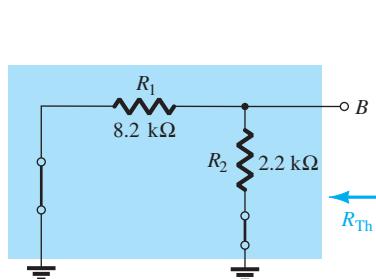


**FIG. 4.55**  
Example 4.20.

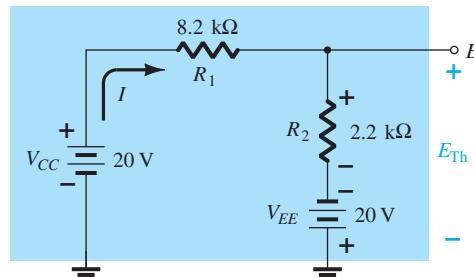
**Solution:** The Thévenin resistance and voltage are determined for the network to the left of the base terminal as shown in Figs. 4.56 and 4.57.

**$R_{Th}$**

$$R_{Th} = 8.2 \text{ k}\Omega \parallel 2.2 \text{ k}\Omega = 1.73 \text{ k}\Omega$$



**FIG. 4.56**  
Determining  $R_{Th}$ .



**FIG. 4.57**  
Determining  $E_{Th}$ .

$$I = \frac{V_{CC} + V_{EE}}{R_1 + R_2} = \frac{20 \text{ V} + 20 \text{ V}}{8.2 \text{ k}\Omega + 2.2 \text{ k}\Omega} = \frac{40 \text{ V}}{10.4 \text{ k}\Omega}$$

$$= 3.85 \text{ mA}$$

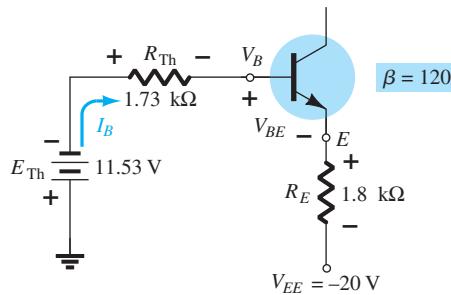
$$E_{Th} = IR_2 - V_{EE}$$

$$= (3.85 \text{ mA})(2.2 \text{ k}\Omega) - 20 \text{ V}$$

$$= -11.53 \text{ V}$$

The network can then be redrawn as shown in Fig. 4.58, where the application of Kirchhoff's voltage law results in

$$-E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E + V_{EE} = 0$$



**FIG. 4.58**  
Substituting the Thévenin equivalent circuit.

Substituting  $I_E = (\beta + 1)I_B$  gives

$$V_{EE} - E_{Th} - V_{BE} - (\beta + 1)I_B R_E - I_B R_{Th} = 0$$

and

$$I_B = \frac{V_{EE} - E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

$$= \frac{20 \text{ V} - 11.53 \text{ V} - 0.7 \text{ V}}{1.73 \text{ k}\Omega + (121)(1.8 \text{ k}\Omega)}$$

$$= \frac{7.77 \text{ V}}{219.53 \text{ k}\Omega}$$

$$= 35.39 \mu\text{A}$$

$$I_C = \beta I_B$$

$$= (120)(35.39 \mu\text{A})$$

$$= 4.25 \text{ mA}$$

$$V_C = V_{CC} - I_C R_C$$

$$= 20 \text{ V} - (4.25 \text{ mA})(2.7 \text{ k}\Omega)$$

$$= 8.53 \text{ V}$$

$$V_B = -E_{Th} - I_B R_{Th}$$

$$= -(11.53 \text{ V}) - (35.39 \mu\text{A})(1.73 \text{ k}\Omega)$$

$$= -11.59 \text{ V}$$

## 4.10 SUMMARY TABLE

Table 4.1 is a review of the most common single-stage BJT configurations with their respective equations. Note the similarities that exist between the equations for the various configurations.

**TABLE 4.1**  
*BJT Bias Configurations*

Type	Configuration	Pertinent Equations
Fixed-bias		$I_B = \frac{V_{CC} - V_{BE}}{R_B}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{CC} - I_C R_C$
Emitter-bias		$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $R_i = (\beta + 1)R_E$ $V_{CE} = V_{CC} - I_C (R_C + R_E)$
Voltage-divider bias		EXACT: $R_{Th} = R_1\parallel R_2, E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2}$ $I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{CC} - I_C (R_C + R_E)$ APPROXIMATE: $\beta R_E \geq 10R_2$ $V_B = \frac{R_2 V_{CC}}{R_1 + R_2}, V_E = V_B - V_{BE}$ $I_E = \frac{V_E}{R_E}, I_B = \frac{I_E}{\beta + 1}$ $V_{CE} = V_{CC} - I_C (R_C + R_E)$
Collector-feedback		$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{CC} - I_C (R_C + R_E)$
Emitter-follower		$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{EE} - I_E R_E$
Common-base		$I_E = \frac{V_{EE} - V_{BE}}{R_E}$ $I_B = \frac{I_E}{\beta + 1}, I_C = \beta I_B$ $V_{CE} = V_{EE} + V_{CC} - I_E (R_C + R_E)$ $V_{CB} = V_{CC} - I_C R_C$

## 4.11 DESIGN OPERATIONS

Discussions thus far have focused on the analysis of existing networks. All the elements are in place, and it is simply a matter of solving for the current and voltage levels of the configuration. The design process is one where a current and/or voltage may be specified and the elements required to establish the designated levels must be determined. This synthesis process requires a clear understanding of the characteristics of the device, the basic equations for the network, and a firm understanding of the basic laws of circuit analysis, such as Ohm's law, Kirchhoff's voltage law, and so on. In most situations the thinking process is challenged to a higher degree in the design process than in the analysis sequence. The path toward a solution is less defined and in fact may require a number of basic assumptions that do not have to be made when simply analyzing a network.

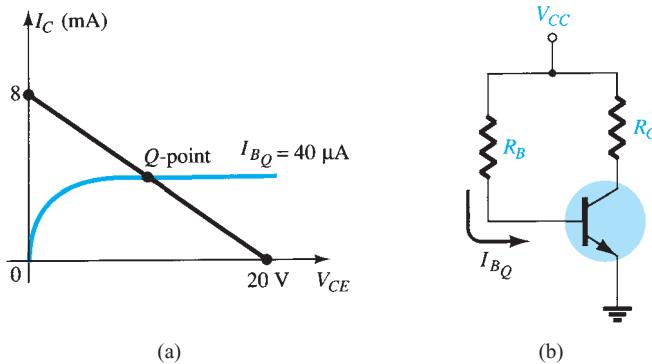
The design sequence is obviously sensitive to the components that are already specified and the elements to be determined. If the transistor and supplies are specified, the design process will simply determine the required resistors for a particular design. Once the theoretical values of the resistors are determined, the nearest standard commercial values are normally chosen and any variations due to not using the exact resistance values are accepted as part of the design. This is certainly a valid approximation considering the tolerances normally associated with resistive elements and the transistor parameters.

If resistive values are to be determined, one of the most powerful equations is simply Ohm's law in the following form:

$$R_{\text{unknown}} = \frac{V_R}{I_R} \quad (4.49)$$

In a particular design the voltage across a resistor can often be determined from specified levels. If additional specifications define the current level, Eq. (4.49) can then be used to calculate the required resistance level. The first few examples will demonstrate how particular elements can be determined from the design specifications. A complete design procedure will then be introduced for two popular configurations.

**EXAMPLE 4.21** Given the device characteristics of Fig. 4.59a, determine  $V_{CC}$ ,  $R_B$ , and  $R_C$  for the fixed-bias configuration of Fig. 4.59b.



**FIG. 4.59**  
Example 4.21.

**Solution:** From the load line

$$V_{CC} = 20 \text{ V}$$

$$I_C = \left. \frac{V_{CC}}{R_C} \right|_{V_{CE}=0 \text{ V}}$$

and

$$R_C = \frac{V_{CC}}{I_C} = \frac{20 \text{ V}}{8 \text{ mA}} = 2.5 \text{ k}\Omega$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

with

$$\begin{aligned} R_B &= \frac{V_{CC} - V_{BE}}{I_B} \\ &= \frac{20 \text{ V} - 0.7 \text{ V}}{40 \mu\text{A}} = \frac{19.3 \text{ V}}{40 \mu\text{A}} \\ &= \mathbf{482.5 \text{ k}\Omega} \end{aligned}$$

Standard resistor values are

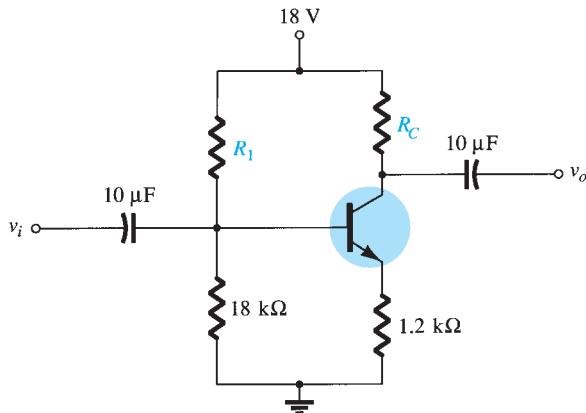
$$\begin{aligned} R_C &= 2.4 \text{ k}\Omega \\ R_B &= 470 \text{ k}\Omega \end{aligned}$$

Using standard resistor values gives

$$I_B = 41.1 \mu\text{A}$$

which is well within 5% of the value specified.

**EXAMPLE 4.22** Given that  $I_{CQ} = 2 \text{ mA}$  and  $V_{CEQ} = 10 \text{ V}$ , determine  $R_1$  and  $R_C$  for the network of Fig. 4.60.



**FIG. 4.60**  
Example 4.22.

**Solution:**

$$\begin{aligned} V_E &= I_E R_E \cong I_C R_E \\ &= (2 \text{ mA})(1.2 \text{ k}\Omega) = 2.4 \text{ V} \\ V_B &= V_{BE} + V_E = 0.7 \text{ V} + 2.4 \text{ V} = 3.1 \text{ V} \\ V_B &= \frac{R_2 V_{CC}}{R_1 + R_2} = 3.1 \text{ V} \\ \text{and } \frac{(18 \text{ k}\Omega)(18 \text{ V})}{R_1 + 18 \text{ k}\Omega} &= 3.1 \text{ V} \end{aligned}$$

$$324 \text{ k}\Omega = 3.1 R_1 + 55.8 \text{ k}\Omega$$

$$3.1 R_1 = 268.2 \text{ k}\Omega$$

$$R_1 = \frac{268.2 \text{ k}\Omega}{3.1} = \mathbf{86.52 \text{ k}\Omega}$$

$$\text{Eq. (4.49): } R_C = \frac{V_{RC}}{I_C} = \frac{V_{CC} - V_C}{I_C}$$

with

$$V_C = V_{CE} + V_E = 10 \text{ V} + 2.4 \text{ V} = 12.4 \text{ V}$$

and

$$\begin{aligned} R_C &= \frac{18 \text{ V} - 12.4 \text{ V}}{2 \text{ mA}} \\ &= \mathbf{2.8 \text{ k}\Omega} \end{aligned}$$

The nearest standard commercial values to  $R_1$  are 82 k $\Omega$  and 91 k $\Omega$ . However, using the series combination of standard values of 82 k $\Omega$  and 4.7 k $\Omega$  = 86.7 k $\Omega$  would result in a value very close to the design level.

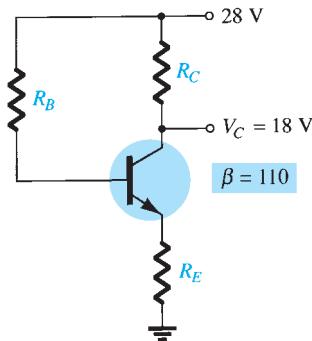


FIG. 4.61

Example 4.23.

**EXAMPLE 4.23** The emitter-bias configuration of Fig. 4.61 has the following specifications:  $I_{CQ} = \frac{1}{2}I_{\text{sat}}$ ,  $I_{\text{sat}} = 8 \text{ mA}$ ,  $V_C = 18 \text{ V}$ , and  $\beta = 110$ . Determine  $R_C$ ,  $R_E$ , and  $R_B$ .

**Solution:**

$$I_{CQ} = \frac{1}{2}I_{\text{sat}} = 4 \text{ mA}$$

$$R_C = \frac{V_{RC}}{I_{CQ}} = \frac{V_{CC} - V_C}{I_{CQ}} = \frac{28 \text{ V} - 18 \text{ V}}{4 \text{ mA}} = 2.5 \text{ k}\Omega$$

$$I_{C_{\text{sat}}} = \frac{V_{CC}}{R_C + R_E}$$

$$\text{and } R_C + R_E = \frac{V_{CC}}{I_{C_{\text{sat}}}} = \frac{28 \text{ V}}{8 \text{ mA}} = 3.5 \text{ k}\Omega$$

$$R_E = 3.5 \text{ k}\Omega - R_C$$

$$= 3.5 \text{ k}\Omega - 2.5 \text{ k}\Omega$$

$$= 1 \text{ k}\Omega$$

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{4 \text{ mA}}{110} = 36.36 \mu\text{A}$$

$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

and

$$R_B + (\beta + 1)R_E = \frac{V_{CC} - V_{BE}}{I_{BQ}}$$

with

$$R_B = \frac{V_{CC} - V_{BE}}{I_{BQ}} - (\beta + 1)R_E$$

$$= \frac{28 \text{ V} - 0.7 \text{ V}}{36.36 \mu\text{A}} - (111)(1 \text{ k}\Omega)$$

$$= \frac{27.3 \text{ V}}{36.36 \mu\text{A}} - 111 \text{ k}\Omega$$

$$= 753.3 \text{ k}\Omega - 111 \text{ k}\Omega$$

$$= 639.8 \text{ k}\Omega$$

For standard values,

$$R_C = 2.4 \text{ k}\Omega$$

$$R_E = 1 \text{ k}\Omega$$

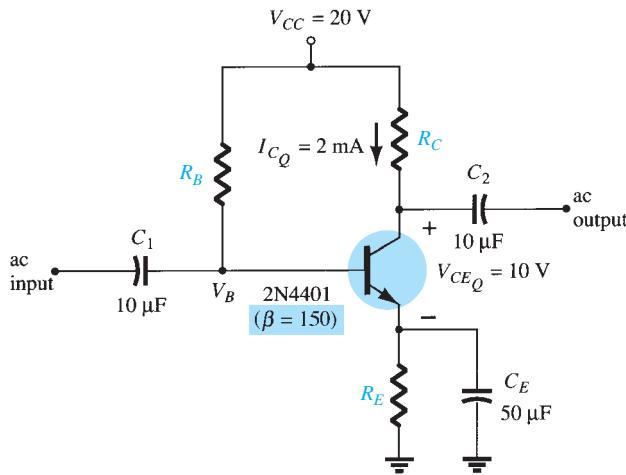
$$R_B = 620 \text{ k}\Omega$$

The discussion to follow will introduce one technique for designing an entire circuit to operate at a specified bias point. Often the manufacturer's specification (spec) sheets provide information on a suggested operating point (or operating region) for a particular transistor. In addition, other system components connected to the given amplifier stage may also define the current swing, voltage swing, value of common supply voltage, and so on, for the design.

In actual practice, many other factors may have to be considered that may affect the selection of the desired operating point. For the moment we concentrate on determining the component values to obtain a specified operating point. The discussion will be limited to the emitter-bias and voltage-divider bias configurations, although the same procedure can be applied to a variety of other transistor circuits.

Consider first the design of the dc bias components of an amplifier circuit having emitter-resistor bias stabilization as shown in Fig. 4.62. The supply voltage and operating point were selected from the manufacturer's information on the transistor used in the amplifier.

The selection of collector and emitter resistors cannot proceed directly from the information just specified. The equation that relates the voltages around the collector-emitter loop has two unknown quantities present—the resistors  $R_C$  and  $R_E$ . At this point some engineering judgment must be made, such as the level of the emitter voltage compared to the applied supply voltage. Recall that the need for including a resistor from emitter to ground was to provide a means of dc bias stabilization so that the change of collector current due to leakage currents in the transistor and the transistor beta would not cause a large shift in the operating point. The emitter resistor cannot be unreasonably large because the voltage across it limits the range of swing of the voltage from collector to emitter (to be noted when the ac response is discussed). The examples examined in this chapter reveal that the voltage from emitter to ground is typically around one-fourth to one-tenth of the supply voltage. Selecting the conservative case of one-tenth will permit calculating the emitter resistor  $R_E$  and the resistor  $R_C$  in a manner similar to the examples just completed. In the next example we perform a complete design of the network of Fig. 4.62 using the criteria just introduced for the emitter voltage.



**FIG. 4.62**  
Emitter-stabilized bias circuit for design consideration.

**EXAMPLE 4.24** Determine the resistor values for the network of Fig. 4.62 for the indicated operating point and supply voltage.

**Solution:**

$$V_E = \frac{1}{10}V_{CC} = \frac{1}{10}(20 \text{ V}) = 2 \text{ V}$$

$$R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_C} = \frac{2 \text{ V}}{2 \text{ mA}} = 1 \text{ k}\Omega$$

$$R_C = \frac{V_{RC}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20 \text{ V} - 10 \text{ V} - 2 \text{ V}}{2 \text{ mA}} = \frac{8 \text{ V}}{2 \text{ mA}} = 4 \text{ k}\Omega$$

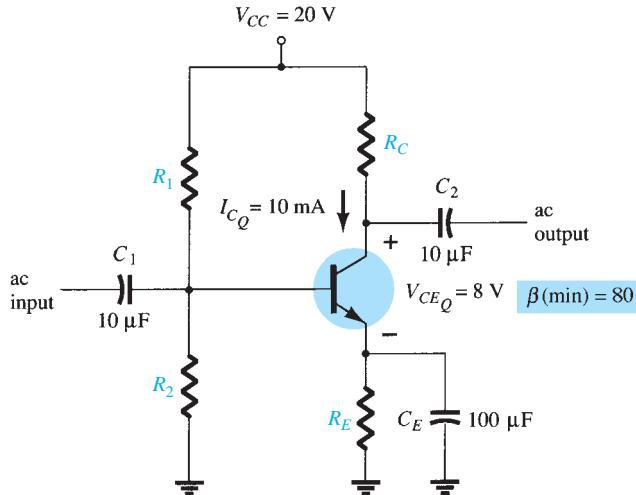
$$I_B = \frac{I_C}{\beta} = \frac{2 \text{ mA}}{150} = 13.33 \mu\text{A}$$

$$R_B = \frac{V_{RB}}{I_B} = \frac{V_{CC} - V_{BE} - V_E}{I_B} = \frac{20 \text{ V} - 0.7 \text{ V} - 2 \text{ V}}{13.33 \mu\text{A}} \cong 1.3 \text{ M}\Omega$$

## Design of a Current-Gain-Stabilized (Beta-Independent) Circuit

The circuit of Fig. 4.63 provides stabilization both for leakage and current gain (beta) changes. The four resistor values shown must be obtained for the specified operating point. Engineering judgment in selecting a value of emitter voltage  $V_E$ , as in the previous design consideration, leads to a direct, straightforward solution for all the resistor values. The design steps are all demonstrated in the next example.

**EXAMPLE 4.25** Determine the levels of  $R_C$ ,  $R_E$ ,  $R_1$ , and  $R_2$  for the network of Fig. 4.63 for the operating point indicated.



**FIG. 4.63**  
Current-gain-stabilized circuit for design considerations.

**Solution:**

$$V_E = \frac{1}{10}V_{CC} = \frac{1}{10}(20 \text{ V}) = 2 \text{ V}$$

$$R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_C} = \frac{2 \text{ V}}{10 \text{ mA}} = 200 \Omega$$

$$R_C = \frac{V_{RC}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20 \text{ V} - 8 \text{ V} - 2 \text{ V}}{10 \text{ mA}} = \frac{10 \text{ V}}{10 \text{ mA}} = 1 \text{ k}\Omega$$

$$V_B = V_{BE} + V_E = 0.7 \text{ V} + 2 \text{ V} = 2.7 \text{ V}$$

The equations for the calculation of the base resistors  $R_1$  and  $R_2$  will require a little thought. Using the value of base voltage calculated above and the value of the supply voltage will provide one equation—but there are two unknowns,  $R_1$  and  $R_2$ . An additional equation can be obtained from an understanding of the operation of these two resistors in providing the necessary base voltage. For the circuit to operate efficiently, it is assumed that the current through  $R_1$  and  $R_2$  should be approximately equal to and much larger than the base current (at least 10:1). This fact and the voltage-divider equation for the base voltage provide the two relationships necessary to determine the base resistors. That is,

$$R_2 \leq \frac{1}{10}\beta R_E$$

and

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC}$$

Substitution yields

$$R_2 \leq \frac{1}{10}(80)(0.2 \text{ k}\Omega) \\ = 1.6 \text{ k}\Omega$$

$$V_B = 2.7 \text{ V} = \frac{(1.6 \text{ k}\Omega)(20 \text{ V})}{R_1 + 1.6 \text{ k}\Omega}$$

and

$$2.7R_1 + 4.32 \text{ k}\Omega = 32 \text{ k}\Omega$$

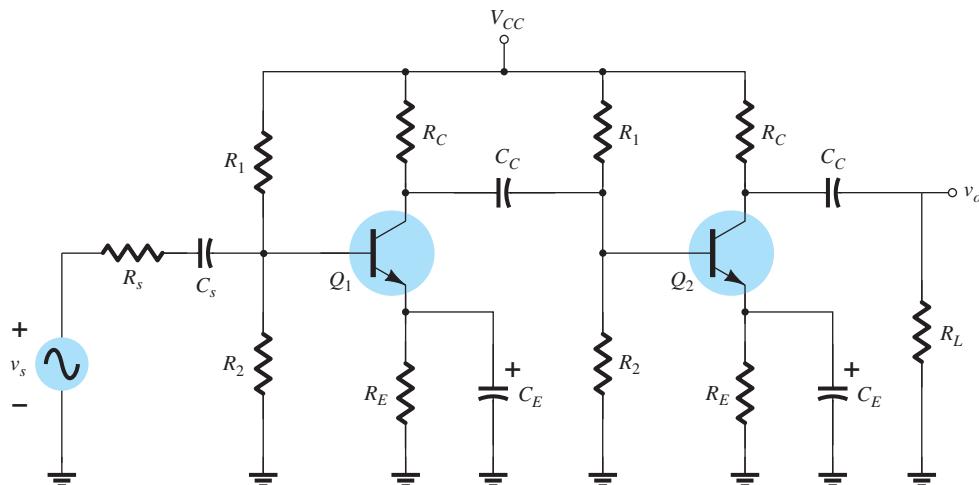
$$2.7R_1 = 27.68 \text{ k}\Omega$$

$$R_1 = \mathbf{10.25 \text{ k}\Omega} \quad (\text{use } 10 \text{ k}\Omega)$$

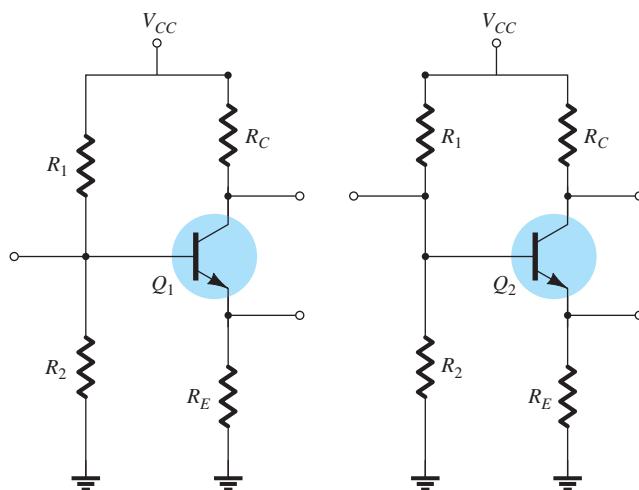
## 4.12 MULTIPLE BJT NETWORKS

The BJT networks introduced thus far have only been single-stage configurations. This section will cover some of the most popular networks using multiple transistors. It will demonstrate how the methods introduced thus far in this chapter can be applied to networks with any number of components.

The **R–C coupling** of Fig. 4.64 is probably the most common. The collector output of one stage is fed directly into the base of the next stage using a coupling capacitor  $C_C$ . The capacitor is chosen to ensure that it will block dc between the stages and act like a short circuit to any ac signal. The network of Fig. 4.64 has two voltage-divider stages, but the same coupling can be used between any combination of networks such as the fixed-bias or emitter-follower configurations. Substituting an open-circuit equivalent for  $C_C$  and the other capacitors of the network will result in the two bias arrangements shown in Fig. 4.65. The methods of analysis introduced in this chapter can then be applied to each stage separately since one stage will not affect the other. Of course, the 20 V dc supply must be applied to each isolated component.

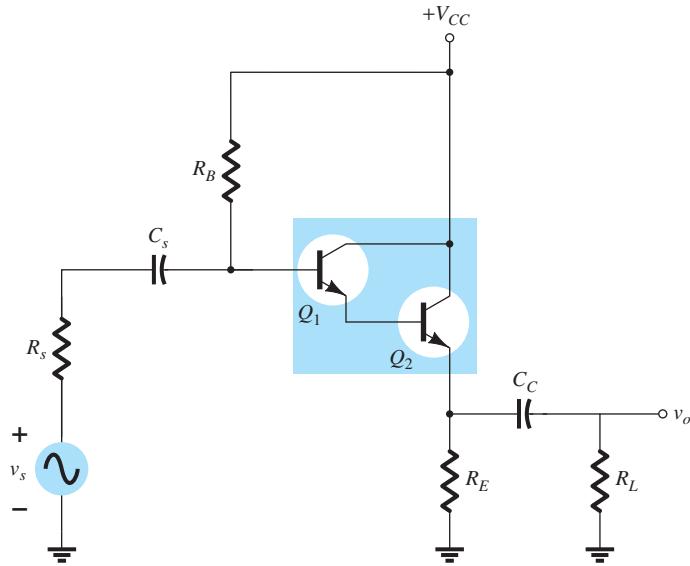


**FIG. 4.64**  
R–C coupled BJT amplifiers.

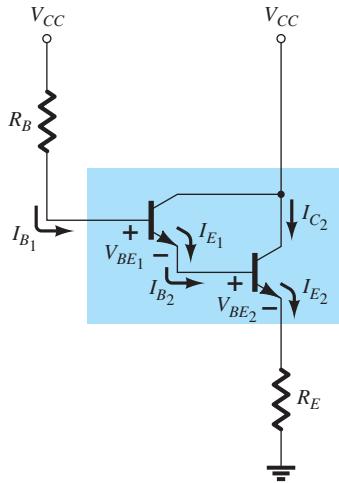


**FIG. 4.65**  
DC equivalent of Fig. 4.64.

The **Darlington** configuration of Fig. 4.66 feeds the output of one stage directly into the input of the succeeding stage. Since the output of Fig. 4.66 is taken directly off the emitter terminal, you will find in the next chapter that the ac gain is very close to 1 but the input impedance is very high, making it attractive for use in amplifiers operating off sources that have a relatively high internal resistance. If a load resistor were added to the collector leg and the output taken off the collector terminal, the configuration would provide a very high gain.



**FIG. 4.66**  
Darlington amplifier.



**FIG. 4.67**  
DC equivalent of Fig. 4.66.

For the dc analysis of Fig. 4.67 assuming a beta  $\beta_1$  for the first transistor and  $\beta_2$  for the second, the base current for the second transistor is

$$I_{B_2} = I_{E_1} = (\beta_1 + 1)I_{B_1}$$

and the emitter current for the second transistor is

$$I_{E_2} = (\beta_2 + 1)I_{B_2} = (\beta_2 + 1)(\beta_1 + 1)I_{B_1}$$

Assuming  $\beta \gg 1$  for each transistor, we find the net beta for the configuration is

$$\beta_D = \beta_1\beta_2 \quad (4.50)$$

which compares directly with a single-stage amplifier having a gain of  $\beta_D$ .

Applying an analysis similar to that of Section 4.4 will result in the following equation for the base current:

$$I_{B_1} = \frac{V_{CC} - V_{BE_1} - V_{BE_2}}{R_B + (\beta_D + 1)R_E}$$

Defining

$$V_{BE_D} = V_{BE_1} + V_{BE_2} \quad (4.51)$$

we have

$$I_{B_1} = \frac{V_{CC} - V_{BE_D}}{R_B + (\beta_D + 1)R_E} \quad (4.52)$$

The currents

$$I_{C_2} \approx I_{E_2} = \beta_D I_{B_1} \quad (4.53)$$

and the dc voltage at the emitter terminal is

$$V_{E_2} = I_{E_2} R_E \quad (4.54)$$

The collector voltage for this configuration is obviously equal to that of the source V.

$$V_{C_2} = V_{CC} \quad (4.55)$$

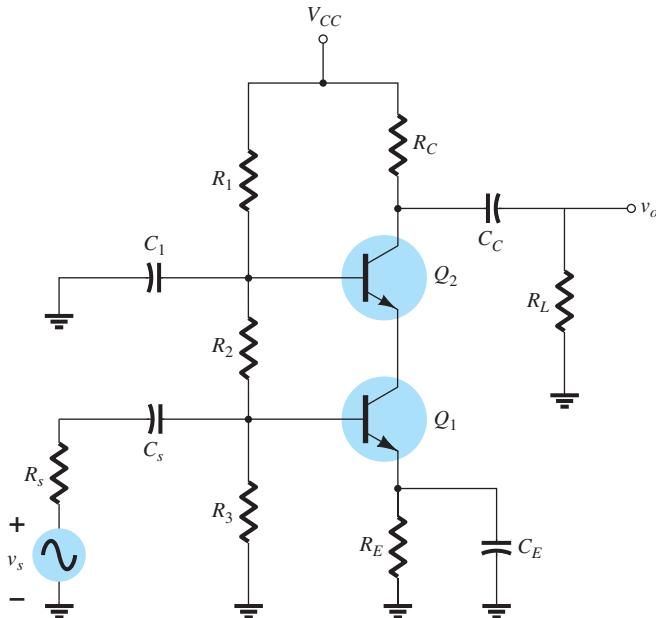
and the voltage across the output of the transistor is

$$V_{CE_2} = V_{CC} - V_{E_2}$$

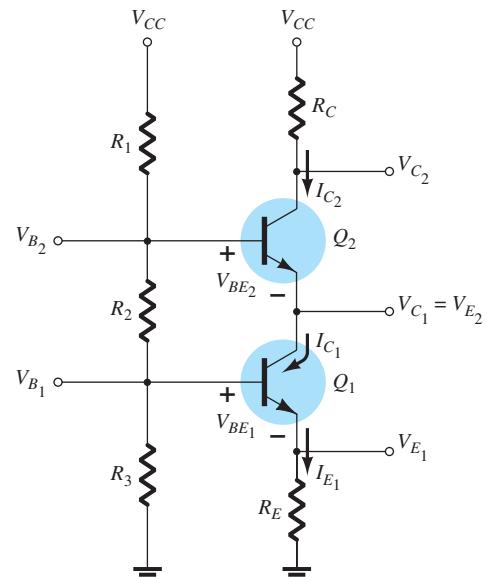
and

$$V_{CE_2} = V_{CC} - V_{E_2} \quad (4.56)$$

The **Cascode** configuration of Fig. 4.68 ties the collector of one transistor to the emitter of the other. In essence it is a voltage-divider network with a common-base configuration at the collector. The result is a network with a high gain and a reduced Miller capacitance—a topic to be examined in Section 9.9.



**FIG. 4.68**  
Cascode amplifier.



**FIG. 4.69**  
DC equivalent of Fig. 4.68.

The dc analysis is initiated by assuming the current through the bias resistors  $R_1$ ,  $R_2$ , and  $R_3$  of Fig. 4.69 is much larger than the base current of each transistor. That is,

$$I_{R_1} \cong I_{R_2} \cong I_{R_3} \gg I_{B_1} \text{ or } I_{B_2}$$

The result is that the voltage at the base of the transistor  $Q_1$  is simply determined by an application of the voltage-divider rule:

$$V_{B_1} = \frac{R_3}{R_1 + R_2 + R_3} V_{CC} \quad (4.57)$$

The voltage at the base of the transistor  $Q_2$  is found in the same manner:

$$V_{B_2} = \frac{(R_2 + R_3)}{R_1 + R_2 + R_3} V_{CC} \quad (4.58)$$

The emitter voltages are then determined by

$$V_{E_1} = V_{B_1} - V_{BE_1} \quad (4.59)$$

and

$$V_{E_2} = V_{B_2} - V_{BE_2} \quad (4.60)$$

with the emitter and collector currents determined by:

$$I_{C_2} \cong I_{E_2} \cong I_{C_1} \cong I_{E_1} = \frac{V_{B_1} - V_{BE_1}}{R_{E_1} + R_{E_2}} \quad (4.61)$$

The collector voltage  $V_{C_1}$ :

$$V_{C_1} = V_{B_2} - V_{BE_2} \quad (4.62)$$

and the collector voltage  $V_{C_2}$ :

$$V_{C_2} = V_{CC} - I_{C_2}R_C \quad (4.63)$$

The current through the biasing resistors is

$$I_{R_1} \cong I_{R_2} \cong I_{R_3} = \frac{V_{CC}}{R_1 + R_2 + R_3} \quad (4.64)$$

and each base current is determined by

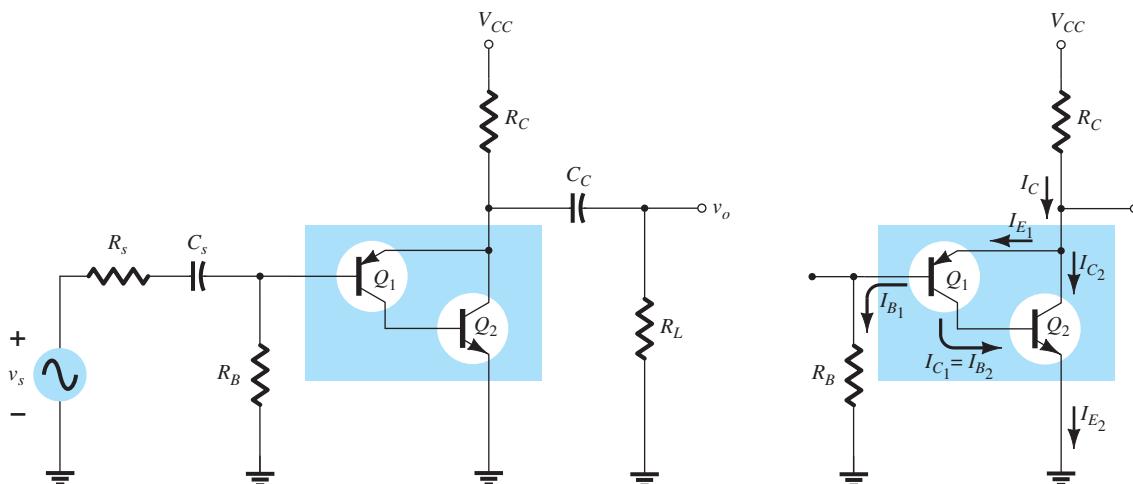
$$I_{B_1} = \frac{I_{C_1}}{\beta_1} \quad (4.65)$$

with

$$I_{B_2} = \frac{I_{C_2}}{\beta_2} \quad (4.66)$$

The next multistage configuration to be introduced is the **Feedback Pair** of Fig. 4.70, which employs both an *npn* and *pnp* transistor. The result is a configuration that provides high gain with increased stability.

The dc version with all the currents labeled appears in Fig. 4.71.



**FIG. 4.70**  
Feedback Pair amplifier.

**FIG. 4.71**  
DC equivalent of Fig. 4.70.

The base current

$$I_{B_2} = I_{C_1} = \beta_1 I_{B_1}$$

and

$$I_{C_2} = \beta_2 I_{B_2}$$

so that

$$I_{C_2} \cong I_{E_2} = \beta_1 \beta_2 I_{B_1} \quad (4.67)$$

The collector current

$$\begin{aligned} I_C &= I_{E_1} + I_{E_2} \\ &\cong \beta_1 I_{B_1} + \beta_1 \beta_2 I_{B_1} \\ &= \beta_1 (1 + \beta_2) I_{B_1} \end{aligned}$$

so that

$$I_C \cong \beta_1 \beta_2 I_{B_1} \quad (4.68)$$

Applying Kirchhoff's voltage law down from the source to ground will result in

$$V_{CC} - I_C R_C - V_{EB_1} - I_{B_1} R_B = 0$$

or

$$V_{CC} - V_{EB_1} - \beta_1 \beta_2 I_{B_1} R_C - I_{B_1} R_B = 0$$

and

$$I_{B_1} = \frac{V_{CC} - V_{EB_1}}{R_B + \beta_1 \beta_2 R_C} \quad (4.69)$$

The base voltage  $V_{B_1}$  is

$$V_{B_1} = I_{B_1} R_B \quad (4.70)$$

and

$$V_{B_2} = V_{BE_2} \quad (4.71)$$

The collector voltage  $V_{C_2} = V_{E_1}$  is

$$V_{C_2} = V_{CC} - I_C R_C \quad (4.72)$$

and

$$V_{C_1} = V_{BE_2} \quad (4.73)$$

In this case

$$V_{CE_2} = V_{C_2} \quad (4.74)$$

and

$$V_{EC_1} = V_{E_1} - V_{C_1}$$

so that

$$V_{EC_1} = V_{C_2} - V_{BE_2} \quad (4.75)$$

The last multistage configuration to be introduced is the **Direct Coupled** amplifier such as appearing in Example 4.26. Note the absence of a coupling capacitor to isolate the dc levels of each stage. The dc levels in one stage will directly affect the dc levels in succeeding stages. The benefit is that the coupling capacitor typically limits the low-frequency response of the amplifier. Without coupling capacitors, the amplifier can amplify signals of very low frequency—in fact down to dc. The disadvantage is that any variation in dc levels due to a variety of reasons in one stage can affect the dc levels in the succeeding stages of the amplifier.

**EXAMPLE 4.26** Determine the dc levels for the currents and voltages of the direct-coupled amplifier of Fig. 4.72. Note that it is a voltage-divider bias configuration followed by a common-collector configuration; one that is excellent in cases wherein the input impedance of the next stage is quite low. The common-collector amplifier is acting like a **buffer** between stages.

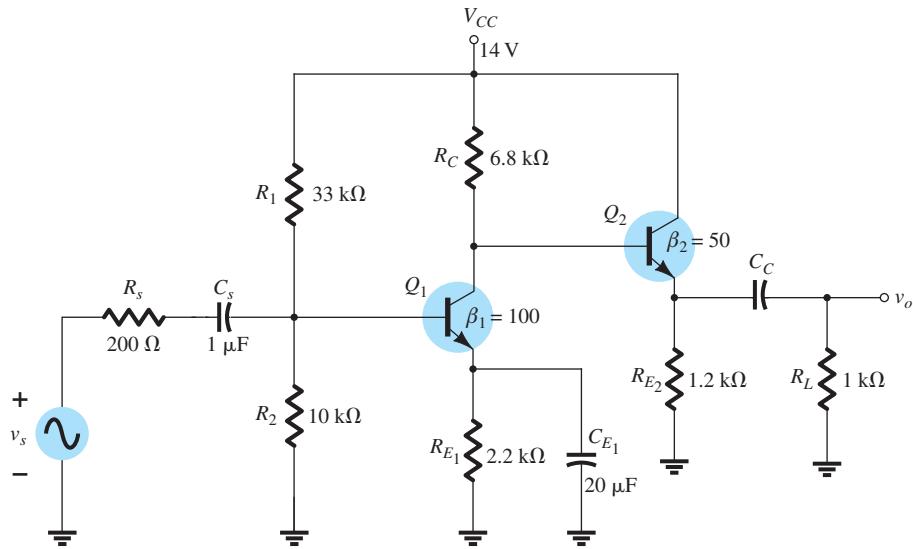


FIG. 4.72

Direct-coupled amplifier.

**Solution:** The dc equivalent of Fig. 4.72 appears as Fig. 4.73. Note that the load and source are no longer part of the picture. For the voltage-divider configuration, the following equations for the base current were developed in Section 4.5.

$$I_{B_1} = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_{E_1}}$$

with

$$R_{Th} = R_1 \parallel R_2$$

and

$$E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

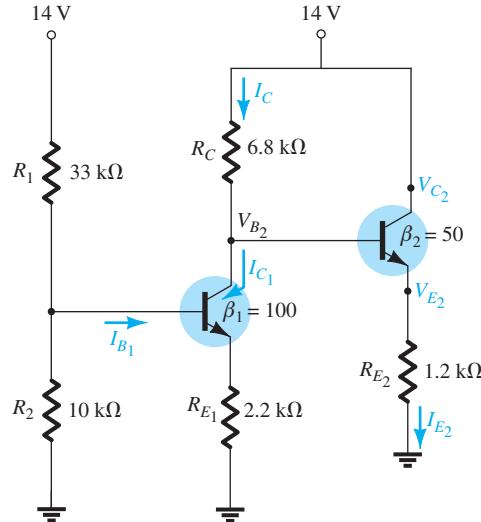


FIG. 4.73

DC equivalent of Fig. 4.72.

In this case,

$$R_{Th} = 33 \text{ k}\Omega \parallel 10 \text{ k}\Omega = 7.67 \text{ k}\Omega$$

and

$$E_{Th} = \frac{10 \text{ k}\Omega(14 \text{ V})}{10 \text{ k}\Omega + 33 \text{ k}\Omega} = 3.26 \text{ V}$$

so that

$$\begin{aligned} I_{B_1} &= \frac{3.26 \text{ V} - 0.7 \text{ V}}{7.67 \text{ k}\Omega + (100 + 1) 2.2 \text{ k}\Omega} \\ &= \frac{2.56 \text{ V}}{229.2 \text{ k}\Omega} \\ &= 11.17 \mu\text{A} \end{aligned}$$

with

$$\begin{aligned} I_{C_1} &= \beta I_{B_1} \\ &= 100 (11.17 \mu\text{A}) \\ &= 1.12 \text{ mA} \end{aligned}$$

In Fig. 4.73 we find that

$$V_{B_2} = V_{CC} - I_C R_C \quad (4.76)$$

$$\begin{aligned} &= 14 \text{ V} - (1.12 \text{ mA})(6.8 \text{ k}\Omega) \\ &= 14 \text{ V} - 7.62 \text{ V} \\ &= 6.38 \text{ V} \end{aligned}$$

and

$$\begin{aligned} V_{E_2} &= V_{B_2} - V_{BE_2} \\ &= 6.38 \text{ V} - 0.7 \text{ V} \\ &= 5.68 \text{ V} \end{aligned}$$

resulting in

$$\begin{aligned} I_{E_2} &= \frac{V_{E_2}}{R_{E_2}} \quad (4.77) \\ &= \frac{5.68 \text{ V}}{1.2 \text{ k}\Omega} \\ &= 4.73 \text{ mA} \end{aligned}$$

Obviously,

$$V_{C_2} = V_{CC} \quad (4.78)$$

$$= 14 \text{ V}$$

and

$$V_{CE_2} = V_{C_2} - V_{E_2}$$

$$\begin{aligned} V_{CE_2} &= V_{CC} - V_{E_2} \quad (4.79) \\ &= 14 \text{ V} - 5.68 \text{ V} \\ &= 8.32 \text{ V} \end{aligned}$$

## 4.13 CURRENT MIRRORS

The **current mirror** is a dc network in which the current through a load is controlled by a current at another point in the network. That is, if the controlling current is raised or lowered the current through the load will change to the same level. The discussion to follow will demonstrate that the effectiveness of the design is dependent on the fact that the two transistors employed have identical characteristics. The basic configuration appears in Fig. 4.74. Note that the two transistors are back to back and the collector of one is connected to the base of the two transistors.

Assume identical transistors will result in  $V_{BE_1} = V_{BE_2}$  and  $I_{B_1} = I_{B_2}$  as defined by the base-to-emitter characteristics of Fig. 4.75. Raise the base to emitter voltage, and the current of each will rise to the same value.

Since the base to emitter voltages of the two transistors in Fig. 4.74 are in parallel, they must have the same voltage. The result is that  $I_{B_1} = I_{B_2}$  at every set base to emitter voltage.

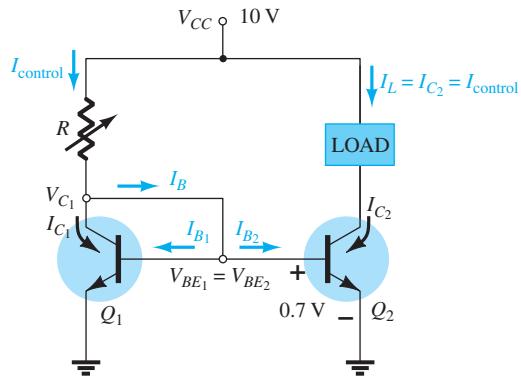
It is clear from Fig. 4.74 that  $I_B = I_{B_1} + I_{B_2}$

and if

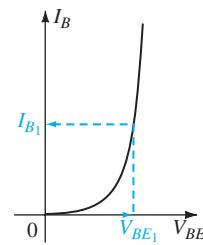
$$I_{B_1} = I_{B_2}$$

then

$$I_B = I_{B_1} + I_{B_1} = 2I_{B_1}$$



**FIG. 4.74**  
Current mirror using back-to-back BJTs.



**FIG. 4.75**  
Base characteristics  
for transistor  $Q_1$   
(and  $Q_2$ ).

In addition,

$$I_{\text{control}} = I_{C_1} + I_B = I_{C_1} + 2I_{B_1}$$

but

$$I_{C_1} = \beta_1 I_{B_1}$$

so

$$I_{\text{control}} = \beta_1 I_{B_1} + 2I_{B_1} = (\beta_1 + 2)I_{B_1}$$

and since  $\beta_1$  is typically  $\gg 2$ ,  $I_{\text{control}} \approx \beta_1 I_{B_1}$

or

$$I_{B_1} = \frac{I_{\text{control}}}{\beta_1} \quad (4.80)$$

If the control current is raised, the resulting  $I_{B_1}$  will increase as determined by Eq. 4.80. If  $I_{B_1}$  increases, the voltage  $V_{BE_1}$  must increase as dictated by the response curve of Fig. 4.75. If  $V_{BE_1}$  increases, then  $V_{BE_2}$  must increase by the same amount and  $I_{B_2}$  will also increase. The result is that  $I_L = I_{C_2} = \beta_1 I_{B_2}$  will also increase to the level established by the control current.

Referring to Fig. 4.74 we find the control current is determined by

$$I_{\text{control}} = \frac{V_{CC} - V_{BE}}{R} \quad (4.81)$$

revealing that for a fixed  $V_{CC}$ , the resistor  $R$  can be used to set the control current.

The network also has a measure of built-in control that will try to ensure that any variation in load current will be corrected by the configuration itself. For instance, if  $I_L$  should try to increase for whatever reason, the base current of  $Q_2$  will also increase due to the relationship  $I_{B_2} = I_{C_2}/\beta_2 = I_L/\beta_2$ . Returning to Fig. 4.101, we find that an increase in  $I_{B_2}$  will cause voltage  $V_{BE_2}$  to increase also. Because the base of  $Q_2$  is connected directly to the collector of  $Q_1$ , the voltage  $V_{CE_1}$  will increase also. This action causes the voltage across the control resistor  $R$  to decrease, causing  $I_R$  to drop. But if  $I_R$  drops, the base current  $I_B$  will drop, causing both  $I_{B_1}$  and  $I_{B_2}$  to drop also. A drop in  $I_{B_2}$  will cause the collector current and therefore the load current to drop also. The result, therefore, is a sensitivity to unwanted changes that the network will make every effort to correct.

The entire sequence of events just described can be presented on a single line as shown below. Note that at one end the load current is trying to increase, and at the end of the sequence the load current is forced to return to its original level.

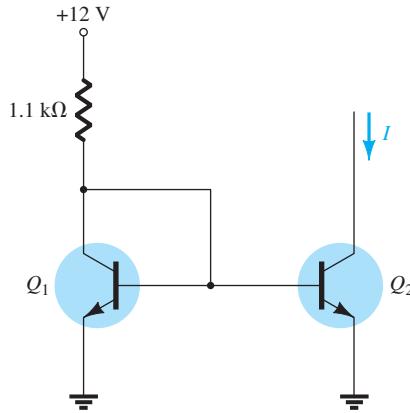
$$I_L \uparrow I_{C_2} \uparrow I_{B_2} \uparrow V_{BE_2} \uparrow V_{CE_1} \downarrow, I_R \downarrow, I_B \downarrow, I_{B_2} \downarrow I_{C_2} \downarrow I_L \downarrow$$

Note

**EXAMPLE 4.27** Calculate the mirrored current  $I$  in the circuit of Fig. 4.76.

**Solution:** Eq. (4.75):

$$I = I_{\text{control}} = \frac{V_{CC} - V_{BE}}{R} = \frac{12 \text{ V} - 0.7 \text{ V}}{1.1 \text{ k}\Omega} = 10.27 \text{ mA}$$



**FIG. 4.76**  
Current mirror circuit for Example 4.27.

**EXAMPLE 4.28** Calculate the current  $I$  through each of the transistor  $Q_2$  and  $Q_3$  in the circuit of Fig. 4.77.

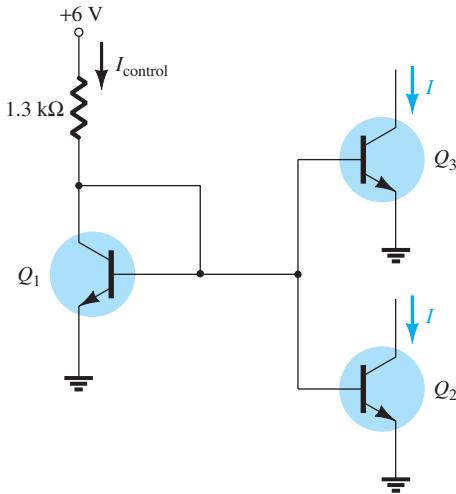
**Solution:** Since  $V_{BE_1} = V_{BE_2} = V_{BE_3}$  then  $I_{B_1} = I_{B_2} = I_{B_3}$

$$\text{Substituting } I_{B_1} = \frac{I_{\text{control}}}{\beta} \text{ and } I_{B_2} = \frac{I}{\beta} \text{ with } I_{B_3} = \frac{I}{\beta}$$

$$\text{we have } \frac{I_{\text{control}}}{\beta} = \frac{I}{\beta} = \frac{I}{\beta}$$

so  $I$  must equal  $I_{\text{control}}$

$$\text{and } I_{\text{control}} = \frac{V_{CC} - V_{BE}}{R} = \frac{6 \text{ V} - 0.7 \text{ V}}{1.3 \text{ k}\Omega} = 4.08 \text{ mA}$$



**FIG. 4.77**  
Current mirror circuit for Example 4.28.

Figure 4.78 shows another form of current mirror to provide higher output impedance than that of Fig. 4.74. The control current through  $R$  is

$$I_{\text{control}} = \frac{V_{CC} - 2V_{BE}}{R} \approx I_C + \frac{I_C}{\beta} = \frac{\beta + 1}{\beta} I_C \approx I_C$$

Assuming that  $Q_1$  and  $Q_2$  are well matched, we find that the output current  $I$  is held constant at

$$I \approx I_C = I_{\text{control}}$$

Again we see that the output current  $I$  is a mirrored value of the current set by the fixed current through  $R$ .

Figure 4.79 shows still another form of current mirror. The junction field effect transistor (see Chapter 6) provides a constant current set at the value of  $I_{DSS}$ . This current is mirrored, resulting in a current through  $Q_2$  of the same value:

$$I = I_{DSS}$$

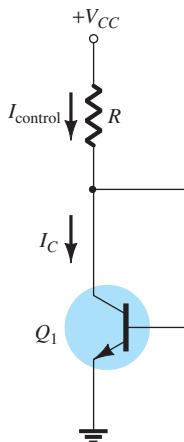


FIG. 4.78

Current mirror circuit with higher output impedance.

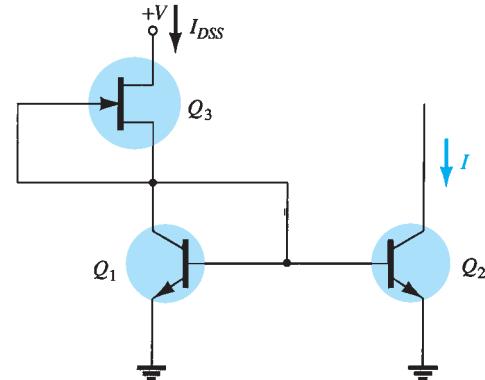


FIG. 4.79

Current mirror connection.

## 4.14 CURRENT SOURCE CIRCUITS

The concept of a power supply provides the starting point in our consideration of current source circuits. A practical voltage source (Fig. 4.80a) is a voltage supply in series with a resistance. An ideal voltage source has  $R = 0$ , whereas a practical source includes some small resistance. A practical current source (Fig. 4.80b) is a current supply in parallel with a resistance. An ideal current source has  $R = \infty\Omega$ , whereas a practical current source includes some very large resistance.

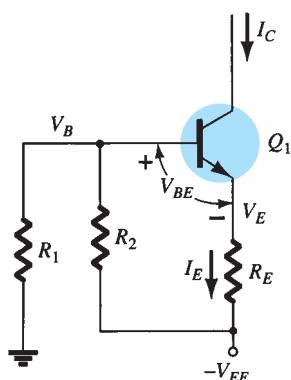
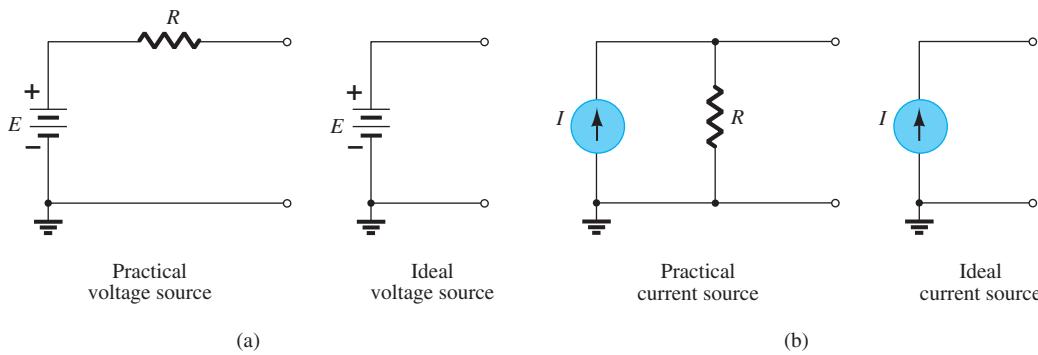


FIG. 4.81

Discrete constant-current source.

An ideal current source provides a constant current regardless of the load connected to it. There are many uses in electronics for a circuit providing a constant current at a very high impedance. Constant-current circuits can be built using bipolar devices, FET devices, and a combination of these components. There are circuits used in discrete form and others more suitable for operation in integrated circuits.

### Bipolar Transistor Constant-Current Source

Bipolar transistors can be connected in a circuit that acts as a constant-current source in a number of ways. Figure 4.81 shows a circuit using a few resistors and an *n-p-n* transistor for

operation as a constant-current circuit. The current through  $I_E$  can be determined as follows. Assuming that the base input impedance is much larger than  $R_1$  or  $R_2$ , we have

$$V_B = \frac{R_1}{R_1 + R_2} (-V_{EE})$$

and

$$V_E = V_B - 0.7 \text{ V}$$

with

$$I_E = \frac{V_E - (-V_{EE})}{R_E} \approx I_C \quad (4.82)$$

where  $I_C$  is the constant current provided by the circuit of Fig. 4.81.

**EXAMPLE 4.29** Calculate the constant current  $I$  in the circuit of Fig. 4.82.

**Solution:**

$$V_B = \frac{R_1}{R_1 + R_2} (-V_{EE}) = \frac{5.1 \text{ k}\Omega}{5.1 \text{ k}\Omega + 5.1 \text{ k}\Omega} (-20 \text{ V}) = -10 \text{ V}$$

$$V_E = V_B - 0.7 \text{ V} = 10 \text{ V} - 0.7 \text{ V} = -10.7 \text{ V}$$

$$\begin{aligned} I = I_E &= \frac{V_E - (-V_{EE})}{R_E} = \frac{-10.7 \text{ V} - (-20 \text{ V})}{2 \text{ k}\Omega} \\ &= \frac{9.3 \text{ V}}{2 \text{ k}\Omega} = 4.65 \text{ mA} \end{aligned}$$

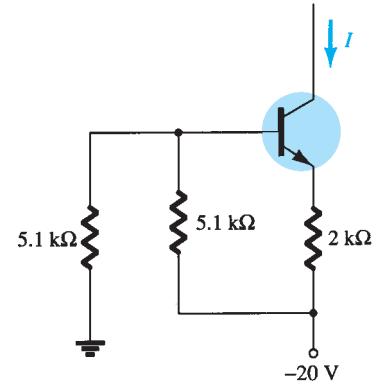


FIG. 4.82

Constant-current source for Example 4.29.

### Transistor/Zener Constant-Current Source

Replacing resistor  $R_2$  with a Zener diode, as shown in Fig. 4.83, provides an improved constant-current source over that of Fig. 4.81. The Zener diode results in a constant current calculated using the base-emitter KVL (Kirchhoff voltage loop) equation. The value of  $I$  can be calculated using

$$I \approx I_E = \frac{V_Z - V_{BE}}{R_E} \quad (4.83)$$

A major point to consider is that the constant current depends on the Zener diode voltage, which remains quite constant, and the emitter resistor  $R_E$ . The voltage supply  $V_{EE}$  has no effect on the value of  $I$ .

**EXAMPLE 4.30** Calculate the constant current  $I$  in the circuit of Fig. 4.84.

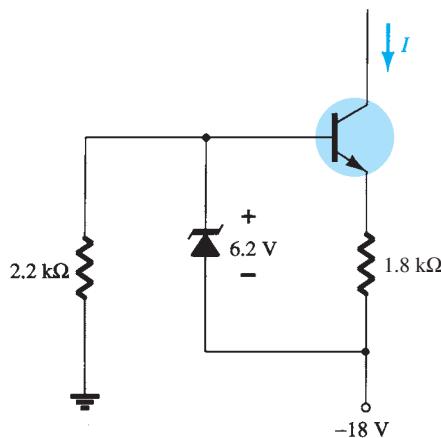


FIG. 4.84

Constant-current circuit for Example 4.30.

**Solution:**

$$\text{Eq. (4.83): } I = \frac{V_Z - V_{BE}}{R_E} = \frac{6.2 \text{ V} - 0.7 \text{ V}}{1.8 \text{ k}\Omega} = 3.06 \text{ mA} \approx 3 \text{ mA}$$

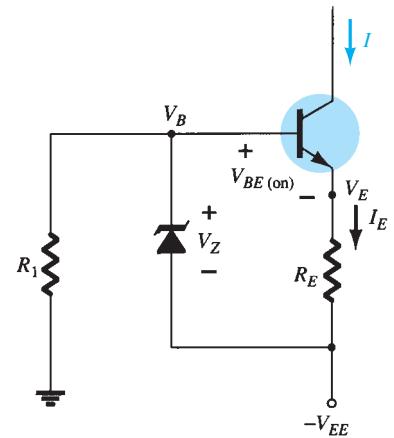


FIG. 4.83

Constant-current circuit using Zener diode.

## 4.15 pnp TRANSISTORS

The analysis thus far has been limited totally to *npn* transistors to ensure that the initial analysis of the basic configurations was as clear as possible and uncomplicated by switching between types of transistors. Fortunately, the analysis of *pnp* transistors follows the same pattern established for *npn* transistors. The level of  $I_B$  is first determined, followed by the application of the appropriate transistor relationships to determine the list of unknown quantities. In fact, the only difference between the resulting equations for a network in which an *npn* transistor has been replaced by a *pnp* transistor is the sign associated with particular quantities.

As noted in Fig. 4.85, the double-subscript notation continues as normally defined. The current directions, however, have been reversed to reflect the actual conduction directions. Using the defined polarities of Fig. 4.85, both  $V_{BE}$  and  $V_{CE}$  will be negative quantities.

Applying Kirchhoff's voltage law to the base-emitter loop results in the following equation for the network of Fig. 4.85:

$$-I_E R_E + V_{BE} - I_B R_B + V_{CC} = 0$$

Substituting  $I_E = (\beta + 1)I_B$  and solving for  $I_B$  yields

$$I_B = \frac{V_{CC} + V_{BE}}{R_B + (\beta + 1)R_E} \quad (4.84)$$

The resulting equation is the same as Eq. (4.17) except for the sign for  $V_{BE}$ . However, in this case  $V_{BE} = -0.7$  V and the substitution of values results in the same sign for each term of Eq. (4.84) as Eq. (4.17). Keep in mind that the direction of  $I_B$  is now defined opposite of that for a *pnp* transistor as shown in Fig. 4.85.

For  $V_{CE}$  Kirchhoff's voltage law is applied to the collector-emitter loop, resulting in the following equation:

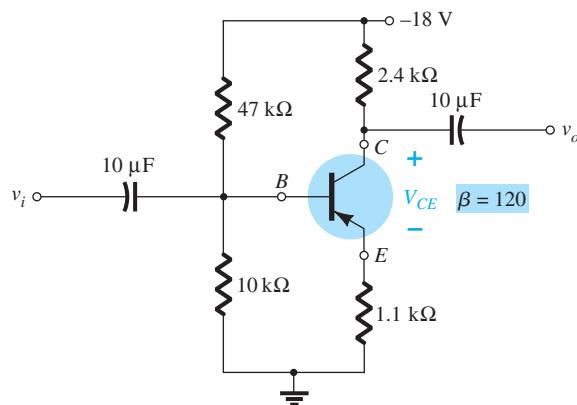
$$-I_E R_E + V_{CE} - I_C R_C + V_{CC} = 0$$

Substituting  $I_E \equiv I_C$  gives

$$V_{CE} = -V_{CC} + I_C(R_C + R_E) \quad (4.85)$$

The resulting equation has the same format as Eq. (4.19), but the sign in front of each term on the right of the equal sign has changed. Because  $V_{CC}$  will be larger than the magnitude of the succeeding term, the voltage  $V_{CE}$  will have a negative sign, as noted in an earlier paragraph.

**EXAMPLE 4.31** Determine  $V_{CE}$  for the voltage-divider bias configuration of Fig. 4.86.



**FIG. 4.86**  
*pnp transistor in a voltage-divider bias configuration.*

$$\beta R_E \geq 10R_2$$

results in

$$(120)(1.1 \text{ k}\Omega) \geq 10(10 \text{ k}\Omega)$$

$$132 \text{ k}\Omega \geq 100 \text{ k}\Omega \quad (\text{satisfied})$$

Solving for  $V_B$ , we have

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(10 \text{ k}\Omega)(-18 \text{ V})}{47 \text{ k}\Omega + 10 \text{ k}\Omega} = -3.16 \text{ V}$$

Note the similarity in format of the equation with the resulting negative voltage for  $V_B$ .

Applying Kirchhoff's voltage law around the base-emitter loop yields

$$+V_B - V_{BE} - V_E = 0$$

and

$$V_E = V_B - V_{BE}$$

Substituting values, we obtain

$$V_E = -3.16 \text{ V} - (-0.7 \text{ V})$$

$$= -3.16 \text{ V} + 0.7 \text{ V}$$

$$= -2.46 \text{ V}$$

Note in the equation above that the standard single- and double-subscript notation is employed. For an *n*p*n* transistor the equation  $V_E = V_B - V_{BE}$  would be exactly the same. The only difference surfaces when the values are substituted.

The current is

$$I_E = \frac{V_E}{R_E} = \frac{2.46 \text{ V}}{1.1 \text{ k}\Omega} = 2.24 \text{ mA}$$

For the collector-emitter loop,

$$-I_E R_E + V_{CE} - I_C R_C + V_{CC} = 0$$

Substituting  $I_E \equiv I_C$  and gathering terms, we have

$$V_{CE} = -V_{CC} + I_C(R_C + R_E)$$

Substituting values gives

$$V_{CE} = -18 \text{ V} + (2.24 \text{ mA})(2.4 \text{ k}\Omega + 1.1 \text{ k}\Omega)$$

$$= -18 \text{ V} + 7.84 \text{ V}$$

$$= \mathbf{-10.16 \text{ V}}$$

## 4.16 TRANSISTOR SWITCHING NETWORKS

The application of transistors is not limited solely to the amplification of signals. Through proper design, transistors can be used as switches for computer and control applications. The network of Fig. 4.87a can be employed as an *inverter* in computer logic circuitry. Note that the output voltage  $V_C$  is opposite to that applied to the base or input terminal. In addition, note the absence of a dc supply connected to the base circuit. The only dc source is connected to the collector or output side, and for computer applications is typically equal to the magnitude of the “high” side of the applied signal—in this case 5 V. The resistor  $R_B$  will ensure that the full applied voltage of 5 V will not appear across the base-to-emitter junction. It will also set the  $I_B$  level for the “on” condition.

Proper design for the inversion process requires that the operating point switch from cutoff to saturation along the load line depicted in Fig. 4.87b. For our purposes we will assume that  $I_C = I_{CEO} \cong 0 \text{ mA}$  when  $I_B = 0 \mu\text{A}$  (an excellent approximation in light of improving construction techniques), as shown in Fig. 4.87b. In addition, we will assume that  $V_{CE} = V_{CE_{sat}} \cong 0 \text{ V}$  rather than the typical 0.1-V to 0.3-V level.

When  $V_i = 5 \text{ V}$ , the transistor will be “on” and the design must ensure that the network is heavily saturated by a level of  $I_B$  greater than that associated with the  $I_B$  curve appearing

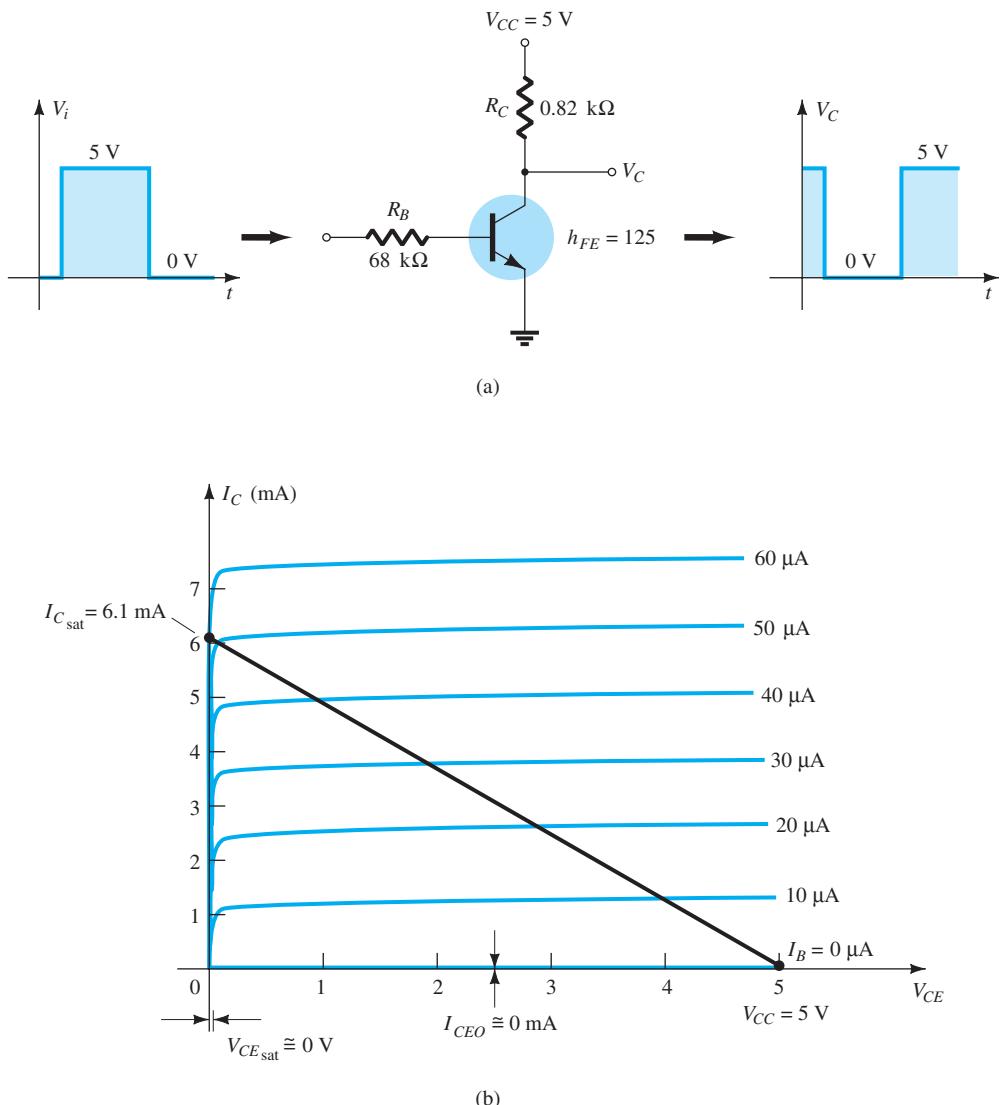


FIG. 4.87

*Transistor inverter.*

near the saturation level. In Fig. 4.87b, this requires that \$I\_B > 50 \mu\text{A}\$. The saturation level for the collector current for the circuit of Fig. 4.87a is defined by

$$I_{C_{\text{sat}}} = \frac{V_{CC}}{R_C} \quad (4.86)$$

The level of \$I\_B\$ in the active region just before saturation results can be approximated by the following equation:

$$I_{B_{\text{max}}} \approx \frac{I_{C_{\text{sat}}}}{\beta_{\text{dc}}}$$

For the saturation level we must therefore ensure that the following condition is satisfied:

$$I_B > \frac{I_{C_{\text{sat}}}}{\beta_{\text{dc}}} \quad (4.87)$$

For the network of Fig. 4.87b, when \$V\_i = 5 \text{ V}\$, the resulting level of \$I\_B\$ is

$$I_B = \frac{V_i - 0.7 \text{ V}}{R_B} = \frac{5 \text{ V} - 0.7 \text{ V}}{68 \text{ k}\Omega} = 63 \mu\text{A}$$

and

$$I_{C_{\text{sat}}} = \frac{V_{CC}}{R_C} = \frac{5 \text{ V}}{0.82 \text{ k}\Omega} \cong 6.1 \text{ mA}$$

Testing Eq. (4.87) gives

$$I_B = 63 \mu\text{A} > \frac{I_{C_{\text{sat}}}}{\beta_{\text{dc}}} = \frac{6.1 \text{ mA}}{125} = 48.8 \mu\text{A}$$

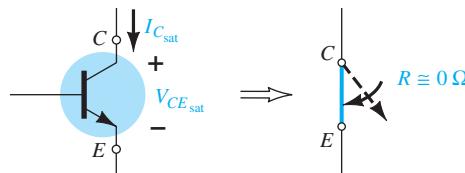
which is satisfied. Certainly, any level of  $I_B$  greater than  $60 \mu\text{A}$  will pass through a  $Q$ -point on the load line that is very close to the vertical axis.

For  $V_i = 0 \text{ V}$ ,  $I_B = 0 \mu\text{A}$ , and because we are assuming that  $I_C = I_{CEO} = 0 \text{ mA}$ , the voltage drop across  $R_C$  as determined by  $V_{RC} = I_C R_C = 0 \text{ V}$ , resulting in  $V_C = +5 \text{ V}$  for the response indicated in Fig. 4.87a.

In addition to its contribution to computer logic, the transistor can also be employed as a switch using the same extremities of the load line. At saturation, the current  $I_C$  is quite high and the voltage  $V_{CE}$  very low. The result is a resistance level between the two terminals determined by

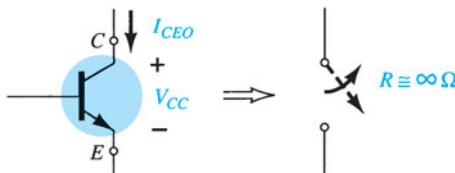
$$R_{\text{sat}} = \frac{V_{CE_{\text{sat}}}}{I_{C_{\text{sat}}}}$$

and is depicted in Fig. 4.88.



**FIG. 4.88**

Saturation conditions and the resulting terminal resistance.



**FIG. 4.89**

Cutoff conditions and the resulting terminal resistance.

Using a typical average value of  $V_{CE_{\text{sat}}}$  such as  $0.15 \text{ V}$  gives

$$R_{\text{sat}} = \frac{V_{CE_{\text{sat}}}}{I_{C_{\text{sat}}}} = \frac{0.15 \text{ V}}{6.1 \text{ mA}} = 24.6 \Omega$$

which is a relatively low value and can be considered as approximately  $0 \Omega$  when placed in series with resistors in the kilohm range.

For  $V_i = 0 \text{ V}$ , as shown in Fig. 4.89, the cutoff condition results in a resistance level of the following magnitude:

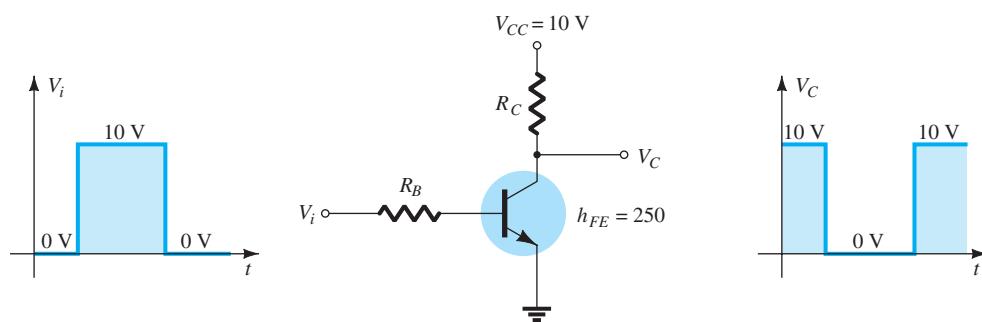
$$R_{\text{cutoff}} = \frac{V_{CC}}{I_{CEO}} = \frac{5 \text{ V}}{0 \text{ mA}} = \infty \Omega$$

resulting in the open-circuit equivalence. For a typical value of  $I_{CEO} = 10 \mu\text{A}$ , the magnitude of the cutoff resistance is

$$R_{\text{cutoff}} = \frac{V_{CC}}{I_{CEO}} = \frac{5 \text{ V}}{10 \mu\text{A}} = 500 \text{ k}\Omega$$

which certainly approaches an open-circuit equivalence for many situations.

**EXAMPLE 4.32** Determine  $R_B$  and  $R_C$  for the transistor inverter of Fig. 4.90 if  $I_{C_{\text{sat}}} = 10 \text{ mA}$ .



**FIG. 4.90**  
Inverter for Example 4.32.

**Solution:** At saturation,

$$I_{C_{\text{sat}}} = \frac{V_{CC}}{R_C}$$

and

$$10 \text{ mA} = \frac{10 \text{ V}}{R_C}$$

so that

$$R_C = \frac{10 \text{ V}}{10 \text{ mA}} = 1 \text{ k}\Omega$$

At saturation,

$$I_B \approx \frac{I_{C_{\text{sat}}}}{\beta_{\text{dc}}} = \frac{10 \text{ mA}}{250} = 40 \mu\text{A}$$

Choosing  $I_B = 60 \mu\text{A}$  to ensure saturation and using

$$I_B = \frac{V_i - 0.7 \text{ V}}{R_B}$$

we obtain

$$R_B = \frac{V_i - 0.7 \text{ V}}{I_B} = \frac{10 \text{ V} - 0.7 \text{ V}}{60 \mu\text{A}} = 155 \text{ k}\Omega$$

Choose  $R_B = 150 \text{ k}\Omega$ , which is a standard value. Then

$$I_B = \frac{V_i - 0.7 \text{ V}}{R_B} = \frac{10 \text{ V} - 0.7 \text{ V}}{150 \text{ k}\Omega} = 62 \mu\text{A}$$

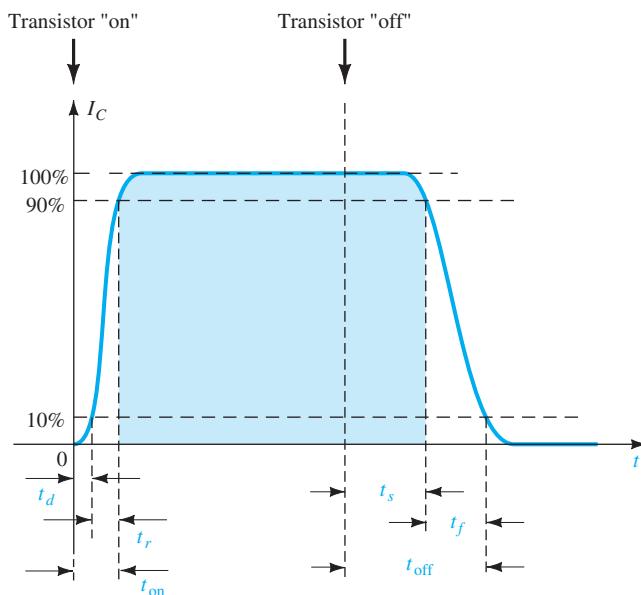
and

$$I_B = 62 \mu\text{A} > \frac{I_{C_{\text{sat}}}}{\beta_{\text{dc}}} = 40 \mu\text{A}$$

Therefore, use  $R_B = 150 \text{ k}\Omega$  and  $R_C = 1 \text{ k}\Omega$ .

There are transistors that are referred to as *switching transistors* due to the speed with which they can switch from one voltage level to the other. In Fig. 3.23c the periods of time defined as  $t_s$ ,  $t_d$ ,  $t_r$ , and  $t_f$  are provided versus collector current. Their impact on the speed of response of the collector output is defined by the collector current response of Fig. 4.91. The total time required for the transistor to switch from the “off” to the “on” state is designated as  $t_{\text{on}}$  and is defined by

$$t_{\text{on}} = t_r + t_d \quad (4.88)$$



**FIG. 4.91**  
Defining the time intervals of a pulse waveform.

with  $t_d$  the delay time between the changing state of the input and the beginning of a response at the output. The time element  $t_r$  is the rise time from 10% to 90% of the final value.

The total time required for a transistor to switch from the “on” to the “off” state is referred to as  $t_{\text{off}}$  and is defined by

$$t_{\text{off}} = t_s + t_f \quad (4.89)$$

where  $t_s$  is the storage time and  $t_f$  the fall time from 90% to 10% of the initial value.

For the general-purpose transistor of Fig. 3.23c at  $I_C = 10 \text{ mA}$ , we find that

$$t_s = 120 \text{ ns}$$

$$t_d = 25 \text{ ns}$$

$$t_r = 13 \text{ ns}$$

and

$$t_f = 12 \text{ ns}$$

so that

$$t_{\text{on}} = t_r + t_d = 13 \text{ ns} + 25 \text{ ns} = 38 \text{ ns}$$

and

$$t_{\text{off}} = t_s + t_f = 120 \text{ ns} + 12 \text{ ns} = 132 \text{ ns}$$

Comparing the values above with the following parameters of a BSV52L switching transistor reveals one of the reasons for choosing a switching transistor when the need arises:

$$t_{\text{on}} = 12 \text{ ns} \text{ and } t_{\text{off}} = 18 \text{ ns}$$

## 4.17 TROUBLESHOOTING TECHNIQUES

The art of troubleshooting is such a broad topic that a full range of possibilities and techniques cannot be covered in a few sections of a book. However, the practitioner should be aware of a few basic maneuvers and measurements that can isolate the problem area and possibly identify a solution.

Quite obviously, the first step in being able to troubleshoot a network is to fully understand the behavior of the network and to have some idea of the expected voltage and current levels. For the transistor in the active region, the most important measurable dc level is the base-to-emitter voltage.

**For an “on” transistor, the voltage  $V_{BE}$  should be in the neighborhood of 0.7 V.**

The proper connections for measuring  $V_{BE}$  appear in Fig. 4.92. Note that the positive (red) lead is connected to the base terminal for an *npn* transistor and the negative (black) lead to the emitter terminal. Any reading totally different from the expected level of about 0.7 V, such as 0, 4, or 12 V or a negative value, would be suspect and the device or network connections should be checked. For a *pnp* transistor, the same connections can be used, but a negative reading should be expected.

A voltage level of equal importance is the collector-to-emitter voltage. Recall from the general characteristics of a BJT that levels of  $V_{CE}$  in the neighborhood of 0.3 V suggest a saturated device—a condition that should not exist unless it is being employed in a switching mode. However:

**For the typical transistor amplifier in the active region,  $V_{CE}$  is usually about 25% to 75% of  $V_{CC}$ .**

For  $V_{CC} = 20 \text{ V}$ , a reading of  $V_{CE}$  of 1 V to 2 V or from 18 V to 20 V as measured in Fig. 4.93 is certainly an uncommon result, and unless the device was knowingly designed for this response, the design and operation should be investigated. If  $V_{CE} = 20 \text{ V}$  (with  $V_{CC} = 20 \text{ V}$ ) at least two possibilities exist—either the device (BJT) is damaged and has the characteristics

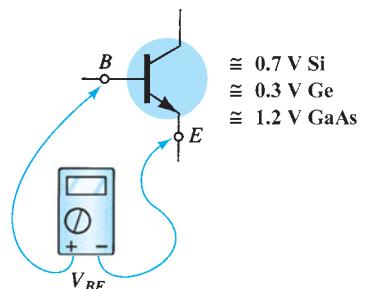


FIG. 4.92

Checking the dc level of  $V_{BE}$ .

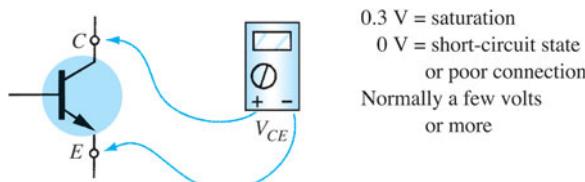
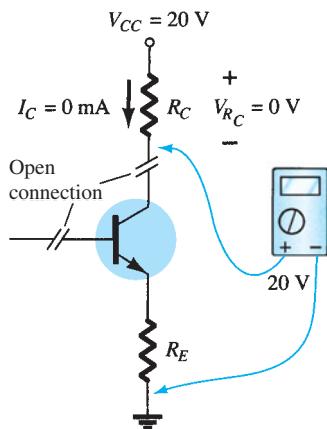
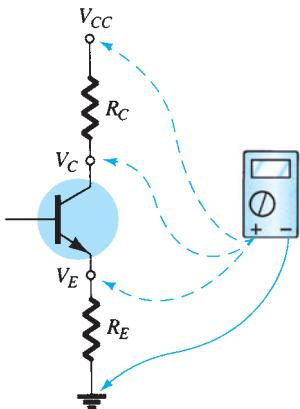


FIG. 4.93

Checking the dc level of  $V_{CE}$ .



**FIG. 4.94**  
Effect of a poor connection or damaged device.



**FIG. 4.95**  
Checking voltage levels with respect to ground.

of an open circuit between collector and emitter terminals or a connection in the collector–emitter or base–emitter circuit loop is open as shown in Fig. 4.94, establishing  $I_C$  at 0 mA and  $V_{R_C} = 0$  V. In Fig. 4.94, the black lead of the voltmeter is connected to the common ground of the supply and the red lead to the bottom terminal of the resistor. The absence of a collector current and a consequent zero voltage drop across  $R_C$  will result in a reading of 20 V. If the meter is connected between the collector terminal and ground of the BJT, the reading will be 0 V because  $V_{CC}$  is blocked from the active device by the open circuit. One of the most common errors in the laboratory is the use of the wrong resistance value for a given design. Imagine the impact of using a 680- $\Omega$  resistor for  $R_B$  rather than the design value of 680 k $\Omega$ . For  $V_{CC} = 20$  V and a fixed-bias configuration, the resulting base current would be

$$I_B = \frac{20\text{ V} - 0.7\text{ V}}{680\text{ }\Omega} = 28.4\text{ mA}$$

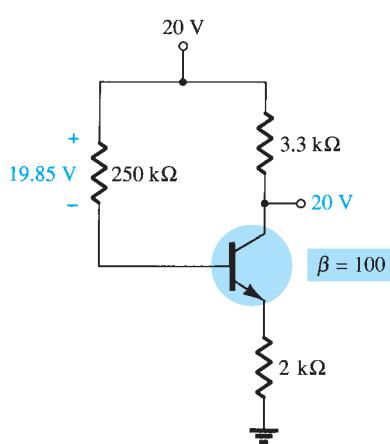
rather than the desired 28.4  $\mu$ A—a significant difference!

A base current of 28.4 mA would certainly place the design in a saturation region and possibly damage the device. Because actual resistor values are often different from the nominal color-code value (recall the common tolerance levels for resistive elements), it is time well spent to measure a resistor before inserting it in the network. The result is measurements closer to theoretical levels and some insurance that the correct resistance value is being employed.

There are times when frustration will develop. You check the device on a curve tracer or other BJT testing instrumentation and it looks good. All resistor levels seem correct, the connections appear solid, and the proper supply voltage has been applied—what next? Now the troubleshooter must strive to attain a higher level of sophistication. Could it be that the internal connection of a lead is faulty? How often has simply touching a lead at the proper point created a “make or break” situation between connections? Perhaps the supply was turned on and set at the proper voltage but the current-limiting knob was left in the zero position, preventing the proper level of current as demanded by the network design. Obviously, the more sophisticated the system, the broader is the range of possibilities. In any case, one of the most effective methods of checking the operation of a network is to check various voltage levels with respect to ground by hooking up the black (negative) lead of a voltmeter to ground and “touching” the important terminals with the red (positive) lead. In Fig. 4.95, if the red lead is connected directly to  $V_{CC}$ , it should read  $V_{CC}$  volts because the network has one common ground for the supply and network parameters. At  $V_C$  the reading should be less, as determined by the drop across  $R_C$ , and  $V_E$  should be less than  $V_C$  by the collector–emitter voltage  $V_{CE}$ . The failure of any of these points to register what would appear to be a reasonable level may be sufficient in itself to define the faulty connection or element. If  $V_{R_C}$  and  $V_{R_E}$  are reasonable values but  $V_{CE}$  is 0 V, the possibility exists that the BJT is damaged and displays a short-circuit equivalence between collector and emitter terminals. As noted earlier, if  $V_{CE}$  registers a level of about 0.3 V as defined by  $V_{CE} = V_C - V_E$  (the difference of the two levels as measured above), the network may be in saturation with a device that may or may not be defective.

It should be somewhat obvious from the discussion above that the voltmeter section of the VOM or DMM is quite important in the troubleshooting process. Current levels are usually calculated from the voltage levels across resistors rather than “breaking” the network to insert the milliammeter section of a multimeter. On large schematics, specific voltage levels are provided with respect to ground for easy checking and identification of possible problem areas. Of course, for the networks covered in this chapter, one must simply be aware of typical levels within the system as defined by the applied potential and general operation of the network.

All in all, the troubleshooting process is a true test of your clear understanding of the proper behavior of a network and the ability to isolate problem areas using a few basic measurements with the appropriate instruments. Experience is the key, and that will come only with continued exposure to practical circuits.



**FIG. 4.96**  
Network for Example 4.33.

**EXAMPLE 4.33** Based on the readings provided in Fig. 4.96, determine whether the network is operating properly and, if not, the probable cause.

**Solution:** The 20 V at the collector immediately reveals that  $I_C = 0$  mA, due to an open circuit or a nonoperating transistor. The level of  $V_{R_B} = 19.85$  V also reveals that the transistor is “off” because the difference of  $V_{CC} - V_{R_B} = 0.15$  V is less than that required

to turn “on” the transistor and provide some voltage for  $V_E$ . In fact, if we assume a short-circuit condition from base to emitter, we obtain the following current through  $R_B$ :

$$I_{R_B} = \frac{V_{CC}}{R_B + R_E} = \frac{20 \text{ V}}{252 \text{ k}\Omega} = 79.4 \mu\text{A}$$

which matches that obtained from

$$I_{R_B} = \frac{V_{R_B}}{R_B} = \frac{19.85 \text{ V}}{250 \text{ k}\Omega} = 79.4 \mu\text{A}$$

If the network were operating properly, the base current should be

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20 \text{ V} - 0.7 \text{ V}}{250 \text{ k}\Omega + (101)(2 \text{ k}\Omega)} = \frac{19.3 \text{ V}}{452 \text{ k}\Omega} = 42.7 \mu\text{A}$$

The result, therefore, is that the transistor is in a damaged state, with a short-circuit condition between base and emitter.

**EXAMPLE 4.34** Based on the readings appearing in Fig. 4.97, determine whether the transistor is “on” and the network is operating properly.

**Solution:** Based on the resistor values of  $R_1$  and  $R_2$  and the magnitude of  $V_{CC}$ , the voltage  $V_B = 4 \text{ V}$  seems appropriate (and in fact it is). The 3.3 V at the emitter results in a 0.7-V drop across the base-to-emitter junction of the transistor, suggesting an “on” transistor. However, the 20 V at the collector reveals that  $I_C = 0 \text{ mA}$ , although the connection to the supply must be “solid” or the 20 V would not appear at the collector of the device. Two possibilities exist—there can be a poor connection between  $R_C$  and the collector terminal of the transistor or the transistor has an open base-to-collector junction. First, check the continuity at the collector junction using an ohm-meter, and if it is okay, check the transistor using one of the methods described in Chapter 3.

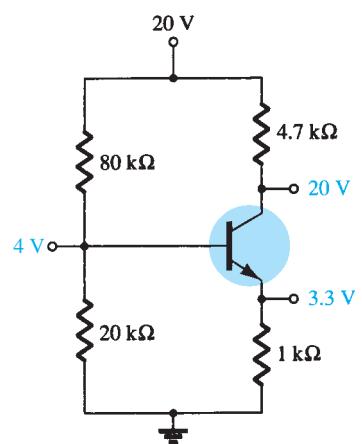


FIG. 4.97

Network for Example 4.34.

## 4.18 BIAS STABILIZATION

The stability of a system is a measure of the sensitivity of a network to variations in its parameters. In any amplifier employing a transistor the collector current  $I_C$  is sensitive to each of the following parameters:

**$\beta$ : increases with increase in temperature**

**$|V_{BE}|$ : decreases about 2.5 mV per degree Celsius ( $^{\circ}\text{C}$ ) increase in temperature**

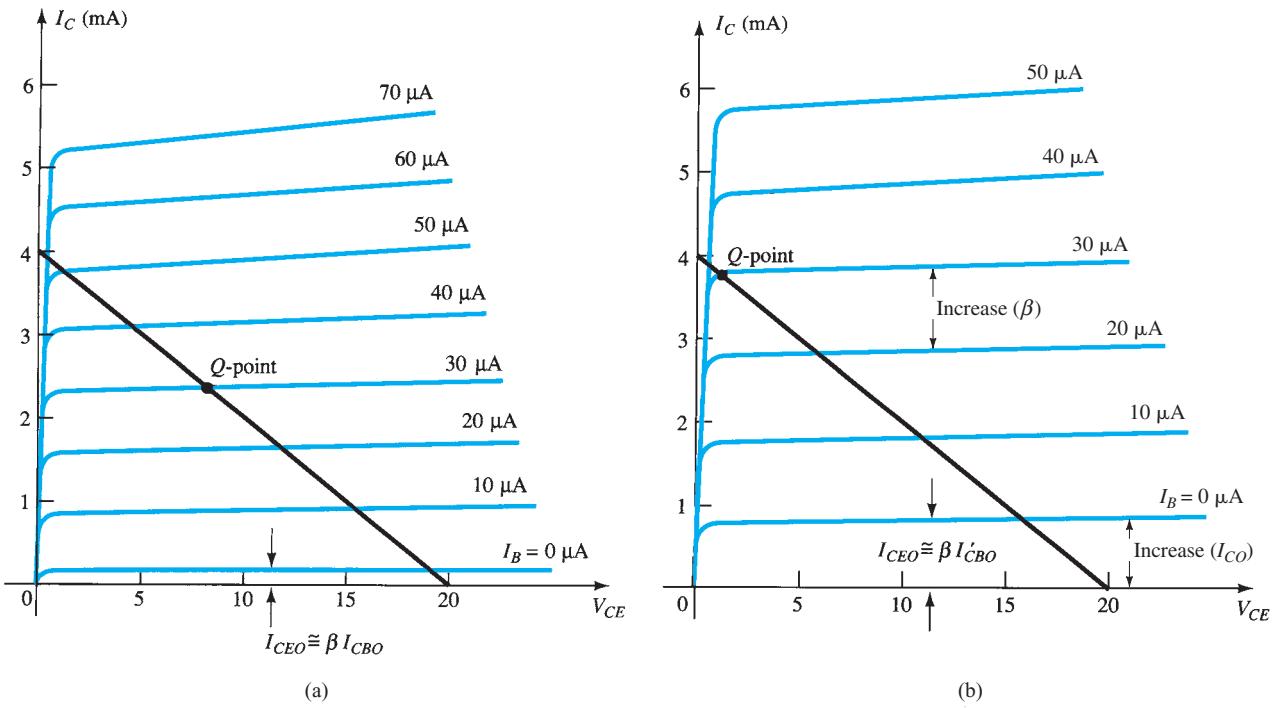
**$I_{CO}$  (reverse saturation current): doubles in value for every  $10^{\circ}\text{C}$  increase in temperature**

Any or all of these factors can cause the bias point to drift from the designed point of operation. Table 4.2 reveals how the levels of  $I_{CO}$  and  $V_{BE}$  change with increase in temperature for a particular transistor. At room temperature (about  $25^{\circ}\text{C}$ )  $I_{CO} = 0.1 \text{ nA}$ , whereas at  $100^{\circ}\text{C}$  (boiling point of water)  $I_{CO}$  is about 200 times larger, at  $20 \text{ nA}$ . For the same temperature variation,  $\beta$  increases from 50 to 80 and  $V_{BE}$  drops from 0.65 V to 0.48 V. Recall that  $I_B$  is quite sensitive to the level of  $V_{BE}$ , especially for levels beyond the threshold value.

**TABLE 4.2**  
Variation of Silicon Transistor Parameters  
with Temperature

$T (^{\circ}\text{C})$	$I_{CO} (\text{nA})$	$\beta$	$V_{BE} (\text{V})$
-65	$0.2 \times 10^{-3}$	20	0.85
25	0.1	50	0.65
100	20	80	0.48
175	$3.3 \times 10^3$	120	0.3

The effect of changes in leakage current ( $I_{CO}$ ) and current gain ( $\beta$ ) on the dc bias point is demonstrated by the common-emitter collector characteristics of Fig. 4.98a and b. Figure 4.98 shows how the transistor collector characteristics change from a temperature of



**FIG. 4.98**

Shift in dc bias point (Q-point) due to change in temperature: (a) 25°C; (b) 100°C.

25°C to a temperature of 100°C. Note that the significant increase in leakage current not only causes the curves to rise, but also causes an increase in beta, as revealed by the larger spacing between curves.

An operating point may be specified by drawing the circuit dc load line on the graph of the collector characteristic and noting the intersection of the load line and the dc base current set by the input circuit. An arbitrary point is marked in Fig. 4.98a at  $I_B = 30 \mu\text{A}$ . Because the fixed-bias circuit provides a base current whose value depends approximately on the supply voltage and base resistor, neither of which is affected by temperature or the change in leakage current or beta, the same base current magnitude will exist at high temperatures as indicated on the graph of Fig. 4.98b. As the figure shows, this will result in the dc bias point's shifting to a higher collector current and a lower collector-emitter voltage operating point. In the extreme, the transistor could be driven into saturation. In any case, the new operating point may not be at all satisfactory, and considerable distortion may result because of the bias-point shift. A better bias circuit is one that will stabilize or maintain the dc bias initially set, so that the amplifier can be used in a changing-temperature environment.

### Stability Factors $S(I_{CO})$ , $S(V_{BE})$ , and $S(\beta)$

A stability factor  $S$  is defined for each of the parameters affecting bias stability as follows:

$$S(I_{CO}) = \frac{\Delta I_C}{\Delta I_{CO}} \quad (4.90)$$

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}} \quad (4.91)$$

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta} \quad (4.92)$$

In each case, the delta symbol ( $\Delta$ ) signifies change in that quantity. The numerator of each equation is the change in collector current as established by the change in the quantity

in the denominator. For a particular configuration, if a change in  $I_{CO}$  fails to produce a significant change in  $I_C$ , the stability factor defined by  $S(I_{CO}) = \Delta I_C / \Delta I_{CO}$  will be quite small. In other words:

**Networks that are quite stable and relatively insensitive to temperature variations have low stability factors.**

In some ways it would seem more appropriate to consider the quantities defined by Eqs. (4.90) through (4.92) to be sensitivity factors because:

**The higher the stability factor, the more sensitive is the network to variations in that parameter.**

The study of stability factors requires the knowledge of differential calculus. Our purpose here, however, is to review the results of the mathematical analysis and to form an overall assessment of the stability factors for a few of the most popular bias configurations. A great deal of literature is available on this subject, and if time permits, you are encouraged to read more on the subject. Our analysis will begin with the  $S(I_{CO})$  level for each configuration.

## **$S(I_{CO})$**

### **Fixed-Bias Configuration**

For the fixed-bias configuration, the following equation results:

$$S(I_{CO}) \equiv \beta \quad (4.93)$$

### **Emitter-Bias Configuration**

For the emitter-bias configuration of Section 4.4, an analysis of the network results in

$$S(I_{CO}) \equiv \frac{\beta(1 + R_B/R_E)}{\beta + R_B/B_E} \quad (4.94)$$

For  $R_B/R_E \gg \beta$ , Eq. (4.94) reduces to the following:

$$S(I_{CO}) \equiv \beta \quad \text{for } R_B/R_E \gg \beta \quad (4.95)$$

as shown on the graph of  $S(I_{CO})$  versus  $R_B/R_E$  in Fig. 4.99.

For  $R_B/R_E \ll 1$ , Eq. (4.94) will approach the following level (as shown in Fig. 4.99):

$$S(I_{CO}) \equiv 1 \quad \text{for } R_B/R_E \ll 1 \quad (4.96)$$

revealing that the stability factor will approach its lowest level as  $R_E$  becomes sufficiently large. Keep in mind, however, that good bias control normally requires that  $R_B$  be greater than  $R_E$ . The result therefore is a situation where the best stability levels are associated with poor design criteria. Obviously, a trade-off must occur that will satisfy both the stability and bias specifications. It is interesting to note in Fig. 4.99 that the lowest value of  $S(I_{CO})$  is 1, revealing that  $I_C$  will always increase at a rate equal to or greater than  $I_{CO}$ .

For the range where  $R_B/R_E$  ranges between 1 and  $(\beta + 1)$ , the stability factor will be determined by

$$S(I_{CO}) \equiv \frac{R_B}{R_E} \quad (4.97)$$

The results reveal that the emitter-bias configuration is quite stable when the ratio  $R_B/R_E$  is as small as possible and the least stable when the same ratio approaches  $\beta$ .

Note that the equation for the fixed-bias configuration matches the maximum value for the emitter-bias configuration. The result clearly reveals that the fixed-bias configuration has a poor stability factor and a high sensitivity to variations in  $I_{CO}$ .

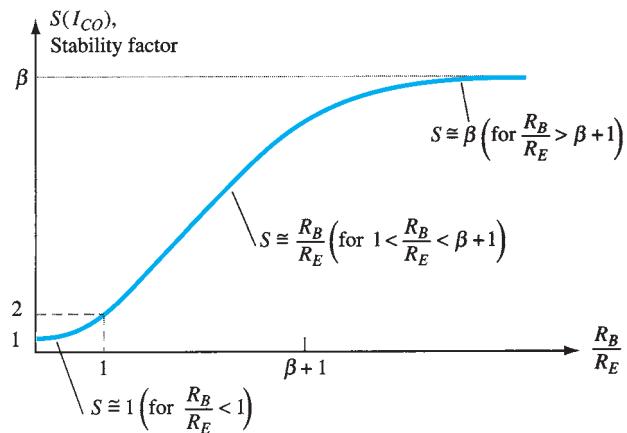


FIG. 4.99

Variation of stability factor  $S(I_{CO})$  with the resistor ratio  $R_B/R_E$  for the emitter-bias configuration.

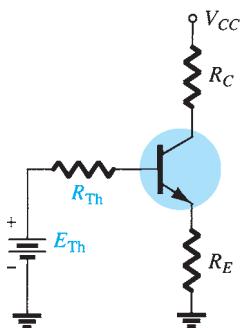


FIG. 4.100

Equivalent circuit for the voltage-divider bias configuration.

### Voltage-Divider Bias Configuration

Recall from Section 4.5 the development of the Thévenin equivalent network appearing in Fig. 4.100, for the voltage-divider bias configuration. For the network of Fig. 4.100, the equation for  $S(I_{CO})$  is the following:

$$S(I_{CO}) \cong \frac{\beta(1 + R_{Th}/R_E)}{\beta + R_{Th}/R_E} \quad (4.98)$$

Note the similarities with Eq. (4.94), where it was determined that  $S(I_{CO})$  had its lowest level and the network had its greatest stability when  $R_E > R_B$ . For Eq. (4.98), the corresponding condition is  $R_E > R_{Th}$ , or  $R_{Th}/R_E$  should be as small as possible. For the voltage-divider bias configuration,  $R_{Th}$  can be much less than the corresponding  $R_{Th}$  of the emitter-bias configuration and still have an effective design.

### Feedback-Bias Configuration ( $R_E = 0 \Omega$ )

In this case,

$$S(I_{CO}) \cong \frac{\beta(1 + R_B/R_C)}{\beta + R_B/R_C} \quad (4.99)$$

Because the equation is similar in format to that obtained for the emitter-bias and voltage-divider bias configurations, the same conclusions regarding the ratio  $R_B/R_C$  can be applied here also.

### Physical Impact

Equations of the type developed above often fail to provide a physical sense for why the networks perform as they do. We are now aware of the relative levels of stability and how the choice of parameters can affect the sensitivity of the network, but without the equations it may be difficult for us to explain in words why one network is more stable than another. The next few paragraphs attempt to fill this void through the use of some of the very basic relationships associated with each configuration.

For the fixed-bias configuration of Fig. 4.101a, the equation for the base current is

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

with the collector current determined by

$$I_C = \beta I_B + (\beta + 1)I_{CO} \quad (4.100)$$

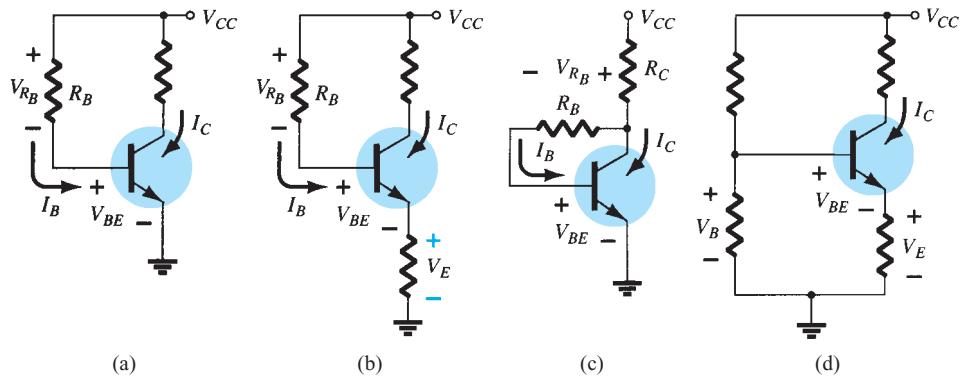


FIG. 4.101

Review of biasing managements and the stability factor  $S(I_{C0})$ .

If  $I_C$  as defined by Eq. (4.93) should increase due to an increase in  $I_{CO}$ , there is nothing in the equation for  $I_B$  that would attempt to offset this undesirable increase in current level (assuming  $V_{BE}$  remains constant). In other words, the level of  $I_C$  would continue to rise with temperature, with  $I_B$  maintaining a fairly constant value—a very unstable situation.

For the emitter-bias configuration of Fig. 4.101b, however, an increase in  $I_C$  due to an increase in  $I_{CO}$  will cause the voltage  $V_E = I_E R_E \cong I_C R_E$  to increase. The result is a drop in the level of  $I_B$  as determined by the following equation:

$$I_B \downarrow = \frac{V_{CC} - V_{BE} - V_E \uparrow}{R_B} \quad (4.101)$$

A drop in  $I_B$  will have the effect of reducing the level of  $I_C$  through transistor action and thereby offset the tendency of  $I_C$  to increase due to an increase in temperature. In total, therefore, the configuration is such that there is a reaction to an increase in  $I_C$  that will tend to oppose the change in bias conditions.

The feedback configuration of Fig. 4.101c operates in much the same way as the emitter-bias configuration when it comes to levels of stability. If  $I_C$  should increase due to an increase in temperature, the level of  $V_{R_C}$  will increase in the equation

$$I_B \downarrow = \frac{V_{CC} - V_{BE} - V_{R_C} \uparrow}{R_B} \quad (4.102)$$

and the level of  $I_B$  will decrease. The result is a stabilizing effect as described for the emitter-bias configuration. One must be aware that the action described above does not happen in a step-by-step sequence. Rather, it is a simultaneous action to maintain the established bias conditions. In other words, the very instant  $I_C$  begins to rise, the network will sense the change and the balancing effect described above will take place.

The most stable of the configurations is the voltage-divider bias network of Fig. 4.101d. If the condition  $\beta R_E \gg 10R_2$  is satisfied, the voltage  $V_B$  will remain fairly constant for changing levels of  $I_C$ . The base-to-emitter voltage of the configuration is determined by  $V_{BE} = V_B - V_E$ . If  $I_C$  should increase,  $V_E$  will increase as described above, and for a constant  $V_B$  the voltage  $V_{BE}$  will drop. A drop in  $V_{BE}$  will establish a lower level of  $I_B$ , which will try to offset the increased level of  $I_C$ .

**EXAMPLE 4.35** Calculate the stability factor and the change in  $I_C$  from 25°C to 100°C for the transistor defined by Table 4.2 for the following emitter-bias arrangements:

- $R_B/R_E = 250$  ( $R_B = 250R_E$ ).
- $R_B/R_E = 10$  ( $R_B = 10R_E$ ).
- $R_B/R_E = 0.01$  ( $R_E = 100R_B$ ).

**Solution:**

$$\begin{aligned} \text{a. } S(I_{CO}) &= \frac{\beta(1 + R_B/R_E)}{\beta + R_B/R_E} \\ &= \frac{50(1 + 250)}{50 + 250} \\ &\approx \mathbf{41.83} \end{aligned}$$

which begins to approach the level defined by  $\beta = 50$ .

The change in  $I_C$  is given by

$$\begin{aligned} \Delta I_C &= [S(I_{CO})](\Delta I_{CO}) = (41.83)(19.9 \text{ nA}) \\ &\approx \mathbf{0.83 \mu A} \end{aligned}$$

$$\begin{aligned} \text{b. } S(I_{CO}) &= \frac{\beta(1 + R_B/R_E)}{\beta + R_B/R_E} \\ &= \frac{50(1 + 10)}{50 + 10} \\ &\approx \mathbf{9.17} \end{aligned}$$

$$\begin{aligned} \Delta I_C &= [S(I_{CO})](\Delta I_{CO}) = (9.17)(19.9 \text{ nA}) \\ &\approx \mathbf{0.18 \mu A} \end{aligned}$$

$$\begin{aligned} \text{c. } S(I_{CO}) &= \frac{\beta(1 + R_B/R_E)}{\beta + R_B/R_E} \\ &= \frac{50(1 + 0.01)}{50 + 0.01} \\ &\approx \mathbf{1.01} \end{aligned}$$

which is certainly very close to the level of 1 forecast if  $R_B/R_E \ll 1$ .

We have

$$\begin{aligned} \Delta I_C &= [S(I_{CO})](\Delta I_{CO}) = 1.01(19.9 \text{ nA}) \\ &= \mathbf{20.1 \text{ nA}} \end{aligned}$$


---

Example 4.35 reveals how lower and lower levels of  $I_{CO}$  for the modern-day BJT transistor have improved the stability level of the basic bias configurations. Even though the change in  $I_C$  is considerably different in a circuit having ideal stability ( $S = 1$ ) from one having a stability factor of 41.83, the change in  $I_C$  is not that significant. For example, the amount of change in  $I_C$  from a dc bias current set at, say, 2 mA, would be from 2 mA to 2.00083 mA in the worst case, which is obviously small enough to be ignored for most applications. Some power transistors exhibit larger leakage currents, but for most amplifier circuits the lower levels of  $I_{CO}$  have had a very positive impact on the stability question.

 **$S(V_{BE})$** 

The stability factor  $S(V_{BE})$  is defined by

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}}$$

**Fixed-Bias Configuration**

For the fixed-bias configuration:

$$S(V_{BE}) \approx \frac{-\beta}{R_B}$$

(4.103)

**Emitter-Bias Configuration**

For the emitter-bias configuration:

$$S(V_{BE}) \approx \frac{-\beta/R_E}{\beta + R_B/R_E}$$

(4.104)

$$S(V_{BE}) \cong \frac{-\beta/R_E}{\beta} = -\frac{1}{R_E} \quad (4.105)$$

which shows that the larger the resistance  $R_E$ , the lower is the stability factor and the more stable is the system.

## Voltage-Divider Configuration

For the voltage-divider configuration:

$$S(V_{BE}) = \frac{-\beta/R_E}{\beta + R_{Th}/R_E} \quad (4.106)$$

## Feedback-Bias Configuration

For the feedback-bias configuration:

$$S(V_{BE}) = \frac{-\beta/R_C}{\beta + R_B/R_C} \quad (4.107)$$

**EXAMPLE 4.36** Determine the stability factor  $S(V_{BE})$  and the change in  $I_C$  from 25°C to 100°C for the transistor defined by Table 4.2 for the following bias arrangements.

- Fixed-bias with  $R_B = 240 \text{ k}\Omega$  and  $\beta = 100$ .
- Emitter-bias with  $R_B = 240 \text{ k}\Omega$ ,  $R_E = 1 \text{ k}\Omega$ , and  $\beta = 100$ .
- Emitter-bias with  $R_B = 47 \text{ k}\Omega$ ,  $R_E = 4.7 \text{ k}\Omega$ , and  $\beta = 100$ .

### Solution:

a. Eq. (4.103): 
$$\begin{aligned} S(V_{BE}) &= -\frac{\beta}{R_B} \\ &= -\frac{100}{240 \text{ k}\Omega} \\ &= -0.417 \times 10^{-3} \end{aligned}$$

and 
$$\begin{aligned} \Delta I_C &= [S(V_{BE})](\Delta V_{BE}) \\ &= (-0.417 \times 10^{-3})(0.48 \text{ V} - 0.65 \text{ V}) \\ &= (-0.417 \times 10^{-3})(-0.17 \text{ V}) \\ &= 70.9 \mu\text{A} \end{aligned}$$

- b. In this case,  $\beta = 100$  and  $R_B/R_E = 240$ . The condition  $\beta \gg R_B/R_E$  is not satisfied, negating the use of Eq. (4.105) and requiring the use of Eq. (4.104).

Eq. (4.104): 
$$\begin{aligned} S(V_{BE}) &= \frac{-\beta/R_E}{\beta + R_B/R_E} \\ &= \frac{-(100)/(1 \text{ k}\Omega)}{100 + (240 \text{ k}\Omega/1 \text{ k}\Omega)} = \frac{-0.1}{100 + 240} \\ &= -0.294 \times 10^{-3} \end{aligned}$$

which is about 30% less than the fixed-bias value due to the additional  $R_E$  term in the denominator of the  $S(V_{BE})$  equation. We have

$$\begin{aligned} \Delta I_C &= [S(V_{BE})](\Delta V_{BE}) \\ &= (-0.294 \times 10^{-3})(-0.17 \text{ V}) \\ &\approx 50 \mu\text{A} \end{aligned}$$

- c. In this case,

$$\beta = 100 \gg \frac{R_B}{R_E} = \frac{47 \text{ k}\Omega}{4.7 \text{ k}\Omega} = 10 \quad (\text{satisfied})$$

Eq. (4.105):

$$\begin{aligned}
 S(V_{BE}) &= -\frac{1}{R_E} \\
 &= -\frac{1}{4.7 \text{ k}\Omega} \\
 &= -0.212 \times 10^{-3} \\
 \text{and} \quad \Delta I_C &= [S(V_{BE})](\Delta V_{BE}) \\
 &= (-0.212 \times 10^{-3})(-0.17 \text{ V}) \\
 &= 36.04 \mu\text{A}
 \end{aligned}$$


---

In Example 4.36, the increase of  $70.9 \mu\text{A}$  will have some impact on the level of  $I_{C_Q}$ . For a situation where  $I_{C_Q} = 2 \text{ mA}$ , the resulting collector current increases to a 3.5% increase.

$$\begin{aligned}
 I_{C_Q} &= 2 \text{ mA} + 70.9 \mu\text{A} \\
 &= 2.0709 \text{ mA}
 \end{aligned}$$

For the voltage-divider configuration, the level of  $R_B$  will be changed to  $R_{Th}$  in Eq. (4.104) (as defined by Fig. 4.100). In Example 4.36, the use of  $R_B = 47 \text{ k}\Omega$  is a questionable design. However,  $R_{Th}$  for the voltage-divider configuration can be this level or lower and still maintain good design characteristics. The resulting equation for  $S(V_{BE})$  for the feedback network will be similar to that of Eq. (4.104) with  $R_E$  replaced by  $R_C$ .

### **S( $\beta$ )**

The last stability factor to be investigated is that of  $S(\beta)$ . The mathematical development is more complex than that encountered for  $S(I_{CO})$  and  $S(V_{BE})$ , as suggested by some of the following equations.

### **Fixed-Bias Configuration**

For the fixed-bias configuration

$$S(\beta) = \frac{I_{C_1}}{\beta_1} \quad (4.108)$$

### **Emitter-Bias Configuration**

For the emitter-bias configuration

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta} = \frac{I_{C_1}(1 + R_B/R_E)}{\beta_1(\beta_2 + R_B/R_E)} \quad (4.109)$$

The notation  $I_{C_1}$  and  $\beta_1$  is used to define their values under one set of network conditions, whereas the notation  $\beta_2$  is used to define the new value of beta as established by such causes as temperature change, variation in  $\beta$  for the same transistor, or a change in transistors.

**EXAMPLE 4.37** Determine  $I_{C_Q}$  at a temperature of  $100^\circ\text{C}$  if  $I_{C_Q} = 2 \text{ mA}$  at  $25^\circ\text{C}$  for the emitter-bias configuration. Use the transistor described by Table 4.2, where  $\beta_1 = 50$  and  $\beta_2 = 80$ , and a resistance ratio  $R_B/R_E$  of 20.

**Solution:**

Eq. (4.109):

$$\begin{aligned}
 S(\beta) &= \frac{I_{C_1}(1 + R_B/R_E)}{\beta_1(1 + \beta_2 + R_B/R_E)} \\
 &= \frac{(2 \times 10^{-3})(1 + 20)}{(50)(1 + 80 + 20)} = \frac{42 \times 10^{-3}}{5050} \\
 &= 8.32 \times 10^{-6}
 \end{aligned}$$

and

$$\begin{aligned}\Delta I_C &= [S(\beta)][\Delta\beta] \\ &= (8.32 \times 10^{-6})(30) \\ &\approx 0.25 \text{ mA}\end{aligned}$$

In conclusion, therefore, the collector current changed from 2 mA at room temperature to 2.25 mA at 100°C, representing a change of 12.5%.

## Voltage-Divider Bias Configuration

For the voltage-divider bias configuration

$$S(\beta) = \frac{I_{C_1}(1 + R_{Th}/R_E)}{\beta_1(\beta_2 + R_{Th}/R_E)} \quad (4.110)$$

## Feedback-bias Configuration

For the collector feedback-bias configuration

$$S(\beta) = \frac{I_{C_1}(R_B + R_C)}{\beta_1(R_B + \beta_2 R_C)} \quad (4.111)$$

## Summary

Now that the three stability factors of importance have been introduced, the total effect on the collector current can be determined using the following equation for each configuration

$$\Delta I_C = S(I_{CO})\Delta I_{CO} + S(V_{BE})\Delta V_{BE} + S(\beta)\Delta\beta \quad (4.112)$$

The equation may initially appear quite complex, but note that each component is simply a stability factor for the configuration multiplied by the resulting change in a parameter between the temperature limits of interest. In addition, the  $\Delta I_C$  to be determined is simply the change in  $I_C$  from the level at room temperature.

For instance, if we examine the fixed-bias configuration, Eq. (4.78) becomes

$$\Delta I_C = \beta\Delta I_{CO} - \frac{\beta}{R_B}\Delta V_{BE} + \frac{I_{C_1}}{\beta_1}\Delta\beta \quad (4.113)$$

after substituting the stability factors as derived in this section. Let us now use Table 4.2 to find the change in collector current for a temperature change from 25°C (room temperature) to 100°C (the boiling point of water). For this range the table reveals that

$$\begin{aligned}\Delta I_{CO} &= 20 \text{ nA} - 0.1 \text{ nA} = 19.9 \text{ nA} \\ \Delta V_{BE} &= 0.48 \text{ V} - 0.65 \text{ V} = -0.17 \text{ V} \quad (\text{note the sign})\end{aligned}$$

and  $\Delta\beta = 80 - 50 = 30$

Starting with a collector current of 2 mA with an  $R_B$  of 240 kΩ, we obtain the resulting change in  $I_C$  due to an increase in temperature of 75°C as follows:

$$\begin{aligned}\Delta I_C &= (50)(19.9 \text{ nA}) - \frac{50}{240 \text{ k}\Omega}(-0.17 \text{ V}) + \frac{2 \text{ mA}}{50}(30) \\ &= 1 \mu\text{A} + 35.42 \mu\text{A} + 1200 \mu\text{A} \\ &= 1.236 \text{ mA}\end{aligned}$$

which is a significant change due primarily to the change in  $\beta$ . The collector current has increased from 2 mA to 3.236 mA, but this was expected in the sense that we recognize from the content of this section that the fixed-bias configuration is the least stable.

If the more stable voltage-divider configuration is employed with a ratio  $R_{Th}/R_E = 2$  and  $R_E = 4.7 \text{ k}\Omega$ , then

$$S(I_{CO}) = 2.89, \quad S(V_{BE}) = -0.2 \times 10^{-3}, \quad S(\beta) = 1.445 \times 10^{-6}$$

$$\begin{aligned} \text{and } \Delta I_C &= (2.89)(19.9 \text{ nA}) - 0.2 \times 10^{-3}(-0.17 \text{ V}) + 1.445 \times 10^{-6}(30) \\ &= 57.51 \text{ nA} + 34 \mu\text{A} + 43.4 \mu\text{A} \\ &= 0.077 \text{ mA} \end{aligned}$$

The resulting collector current is 0.077 mA, or essentially 2.1 mA, compared to the 2.0 mA at 25°C. The network is obviously a great deal more stable than the fixed-bias configuration, as mentioned in earlier discussions. In this case,  $S(\beta)$  did not override the other two factors, and the effects of  $S(V_{BE})$  and  $S(I_{CO})$  were equally important. In fact, at higher temperatures, the effects of  $S(I_{CO})$  and  $S(V_{BE})$  will be greater than  $S(\beta)$  for the device of Table 4.2. For temperatures below 25°C,  $I_C$  will decrease with increasingly negative temperature levels.

The effect of  $S(I_{CO})$  in the design process is becoming a lesser concern because of improved manufacturing techniques, which continue to lower the level of  $I_{CO} = I_{CBO}$ . It should also be mentioned that for a particular transistor the variation in levels of  $I_{CBO}$  and  $V_{BE}$  from one transistor to another in a lot is almost negligible compared to the variation in beta. In addition, the results of the analysis above support the fact that for a good stabilized design:

**General Conclusion:**

*The ratio  $R_B/R_E$  or  $R_{Th}/R_E$  should be as small as possible with due consideration to all aspects of the design, including the ac response.*

Although the analysis above may have been clouded by some of the complex equations for some of the sensitivities, the purpose here was to develop a higher level of awareness of the factors that go into a good design and to be more intimate with the transistor parameters and their impact on the network's performance. The analysis of the earlier sections was for idealized situations with nonvarying parameter values. We are now more aware of how the dc response of the design can vary with the parameter variations of a transistor.

## 4.19 PRACTICAL APPLICATIONS

As with the diodes in Chapter 2, it would be virtually impossible to provide even a surface treatment of the broad areas of application of BJTs. However, a few applications are chosen here to demonstrate how different facets of the characteristics of BJTs are used to perform various functions.

### BJT Diode Usage and Protective Capabilities

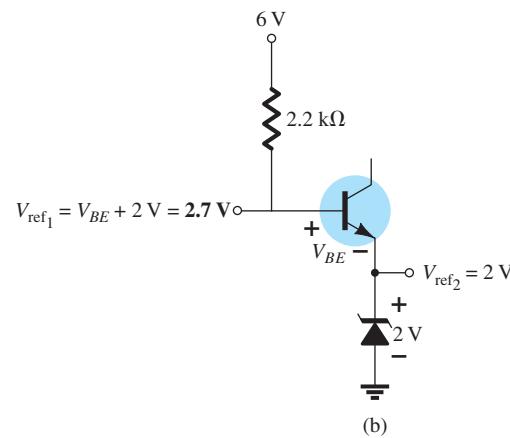
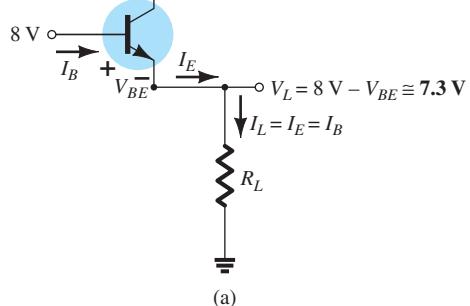
As you begin to scan complex networks you will often find transistors being used where all three terminals are not connected in the network—particularly the collector lead. In such cases it is most likely being used as a diode rather than a transistor. There are a number of reasons for such use, including the fact that it is cheaper to buy a large number of transistors rather than a smaller bundle and then pay separately for specific diodes. Also, in ICs the manufacturing process may be more direct to make additional transistors that introduce the diode construction sequence. Two examples of its use as a diode appear in Fig. 4.102. In Fig. 4.102a it is being used in a simple diode network. In Fig. 4.102b it is being used to establish a reference level.

Often times you will see a diode connected directly across a device as shown in Fig. 4.103 to simply ensure that the voltage across a device or system with the polarity shown cannot exceed the forward bias voltage of 0.7 V. In the reverse direction if the breakdown strength is sufficiently high it will simply appear as an open circuit. Again, however, only two terminals of the BJT are being employed.

The point to be made is that one should not assume that every BJT transistor in a network is being used for amplification or as a buffer between stages. The number of areas of application for BJTs beyond these areas is quite extensive.

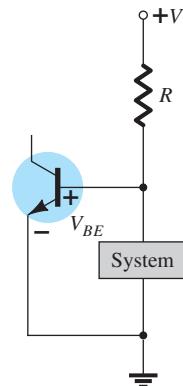
### Relay Driver

This application is in some ways a continuation of the discussion introduced for diodes about how the effects of inductive kick can be minimized through proper design. In Fig. 4.104a, a transistor is used to establish the current necessary to energize the relay in the

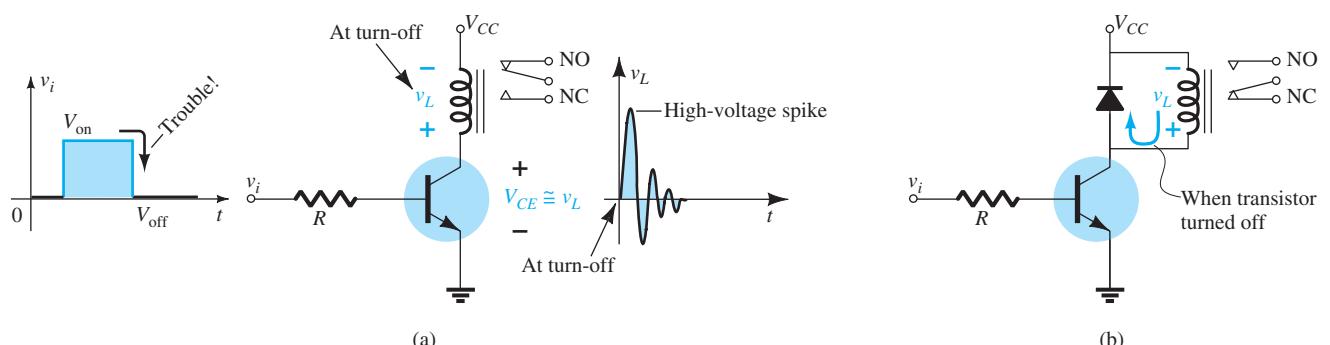

**FIG. 4.102**

*BJT applications as a diode: (a) simple series diode circuit; (b) setting a reference level.*

collector circuit. With no input at the base of the transistor, the base current, collector current, and coil current are essentially 0 A, and the relay sits in the unenergized state (normally open, NO). However, when a positive pulse is applied to the base, the transistor turns on, establishing sufficient current through the coil of the electromagnet to close the relay. Problems can now develop when the signal is removed from the base to turn off the transistor and deenergize the relay. Ideally, the current through the coil and the transistor will quickly drop to zero, the arm of the relay will be released, and the relay will simply remain dormant until the next “on” signal. However, we know from our basic circuit courses that the current through a coil cannot change instantaneously, and, in fact, the more quickly it changes, the greater the induced voltage across the coil as defined by  $v_L = L(di_L/dt)$ . In this case, the rapidly changing current through the coil will develop a large voltage across the coil with the polarity shown in Fig. 4.104a, which will appear directly across the output of the transistor. The chances are likely that its magnitude will exceed the maximum ratings of the transistor, and the semiconductor device will be permanently damaged. The voltage across the coil will not remain at its highest switching level but will oscillate as shown until its level drops to zero as the system settles down.


**FIG. 4.103**

*Acting as a protective device.*


**FIG. 4.104**

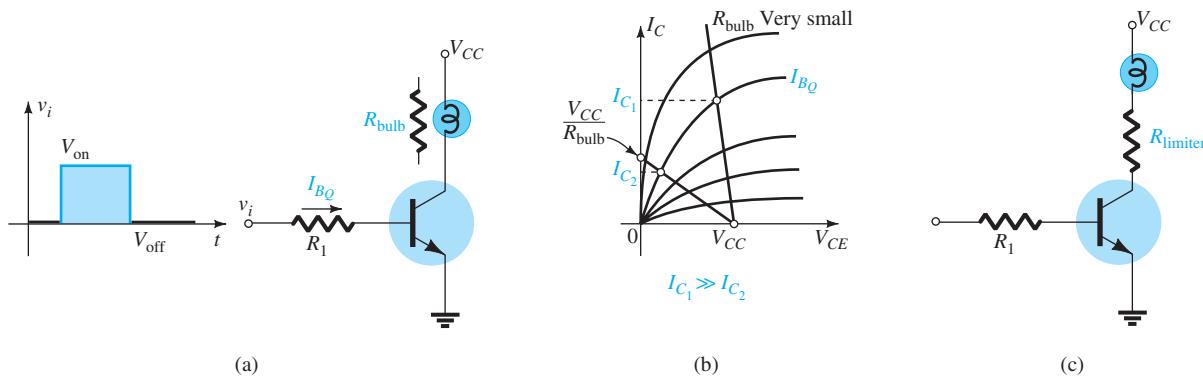
*Relay driver: (a) absence of protective device; (b) with a diode across the relay coil.*

This destructive action can be subdued by placing a diode across the coil as shown in Fig. 4.104b. During the “on” state of the transistor, the diode is back-biased; it sits like an open circuit and doesn’t affect a thing. However, when the transistor turns off, the voltage across the coil will reverse and will forward-bias the diode, placing the diode in its “on” state. The current through the inductor established during the “on” state of the transistor can then continue to flow through the diode, eliminating the severe change in current level. Because the inductive current is switched to the diode almost instantaneously after the “off” state is established, the diode must have a current rating to match the current through the inductor and the transistor when in the “on” state. Eventually, because of the resistive

elements in the loop, including the resistance of the coil windings and the diode, the high-frequency (quickly oscillating) variation in voltage level across the coil will decay to zero, and the system will settle down.

### Light Control

In Fig. 4.105a, a transistor is used as a switch to control the “on” and “off” states of the lightbulb in the collector branch of the network. When the switch is in the “on” position, we have a fixed-bias situation where the base-to-emitter voltage is at its 0.7-V level, and the base current is controlled by the resistor  $R_1$  and the input impedance of the transistor. The current through the bulb will then be beta times the base current, and the bulb will light up. A problem can develop, however, if the bulb has not been on for a while. When a lightbulb is first turned on, its resistance is quite low, even though the resistance will increase rapidly the longer the bulb is on. This can cause a momentary high level of collector current, which could damage the bulb and the transistor over time. In Fig. 4.105b, for instance, the load line for the same network with a cold and a hot resistance for the bulb is included. Note that even though the base current is set by the base circuit, the intersection with the load line results in a higher current for the cold lightbulb. Any concern about the turn-on level can easily be corrected by inserting an additional small resistor in series with the lightbulb, as shown in Fig. 4.105c, just to ensure a limit on the initial surge in current when the bulb is first turned on.



**FIG. 4.105**

Using the transistor as a switch to control the on–off states of a bulb: (a) network; (b) effect of low bulb resistance on collector current; (c) limiting resistor.

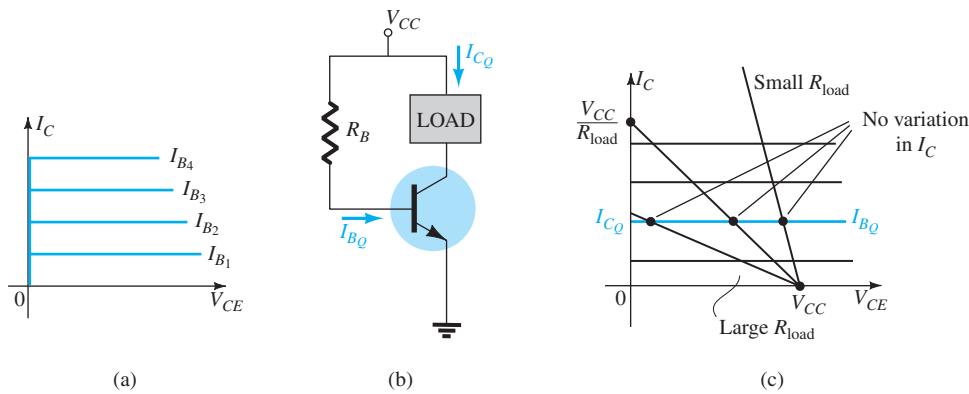
### Maintaining a Fixed Load Current

If we assume that the characteristics of a transistor have the ideal appearance of Fig. 4.106a (constant beta throughout) a source, fairly independent of the applied load, can be constructed using the simple transistor configuration of Fig. 4.106b. The base current is fixed so no matter where the load line is, the load or collector current remains the same. In other words, the collector current is independent of the load in the collector circuit. However, because the actual characteristics are more like those in Fig. 4.106b, where beta will vary from point to point, and even though the base current may be fixed by the configuration, the beta will vary from point to point with the load intersection, and  $I_C = I_L$  will vary—not characteristic of a good current source. Recall, however, that the voltage-divider configuration resulted in a low level of sensitivity to beta, so perhaps if that biasing arrangement is used, the current source equivalent is closer to reality. In fact, that is the case. If a biasing arrangement such as shown in Fig. 4.107 is employed, the sensitivity to changes in operating point due to varying loads is much less, and the collector current will remain fairly constant for changes in load resistance in the collector branch. In fact, the emitter voltage is determined by

$$V_E = V_B - 0.7 \text{ V}$$

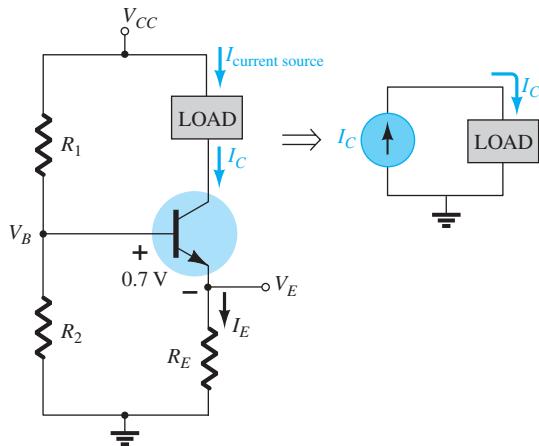
with the collector or load current determined by

$$I_C \cong I_E = \frac{V_E}{R_E} = \frac{V_B - 0.7 \text{ V}}{R_E}$$


**FIG. 4.106**

*Building a constant-current source assuming ideal BJT characteristics: (a) ideal characteristics; (b) network; (c) demonstrating why  $I_C$  remains constant.*

Using Fig. 4.107, we can describe the improved stability by examining the case where  $I_C$  may be trying to rise for any number of reasons. The result is that  $I_E = I_C$  will also rise and the voltage  $V_{RE} = I_E R_E$  will increase. However, if we assume  $V_B$  to be fixed (a good assumption because its level is determined by two fixed resistors and a voltage source), the base-to-emitter voltage  $V_{BE} = V_B - V_{RE}$  will drop. A drop in  $V_{BE}$  will cause  $I_B$  and therefore  $I_C (= \beta I_B)$  to drop. The result is a situation where any tendency for  $I_C$  to increase will be met with a network reaction that will work against the change to stabilize the system.



**FIG. 4.107**  
*Network establishing a fairly constant current source due to its reduced sensitivity to changes in beta.*

### Alarm System with a CCS

An alarm system with a constant-current source of the type just introduced appears in Fig. 4.108. Because  $\beta R_E = (100)(1 \text{ k}\Omega) = 100 \text{ k}\Omega$  is much greater than  $R_1$ , we can use the approximate approach and find the voltage  $V_{R_1}$ ,

$$V_{R_1} = \frac{2 \text{ k}\Omega(16 \text{ V})}{2 \text{ k}\Omega + 4.7 \text{ k}\Omega} = 4.78 \text{ V}$$

and then the voltage across  $R_E$ ,

$$V_{R_E} = V_{R_1} - 0.7 \text{ V} = 4.78 \text{ V} - 0.7 \text{ V} = 4.08 \text{ V}$$

and finally the emitter and collector current,

$$I_E = \frac{V_{R_E}}{R_E} = \frac{4.08 \text{ V}}{1 \text{ k}\Omega} = 4.08 \text{ mA} \cong 4 \text{ mA} = I_C$$

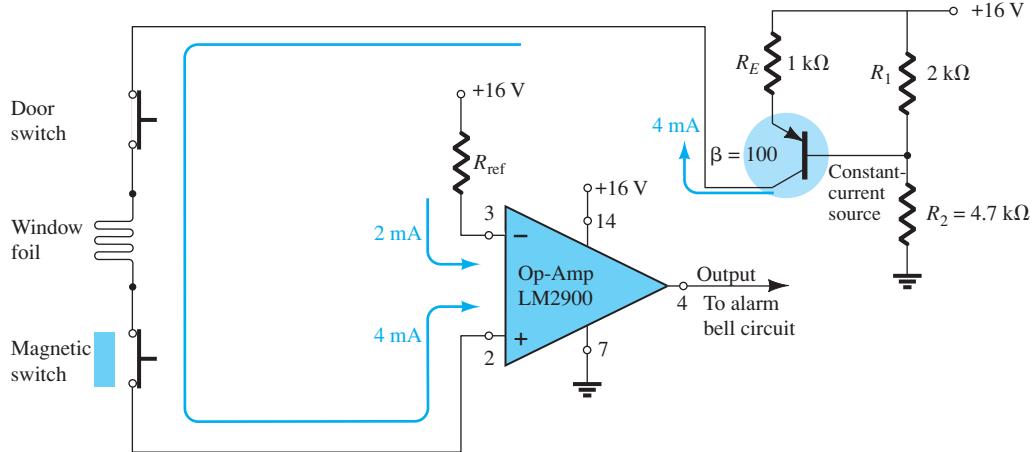


FIG. 4.108

An alarm system with a constant-current source and an op-amp comparator.

Because the collector current is the current through the circuit, the 4-mA current will remain fairly constant for slight variations in network loading. Note that the current passes through a series of sensor elements and finally into an op-amp designed to compare the 4-mA level with the set level of 2 mA. (Although the op-amp may be a new device to you, it will be discussed in detail in Chapter 10—you will not need to know the details of its behavior for this application.)

The LM2900 operational amplifier of Fig. 4.108 is one of four found in the dual-in-line integrated circuit package appearing in Fig. 4.109a. Pins 2, 3, 4, 7, and 14 were used

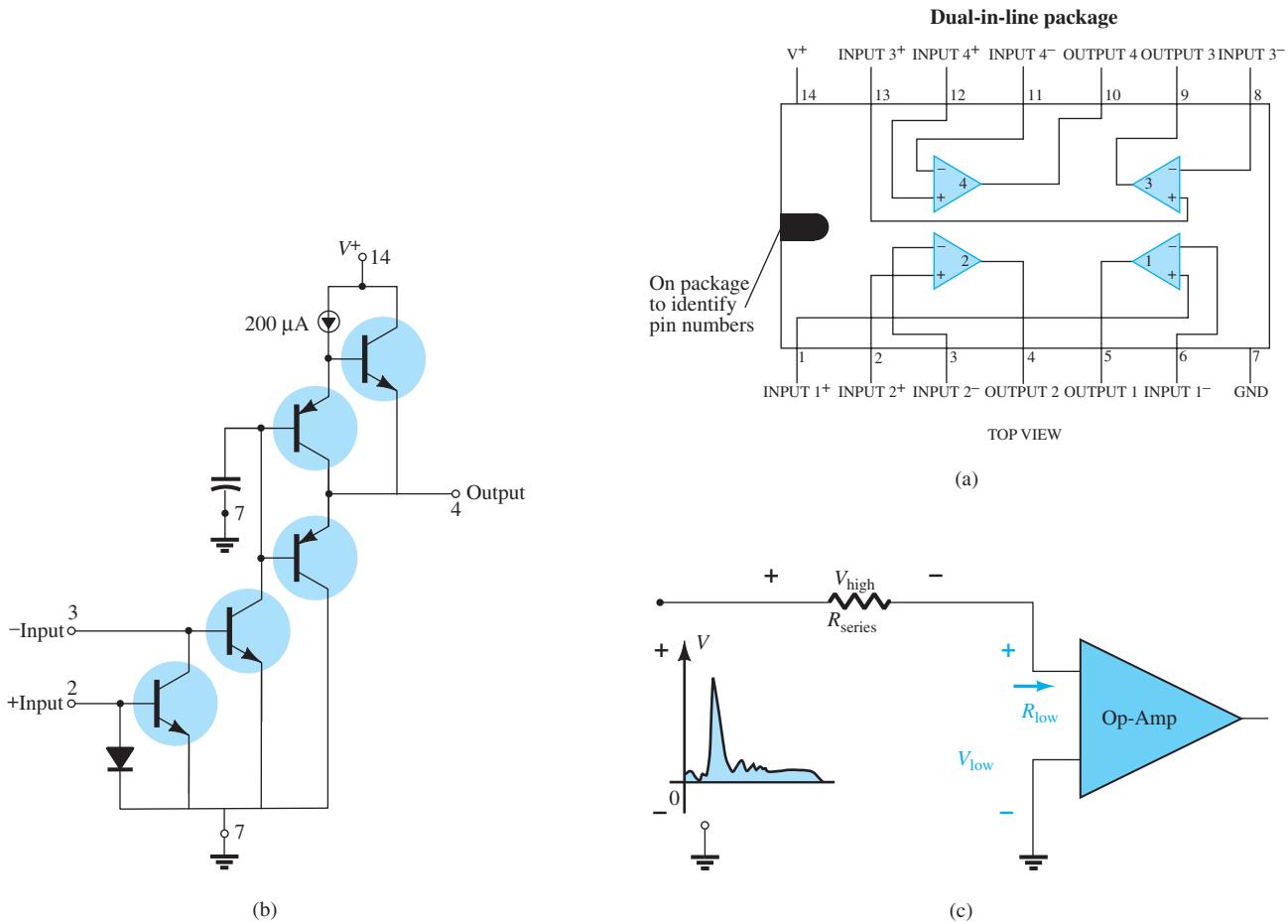


FIG. 4.109

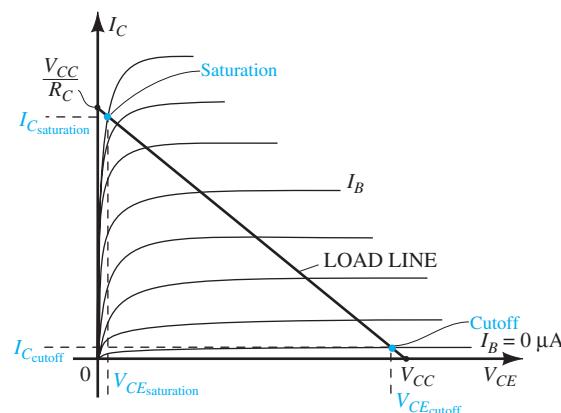
LM2900 operational amplifier: (a) dual-in-line package (DIP); (b) components; (c) impact of low-input impedance.

for the design of Fig. 4.108. For the sake of interest only, note in Fig. 4.109b the number of elements required to establish the desired terminal characteristics for the op-amp—as mentioned earlier, the details of its internal operation are left for another time. The 2 mA at terminal 3 of the op-amp is a *reference* current established by the 16-V source and  $R_{\text{ref}}$  at the negative side of the op-amp input. The 2-mA current level is required as a level against which the 4-mA current of the network is to be compared. As long as the 4-mA current on the positive input to the op-amp remains constant, the op-amp will provide a “high” output voltage, exceeding 13.5 V, with a typical level of 14.2 V (according to the specification sheets for the op-amp). However, if the sensor current drops from 4 mA to a level below 2 mA, the op-amp will respond with a “low” output voltage, typically about 0.1 V. The output of the op-amp will then signal the alarm circuit about the disturbance. Note from the above that it is not necessary for the sensor current to drop all the way down to 0 mA to signal the alarm circuit. Only a variation around the reference level that appears unusual is required—a good alarm feature.

One very important characteristic of this particular op-amp is the low-input impedance as shown in Fig. 4.109c. This feature is important because one does not want alarm circuits reacting to every voltage spike or turbulence that comes down the line because of some external switching action or outside forces such as lightning. In Fig. 4.109c, for instance, if a high-voltage spike should appear at the input to the series configuration, most of the voltage will appear across the series resistor rather than the op-amp—thus preventing a false output and an activation of the alarm.

## Logic Gates

In this application we will expand on the coverage of transistor switching networks in Section 4.15. To review, the collector-to-emitter impedance of a transistor is quite low near or at saturation and large near or at cutoff. For instance, the load line defines *saturation* as the point where the current is quite high and the collector-to-emitter voltage quite low as shown in Fig. 4.110. The resulting resistance, defined by  $R_{\text{sat}} = \frac{V_{CE_{\text{sat(low)}}}}{I_{C_{\text{sat(high)}}}}$ , is quite low and is often approximated as a short circuit. At *cutoff*, the current is relatively low and the voltage near its maximum value as shown in Fig. 4.110, resulting in a very high impedance between the collector and emitter terminal, which is often approximated by an open circuit.

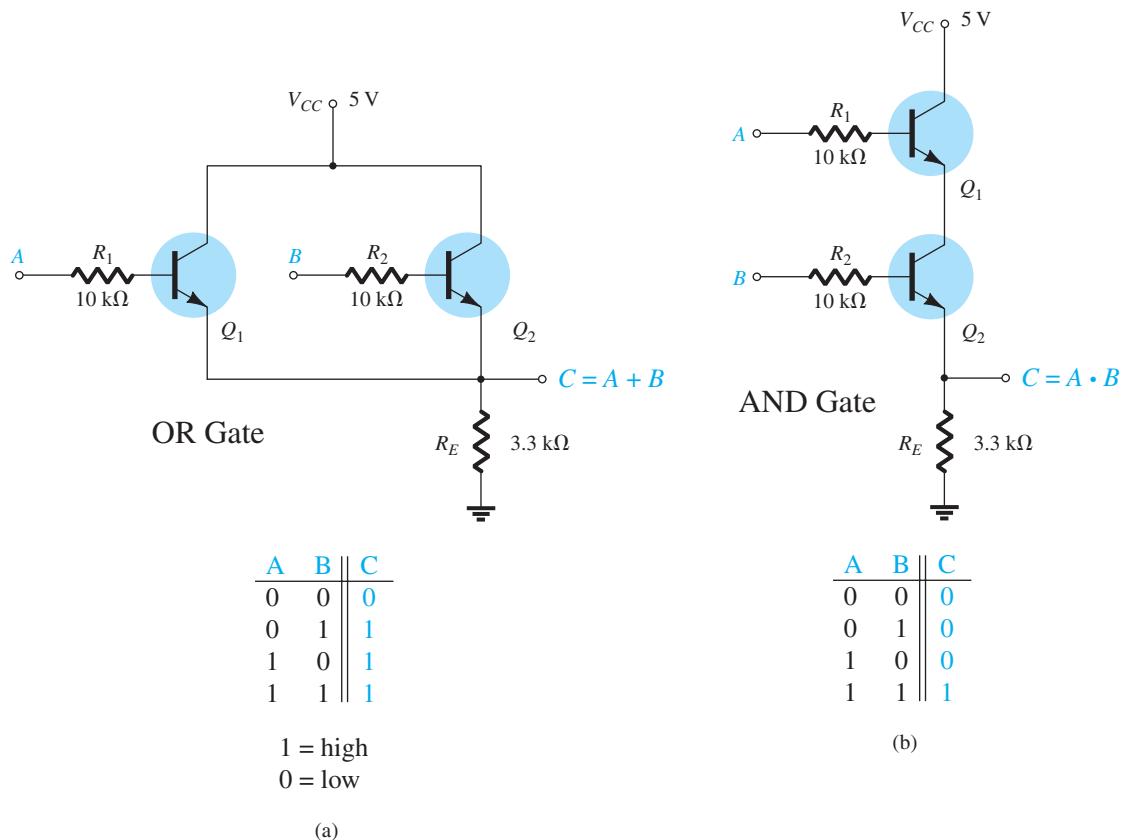


**FIG. 4.110**  
Points of operation for a BJT logic gate.

The above impedance levels established by “on” and “off” transistors make it relatively easy to understand the operation of the logic gates of Fig. 4.111. Because there are two inputs to each gate, there are four possible combinations of voltages at the input to the transistors. A 1, or “on,” state is defined by a high voltage at the base terminal to turn the transistor on. A 0, or “off,” state is defined by 0 V at the base, ensuring that transistor is off. If both A and B of the OR gate of Fig. 4.111a have a low or 0-V input, both transistors are off (cutoff), and the impedance between the collector and the emitter of each transistor can be approximated by an open circuit. Mentally replacing both transistors by open circuits

between the collector and the emitter will remove any connection between the applied bias of 5 V and the output. The result is zero current through each transistor and through the 3.3-k $\Omega$  resistor. The output voltage is therefore 0 V, or “low”—a 0 state. On the other hand, if transistor  $Q_1$  is on and  $Q_2$  is off due to a positive voltage at the base of  $Q_1$  and 0 V at the base of  $Q_2$ , then the short-circuit equivalent between the collector and emitter for transistor  $Q_1$  can be applied, and the voltage at the output is 5 V, or “high”—a 1 state. Finally, if both transistors are turned on by a positive voltage applied to the base of each, they will both ensure that the output voltage is 5 V, or “high”—a 1 state. The operation of the OR gate is properly defined: an output if either input terminal has applied turn-on voltage or if both are in the “on” state. A 0 state exists only if both do not have a 1 state at the input terminals.

The AND gate of Fig. 4.111b requires that the output be high only if both inputs have a turn-on voltage applied. If both are in the “on” state, a short-circuit equivalent can be used for the connection between the collector and the emitter of each transistor, providing a direct path from the applied 5-V source to the output—thereby establishing a high, or 1, state at the output terminal. If one or both transistors are off due to 0 V at the input terminal, an open circuit is placed in series with the path from the 5-V supply voltage to the output, and the output voltage is 0 V, or an “off” state.



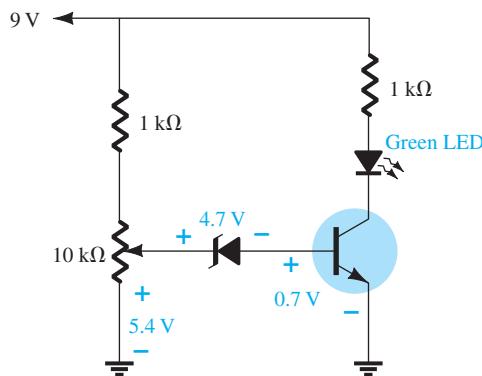
**FIG. 4.111**  
BJT logic gates: (a) OR; (b) AND.

### Voltage Level Indicator

The last application to be introduced in this section, the voltage level indicator, includes three of the elements introduced thus far: the transistor, the Zener diode, and the LED. The voltage level indicator is a relatively simple network using a green LED to indicate when the source voltage is close to its monitoring level of 9 V. In Fig. 4.112 the potentiometer is set to establish 5.4 V at the point indicated. The result is sufficient voltage to turn on both

the 4.7-V Zener and the transistor and establish a collector current through the LED sufficient in magnitude to turn on the green LED.

Once the potentiometer is set, the LED will emit its green light as long as the supply voltage is near 9 V. However, if the terminal voltage of the 9-V battery should decrease, the voltage set up by the voltage-divider network may drop to 5 V from 5.4 V. At 5 V there is insufficient voltage to turn on both the Zener and the transistor, and the transistor will be in the “off” state. The LED will immediately turn off, revealing that the supply voltage has dropped below 9 V or that the power source has been disconnected.



**FIG. 4.112**  
Voltage level indicator.

## 4.20 SUMMARY

### Important Conclusions and Concepts

- No matter what type of configuration a transistor is used in, the basic relationships between the currents are **always the same**, and the base-to-emitter voltage is the **threshold value** if the transistor is in the “on” state.
- The operating point defines where the transistor will operate on its characteristic curves under **dc conditions**. For linear (minimum distortion) amplification, the dc operating point should not be too close to the maximum power, voltage, or current rating and should avoid the regions of saturation and cutoff.
- For most configurations the dc analysis begins with a determination of the **base current**.
- For the dc analysis of a transistor network, all capacitors are replaced by an **open-circuit equivalent**.
- The fixed-bias configuration is the simplest of transistor biasing arrangements, but it is also quite unstable due its **sensitivity to beta** at the operating point.
- Determining the saturation (maximum) collector current for any configuration can usually be done quite easily if an **imaginary short circuit** is superimposed between the collector and emitter terminals of the transistor. The resulting current through the short is then the saturation current.
- The equation for the load line of a transistor network can be found by applying **Kirchhoff's voltage law** to the output or collector network. The *Q*-point is then determined by finding the **intersection** between the base current and the load line drawn on the device characteristics.
- The emitter-stabilized biasing arrangement is less sensitive to changes in beta—providing more stability for the network. Keep in mind, however, that any resistance in the emitter leg is “seen” at the base of the transistor as a much **larger resistor**, a fact that will reduce the base current of the configuration.
- The voltage-divider bias configuration is probably the most common of all the configurations. Its popularity is due primarily to its **low sensitivity** to changes in beta from one transistor to another of the same lot (with the same transistor label). The exact analysis can be applied to any configuration, but the approximate one can be applied only if the reflected emitter resistance as seen at the base is **much larger** than the lower resistor of the voltage-divider bias arrangement connected to the base of the transistor.

10. When analyzing the dc bias with a voltage feedback configuration, be sure to remember that **both** the emitter resistor and the collector resistor are reflected back to the base circuit by beta. The least sensitivity to beta is obtained when the reflected resistance is much larger than the feedback resistor between the base and the collector.
11. For the common-base configuration the **emitter current is normally determined first** due to the presence of the base-to-emitter junction in the same loop. Then the fact that the emitter and the collector currents are essentially of the same magnitude is employed.
12. A clear understanding of the procedure employed to analyze a dc transistor network will usually permit a design of the same configuration with a minimum of difficulty and confusion. Simply start with those relationships that **minimize the number of unknowns** and then proceed to make some decisions about the unknown elements of the network.
13. In a switching configuration, a transistor quickly moves between **saturation and cutoff, or vice versa**. Essentially, the impedance between collector and emitter can be approximated as a short circuit for saturation and an open circuit for cutoff.
14. When checking the operation of a dc transistor network, first check that the base-to-emitter voltage is very close to **0.7 V** and that the collector-to-emitter voltage is between **25% and 75% of the applied voltage  $V_{CC}$** .
15. The analysis of *pnp* configurations is exactly the same as that applied to *npn* transistors with the exception that current directions will **reverse** and voltages will have the **opposite polarities**.
16. Beta is very sensitive to **temperature**, and  $V_{BE}$  **decreases** about 2.5 mV (0.0025 V) for each 1° increase in temperature on a Celsius scale. The reverse saturation current typically **doubles** for every 10° increase in Celsius temperature.
17. Keep in mind that networks that are the **most stable** and least sensitive to temperature changes have the **smallest stability factors**.

## Equations

$$V_{BE} \approx 0.7 \text{ V}, \quad I_E = (\beta + 1)I_B \approx I_C, \quad I_C = \beta I_B$$

Fixed bias:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}, \quad I_C = \beta I_B$$

Emitter stabilized:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}, \quad R_i = (\beta + 1)R_E$$

Voltage-divider bias:

$$\text{Exact: } R_{Th} = R_1 \| R_2, \quad E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2}, \quad I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

*Approximate: Test*  $\beta R_E \geq 10R_2$

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}, \quad V_E = V_B - V_{BE}, \quad I_E = \frac{V_E}{R_E} \cong I_C$$

DC bias with voltage feedback:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}, \quad I'_C \cong I_C \cong I_E$$

Common base:

$$I_E = \frac{V_{EE} - V_{BE}}{R_E}, \quad I_C \cong I_E$$

Transistor switching networks:

$$I_{C_{sat}} = \frac{V_{CC}}{R_C}, \quad I_B > \frac{I_{C_{sat}}}{\beta_{dc}}, \quad R_{sat} = \frac{V_{CE_{sat}}}{I_{C_{sat}}}, \quad t_{on} = t_r + t_d, \quad t_{off} = t_s + t_f$$

$$S(I_{CO}) = \frac{\Delta I_C}{\Delta I_{CO}}, \quad S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}}, \quad S(\beta) = \frac{\Delta I_C}{\Delta \beta}$$

 $S(I_{CO})$ :

$$\text{Fixed bias: } S(I_{CO}) \cong \beta$$

$$\text{Emitter bias: } S(I_{CO}) = \frac{\beta(1 + R_B/R_E)^*}{\beta + R_B/R_E}$$

\*Voltage-divider bias: Change  $R_B$  to  $R_{Th}$  in above equation.\*Feedback bias: Change  $R_E$  to  $R_C$  in above equation. $S(V_{BE})$ :

$$\text{Fixed bias: } S(V_{BE}) = -\frac{\beta}{R_B}$$

$$\text{Emitter bias: } S(V_{BE}) = \frac{-\beta/R_E^\dagger}{\beta + R_B/R_E}$$

†Voltage-divider bias: Change  $R_B$  to  $R_{Th}$  in above equation.†Feedback bias: Change  $R_E$  to  $R_C$  in above equation. $S(\beta)$ :

$$\text{Fixed bias: } S(\beta) = \frac{I_{C_1}}{\beta_1}$$

$$\text{Emitter bias: } S(\beta) = \frac{I_{C_1}(1 + R_B/R_E)^{\ddagger}}{\beta_1(1 + \beta_2 + R_B/R_E)}$$

‡Voltage-divider bias: Change  $R_B$  to  $R_{Th}$  in above equation.‡Feedback bias: Change  $R_E$  to  $R_C$  in above equation.

## 4.21 COMPUTER ANALYSIS

### Cadence OrCAD

**Voltage-Divider Configuration** The results of Example 4.8 will now be verified using Cadence OrCAD. Using methods described in detail in the previous chapters, we can construct the network of Fig. 4.113. Recall from the previous chapter that the transistor is found under the **EVAL** library, the dc source under the **SOURCE** library, and the resistors under the **ANALOG** library. The capacitor has not been called up earlier but can also be found in the **ANALOG** library. For the transistor, the list of available transistors can be found in the **EVAL** library.

The value of beta is changed to 140 to match Example 4.8 by first clicking on the transistor symbol on the screen. It will then appear boxed in red to reveal it is in an active status. Then proceed with **Edit-PSpice Model**, and the **PSpice Model Editor Demo** dialog box will appear in which **Bf** can be changed to **140**. As you try to leave the dialog box the **Model Editor/16.3** dialog box will appear asking if you want to save the changes in the network library. Once they are saved, the screen will automatically return with beta set at its new value.

The analysis can then proceed by selecting the **New simulation profile** key (looks like a printout with an asterisk in the top left corner) to obtain the **New Simulation** dialog box. Insert Fig. 4.113 and select **Create**. The **Simulation Settings** dialog box will appear in which **Bias Point** is selected under the **Analysis Type** heading. An **OK**, and the system is ready for simulation.

Proceed by selecting the **Run PSpice** key (white arrow in green background) or the sequence **PSpice-Run**. The bias voltages will appear as shown in Fig. 4.113 if the **V** option selected. The collector-to-emitter voltage is 13.19 V – 1.333 V = 11.857 V versus 12.22 V of Example 4.8. The difference is primarily due to the fact that we are using an actual transistor whose parameters are very sensitive to the operating conditions. Also recall the difference in beta from the specification value and the value obtained from the plot of the previous chapter.

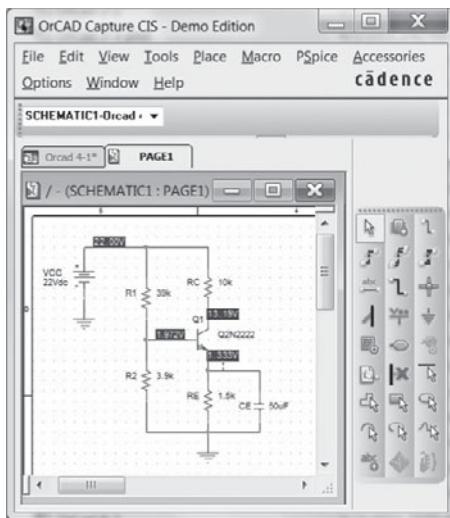


FIG. 4.113

Applying PSpice Windows to the voltage-divider configuration of Example 4.8.

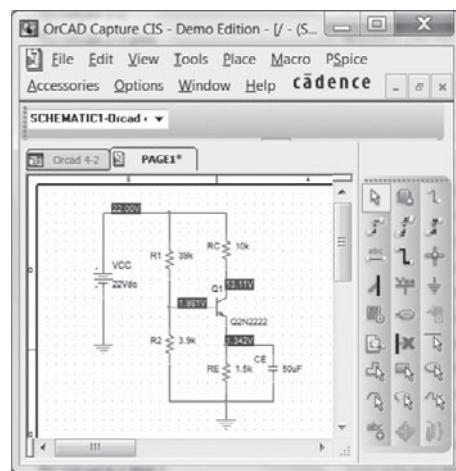


FIG. 4.114

Response obtained after changing  $\beta$  from 140 to 255.9 for the network of Fig. 4.113.

Because the voltage-divider network has a low sensitivity to changes in beta, let us return to the transistor specifications and replace beta by the default value of 255.9 and see how the results change. The result is the printout of Fig. 4.114, with voltage levels very close to those obtained in Fig. 4.113.

*Note the distinct advantage of having the network set up in memory. Any parameter can now be changed and a new solution obtained almost instantaneously—a wonderful advantage in the design process.*

**Fixed-Bias Configuration** Although the voltage-divider bias network is relatively insensitive to changes in the beta value, the fixed-bias configuration is very sensitive to beta variations. This can be demonstrated by setting up the fixed-bias configuration of Example 4.1 using a beta of 50 for the first run. The results of Fig. 4.115 demonstrate that the design is a fairly good one. The collector or collector-to-emitter voltage is appropriate for the applied source. The resulting base and collector currents are fairly common for a good design.

However, if we now go back to the transistor specifications and change beta back to the default value of 255.9, we obtain the results of Fig. 4.116. The collector voltage is now only 0.113 V at a current of 5.4 mA—a terrible operating point. Any applied ac signal would be severely truncated due to the low collector voltage.

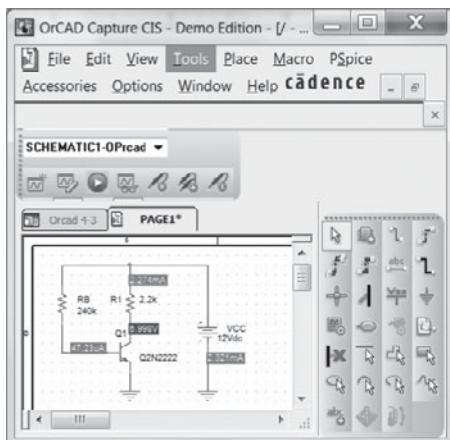


FIG. 4.115

Fixed-bias configuration with a  $\beta$  of 50.

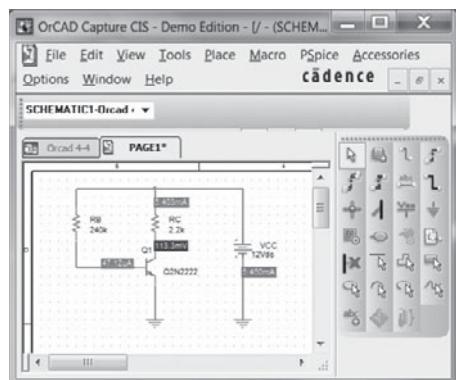


FIG. 4.116

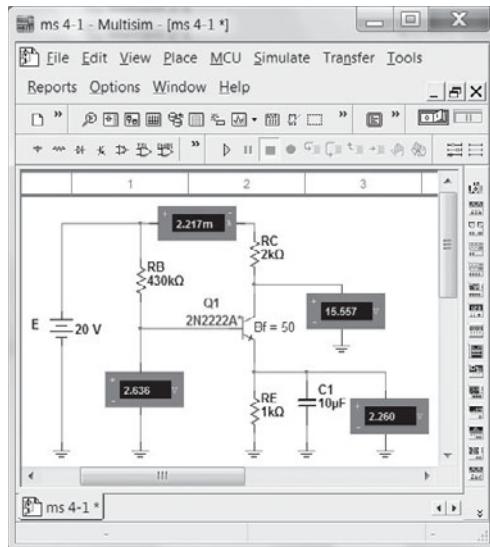
Network of Fig. 4.115 with a  $\beta$  of 255.9.

Clearly, therefore, from the preceding analysis, the voltage-divider configuration is the preferred design if there is any concern about beta variations.

## Multisim

Multisim will now be applied to the fixed-bias network of Example 4.4 to provide an opportunity to review the transistor options internal to the software package and to compare results with the handwritten approximate solution.

All the components of Fig. 4.117 except the transistor can be entered using the procedure described in Chapter 2. Transistors are available through the **Transistor** key pad, which is the fourth option down on the **Component** toolbar. When it is selected, the **Select a Component** dialog box will appear, from which **BJT\_NPN** is chosen. The result is a **Component** list, from which **2N2222A** can be selected. An **OK**, and the transistor will appear on the screen with the labels **Q1** and **2N2222A**. The label **Bf = 50** can be added by first selecting **Place** in the top toolbar followed by the **Text** option. Place the resulting marker in the area you want to place the text and click once more. The result is a blank space with a blinking marker for where the text will appear when entered. When finished, a second double-click, and the label is set. To move the label to the position shown in Fig. 4.117, simply click on the label to place the four small squares around the device. Then click it once more and drag it to the desired position. Release the clicker, and it is in place. Another click, and the four small markers will disappear.



**FIG. 4.117**  
Verifying the results of Example 4.4 using Multisim.

Even though the label may say **Bf = 50**, the transistor will still have the default parameters stored in memory. To change the parameters, the first step is to click on the device to establish the device boundaries. Then select **Edit**, followed by **Properties**, to obtain the **BJT\_NPN** dialog box. If it is not already present, select **Value** and then **Edit Model**. The result will be the **Edit Model** dialog box in which  $\beta$  and  $I_s$  can be set to 50 and 1 nA, respectively. Then choose **Change Part Model** to obtain the **BJT\_NPN** dialog box again and select **OK**. The transistor symbol on the screen will now have an asterisk to indicate that the default parameters have been modified. One more click to remove the four markers, and the transistor is set with its new parameters.

The indicators appearing in Fig. 4.117 were set as described in the previous chapter.

Finally, the network must be simulated using one of the methods described in Chapter 2. For this example the switch was set to the **1** position and then back to the **0** position after the Indicator values stabilized. The relatively low levels of current were partially responsible for the low level of this voltage.

The results are a close match with those of Example 4.4 with  $I_C = 2.217 \text{ mA}$ ,  $V_B = 2.636 \text{ V}$ ,  $V_C = 15.557 \text{ V}$ , and  $V_E = 2.26 \text{ V}$ .

The relatively few comments required here to permit the analysis of transistor networks is a clear indication that the breadth of analysis using Multisim can be expanded dramatically without having to learn a whole new set of rules—a very welcome characteristic of most technology software packages.

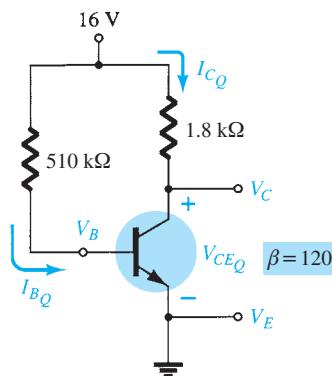
## PROBLEMS

\*Note: Asterisks indicate more difficult problems.

### 4.3 Fixed-Bias Configuration

1. For the fixed-bias configuration of Fig. 4.118, determine:

- a.  $I_{BQ}$ . **30  $\mu\text{A}$**
- b.  $I_{CQ}$ . **3.6 mA**
- c.  $V_{CEQ}$ . **9.52 V**
- d.  $V_C$ . **9.52V**
- e.  $V_B$ . **0.7V**
- f.  $V_E$ . **0 V**



**FIG. 4.118**

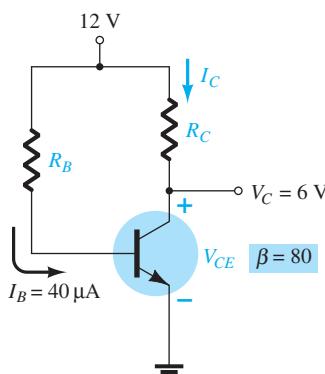
Problems 1, 4, 6, 7, 14, 65, 69, 71, and 75.

2. Given the information appearing in Fig. 4.119, determine:

- a.  $I_C$ .
- b.  $R_C$ .
- c.  $R_B$ .
- d.  $V_{CE}$ .

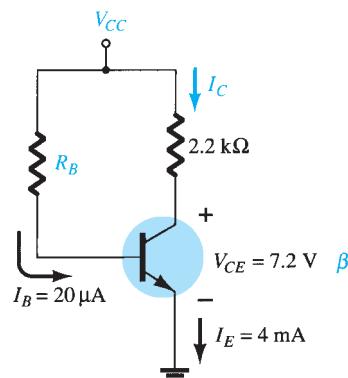
3. Given the information appearing in Fig. 4.120, determine:

- a.  $I_C$ .
- b.  $V_{CC}$ .
- c.  $\beta$ .
- d.  $R_B$ .



**FIG. 4.119**

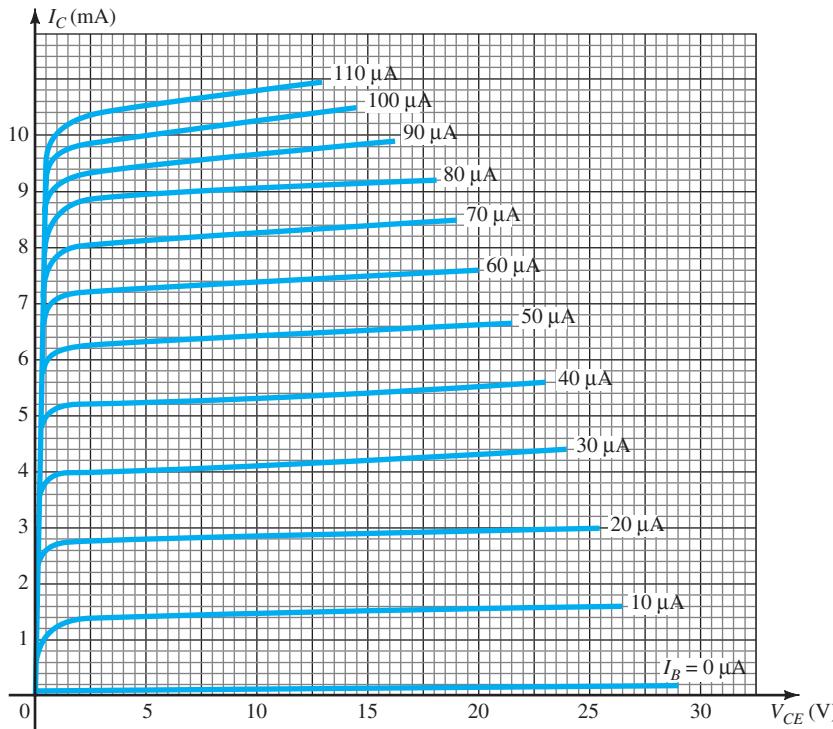
Problem 2.



**FIG. 4.120**

Problem 3.

4. Find the saturation current ( $I_{C_{\text{sat}}}$ ) for the fixed-bias configuration of Fig. 4.118.
- \*5. Given the BJT transistor characteristics of Fig. 4.121:
- Draw a load line on the characteristics determined by  $E = 21 \text{ V}$  and  $R_C = 3 \text{ k}\Omega$  for a fixed-bias configuration.
  - Choose an operating point midway between cutoff and saturation. Determine the value of  $R_B$  to establish the resulting operating point.
  - What are the resulting values of  $I_{C_Q}$  and  $V_{CE_Q}$ ?
  - What is the value of  $\beta$  at the operating point?
  - What is the value of  $\alpha$  defined by the operating point?
  - What is the saturation current ( $I_{C_{\text{sat}}}$ ) for the design?
  - Sketch the resulting fixed-bias configuration.
  - What is the dc power dissipated by the device at the operating point?
  - What is the power supplied by  $V_{CC}$ ?
  - Determine the power dissipated by the resistive elements by taking the difference between the results of parts (h) and (i).

**FIG. 4.121**

Problems 5, 6, 9, 13, 24, 44, and 57.

- a.** Ignoring the provided value of  $\beta_{(120)}$  draw the load line for the network of Fig. 4.118 on the characteristics of Fig. 4.121.
- b.** Find the  $Q$ -point and the resulting  $I_{C_Q}$  and  $V_{CE_Q}$ .
- c.** What is the beta value at this  $Q$ -point?
- If the base resistor of Fig. 4.118 is increased to  $910 \text{ k}\Omega$ , find the new  $Q$ -point and resulting values of  $I_{C_Q}$  and  $V_{CE_Q}$ .

#### 4.4 Emitter-Bias Configuration

- For the emitter-stabilized bias circuit of Fig. 4.122, determine:
  - $I_{B_Q}$ .
  - $I_{C_Q}$ .
  - $V_{CE_Q}$ .
  - $V_C$ .
  - $V_B$ .
  - $V_E$ .

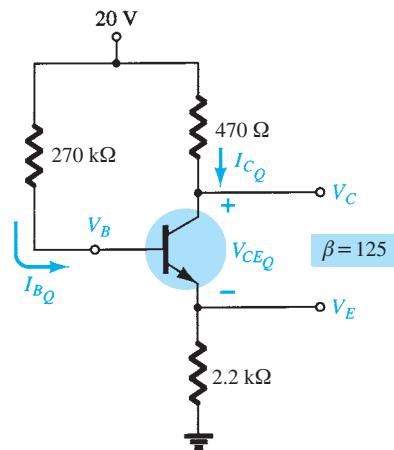


FIG. 4.122

Problems 8, 9, 12, 14, 66, 69, 72, and 76.

9. a. Draw the load line for the network of Fig. 4.122 on the characteristics of Fig. 4.121 using  $\beta$  from problem 8 to find  $I_{BQ}$ .  
 b. Find the  $Q$ -point and resulting values  $I_{CQ}$  and  $V_{CEQ}$ .  
 c. Find the value of  $\beta$  at the  $Q$ -point.  
 d. How does the value of part (c) compare with  $\beta = 125$  in problem 8?  
 e. Why are the results for problem 9 different from those of problem 8?
10. Given the information provided in Fig. 4.123, determine:  
 a.  $R_C$ .  
 b.  $R_E$ .  
 c.  $R_B$ .  
 d.  $V_{CE}$ .  
 e.  $V_B$ .
11. Given the information provided in Fig. 4.124, determine:  
 a.  $\beta$ .  
 b.  $V_{CC}$ .  
 c.  $R_B$ .

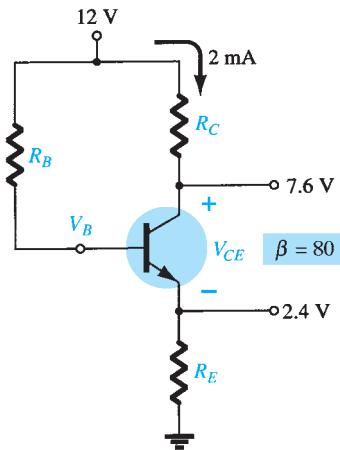


FIG. 4.123

Problem 10.

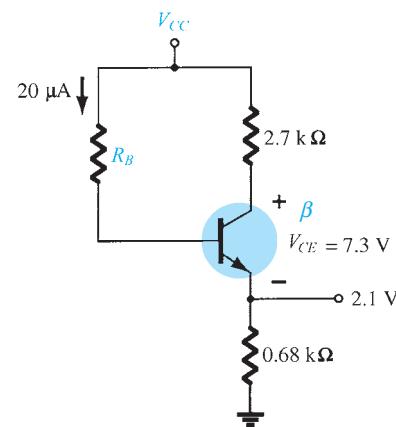


FIG. 4.124

Problem 11.

12. Determine the saturation current ( $I_{C_{sat}}$ ) for the network of Fig. 4.122.
- \*13. Using the characteristics of Fig. 4.121, determine the following for an emitter-bias configuration if a  $Q$ -point is defined at  $I_{CQ} = 4$  mA and  $V_{CEQ} = 10$  V.  
 a.  $R_C$  if  $V_{CC} = 24$  V and  $R_E = 1.2$  kΩ.  
 b.  $\beta$  at the operating point.  
 c.  $R_B$ .  
 d. Power dissipated by the transistor.  
 e. Power dissipated by the resistor  $R_C$ .

- \*14. a. Determine  $I_C$  and  $V_{CE}$  for the network of Fig. 4.118.  
 b. Change  $\beta$  to 180 and determine the new value of  $I_C$  and  $V_{CE}$  for the network of Fig. 4.118.  
 c. Determine the magnitude of the percentage change in  $I_C$  and  $V_{CE}$  using the following equations:

$$\% \Delta I_C = \left| \frac{I_{C(\text{part b})} - I_{C(\text{part a})}}{I_{C(\text{part a})}} \right| \times 100\%, \quad \% \Delta V_{CE} = \left| \frac{V_{CE(\text{part b})} - V_{CE(\text{part a})}}{V_{CE(\text{part a})}} \right| \times 100\%$$

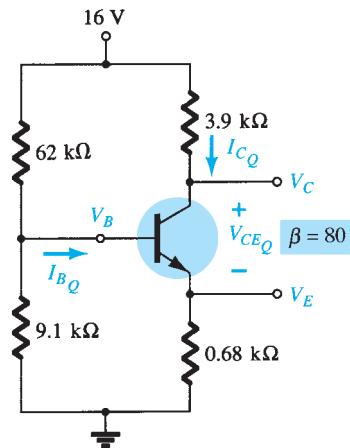
- d. Determine  $I_C$  and  $V_{CE}$  for the network of Fig. 4.122.  
 e. Change  $\beta$  to 187.5 and determine the new value of  $I_C$  and  $V_{CE}$  for the network of Fig. 4.122.  
 f. Determine the magnitude of the percentage change in  $I_C$  and  $V_{CE}$  using the following equations:

$$\% \Delta I_C = \left| \frac{I_{C(\text{part c})} - I_{C(\text{part d})}}{I_{C(\text{part d})}} \right| \times 100\%, \quad \% \Delta V_{CE} = \left| \frac{V_{CE(\text{part c})} - V_{CE(\text{part d})}}{V_{CE(\text{part d})}} \right| \times 100\%$$

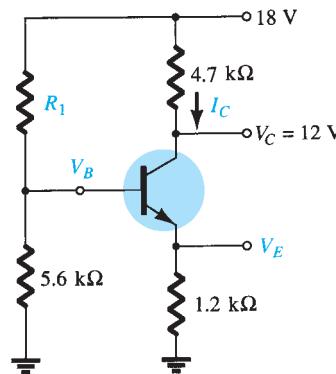
- g. In each of the above, the magnitude of  $\beta$  was increased 50%. Compare the percentage change in  $I_C$  and  $V_{CE}$  for each configuration, and comment on which seems to be less sensitive to changes in  $\beta$ .

#### 4.5 Voltage-Divider Bias Configuration

15. For the voltage-divider bias configuration of Fig. 4.125, determine:  
 a.  $I_{BQ}$ .  
 b.  $I_{CQ}$ .  
 c.  $V_{CEQ}$ .  
 d.  $V_C$ .  
 e.  $V_E$ .  
 f.  $V_B$ .
16. a. Repeat problem 15 for  $\beta = 140$  using the general approach (not the approximate).  
 b. What levels are affected the most? Why?
17. Given the information provided in Fig. 4.126, determine:  
 a.  $I_C$ .  
 b.  $V_E$ .  
 c.  $V_B$ .  
 d.  $R_1$ .



**FIG. 4.125**  
Problems 15, 16, 20, 23, 25, 67,  
69, 70, 73, and 77.



**FIG. 4.126**  
Problems 17 and 19.

18. Given the information appearing in Fig. 4.127, determine:  
 a.  $I_C$ .  
 b.  $V_E$ .  
 c.  $V_{CC}$ .  
 d.  $V_{CE}$ .  
 e.  $V_B$ .  
 f.  $R_1$ .

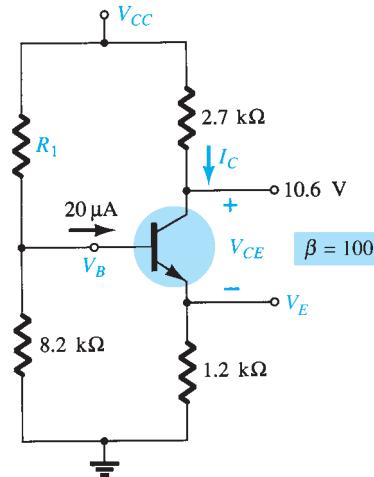


FIG. 4.127

Problem 18.

19. Determine the saturation current ( $I_{C_{\text{sat}}}$ ) for the network of Fig. 4.125.
20. a. Repeat problem 16 with  $\beta = 140$  using the approximate approach and compare results.  
b. Is the approximate approach valid?
- \*21. Determine the following for the voltage-divider configuration of Fig. 4.128 using the approximate approach if the condition established by Eq. (4.33) is satisfied.
  - a.  $I_C$ .
  - b.  $V_{CE}$ .
  - c.  $I_B$ .
  - d.  $V_E$ .
  - e.  $V_B$ .

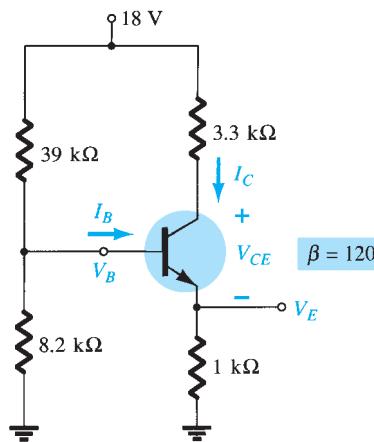


FIG. 4.128

Problems 21, 22, and 26.

- \*22. Repeat Problem 21 using the exact (Thévenin) approach and compare solutions. Based on the results, is the approximate approach a valid analysis technique if Eq. (4.33) is satisfied?
23. a. Determine  $I_{C_Q}$ ,  $V_{CE_Q}$ , and  $I_{B_Q}$  for the network of Problem 15 (Fig. 4.125) using the approximate approach even though the condition established by Eq. (4.33) is not satisfied.  
b. Determine  $I_{C_Q}$ ,  $V_{CE_Q}$ , and  $I_{B_Q}$  using the exact approach.  
c. Compare solutions and comment on whether the difference is sufficiently large to require standing by Eq. (4.33) when determining which approach to employ.
- \*24. a. Using the characteristics of Fig. 4.121, determine  $R_C$  and  $R_E$  for a voltage-divider network having a  $Q$ -point of  $I_{C_Q} = 5$  mA and  $V_{CE_Q} = 8$  V. Use  $V_{CC} = 24$  V and  $R_C = 3R_E$ .  
b. Find  $V_E$ .  
c. Determine  $V_B$ .  
d. Find  $R_2$  if  $R_1 = 24$  k $\Omega$  assuming that  $\beta R_E > 10R_2$ .  
e. Calculate  $\beta$  at the  $Q$ -point.  
f. Test Eq. (4.33), and note whether the assumption of part (d) is correct.

- \*25. a. Determine  $I_C$  and  $V_{CE}$  for the network of Fig. 4.125.  
 b. Change  $\beta$  to 120 (50% increase), and determine the new values of  $I_C$  and  $V_{CE}$  for the network of Fig. 4.125.  
 c. Determine the magnitude of the percentage change in  $I_C$  and  $V_{CE}$  using the following equations:

$$\% \Delta I_C = \left| \frac{I_{C(\text{part b})} - I_{C(\text{part a})}}{I_{C(\text{part a})}} \right| \times 100\%, \quad \% \Delta V_{CE} = \left| \frac{V_{CE(\text{part b})} - V_{CE(\text{part a})}}{V_{CE(\text{part a})}} \right| \times 100\%$$

- d. Compare the solution to part (c) with the solutions obtained for parts (c) and (f) of Problem 14.  
 e. Based on the results of part (d), which configuration is least sensitive to variations in  $\beta$ ?  
 \*26. a. Repeat parts (a) through (e) of Problem 25 for the network of Fig. 4.128. Change  $\beta$  to 180 in part (b).  
 b. What general conclusions can be made about networks in which the condition  $\beta R_E > 10R_2$  is satisfied and the quantities  $I_C$  and  $V_{CE}$  are to be determined in response to a change in  $\beta$ ?

#### 4.6 Collector-Feedback Configuration

27. For the collector-feedback configuration of Fig. 4.129, determine:

- $I_B$ .
- $I_C$ .
- $V_C$ .

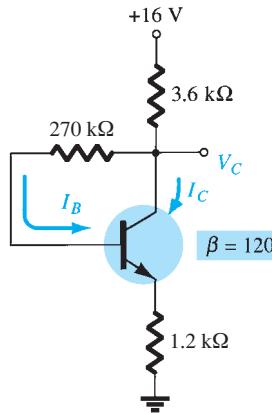


FIG. 4.129

Problems 27, 28, 74, and 78.

28. For the network of problem 27

- Determine  $I_{C_Q}$  using the equation  $I_{C_Q} \cong \frac{V'}{R'} = \frac{V_{CC} - V_{BE}}{R_C + R_E}$
- Compare with the results of problem 27 for  $I_{C_Q}$ .
- Compare  $R'$  to  $R_{F/\beta}$ .
- Is the statement valid that the larger  $R'$  is compared with  $R_{F/\beta}$ , the more accurate the equation  $I_{C_Q} \cong \frac{V'}{R'}$ ? Prove using a short derivation for the exact current  $I_{C_Q}$ .
- Repeat parts (a) and (b) for  $\beta = 240$  and comment on the new level of  $I_{C_Q}$ .

29. For the voltage feedback network of Fig. 4.130, determine:

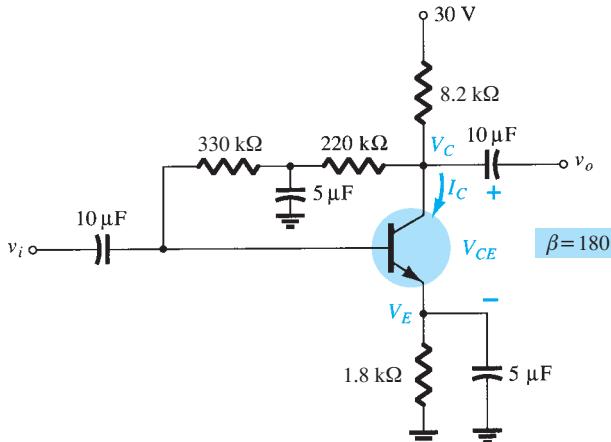
- $I_C$ .
- $V_C$ .
- $V_E$ .
- $V_{CE}$ .

30. a. Compare levels of  $R' = R_C + R_E$  to  $R_{F/\beta}$  for the network of Fig. 4.131.  
 b. Is the approximation  $I_{C_Q} \cong V'/R'$  valid?

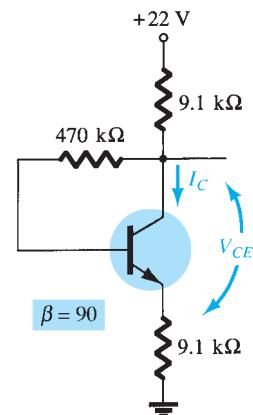
- \*31. a. Determine the levels of  $I_C$  and  $V_{CE}$  for the network of Fig. 4.131.  
 b. Change  $\beta$  to 135 (50% increase), and calculate the new levels of  $I_C$  and  $V_{CE}$ .  
 c. Determine the magnitude of the percentage change in  $I_C$  and  $V_{CE}$  using the following equations:

$$\% \Delta I_C = \left| \frac{I_{C(\text{part b})} - I_{C(\text{part a})}}{I_{C(\text{part a})}} \right| \times 100\%, \quad \% \Delta V_{CE} = \left| \frac{V_{CE(\text{part b})} - V_{CE(\text{part a})}}{V_{CE(\text{part a})}} \right| \times 100\%$$

- d. Compare the results of part (c) with those of Problems 14(c), 14(f), and 25(c). How does the collector-feedback network stack up against the other configurations in sensitivity to changes in  $\beta$ ?



**FIG. 4.130**  
Problems 29 and 30.

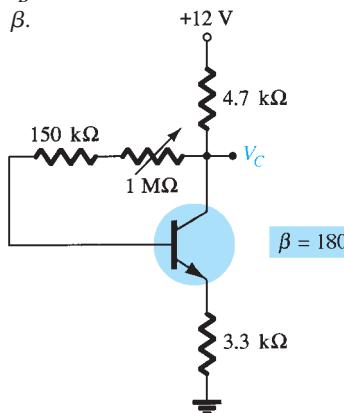


**FIG. 4.131**  
Problems 30 and 31.

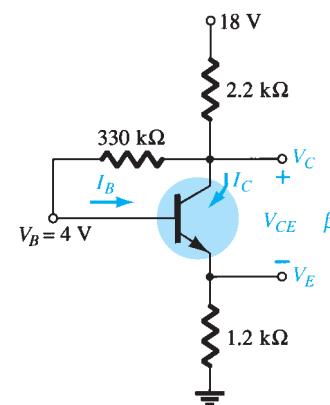
32. Determine the range of possible values for  $V_C$  for the network of Fig. 4.132 using the 1-MΩ potentiometer.

\*33. Given  $V_B = 4$  V for the network of Fig. 4.133, determine:

- $V_E$ .
- $I_C$ .
- $V_C$ .
- $V_{CE}$ .
- $I_B$ .
- $\beta$ .



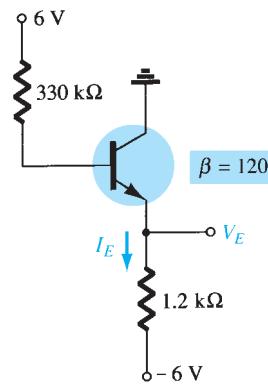
**FIG. 4.132**  
Problem 32.



**FIG. 4.133**  
Problem 33.

#### 4.7 Emitter-Follower Configuration

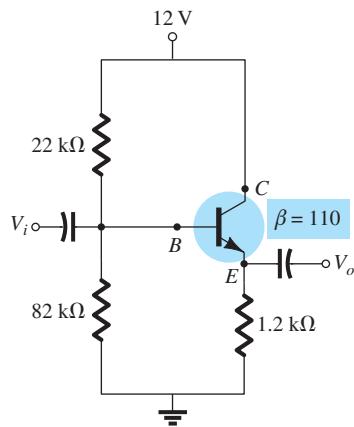
\*34. Determine the level of  $V_E$  and  $I_E$  for the network of Fig. 4.134.



**FIG. 4.134**  
Problem 34.

35. For the emitter follower network of Fig. 4.135

- Find  $I_B$ ,  $I_C$ , and  $I_E$ .
- Determine  $V_B$ ,  $V_C$ , and  $V_E$ .
- Calculate  $V_{BC}$  and  $V_{CE}$ .



**FIG. 4.135**  
Problem 35.

#### 4.8 Common-Base Configuration

- \*36. For the network of Fig. 4.136, determine:

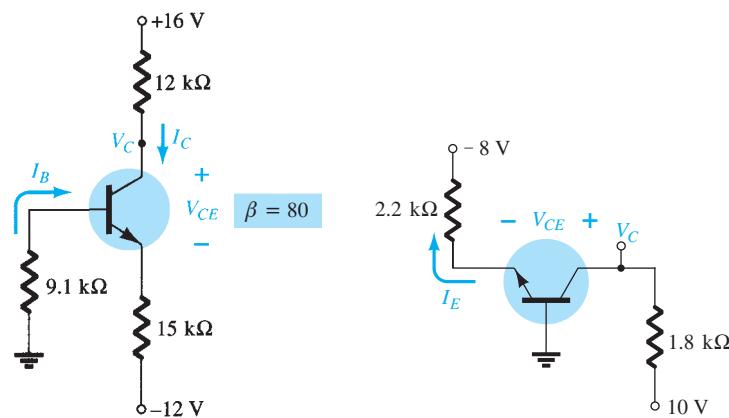
- $I_B$ .
- $I_C$ .
- $V_{CE}$ .
- $V_C$ .

- \*37. For the network of Fig. 4.137, determine:

- $I_E$ .
- $V_C$ .
- $V_{CE}$ .

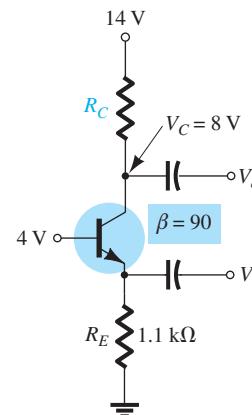
38. For the common-base network of Fig. 4.138

- Using the information provided determine the value of  $R_C$ .
- Find the currents  $I_B$  and  $I_E$ .
- Determine the voltages  $V_{BC}$  and  $V_{CE}$ .



**FIG. 4.136**  
Problem 36.

**FIG. 4.137**  
Problem 37.



**FIG. 4.138**  
Problem 38.

#### 4.9 Miscellaneous Bias Configurations

- \*39. For the network of Fig. 4.139, determine:

- $I_B$ .
- $I_C$ .
- $V_E$ .
- $V_{CE}$ .

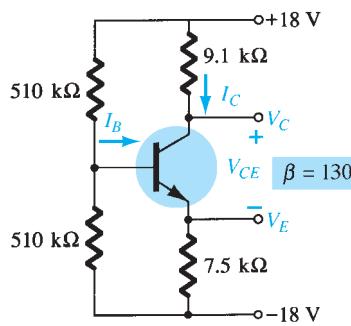


FIG. 4.139

Problem 39.

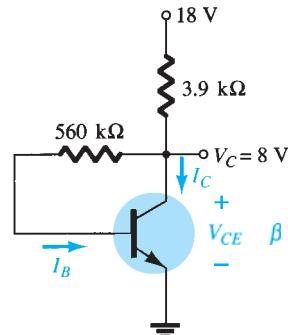


FIG. 4.140

Problems 40 and 68.

40. Given  $V_C = 8$  V for the network of Fig. 4.140, determine:

- $I_B$ .
- $I_C$ .
- $\beta$ .
- $V_{CE}$ .

#### 4.11 Design Operations

41. Determine  $R_C$  and  $R_B$  for a fixed-bias configuration if  $V_{CC} = 12$  V,  $\beta = 80$ , and  $I_{CQ} = 2.5$  mA with  $V_{CEQ} = 6$  V. Use standard values.
42. Design an emitter-stabilized network at  $I_{CQ} = \frac{1}{2}I_{C\text{sat}}$  and  $V_{CEQ} = \frac{1}{2}V_{CC}$ . Use  $V_{CC} = 20$  V,  $I_{C\text{sat}} = 10$  mA,  $\beta = 120$ , and  $R_C = 4R_E$ . Use standard values.
43. Design a voltage-divider bias network using a supply of 24 V, a transistor with a beta of 110, and an operating point of  $I_{CQ} = 4$  mA and  $V_{CEQ} = 8$  V. Choose  $V_E = \frac{1}{8}V_{CC}$ . Use standard values.
- \*44. Using the characteristics of Fig. 4.121, design a voltage-divider configuration to have a saturation level of 10 mA and a  $Q$ -point one-half the distance between cutoff and saturation. The available supply is 28 V, and  $V_E$  is to be one-fifth of  $V_{CC}$ . The condition established by Eq. (4.33) should also be met to provide a high stability factor. Use standard values.

#### 4.12 Multiple BJT Networks

45. For the  $R-C$ -coupled amplifier of Fig. 4.141 determine
- the voltages  $V_B$ ,  $V_C$ , and  $V_E$  for each transistor.
  - the currents  $I_B$ ,  $I_C$ , and  $I_E$  for each transistor

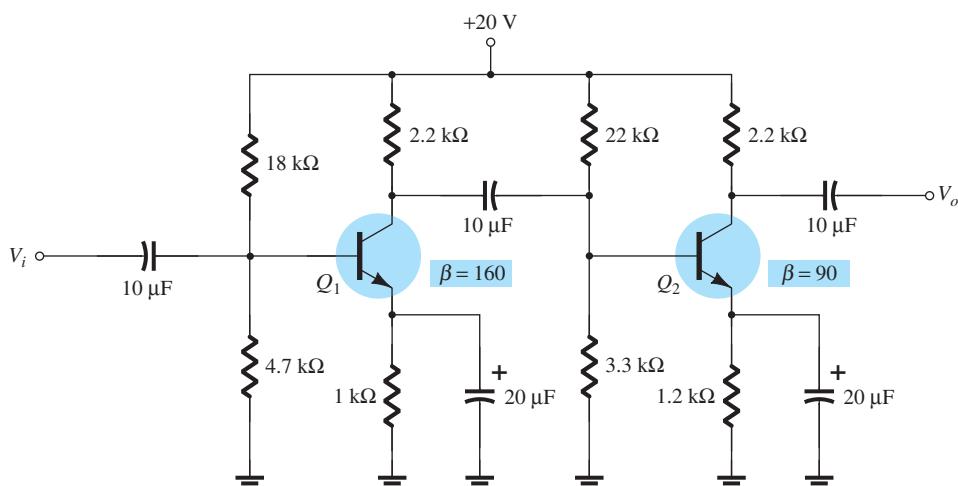
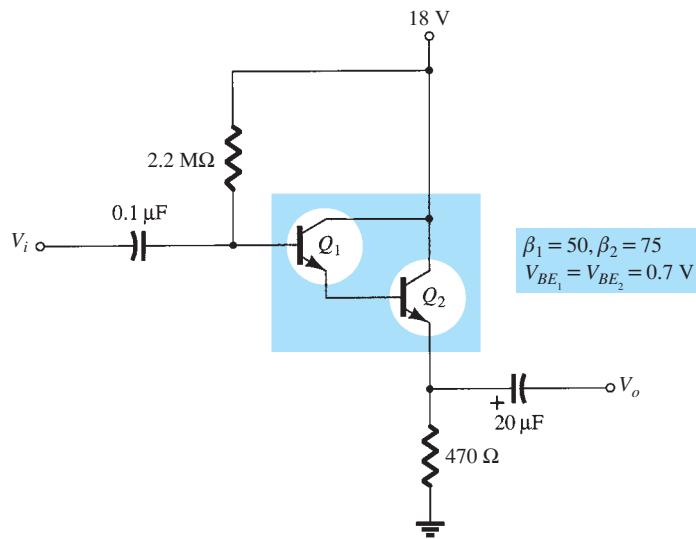


FIG. 4.141

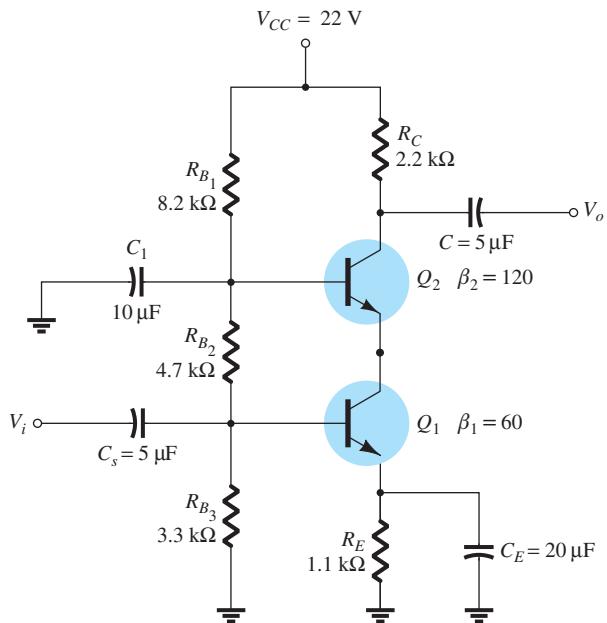
Problem 45.

46. For the Darlington amplifier of Fig. 4.142 determine
- the level of  $\beta_D$ .
  - the base current of each transistor.
  - the collector current of each transistor.
  - the voltages  $V_{C_1}$ ,  $V_{C_2}$ ,  $V_{E_1}$ , and  $V_{E_2}$ .



**FIG. 4.142**  
Problem 46.

47. For the cascode amplifier of Fig. 4.143 determine  
 a. the base and collector currents of each transistor.  
 b. the voltages  $V_{B1}$ ,  $V_{B2}$ ,  $V_{E1}$ ,  $V_{C1}$ ,  $V_{E2}$ , and  $V_{C2}$ .

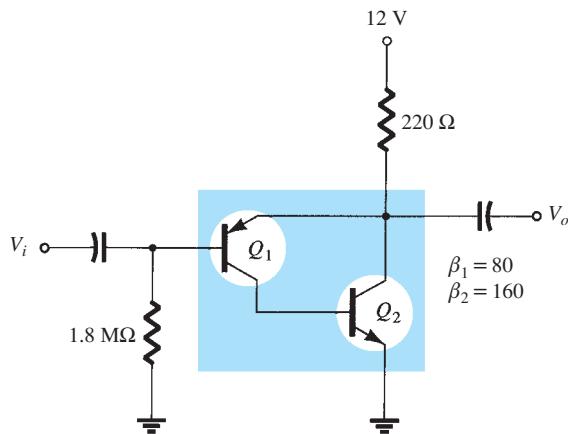


**FIG. 4.143**  
Problem 47.

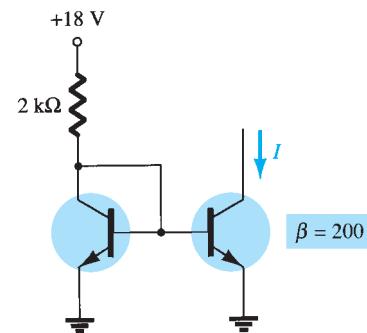
48. For the feedback amplifier of Fig. 4.144 determine  
 a. the base and collector current of each transistor.  
 b. the base, emitter, and collector voltages of each transistor.

#### 4.13 Current Mirror Circuits

49. Calculate the mirrored current  $I$  in the circuit of Fig. 4.145.

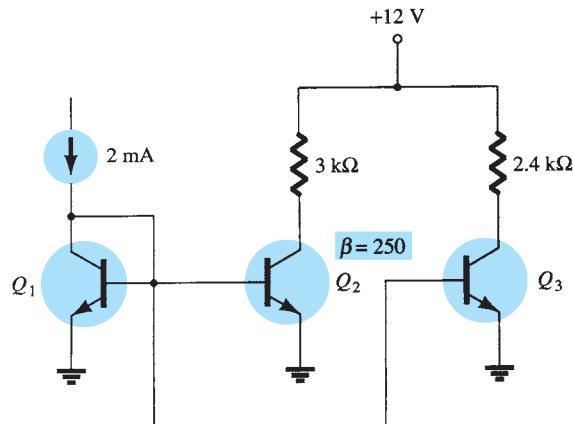
**FIG. 4.144**

Problem 48.

**FIG. 4.145**

Problem 49.

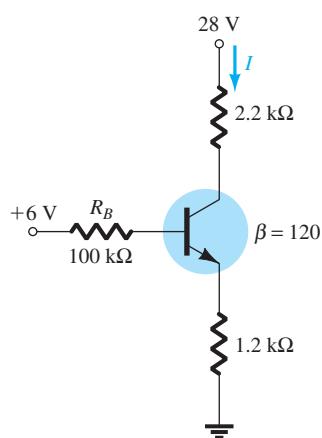
- \*50. Calculate collector currents for  $Q_1$  and  $Q_2$  in Fig. 4.146.

**FIG. 4.146**

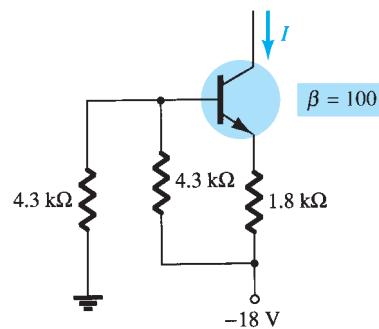
Problem 50.

#### 4.14 Current Source Circuits

51. Calculate the current through the  $2.2\text{-k}\Omega$  load in the circuit of Fig. 4.147.  
52. For the circuit of Fig. 4.148, calculate the current  $I$ .

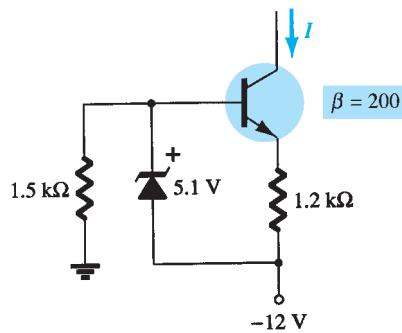
**FIG. 4.147**

Problem 51.

**FIG. 4.148**

Problem 52.

\*53. Calculate the current  $I$  in the circuit of Fig. 4.149.



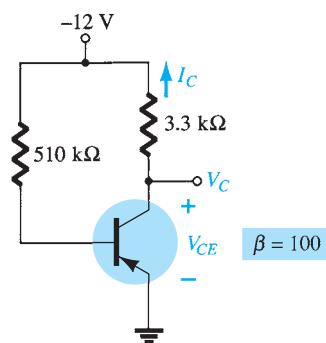
**FIG. 4.149**

Problem 53.

#### 4.15 pnp Transistors

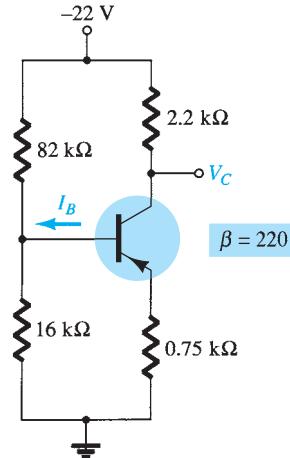
54. Determine  $V_C$ ,  $V_{CE}$ , and  $I_C$  for the network of Fig. 4.150.

55. Determine  $V_C$  and  $I_B$  for the network of Fig. 4.151.



**FIG. 4.150**

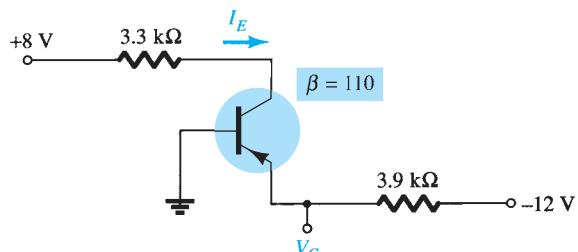
Problem 54.



**FIG. 4.151**

Problem 55.

56. Determine  $I_E$  and  $V_C$  for the network of Fig. 4.152.

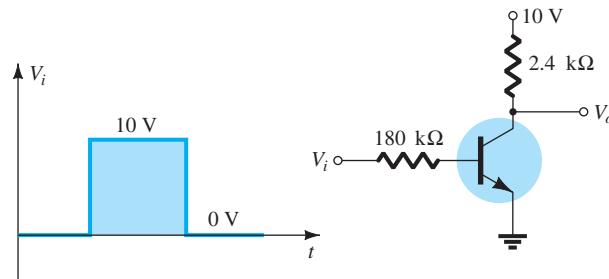


**FIG. 4.152**

Problem 56.

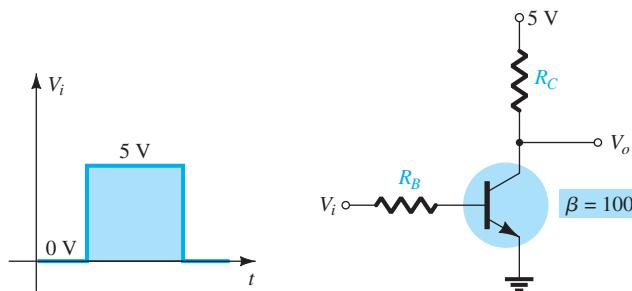
#### 4.16 Transistor Switching Networks

\*57. Using the characteristics of Fig. 4.121, determine the appearance of the output waveform for the network of Fig. 4.153. Include the effects of  $V_{CE,\text{sat}}$ , and determine  $I_B$ ,  $I_{B,\text{max}}$ , and  $I_{C,\text{sat}}$  when  $V_i = 10$  V. Determine the collector-to-emitter resistance at saturation and cutoff.



**FIG. 4.153**  
Problem 57.

- \*58. Design the transistor inverter of Fig. 4.154 to operate with a saturation current of 8 mA using a transistor with a beta of 100. Use a level of  $I_B$  equal to 120% of  $I_{B_{\max}}$  and standard resistor values.

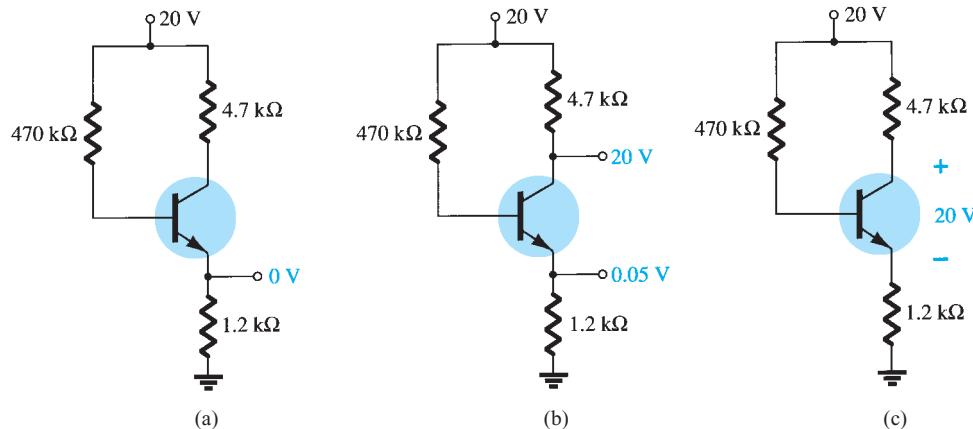


**FIG. 4.154**  
Problem 58.

59. a. Using the characteristics of Fig. 3.23e, determine  $t_{on}$  and  $t_{off}$  at a current of 2 mA. Note the use of log scales and the possible need to refer to Section 9.2.  
 b. Repeat part (a) at a current of 10 mA. How have  $t_{on}$  and  $t_{off}$  changed with increase in collector current?  
 c. For parts (a) and (b), sketch the pulse waveform of Fig. 4.91 and compare results.

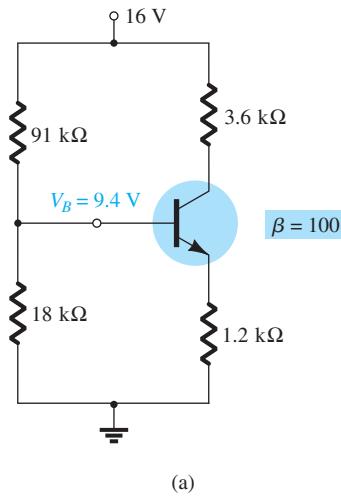
#### 4.17 Troubleshooting Techniques

- \*60. The measurements of Fig. 4.155 all reveal that the network is not functioning correctly. List as many reasons as you can for the measurements obtained.

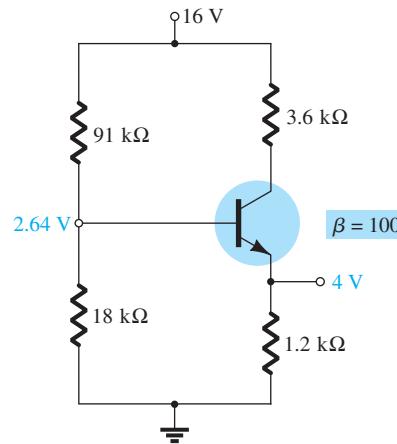


**FIG. 4.155**  
Problem 60.

- \*61. The measurements appearing in Fig. 4.156 reveal that the networks are not operating properly. Be specific in describing why the levels obtained reflect a problem with the expected network behavior. In other words, the levels obtained reflect a very specific problem in each case.



(a)



(b)

**FIG. 4.156**  
Problem 61.

62. For the circuit of Fig. 4.157:

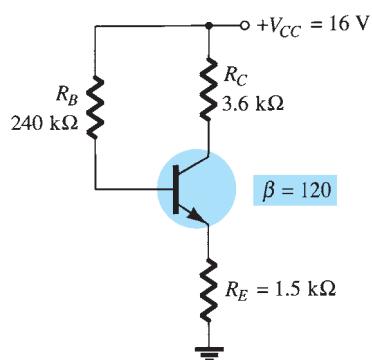
- Does  $V_C$  increase or decrease if  $R_B$  is increased?
- Does  $I_C$  increase or decrease if  $\beta$  is reduced?
- What happens to the saturation current if  $\beta$  is increased?
- Does the collector current increase or decrease if  $V_{CC}$  is reduced?
- What happens to  $V_{CE}$  if the transistor is replaced by one with smaller  $\beta$ ?

63. Answer the following questions about the circuit of Fig. 4.158:

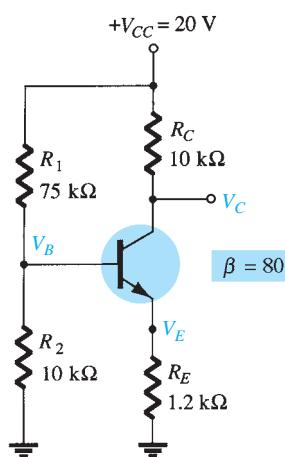
- What happens to the voltage  $V_C$  if the transistor is replaced by one having a larger value of  $\beta$ ?
- What happens to the voltage  $V_{CE}$  if the ground leg of resistor  $R_{B_2}$  opens (does not connect to ground)?
- What happens to  $I_C$  if the supply voltage is low?
- What voltage  $V_{CE}$  would occur if the transistor base-emitter junction fails by becoming open?
- What voltage  $V_{CE}$  would result if the transistor base-emitter junction fails by becoming a short?

\*64. Answer the following questions about the circuit of Fig. 4.159:

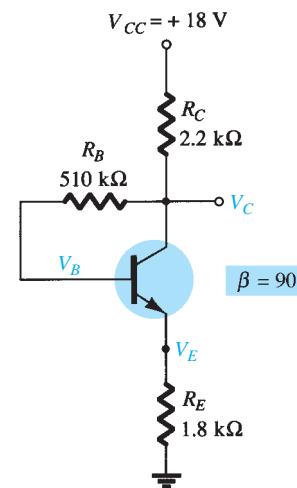
- What happens to the voltage  $V_C$  if the resistor  $R_B$  is open?
- What should happen to  $V_{CE}$  if  $\beta$  increases due to temperature?
- How will  $V_E$  be affected when replacing the collector resistor with one whose resistance is at the lower end of the tolerance range?
- If the transistor collector connection becomes open, what will happen to  $V_E$ ?
- What might cause  $V_{CE}$  to become nearly 18 V?



**FIG. 4.157**  
Problem 62.



**FIG. 4.158**  
Problem 63.



**FIG. 4.159**  
Problem 64.

**4.18 Bias Stabilization**

- 65.** Determine the following for the network of Fig. 4.118:
- $S(I_{CO})$ .
  - $S(V_{BE})$ .
  - $S(\beta)$ , using  $T_1$  as the temperature at which the parameter values are specified and  $\beta(T_2)$  as 25% more than  $\beta(T_1)$ .
  - Determine the net change in  $I_C$  if a change in operating conditions results in  $I_{CO}$  increasing from  $0.2 \mu\text{A}$  to  $10 \mu\text{A}$ ,  $V_{BE}$  drops from  $0.7 \text{ V}$  to  $0.5 \text{ V}$ , and  $\beta$  increases 25%.
- \*66.** For the network of Fig. 4.122, determine:
- $S(I_{CO})$ .
  - $S(V_{BE})$ .
  - $S(\beta)$ , using  $T_1$  as the temperature at which the parameter values are specified and  $\beta(T_2)$  as 25% more than  $\beta(T_1)$ .
  - Determine the net change in  $I_C$  if a change in operating conditions results in  $I_{CO}$  increasing from  $0.2 \mu\text{A}$  to  $10 \mu\text{A}$ ,  $V_{BE}$  drops from  $0.7 \text{ V}$  to  $0.5 \text{ V}$ , and  $\beta$  increases 25%.
- \*67.** For the network of Fig. 4.125, determine:
- $S(I_{CO})$ .
  - $S(V_{BE})$ .
  - $S(\beta)$ , using  $T_1$  as the temperature at which the parameter values are specified and  $\beta(T_2)$  as 25% more than  $\beta(T_1)$ .
  - Determine the net change in  $I_C$  if a change in operating conditions results in  $I_{CO}$  increasing from  $0.2 \mu\text{A}$  to  $10 \mu\text{A}$ ,  $V_{BE}$  drops from  $0.7 \text{ V}$  to  $0.5 \text{ V}$ , and  $\beta$  increases 25%.
- \*68.** For the network of Fig. 4.140, determine:
- $S(I_{CO})$ .
  - $S(V_{BE})$ .
  - $S(\beta)$ , using  $T_1$  as the temperature at which the parameter values are specified and  $\beta(T_2)$  as 25% more than  $\beta(T_1)$ .
  - Determine the net change in  $I_C$  if a change in operating conditions results in  $I_{CO}$  increasing from  $0.2 \mu\text{A}$  to  $10 \mu\text{A}$ ,  $V_{BE}$  drops from  $0.7 \text{ V}$  to  $0.5 \text{ V}$ , and  $\beta$  increases 25%.
- \*69.** Compare the relative values of stability for Problems 65 through 68. The results for Exercises 65 and 67 can be found in Appendix E. Can any general conclusions be derived from the results?
- \*70.** **a.** Compare the levels of stability for the fixed-bias configuration of Problem 65.  
**b.** Compare the levels of stability for the voltage-divider configuration of Problem 67.  
**c.** Which factors of parts (a) and (b) seem to have the most influence on the stability of the system, or is there no general pattern to the results?

**4.21 Computer Analysis**

- 71.** Perform a PSpice analysis of the network of Fig. 4.118. That is, determine  $I_C$ ,  $V_{CE}$ , and  $I_B$ .
- 72.** Repeat Problem 71 for the network of Fig. 4.122.
- 73.** Repeat Problem 71 for the network of Fig. 4.125.
- 74.** Repeat Problem 71 for the network of Fig. 4.129.
- 75.** Repeat Problem 71 using Multisim.
- 76.** Repeat Problem 72 using Multisim.
- 77.** Repeat Problem 73 using Multisim.
- 78.** Repeat Problem 74 using Multisim.

# 5

## BJT AC Analysis

### CHAPTER OBJECTIVES

- Become familiar with the  $r_e$ , hybrid, and hybrid  $\pi$  models for the BJT transistor.
- Learn to use the equivalent model to find the important ac parameters for an amplifier.
- Understand the effects of a source resistance and load resistor on the overall gain and characteristics of an amplifier.
- Become aware of the general ac characteristics of a variety of important BJT configurations.
- Begin to understand the advantages associated with the two-port systems approach to single- and multistage amplifiers.
- Develop some skill in troubleshooting ac amplifier networks.

### 5.1 INTRODUCTION

The basic construction, appearance, and characteristics of the transistor were introduced in Chapter 3. The dc biasing of the device was then examined in detail in Chapter 4. We now begin to examine the ac response of the BJT amplifier by reviewing the *models* most frequently used to represent the transistor in the sinusoidal ac domain.

One of our first concerns in the sinusoidal ac analysis of transistor networks is the magnitude of the input signal. It will determine whether *small-signal* or *large-signal* techniques should be applied. There is no set dividing line between the two, but the application—and the magnitude of the variables of interest relative to the scales of the device characteristics—will usually make it quite clear which method is appropriate. The small-signal technique is introduced in this chapter, and large-signal applications are examined in Chapter 12.

There are three models commonly used in the small-signal ac analysis of transistor networks: the  $r_e$  model, the hybrid  $\pi$  model, and the hybrid equivalent model. This chapter introduces all three but emphasizes the  $r_e$  model.

### 5.2 AMPLIFICATION IN THE AC DOMAIN

It was demonstrated in Chapter 3 that the transistor can be employed as an amplifying device. That is, the output sinusoidal signal is greater than the input sinusoidal signal, or, stated another way, the output ac power is greater than the input ac power. The question then arises as to how the ac power output can be greater than the input ac power. Conservation of energy dictates that over time the total power output,  $P_o$ , of a system cannot be greater than its power

input,  $P_i$ , and that the efficiency defined by  $\eta = P_o/P_i$  cannot be greater than 1. The factor missing from the discussion above that permits an ac power output greater than the input ac power is the applied dc power. It is the principal contributor to the total output power even though part of it is dissipated by the device and resistive elements. In other words, there is an “exchange” of dc power to the ac domain that permits establishing a higher output ac power. In fact, a *conversion efficiency* is defined by  $\eta = P_{o(ac)}/P_{i(dc)}$ , where  $P_{o(ac)}$  is the ac power to the load and  $P_{i(dc)}$  is the dc power supplied.

Perhaps the role of the dc supply can best be described by first considering the simple dc network of Fig. 5.1. The resulting direction of flow is indicated in the figure with a plot of the current  $i$  versus time. Let us now insert a control mechanism such as that shown in Fig. 5.2. The control mechanism is such that the application of a relatively small signal to the control mechanism can result in a substantial oscillation in the output circuit.

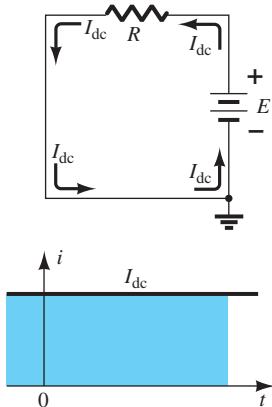


FIG. 5.1

Steady current established by a dc supply.

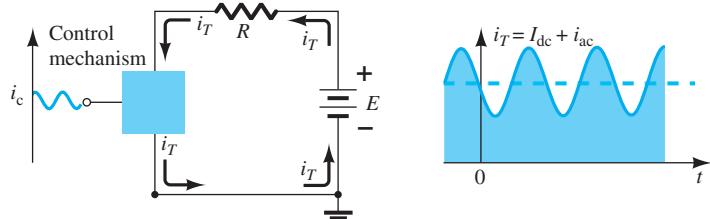


FIG. 5.2

Effect of a control element on the steady-state flow of the electrical system of Fig. 5.1.

That is, for this example,

$$i_{ac(p-p)} \gg i_{c(p-p)}$$

and amplification in the ac domain has been established. The peak-to-peak value of the output current far exceeds that of the control current.

For the system of Fig. 5.2, the peak value of the oscillation in the output circuit is controlled by the established dc level. Any attempt to exceed the limit set by the dc level will result in a “clipping” (flattening) of the peak region at the high and low end of the output signal. In general, therefore, proper amplification design requires that the dc and ac components be sensitive to each other’s requirements and limitations.

However, it is extremely helpful to realize that:

**The superposition theorem is applicable for the analysis and design of the dc and ac components of a BJT network, permitting the separation of the analysis of the dc and ac responses of the system.**

In other words, one can make a complete dc analysis of a system before considering the ac response. Once the dc analysis is complete, the ac response can be determined using a completely ac analysis. It happens, however, that one of the components appearing in the ac analysis of BJT networks will be determined by the dc conditions, so there is still an important link between the two types of analysis.

### 5.3 BJT TRANSISTOR MODELING

The key to transistor small-signal analysis is the use of the equivalent circuits (models) to be introduced in this chapter.

**A model is a combination of circuit elements, properly chosen, that best approximates the actual behavior of a semiconductor device under specific operating conditions.**

Once the ac equivalent circuit is determined, the schematic symbol for the device can be replaced by this equivalent circuit and the basic methods of circuit analysis applied to determine the desired quantities of the network.

In the formative years of transistor network analysis the *hybrid equivalent network* was employed the most frequently. Specification sheets included the parameters in their listing, and analysis was simply a matter of inserting the equivalent circuit with the listed values.

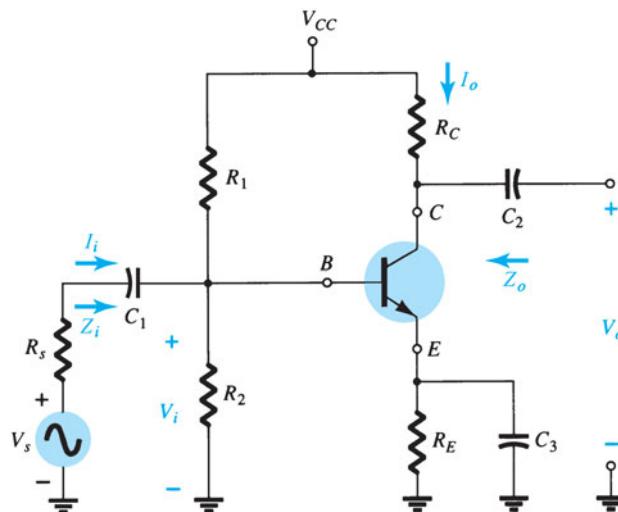
The drawback to using this equivalent circuit, however, is that it is *defined for a set of operating conditions that might not match the actual operating conditions*. In most cases, this is not a serious flaw because the actual operating conditions are relatively close to the chosen operating conditions on the data sheets. In addition, there is always a variation in actual resistor values and given transistor beta values, so as an approximate approach it was quite reliable. Manufacturers continue to specify the hybrid parameter values for a particular operating point on their specification sheets. They really have no choice. They want to give the user some idea of the value of each important parameter so comparisons can be made between transistors, but they really do not know the user's actual operating conditions.

In time the use of the  $r_e$  model became the more desirable approach because an important parameter of the equivalent circuit was determined by the actual operating conditions rather than using a data sheet value that in some cases could be quite different. Unfortunately, however, one must still turn to the data sheets for some of the other parameters of the equivalent circuit. The  $r_e$  model also failed to include a feedback term, which in some cases can be important if not simply troublesome.

The  $r_e$  model is really a reduced version of the *hybrid  $\pi$  model* used almost exclusively for high-frequency analysis. This model also includes a connection between output and input to include the feedback effect of the output voltage and the input quantities. The full hybrid model is introduced in Chapter 9.

Throughout the text the  $r_e$  model is the model of choice unless the discussion centers on the description of each model or a region of examination that predetermines the model that should be used. Whenever possible, however, a comparison between models will be discussed to show how closely related they really are. It is also important that once you gain a proficiency with one model it will carry over to an investigation using a different model, so moving from one to another will not be a dramatic undertaking.

In an effort to demonstrate the effect that the ac equivalent circuit will have on the analysis to follow, consider the circuit of Fig. 5.3. Let us assume for the moment that the small-signal ac equivalent circuit for the transistor has already been determined. Because we are interested only in the ac response of the circuit, all the dc supplies can be replaced by a zero-potential equivalent (short circuit) because they determine only the dc (quiescent level) of the output voltage and not the magnitude of the swing of the ac output. This is clearly demonstrated by Fig. 5.4. The dc levels were simply important for determining the proper  $Q$ -point of operation. Once determined, the dc levels can be ignored in the ac analysis of the network. In addition, the coupling capacitors  $C_1$  and  $C_2$  and bypass capacitor  $C_3$  were chosen to have a very small reactance at the frequency of application. Therefore, they, too, may for all practical purposes be replaced by a low-resistance path or a short circuit. Note that this will result in the "shorting out" of the dc biasing resistor  $R_E$ . Recall that capacitors assume an "open-circuit" equivalent under dc steady-state conditions, permitting an isolation between stages for the dc levels and quiescent conditions.



**FIG. 5.3**  
Transistor circuit under examination in this introductory discussion.

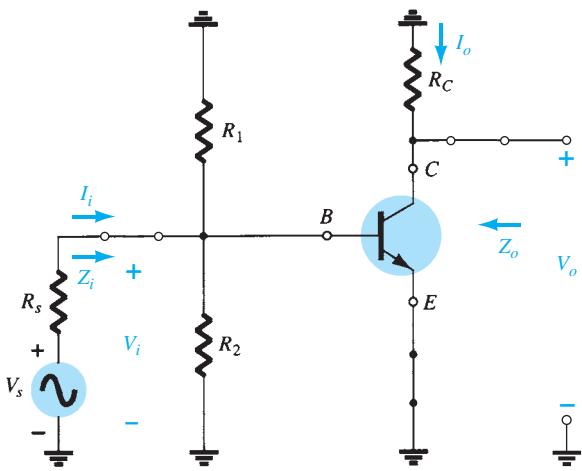


FIG. 5.4

The network of Fig. 5.3 following removal of the dc supply and insertion of the short-circuit equivalent for the capacitors.

It is important as you progress through the modifications of the network to define the ac equivalent that the parameters of interest such as  $Z_i$ ,  $Z_o$ ,  $I_i$ , and  $I_o$  as defined by Fig. 5.5 be carried through properly. Even though the network appearance may change, you want to be sure the quantities you find in the reduced network are the same as defined by the original network. In both networks the input impedance is defined from base to ground, the input current as the base current of the transistor, the output voltage as the voltage from collector to ground, and the output current as the current through the load resistor  $R_C$ .

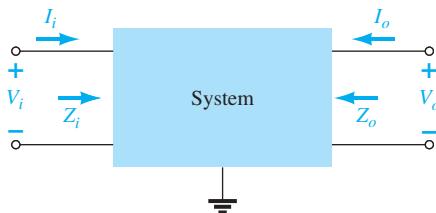


FIG. 5.5

Defining the important parameters of any system.

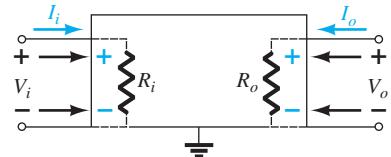


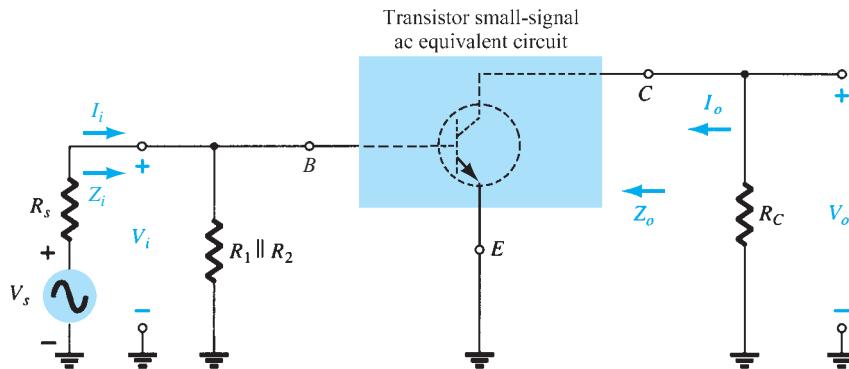
FIG. 5.6

Demonstrating the reason for the defined directions and polarities.

The parameters of Fig. 5.5 can be applied to any system whether it has one or a thousand components. For all the analysis to follow in this text, the directions of the currents, the polarities of the voltages, and the direction of interest for the impedance levels are as appearing in Fig. 5.5. In other words, the input current  $I_i$  and output current  $I_o$  are, by definition, defined to enter the system. If, in a particular example, the output current is leaving the system rather than entering the system as shown in Fig. 5.5, a minus sign must be applied. The defined polarities for the input and output voltages are also as appearing in Fig. 5.5. If  $V_o$  has the opposite polarity, the minus sign must be applied. Note that  $Z_i$  is the impedance "looking into" the system, whereas  $Z_o$  is the impedance "looking back into" the system from the output side. By choosing the defined directions for the currents and voltages as appearing in Fig. 5.5, both the input impedance and output impedance are defined as having positive values. For example, in Fig. 5.6 the input and output impedances for a particular system are both resistive. For the direction of  $I_i$  and  $I_o$  the resulting voltage across the resistive elements will have the same polarity as  $V_i$  and  $V_o$ , respectively. If  $I_o$  had been defined as the opposite direction in Fig. 5.5 a minus sign would have to be applied. For each case  $Z_i = V_i/I_i$  and  $Z_o = V_o/I_o$  with positive results if they all have the defined directions and polarity of Fig. 5.5. If the output current of an actual system has a direction opposite to that

of Fig. 5.5 a minus sign must be applied to the result because  $V_o$  must be defined as appearing in Fig. 5.5. Keep Fig. 5.5 in mind as you analyze the BJT networks in this chapter. It is an important introduction to “System Analysis,” which is becoming so important with the expanded use of packaged IC systems.

If we establish a common ground and rearrange the elements of Fig. 5.4,  $R_1$  and  $R_2$  will be in parallel, and  $R_C$  will appear from collector to emitter as shown in Fig. 5.7. Because the components of the transistor equivalent circuit appearing in Fig. 5.7 employ familiar components such as resistors and independent controlled sources, analysis techniques such as superposition, Thévenin’s theorem, and so on, can be applied to determine the desired quantities.



**FIG. 5.7**  
Circuit of Fig. 5.4 redrawn for small-signal ac analysis.

Let us further examine Fig. 5.7 and identify the important quantities to be determined for the system. Because we know that the transistor is an amplifying device, we would expect some indication of how the output voltage  $V_o$  is related to the input voltage  $V_i$ —the *voltage gain*. Note in Fig. 5.7 for this configuration that the *current gain* is defined by  $A_i = I_o/I_i$ .

In summary, therefore, the ac equivalent of a transistor network is obtained by:

1. *Setting all dc sources to zero and replacing them by a short-circuit equivalent*
2. *Replacing all capacitors by a short-circuit equivalent*
3. *Removing all elements bypassed by the short-circuit equivalents introduced by steps 1 and 2*
4. *Redrawing the network in a more convenient and logical form*

In the sections to follow, a transistor equivalent model will be introduced to complete the ac analysis of the network of Fig. 5.7.

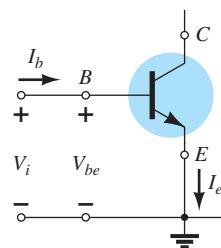
## 5.4 THE $r_e$ TRANSISTOR MODEL

The  $r_e$  model for the CE, CB, and CC BJT transistor configurations will now be introduced with a short description of why each is a good approximation to the actual behavior of a BJT transistor.

### Common-Emitter Configuration

The equivalent circuit for the common-emitter configuration will be constructed using the device characteristics and a number of approximations. Starting with the input side, we find the applied voltage  $V_i$  is equal to the voltage  $V_{be}$  with the input current being the base current  $I_b$  as shown in Fig. 5.8.

Recall from Chapter 3 that because the current through the forward-biased junction of the transistor is  $I_E$ , the characteristics for the input side appear as shown in Fig. 5.9a for various levels of  $V_{BE}$ . Taking the average value for the curves of Fig. 5.9a will result in the single curve of Fig. 5.9b, which is simply that of a forward-biased diode.



**FIG. 5.8**  
Finding the input equivalent circuit for a BJT transistor.

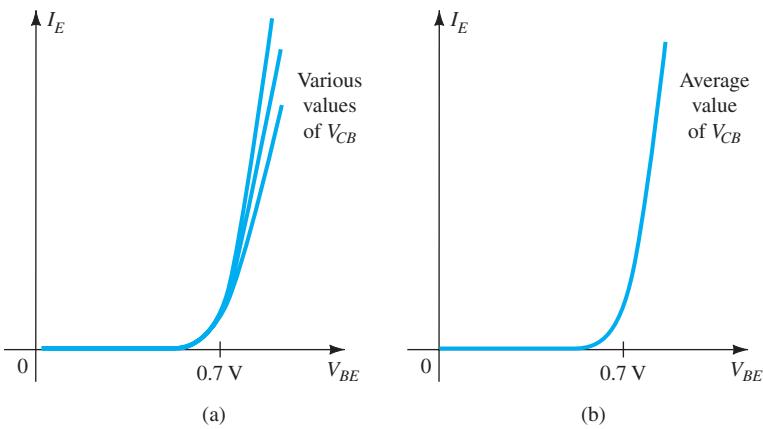


FIG. 5.9

Defining the average curve for the characteristics of Fig. 5.9a.

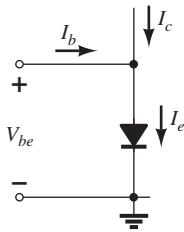


FIG. 5.10

Equivalent circuit for the input side of a BJT transistor.

For the equivalent circuit, therefore, the input side is simply a single diode with a current  $I_e$ , as shown in Fig. 5.10. However, we must now add a component to the network that will establish the current  $I_e$  of Fig. 5.10 using the output characteristics.

If we redraw the collector characteristics to have a constant  $\beta$  as shown in Fig. 5.11 (another approximation), the entire characteristics at the output section can be replaced by a controlled source whose magnitude is beta times the base current as shown in Fig. 5.11. Because all the input and output parameters of the original configuration are now present, the equivalent network for the common-emitter configuration has been established in Fig. 5.12.

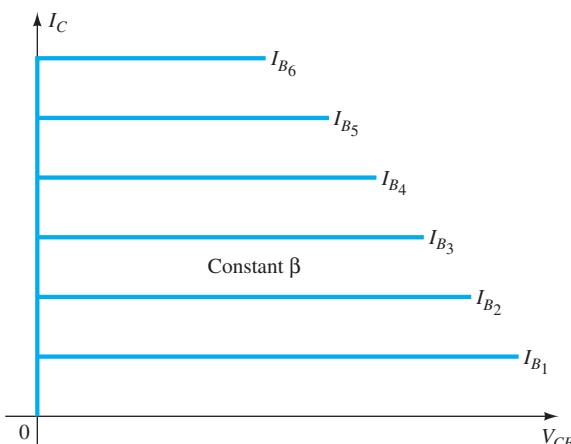


FIG. 5.11

Constant  $\beta$  characteristics.

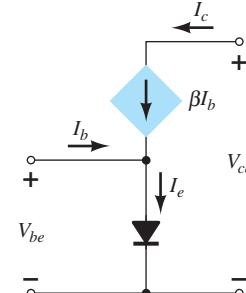


FIG. 5.12

BJT equivalent circuit.

The equivalent model of Fig. 5.12 can be awkward to work with due to the direct connection between input and output networks. It can be improved by first replacing the diode by its equivalent resistance as determined by the level of  $I_E$ , as shown in Fig. 5.13. Recall from Section 1.8 that the diode resistance is determined by  $r_D = 26 \text{ mV}/I_D$ . Using the subscript  $e$  because the determining current is the emitter current will result in  $r_e = 26 \text{ mV}/I_E$ .

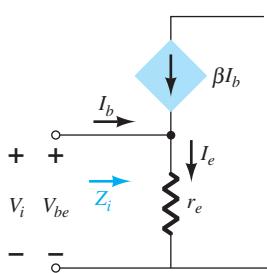


FIG. 5.13  
Defining the level of  $Z_i$ .

Now, for the input side:

$$Z_i = \frac{V_i}{I_b} = \frac{V_{be}}{I_b}$$

Solving for  $V_{be}$ :

$$\begin{aligned} V_{be} &= I_e r_e = (I_c + I_b) r_e = (\beta I_b + I_b) r_e \\ &= (\beta + 1) I_b r_e \end{aligned}$$

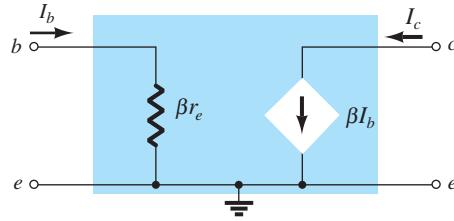
and

$$Z_i = \frac{V_{be}}{I_b} = \frac{(\beta + 1) I_b r_e}{I_b} = (\beta + 1) r_e$$

$Z_i = (\beta + 1) r_e \approx \beta r_e$

(5.1)

The result is that the impedance seen “looking into” the base of the network is a resistor equal to beta times the value of  $r_e$ , as shown in Fig. 5.14. The collector output current is still linked to the input current by beta as shown in the same figure.



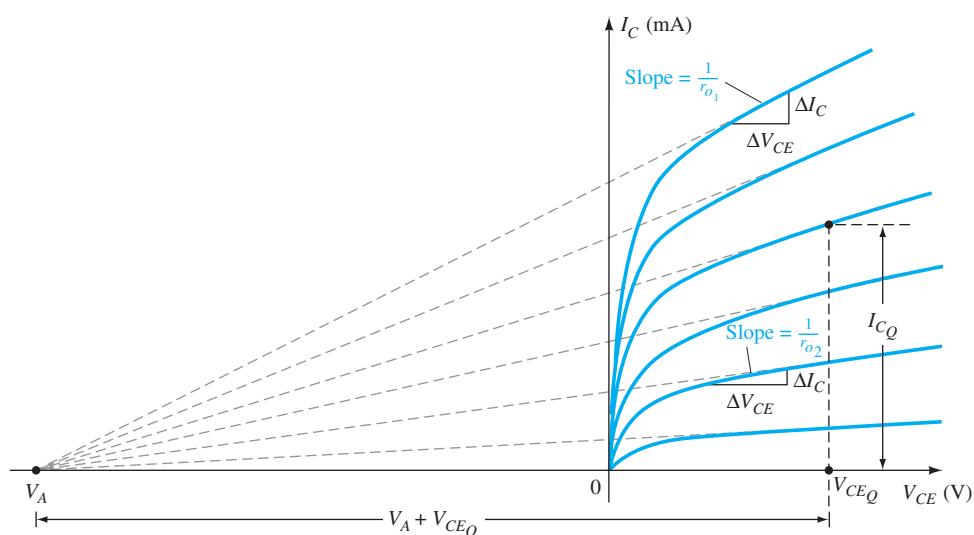
**FIG. 5.14**  
Improved BJT equivalent circuit.

The equivalent circuit has therefore been defined for the ideal characteristics of Fig. 5.11, but now the input and output circuits are isolated and only linked by the controlled source—a form much easier to work with when analyzing networks.

## Early Voltage

We now have a good representation for the input circuit, but aside from the collector output current being defined by the level of beta and  $I_B$ , we do not have a good representation for the output impedance of the device. In reality the characteristics do not have the ideal appearance of Fig. 5.11. Rather, they have a slope as shown in Fig. 5.15 that defines the output impedance of the device. The steeper the slope, the less the output impedance and the less ideal the transistor. In general, it is desirable to have large output impedances to avoid loading down the next stage of a design. If the slope of the curves is extended until they reach the horizontal axis, it is interesting to note in Fig. 5.15 that they will all intersect at a voltage called the Early voltage. This intersection was first discovered by James M. Early in 1952. As the base current increases the slope of the line increases, resulting in an increase in output impedance with increase in base and collector current. For a particular collector and base current as shown in Fig. 5.15, the output impedance can be found using the following equation:

$$r_o = \frac{\Delta V}{\Delta I} = \frac{V_A + V_{CEQ}}{I_{CQ}} \quad (5.2)$$



**FIG. 5.15**  
Defining the Early voltage and the output impedance of a transistor.

Typically, however, the Early voltage is sufficiently large compared with the applied collector-to-emitter voltage to permit the following approximation.

$$r_o \cong \frac{V_A}{I_{CQ}} \quad (5.3)$$

Clearly, since  $V_A$  is a fixed voltage, the larger the collector current, the less the output impedance.

For situations where the Early voltage is not available the output impedance can be found from the characteristics at any base or collector current using the following equation:

$$\text{Slope} = \frac{\Delta y}{\Delta x} = \frac{\Delta I_C}{\Delta V_{CE}} = \frac{1}{r_o}$$

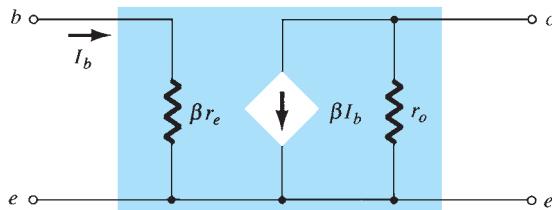
and

$$r_o = \frac{\Delta V_{CE}}{\Delta I_C} \quad (5.4)$$

For the same change in voltage in Fig. 5.15 the resulting change in current  $\Delta I_C$  is significantly less for  $r_{o2}$  than  $r_{o1}$ , resulting in  $r_{o2}$  being much larger than  $r_{o1}$ .

In situations where the specification sheets of a transistor do not include the Early voltage or the output characteristics, the output impedance can be determined from the hybrid parameter  $h_{oe}$  that is normally plotted on every specification sheet. It is a quantity that will be described in detail in Section 5.19.

In any event, an output impedance can now be defined that will appear as a resistor in parallel with the output as shown in the equivalent circuit of Fig. 5.16.

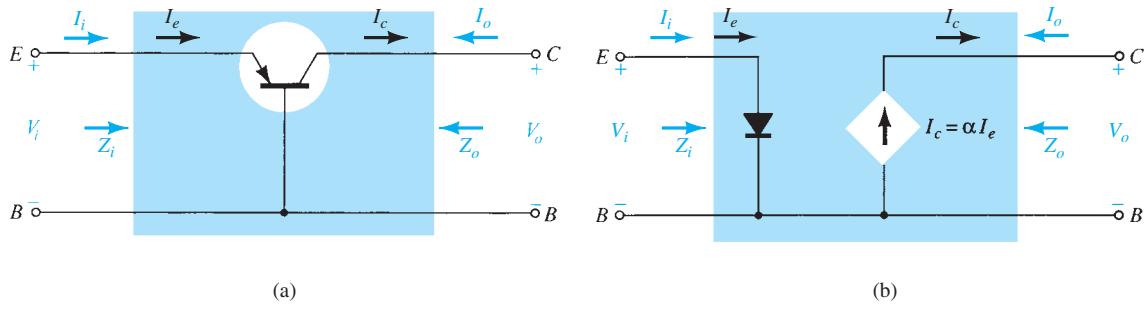


**FIG. 5.16**  
 $r_e$  model for the common-emitter transistor configuration including effects of  $r_o$

The equivalent circuit of Fig. 5.16 will be used throughout the analysis to follow for the common-emitter configuration. Typical values of beta run from 50 to 200, with values of  $\beta r_e$  typically running from a few hundred ohms to a maximum of  $6 \text{ k}\Omega$  to  $7 \text{ k}\Omega$ . The output resistance  $r$  is typically in the range of  $40 \text{ k}\Omega$  to  $50 \text{ k}\Omega$ .

### Common-Base Configuration

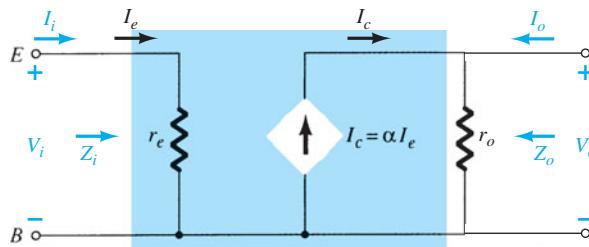
The common-base equivalent circuit will be developed in much the same manner as applied to the common-emitter configuration. The general characteristics of the input and output circuit will generate an equivalent circuit that will approximate the actual behavior of the device. Recall for the common-emitter configuration the use of a diode to represent the connection from base to emitter. For the common-base configuration of Fig. 5.17a the *pnp* transistor employed will present the same possibility at the input circuit. The result is the use of a diode in the equivalent circuit as shown in Fig. 5.17b. For the output circuit, if we return to Chapter 3 and review Fig. 3.8, we find that the collector current is related to the emitter current by alpha  $\alpha$ . In this case, however, the controlled source defining the collector current as inserted in Fig. 5.17b is opposite in direction to that of the controlled source of the common-emitter configuration. The direction of the collector current in the output circuit is now opposite that of the defined output current.



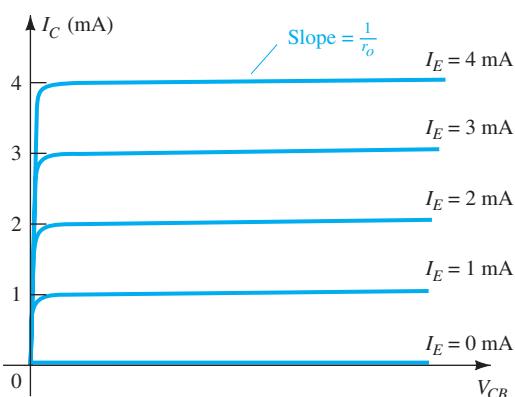
**FIG. 5.17**  
(a) Common-base BJT transistor; (b) equivalent circuit for configuration of (a).

For the ac response, the diode can be replaced by its equivalent ac resistance determined by  $r_e = 26 \text{ mV}/I_E$  as shown in Fig. 5.18. Take note of the fact that the emitter current continues to determine the equivalent resistance. An additional output resistance can be determined from the characteristics of Fig. 5.19 in much the same manner as applied to the common-emitter configuration. The almost horizontal lines clearly reveal that the output resistance  $r_o$  as appearing in Fig. 5.18 will be quite high and certainly much higher than that for the typical common-emitter configuration.

The network of Fig. 5.18 is therefore an excellent equivalent circuit for the analysis of most common-base configurations. It is similar in many ways to that of the common-emitter configuration. In general, common-base configurations have very low input impedance because it is essentially simply  $r_e$ . Typical values extend from a few ohms to perhaps  $50 \Omega$ . The output impedance  $r_o$  will typically extend into the megohm range. Because the output current is opposite to the defined  $I_o$  direction, you will find in the analysis to follow that there is no phase shift between the input and output voltages. For the common-emitter configuration there is a  $180^\circ$  phase shift.



**FIG. 5.18**  
Common base  $r_e$  equivalent circuit.



**FIG. 5.19**  
Defining  $Z_o$

## Common-Collector Configuration

For the common-collector configuration, the model defined for the common-emitter configuration of Fig. 5.16 is normally applied rather than defining a model for the common-collector configuration. In subsequent chapters, a number of common-collector configurations will be investigated, and the effect of using the same model will become quite apparent.

### npn versus pnp

The dc analysis of *npn* and *pnp* configurations is quite different in the sense that the currents will have opposite directions and the voltages opposite polarities. However, for an ac analysis where the signal will progress between positive and negative values, the ac equivalent circuit will be the same.

## 5.5 COMMON-EMITTER FIXED-BIAS CONFIGURATION

The transistor models just introduced will now be used to perform a small-signal ac analysis of a number of standard transistor network configurations. The networks analyzed represent the majority of those appearing in practice. Modifications of the standard configurations will be relatively easy to examine once the content of this chapter is reviewed and understood. For each configuration, the effect of an output impedance is examined for completeness.

The computer analysis section includes a brief description of the transistor model employed in the PSpice and Multisim software packages. It demonstrates the range and depth of the available computer analysis systems and how relatively easy it is to enter a complex network and print out the desired results. The first configuration to be analyzed in detail is the common-emitter *fixed-bias* network of Fig. 5.20. Note that the input signal  $V_i$  is applied to the base of the transistor, whereas the output  $V_o$  is off the collector. In addition, recognize that the input current  $I_i$  is not the base current, but the source current, and the output current  $I_o$  is the collector current. The small-signal ac analysis begins by removing the dc effects of  $V_{CC}$  and replacing the dc blocking capacitors  $C_1$  and  $C_2$  by short-circuit equivalents, resulting in the network of Fig. 5.21.

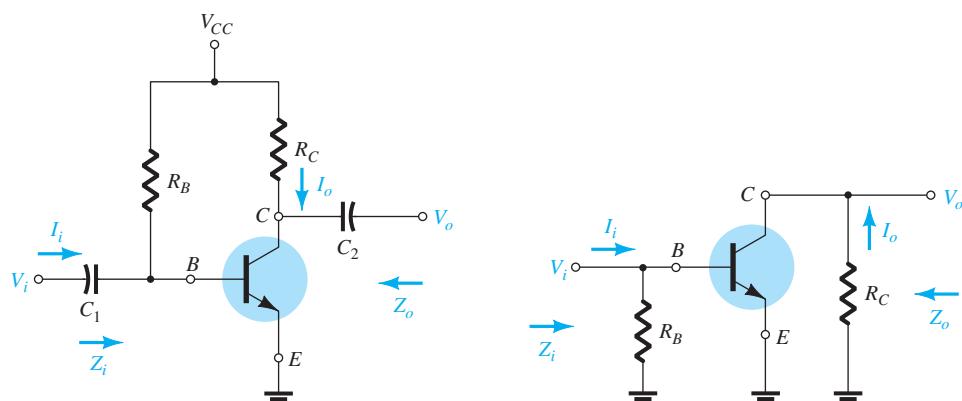


FIG. 5.20

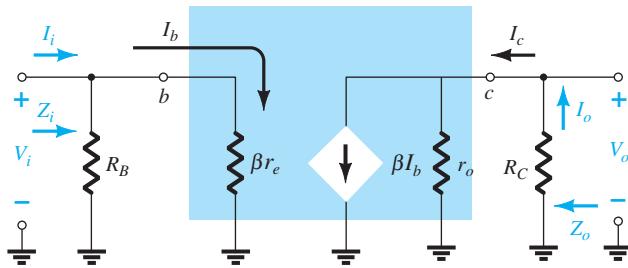
Common-emitter fixed-bias configuration.

FIG. 5.21

Network of Fig. 5.20 following the removal of the effects of  $V_{CC}$ ,  $C_1$ , and  $C_2$ .

Note in Fig. 5.21 that the common ground of the dc supply and the transistor emitter terminal permits the relocation of  $R_B$  and  $R_C$  in parallel with the input and output sections of the transistor, respectively. In addition, note the placement of the important network parameters  $Z_i$ ,  $Z_o$ ,  $I_i$ , and  $I_o$  on the redrawn network. Substituting the  $r_e$  model for the common-emitter configuration of Fig. 5.21 results in the network of Fig. 5.22.

The next step is to determine  $\beta$ ,  $r_e$ , and  $r_o$ . The magnitude of  $\beta$  is typically obtained from a specification sheet or by direct measurement using a curve tracer or transistor


**FIG. 5.22**

Substituting the  $r_e$  model into the network of Fig. 5.21.

testing instrument. The value of  $r_e$  must be determined from a dc analysis of the system, and the magnitude of  $r_o$  is typically obtained from the specification sheet or characteristics. Assuming that  $\beta$ ,  $r_e$ , and  $r_o$  have been determined will result in the following equations for the important two-port characteristics of the system.

**Z<sub>i</sub>** Figure 5.22 clearly shows that

$$Z_i = R_B \parallel \beta r_e \quad \text{ohms} \quad (5.5)$$

For the majority of situations  $R_B$  is greater than  $\beta r_e$  by more than a factor of 10 (recall from the analysis of parallel elements that the total resistance of two parallel resistors is always less than the smallest and very close to the smallest if one is much larger than the other), permitting the following approximation:

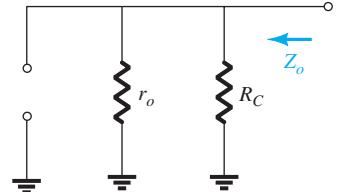
$$Z_i \approx \beta r_e \quad R_B \geq 10\beta r_e \quad \text{ohms} \quad (5.6)$$

**Z<sub>o</sub>** Recall that the output impedance of any system is defined as the impedance  $Z_o$  determined when  $V_i = 0$ . For Fig. 5.22, when  $V_i = 0$ ,  $I_i = I_b = 0$ , resulting in an open-circuit equivalence for the current source. The result is the configuration of Fig. 5.23. We have

$$Z_o = R_C \parallel r_o \quad \text{ohms} \quad (5.7)$$

If  $r_o \geq 10R_C$ , the approximation  $R_C \parallel r_o \approx R_C$  is frequently applied, and

$$Z_o \approx R_C \quad r_o \geq 10R_C \quad (5.8)$$



**FIG. 5.23**  
 Determining  $Z_o$  for the network  
 of Fig. 5.22.

**A<sub>v</sub>** The resistors  $r_o$  and  $R_C$  are in parallel, and

$$V_o = -\beta I_b (R_C \parallel r_o)$$

but

$$I_b = \frac{V_i}{\beta r_e}$$

so that

$$V_o = -\beta \left( \frac{V_i}{\beta r_e} \right) (R_C \parallel r_o)$$

and

$$A_v = \frac{V_o}{V_i} = -\frac{(R_C \parallel r_o)}{r_e} \quad (5.9)$$

If  $r_o \geq 10R_C$ , so that the effect of  $r_o$  can be ignored,

$$A_v = -\frac{R_C}{r_e} \quad r_o \geq 10R_C \quad (5.10)$$

Note the explicit absence of  $\beta$  in Eqs. (5.9) and (5.10), although we recognize that  $\beta$  must be utilized to determine  $r_e$ .

**Phase Relationship** The negative sign in the resulting equation for  $A_v$  reveals that a  $180^\circ$  phase shift occurs between the input and output signals, as shown in Fig. 5.24. This is a result of the fact that  $\beta I_b$  establishes a current through  $R_C$  that will result in a voltage across  $R_C$ , the opposite of that defined by  $V_o$ .

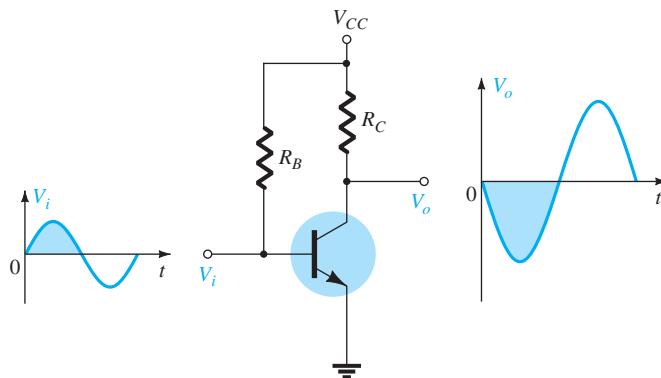


FIG. 5.24

Demonstrating the  $180^\circ$  phase shift between input and output waveforms.

**EXAMPLE 5.1** For the network of Fig. 5.25:

- Determine  $r_e$ .
- Find  $Z_l$  (with  $r_o = \infty \Omega$ ).
- Calculate  $Z_o$  (with  $r_o = \infty \Omega$ ).
- Determine  $A_v$  (with  $r_o = \infty \Omega$ ).
- Repeat parts (c) and (d) including  $r_o = 50 \text{ k}\Omega$  in all calculations and compare results.

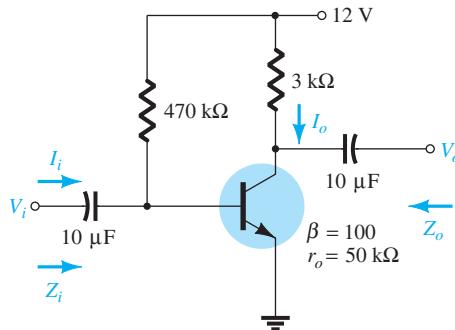


FIG. 5.25

Example 5.1.

**Solution:**

- DC analysis:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 \text{ V} - 0.7 \text{ V}}{470 \text{ k}\Omega} = 24.04 \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (101)(24.04 \mu\text{A}) = 2.428 \text{ mA}$$

$$r_e = \frac{26 \text{ mV}}{I_E} = \frac{26 \text{ mV}}{2.428 \text{ mA}} = 10.71 \Omega$$

$$\text{b. } \beta r_e = (100)(10.71 \Omega) = 1.071 \text{ k}\Omega$$

$$Z_i = R_B \parallel \beta r_e = 470 \text{ k}\Omega \parallel 1.071 \text{ k}\Omega = 1.07 \text{ k}\Omega$$

$$\text{c. } Z_o = R_C = 3 \text{ k}\Omega$$

$$\text{d. } A_v = -\frac{R_C}{r_e} = -\frac{3 \text{ k}\Omega}{10.71 \Omega} = -280.11$$

$$e. Z_o = r_o \| R_C = 50 \text{ k}\Omega \| 3 \text{ k}\Omega = 2.83 \text{ k}\Omega \text{ vs. } 3 \text{ k}\Omega$$

$$A_v = -\frac{r_o \| R_C}{r_e} = \frac{2.83 \text{ k}\Omega}{10.71 \text{ }\Omega} = -264.24 \text{ vs. } -280.11$$

## 5.6 VOLTAGE-DIVIDER BIAS

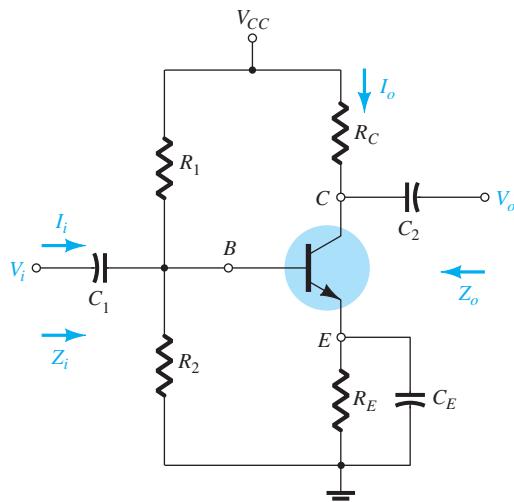
The next configuration to be analyzed is the *voltage-divider* bias network of Fig. 5.26. Recall that the name of the configuration is a result of the voltage-divider bias at the input side to determine the dc level of  $V_B$ .

Substituting the  $r_e$  equivalent circuit results in the network of Fig. 5.27. Note the absence of  $R_E$  due to the low-impedance shorting effect of the bypass capacitor,  $C_E$ . That is, at the frequency (or frequencies) of operation, the reactance of the capacitor is so small compared to  $R_E$  that it is treated as a short circuit across  $R_E$ . When  $V_{CC}$  is set to zero, it places one end of  $R_1$  and  $R_C$  at ground potential as shown in Fig. 5.27. In addition, note that  $R_1$  and  $R_2$  remain part of the input circuit, whereas  $R_C$  is part of the output circuit. The parallel combination of  $R_1$  and  $R_2$  is defined by

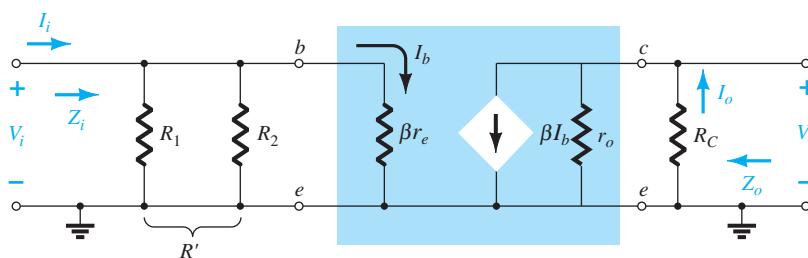
$$R' = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2} \quad (5.11)$$

**Z<sub>i</sub>** From Fig. 5.27

$$Z_i = R' \| \beta r_e \quad (5.12)$$



**FIG. 5.26**  
Voltage-divider bias configuration.



**FIG. 5.27**

Substituting the  $r_e$  equivalent circuit into the ac equivalent network of Fig. 5.26.

**Z<sub>o</sub>** From Fig. 5.27 with  $V_i$  set to 0 V, resulting in  $I_b = 0 \mu\text{A}$  and  $\beta I_b = 0 \text{ mA}$ ,

$$Z_o = R_C \| r_o \quad (5.13)$$

If  $r_o \geq 10R_C$ ,

$$Z_o \equiv R_C \quad r_o \geq 10R_C \quad (5.14)$$

**A<sub>v</sub>** Because  $R_C$  and  $r_o$  are in parallel,

$$V_o = -(\beta I_b)(R_C \| r_o)$$

and

$$I_b = \frac{V_i}{\beta r_e}$$

so that

$$V_o = -\beta \left( \frac{V_i}{\beta r_e} \right) (R_C \| r_o)$$

and

$$A_v = \frac{V_o}{V_i} = \frac{-R_C \| r_o}{r_e} \quad (5.15)$$

which you will note is an exact duplicate of the equation obtained for the fixed-bias configuration.

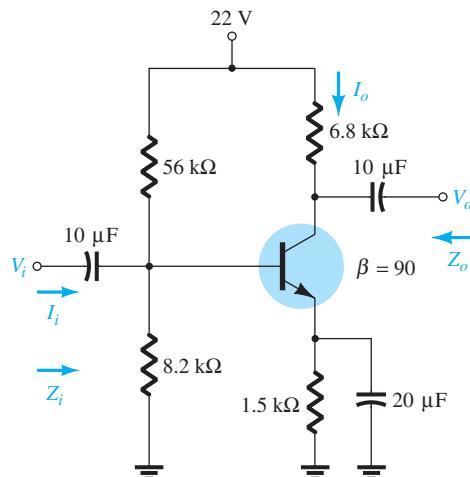
For  $r_o \geq 10R_C$ ,

$$A_v = \frac{V_o}{V_i} \equiv -\frac{R_C}{r_e} \quad r_o \geq 10R_C \quad (5.16)$$

**Phase Relationship** The negative sign of Eq. (5.15) reveals a  $180^\circ$  phase shift between  $V_o$  and  $V_i$ .

**EXAMPLE 5.2** For the network of Fig. 5.28, determine:

- $r_e$ .
- $Z_i$ .
- $Z_o$  ( $r_o = \infty \Omega$ ).
- $A_v$  ( $r_o = \infty \Omega$ ).
- The parameters of parts (b) through (d) if  $r_o = 50 \text{ k}\Omega$  and compare results.



**FIG. 5.28**  
Example 5.2.

a. DC: Testing  $\beta R_E > 10R_2$ ,

$$(90)(1.5 \text{ k}\Omega) > 10(8.2 \text{ k}\Omega)$$

$$135 \text{ k}\Omega > 82 \text{ k}\Omega \text{ (satisfied)}$$

Using the approximate approach, we obtain

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{(8.2 \text{ k}\Omega)(22 \text{ V})}{56 \text{ k}\Omega + 8.2 \text{ k}\Omega} = 2.81 \text{ V}$$

$$V_E = V_B - V_{BE} = 2.81 \text{ V} - 0.7 \text{ V} = 2.11 \text{ V}$$

$$I_E = \frac{V_E}{R_E} = \frac{2.11 \text{ V}}{1.5 \text{ k}\Omega} = 1.41 \text{ mA}$$

$$r_e = \frac{26 \text{ mV}}{I_E} = \frac{26 \text{ mV}}{1.41 \text{ mA}} = 18.44 \text{ }\Omega$$

b.  $R' = R_1 \| R_2 = (56 \text{ k}\Omega) \| (8.2 \text{ k}\Omega) = 7.15 \text{ k}\Omega$

$$Z_i = R' \|\beta r_e = 7.15 \text{ k}\Omega \|(90)(18.44 \text{ }\Omega) = 7.15 \text{ k}\Omega \|\ 1.66 \text{ k}\Omega \\ = 1.35 \text{ k}\Omega$$

c.  $Z_o = R_C = 6.8 \text{ k}\Omega$

d.  $A_v = -\frac{R_C}{r_e} = -\frac{6.8 \text{ k}\Omega}{18.44 \text{ }\Omega} = -368.76$

e.  $Z_i = 1.35 \text{ k}\Omega$

$$Z_o = R_C \| r_o = 6.8 \text{ k}\Omega \| 50 \text{ k}\Omega = 5.98 \text{ k}\Omega \text{ vs. } 6.8 \text{ k}\Omega$$

$$A_v = -\frac{R_C \| r_o}{r_e} = -\frac{5.98 \text{ k}\Omega}{18.44 \text{ }\Omega} = -324.3 \text{ vs. } -368.76$$

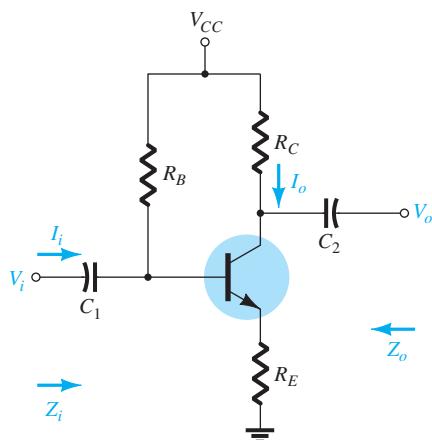
There was a measurable difference in the results for  $Z_o$  and  $A_v$ , because the condition  $r_o \geq 10R_C$  was *not* satisfied.

## 5.7 CE Emitter-Bias Configuration

The networks examined in this section include an emitter resistor that may or may not be bypassed in the ac domain. We first consider the unbypassed situation and then modify the resulting equations for the bypassed configuration.

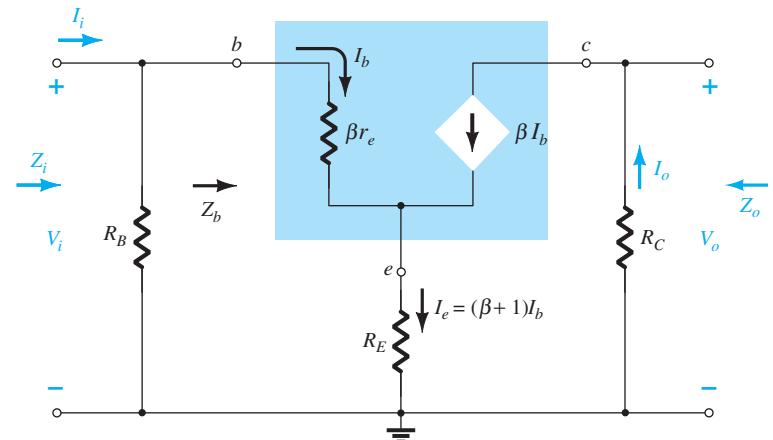
### Unbypassed

The most fundamental of unbypassed configurations appears in Fig. 5.29. The  $r_e$  equivalent model is substituted in Fig. 5.30, but note the absence of the resistance  $r_o$ . The effect of  $r_o$  is to make the analysis a great deal more complicated, and considering the fact that in



**FIG. 5.29**

CE emitter-bias configuration.



**FIG. 5.30**

Substituting the  $r_e$  equivalent circuit into the ac equivalent network of Fig. 5.29.

most situations its effect can be ignored, it will not be included in the present analysis. However, the effect of  $r_o$  will be discussed later in this section.

Applying Kirchhoff's voltage law to the input side of Fig. 5.30 results in

$$V_i = I_b \beta r_e + I_e R_E$$

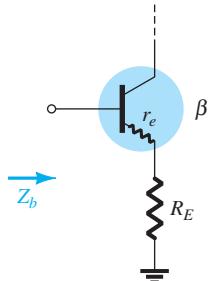
or

$$V_i = I_b \beta r_e + (\beta + 1) I_b R_E$$

and the input impedance looking into the network to the right of  $R_B$  is

$$Z_b = \frac{V_i}{I_b} = \beta r_e + (\beta + 1) R_E$$

The result as displayed in Fig. 5.31 reveals that the input impedance of a transistor with an unbypassed resistor  $R_E$  is determined by



**FIG. 5.31**

Defining the input impedance of a transistor with an unbypassed emitter resistor.

Because  $\beta$  is normally much greater than 1, the approximate equation is

$$Z_b \approx \beta r_e + \beta R_E$$

and

$$Z_b \approx \beta(r_e + R_E) \quad (5.18)$$

Because  $R_E$  is usually greater than  $r_e$ , Eq. (5.18) can be further reduced to

$$Z_b \approx \beta R_E \quad (5.19)$$

**Z<sub>i</sub>** Returning to Fig. 5.30, we have

$$Z_i = R_B \| Z_b \quad (5.20)$$

**Z<sub>o</sub>** With  $V_i$  set to zero,  $I_b = 0$ , and  $\beta I_b$  can be replaced by an open-circuit equivalent. The result is

$$Z_o = R_C \quad (5.21)$$

### A<sub>v</sub>

$$I_b = \frac{V_i}{Z_b}$$

and

$$\begin{aligned} V_o &= -I_o R_C = -\beta I_b R_C \\ &= -\beta \left( \frac{V_i}{Z_b} \right) R_C \end{aligned}$$

with

$$A_v = \frac{V_o}{V_i} = -\frac{\beta R_C}{Z_b} \quad (5.22)$$

Substituting  $Z_b \approx \beta(r_e + R_E)$  gives

$$A_v = \frac{V_o}{V_i} \approx -\frac{R_C}{r_e + R_E} \quad (5.23)$$

and for the approximation  $Z_b \approx \beta R_E$ ,

$$A_v = \frac{V_o}{V_i} \approx -\frac{R_C}{R_E} \quad (5.24)$$

Note the absence of  $\beta$  from the equation for  $A_v$  demonstrating an independence in variation of  $\beta$ .

**Phase Relationship** The negative sign in Eq. (5.22) again reveals a  $180^\circ$  phase shift between  $V_o$  and  $V_i$ .

**Effect of  $r_o$**  The equations appearing below will clearly reveal the additional complexity resulting from including  $r_o$  in the analysis. Note in each case, however, that when certain conditions are met, the equations return to the form just derived. The derivation of each equation is beyond the needs of this text and is left as an exercise for the reader. Each equation can be derived through *careful* application of the basic laws of circuit analysis such as Kirchhoff's voltage and current laws, source conversions, Thévenin's theorem, and so on. The equations were included to remove the nagging question of the effect of  $r_o$  on the important parameters of a transistor configuration.

### Z<sub>b</sub>

$$Z_b = \beta r_e + \left[ \frac{(\beta + 1) + R_C/r_o}{1 + (R_C + R_E)/r_o} \right] R_E \quad (5.25)$$

Because the ratio  $R_C/r_o$  is always much less than  $(\beta + 1)$ ,

$$Z_b \approx \beta r_e + \frac{(\beta + 1)R_E}{1 + (R_C + R_E)/r_o}$$

For  $r_o \geq 10(R_C + R_E)$ ,

$$Z_b \approx \beta r_e + (\beta + 1)R_E$$

which compares directly with Eq. (5.17).

In other words, if  $r_o \geq 10(R_C + R_E)$ , all the equations derived earlier result. Because  $\beta + 1 \approx \beta$ , the following equation is an excellent one for most applications:

$$Z_b \approx \beta(r_e + R_E) \quad r_o \geq 10(R_C + R_E) \quad (5.26)$$

### Z<sub>o</sub>

$$Z_o = R_C \parallel \left[ r_o + \frac{\beta(r_o + r_e)}{1 + \frac{\beta r_e}{R_E}} \right] \quad (5.27)$$

However,  $r_o \gg r_e$ , and

$$Z_o \approx R_C \parallel r_o \left[ 1 + \frac{\beta}{1 + \frac{\beta r_e}{R_E}} \right]$$

which can be written as

$$Z_o \approx R_C \parallel r_o \left[ 1 + \frac{1}{\frac{1}{\beta} + \frac{r_e}{R_E}} \right]$$

Typically  $1/\beta$  and  $r_e/R_E$  are less than one with a sum usually less than one. The result is a multiplying factor for  $r_o$  greater than one. For  $\beta = 100$ ,  $r_e = 10 \Omega$ , and  $R_E = 1 \text{ k}\Omega$ ,

$$\frac{1}{\beta + \frac{r_e}{R_E}} = \frac{1}{100 + \frac{10 \Omega}{1000 \Omega}} = \frac{1}{0.02} = 50$$

and

$$Z_o = R_C \parallel 51r_o$$

which is certainly simply  $R_C$ . Therefore,

$$Z_o \approx R_C \quad \text{Any level of } r_o \quad (5.28)$$

which was obtained earlier.

$$A_v = \frac{V_o}{V_i} = \frac{-\frac{\beta R_C}{Z_b} \left[ 1 + \frac{r_e}{r_o} \right] + \frac{R_C}{r_o}}{1 + \frac{R_C}{r_o}} \quad (5.29)$$

The ratio  $\frac{r_e}{r_o} \ll 1$ , and

$$A_v = \frac{V_o}{V_i} \cong \frac{-\frac{\beta R_C}{Z_b} + \frac{R_C}{r_o}}{1 + \frac{R_C}{r_o}}$$

For  $r_o \geq 10R_C$ ,

$$A_v = \frac{V_o}{V_i} \cong -\frac{\beta R_C}{Z_b} \quad r_o \geq 10R_C \quad (5.30)$$

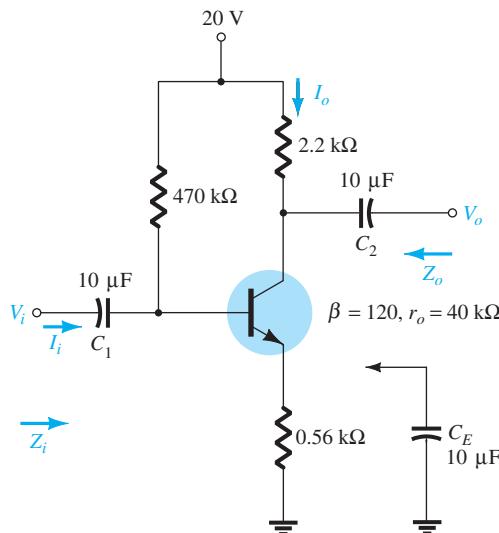
as obtained earlier.

### Bypassed

If  $R_E$  of Fig. 5.29 is bypassed by an emitter capacitor  $C_E$ , the complete  $r_e$  equivalent model can be substituted, resulting in the same equivalent network as Fig. 5.22. Equations (5.5) to (5.10) are therefore applicable.

**EXAMPLE 5.3** For the network of Fig. 5.32, without  $C_E$  (unbypassed), determine:

- a.  $r_e$ .
- b.  $Z_i$ .
- c.  $Z_o$ .
- d.  $A_v$ .



**FIG. 5.32**  
Example 5.3.

### Solution:

- a. DC:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20 \text{ V} - 0.7 \text{ V}}{470 \text{ k}\Omega + (121)0.56 \text{ k}\Omega} = 35.89 \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (121)(35.89 \mu\text{A}) = 4.34 \text{ mA}$$

$$\text{and } r_e = \frac{26 \text{ mV}}{I_E} = \frac{26 \text{ mV}}{4.34 \text{ mA}} = 5.99 \Omega$$

b. Testing the condition  $r_o \geq 10(R_C + R_E)$ , we obtain

$$40 \text{ k}\Omega \geq 10(2.2 \text{ k}\Omega + 0.56 \text{ k}\Omega)$$

$$40 \text{ k}\Omega \geq 10(2.76 \text{ k}\Omega) = 27.6 \text{ k}\Omega \text{ (satisfied)}$$

Therefore,

$$\begin{aligned} Z_b &\cong \beta(r_e + R_E) = 120(5.99 \Omega + 560 \Omega) \\ &= 67.92 \text{ k}\Omega \end{aligned}$$

and

$$\begin{aligned} Z_i &= R_B \| Z_b = 470 \text{ k}\Omega \| 67.92 \text{ k}\Omega \\ &= \mathbf{59.34 \text{ k}\Omega} \end{aligned}$$

c.  $Z_o = R_C = 2.2 \text{ k}\Omega$

d.  $r_o \geq 10R_C$  is satisfied. Therefore,

$$\begin{aligned} A_v &= \frac{V_o}{V_i} \cong -\frac{\beta R_C}{Z_b} = -\frac{(120)(2.2 \text{ k}\Omega)}{67.92 \text{ k}\Omega} \\ &= \mathbf{-3.89} \end{aligned}$$

compared to  $-3.93$  using Eq. (5.20):  $A_v \cong -R_C/R_E$ .

**EXAMPLE 5.4** Repeat the analysis of Example 5.3 with  $C_E$  in place.

**Solution:**

a. The dc analysis is the same, and  $r_e = 5.99 \Omega$ .

b.  $R_E$  is “shorted out” by  $C_E$  for the ac analysis. Therefore,

$$\begin{aligned} Z_i &= R_B \| Z_b = R_B \| \beta r_e = 470 \text{ k}\Omega \| (120)(5.99 \Omega) \\ &= 470 \text{ k}\Omega \| 718.8 \Omega \cong \mathbf{717.70 \Omega} \end{aligned}$$

c.  $Z_o = R_C = 2.2 \text{ k}\Omega$

$$\begin{aligned} d. A_v &= -\frac{R_C}{r_e} \\ &= -\frac{2.2 \text{ k}\Omega}{5.99 \Omega} = \mathbf{-367.28} \text{ (a significant increase)} \end{aligned}$$

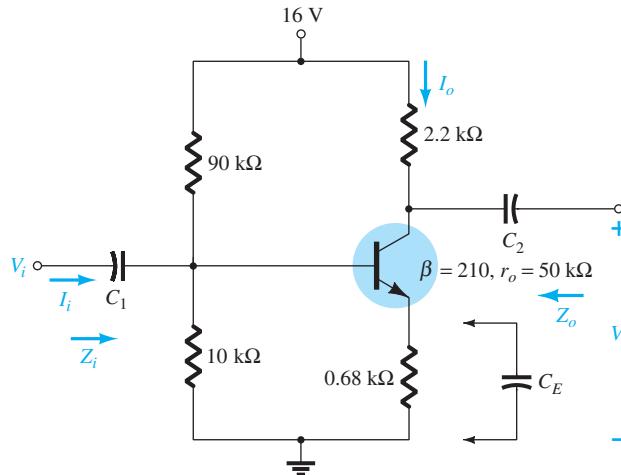
**EXAMPLE 5.5** For the network of Fig. 5.33 (with  $C_E$  unconnected), determine (using appropriate approximations):

a.  $r_e$ .

b.  $Z_i$ .

c.  $Z_o$ .

d.  $A_v$ .



**FIG. 5.33**

Example 5.5.

**Solution:**

- a. Testing  $\beta R_E > 10R_2$ ,

$$(210)(0.68 \text{ k}\Omega) > 10(10 \text{ k}\Omega)$$

$$142.8 \text{ k}\Omega > 100 \text{ k}\Omega (\text{satisfied})$$

we have

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{10 \text{ k}\Omega}{90 \text{ k}\Omega + 10 \text{ k}\Omega} (16 \text{ V}) = 1.6 \text{ V}$$

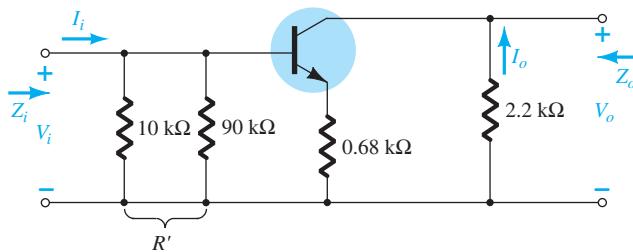
$$V_E = V_B - V_{BE} = 1.6 \text{ V} - 0.7 \text{ V} = 0.9 \text{ V}$$

$$I_E = \frac{V_E}{R_E} = \frac{0.9 \text{ V}}{0.68 \text{ k}\Omega} = 1.324 \text{ mA}$$

$$r_e = \frac{26 \text{ mV}}{I_E} = \frac{26 \text{ mV}}{1.324 \text{ mA}} = \mathbf{19.64 \Omega}$$

- b. The ac equivalent circuit is provided in Fig. 5.34. The resulting configuration is different from Fig. 5.30 only by the fact that now

$$R_B = R' = R_1 \| R_2 = 9 \text{ k}\Omega$$



**FIG. 5.34**

The ac equivalent circuit of Fig. 5.33.

The testing conditions of  $r_o \geq 10(R_C + R_E)$  and  $r_o \geq 10R_C$  are both satisfied. Using the appropriate approximations yields

$$Z_b \cong \beta R_E = 142.8 \text{ k}\Omega$$

$$\begin{aligned} Z_i &= R_B \| Z_b = 9 \text{ k}\Omega \| 142.8 \text{ k}\Omega \\ &= \mathbf{8.47 \text{ k}\Omega} \end{aligned}$$

c.  $Z_o = R_C = \mathbf{2.2 \text{ k}\Omega}$

d.  $A_v = -\frac{R_C}{R_E} = -\frac{2.2 \text{ k}\Omega}{0.68 \text{ k}\Omega} = \mathbf{-3.24}$

**EXAMPLE 5.6** Repeat Example 5.5 with  $C_E$  in place.

**Solution:**

- a. The dc analysis is the same, and  $r_e = \mathbf{19.64 \Omega}$ .

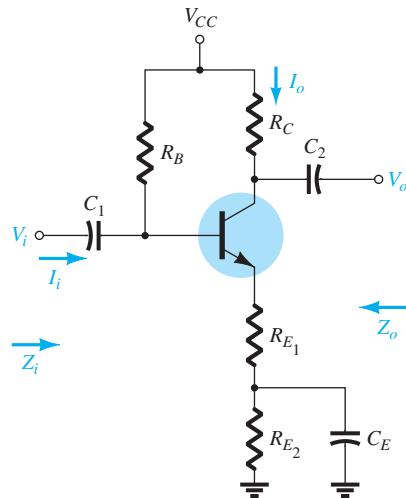
b.  $Z_b = \beta r_e = (210)(19.64 \Omega) \cong 4.12 \text{ k}\Omega$

$$\begin{aligned} Z_i &= R_B \| Z_b = 9 \text{ k}\Omega \| 4.12 \text{ k}\Omega \\ &= \mathbf{2.83 \text{ k}\Omega} \end{aligned}$$

c.  $Z_o = R_C = \mathbf{2.2 \text{ k}\Omega}$

d.  $A_v = -\frac{R_C}{r_e} = -\frac{2.2 \text{ k}\Omega}{19.64 \Omega} = \mathbf{-112.02}$  (a significant increase)

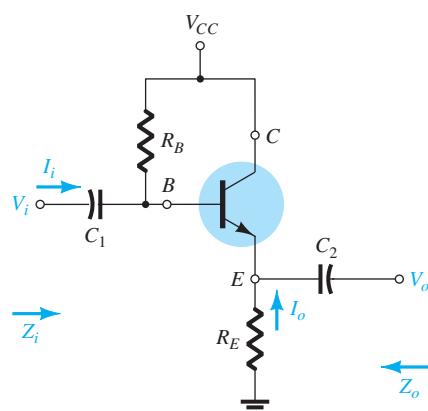
Another variation of an emitter-bias configuration is shown in Fig. 5.35. For the dc analysis, the emitter resistance is  $R_{E_1} + R_{E_2}$ , whereas for the ac analysis, the resistor  $R_E$  in the equations above is simply  $R_{E_1}$  with  $R_{E_2}$  bypassed by  $C_E$ .

**FIG. 5.35**

An emitter-bias configuration with a portion of the emitter-bias resistance bypassed in the ac domain.

## 5.8 Emitter-Follower Configuration

When the output is taken from the emitter terminal of the transistor as shown in Fig. 5.36, the network is referred to as an *emitter-follower*. The output voltage is always slightly less than the input signal due to the drop from base to emitter, but the approximation  $A_v \approx 1$  is usually a good one. Unlike the collector voltage, the emitter voltage is in phase with the signal  $V_i$ . That is, both  $V_o$  and  $V_i$  attain their positive and negative peak values at the same time. The fact that  $V_o$  “follows” the magnitude of  $V_i$  with an in-phase relationship accounts for the terminology *emitter-follower*.



**FIG. 5.36**  
Emitter-follower configuration.

The most common emitter-follower configuration appears in Fig. 5.36. In fact, because the collector is grounded for ac analysis, it is actually a *common-collector* configuration. Other variations of Fig. 5.36 that draw the output off the emitter with  $V_o \approx V_i$  will appear later in this section.

The emitter-follower configuration is frequently used for impedance-matching purposes. It presents a high impedance at the input and a low impedance at the output, which is the direct opposite of the standard fixed-bias configuration. The resulting effect is much the same as that obtained with a transformer, where a load is matched to the source impedance for maximum power transfer through the system.

Substituting the  $r_e$  equivalent circuit into the network of Fig. 5.36 results in the network of Fig. 5.37. The effect of  $r_o$  will be examined later in the section.

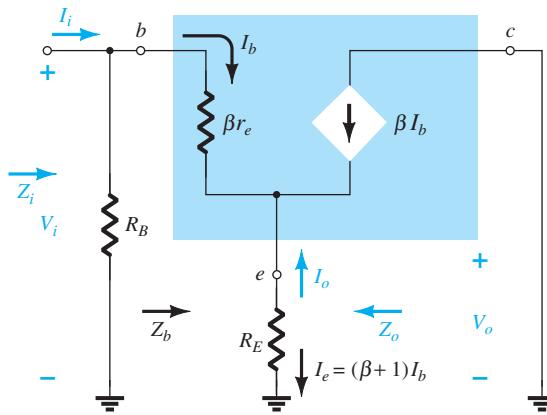


FIG. 5.37

Substituting the  $r_e$  equivalent circuit into the ac equivalent network of Fig. 5.36.

**Z<sub>i</sub>** The input impedance is determined in the same manner as described in the preceding section:

$$Z_i = R_B \parallel Z_b \quad (5.31)$$

with

$$Z_b = \beta r_e + (\beta + 1)R_E \quad (5.32)$$

or

$$Z_b \approx \beta(r_e + R_E) \quad (5.33)$$

and

$$Z_b \approx \beta R_E \quad R_E \gg r_e \quad (5.34)$$

**Z<sub>o</sub>** The output impedance is best described by first writing the equation for the current  $I_b$ ,

$$I_b = \frac{V_i}{Z_b}$$

and then multiplying by  $(\beta + 1)$  to establish  $I_e$ . That is,

$$I_e = (\beta + 1)I_b = (\beta + 1)\frac{V_i}{Z_b}$$

Substituting for  $Z_b$  gives

$$I_e = \frac{(\beta + 1)V_i}{\beta r_e + (\beta + 1)R_E}$$

or

$$I_e = \frac{V_i}{[\beta r_e / (\beta + 1)] + R_E}$$

but

$$(\beta + 1) \approx \beta$$

and

$$\frac{\beta r_e}{\beta + 1} \approx \frac{\beta r_e}{\beta} = r_e$$

so that

$$I_e \approx \frac{V_i}{r_e + R_E} \quad (5.35)$$

If we now construct the network defined by Eq. (5.35), the configuration of Fig. 5.38 results.

To determine  $Z_o$ ,  $V_i$  is set to zero and

$$Z_o = R_E \parallel r_e \quad (5.36)$$

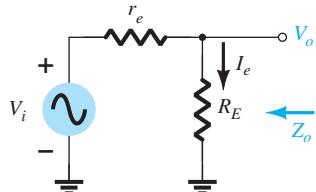


FIG. 5.38

Defining the output impedance for the emitter-follower configuration.

Because  $R_E$  is typically much greater than  $r_e$ , the following approximation is often applied:

$$Z_o \approx r_e \quad (5.37)$$

**A<sub>v</sub>** Figure 5.38 can be used to determine the voltage gain through an application of the voltage-divider rule:

$$V_o = \frac{R_E V_i}{R_E + r_e}$$

and

$$A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e} \quad (5.38)$$

Because  $R_E$  is usually much greater than  $r_e$ ,  $R_E + r_e \approx R_E$  and

$$A_v = \frac{V_o}{V_i} \approx 1 \quad (5.39)$$

**Phase Relationship** As revealed by Eq. (5.38) and earlier discussions of this section,  $V_o$  and  $V_i$  are in phase for the emitter-follower configuration.

### Effect of $r_o$ $Z_i$

$$Z_b = \beta r_e + \frac{(\beta + 1)R_E}{1 + \frac{R_E}{r_o}} \quad (5.40)$$

If the condition  $r_o \geq 10R_E$  is satisfied,

$$Z_b = \beta r_e + (\beta + 1)R_E$$

which matches earlier conclusions with

$$Z_b \approx \beta(r_e + R_E) \quad r_o \geq 10R_E \quad (5.41)$$

### $Z_o$

$$Z_o = r_o \| R_E \| \frac{\beta r_e}{(\beta + 1)} \quad (5.42)$$

Using  $\beta + 1 \approx \beta$ , we obtain

$$Z_o = r_o \| R_E \| r_e$$

and because  $r_o \gg r_e$ ,

$$Z_o \approx R_E \| r_e \quad \text{Any } r_o \quad (5.43)$$

### **A<sub>v</sub>**

$$A_v = \frac{(\beta + 1)R_E / Z_b}{1 + \frac{R_E}{r_o}} \quad (5.44)$$

If the condition  $r_o \geq 10R_E$  is satisfied and we use the approximation  $\beta + 1 \approx \beta$ , we find

$$A_v \approx \frac{\beta R_E}{Z_b}$$

But

$$Z_b \cong \beta(r_e + R_E)$$

so that

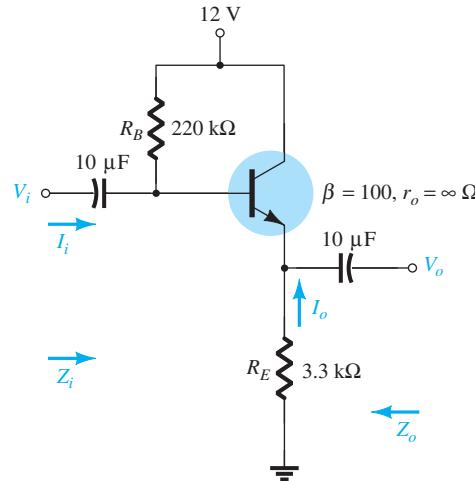
$$A_v \cong \frac{\beta R_E}{\beta(r_e + R_E)}$$

and

$$A_v \cong \frac{R_E}{r_e + R_E} \quad r_o \geq 10R_E \quad (5.45)$$

**EXAMPLE 5.7** For the emitter-follower network of Fig. 5.39, determine:

- a.  $r_e$ .
- b.  $Z_i$ .
- c.  $Z_o$ .
- d.  $A_v$ .
- e. Repeat parts (b) through (d) with  $r_o = 25 \text{ k}\Omega$  and compare results.

**FIG. 5.39**

Example 5.7.

**Solution:**

$$\begin{aligned} \text{a. } I_B &= \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} \\ &= \frac{12 \text{ V} - 0.7 \text{ V}}{220 \text{ k}\Omega + (101)3.3 \text{ k}\Omega} = 20.42 \mu\text{A} \end{aligned}$$

$$\begin{aligned} I_E &= (\beta + 1)I_B \\ &= (101)(20.42 \mu\text{A}) = 2.062 \text{ mA} \end{aligned}$$

$$r_e = \frac{26 \text{ mV}}{I_E} = \frac{26 \text{ mV}}{2.062 \text{ mA}} = \mathbf{12.61 \Omega}$$

$$\begin{aligned} \text{b. } Z_b &= \beta r_e + (\beta + 1)R_E \\ &= (100)(12.61 \Omega) + (101)(3.3 \text{ k}\Omega) \\ &= 1.261 \text{ k}\Omega + 333.3 \text{ k}\Omega \\ &= 334.56 \text{ k}\Omega \cong \beta R_E \end{aligned}$$

$$\begin{aligned} Z_i &= R_B \| Z_b = 220 \text{ k}\Omega \| 334.56 \text{ k}\Omega \\ &= \mathbf{132.72 \text{ k}\Omega} \end{aligned}$$

$$\begin{aligned} \text{c. } Z_o &= R_E \| r_e = 3.3 \text{ k}\Omega \| 12.61 \Omega \\ &= \mathbf{12.56 \Omega} \cong r_e \end{aligned}$$

$$\begin{aligned} \text{d. } A_v &= \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e} = \frac{3.3 \text{ k}\Omega}{3.3 \text{ k}\Omega + 12.61 \Omega} \\ &= \mathbf{0.996} \cong 1 \end{aligned}$$

e. Checking the condition  $r_o \geq 10R_E$ , we have

$$25 \text{ k}\Omega \geq 10(3.3 \text{ k}\Omega) = 33 \text{ k}\Omega$$

which is *not* satisfied. Therefore,

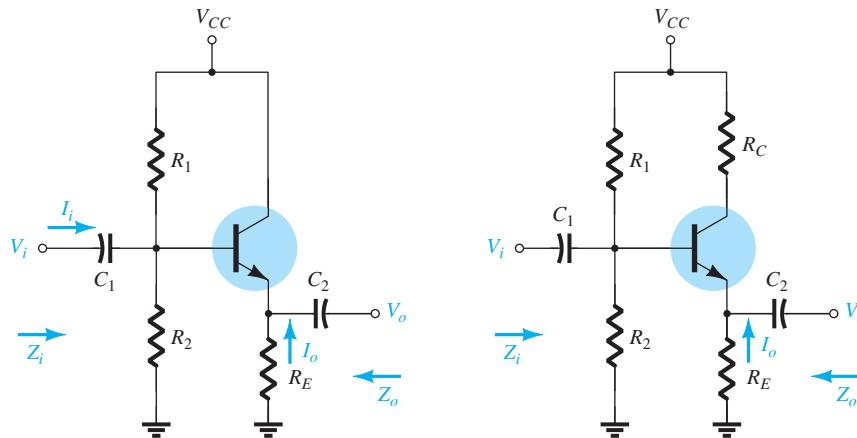
$$\begin{aligned} Z_b &= \beta r_e + \frac{(\beta + 1)R_E}{1 + \frac{R_E}{r_o}} = (100)(12.61 \Omega) + \frac{(100 + 1)3.3 \text{ k}\Omega}{1 + \frac{3.3 \text{ k}\Omega}{25 \text{ k}\Omega}} \\ &= 1.261 \text{ k}\Omega + 294.43 \text{ k}\Omega \\ &= 295.7 \text{ k}\Omega \\ \text{with } Z_i &= R_B \| Z_b = 220 \text{ k}\Omega \| 295.7 \text{ k}\Omega \\ &= \mathbf{126.15 \text{ k}\Omega} \text{ vs. } 132.72 \text{ k}\Omega \text{ obtained earlier} \\ Z_o &= R_E \| r_e = \mathbf{12.56 \Omega} \text{ as obtained earlier} \\ A_v &= \frac{(\beta + 1)R_E/Z_b}{\left[1 + \frac{R_E}{r_o}\right]} = \frac{(100 + 1)(3.3 \text{ k}\Omega)/295.7 \text{ k}\Omega}{\left[1 + \frac{3.3 \text{ k}\Omega}{25 \text{ k}\Omega}\right]} \\ &= \mathbf{0.996 \cong 1} \end{aligned}$$

matching the earlier result.

In general, therefore, even though the condition  $r_o \geq 10R_E$  is not satisfied, the results for  $Z_o$  and  $A_v$  are the same, with  $Z_i$  only slightly less. The results suggest that for most applications a good approximation for the actual results can be obtained by simply ignoring the effects of  $r_o$  for this configuration.

The network of Fig. 5.40 is a variation of the network of Fig. 5.36, which employs a voltage-divider input section to set the bias conditions. Equations (5.31) to (5.34) are changed only by replacing  $R_B$  by  $R' = R_1 \| R_2$ .

The network of Fig. 5.41 also provides the input/output characteristics of an emitter-follower, but includes a collector resistor  $R_C$ . In this case  $R_B$  is again replaced by the parallel combination of  $R_1$  and  $R_2$ . The input impedance  $Z_i$  and output impedance  $Z_o$  are unaffected by  $R_C$  because it is not reflected into the base or emitter equivalent networks. In fact, the only effect of  $R_C$  is to determine the  $Q$ -point of operation.



**FIG. 5.40**

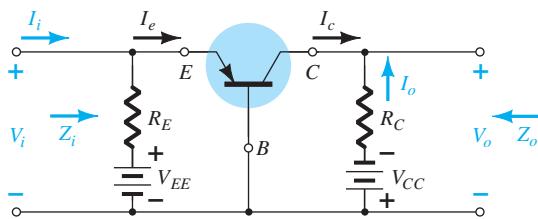
Emitter-follower configuration with a voltage-divider biasing arrangement.

**FIG. 5.41**

Emitter-follower configuration with a collector resistor  $R_C$ .

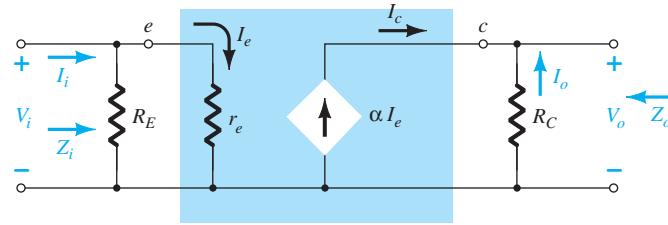
## 5.9 COMMON-BASE CONFIGURATION

The common-base configuration is characterized as having a relatively low input and a high output impedance and a current gain less than 1. The voltage gain, however, can be quite large. The standard configuration appears in Fig. 5.42, with the common-base  $r_e$  equivalent model substituted in Fig. 5.43. The transistor output impedance  $r_o$  is not included for the



**FIG. 5.42**

Common-base configuration.



**FIG. 5.43**

Substituting the  $r_e$  equivalent circuit into the ac equivalent network of Fig. 5.44.

common-base configuration because it is typically in the megohm range and can be ignored in parallel with the resistor  $R_C$ .

**$Z_i$**

$$Z_i = R_E \parallel r_e \quad (5.46)$$

**$Z_o$**

$$Z_o = R_C \quad (5.47)$$

**$A_v$**

$$V_o = -I_o R_C = -(-I_c) R_C = \alpha I_e R_C$$

with

$$I_e = \frac{V_i}{r_e}$$

so that

$$V_o = \alpha \left( \frac{V_i}{r_e} \right) R_C$$

and

$$A_v = \frac{V_o}{V_i} = \frac{\alpha R_C}{r_e} \cong \frac{R_C}{r_e} \quad (5.48)$$

**$A_i$**  Assuming that  $R_E \gg r_e$  yields

$$I_e = I_i$$

and

$$I_o = -\alpha I_e = -\alpha I_i$$

with

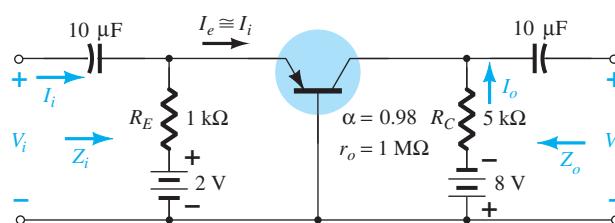
$$A_i = \frac{I_o}{I_i} = -\alpha \cong -1 \quad (5.49)$$

**Phase Relationship** The fact that  $A_v$  is a positive number shows that  $V_o$  and  $V_i$  are in phase for the common-base configuration.

**Effect of  $r_o$**  For the common-base configuration,  $r_o = 1/h_{ob}$  is typically in the megohm range and sufficiently larger than the parallel resistance  $R_C$  to permit the approximation  $r_o \parallel R_C \cong R_C$ .

**EXAMPLE 5.8** For the network of Fig. 5.44, determine:

- a.  $r_e$ .
- b.  $Z_i$ .
- c.  $Z_o$ .
- d.  $A_v$ .
- e.  $A_i$ .



**FIG. 5.44**

Example 5.8.

$$a. I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{2\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = \frac{1.3\text{ V}}{1\text{ k}\Omega} = 1.3\text{ mA}$$

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{1.3\text{ mA}} = 20\text{ }\Omega$$

$$b. Z_i = R_E \| r_e = 1\text{ k}\Omega \| 20\text{ }\Omega$$

$$= 19.61\text{ }\Omega \cong r_e$$

$$c. Z_o = R_C = 5\text{ k}\Omega$$

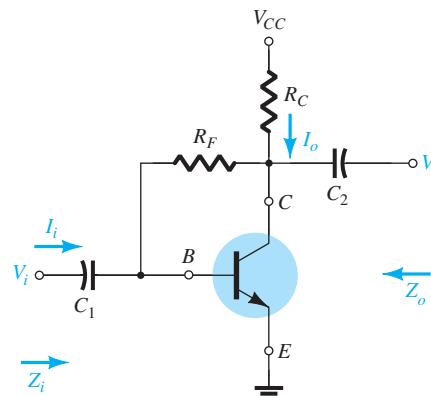
$$d. A_v \cong \frac{R_C}{r_e} = \frac{5\text{ k}\Omega}{20\text{ }\Omega} = 250$$

$$e. A_i = -0.98 \cong -1$$

## 5.10 COLLECTOR FEEDBACK CONFIGURATION

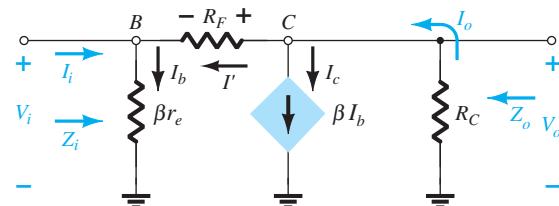
The collector feedback network of Fig. 5.45 employs a feedback path from collector to base to increase the stability of the system as discussed in Section 4.6. However, the simple maneuver of connecting a resistor from base to collector rather than base to dc supply has a significant effect on the level of difficulty encountered when analyzing the network.

Some of the steps to be performed below are the result of experience working with such configurations. It is not expected that a new student of the subject would choose the sequence of steps described below without taking a wrong step or two. Substituting the equivalent circuit and redrawing the network results in the configuration of Fig. 5.46. The effects of a transistor output resistance  $r_o$  will be discussed later in the section.



**FIG. 5.45**

Collector feedback configuration.



**FIG. 5.46**

Substituting the  $r_e$  equivalent circuit into the ac equivalent network of Fig. 5.45.

**Z<sub>i</sub>**

$$I_o = I' + \beta I_b$$

and

$$I' = \frac{V_o - V_i}{R_F}$$

but

$$V_o = -I_o R_C = -(I' + \beta I_b) R_C$$

with

$$V_i = I_b \beta r_e$$

so that

$$I' = -\frac{(I' + \beta I_b) R_C - I_b \beta r_e}{R_F} = -\frac{I' R_C}{R_F} - \frac{\beta I_b R_C}{R_F} - \frac{I_b \beta r_e}{R_F}$$

which when rearranged in the following:

$$I' \left( 1 + \frac{R_C}{R_F} \right) = -\beta I_b \frac{(R_C + r_e)}{R_F}$$

and finally,

$$I' = -\beta I_b \frac{(R_C + r_e)}{R_C + R_F}$$

Now  $Z_i = \frac{V_i}{I_i}$ :

and

$$I_i = I_b - I' = I_b + \beta I_b \frac{(R_C + r_e)}{R_C + R_F}$$

or

$$I_i = I_b \left( 1 + \beta \frac{(R_C + r_e)}{R_C + R_F} \right)$$

Substituting for  $V_i$  in the above equation for  $Z_i$  leaves

$$Z_i = \frac{V_i}{I_i} = \frac{I_b \beta r_e}{I_b \left( 1 + \beta \frac{(R_C + r_e)}{R_C + R_F} \right)} = \frac{\beta r_e}{1 + \beta \frac{(R_C + r_e)}{R_C + R_F}}$$

Since  $R_C \gg r_e$

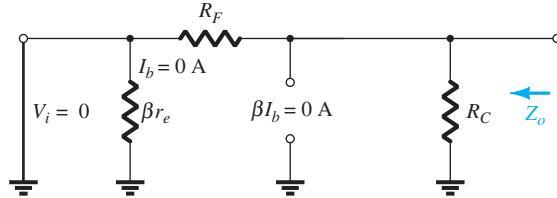
$$Z_i = \frac{\beta r_e}{1 + \frac{\beta R_C}{R_C + R_F}}$$

or

$$Z_i = \frac{r_e}{\frac{1}{\beta} + \frac{R_C}{R_C + R_F}} \quad (5.50)$$

**Z<sub>o</sub>** If we set  $V_i$  to zero as required to define  $Z_o$ , the network will appear as shown in Fig. 5.47. The effect of  $\beta r_e$  is removed, and  $R_F$  appears in parallel with  $R_C$  and

$$Z_o \equiv R_C \| R_F \quad (5.51)$$



**FIG. 5.47**  
Defining  $Z_o$  for the collector feedback configuration.

**A<sub>v</sub>**

$$V_o = -I_o R_C = -(I' + \beta I_b) R_C \\ = -\left( -\beta I_b \frac{(R_C + r_e)}{R_C + R_F} + \beta I_b \right) R_C$$

or

$$V_o = -\beta I_b \left( 1 - \frac{(R_C + r_e)}{R_C + R_F} \right) R_C$$

Then

$$A_v = \frac{V_o}{V_i} = \frac{-\beta I_b \left( 1 - \frac{(R_C + r_e)}{R_C + R_F} \right) R_C}{\beta r_e I_b} \\ = -\left( 1 - \frac{(R_C + r_e)}{R_C + R_F} \right) \frac{R_C}{r_e}$$

For  $R_C \gg r_e$

$$A_v = -\left( 1 - \frac{R_C}{R_C + R_F} \right) \frac{R_C}{r_e}$$

or

$$A_v = -\frac{(R_C + R_F - R_C)R_C}{R_C + R_F} \frac{R_C}{r_e}$$

and

$$A_v = -\left(\frac{R_F}{R_C + R_F}\right) \frac{R_C}{r_e} \quad (5.52)$$

For  $R_F \gg R_C$ 

$$A_v \cong -\frac{R_C}{r_e} \quad (5.53)$$

**Phase Relationship** The negative sign of Eq. (5.52) indicates a  $180^\circ$  phase shift between  $V_o$  and  $V_i$ .

### Effect of $r_o$

**Z<sub>i</sub>** A complete analysis without applying approximations results in

$$Z_i = \frac{1 + \frac{R_C \| r_o}{R_F}}{\frac{1}{\beta r_e} + \frac{1}{R_F} + \frac{R_C \| r_o}{\beta r_e R_F} + \frac{R_C \| r_o}{R_F r_e}} \quad (5.54)$$

Applying the condition  $r_o \geq 10R_C$ , we obtain

$$Z_i = \frac{1 + \frac{R_C}{R_F}}{\frac{1}{\beta r_e} + \frac{1}{R_F} + \frac{R_C}{\beta r_e R_F} + \frac{R_C}{R_F r_e}} = \frac{r_e \left[ 1 + \frac{R_C}{R_F} \right]}{\frac{1}{\beta} + \frac{1}{R_F} \left[ r_e + \frac{R_C}{\beta} + R_C \right]}$$

Applying  $R_C \gg r_e$  and  $\frac{R_C}{\beta}$ ,

$$Z_i \cong \frac{r_e \left[ 1 + \frac{R_C}{R_F} \right]}{\frac{1}{\beta} + \frac{R_C}{R_F}} = \frac{r_e \left[ \frac{R_F + R_C}{R_F} \right]}{\frac{R_F + \beta R_C}{\beta R_F}} = \frac{r_e}{\frac{1}{\beta} \left( \frac{R_F}{R_F + R_C} \right) + \frac{R_C}{R_C + R_F}}$$

but, since  $R_F$  typically  $\gg R_C$ ,  $R_F + R_C \cong R_F$  and  $\frac{R_F}{R_F + R_C} = 1$ 

$$Z_i \cong \frac{r_e}{\frac{1}{\beta} + \frac{R_C}{R_C + R_F}} \quad r_o \gg R_C, R_F > R_C \quad (5.55)$$

as obtained earlier.

**Z<sub>o</sub>** Including  $r_o$  in parallel with  $R_C$  in Fig. 5.47 results in

$$Z_o = r_o \| R_C \| R_F \quad (5.56)$$

For  $r_o \geq 10R_C$ ,

$$Z_o \cong R_C \| R_F \quad r_o \geq 10R_C \quad (5.57)$$

as obtained earlier. For the common condition of  $R_F \gg R_C$ ,

$$Z_o \cong R_C \quad r_o \geq 10R_C, R_F \gg R_C \quad (5.58)$$

$$A_v = -\left(\frac{R_F}{R_C + R_F}\right) \frac{R_C \| r_o}{r_e} \quad (5.59)$$

For  $r_o \geq 10R_C$ ,

$$A_v \cong -\left(\frac{R_F}{R_C + R_F}\right) \frac{R_C}{r_e} \quad r_o \geq 10R_C \quad (5.60)$$

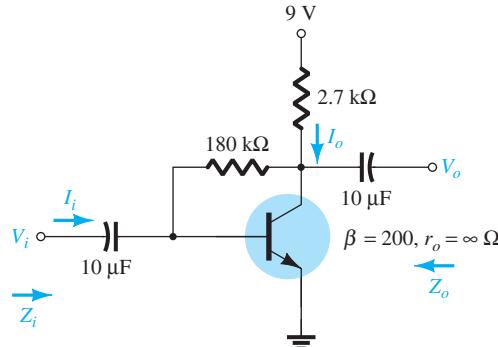
and for  $R_F \gg R_C$

$$A_v \cong -\frac{R_C}{r_e} \quad r_o \geq 10R_C, R_F \geq R_C \quad (5.61)$$

as obtained earlier.

**EXAMPLE 5.9** For the network of Fig. 5.48, determine:

- a.  $r_e$ .
- b.  $Z_i$ .
- c.  $Z_o$ .
- d.  $A_v$ .
- e. Repeat parts (b) through (d) with  $r_o = 20 \text{ k}\Omega$  and compare results.



**FIG. 5.48**  
Example 5.9.

**Solution:**

$$\begin{aligned} \text{a. } I_B &= \frac{V_{CC} - V_{BE}}{R_F + \beta R_C} = \frac{9 \text{ V} - 0.7 \text{ V}}{180 \text{ k}\Omega + (200)2.7 \text{ k}\Omega} \\ &= 11.53 \mu\text{A} \end{aligned}$$

$$I_E = (\beta + 1)I_B = (201)(11.53 \mu\text{A}) = 2.32 \text{ mA}$$

$$r_e = \frac{26 \text{ mV}}{I_E} = \frac{26 \text{ mV}}{2.32 \text{ mA}} = 11.21 \Omega$$

$$\begin{aligned} \text{b. } Z_i &= \frac{r_e}{\frac{1}{\beta} + \frac{R_C}{R_C + R_F}} = \frac{11.21 \Omega}{\frac{1}{200} + \frac{2.7 \text{ k}\Omega}{182.7 \text{ k}\Omega}} = \frac{11.21 \Omega}{0.005 + 0.0148} \\ &= \frac{11.21 \Omega}{0.0198} = 566.16 \Omega \end{aligned}$$

$$\text{c. } Z_o = R_C \| R_F = 2.7 \text{ k}\Omega \| 180 \text{ k}\Omega = 2.66 \text{ k}\Omega$$

$$\text{d. } A_v = -\frac{R_C}{r_e} = -\frac{2.7 \text{ k}\Omega}{11.21 \Omega} = -240.86$$

e.  $Z_i$ : The condition  $r_o \geq 10R_C$  is *not* satisfied. Therefore,

$$Z_i = \frac{1 + \frac{R_C \| r_o}{R_F}}{\frac{1}{\beta r_e} + \frac{1}{R_F} + \frac{R_C \| r_o}{\beta r_e R_F} + \frac{R_C \| r_o}{R_F r_e}} = \frac{1 + \frac{2.7 \text{ k}\Omega \| 20 \text{ k}\Omega}{180 \text{ k}\Omega}}{\frac{1}{(200)(11.21)} + \frac{1}{180 \text{ k}\Omega} + \frac{2.7 \text{ k}\Omega \| 20 \text{ k}\Omega}{(200)(11.21 \Omega)(180 \text{ k}\Omega)} + \frac{2.7 \text{ k}\Omega \| 20 \text{ k}\Omega}{(180 \text{ k}\Omega)(11.21 \Omega)}}$$

$$= \frac{1 + \frac{2.38 \text{ k}\Omega}{180 \text{ k}\Omega}}{0.45 \times 10^{-3} + 0.006 \times 10^{-3} + 5.91 \times 10^{-6} + 1.18 \times 10^{-3}} = \frac{1 + 0.013}{1.64 \times 10^{-3}}$$

$$= \mathbf{617.7 \Omega} \text{ vs. } 566.16 \Omega \text{ above}$$

**Z<sub>o</sub>:**

$$Z_o = r_o \| R_C \| R_F = 20 \text{ k}\Omega \| 2.7 \text{ k}\Omega \| 180 \text{ k}\Omega$$

$$= \mathbf{2.35 \text{ k}\Omega} \text{ vs. } 2.66 \text{ k}\Omega \text{ above}$$

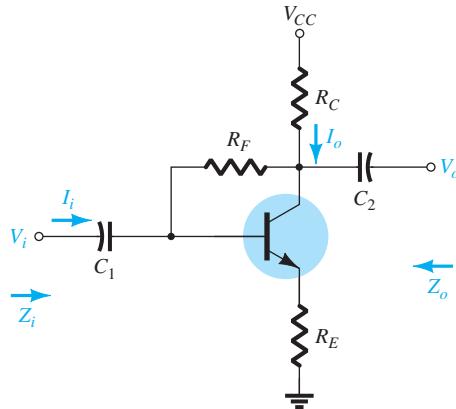
**A<sub>v</sub>:**

$$= -\left(\frac{R_F}{R_C \| r_o + R_F}\right) \frac{R_C \| r_o}{r_e} = -\left[\frac{180 \text{ k}\Omega}{2.38 \text{ k}\Omega + 180 \text{ k}\Omega}\right] \frac{2.38 \text{ k}\Omega}{11.21}$$

$$= -[0.987] 212.3$$

$$= \mathbf{-209.54}$$

For the configuration of Fig. 5.49, Eqs. (5.61) through (5.63) determine the variables of interest. The derivations are left as an exercise at the end of the chapter.



**FIG. 5.49**

Collector feedback configuration with an emitter resistor  $R_E$ .

**Z<sub>i</sub>**

$$Z_i \cong \frac{R_E}{\left[ \frac{1}{\beta} + \frac{(R_E + R_C)}{R_F} \right]} \quad (5.62)$$

**Z<sub>o</sub>**

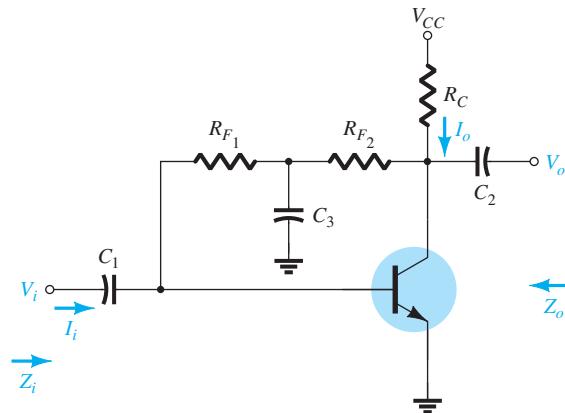
$$Z_o = R_C \| R_F \quad (5.63)$$

**A<sub>v</sub>**

$$A_v \cong -\frac{R_C}{R_E} \quad (5.64)$$

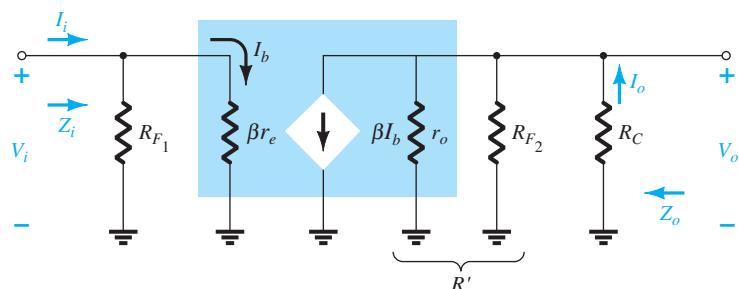
## 5.11 COLLECTOR DC FEEDBACK CONFIGURATION

The network of Fig. 5.50 has a dc feedback resistor for increased stability, yet the capacitor  $C_3$  will shift portions of the feedback resistance to the input and output sections of the network in the ac domain. The portion of  $R_F$  shifted to the input or output side will be determined by the desired ac input and output resistance levels.



**FIG. 5.50**  
Collector dc feedback configuration.

At the frequency or frequencies of operation, the capacitor will assume a short-circuit equivalent to ground due to its low impedance level compared to the other elements of the network. The small-signal ac equivalent circuit will then appear as shown in Fig. 5.51.



**FIG. 5.51**  
Substituting the  $r_e$  equivalent circuit into the ac equivalent network of Fig. 5.50.

**$Z_i$**

$$Z_i = R_{F1} \parallel \beta r_e \quad (5.65)$$

**$Z_o$**

$$Z_o = R_C \parallel R_{F2} \parallel r_o \quad (5.66)$$

For  $r_o \geq 10R_C$ ,

$$Z_o \cong R_C \parallel R_{F2} \quad r_o \geq 10R_C \quad (5.67)$$

**$A_v$**

$$R' = r_o \parallel R_{F2} \parallel R_C$$

and

$$V_o = -\beta I_b R'$$

but

$$I_b = \frac{V_i}{\beta r_e}$$

and

$$V_o = -\beta \frac{V_i}{\beta r_e} R'$$

so that

$$A_v = \frac{V_o}{V_i} = -\frac{r_o \| R_{F_2} \| R_C}{r_e} \quad (5.68)$$

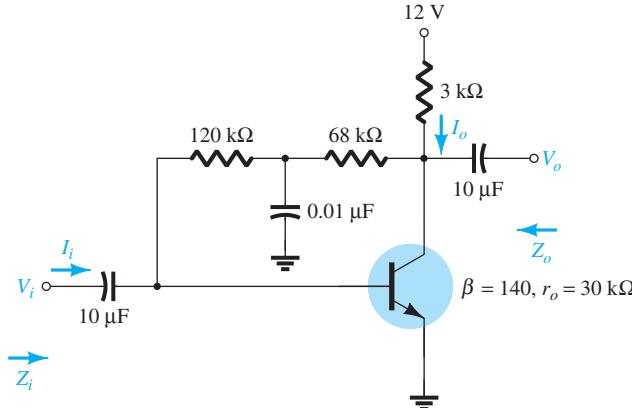
For  $r_o \geq 10R_C$ ,

$$A_v = \frac{V_o}{V_i} \cong -\frac{R_{F_2} \| R_C}{r_e} \quad (5.69)$$

**Phase Relationship** The negative sign in Eq. (5.68) clearly reveals a  $180^\circ$  phase shift between input and output voltages.

**EXAMPLE 5.10** For the network of Fig. 5.52, determine:

- a.  $r_e$ .
- b.  $Z_i$ .
- c.  $Z_o$ .
- d.  $A_v$ .
- e.  $V_o$  if  $V_i = 2 \text{ mV}$



**FIG. 5.52**  
Example 5.10.

**Solution:**

$$\begin{aligned} \text{a. DC: } I_B &= \frac{V_{CC} - V_{BE}}{R_F + \beta R_C} \\ &= \frac{12 \text{ V} - 0.7 \text{ V}}{(120 \text{ k}\Omega + 68 \text{ k}\Omega) + (140)3 \text{ k}\Omega} \\ &= \frac{11.3 \text{ V}}{608 \text{ k}\Omega} = 18.6 \mu\text{A} \end{aligned}$$

$$\begin{aligned} I_E &= (\beta + 1)I_B = (141)(18.6 \mu\text{A}) \\ &= 2.62 \text{ mA} \end{aligned}$$

$$r_e = \frac{26 \text{ mV}}{I_E} = \frac{26 \text{ mV}}{2.62 \text{ mA}} = 9.92 \Omega$$

$$\text{b. } \beta r_e = (140)(9.92 \Omega) = 1.39 \text{ k}\Omega$$

The ac equivalent network appears in Fig. 5.53.

$$\begin{aligned} Z_i &= R_{F_1} \| \beta r_e = 120 \text{ k}\Omega \| 1.39 \text{ k}\Omega \\ &\cong 1.37 \text{ k}\Omega \end{aligned}$$

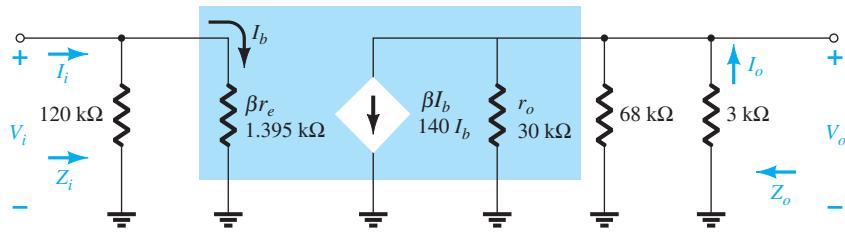


FIG. 5.53

Substituting the  $r_e$  equivalent circuit into the ac equivalent network of Fig. 5.52.

- c. Testing the condition  $r_o \geq 10R_C$ , we find

$$30 \text{ k}\Omega \geq 10(3 \text{ k}\Omega) = 30 \text{ k}\Omega$$

which is satisfied through the equals sign in the condition. Therefore,

$$\begin{aligned} Z_o &\equiv R_C \| R_{F_2} = 3 \text{ k}\Omega \| 68 \text{ k}\Omega \\ &= \mathbf{2.87 \text{ k}\Omega} \end{aligned}$$

- d.  $r_o \geq 10R_C$ ; therefore,

$$\begin{aligned} A_v &\equiv -\frac{R_{F_2} \| R_C}{r_e} = -\frac{68 \text{ k}\Omega \| 3 \text{ k}\Omega}{9.92 \text{ }\Omega} \\ &\equiv -\frac{2.87 \text{ k}\Omega}{9.92 \text{ }\Omega} \\ &\equiv \mathbf{-289.3} \end{aligned}$$

e.  $|A_v| = 289.3 = \frac{V_o}{V_i}$

$$V_o = 289.3V_i = 289.3(2 \text{ mV}) = \mathbf{0.579 \text{ V}}$$

## 5.12 EFFECT OF $R_L$ AND $R_s$

All the parameters determined in the last few sections have been for an unloaded amplifier with the input voltage connected directly to a terminal of the transistor. In this section the effect of applying a load to the output terminal and the effect of using a source with an internal resistance will be investigated. The network of Fig. 5.54a is typical of those investigated in the previous section. Because a resistive load was not attached to the output terminal, the gain is commonly referred to as the no-load gain and given the following notation:

$$A_{v_{NL}} = \frac{V_o}{V_i} \quad (5.70)$$

In Fig. 5.54b a load has been added in the form of a resistor  $R_L$ , which will change the overall gain of the system. This loaded gain is typically given the following notation:

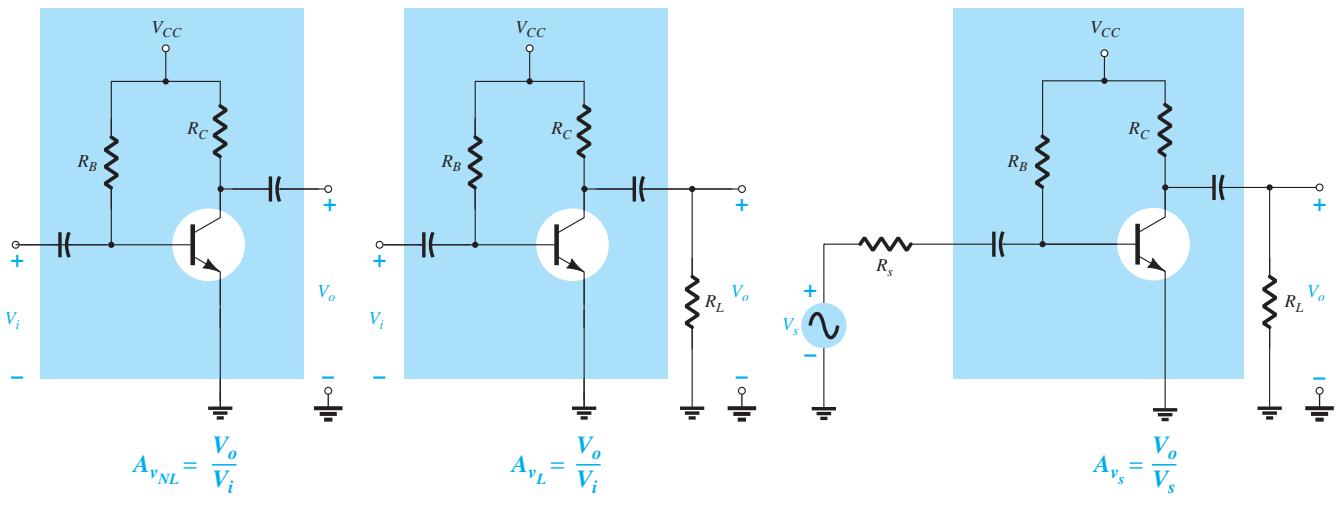
$$A_{v_L} = \frac{V_o}{V_i} \quad \text{with } R_L \quad (5.71)$$

In Fig. 5.54c both a load and a source resistance have been introduced, which will have an additional effect on the gain of the system. The resulting gain is typically given the following notation:

$$A_{v_s} = \frac{V_o}{V_s} \quad \text{with } R_L \text{ and } R_s \quad (5.72)$$

The analysis to follow will show that:

**The loaded voltage gain of an amplifier is always less than the no-load gain.**



**FIG. 5.54**

Amplifier configurations: (a) unloaded; (b) loaded; (c) loaded with a source resistance.

In other words, the addition of a load resistor  $R_L$  to the configuration of Fig. 5.54a will always have the effect of reducing the gain below the no-load level.

Furthermore:

**The gain obtained with a source resistance in place will always be less than that obtained under loaded or unloaded conditions due to the drop in applied voltage across the source resistance.**

In total, therefore, the highest gain is obtained under no-load conditions and the lowest gain with a source impedance and load in place. That is:

**For the same configuration  $A_{v_{NL}} > A_{v_L} > A_{v_s}$ .**

It will also be interesting to verify that:

**For a particular design, the larger the level of  $R_L$ , the greater is the level of ac gain.**

In other words, the larger the load resistance, the closer it is to an open-circuit approximation that would result in the higher no-load gain.

In addition:

**For a particular amplifier, the smaller the internal resistance of the signal source, the greater is the overall gain.**

In other words, the closer the source resistance is to a short-circuit approximation, the greater is the gain because the effect of  $R_s$  will essentially be eliminated.

**For any network, such as those shown in Fig. 5.54 that have coupling capacitors, the source and load resistance do not affect the dc biasing levels.**

The conclusions listed above are all quite important in the amplifier design process. When one purchases a packaged amplifier, the listed gain and all the other parameters are for the *unloaded situation*. The gain that results due to the application of a load or source resistance can have a dramatic effect on all the amplifier parameters, as will be demonstrated in the examples to follow.

In general, there are two directions one can take to analyze networks with an applied load and/or source resistance. One approach is to simply insert the equivalent circuit, as was demonstrated in Section 5.11, and use methods of analysis to determine the quantities of interest. The second is to define a two-port equivalent model and use the parameters determined for the no-load situation. The analysis to follow in this section will use the first approach, leaving the second method for Section 5.14.

For the fixed-bias transistor amplifier of Fig. 5.54c, substituting the  $r_e$  equivalent circuit for the transistor and removing the dc parameters results in the configuration of Fig. 5.55.

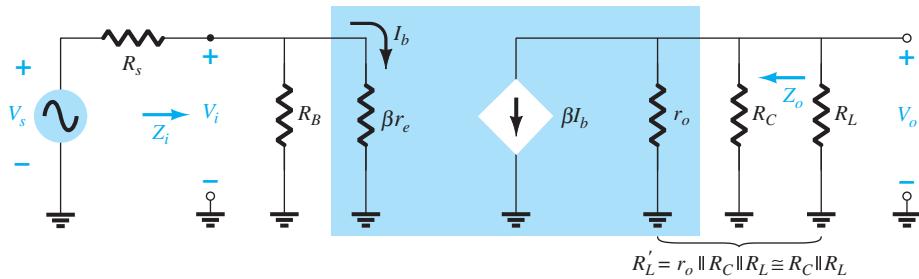


FIG. 5.55

The ac equivalent network for the network of Fig. 5.54c.

It is particularly interesting that Fig. 5.55 is exactly the same in appearance as Fig. 5.22 except that now there is a load resistance in parallel with  $R_C$  and a source resistance has been introduced in series with a source  $V_s$ .

The parallel combination of

$$R'_L = r_o \parallel R_C \parallel R_L \equiv R_C \parallel R_L$$

and

$$V_o = -\beta I_b R'_L = -\beta I_b (R_C \parallel R_L)$$

with

$$I_b = \frac{V_i}{\beta r_e}$$

gives

$$V_o = -\beta \left( \frac{V_i}{\beta r_e} \right) (R_C \parallel R_L)$$

so that

$$A_{v_L} = \frac{V_o}{V_i} = -\frac{R_C \parallel R_L}{r_e} \quad (5.73)$$

The only difference in the gain equation using  $V_i$  as the input voltage is the fact that  $R_C$  of Eq. (5.10) has been replaced by the parallel combination of  $R_C$  and  $R_L$ . This makes good sense because the output voltage of Fig. 5.55 is now across the parallel combination of the two resistors.

The input impedance is

$$Z_i = R_B \parallel \beta r_e \quad (5.74)$$

as before, and the output impedance is

$$Z_o = R_C \parallel r_o \quad (5.75)$$

as before.

If the overall gain from signal source  $V_s$  to output voltage  $V_o$  is desired, it is only necessary to apply the voltage-divider rule as follows:

$$V_i = \frac{Z_i V_s}{Z_i + R_s}$$

and

$$\frac{V_i}{V_s} = \frac{Z_i}{Z_i + R_s}$$

or

$$A_{v_s} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \cdot \frac{V_i}{V_s} = A_{v_L} \frac{Z_i}{Z_i + R_s}$$

so that

$$A_{v_s} = \frac{Z_i}{Z_i + R_s} A_{v_L} \quad (5.76)$$

Because the factor  $Z_i/(Z_i + R_s)$  must always be less than one, Eq. (5.76) clearly supports the fact that the signal gain  $A_{v_s}$  is always less than the loaded gain  $A_{v_L}$ .

**EXAMPLE 5.11** Using the parameter values for the fixed-bias configuration of Example 5.1 with an applied load of  $4.7 \text{ k}\Omega$  and a source resistance of  $0.3 \text{ k}\Omega$ , determine the following and compare to the no-load values:

- $A_{vL}$ .
- $A_{vs}$ .
- $Z_i$ .
- $Z_o$ .

**Solution:**

a. Eq. (5.73):  $A_{vL} = -\frac{R_C \| R_L}{r_e} = -\frac{3 \text{ k}\Omega \| 4.7 \text{ k}\Omega}{10.71 \Omega} = -\frac{1.831 \text{ k}\Omega}{10.71 \Omega} = -170.98$

which is significantly less than the no-load gain of  $-280.11$ .

b. Eq. (5.76):  $A_{vs} = \frac{Z_i}{Z_i + R_s} A_{vL}$

With  $Z_i = 1.07 \text{ k}\Omega$  from Example 5.1, we have

$$A_{vs} = \frac{1.07 \text{ k}\Omega}{1.07 \text{ k}\Omega + 0.3 \text{ k}\Omega} (-170.98) = -133.54$$

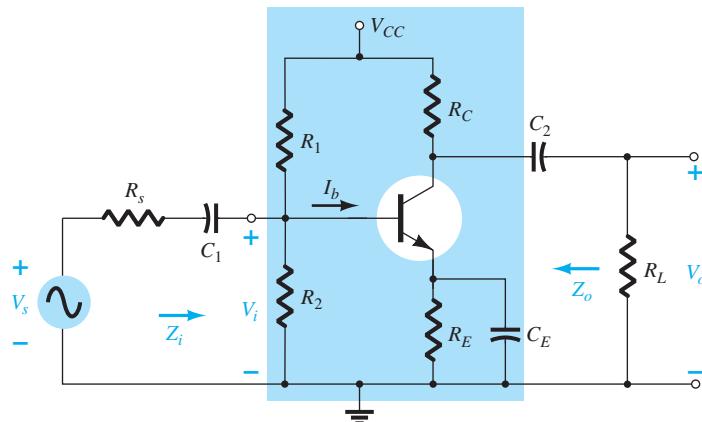
which again is significantly less than  $A_{vNL}$  or  $A_{vL}$ .

c.  $Z_i = 1.07 \text{ k}\Omega$  as obtained for the no-load situation.

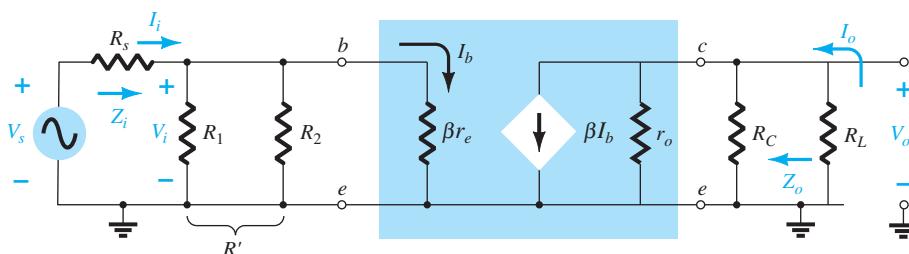
d.  $Z_o = R_C = 3 \text{ k}\Omega$  as obtained for the no-load situation.

The example clearly demonstrates that  $A_{vNL} > A_{vL} > A_{vs}$ .

For the voltage-divider configuration of Fig. 5.56 with an applied load and series source resistor the ac equivalent network is as shown in Fig. 5.57.



**FIG. 5.56**  
Voltage-divider bias configuration with  $R_s$  and  $R_L$ .



**FIG. 5.57**  
Substituting the  $r_e$  equivalent circuit into the ac equivalent network of Fig. 5.56.

First note the strong similarities with Fig. 5.55, with the only difference being the parallel connection of  $R_1$  and  $R_2$  instead of just  $R_B$ . Everything else is exactly the same. The following equations result for the important parameters of the configuration:

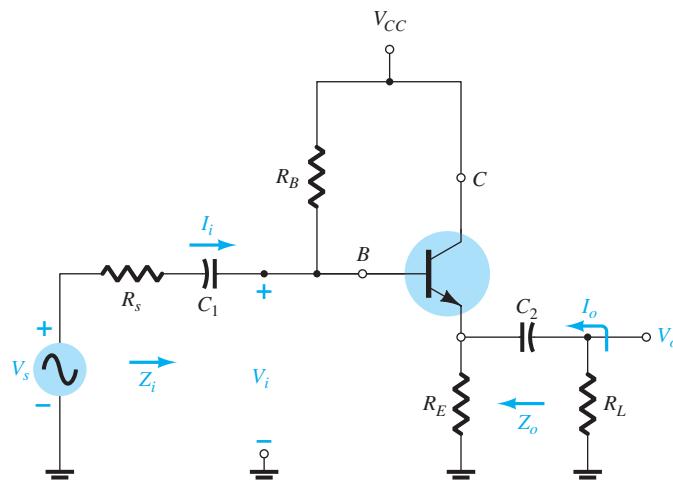
$$A_{v_L} = \frac{V_o}{V_i} = -\frac{R_C \parallel R_L}{r_e} \quad (5.77)$$

$$Z_i = R_1 \parallel R_2 \parallel \beta r_e \quad (5.78)$$

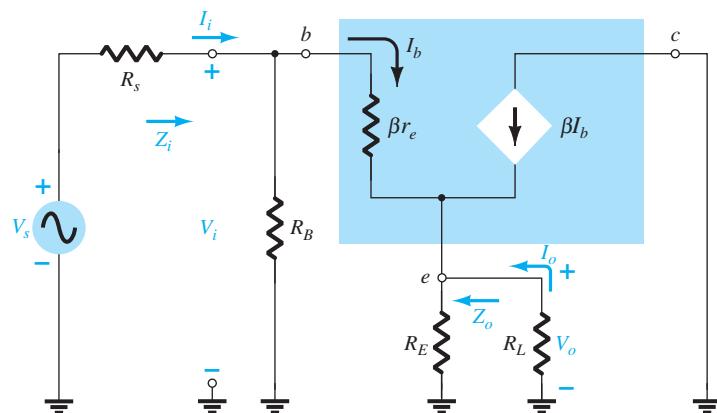
$$Z_o = R_C \parallel r_o \quad (5.79)$$

For the emitter-follower configuration of Fig. 5.58 the small-signal ac equivalent network is as shown in Fig. 5.59. The only difference between Fig. 5.59 and the unloaded configuration of Fig. 5.37 is the parallel combination of  $R_E$  and  $R_L$  and the addition of the source resistor  $R_s$ . The equations for the quantities of interest can therefore be determined by simply replacing  $R_E$  by  $R_E \parallel R_L$  wherever  $R_E$  appears. If  $R_E$  does not appear in an equation, the load resistor  $R_L$  does not affect that parameter. That is,

$$A_{v_L} = \frac{V_o}{V_i} = \frac{R_E \parallel R_L}{R_E \parallel R_L + r_e} \quad (5.80)$$



**FIG. 5.58**  
Emitter-follower configuration with  $R_s$  and  $R_L$ .



**FIG. 5.59**  
Substituting the  $r_e$  equivalent circuit into the ac equivalent network of Fig. 5.58.

$$Z_i = R_B \parallel Z_b$$

(5.81)

$$Z_b \cong \beta(R_E \parallel R_L)$$

(5.82)

$$Z_o \cong r_e$$

(5.83)

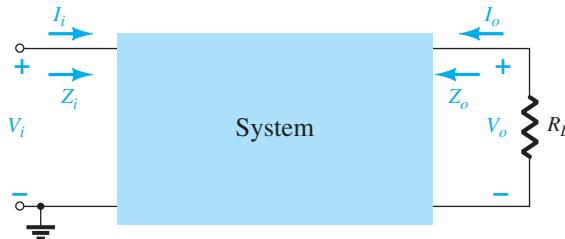
The effect of a load resistor and a source impedance on the remaining BJT configurations will not be examined in detail here, although Table 5.1 in Section 5.14 will review the results for each configuration.

## 5.13 DETERMINING THE CURRENT GAIN

You may have noticed in the previous sections that the current gain was not determined for each configuration. Earlier editions of this text did have the details of finding that gain, but in reality the voltage gain is usually the gain of most importance. The absence of the derivations should not cause concern because:

*For each transistor configuration, the current gain can be determined directly from the voltage gain, the defined load, and the input impedance.*

The derivation of the equation linking the voltage and current gains can be derived using the two-port configuration of Fig. 5.60.



**FIG. 5.60**  
Determining the current gain using the voltage gain.

The current gain is defined by

$$A_i = \frac{I_o}{I_i} \quad (5.84)$$

Applying Ohm's law to the input and output circuits results in

$$I_i = \frac{V_i}{Z_i} \quad \text{and} \quad I_o = -\frac{V_o}{R_L}$$

The minus sign associated with the output equation is simply there to indicate that the polarity of the output voltage is determined by an output current having the opposite direction. By definition, the input and output currents have a direction entering the two-port configuration.

Substituting into Eq. (5.84) then results in

$$A_{i_L} = \frac{I_o}{I_i} = \frac{-\frac{V_o}{R_L}}{\frac{V_i}{Z_i}} = -\frac{V_o}{V_i} \cdot \frac{Z_i}{R_L}$$

and the following important equation:

$$A_{i_L} = -A_{v_L} \frac{Z_i}{R_L}$$

(5.85)

The value of  $R_L$  is defined by the location of  $V_o$  and  $I_o$ .

To demonstrate the validity of Eq. (5.82), consider the voltage-divider bias configuration of Fig. 5.28.

Using the results of Example 5.2, we find

$$I_i = \frac{V_i}{Z_i} = \frac{V_i}{1.35 \text{ k}\Omega} \text{ and } I_o = -\frac{V_o}{R_L} = -\frac{V_o}{6.8 \text{ k}\Omega}$$

so that

$$A_{i_L} = \frac{I_o}{I_i} = \frac{\left(-\frac{V_o}{6.8 \text{ k}\Omega}\right)}{\frac{V_i}{1.35 \text{ k}\Omega}} = -\left(\frac{V_o}{V_i}\right)\left(\frac{1.35 \text{ k}\Omega}{6.8 \text{ k}\Omega}\right)$$

$$= -(-368.76)\left(\frac{1.35 \text{ k}\Omega}{6.8 \text{ k}\Omega}\right) = 73.2$$

$$\text{Using Eq. 5.82: } A_{i_L} = -A_{v_L} \frac{Z_i}{R_L} = -(-368.76)\left(\frac{1.35 \text{ k}\Omega}{6.8 \text{ k}\Omega}\right) = 73.2$$

which has the same format as the resulting equation above and the same result.

The solution to the current gain in terms of the network parameters will be more complicated for some configurations if a solution is desired in terms of the network parameters. However, if a numerical solution is all that is desired, it is simply a matter of substituting the value of the three parameters from an analysis of the voltage gain.

As a second example, consider the common-base bias configuration of Section 5.9. In this case the voltage gain is

$$A_{v_L} \cong \frac{R_C}{r_e}$$

and the input impedance is

$$Z_i \cong R_E \| r_e \cong r_e$$

with  $R_L$  defined as  $R_C$  due to the location of  $I_o$ .

The result is the following:

$$A_{i_L} = -A_{v_L} \frac{Z_i}{R_L} = \left(-\frac{R_C}{r_e}\right) \left(\frac{r_e}{R_C}\right) \cong -1$$

which agrees with the solution of that section because  $I_c \cong I_e$ . Note, in this case, that the output current has the opposite direction to that appearing in the networks of that section due to the minus sign.

## 5.14 SUMMARY TABLES

The last few sections have included a number of derivations for unloaded and loaded BJT configurations. The material is so extensive that it seemed appropriate to review most of the conclusions for the various configurations in summary tables for quick comparisons. Although the equations using the hybrid parameters have not been discussed in detail at this point, they are included to make the tables complete. The use of hybrid parameters will be considered in a later section of this chapter. In each case the waveforms included demonstrate the phase relationship between input and output voltages. They also reveal the relative magnitude of the voltages at the input and output terminals.

Table 5.1 is for the unloaded situation, whereas Table 5.2 includes the effect of  $R_s$  and  $R_L$ .

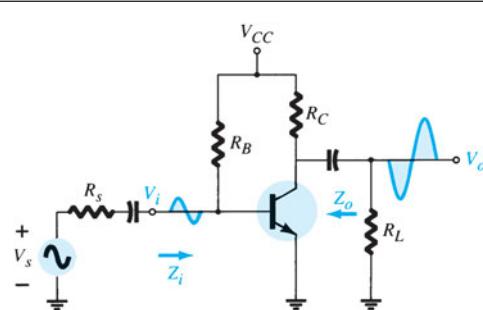
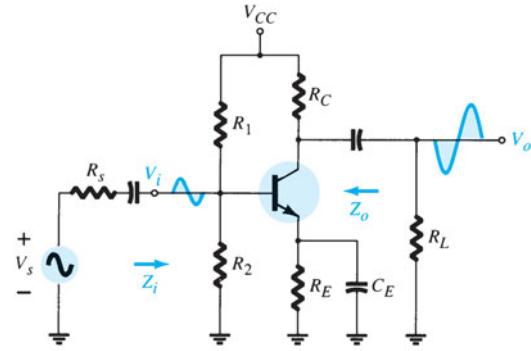
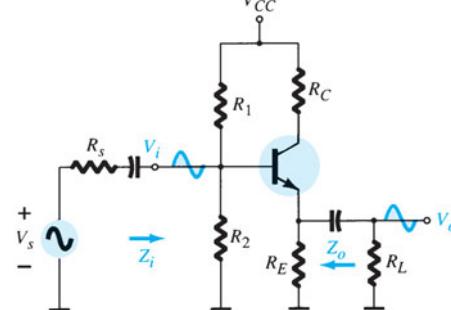
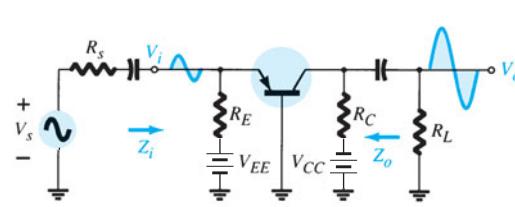
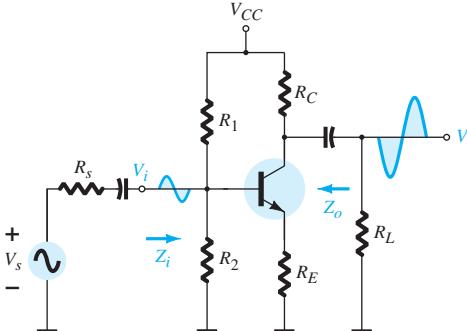
## 5.15 TWO-PORT SYSTEMS APPROACH

In the design process, it is often necessary to work with the terminal characteristics of a device rather than the individual components of the system. In other words, the designer is handed a packaged product with a list of data regarding its characteristics but has no access to the internal construction. This section will relate the important parameters determined for a number of configurations in the previous sections to the important parameters of this packaged system. The result will be an understanding of how each parameter of the

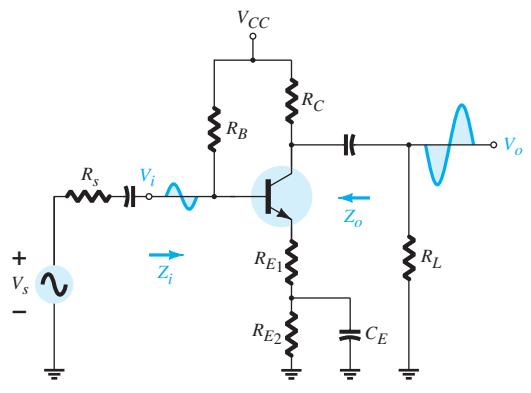
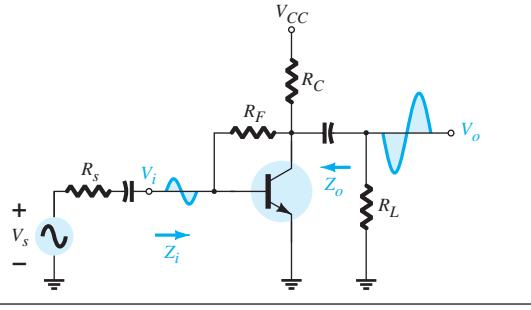
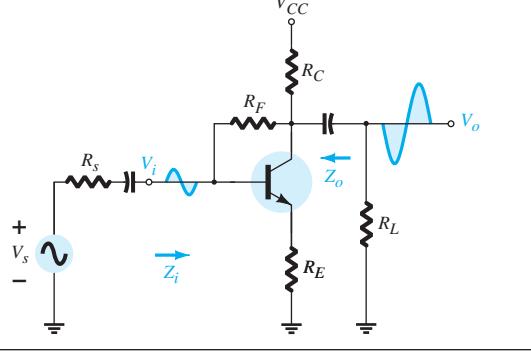
**TABLE 5.1**  
Unloaded BJT Transistor Amplifiers

Configuration	$Z_i$	$Z_o$	$A_v$	$A_i$
Fixed-bias:				
	Medium ( $1\text{ k}\Omega$ ) $= R_B \parallel \beta r_e$ $\approx \beta r_e$ $(R_B \geq 10\beta r_e)$	Medium ( $2\text{ k}\Omega$ ) $= R_C \parallel r_o$ $\approx R_C$ $(r_o \geq 10R_C)$	High ( $-200$ ) $= -\frac{(R_C \parallel r_o)}{r_e}$ $\approx -\frac{R_C}{r_e}$ $(r_o \geq 10R_C)$	High ( $100$ ) $= \frac{\beta R_B r_o}{(r_o + R_C)(R_B + \beta r_e)}$ $\approx \beta$ $(r_o \geq 10R_C, R_B \geq 10\beta r_e)$
Voltage-divider bias:				
	Medium ( $1\text{ k}\Omega$ ) $= R_1 \parallel R_2 \parallel \beta r_e$	Medium ( $2\text{ k}\Omega$ ) $= R_C \parallel r_o$ $\approx R_C$ $(r_o \geq 10R_C)$	High ( $-200$ ) $= -\frac{R_C \parallel r_o}{r_e}$ $\approx -\frac{R_C}{r_e}$ $(r_o \geq 10R_C)$	High ( $50$ ) $= \frac{\beta(R_1 \parallel R_2)r_o}{(r_o + R_C)(R_1 \parallel R_2 + \beta r_e)}$ $\approx \frac{\beta(R_1 \parallel R_2)}{R_1 \parallel R_2 + \beta r_e}$ $(r_o \geq 10R_C)$
Unbypassed emitter bias:				
	High ( $100\text{ k}\Omega$ ) $= R_B \parallel Z_b$ $Z_b \approx \beta(r_e + R_E)$ $\approx R_B \parallel \beta R_E$ $(R_E \gg r_e)$	Medium ( $2\text{ k}\Omega$ ) $= R_C$ $(\text{any level of } r_o)$	Low ( $-5$ ) $= -\frac{R_C}{r_e + R_E}$ $\approx -\frac{R_C}{R_E}$ $(R_E \gg r_e)$	High ( $50$ ) $\approx -\frac{\beta R_B}{R_B + Z_b}$
Emitter-follower:				
	High ( $100\text{ k}\Omega$ ) $= R_B \parallel Z_b$ $Z_b \approx \beta(r_e + R_E)$ $\approx R_B \parallel \beta R_E$ $(R_E \gg r_e)$	Low ( $20\ \Omega$ ) $= R_E \parallel r_e$ $\approx r_e$ $(R_E \gg r_e)$	Low ( $\approx 1$ ) $= \frac{R_E}{R_E + r_e}$ $\approx 1$	High ( $-50$ ) $\approx -\frac{\beta R_B}{R_B + Z_b}$
Common-base:				
	Low ( $20\ \Omega$ ) $= R_E \parallel r_e$ $\approx r_e$ $(R_E \gg r_e)$	Medium ( $2\text{ k}\Omega$ ) $= R_C$	High ( $200$ ) $\approx \frac{R_C}{r_e}$	Low ( $-1$ ) $\approx -1$
Collector feedback:				
	Medium ( $1\text{ k}\Omega$ ) $= \frac{r_e}{\frac{1}{\beta} + \frac{R_C}{R_F}}$ $\approx R_C \parallel R_F$ $(r_o \geq 10R_C)$	Medium ( $2\text{ k}\Omega$ ) $\approx -\frac{R_C}{r_e}$	High ( $-200$ ) $\approx -\frac{R_C}{r_e}$ $(r_o \geq 10R_C, R_F \gg R_C)$	High ( $50$ ) $= \frac{\beta R_F}{R_F + \beta R_C}$ $\approx \frac{R_F}{R_C}$

**TABLE 5.2**  
BJT Transistor Amplifiers Including the Effect of  $R_s$  and  $R_L$

Configuration	$A_{vL} = V_o/V_i$	$Z_i$	$Z_o$
	$\frac{-(R_L \parallel R_C)}{r_e}$	$R_B \parallel \beta r_e$	$R_C$
	Including $r_o$ : $\frac{-(R_L \parallel R_C \parallel r_o)}{r_e}$	$R_B \parallel \beta r_e$	$R_C \parallel r_o$
	$\frac{-(R_L \parallel R_C)}{r_e}$	$R_1 \parallel R_2 \parallel \beta r_e$	$R_C$
	Including $r_o$ : $\frac{-(R_L \parallel R_C \parallel r_o)}{r_e}$	$R_1 \parallel R_2 \parallel \beta r_e$	$R_C \parallel r_o$
	$\cong 1$	$R'_E = R_L \parallel R_E$ $R_1 \parallel R_2 \parallel \beta(r_e + R'_E)$	$R'_s = R_s \parallel R_1 \parallel R_2$ $R_E \parallel \left( \frac{R'_s}{\beta} + r_e \right)$
	Including $r_o$ : $\cong 1$	$R_1 \parallel R_2 \parallel \beta(r_e + R'_E)$	$R_E \parallel \left( \frac{R'_s}{\beta} + r_e \right)$
	$\cong \frac{-(R_L \parallel R_C)}{r_e}$	$R_E \parallel r_e$	$R_C$
	Including $r_o$ : $\cong \frac{-(R_L \parallel R_C \parallel r_o)}{r_e}$	$R_E \parallel r_e$	$R_C \parallel r_o$
	$\frac{-(R_L \parallel R_C)}{R_E}$	$R_1 \parallel R_2 \parallel \beta(r_e + R_E)$	$R_C$
	Including $r_o$ : $\frac{-(R_L \parallel R_C)}{R_E}$	$R_1 \parallel R_2 \parallel \beta(r_e + R_E)$	$\cong R_C$

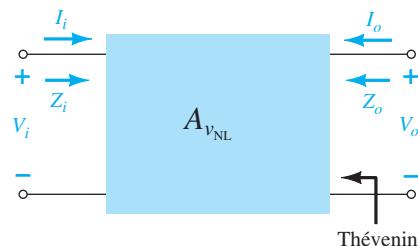
**TABLE 5.2 (Continued)**  
BJT Transistor Amplifiers Including the Effect of  $R_s$  and  $R_L$

Configuration	$A_{vL} = V_o/V_i$	$Z_i$	$Z_o$
	$\frac{-(R_L \  R_C)}{R_{E_1}}$	$R_B \  \beta(r_e + R_{E_1})$	$R_C$
	Including $r_o$ :	$\frac{-(R_L \  R_C)}{R_{E_t}}$	$\cong R_C$
	$\frac{-(R_L \  R_C)}{r_e}$	$\beta r_e \  \frac{R_F}{ A_v }$	$R_C$
	Including $r_o$ :	$\frac{-(R_L \  R_C \  r_o)}{r_e}$	$R_C \  R_F \  r_o$
	$\frac{-(R_L \  R_C)}{R_E}$	$\beta R_E \  \frac{R_F}{ A_v }$	$\cong R_C \  R_F$
	Including $r_o$ :	$\cong \frac{-(R_L \  R_C)}{R_E}$	$\cong \beta R_E \  \frac{R_F}{ A_v }$

packaged system relates to the actual amplifier or network. The system of Fig. 5.61 is called a two-port system because there are two sets of terminals—one at the input and the other at the output. At this point it is particularly important to realize that

**the data surrounding a packaged system is the no-load data.**

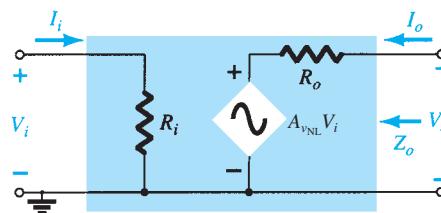
This should be fairly obvious because the load has not been applied, nor does it come with the load attached to the package.



**FIG. 5.61**  
Two-port system.

For the two-port system of Fig. 5.61 the polarity of the voltages and the direction of the currents are as defined. If the currents have a different direction or the voltages have a different polarity from that appearing in Fig. 5.61, a negative sign must be applied. Note again the use of the label  $A_{vNL}$  to indicate that the provided voltage gain will be the no-load value.

For amplifiers the parameters of importance have been sketched within the boundaries of the two-port system as shown in Fig. 5.62. The input and output resistance of a packaged amplifier are normally provided along with the no-load gain. They can then be inserted as shown in Fig. 5.62 to represent the seated package.



**FIG. 5.62**  
Substituting the internal elements for the two-port system of Fig. 5.61.

For the no-load situation the output voltage is

$$V_o = A_{vNL} V_i \quad (5.86)$$

due to the fact that  $I = 0A$ , resulting in  $I_o R_o = 0V$ .

The output resistance is defined by  $V_i = 0V$ . Under such conditions the quantity  $A_{vNL} V_i$  is zero volts also and can be replaced by a short-circuit equivalent. The result is

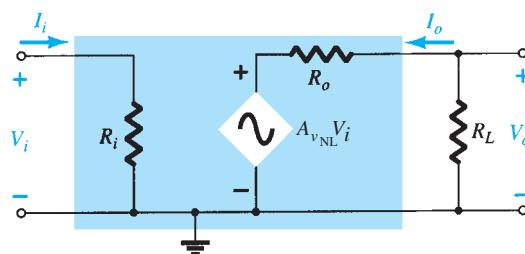
$$Z_o = R_o \quad (5.87)$$

Finally, the input impedance  $Z_i$  simply relates the applied voltage to the resulting input current and

$$Z_i = R_i \quad (5.88)$$

For the no-load situation, the current gain is undefined because the load current is zero. There is, however, a no-load voltage gain equal to  $A_{vNL}$ .

The effect of applying a load to a two-port system will result in the configuration of Fig. 5.63. Ideally, all the parameters of the model are unaffected by changing loads and levels of source resistance. However, for some transistor configurations the applied load can affect the input resistance, whereas for others the output resistance can be affected by the source resistance. In all cases, however, by simple definition, the no-load gain is unaffected by the application of any load. In any case, once  $A_{vNL}$ ,  $R_i$ , and  $R_o$  are defined for a particular configuration, the equations about to be derived can be employed.



**FIG. 5.63**  
Applying a load to the two-port system of Fig. 5.62.

Applying the voltage-divider rule to the output circuit results in

$$V_o = \frac{R_L A_{v_{NL}} V_i}{R_L + R_o}$$

and

$$A_{v_L} = \frac{V_o}{V_i} = \frac{R_L}{R_L + R_o} A_{v_{NL}} \quad (5.89)$$

Because the ratio  $R_L/(R_L + R_o)$  is always less than 1, we have further evidence that the loaded voltage gain of an amplifier is always less than the no-load level.

The current gain is then determined by

$$A_{i_L} = \frac{I_o}{I_i} = \frac{-V_o/R_L}{V_i/Z_i} = -\frac{V_o}{V_i} \frac{Z_i}{R_L}$$

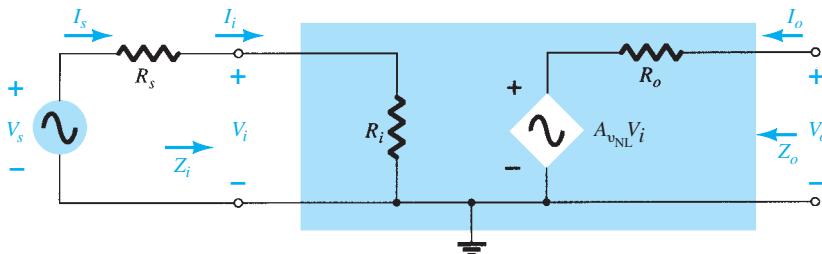
and

$$A_{i_L} = -A_{v_L} \frac{Z_i}{R_L} \quad (5.90)$$

as obtained earlier. In general, therefore, the current gain can be obtained from the voltage gain and impedance parameters  $Z_i$  and  $R_L$ . The next example will demonstrate the usefulness and validity of Eqs. (5.89) and (5.90).

Our attention will now turn to the input side of the two-port system and the effect of an internal source resistance on the gain of an amplifier. In Fig. 5.64, a source with an internal resistance has been applied to the basic two-port system. The definitions of  $Z_i$  and  $A_{v_{NL}}$  are such that:

**The parameters  $Z_i$  and  $A_{v_{NL}}$  of a two-port system are unaffected by the internal resistance of the applied source.**



**FIG. 5.64**  
Including the effects of the source resistance  $R_s$ .

However:

**The output impedance may be affected by the magnitude of  $R_s$ .**

The fraction of the applied signal reaching the input terminals of the amplifier of Fig. 5.64 is determined by the voltage-divider rule. That is,

$$V_i = \frac{R_i V_s}{R_i + R_s} \quad (5.91)$$

Equation (5.91) clearly shows that the larger the magnitude of  $R_s$ , the lower is the voltage at the input terminals of the amplifier. In general, therefore, as mentioned earlier, for a particular amplifier, the larger the internal resistance of a signal source, the lower is the overall gain of the system.

For the two-port system of Fig. 5.64,

$$V_o = A_{v_{NL}} V_i$$

and

$$V_i = \frac{R_i V_s}{R_i + R_s}$$

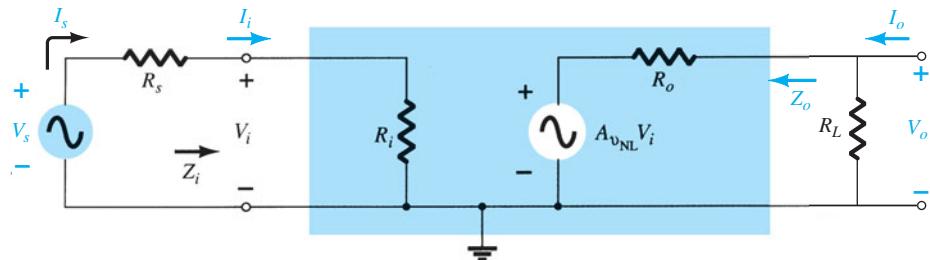
so that

$$V_o = A_{v_{NL}} \frac{R_i}{R_i + R_s} V_s$$

and

$$A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} A_{v_{NL}} \quad (5.92)$$

The effects of  $R_s$  and  $R_L$  have now been demonstrated on an individual basis. The next natural question is how the presence of both factors in the same network will affect the total gain. In Fig. 5.65, a source with an internal resistance  $R_s$  and a load  $R_L$  have been applied to a two-port system for which the parameters  $Z_i$ ,  $A_{v_{NL}}$ , and  $Z_o$  have been specified. For the moment, let us assume that  $Z_i$  and  $Z_o$  are unaffected by  $R_L$  and  $R_s$ , respectively.



**FIG. 5.65**  
Considering the effects of  $R_s$  and  $R_L$  on the gain of an amplifier.

At the input side we find

$$\text{Eq. (5.91): } V_i = \frac{R_i V_s}{R_i + R_s}$$

or

$$\frac{V_i}{V_s} = \frac{R_i}{R_i + R_s} \quad (5.93)$$

and at the output side,

$$V_o = \frac{R_L}{R_L + R_o} A_{v_{NL}} V_i$$

$$\text{or } A_{v_L} = \frac{V_o}{V_i} = \frac{R_L A_{v_{NL}}}{R_L + R_o} = \frac{R_L}{R_L + R_o} A_{v_{NL}} \quad (5.94)$$

For the total gain  $A_{v_s} = V_o/V_s$ , the following mathematical steps can be performed:

$$A_{v_s} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \cdot \frac{V_i}{V_s} \quad (5.95)$$

and substituting Eqs. (5.93) and (5.94) results in

$$A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} \cdot \frac{R_L}{R_L + R_o} A_{v_{NL}} \quad (5.96)$$

Because  $I_i = V_i/R_i$ , as before,

$$A_{i_L} = -A_{v_L} \frac{R_i}{R_L} \quad (5.97)$$

or, using  $I_s = V_s/(R_s + R_i)$ ,

$$A_{i_s} = -A_{v_s} \frac{R_s + R_i}{R_L} \quad (5.98)$$

However,  $I_i = I_s$ , so Eqs. (5.97) and (5.98) generate the same result. Equation (5.96) clearly reveals that both the source and the load resistance will reduce the overall gain of the system.

The two reduction factors of Eq. (5.96) form a product that has to be carefully considered in any design procedure. It is not sufficient to ensure that  $R_s$  is relatively small if the effect of the magnitude of  $R_L$  is ignored. For instance, in Eq. (5.96), if the first factor is 0.9 and the second factor is 0.2, the product of the two results in an overall reduction factor equal to  $(0.9)(0.2) = 0.18$ , which is close to the lower factor. The effect of the excellent 0.9 level was completely wiped out by the significantly lower second multiplier. If both were 0.9-level factors, the net result would be  $(0.9)(0.9) = 0.81$ , which is still quite high. Even if the first were 0.9 and the second 0.7, the net result of 0.63 would still be respectable. In general, therefore, for good overall gain the effects of  $R_s$  and  $R_L$  must be evaluated individually and as a product.

**EXAMPLE 5.12** Determine  $A_{v_L}$  and  $A_{v_s}$  for the network of Example 5.11 and compare solutions. Example 5.1 showed that  $A_{v_{NL}} = -280$ ,  $Z_i = 1.07 \text{ k}\Omega$ , and  $Z_o = 3 \text{ k}\Omega$ . In Example 5.11,  $R_L = 4.7 \text{ k}\Omega$  and  $R_s = 0.3 \text{ k}\Omega$ .

**Solution:**

$$\begin{aligned} \text{a. Eq. (5.89): } A_{v_L} &= \frac{R_L}{R_L + R_o} A_{v_{NL}} \\ &= \frac{4.7 \text{ k}\Omega}{4.7 \text{ k}\Omega + 3 \text{ k}\Omega} (-280.11) \\ &= \mathbf{-170.98} \end{aligned}$$

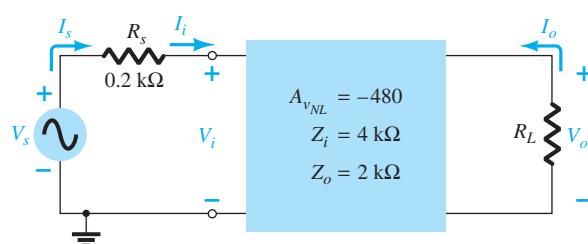
as in Example 5.11.

$$\begin{aligned} \text{b. Eq. (5.96): } A_{v_s} &= \frac{R_i}{R_i + R_s} \cdot \frac{R_L}{R_L + R_o} A_{v_{NL}} \\ &= \frac{1.07 \text{ k}\Omega}{1.07 \text{ k}\Omega + 0.3 \text{ k}\Omega} \cdot \frac{4.7 \text{ k}\Omega}{4.7 \text{ k}\Omega + 3 \text{ k}\Omega} (-280.11) \\ &= (0.781)(0.610)(-280.11) \\ &= \mathbf{-133.45} \end{aligned}$$

as in Example 5.11.

**EXAMPLE 5.13** Given the packaged (no-entry-possible) amplifier of Fig. 5.66:

- Determine the gain  $A_{v_L}$  and compare it to the no-load value with  $R_L = 1.2 \text{ k}\Omega$ .
- Repeat part (a) with  $R_L = 5.6 \text{ k}\Omega$  and compare solutions.
- Determine  $A_{v_s}$  with  $R_L = 1.2 \text{ k}\Omega$ .
- Find the current gain  $A_i = \frac{I_o}{I_i} = \frac{I_o}{I_s}$  with  $R_L = 5.6 \text{ k}\Omega$ .



**FIG. 5.66**  
Amplifier for Example 5.13.

**Solution:**

$$\begin{aligned}
 \text{a. Eq. (5.89): } A_{v_L} &= \frac{R_L}{R_L + R_o} A_{v_{NL}} \\
 &= \frac{1.2 \text{ k}\Omega}{1.2 \text{ k}\Omega + 2 \text{ k}\Omega} (-480) = (0.375)(-480) \\
 &= \mathbf{-180}
 \end{aligned}$$

which is a dramatic drop from the no-load value.

$$\begin{aligned}
 \text{b. Eq. (5.89): } A_{v_L} &= \frac{R_L}{R_L + R_o} A_{v_{NL}} \\
 &= \frac{5.6 \text{ k}\Omega}{5.6 \text{ k}\Omega + 2 \text{ k}\Omega} (-480) = (0.737)(-480) \\
 &= \mathbf{-353.76}
 \end{aligned}$$

which clearly reveals that the larger the load resistor, the better is the gain.

$$\begin{aligned}
 \text{c. Eq. (5.96): } A_{v_s} &= \frac{R_i}{R_i + R_s} \cdot \frac{R_L}{R_L + R_o} A_{v_{NL}} \\
 &= \frac{4 \text{ k}\Omega}{4 \text{ k}\Omega + 0.2 \text{ k}\Omega} \cdot \frac{1.2 \text{ k}\Omega}{1.2 \text{ k}\Omega + 2 \text{ k}\Omega} (-480) \\
 &= (0.952)(0.375)(-480) \\
 &= \mathbf{-171.36}
 \end{aligned}$$

which is fairly close to the loaded gain  $A_v$  because the input impedance is considerably more than the source resistance. In other words, the source resistance is relatively small compared to the input impedance of the amplifier.

$$\begin{aligned}
 \text{d. } A_{i_L} &= \frac{I_o}{I_i} = \frac{I_o}{I_s} = -A_{v_L} \frac{Z_i}{R_L} \\
 &= -(-353.76) \left( \frac{4 \text{ k}\Omega}{5.6 \text{ k}\Omega} \right) = -(-353.76)(0.714) \\
 &= \mathbf{252.6}
 \end{aligned}$$


---

It is important to realize that when using the two-port equations in some configurations the input impedance is sensitive to the applied load (such as the emitter-follower and collector feedback) and in some the output impedance is sensitive to the applied source resistance (such as the emitter-follower). In such cases the no-load parameters for  $Z_i$  and  $Z_o$  have to first be calculated before substituting into the two-port equations. For most packaged systems such as op-amps this sensitivity of the input and output parameters to the applied load or source resistance is minimized to eliminate the need to be concerned about changes from the no-load levels when using the two-port equations.

## 5.16 CASCADED SYSTEMS

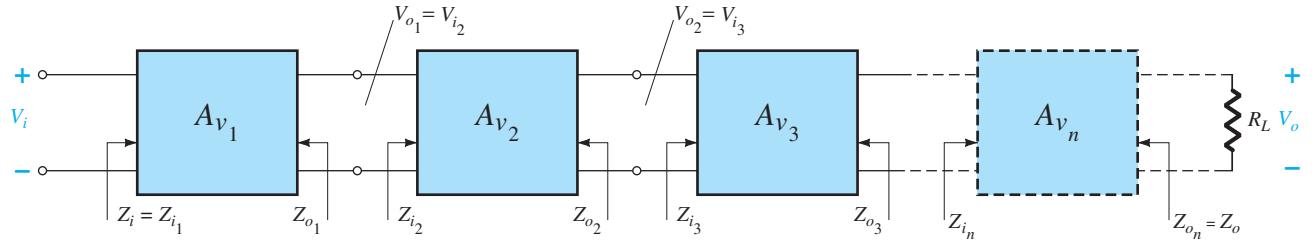
The two-port systems approach is particularly useful for cascaded systems such as that appearing in Fig. 5.67, where  $A_{v_1}$ ,  $A_{v_2}$ ,  $A_{v_3}$ , and so on, are the voltage gains of each stage *under loaded conditions*. That is,  $A_{v_1}$  is determined with the *input impedance to  $A_{v_2}$  acting as the load on  $A_{v_1}$* . For  $A_{v_2}$ ,  $A_{v_1}$  will determine the signal strength and source impedance at the input to  $A_{v_2}$ . The total gain of the system is then determined by the product of the individual gains as follows:

$$A_{v_T} = A_{v_1} \cdot A_{v_2} \cdot A_{v_3} \cdots \quad (5.99)$$

and the total current gain is given by

$$A_{i_T} = -A_{v_T} \frac{Z_{i_1}}{R_L} \quad (5.100)$$

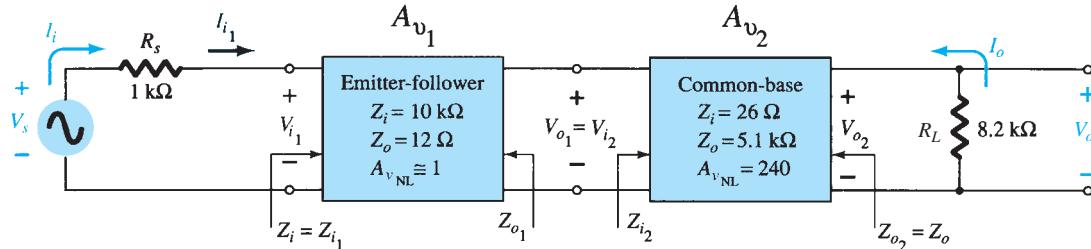
No matter how perfect the system design, the application of a succeeding stage or load to a two-port system will affect the voltage gain. Therefore, there is no possibility of a situation where  $A_{v_1}$ ,  $A_{v_2}$ , and so on, of Fig. 5.67 are simply the no-load values. The no-load parameters can be used to determine the loaded gains of each stage, but Eq. (5.99) requires the loaded values. The load on stage 1 is  $Z_{i_2}$ , on stage 2  $Z_{i_3}$ , on stage 3  $Z_{i_n}$ , and so on.



**FIG. 5.67**  
Cascaded system.

**EXAMPLE 5.14** The two-stage system of Fig. 5.68 employs a transistor emitter-follower configuration prior to a common-base configuration to ensure that the maximum percentage of the applied signal appears at the input terminals of the common-base amplifier. In Fig. 5.68, the no-load values are provided for each system, with the exception of  $Z_i$  and  $Z_o$  for the emitter-follower, which are the loaded values. For the configuration of Fig. 5.68, determine:

- The loaded gain for each stage.
- The total gain for the system,  $A_v$  and  $A_{v_s}$ .
- The total current gain for the system.
- The total gain for the system if the emitter-follower configuration were removed.



**FIG. 5.68**  
Example 5.14.

### Solution:

- For the emitter-follower configuration, the loaded gain is (by Eq. (5.94))

$$V_{o1} = \frac{Z_{i2}}{Z_{i2} + Z_{o1}} A_{v_{NL}} V_{i1} = \frac{26 \Omega}{26 \Omega + 12 \Omega} (1) V_{i1} = 0.684 V_{i1}$$

$$\text{and } A_{V_i} = \frac{V_{o1}}{V_{i1}} = 0.684$$

For the common-base configuration,

$$V_{o2} = \frac{R_L}{R_L + R_{o2}} A_{v_{NL}} V_{i2} = \frac{8.2 \text{ k}\Omega}{8.2 \text{ k}\Omega + 5.1 \text{ k}\Omega} (240) V_{i2} = 147.97 V_{i2}$$

$$\text{and } A_{V_2} = \frac{V_{o2}}{V_{i2}} = 147.97$$

- Eq. (5.99):  $A_{v_T} = A_{v_1} A_{v_2}$   
 $= (0.684)(147.97)$   
 $= 101.20$

$$\text{Eq. (5.91): } A_{v_s} = \frac{Z_{i_1}}{Z_{i_1} + R_s} A_{v_T} = \frac{(10 \text{ k}\Omega)(101.20)}{10 \text{ k}\Omega + 1 \text{ k}\Omega} = 92$$

$$\text{c. Eq. (5.100): } A_{i_T} = -A_{v_T} \frac{Z_{i_1}}{R_L} = -(101.20) \left( \frac{10 \text{ k}\Omega}{8.2 \text{ k}\Omega} \right) = -123.41$$

$$\text{d. Eq. (5.91): } V_i = \frac{Z_{i_{CB}}}{Z_{i_{CB}} + R_s} V_s = \frac{26 \Omega}{26 \Omega + 1 \text{ k}\Omega} V_s = 0.025 V_s$$

$$\text{and } \frac{V_i}{V_s} = 0.025 \quad \text{with } \frac{V_o}{V_i} = 147.97 \quad \text{from above}$$

$$\text{and } A_{v_s} = \frac{V_o}{V_s} = \frac{V_i}{V_s} \cdot \frac{V_o}{V_i} = (0.025)(147.97) = 3.7$$

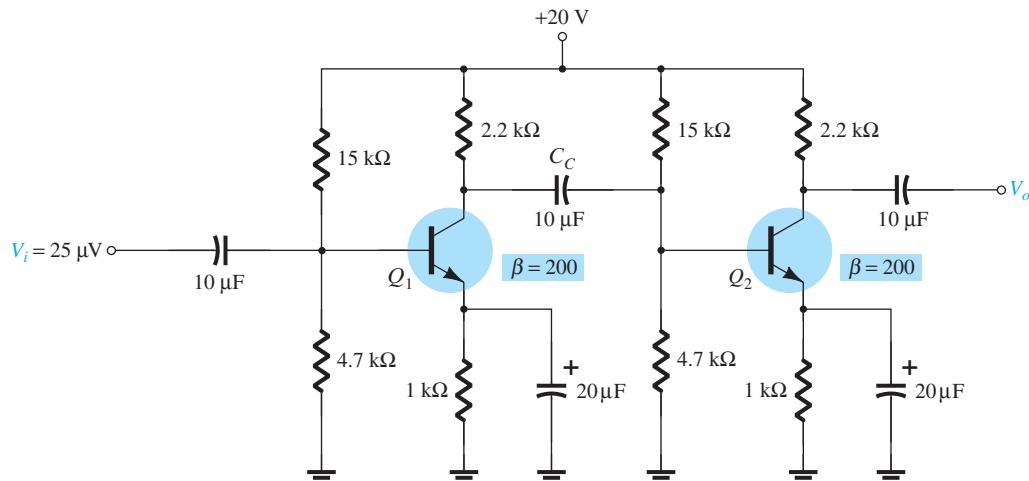
In total, therefore, the gain is about 25 times greater with the emitter-follower configuration to draw the signal to the amplifier stages. Note, however, that it is also important that the output impedance of the first stage is relatively close to the input impedance of the second stage, otherwise the signal would have been “lost” again by the voltage-divider action.

### RC-Coupled BJT Amplifiers

One popular connection of amplifier stages is the *RC*-coupled variety shown in Fig. 5.69 in the next example. The name is derived from the capacitive coupling capacitor  $C_c$  and the fact that the load on the first stage is an *RC* combination. The coupling capacitor isolates the two stages from a dc viewpoint but acts as a short-circuit equivalent for the ac response. The input impedance of the second stage acts as a load on the first stage, permitting the same approach to the analysis as described in the last two sections.

#### EXAMPLE 5.15

- Calculate the no-load voltage gain and output voltage of the *RC*-coupled transistor amplifiers of Fig. 5.69.
- Calculate the overall gain and output voltage if a  $4.7 \text{ k}\Omega$  load is applied to the second stage, and compare to the results of part (a).
- Calculate the input impedance of the first stage and the output impedance of the second stage.



**FIG. 5.69**  
*RC-coupled BJT amplifier for Example 5.15.*

#### Solution:

- The dc bias analysis results in the following for each transistor:

$$V_B = 4.8 \text{ V}, \quad V_E = 4.1 \text{ V}, \quad V_C = 11 \text{ V}, \quad I_E = 4.1 \text{ mA}$$

$$r_e = \frac{26 \text{ mV}}{I_E} = \frac{26 \text{ mV}}{4.1 \text{ mA}} = 6.34 \Omega$$

The loading of the second stage is

$$Z_{i_2} = R_1 \| R_2 \| \beta r_e$$

which results in the following gain for the first stage:

$$\begin{aligned} A_{v_1} &= -\frac{R_C \| (R_1 \| R_2 \| \beta r_e)}{r_e} \\ &= -\frac{(2.2 \text{ k}\Omega) \| [15 \text{ k}\Omega \| 4.7 \text{ k}\Omega \| (200)(6.34 \Omega)]}{6.34 \Omega} \\ &= -\frac{659.2 \Omega}{6.34 \Omega} = -104 \end{aligned}$$

For the unloaded second stage the gain is

$$A_{v_{2(\text{NL})}} = -\frac{R_C}{r_e} = -\frac{2.2 \text{ k}\Omega}{6.34 \Omega} = -347$$

resulting in an overall gain of

$$A_{v_{T(\text{NL})}} = A_{v_1} A_{v_{2(\text{NL})}} = (-104)(-347) \cong 36.1 \times 10^3$$

The output voltage is then

$$V_o = A_{v_{T(\text{NL})}} V_i = (36.1 \times 10^3)(25 \mu\text{V}) \cong 902.5 \text{ mV}$$

b. The overall gain with the 10-kΩ load applied is

$$A_{v_T} = \frac{V_o}{V_i} = \frac{R_L}{R_L + Z_o} A_{v_{T(\text{NL})}} = \frac{4.7 \text{ k}\Omega}{4.7 \text{ k}\Omega + 2.2 \text{ k}\Omega} (36.1 \times 10^3) \cong 24.6 \times 10^3$$

which is considerably less than the unloaded gain because  $R_L$  is relatively close to  $R_C$ .

$$\begin{aligned} V_o &= A_{v_T} V_i \\ &= (24.6 \times 10^3)(25 \mu\text{V}) \\ &= 615 \text{ mV} \end{aligned}$$

c. The input impedance of the first stage is

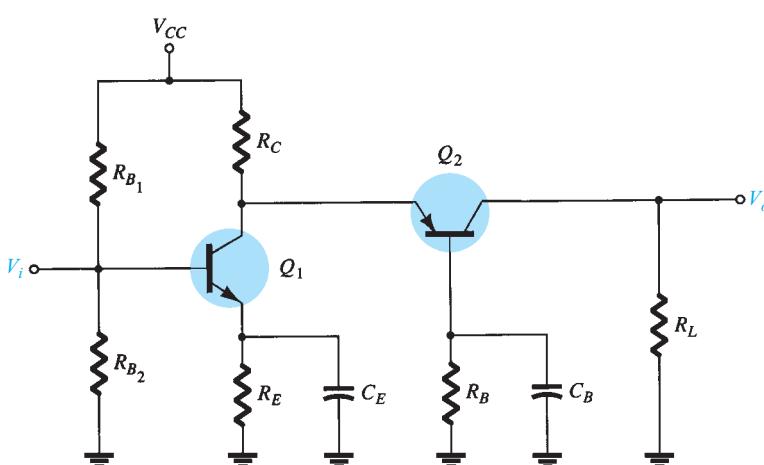
$$Z_{i_1} = R_1 \| R_2 \| \beta r_e = 4.7 \text{ k}\Omega \| 15 \text{ k}\Omega \| (200)(6.34 \Omega) = 0.94 \text{ k}\Omega$$

whereas the output impedance for the second stage is

$$Z_{o_2} = R_C = 2.2 \text{ k}\Omega$$

## Cascode Connection

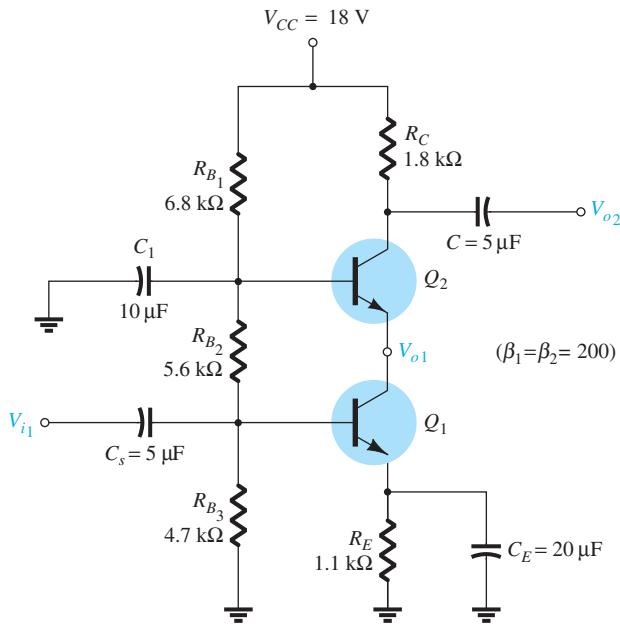
The cascode configuration has one of two configurations. In each case the collector of the leading transistor is connected to the emitter of the following transistor. One possible arrangement appears in Fig. 5.70; the second is shown in Fig. 5.71 in the following example.



**FIG. 5.70**  
Cascode configuration.

The arrangements provide a relatively high-input impedance with low voltage gain for the first stage to ensure the input Miller capacitance (to be discussed in Section 9.9) is at a minimum, whereas the following CB stage provides an excellent high-frequency response.

**EXAMPLE 5.16** Calculate the no-load voltage gain for the cascode configuration of Fig. 5.71.



**FIG. 5.71**  
Practical cascode circuit for Example 5.16.

**Solution:** The dc analysis results in

$$V_{B_1} = 4.9 \text{ V}, \quad V_{B_2} = 10.8 \text{ V}, \quad I_{C_1} \approx I_{C_2} = 3.8 \text{ mA}$$

because  $I_{E_1} \approx I_{E_2}$  the dynamic resistance for each transistor is

$$r_e = \frac{26 \text{ mV}}{I_E} \approx \frac{26 \text{ mV}}{3.8 \text{ mA}} = 6.8 \Omega$$

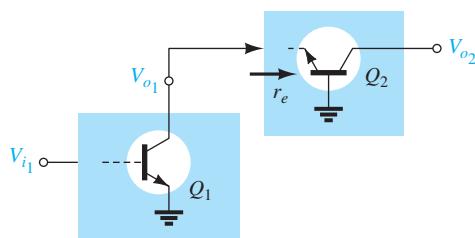
The loading on the transistor  $Q_1$  is the input impedance of the  $Q_2$  transistor in the CB configuration as shown by  $r_e$  in Fig 5.72.

The result is the replacement of  $R_C$  in the basic no-load equation for the gain of the CB configuration, with the input impedance of a CB configuration as follows:

$$A_{v1} = -\frac{R_C}{r_e} = -\frac{r_e}{r_e} = -1$$

with the voltage gain for the second stage (common base) of

$$A_{v2} = \frac{R_C}{r_e} = \frac{1.8 \text{ k}\Omega}{6.8 \Omega} = 265$$

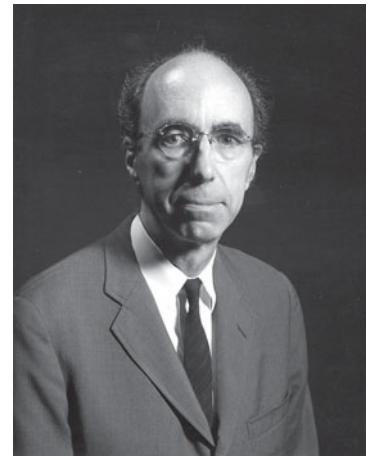


**FIG. 5.72**  
Defining the load of  $Q_1$ .

The overall no-load gain is

$$A_{v_T} = A_{v_1} A_{v_2} = (-1)(265) = -265$$

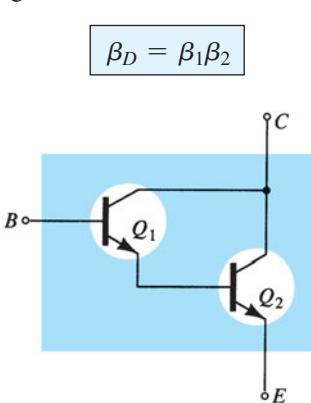
As expected, in Example 5.16, the CE stage provides a higher input impedance than can be expected from the CB stage. With a voltage gain of about 1 for the first stage, the Miller-effect input capacitance is kept quite low to support a good high-frequency response. A large voltage gain of 265 was provided by the CB stage to give the overall design a good input impedance level with desirable gain levels.



American (Pittsburgh, PA; Exeter, NH)  
(1906–1997)

**Department Head at Bell Laboratories**  
Professor, Department of Electrical and Computer Engineering, University of New Hampshire

Dr. Sidney Darlington earned his B.S. in physics at Harvard, his B.S. in electrical communication at MIT, and his Ph.D. at Columbia University. In 1929 he joined Bell Laboratories, where he was head of the Circuits and Control Department. During that period he became good friends with other important contributors such as Edward Norton and Hendrik Bode. A holder of 24 U.S. patents, he was awarded the Presidential Medal of Freedom, the highest civilian honor in the United States, in 1945 for his contributions to network design during World War II. An elected member of the National Academy of Engineering, he also received the IEEE Edison Medal in 1975 and the IEEE Medal of Honor in 1981. His U.S. patent 2 663 806 titled "Semiconductor Signal Translating Device" was issued on December 22, 1953, describing how two transistors could be constructed in the Darlington configuration on the same substrate—often looked upon as the beginnings of compound IC construction. Dr. Darlington was also responsible for the introduction and development of the Chirp technique, used throughout the world in waveguide transmission and radar systems. He is a primary contributor to the Bell Laboratories Command Guidance System that guides most of the rockets used today to place satellites in orbit. It uses a combination of radar tracking on the ground with inertial control in the rocket itself. Dr. Darlington was an avid outdoorsman as a hiker and member of the Appalachian Mountain Club. One of his proudest accomplishments was being able to climb Mt. Washington at the age of 80.

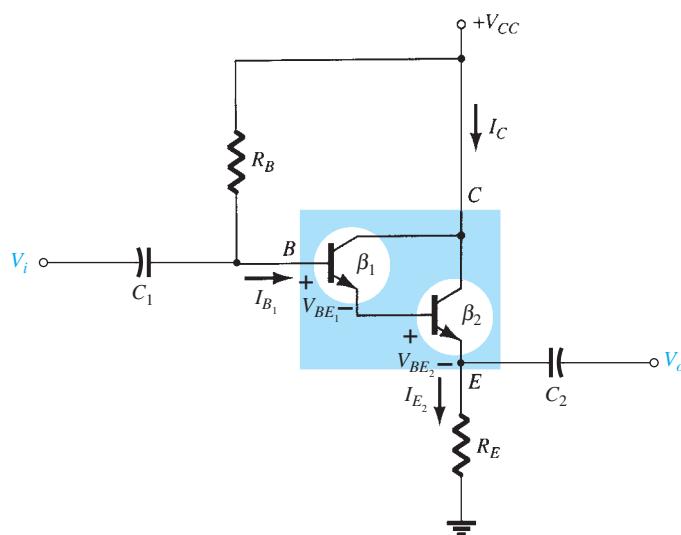


**FIG. 5.73**  
Darlington combination.

The configuration was first introduced by Dr. Sidney Darlington in 1953. A short biography appears as Fig 5.74.

### Emitter-Follower Configuration

A Darlington amplifier used in an emitter-follower configuration appears in Fig. 5.75. The primary impact of using the Darlington configuration is an input impedance much larger than



**FIG. 5.75**  
Emitter-follower configuration with a Darlington amplifier.

**FIG. 5.74**

Sidney Darlington (Courtesy of AT&T Archives and History Center.)

that obtained with a single-transistor network. The current gain is also larger, but the voltage gain for a single-transistor or Darlington configuration remains slightly less than one.

**DC Bias** The case current is determined using a modified version of Eq. 4.44. There are now two base-to-emitter voltage drops to include and the beta of a single transistor is replaced by the Darlington combination of Eq. 5.101.

$$I_{B_1} = \frac{V_{CC} - V_{BE_1} - V_{BE_2}}{R_B + \beta_D R_E} \quad (5.102)$$

The emitter current of  $Q_1$  is equal to the base current of  $Q_2$  so that

$$I_{E_2} = \beta_2 I_{B_2} = \beta_2 I_{E_1} = \beta_2 (\beta_1 I_{E_1}) = \beta_1 \beta_2 I_{B_1}$$

resulting in

$$I_{C_2} \cong I_{E_2} = \beta_D I_{B_1} \quad (5.103)$$

The collector voltage of both transistors is

$$V_{C_1} = V_{C_2} = V_{CC} \quad (5.104)$$

the emitter voltage of  $Q_2$

$$V_{E_2} = I_{E_2} R_E \quad (5.105)$$

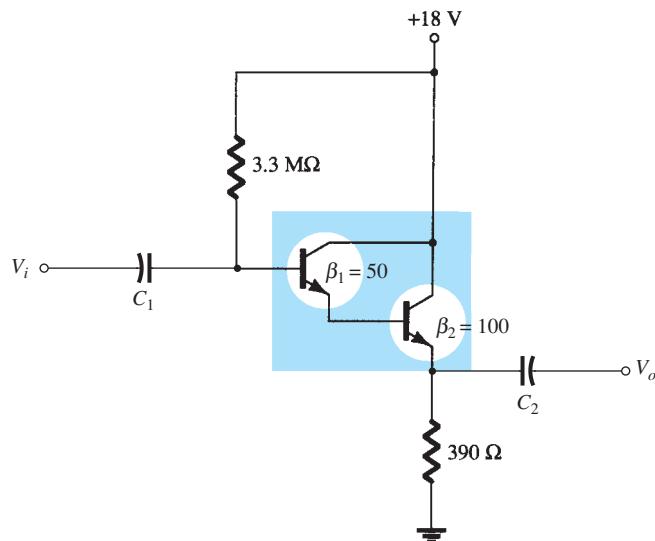
the base voltage of  $Q_1$

$$V_{B_1} = V_{CC} - I_{B_1} R_B = V_{E_2} + V_{BE_1} + V_{BE_2} \quad (5.106)$$

the collector-emitter voltage of  $Q$

$$V_{CE_2} = V_{C_2} - V_{E_2} = V_{CC} - V_{E_2} \quad (5.107)$$

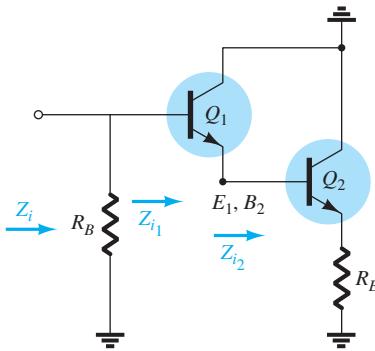
**EXAMPLE 5.17** Calculate the dc bias voltages and currents for the Darlington configuration of Fig. 5.76.



**FIG. 5.76**  
Circuit for Example 5.17.

$$\begin{aligned}
 \beta_D &= \beta_1\beta_2 = (50)(100) = 5000 \\
 I_{B_1} &= \frac{V_{CC} - V_{BE_1} - V_{BE_2}}{R_B + \beta_D R_E} = \frac{18 \text{ V} - 0.7 \text{ V} - 0.7 \text{ V}}{3.3 \text{ M}\Omega + (5000)(390 \text{ }\Omega)} \\
 &= \frac{18 \text{ V} - 1.4 \text{ V}}{3.3 \text{ M}\Omega + 1.95 \text{ M}\Omega} = \frac{16.6 \text{ V}}{5.25 \text{ M}\Omega} = 3.16 \mu\text{A} \\
 I_{C_2} &\cong I_{E_2} = \beta_D I_{B_1} = (5000)(3.16 \text{ mA}) = 15.80 \text{ mA} \\
 V_{C_1} &= V_{C_2} = 18 \text{ V} \\
 V_{E_2} &= I_{E_2} R_E = (15.80 \text{ mA})(390 \text{ }\Omega) = 6.16 \text{ V} \\
 V_{B_1} &= V_{E_2} + V_{BE_1} + V_{BE_2} = 6.16 \text{ V} + 0.7 \text{ V} + 0.7 \text{ V} = 7.56 \text{ V} \\
 V_{CE_2} &= V_{CC} - V_{E_2} = 18 \text{ V} - 6.16 \text{ V} = 11.84 \text{ V}
 \end{aligned}$$

**AC Input Impedance** The ac input impedance can be determined using the ac equivalent network of Fig. 5.77.



**FIG. 5.77**

Finding  $Z_i$ .

As defined in Fig. 5.77:

$$Z_{i_2} = \beta_2(r_{e_2} + R_E)$$

$$Z_{i_1} = \beta_1(r_{e_1} + Z_{i_2})$$

so that

$$Z_{i_1} = \beta_1(r_{e_1} + \beta_2(r_{e_2} + R_E))$$

$$R_E \gg r_{e_2}$$

Assuming

$$Z_{i_1} = \beta_1(r_{e_1} + \beta_2 R_E)$$

and

$$\beta_2 R_E \gg r_{e_1}$$

Since

$$Z_{i_1} \cong \beta_1 \beta_2 R_E$$

and since

$$Z_i = R_B \| Z_{i_1}$$

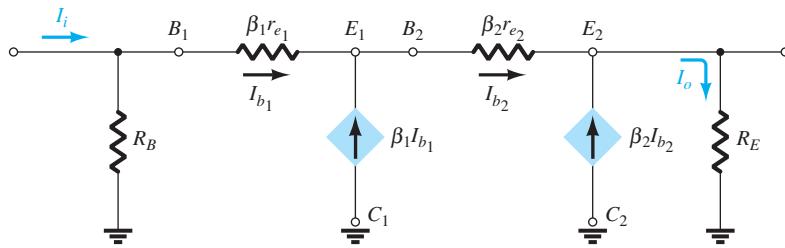
$$Z_i = R_B \| \beta_1 \beta_2 R_E = R_B \| \beta_D R_E \quad (5.108)$$

For the network of Fig. 5.76

$$\begin{aligned}
 Z_i &= R_B \| \beta_D R_E \\
 &= 3.3 \text{ M}\Omega \| (5000)(390 \text{ }\Omega) = 3.3 \text{ M}\Omega \| 1.95 \text{ M}\Omega \\
 &= 1.38 \text{ M}\Omega
 \end{aligned}$$

Note in the preceding analysis that the values of  $r_e$  were not compared but dropped compared to much larger quantities. In a Darlington configuration the values of  $r_e$  will be different because the emitter current through each transistor will be different. Also, keep in mind that chances are the beta values for each transistor will be different because they deal with different current levels. The fact remains, however, that the product of the two beta values will equal  $\beta_D$ , as indicated on the specification sheet.

**AC Current Gain** The current gain can be determined from the equivalent network of Fig. 5.78. The output impedance of each transistor is ignored and the parameters for each transistor are employed.



**FIG. 5.78**  
Determining  $A_i$  for the network of Fig. 5.75.

$$\text{Solving for the output current: } I_o = I_{b2} + \beta_2 I_{b2} = (\beta_2 + 1)I_{b2}$$

with

$$I_{b2} = \beta_1 I_{b1} + I_{b1} = (\beta_1 + 1)I_{b1}$$

Then

$$I_o = (\beta_2 + 1)(\beta_1 + 1)I_{b1}$$

Using the current-divider rule on the input circuit:

$$I_{b1} = \frac{R_B}{R_B + Z_i} I_i = \frac{R_B}{R_B + \beta_1 \beta_2 R_E} I_i$$

and

$$I_o = (\beta_2 + 1)(\beta_1 + 1) \left( \frac{R_B}{R_B + \beta_1 \beta_2 R_E} \right) I_i$$

so that

$$A_i = \frac{I_o}{I_i} = \frac{(\beta_1 + 1)(\beta_2 + 1)R_B}{R_B + \beta_1 \beta_2 R_E}$$

Using  $\beta_1, \beta_2 \gg 1$

$$A_i = \frac{I_o}{I_i} \cong \frac{\beta_1 \beta_2 R_B}{R_B + \beta_1 \beta_2 R_E} \quad (5.109)$$

or

$$A_i = \frac{I_o}{I_i} \cong \frac{\beta_D R_B}{R_B + \beta_D R_E} \quad (5.110)$$

For Fig. 5.76:

$$\begin{aligned} A_i &= \frac{I_o}{I_i} = \frac{\beta_D R_B}{R_B + \beta_D R_E} = \frac{(5000)(3.3 \text{ M}\Omega)}{3.3 \text{ M}\Omega + 1.95 \text{ M}\Omega} \\ &= 3.14 \times 10^3 \end{aligned}$$

**AC Voltage Gain** The voltage gain can be determined using Fig. 5.77 and the following derivation:

$$V_o = I_o R_E$$

$$V_i = I_i (R_B \parallel Z_i)$$

$$R_B \parallel Z_i = R_B \parallel \beta_D R_E = \frac{\beta_D R_B R_E}{R_B + \beta_D R_E}$$

and

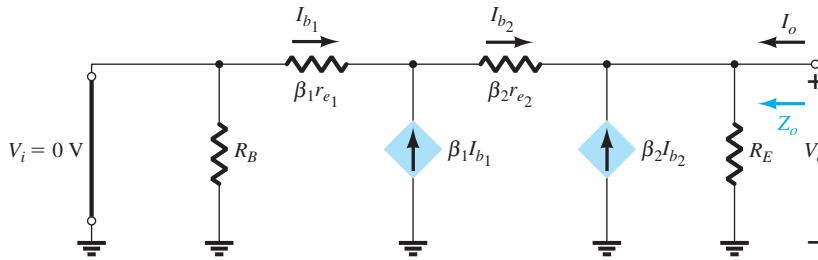
$$\begin{aligned} A_v &= \frac{V_o}{V_i} = \frac{I_o R_E}{I_i (R_B \parallel Z_i)} = (A_i) \left( \frac{R_E}{R_B \parallel Z_i} \right) \\ &= \left[ \frac{\beta_D R_B}{R_B + \beta_D R_E} \right] \left[ \frac{R_E}{\beta_D R_B R_E} \right] \end{aligned}$$

and

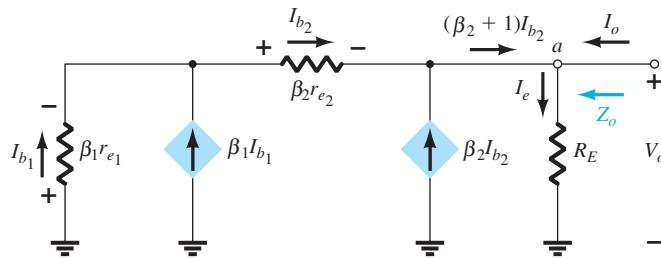
$$A_v \cong 1 \text{ (in reality less than one)} \quad (5.111)$$

an expected result for the emitter-follower configuration.

**AC Output Impedance** The output impedance will be determined by going back to Fig. 5.78 and setting  $V_i$  to zero volts as shown in Fig. 5.79. The resistor  $R_B$  is “shorted out,” resulting in the configuration of Fig. 5.80. Note in Figs. 5.82 and 5.83 that the output current has been redefined to match standard nomenclature and properly defined  $Z_o$ .



**FIG. 5.79**  
Determining  $Z_o$ .



**FIG. 5.80**  
Redrawn of network of Fig. 5.79.

At point  $a$  Kirchhoff's current law will result in  $I_o + (\beta_2 + 1)I_{b_2} = I_e$ :

$$I_o = I_e - (\beta_2 + 1)I_{b_2}$$

Applying Kirchhoff's voltage law around the entire outside loop will result in

$$-I_{b_1}\beta_1r_{e_1} - I_{b_2}\beta_2r_{e_2} - V_o = 0$$

$$\text{and } V_o = I_{b_1}\beta_1r_{e_1} + I_{b_2}\beta_2r_{e_2}$$

$$\text{Substituting } I_{b_2} = (\beta_1 + 1)I_{b_1}$$

$$\begin{aligned} V_o &= -I_{b_1}\beta_1r_{e_1} - (\beta_1 + 1)I_{b_1}\beta_2r_{e_2} \\ &= -I_{b_1}[\beta_1r_{e_1} + (\beta_1 + 1)\beta_2r_{e_2}] \end{aligned}$$

$$\text{and } I_{b_1} = -\frac{V_o}{\beta_1r_{e_1} + (\beta_1 + 1)\beta_2r_{e_2}}$$

$$\text{with } I_{b_2} = (\beta_1 + 1)I_{b_1} = (\beta_1 + 1)\left[-\frac{V_o}{\beta_1r_{e_1} + (\beta_1 + 1)\beta_2r_{e_2}}\right]$$

$$\text{so that } I_{b_2} = -\left[\frac{\beta_1 + 1}{\beta_1r_{e_1} + (\beta_1 + 1)\beta_2r_{e_2}}\right]V_o$$

$$\text{Going back } I_o = I_e - (\beta_2 + 1)I_{b_2} = I_e - (\beta_2 + 1)\left(-\frac{(\beta_1 + 1)V_o}{\beta_1r_{e_1} + (\beta_1 + 1)\beta_2r_{e_2}}\right)$$

$$\text{or } I_o = \frac{V_o}{R_E} + \frac{(\beta_1 + 1)(\beta_2 + 1)V_o}{\beta_1r_{e_1} + (\beta_1 + 1)\beta_2r_{e_2}}$$

Because  $\beta_1, \beta_2 \gg 1$

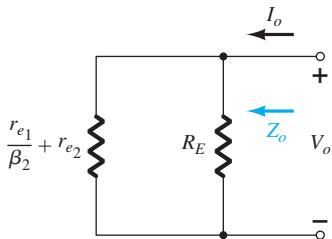
$$I_o = \frac{V_o}{R_E} + \frac{\beta_1\beta_2 V_o}{\beta_1 r_{e_1} + \beta_1\beta_2 r_{e_2}} = \frac{V_o}{R_E} + \frac{V_o}{\frac{\beta_1 r_{e_1}}{\beta_1\beta_2} + \frac{r_{e_2}}{\beta_1\beta_2}}$$

$$I_o = \frac{V_o}{R_E} + \frac{V_o}{\frac{r_{e_1}}{\beta_2} + r_{e_2}}$$

which defines the parallel resistance network of Fig. 5.81.

In general,  $R_E \gg \left(\frac{r_{e_1}}{\beta_2} + r_{e_2}\right)$  so the output impedance is defined by

$$Z_o = \frac{r_{e_1}}{\beta_2} + r_{e_2} \quad (5.112)$$



**FIG. 5.81**

Resulting network defined by  $Z_o$ .

Using the dc results, the value of  $r_{e_2}$  and  $r_{e_1}$  can be determined as follows.

$$r_{e_2} = \frac{26 \text{ mV}}{I_{E_2}} = \frac{26 \text{ mV}}{15.80 \text{ mA}} = 1.65 \Omega$$

and

$$I_{E_1} = I_{B_2} = \frac{I_{E_2}}{\beta_2} = \frac{15.80 \text{ mA}}{100} = 0.158 \text{ mA}$$

so that

$$r_{e_1} = \frac{26 \text{ mV}}{0.158 \text{ mA}} = 164.5 \Omega$$

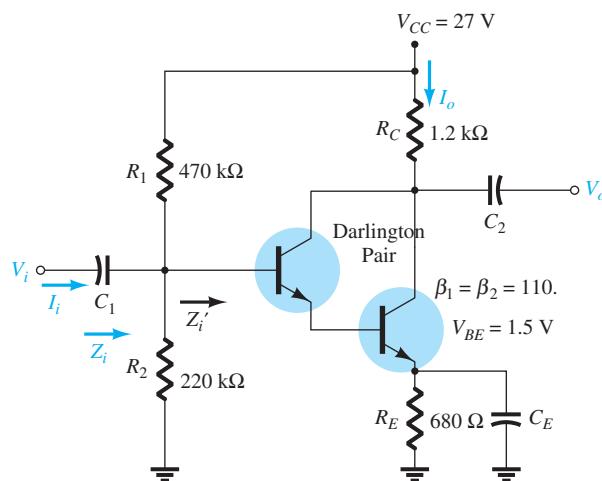
The output impedance for the network of Fig. 5.78 is therefore:

$$Z_o \cong \frac{r_{e_1}}{\beta_2} + r_{e_2} = \frac{164.5 \Omega}{100} + 1.65 \Omega = 1.645 \Omega + 1.65 \Omega = 3.30 \Omega$$

In general, the output impedance for the configuration of Fig. 5.78 is very low—in the order of a few ohms at most.

## Voltage-Divider Amplifier

**DC Bias** Let us now investigate the effect of the Darlington configuration in a basic amplifier configuration as shown in Fig. 5.82. Note that now there is a collector resistor  $R_C$ , and the emitter terminal of the Darlington circuit is connected to ground for ac conditions. As noted on Fig. 5.82, the beta of each transistor is provided along with the resulting voltage from base to emitter.



**FIG. 5.82**  
Amplifier configuration using a Darlington pair.

The dc analysis can proceed as follows:

$$\beta_D = \beta_1\beta_2 = (110 \times 110) = 12,100$$

$$V_B = \frac{R_2}{R_2 + R_1} V_{CC} = \frac{220 \text{ k}\Omega (27 \text{ V})}{220 \text{ k}\Omega + 470 \text{ k}\Omega} = 8.61 \text{ V}$$

$$V_E = V_B - V_{BE} = 8.61 \text{ V} - 1.5 \text{ V} = 7.11 \text{ V}$$

$$I_E = \frac{V_E}{R_E} = \frac{7.11 \text{ V}}{680 \text{ }\Omega} = 10.46 \text{ mA}$$

$$I_B = \frac{I_E}{\beta_D} = \frac{10.46 \text{ mA}}{12,100} = 0.864 \mu\text{A}$$

Using the preceding results the values of  $r_{e_2}$  and  $r_{e_1}$  can be determined:

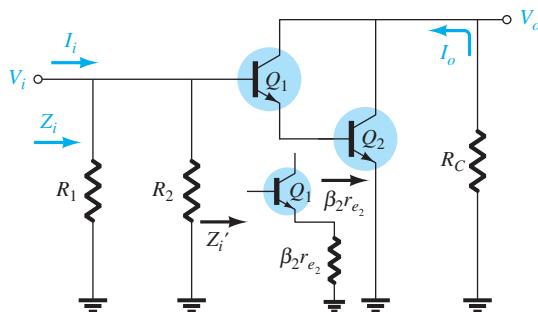
$$r_{e_2} = \frac{26 \text{ mV}}{I_{E_2}} = \frac{26 \text{ mV}}{10.46 \text{ mA}} = 2.49 \text{ }\Omega$$

$$I_{E_1} = I_{B_2} = \frac{I_{E_2}}{\beta_2} = \frac{10.46 \text{ mA}}{110} = 0.095 \text{ mA}$$

and  $r_{e_1} = \frac{26 \text{ mV}}{I_{E_1}} = \frac{26 \text{ mV}}{0.095 \text{ mA}} = 273.7 \text{ }\Omega$

**AC Input Impedance** The ac equivalent of Fig. 5.82 appears as Fig. 5.83. The resistors  $R_1$  and  $R_2$  are in parallel with the input impedance to the Darlington pair, assuming the second transistor found by assuming the second transistor acts like an  $R_E$  load on the first as shown in Fig. 5.83.

That is,  $Z'_i = \beta_1 r_{e_1} + \beta_1 (\beta_2 r_{e_2})$



**FIG. 5.83**  
Defining  $Z'_i$  and  $Z_i$ .

and

$$Z'_i = \beta_1 [r_{e_1} + \beta_2 r_{e_2}] \quad (5.113)$$

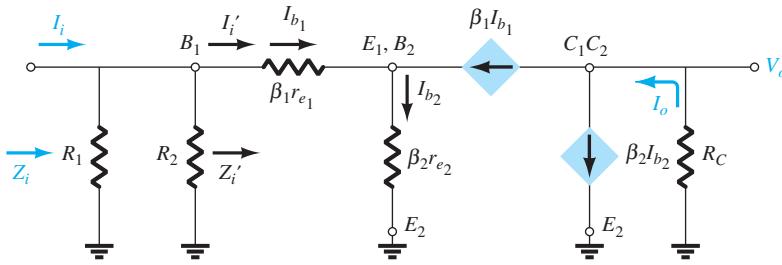
For the network of Fig. 5.82:

$$\begin{aligned} Z'_i &= 110[273.7 \text{ }\Omega + (110)(2.49 \text{ }\Omega)] \\ &= 110[273.7 \text{ }\Omega + 273.9 \text{ }\Omega] \\ &= 110[547.6 \text{ }\Omega] \\ &= 60.24 \text{ k}\Omega \end{aligned}$$

and

$$\begin{aligned} Z_i &= R_1 \parallel R_2 \parallel Z'_i \\ &= 470 \text{ k}\Omega \parallel 220 \text{ k}\Omega \parallel 60.24 \text{ k}\Omega \\ &= 149.86 \text{ k}\Omega \parallel 60.24 \text{ k}\Omega \\ &= 42.97 \text{ k}\Omega \end{aligned}$$

**AC Current Gain** The complete ac equivalent of Fig. 5.82 appears as Fig. 5.84.



**FIG. 5.84**  
ac equivalent network for Fig. 5.82.

The output current

$$I_o = \beta_1 I_{b_1} + \beta_2 I_{b_2}$$

with

$$I_{b_2} = (\beta_1 + 1) I_{b_1}$$

so that

$$I_o = \beta_1 I_{b_1} + \beta_2 (\beta_1 + 1) I_{b_1}$$

and with

$$I_{b_1} = I'_i$$

we find

$$I_o = \beta_1 I'_i + \beta_2 (\beta_1 + 1) I'_i$$

and

$$A'_i = \frac{I_o}{I'_i} = \beta_1 + \beta_2 (\beta_1 + 1)$$

$$\cong \beta_1 + \beta_2 \beta_1 = \beta_1 (1 + \beta_2)$$

$$\cong \beta_1 \beta_2$$

and finally

$$A'_i = \frac{I_o}{I'_i} = \beta_1 \beta_2 = \beta_D \quad (5.114)$$

For the original structure:  $I'_i = \frac{R_1 \| R_2 I_i}{R_1 \| R_2 + Z'_i}$  or  $\frac{I'_i}{I_i} = \frac{R_1 \| R_2}{R_1 \| R_2 + Z'_i}$

$$\text{but } A_i = \frac{I_o}{I_i} = \left( \frac{I_o}{I'_i} \right) \left( \frac{I'_i}{I_i} \right)$$

so that

$$A_i = \frac{\beta_D (R_1 \| R_2)}{R_1 \| R_2 + Z'_i} \quad (5.115)$$

For Fig. 5.82

$$A_i = \frac{(12,100)(149.86 \text{ k}\Omega)}{149.86 \text{ k}\Omega + 60.24 \text{ k}\Omega} \\ = 8630.7$$

Note the significant drop in current gain due to  $R_1$  and  $R_2$ .

**AC Voltage Gain** The input voltage is the same across  $R_1$  and  $R_2$  and at the base of the first transistor as shown in Fig. 5.84.

The result is

$$A_v = \frac{V_o}{V_i} = -\frac{I_o R_C}{I'_i Z'_i} = -A_i \left( \frac{R_C}{Z'_i} \right)$$

and

$$A_v = -\frac{\beta_D R_C}{Z'_i} \quad (5.116)$$

For the network of Fig. 5.82,

$$A_v = -\frac{\beta_D R_C}{Z'_i} = -\frac{(12,000)(1.2 \text{ k}\Omega)}{60.24 \text{ k}\Omega} = -241.04$$

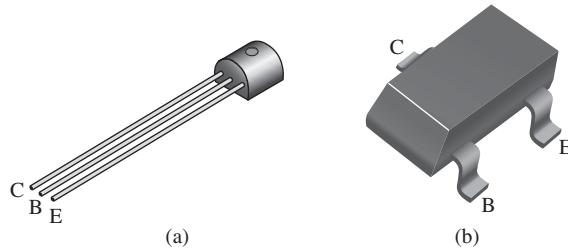
**AC Output Impedance** Because the output impedance in  $R_C$  is parallel with the collector to emitter terminals of the transistor, we can look back on similar situations and find that the output impedance is defined by

$$Z_o \equiv R_C \| r_{o_2} \quad (5.117)$$

where  $r_{o_2}$  is the output resistance of the transistor  $Q_2$ .

### Packaged Darlington Amplifier

Because the Darlington connection is so popular, a number of manufacturers provide packaged units such as shown in Fig. 5.85. Typically, the two BJTs are constructed on a single chip rather than separate BJT units. Note that only one set of collector, base, and emitter terminals is provided for each configuration. These, of course, are the base of the transistor  $Q_1$ , the collector of  $Q_1$  and  $Q_2$ , and the emitter of  $Q_2$ .



**FIG. 5.85**  
Packaged Darlington amplifiers: (a) TO-92 package;  
(b) Super SOT™-3 package.

In Fig. 5.86 some of the ratings for an MPSA28 Fairchild Semiconductor Darlington amplifier are provided. In particular, note that the maximum collector-to-emitter voltage of 80 V is also the breakdown voltage. The same is true for the collector-to-base and emitter-to-base voltages, although notice how much lower the maximum ratings are for the base-to-emitter junction. Because of the Darlington configuration, the maximum current rating for the collector current has jumped to 800 mA—far exceeding levels we have encountered

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#### Absolute Maximum Ratings

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$V_{CES}$	Collector-Emitter Voltage	80 V
$V_{CBO}$	Collector-Base Voltage	80 V
$V_{EBO}$	Emitter-Base Voltage	12 V
$I_C$	Collector Current-Continuous	800 mA

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#### Electrical Characteristics

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$V_{(BR)CES}$	Collector-Emitter Breakdown Voltage	80 V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	80 V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	12 V
$I_{CBO}$	Collector Cutoff Current	100 mA
$I_{EBO}$	Emitter Cutoff Current	100 mA

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#### On Characteristics

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$h_{FE}$	DC Current Gain	10,000
$V_{CE(\text{sat})}$	Collector-Emitter Saturation Voltage	1.2 V
$V_{BE(\text{on})}$	Base-Emitter on Voltage	2.0 V

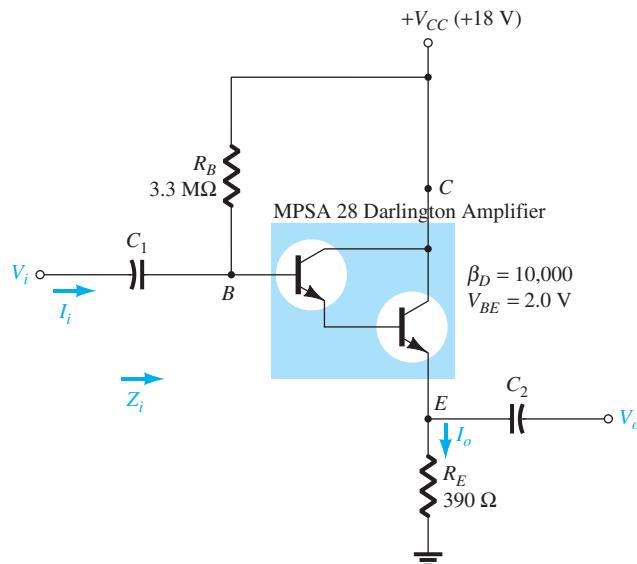
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**FIG. 5.86**

MPSA 28 Fairchild Semiconductor Darlington amplifier ratings.

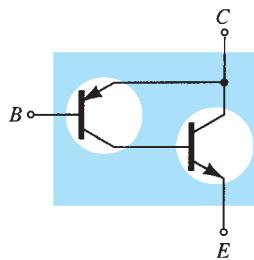
for single-transistor networks. The dc current gain is rated at the high level of 10,000 and the base-to-emitter potential in the “on” state is 2 V, which certainly exceeds the 1.4 V we have used for individual transistors. Finally, it is interesting to note that the level of  $I_{CEO}$  is much higher at 500 nA than for a typical single-transistor unit.

In the packaged format the network of Fig. 5.75 would appear as shown in Fig. 5.87. Using  $\beta_D$  and the provided value of  $V_{BE} (=V_{BE_1} + V_{BE_2})$ , all the equations appearing in this section can be applied.



**FIG. 5.87**  
Darlington emitter-follower circuit.

### 5.18 FEEDBACK PAIR



**FIG. 5.88**

Feedback pair connection.

The feedback pair connection (see Fig. 5.88) is a two-transistor circuit that operates like the Darlington circuit. Notice that the feedback pair uses a *pnp* transistor driving an *npn* transistor, the two devices acting effectively much like one *pnp* transistor. As with a Darlington connection, the feedback pair provides very high current gain (the product of the transistor current gains), high input impedance, low output impedance, and a voltage gain slightly less than one. Initially, it may appear that it would have a high voltage gain because the output is taken off the collector with a resistor  $R_C$  in place. However, the *pnp-npn* combination results in terminal characteristics very similar to that of the emitter-follower configuration. A typical application (see Chapter 12) uses a Darlington and a feedback-pair connection to provide complementary transistor operation. A practical network employing a feedback pair is provided in Fig. 5.89 for investigation.

### DC Bias

The dc bias calculations that follow use practical simplifications wherever possible to provide simpler results. From the  $Q_1$  base-emitter loop, one obtains

$$\begin{aligned} V_{CC} - I_C R_C - V_{EB_1} - I_{B_1} R_B &= 0 \\ V_{CC} - (\beta_1 \beta_2 I_{B_1}) R_C - V_{EB_1} - I_{B_1} R_B &= 0 \end{aligned}$$

The base current is then

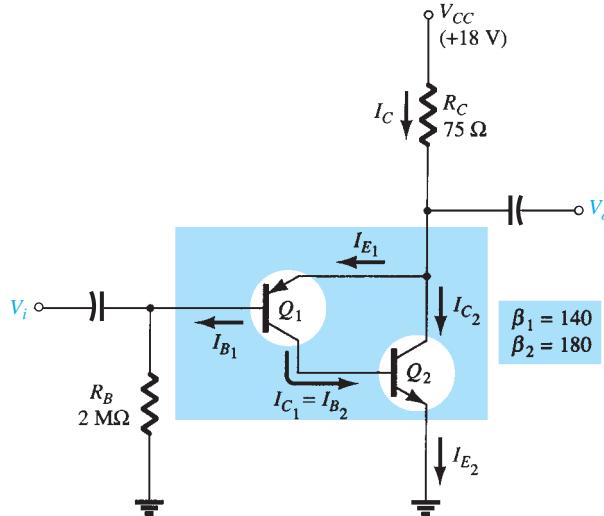
$$I_{B_1} = \frac{V_{CC} - V_{BE_1}}{R_B + \beta_1 \beta_2 R_C} \quad (5.118)$$

The collector current of  $Q_1$  is

$$I_{C_1} = \beta_1 I_{B_1} = I_{B_2}$$

which is also the base  $Q_2$  current. The transistor  $Q_2$  collector current is

$$I_{C_2} = \beta_2 I_{B_2} \approx I_{E_2}$$



**FIG. 5.89**  
Operation of a feedback pair.

so that the current through  $R_C$  is

$$I_C = I_{E_1} + I_{C_2} \approx I_{B_2} + I_{C_2} \quad (5.119)$$

The voltages

$$V_{C_2} = V_{E_1} = V_{CC} - I_C R_C \quad (5.120)$$

and

$$V_{B_1} = I_{B_1} R_B \quad (5.121)$$

with

$$V_{BC_1} = V_{B_1} - V_{BE_2} = V_{B_1} - 0.7 \text{ V} \quad (5.122)$$

**EXAMPLE 5.18** Calculate the dc bias currents and voltages for the circuit of Fig. 5.89 to provide  $V_o$  at one-half the supply voltage (9 V).

**Solution:**

$$I_{B_1} = \frac{18 \text{ V} - 0.7 \text{ V}}{2 \text{ M}\Omega + (140)(180)(75 \Omega)} = \frac{17.3 \text{ V}}{3.89 \times 10^6} = 4.45 \mu\text{A}$$

The base  $Q_2$  current is then

$$I_{B_2} = I_{C_1} = \beta_1 I_{B_1} = 140(4.45 \mu\text{A}) = 0.623 \text{ mA}$$

resulting in a  $Q_2$  collector current of

$$I_{C_2} = \beta_2 I_{B_2} = 180(0.623 \text{ mA}) = 112.1 \text{ mA}$$

and the current through  $R_C$  is then

$$\text{Eq. (5.119): } I_C = I_{E_1} + I_{C_2} = 0.623 \text{ mA} + 112.1 \text{ mA} \approx I_{C_2} = 112.1 \text{ mA}$$

$$\begin{aligned} V_{C_2} &= V_{E_1} = 18 \text{ V} - (112.1 \text{ mA})(75 \Omega) \\ &= 18 \text{ V} - 8.41 \text{ V} \\ &= 9.59 \text{ V} \end{aligned}$$

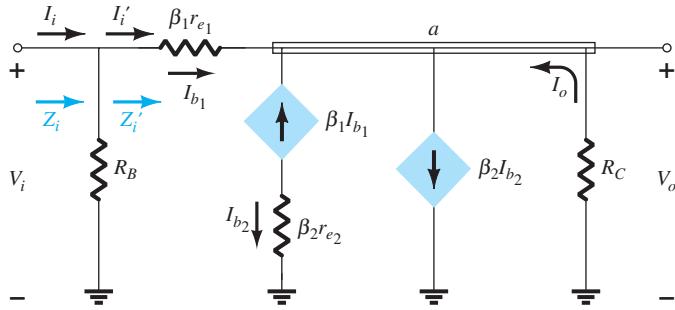
$$V_{B_1} = I_{B_1} R_B = (4.45 \mu\text{A})(2 \text{ M}\Omega)$$

$$= 8.9 \text{ V}$$

$$\begin{aligned} V_{BC_1} &= V_{B_1} - 0.7 \text{ V} = 8.9 \text{ V} - 0.7 \text{ V} \\ &= 8.2 \text{ V} \end{aligned}$$

## AC Operation

The ac equivalent circuit for that of Fig. 5.89 is drawn in Fig. 5.90.



**FIG. 5.90**  
ac equivalent for the network of Fig. 5.89.

**Input Impedance,  $Z'_i$**  The ac input impedance seen looking into the base of transistor  $Q_1$  is determined as follows:

$$Z'_i = \frac{V_i}{I'_i}$$

Applying Kirchhoff's current law at node  $a$  and defining  $I_c = I_o$ :

$$I_{b1} + \beta_1 I_{b1} - \beta_2 I_{b2} + I_o = 0$$

with  $I_{b2} = -\beta_1 I_{b1}$  as noted in Fig. 5.90.

The result is

$$I_{b1} + \beta_1 I_{b1} - \beta_2(-\beta_1 I_{b1}) + I_o = 0$$

and

$$I_o = -I_{b1} - \beta_1 I_{b1} - \beta_1 \beta_2 I_{b1}$$

or

$$I_o = -I_{b1}(1 + \beta_1) - \beta_1 \beta_2 I_{b1}$$

but

$$\beta_1 \gg 1$$

and

$$\begin{aligned} I_o &= -\beta_1 I_{b1} - \beta_1 \beta_2 I_{b1} = -I_{b1}(\beta_1 + \beta_1 \beta_2) \\ &= -I_{b1} \beta_1(1 + \beta_2) \end{aligned}$$

resulting in:

$$I_o \cong -\beta_1 \beta_2 I_{b1} \quad (5.123)$$

Now,  $I_{b1} = \frac{V_i - V_o}{\beta_1 r_{e1}}$  from Fig. 5.90

and

$$V_o = -I_o R_C = -(-\beta_1 \beta_2 I_{b1}) R_C = \beta_1 \beta_2 I_{b1} R_C$$

so

$$I_{b1} = \frac{V_i - \beta_1 \beta_2 I_{b1} R_C}{\beta_1 r_{e1}}$$

Rearranging:

$$I_{b1} \beta_1 r_{e1} = V_i - \beta_1 \beta_2 I_{b1} R_C$$

and

$$I_{b1} (\beta_1 r_{e1} + \beta_1 \beta_2 R_C) = V_i$$

so

$$I_{b1} = I'_i = \frac{V_i}{\beta_1 r_{e1} + \beta_1 \beta_2 R_C}$$

and

$$V'_i = \frac{V_i}{I'_i} = \frac{V_i}{\frac{V_i}{\beta_1 r_{e1} + \beta_1 \beta_2 R_C}} = \frac{V_i}{\beta_1 r_{e1} + \beta_1 \beta_2 R_C}$$

so that

$$Z'_i = \beta_1 r_{e1} + \beta_1 \beta_2 R_C \quad (5.124)$$

In general,

$$\beta_1 \beta_2 R_C \gg \beta_1 r_{e1}$$

and

$$Z'_i \cong \beta_1 \beta_2 R_C \quad (5.125)$$

with

$$Z_i = R_B \| Z'_i$$

(5.126)

For the network of Fig. 5.89:  $r_{e_1} = \frac{26 \text{ mV}}{I_{E_1}} = \frac{26 \text{ mV}}{0.623 \text{ mA}} = 41.73 \Omega$

and

$$\begin{aligned} Z'_i &= \beta_1 r_{e_1} + \beta_1 \beta_2 R_C \\ &= (140)(41.73 \Omega) + (140)(180)(75 \Omega) \\ &= 5842.2 \Omega + 1.89 \text{ M}\Omega \\ &= \mathbf{1.895 \text{ M}\Omega} \end{aligned}$$

where Eq. (5.125) results in  $Z'_i \cong \beta_1 \beta_2 R_C = (140)(180)(75 \Omega) = \mathbf{1.89 \text{ M}\Omega}$ , validating the above approximations.

## Current Gain

Defining  $I_{b_1} = I'_i$  as shown in Fig. 5.90 will permit finding the current gain  $A'_i = I_o/I'_i$ .

Looking back on the derivation of  $Z_i$  we found  $I_o = -\beta_1 \beta_2 I_{b_1} = -\beta_1 \beta_2 I'_i$

resulting in

$$A'_i = \frac{I_o}{I'_i} = -\beta_1 \beta_2 \quad (5.127)$$

The current gain  $A_i = I_o/I_i$  can be determined using the fact that

$$A_i = \frac{I_o}{I_i} = \frac{I_o}{I'_i} \cdot \frac{I'_i}{I_i}$$

$$\text{For the input side: } I'_i = \frac{R_B I_i}{R_B + Z'_i} = \frac{R_B I_i}{R_B + \beta_1 \beta_2 R_C}$$

$$\text{Substituting: } A_i = \frac{I_o}{I'_i} \cdot \frac{I'_i}{I_i} = (-\beta_1 \beta_2) \left( \frac{R_B}{R_B + \beta_1 \beta_2 R_C} \right)$$

So that

$$A_i = \frac{I_o}{I_i} = \frac{-\beta_1 \beta_2 R_B}{R_B + \beta_1 \beta_2 R_C} \quad (5.128)$$

The negative sign appears because both  $I_i$  and  $I_o$  are defined as entering the network.

$$\begin{aligned} \text{For the network of Fig. 5.89: } A'_i &= \frac{I_o}{I'_i} = -\beta_1 \beta_2 \\ &= -(140)(180) \\ &= \mathbf{-25.2 \times 10^3} \\ A_i &= \frac{-\beta_1 \beta_2 R_B}{R_B + \beta_1 \beta_2 R_C} = -\frac{(140)(180)(2 \text{ M}\Omega)}{2 \text{ M}\Omega + 1.89 \text{ M}\Omega} \\ &= -\frac{50,400 \text{ M}\Omega}{3.89 \text{ M}\Omega} \\ &= \mathbf{-12.96 \times 10^3} (\cong \text{half of } A'_i) \end{aligned}$$

## Voltage Gain

The voltage gain can quickly be determined using the results obtained above.

That is,

$$A_v = \frac{V_o}{V_i} = \frac{-I_o R_C}{I'_i Z'_i}$$

$$= -\frac{(-\beta_1 \beta_2 I'_i) R_C}{I'_i (\beta_1 r_{e_1} + \beta_1 \beta_2 R_C)}$$

$$A_v = \frac{\beta_2 R_C}{r_{e_1} + \beta_2 R_C} \quad (5.129)$$

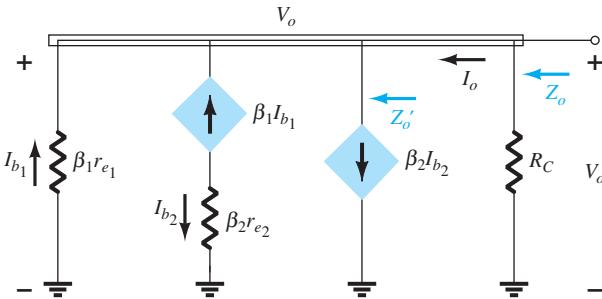
which is simply the following if we apply the approximation:  $\beta_2 R_C \gg r_{e_1}$

$$A_v \cong \frac{\beta_2 R_C}{\beta_2 R_C} = 1$$

$$\begin{aligned} \text{For the network of Fig. 5.89: } A_v &= \frac{\beta_2 R_C}{r_{e_1} + \beta_2 R_C} = \frac{(180)(75 \Omega)}{41.73 \Omega + (180)(75 \Omega)} \\ &= \frac{13.5 \times 10^3 \Omega}{41.73 \Omega + 13.5 \times 10^3 \Omega} \\ &= \mathbf{0.997} \cong 1 \text{ (as indicated above)} \end{aligned}$$

### Output Impedance

The output impedance  $Z'_o$  is defined in Fig. 5.91 when  $V_i$  is set to zero volts.



**FIG. 5.91**  
Determining  $Z'_o$  and  $Z_o$ .

Using the fact that  $I_o = -\beta_1 \beta_2 I_{b_1}$  from calculations above, we find that

$$Z'_o = \frac{V_o}{I_o} = \frac{V_o}{-\beta_1 \beta_2 I_{b_1}}$$

but

$$I_{b_1} = -\frac{V_o}{\beta_1 r_{e_1}}$$

and

$$Z'_o = \frac{V_o}{-\beta_1 \beta_2 \left( -\frac{V_o}{\beta_1 r_{e_1}} \right)} = \frac{\beta_1 r_{e_1}}{\beta_1 \beta_2}$$

so that

$$Z'_o = \frac{r_{e_1}}{\beta_2} \quad (5.130)$$

with

$$Z_o = R_C \parallel \frac{r_{e_1}}{\beta_2} \quad (5.131)$$

However,

$$R_C \gg \frac{r_{e_1}}{\beta_2}$$

leaving

$$Z_o \cong \frac{r_{e_1}}{\beta_2} \quad (5.132)$$

which will be a very low value.

For the network of Fig. 5.89:

$$Z_o \cong \frac{41.73 \Omega}{180} = \mathbf{0.23 \Omega}$$

The preceding analysis shows that the feedback pair connection of Fig. 5.89 provides operation with voltage gain very near 1 (just as with a Darlington emitter-follower), a very high current gain, a very low output impedance, and a high input impedance.

The hybrid equivalent model was mentioned in the earlier sections of this chapter as one that was used in the early years before the popularity of the  $r_e$  model developed. Today there is a mix of usage depending on the level and direction of the investigation.

*The  $r_e$  model has the advantage that the parameters are defined by the actual operating conditions,*

whereas

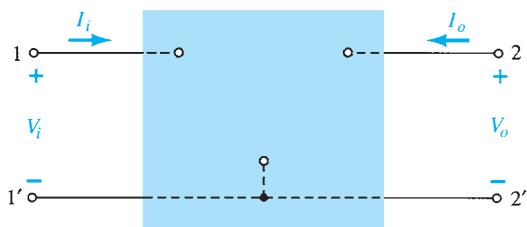
*the parameters of the hybrid equivalent circuit are defined in general terms for any operating conditions.*

In other words, the hybrid parameters may not reflect the actual operating conditions but simply provide an indication of the level of each parameter to expect for general use. The  $r_e$  model suffers from the fact that parameters such as the output impedance and the feedback elements are not available, whereas the hybrid parameters provide the entire set on the specification sheet. In most cases, if the  $r_e$  model is employed, the investigator will simply examine the specification sheet to have some idea of what the additional elements might be. This section will show how one can go from one model to the other and how the parameters are related. Because all specification sheets provide the hybrid parameters and the model is still extensively used, it is important to be aware of both models. The hybrid parameters as shown in Fig. 5.92 are derived from the specification sheet for the 2N4400 transistor described in Chapter 3. The values are provided at a dc collector current of 1 mA and a collector-to-emitter voltage of 10 V. In addition, a range of values is provided for each parameter for guidance in the initial design or analysis of a system. One obvious advantage of the specification sheet listing is the immediate knowledge of typical levels for the parameters of the device as compared to other transistors.

		Min.	Max.	
Input impedance ( $I_C = 1 \text{ mA dc}, V_{CE} = 10 \text{ V dc}, f = 1 \text{ kHz}$ )	$h_{ie}$	0.5	7.5	$\text{k}\Omega$
Voltage feedback ratio ( $I_C = 1 \text{ mA dc}, V_{CE} = 10 \text{ V dc}, f = 1 \text{ kHz}$ )	$h_{re}$	0.1	8.0	$\times 10^{-4}$
Small-signal current gain ( $I_C = 1 \text{ mA dc}, V_{CE} = 10 \text{ V dc}, f = 1 \text{ kHz}$ )	$h_{fe}$	20	250	—
Output admittance ( $I_C = 1 \text{ mA dc}, V_{CE} = 10 \text{ V dc}, f = 1 \text{ kHz}$ )	$h_{oe}$	1.0	30	$1 \mu\text{S}$

**FIG. 5.92**  
Hybrid parameters for the 2N4400 transistor.

The description of the hybrid equivalent model will begin with the general two-port system of Fig. 5.93. The following set of equations (5.131) and (5.132) is only one of a number of ways in which the four variables of Fig. 5.93 can be related. It is the most frequently employed in transistor circuit analysis, however, and therefore is discussed in detail in this chapter.



**FIG. 5.93**  
Two-port system.

$$V_i = h_{11}I_i + h_{12}V_o \quad (5.133)$$

$$I_o = h_{21}I_i + h_{22}V_o \quad (5.134)$$

The parameters relating the four variables are called *h-parameters*, from the word “hybrid.” The term *hybrid* was chosen because the mixture of variables ( $V$  and  $I$ ) in each equation results in a “hybrid” set of units of measurement for the *h*-parameters. A clearer understanding of what the various *h*-parameters represent and how we can determine their magnitude can be developed by isolating each and examining the resulting relationship.

**$h_{11}$**  If we arbitrarily set  $V_o = 0$  (short circuit the output terminals) and solve for  $h_{11}$  in Eq. (5.133), we find

$$h_{11} = \left. \frac{V_i}{I_i} \right|_{V_o=0} \quad \text{ohms} \quad (5.135)$$

The ratio indicates that the parameter  $h_{11}$  is an impedance parameter with the units of ohms. Because it is the ratio of the *input* voltage to the *input* current with the output terminals *shorted*, it is called the *short-circuit input-impedance parameter*. The subscript 11 of  $h_{11}$  refers to the fact that the parameter is determined by a ratio of quantities measured at the input terminals.

**$h_{12}$**  If  $I_i$  is set equal to zero by opening the input leads, the following results for  $h_{12}$ :

$$h_{12} = \left. \frac{V_i}{V_o} \right|_{I_i=0} \quad \text{unitless} \quad (5.136)$$

The parameter  $h_{12}$ , therefore, is the ratio of the input voltage to the output voltage with the input current equal to zero. It has no units because it is a ratio of voltage levels and is called the *open-circuit reverse transfer voltage ratio parameter*. The subscript 12 of  $h_{12}$  indicates that the parameter is a transfer quantity determined by a ratio of input (1) to output (2) measurements. The first integer of the subscript defines the measured quantity to appear in the numerator; the second integer defines the source of the quantity to appear in the denominator. The term *reverse* is included because the ratio is an input voltage over an output voltage rather than the reverse ratio typically of interest.

**$h_{21}$**  If in Eq. (5.134)  $V_o$  is set equal to zero by again shorting the output terminals, the following results for  $h_{21}$ :

$$h_{21} = \left. \frac{I_o}{I_i} \right|_{V_o=0} \quad \text{unitless} \quad (5.137)$$

Note that we now have the ratio of an output quantity to an input quantity. The term *forward* will now be used rather than *reverse* as indicated for  $h_{12}$ . The parameter  $h_{21}$  is the ratio of the output current to the input current with the output terminals shorted. This parameter, like  $h_{12}$ , has no units because it is the ratio of current levels. It is formally called the *short-circuit forward transfer current ratio parameter*. The subscript 21 again indicates that it is a transfer parameter with the output quantity (2) in the numerator and the input quantity (1) in the denominator.

**$h_{22}$**  The last parameter,  $h_{22}$ , can be found by again opening the input leads to set  $I_i = 0$  and solving for  $h_{22}$  in Eq. (5.134):

$$h_{22} = \left. \frac{I_o}{V_o} \right|_{I_i=0} \quad \text{siemens} \quad (5.138)$$

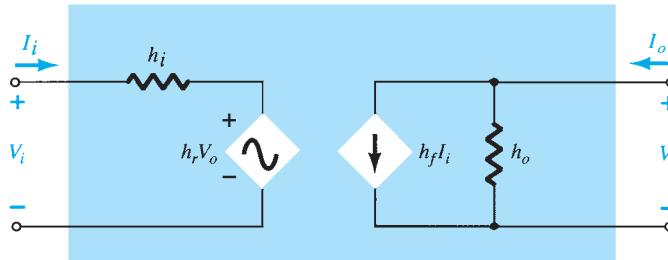
Because it is the ratio of the output current to the output voltage, it is the output conductance parameter, and it is measured in siemens (S). It is called the *open-circuit output admittance parameter*. The subscript 22 indicates that it is determined by a ratio of output quantities.

Because each term of Eq. (5.133) has the unit volt, let us apply Kirchhoff's voltage law "in reverse" to find a circuit that "fits" the equation. Performing this operation results in the circuit of Fig. 5.94. Because the parameter  $h_{11}$  has the unit ohm, it is represented by a resistor in Fig. 5.94. The quantity  $h_{12}$  is dimensionless and therefore simply appears as a multiplying factor of the "feedback" term in the input circuit.

Because each term of Eq. (5.134) has the units of current, let us now apply Kirchhoff's current law "in reverse" to obtain the circuit of Fig. 5.95. Because  $h_{22}$  has the units of admittance, which for the transistor model is conductance, it is represented by the resistor symbol. Keep in mind, however, that the resistance in ohms of this resistor is equal to the reciprocal of conductance ( $1/h_{22}$ ).

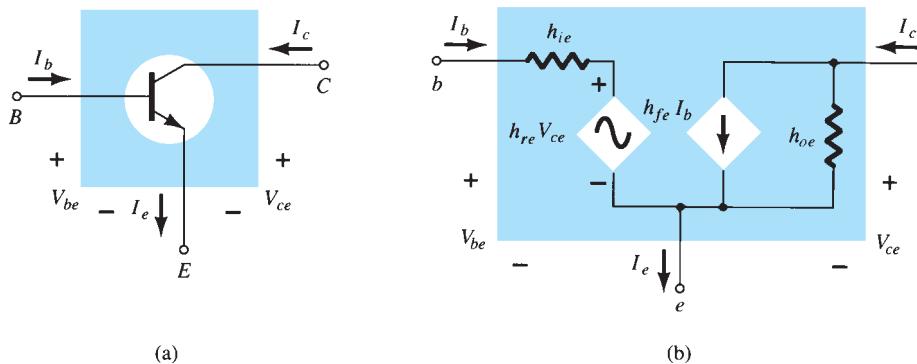
The complete "ac" equivalent circuit for the basic three-terminal linear device is indicated in Fig. 5.96 with a new set of subscripts for the  $h$ -parameters. The notation of Fig. 5.96 is of a more practical nature because it relates the  $h$ -parameters to the resulting ratio obtained in the last few paragraphs. The choice of letters is obvious from the following listing:

- $h_{11} \rightarrow$  input resistance  $\rightarrow h_i$
- $h_{12} \rightarrow$  reverse transfer voltage ratio  $\rightarrow h_r$
- $h_{21} \rightarrow$  forward transfer current ratio  $\rightarrow h_f$
- $h_{22} \rightarrow$  output conductance  $\rightarrow h_o$

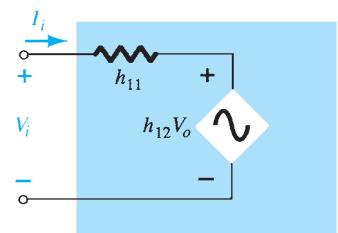


**FIG. 5.96**  
Complete hybrid equivalent circuit.

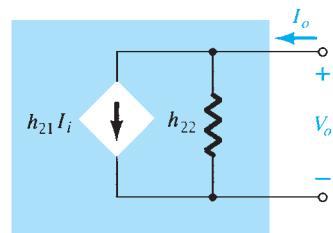
The circuit of Fig. 5.96 is applicable to any linear three-terminal electronic device or system with no internal independent sources. For the transistor, therefore, even though it has three basic configurations, *they are all three-terminal configurations*, so that the resulting equivalent circuit will have the same format as shown in Fig. 5.96. In each case, the bottom of the input and output sections of the network of Fig. 5.96 can be connected as shown in Fig. 5.97 because the potential level is the same. Essentially, therefore, the transistor model is a three-terminal two-port system. The  $h$ -parameters, however, will change with each configuration. To distinguish which parameter has been used or which is available, a second



**FIG. 5.97**  
Common-emitter configuration: (a) graphical symbol; (b) hybrid equivalent circuit.

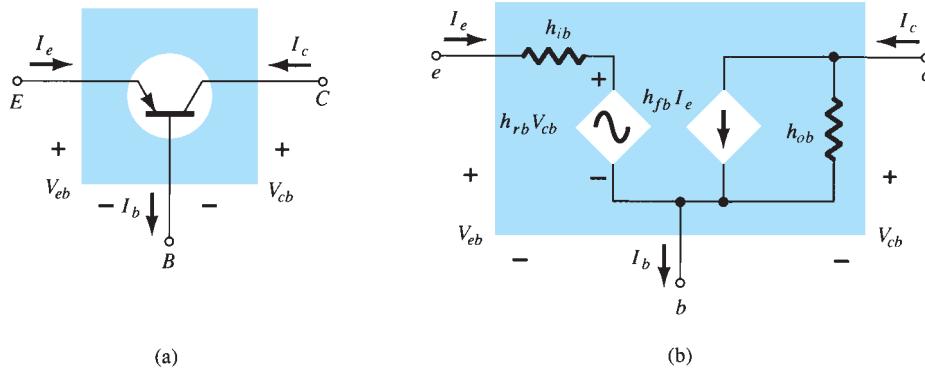


**FIG. 5.94**  
Hybrid input equivalent circuit.



**FIG. 5.95**  
Hybrid output equivalent circuit.

subscript has been added to the  $h$ -parameter notation. For the common-base configuration, the lowercase letter  $b$  was added, whereas for the common-emitter and common-collector configurations, the letters  $e$  and  $c$  were added, respectively. The hybrid equivalent network for the common-emitter configuration appears with the standard notation in Fig. 5.97. Note that  $I_i = I_b$ ,  $I_o = I_c$ , and, through an application of Kirchhoff's current law,  $I_e = I_b + I_c$ . The input voltage is now  $V_{be}$ , with the output voltage  $V_{ce}$ . For the common-base configuration of Fig. 5.98,  $I_i = I_e$ ,  $I_o = I_c$  with  $V_{eb} = V_i$  and  $V_{cb} = V_o$ . The networks of Figs. 5.97 and 5.98 are applicable for *pnp* or *npn* transistors.



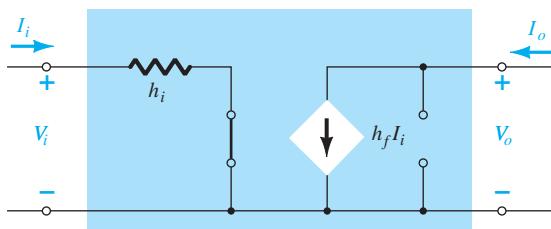
**FIG. 5.98**  
Common-base configuration: (a) graphical symbol; (b) hybrid equivalent circuit.

The fact that both a Thévenin and a Norton circuit appear in the circuit of Fig. 5.96 was further impetus for calling the resultant circuit a *hybrid* equivalent circuit. Two additional transistor equivalent circuits, not to be discussed in this text, called the *z*-parameter and *y*-parameter equivalent circuits, use either the voltage source or the current source, but not both, in the same equivalent circuit. In Appendix A the magnitudes of the various parameters will be found from the transistor characteristics in the region of operation resulting in the desired *small-signal equivalent network* for the transistor.

For the common-emitter and common-base configurations, the magnitude of  $h_r$  and  $h_o$  is often such that the results obtained for the important parameters such as  $Z_i$ ,  $Z_o$ ,  $A_v$ , and  $A_i$  are only slightly affected if  $h_r$  and  $h_o$  are not included in the model.

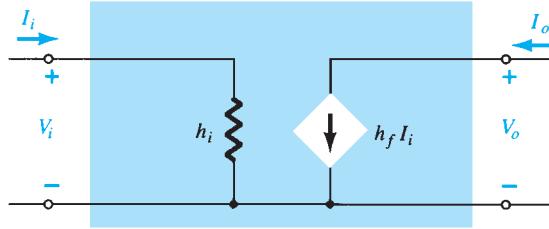
Because  $h_r$  is normally a relatively small quantity, its removal is approximated by  $h_r \approx 0$  and  $h_r V_o = 0$ , resulting in a short-circuit equivalent for the feedback element as shown in Fig. 5.99. The resistance determined by  $1/h_o$  is often large enough to be ignored in comparison to a parallel load, permitting its replacement by an open-circuit equivalent for the CE and CB models, as shown in Fig. 5.99.

The resulting equivalent of Fig. 5.100 is quite similar to the general structure of the common-base and common-emitter equivalent circuits obtained with the  $r_e$  model. In fact,



**FIG. 5.99**

Effect of removing  $h_{re}$  and  $h_{oe}$  from the hybrid equivalent circuit.



**FIG. 5.100**

Approximate hybrid equivalent model.

the hybrid equivalent and the  $r_e$  models for each configuration are repeated in Fig. 5.101 for comparison. It should be reasonably clear from Fig. 5.101a that

$$h_{ie} = \beta r_e \quad (5.139)$$

and

$$h_{fe} = \beta_{ac} \quad (5.140)$$

From Fig. 5.101b,

$$h_{ib} = r_e \quad (5.141)$$

and

$$h_{fb} = -\alpha \approx -1 \quad (5.142)$$

In particular, note that the minus sign in Eq. (5.142) accounts for the fact that the current source of the standard hybrid equivalent circuit is pointing down rather than in the actual direction as shown in the  $r_e$  model of Fig. 5.101b.

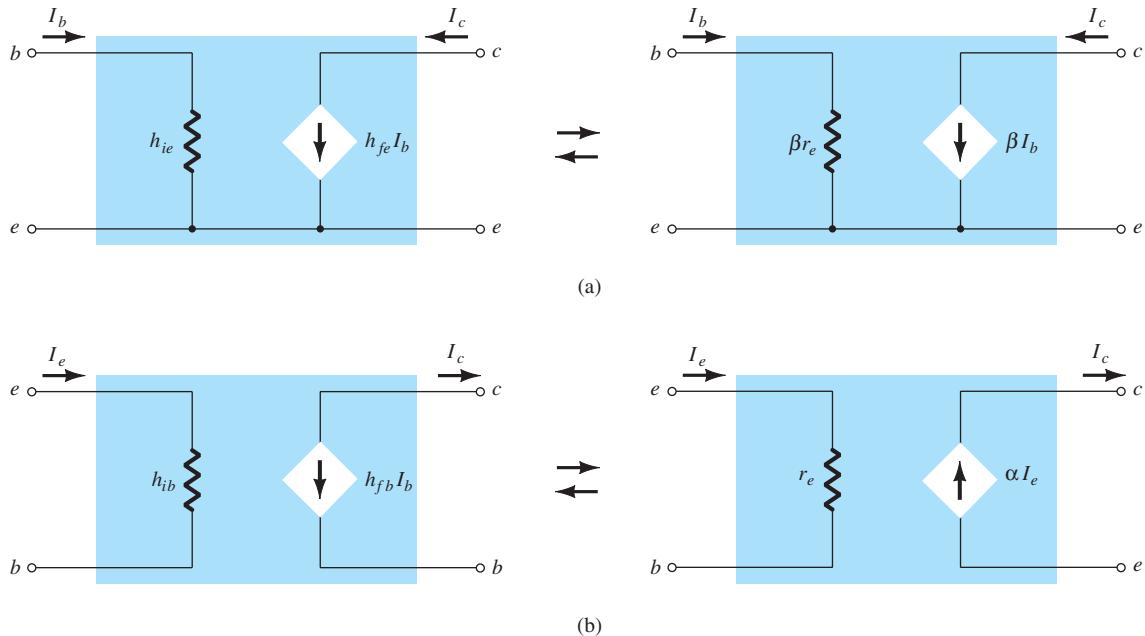


FIG. 5.101

Hybrid versus  $r_e$  model: (a) common-emitter configuration; (b) common-base configuration.

**EXAMPLE 5.19** Given  $I_E = 2.5 \text{ mA}$ ,  $h_{fe} = 140$ ,  $h_{oe} = 20 \mu\text{S}$  ( $\mu\text{mho}$ ), and  $h_{ob} = 0.5 \mu\text{S}$ , determine:

- The common-emitter hybrid equivalent circuit.
- The common-base  $r_e$  model.

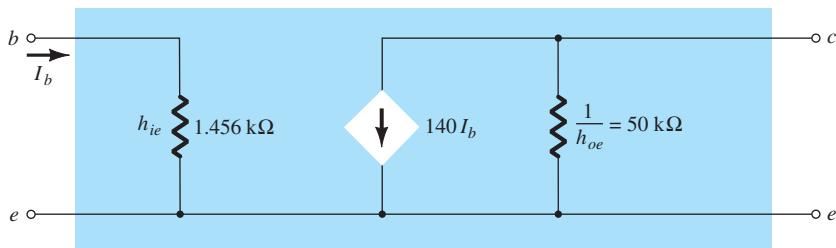
**Solution:**

a.  $r_e = \frac{26 \text{ mV}}{I_E} = \frac{26 \text{ mV}}{2.5 \text{ mA}} = 10.4 \Omega$

$h_{ie} = \beta r_e = (140)(10.4 \Omega) = 1.456 \text{ k}\Omega$

$r_o = \frac{1}{h_{oe}} = \frac{1}{20 \mu\text{S}} = 50 \text{ k}\Omega$

Note Fig. 5.102.

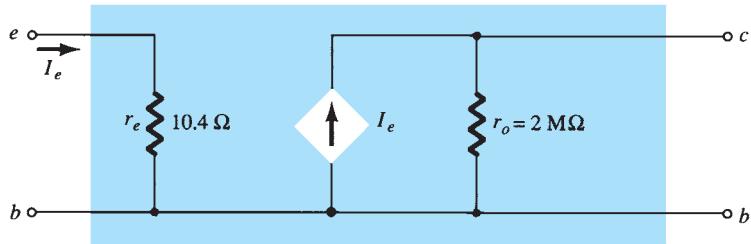
**FIG. 5.102**

Common-emitter hybrid equivalent circuit for the parameters of Example 5.19.

b.  $r_e = 10.4 \Omega$

$$\alpha \approx 1, \quad r_o = \frac{1}{h_{ob}} = \frac{1}{0.5 \mu\text{S}} = 2 \text{ M}\Omega$$

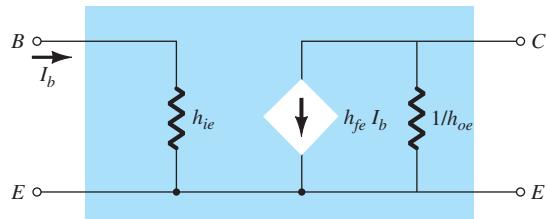
Note Fig. 5.103.

**FIG. 5.103**Common-base  $r_e$  model for the parameters of Example 5.19.

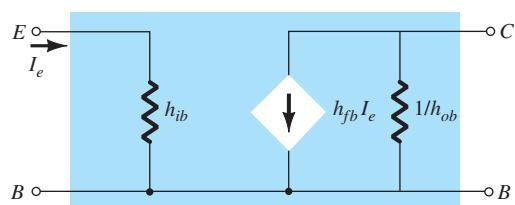
A series of equations relating the parameters of each configuration for the hybrid equivalent circuit is provided in Appendix B. In Section 5.23 it is demonstrated that the hybrid parameter  $h_{fe}$  ( $\beta_{ac}$ ) is the least sensitive of the hybrid parameters to a change in collector current. Assuming, therefore, that  $h_{fe} = \beta$  is a constant for the range of interest, is a fairly good approximation. It is  $h_{ie} = \beta r_e$  that will vary significantly with  $I_C$  and should be determined at operating levels because it can have a real effect on the gain levels of a transistor amplifier.

## 5.20 APPROXIMATE HYBRID EQUIVALENT CIRCUIT

The analysis using the approximate hybrid equivalent circuit of Fig. 5.104 for the common-emitter configuration and of Fig. 5.105 for the common-base configuration is very similar to that just performed using the  $r_e$  model. A brief overview of some of the most important configurations will be included in this section to demonstrate the similarities in approach and the resulting equations.

**FIG. 5.104**

Approximate common-emitter hybrid equivalent circuit.

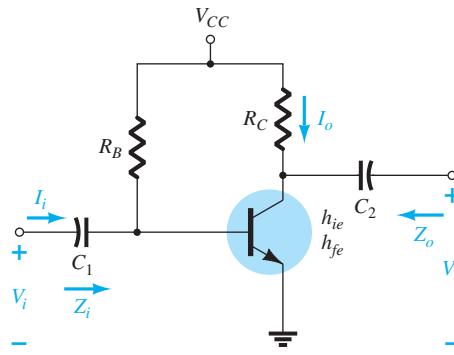
**FIG. 5.105**

Approximate common-base hybrid equivalent circuit.

Because the various parameters of the hybrid model are specified by a data sheet or experimental analysis, the dc analysis associated with use of the  $r_e$  model is not an integral part of the use of the hybrid parameters. In other words, when the problem is presented, the parameters such as  $h_{ie}$ ,  $h_{fe}$ ,  $h_{ib}$ , and so on, are specified. Keep in mind, however, that the hybrid parameters and components of the  $r_e$  model are related by the following equations, as discussed earlier in this chapter:  $h_{ie} = \beta r_e$ ,  $h_{fe} = \beta$ ,  $h_{oe} = 1/r_o$ ,  $h_{fb} = -\alpha$ , and  $h_{ib} = r_e$ .

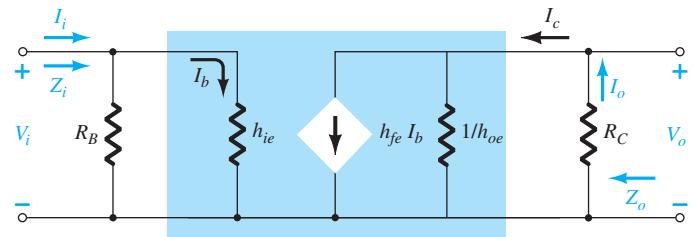
### Fixed-Bias Configuration

For the fixed-bias configuration of Fig. 5.106, the small-signal ac equivalent network will appear as shown in Fig. 5.107 using the approximate common-emitter hybrid equivalent model. Compare the similarities in appearance with Fig. 5.22 and the  $r_e$  model analysis. The similarities suggest that the analyses will be quite similar, and the results of one can be directly related to the other.



**FIG. 5.106**

Fixed-bias configuration.



**FIG. 5.107**

Substituting the approximate hybrid equivalent circuit into the ac equivalent network of Fig. 5.106.

**Z<sub>i</sub>** From Fig. 5.107,

$$Z_i = R_B \| h_{ie} \quad (5.143)$$

**Z<sub>o</sub>** From Fig. 5.107,

$$Z_o = R_C \| 1/h_{oe} \quad (5.144)$$

**A<sub>v</sub>** Using  $R' = 1/h_{oe} \| R_C$ , we obtain

$$\begin{aligned} V_o &= -I_o R' = -I_C R' \\ &= -h_{fe} I_b R' \end{aligned}$$

and

$$I_b = \frac{V_i}{h_{ie}}$$

with

$$V_o = -h_{fe} \frac{V_i}{h_{ie}} R'$$

so that

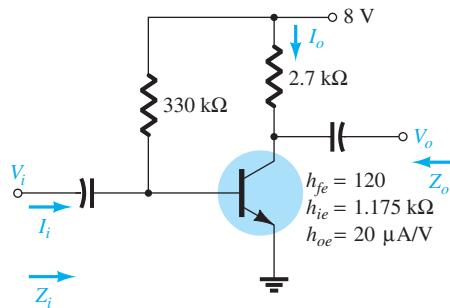
$$A_v = \frac{V_o}{V_i} = -\frac{h_{ie}(R_C \| 1/h_{oe})}{h_{ie}} \quad (5.145)$$

**A<sub>i</sub>** Assuming that  $R_B \gg h_{ie}$  and  $1/h_{oe} \geq 10R_C$ , we find  $I_b \cong I_i$  and  $I_o = I_c = h_{fe}I_b = h_{fe}I_i$ , and so

$$A_i = \frac{I_o}{I_i} \cong h_{fe} \quad (5.146)$$

**EXAMPLE 5.20** For the network of Fig. 5.108, determine:

- $Z_i$ .
- $Z_o$ .
- $A_v$ .
- $A_i$ .



**FIG. 5.108**

Example 5.20.

**Solution:**

a.  $Z_i = R_B \parallel h_{ie} = 330 \text{ k}\Omega \parallel 1.175 \text{ k}\Omega$   
 $\cong h_{ie} = 1.171 \text{ k}\Omega$

b.  $r_o = \frac{1}{h_{oe}} = \frac{1}{20 \mu\text{A}/\text{V}} = 50 \text{ k}\Omega$

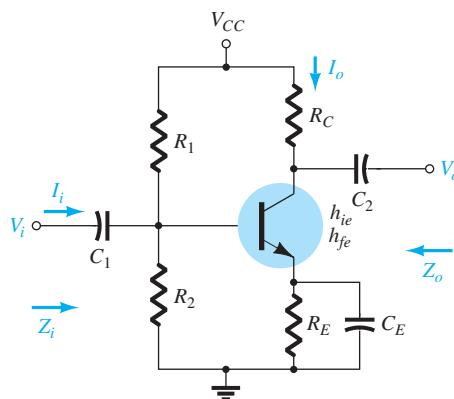
$$Z_o = \frac{1}{h_{oe}} \parallel R_C = 50 \text{ k}\Omega \parallel 2.7 \text{ k}\Omega = 2.56 \text{ k}\Omega \cong R_C$$

c.  $A_v = -\frac{h_{fe}(R_C \parallel 1/h_{oe})}{h_{ie}} = -\frac{(120)(2.7 \text{ k}\Omega \parallel 50 \text{ k}\Omega)}{1.171 \text{ k}\Omega} = -262.34$

d.  $A_i \cong h_{fe} = 120$

### Voltage-Divider Configuration

For the voltage-divider bias configuration of Fig. 5.109, the resulting small-signal ac equivalent network will have the same appearance as Fig. 5.107, with  $R_B$  replaced by  $R' = R_1 \parallel R_2$ .



**FIG. 5.109**

Voltage-divider bias configuration.

**Z<sub>i</sub>** From Fig. 5.107 with  $R_B = R'$ ,

$$Z_i = R_1 \parallel R_2 \parallel h_{ie} \quad (5.147)$$

**Z<sub>o</sub>** From Fig. 5.107,

$$Z_o \approx R_C \quad (5.148)$$

**A<sub>v</sub>**

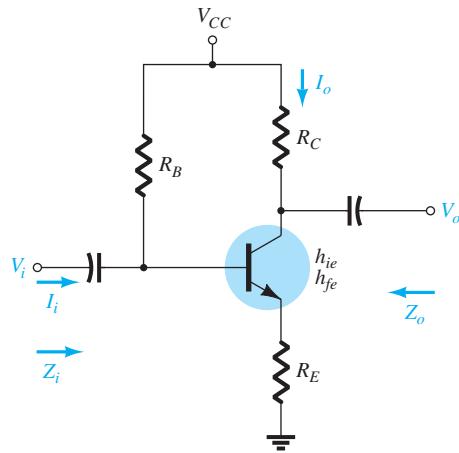
$$A_v = -\frac{h_{fe}(R_C \parallel 1/h_{oe})}{h_{ie}} \quad (5.149)$$

**A<sub>i</sub>**

$$A_i = \frac{h_{fe}(R_1 \parallel R_2)}{R_1 \parallel R_2 + h_{ie}} \quad (5.150)$$

### Unbypassed Emitter-Bias Configuration

For the CE unbypassed emitter-bias configuration of Fig. 5.110, the small-signal ac model will be the same as Fig. 5.30, with  $\beta r_e$  replaced by  $h_{ie}$  and  $\beta I_b$  by  $h_{fe}I_b$ . The analysis will proceed in the same manner.



**FIG. 5.110**  
CE unbypassed emitter-bias configuration.

**Z<sub>i</sub>**

$$Z_b \approx h_{fe}R_E \quad (5.151)$$

and

$$Z_i = R_B \parallel Z_b \quad (5.152)$$

**Z<sub>o</sub>**

$$Z_o = R_C \quad (5.153)$$

**A<sub>v</sub>**

$$A_v = -\frac{h_{fe}R_C}{Z_b} \cong -\frac{h_{fe}R_C}{h_{fe}R_E}$$

and

$$A_v \cong -\frac{R_C}{R_E} \quad (5.154)$$

$$A_i = -\frac{h_{fe}R_B}{R_B + Z_b} \quad (5.155)$$

or

$$A_i = -A_v \frac{Z_i}{R_C} \quad (5.156)$$

### Emitter-Follower Configuration

For the emitter-follower of Fig. 5.38, the small-signal ac model will match that of Fig. 5.111, with  $\beta r_e = h_{ie}$  and  $\beta = h_{fe}$ . The resulting equations will therefore be quite similar.

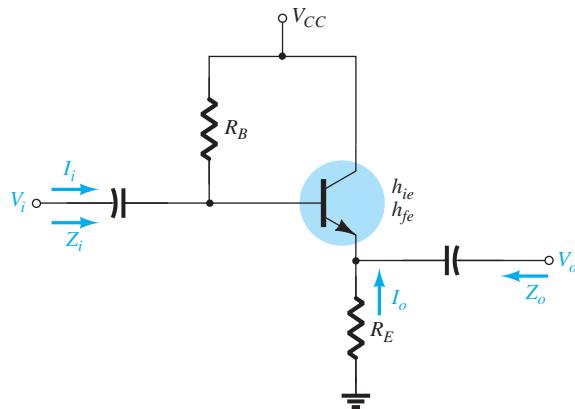


FIG. 5.111

Emitter-follower configuration.

$$Z_b \equiv h_{fe}R_E \quad (5.157)$$

$$Z_i = R_B \parallel Z_b \quad (5.158)$$

**Z<sub>i</sub>** For  $Z_o$ , the output network defined by the resulting equations will appear as shown in Fig. 5.112. Review the development of the equations in Section 5.8 and

$$Z_o = R_E \parallel \frac{h_{ie}}{1 + h_{fe}}$$

or, because  $1 + h_{fe} \approx h_{fe}$ ,

$$Z_o \equiv R_E \parallel \frac{h_{ie}}{h_{fe}} \quad (5.159)$$

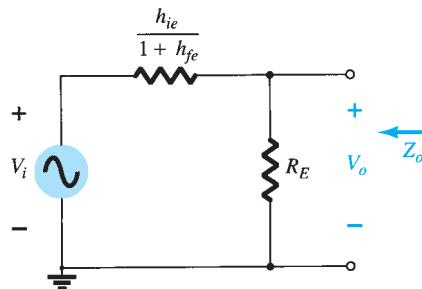


FIG. 5.112

Defining  $Z_o$  for the emitter-follower configuration.

**A<sub>v</sub>** For the voltage gain, the voltage-divider rule can be applied to Fig. 5.112 as follows:

$$V_o = \frac{R_E(V_i)}{R_E + h_{ie}/(1 + h_{fe})}$$

but, since  $1 + h_{fe} \approx h_{fe}$ ,

$$A_v = \frac{V_o}{V_i} \approx \frac{R_E}{R_E + h_{ie}/h_{fe}} \quad (5.160)$$

**A<sub>i</sub>**

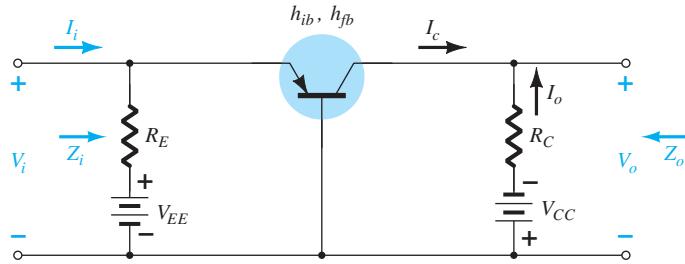
$$A_i = \frac{h_{fe} R_B}{R_B + Z_b} \quad (5.161)$$

or

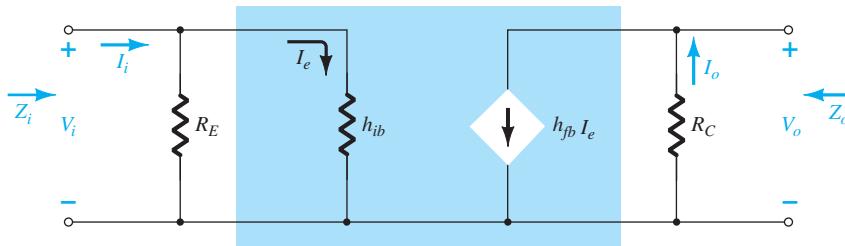
$$A_i = -A_v \frac{Z_i}{R_E} \quad (5.162)$$

### Common-Base Configuration

The last configuration to be examined with the approximate hybrid equivalent circuit will be the common-base amplifier of Fig. 5.113. Substituting the approximate common-base hybrid equivalent model results in the network of Fig. 5.114, which is very similar to Fig. 5.44.



**FIG. 5.113**  
Common-base configuration.



**FIG. 5.114**  
Substituting the approximate hybrid equivalent circuit into the ac equivalent network of Fig. 5.113.

We have the following results from Fig. 5.114.

**Z<sub>i</sub>**

$$Z_i = R_E \parallel h_{ib} \quad (5.163)$$

**Z<sub>o</sub>**

$$Z_o = R_C \quad (5.164)$$

**A<sub>v</sub>**

$$V_o = -I_o R_C = -(h_{fb} I_e) R_C$$

with  $I_e = \frac{V_i}{h_{ib}}$  and  $V_o = -h_{fb} \frac{V_i}{h_{ib}} R_C$

so that

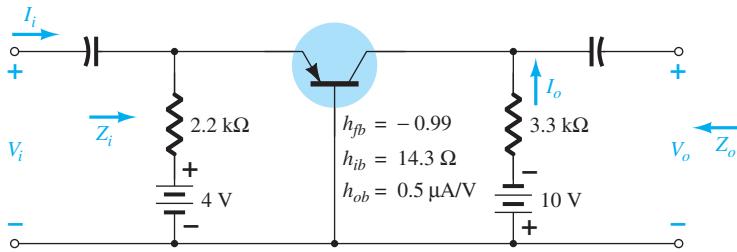
$$A_v = \frac{V_o}{V_i} = -\frac{h_{fb} R_C}{h_{ib}} \quad (5.165)$$

**A<sub>i</sub>**

$$A_i = \frac{I_o}{I_i} = h_{fb} \cong -1 \quad (5.166)$$

**EXAMPLE 5.21** For the network of Fig. 5.115, determine:

- a.  $Z_i$ .
- b.  $Z_o$ .
- c.  $A_v$ .
- d.  $A_i$ .



**FIG. 5.115**  
Example 5.21.

**Solution:**

- a.  $Z_i = R_E \| h_{ib} = 2.2 \text{ k}\Omega \| 14.3 \Omega = 14.21 \text{ }\Omega \cong h_{ib}$
- b.  $r_o = \frac{1}{h_{ob}} = \frac{1}{0.5 \mu\text{A}/\text{V}} = 2 \text{ M}\Omega$
- c.  $Z_o = \frac{1}{h_{ob}} \| R_C \cong R_C = 3.3 \text{ k}\Omega$
- c.  $A_v = -\frac{h_{fb} R_C}{h_{ib}} = -\frac{(-0.99)(3.3 \text{ k}\Omega)}{14.21} = 229.91$
- d.  $A_i \cong h_{fb} = -1$

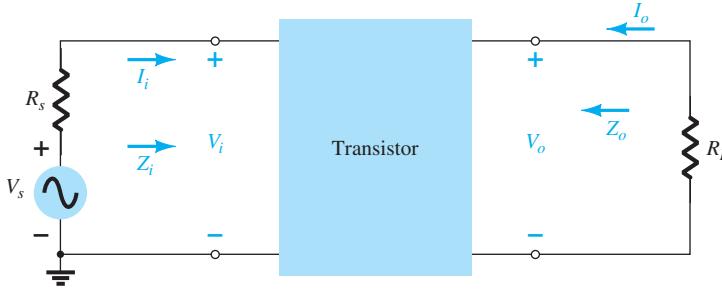
The remaining configurations that were not analyzed in this section are left as an exercise in the problem section of this chapter. It is assumed that the analysis above clearly reveals the similarities in approach using the  $r_e$  or approximate hybrid equivalent models, thereby removing any real difficulty with analyzing the remaining networks of the earlier sections.

## 5.21 COMPLETE HYBRID EQUIVALENT MODEL

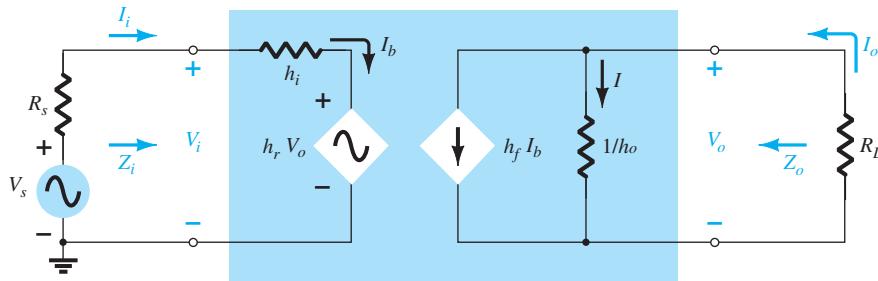
The analysis of Section 5.20 was limited to the approximate hybrid equivalent circuit with some discussion about the output impedance. In this section, we employ the complete equivalent circuit to show the effect of  $h_r$  and define in more specific terms the effect of  $h_o$ . It is important to realize that because the hybrid equivalent model has the same appearance for the common-base, common-emitter, and common-collector configurations, the equations developed in this section can be applied to each configuration. It is only necessary to

insert the parameters defined for each configuration. That is, for a common-base configuration,  $h_{fb}$ ,  $h_{ib}$ , and so on, are employed, whereas for a common-emitter configuration,  $h_{fe}$ ,  $h_{ie}$ , and so on, are used. Recall that Appendix A permits a conversion from one set to the other if one set is provided and the other is required.

Consider the general configuration of Fig. 5.116 with the two-port parameters of particular interest. The complete hybrid equivalent model is then substituted in Fig. 5.117 using parameters that do not specify the type of configuration. In other words, the solutions will be in terms of  $h_i$ ,  $h_r$ ,  $h_f$ , and  $h_o$ . Unlike the analysis of previous sections of this chapter, here the current gain  $A_i$  will be determined first because the equations developed will prove useful in the determination of the other parameters.



**FIG. 5.116**  
Two-port system.



**FIG. 5.117**  
Substituting the complete hybrid equivalent circuit into the two-port system of Fig. 5.116.

### Current Gain, $A_i = I_o/I_i$

Applying Kirchhoff's current law to the output circuit yields

$$I_o = h_f I_b + I = h_f I_i + \frac{V_o}{1/h_o} = h_f I_i + h_o V_o$$

Substituting  $V_o = -I_o R_L$  gives

$$I_o = h_f I_i - h_o R_L I_o$$

Rewriting the equation above, we have

$$I_o + h_o R_L I_o = h_f I_i$$

and

$$I_o(1 + h_o R_L) = h_f I_i$$

so that

$$A_i = \frac{I_o}{I_i} = \frac{h_f}{1 + h_o R_L} \quad (5.167)$$

Note that the current gain reduces to the familiar result of  $A_i = h_f$  if the factor  $h_o R_L$  is sufficiently small compared to 1.

### Voltage Gain, $A_v = V_o/V_i$

Applying Kirchhoff's voltage law to the input circuit results in

$$V_i = I_i h_i + h_r V_o$$

Substituting  $I_i = (1 + h_o R_L) I_o / h_f$  from Eq. (5.167) and  $I_o = -V_o / R_L$  from above results in

$$V_i = \frac{-(1 + h_o R_L) h_i}{h_f R_L} V_o + h_r V_o$$

Solving for the ratio  $V_o / V_i$  yields

$$A_v = \frac{V_o}{V_i} = \frac{-h_f R_L}{h_i + (h_i h_o - h_f h_r) R_L} \quad (5.168)$$

In this case, the familiar form of  $A_v = -h_f R_L / h_i$  returns if the factor  $(h_i h_o - h_f h_r) R_L$  is sufficiently small compared to  $h_i$ .

### Input Impedance, $Z_i = V_i/I_i$

For the input circuit,

$$V_i = h_i I_i + h_r V_o$$

Substituting

$$V_o = -I_o R_L$$

we have

$$V_i = h_i I_i - h_r R_L I_o$$

Because

$$A_i = \frac{I_o}{I_i}$$

$$I_o = A_i I_i$$

so that the equation above becomes

$$V_i = h_i I_i - h_r R_L A_i I_i$$

Solving for the ratio  $V_i / I_i$ , we obtain

$$Z_i = \frac{V_i}{I_i} = h_i - h_r R_L A_i$$

and substituting

$$A_i = \frac{h_f}{1 + h_o R_L}$$

yields

$$Z_i = \frac{V_i}{I_i} = h_i - \frac{h_f h_r R_L}{1 + h_o R_L} \quad (5.169)$$

The familiar form of  $Z_i = h_i$  is obtained if the second factor in the denominator  $(h_o R_L)$  is sufficiently smaller than one.

### Output Impedance, $Z_o = V_o/I_o$

The output impedance of an amplifier is defined to be the ratio of the output voltage to the output current with the signal  $V_s$  set to zero. For the input circuit with  $V_s = 0$ ,

$$I_i = -\frac{h_r V_o}{R_s + h_i}$$

Substituting this relationship into the equation from the output circuit yields

$$\begin{aligned} I_o &= h_f I_i + h_o V_o \\ &= -\frac{h_f h_r V_o}{R_s + h_i} + h_o V_o \end{aligned}$$

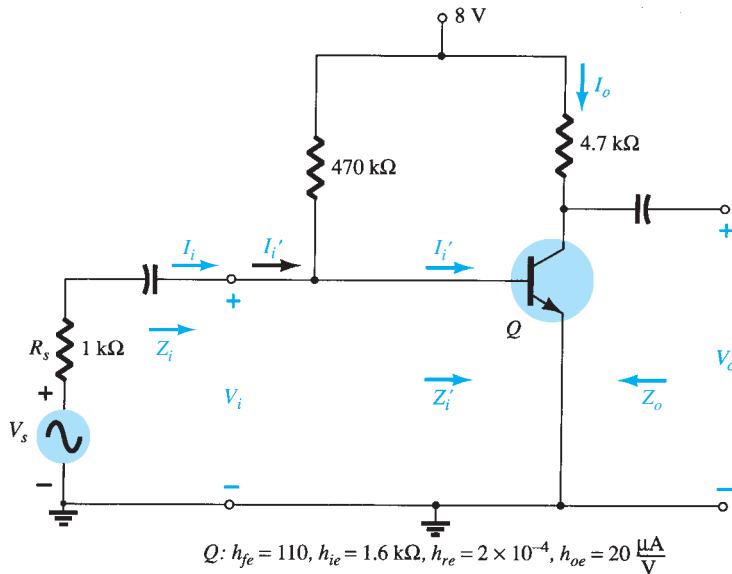
and

$$Z_o = \frac{V_o}{I_o} = \frac{1}{h_o - [h_f h_r / (h_i + R_s)]} \quad (5.170)$$

In this case, the output impedance is reduced to the familiar form  $Z_o = 1/h_o$  for the transistor when the second factor in the denominator is sufficiently smaller than the first.

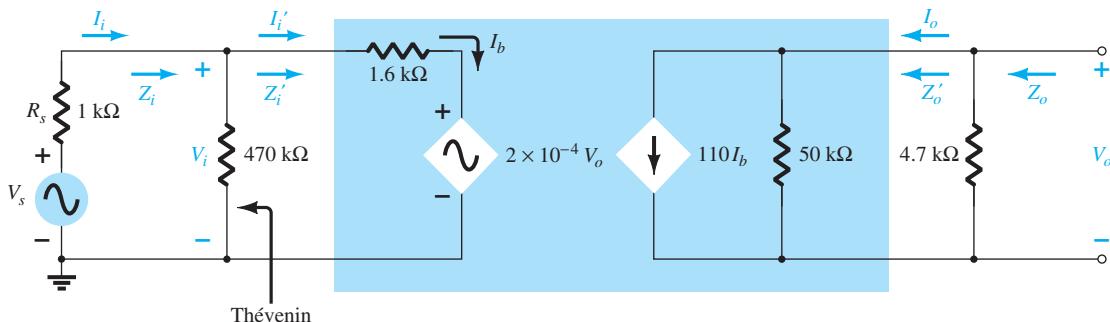
**EXAMPLE 5.22** For the network of Fig. 5.118, determine the following parameters using the complete hybrid equivalent model and compare to the results obtained using the approximate model.

- $Z_i$  and  $Z'_i$ .
- $A_v$ .
- $A_i = I_o/I_i$ .
- $Z'_o$  (within  $R_C$ ) and  $Z_o$  (including  $R_C$ ).

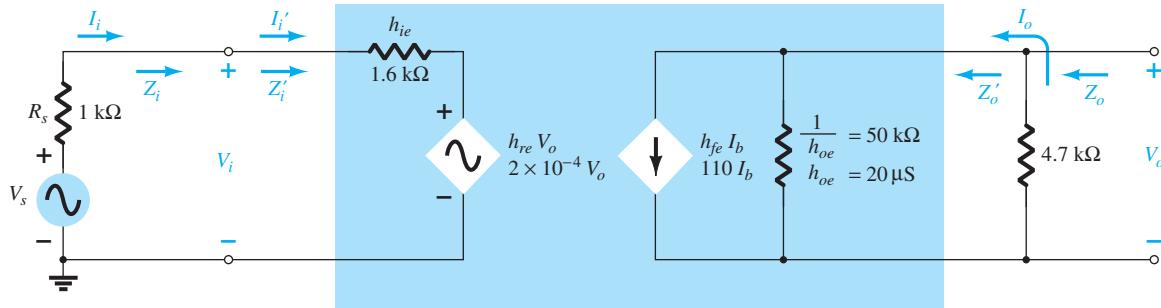


**FIG. 5.118**  
Example 5.22.

**Solution:** Now that the basic equations for each quantity have been derived, the order in which they are calculated is arbitrary. However, the input impedance is often a useful quantity to know, and therefore will be calculated first. The complete common-emitter hybrid equivalent circuit has been substituted and the network redrawn as shown in Fig. 5.119. A Thévenin equivalent circuit for the input section of Fig. 5.119 results in the input equivalent of Fig. 5.120 because  $E_{Th} \equiv V_s$  and  $R_{Th} \equiv R_s = 1\text{ k}\Omega$  (a result of  $R_B = 470\text{ k}\Omega$  being much greater than  $R_s = 1\text{ k}\Omega$ ). In this example,  $R_L = R_C$ , and  $I_o$  is defined as the current through  $R_C$  as in previous examples of this chapter. The output impedance  $Z_o$  as defined by Eq. (5.170) is for the output transistor terminals only. It does not include the effects of  $R_C$ .  $Z_o$  is simply the parallel combination of  $Z_o$  and  $R_L$ . The resulting configuration of



**FIG. 5.119**  
Substituting the complete hybrid equivalent circuit into the ac equivalent network of Fig. 5.118.



**FIG. 5.120**

Replacing the input section of Fig. 5.119 with a Thévenin equivalent circuit.

Fig. 5.120 is then an exact duplicate of the defining network of Fig. 5.117, and the equations derived above can be applied.

a. Eq. (5.169):

$$\begin{aligned} Z_i &= \frac{V_i}{I_i} = h_{ie} - \frac{h_{fe}h_{re}R_L}{1 + h_{oe}R_L} \\ &= 1.6 \text{ k}\Omega - \frac{(110)(2 \times 10^{-4})(4.7 \text{ k}\Omega)}{1 + (20 \mu\text{s})(4.7 \text{ k}\Omega)} \\ &= 1.6 \text{ k}\Omega - 94.52 \Omega \\ &= \mathbf{1.51 \text{ k}\Omega} \end{aligned}$$

versus 1.6 kΩ using simply  $h_{ie}$ ; and

$$Z'_i = 470 \text{ k}\Omega \| Z_i \cong Z_i = \mathbf{1.51 \text{ k}\Omega}$$

b. Eq. (5.168):

$$\begin{aligned} A_v &= \frac{V_o}{V_i} = \frac{-h_{fe}R_L}{h_{ie} + (h_{ie}h_{oe} - h_{fe}h_{re})R_L} \\ &= \frac{-(110)(4.7 \text{ k}\Omega)}{1.6 \text{ k}\Omega + [(1.6 \text{ k}\Omega)(20 \mu\text{s}) - (110)(2 \times 10^{-4})]4.7 \text{ k}\Omega} \\ &= \frac{-517 \times 10^3 \Omega}{1.6 \text{ k}\Omega + (0.032 - 0.022)4.7 \text{ k}\Omega} \\ &= \frac{-517 \times 10^3 \Omega}{1.6 \text{ k}\Omega + 47 \Omega} \\ &= \mathbf{-313.9} \end{aligned}$$

versus  $-323.125$  using  $A_v \cong -h_{fe}R_L/h_{ie}$ .

c. Eq. (5.167):

$$\begin{aligned} A'_i &= \frac{I_o}{I'_i} = \frac{h_{fe}}{1 + h_{oe}R_L} = \frac{110}{1 + (20 \mu\text{s})(4.7 \text{ k}\Omega)} \\ &= \frac{110}{1 + 0.094} = \mathbf{100.55} \end{aligned}$$

versus 110 using simply  $h_{fe}$ . Because  $470 \text{ k}\Omega \gg Z'_i$ ,  $I_i \cong I'_i$  and  $A_i \cong 100.55$  also.

d. Eq. (5.170):

$$\begin{aligned} Z'_o &= \frac{V_o}{I_o} = \frac{1}{h_{oe} - [h_{fe}h_{re}/(h_{ie} + R_s)]} \\ &= \frac{1}{20 \mu\text{s} - [(110)(2 \times 10^{-4})/(1.6 \text{ k}\Omega + 1 \text{ k}\Omega)]} \\ &= \frac{1}{20 \mu\text{s} - 8.46 \mu\text{s}} \\ &= \frac{1}{11.54 \mu\text{s}} \\ &= \mathbf{86.66 \text{ k}\Omega} \end{aligned}$$

which is greater than the value determined from  $1/h_{oe}$ , 50 k $\Omega$ ; and

$$Z_o = R_C \| Z'_o = 4.7 \text{ k}\Omega \| 86.66 \text{ k}\Omega = \mathbf{4.46 \text{ k}\Omega}$$

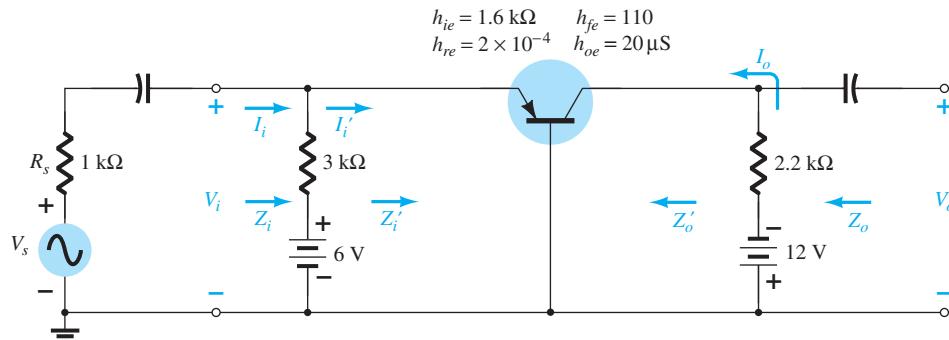
versus 4.7 k $\Omega$  using only  $R_C$ .

Note from the results above that the approximate solutions for  $A_v$  and  $Z_i$  were very close to those calculated with the complete equivalent model. In fact, even  $A_i$  was off by less than 10%. The higher value of  $Z'_o$  only contributed to our earlier conclusion that  $Z'_o$  is often so high that it can be ignored compared to the applied load. However, keep in mind that when there is a need to determine the effect of  $h_{re}$  and  $h_{oe}$ , the complete hybrid equivalent model must be used, as described earlier.

The specification sheet for a particular transistor typically provides the common-emitter parameters as noted in Fig. 5.92. The next example will employ the same transistor parameters appearing in Fig. 5.118 in a *pnp* common-base configuration to introduce the parameter conversion procedure and emphasize the fact that the hybrid equivalent model maintains the same layout.

**EXAMPLE 5.23** For the common-base amplifier of Fig. 5.121, determine the following parameters using the complete hybrid equivalent model and compare the results to those obtained using the approximate model.

- a.  $Z_i$
- b.  $A_i$
- c.  $A_v$ .
- d.  $Z_o$



**FIG. 5.121**  
Example 5.23.

**Solution:** The common-base hybrid parameters are derived from the common-emitter parameters using the approximate equations of Appendix B:

$$h_{ib} \cong \frac{h_{ie}}{1 + h_{fe}} = \frac{1.6 \text{ k}\Omega}{1 + 110} = \mathbf{14.41 \Omega}$$

Note how closely the magnitude compares with the value determined from

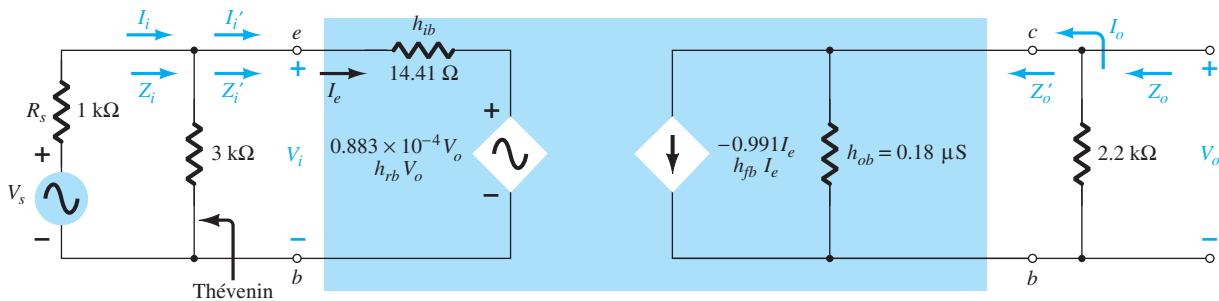
$$h_{ib} = r_e = \frac{h_{ie}}{\beta} = \frac{1.6 \text{ k}\Omega}{110} = 14.55 \Omega$$

Also,

$$h_{rb} \cong \frac{h_{ie}h_{oe}}{1 + h_{fe}} - h_{re} = \frac{(1.6 \text{ k}\Omega)(20 \mu\text{S})}{1 + 110} - 2 \times 10^{-4} \\ = \mathbf{0.883 \times 10^{-4}}$$

$$h_{fb} \cong \frac{-h_{fe}}{1 + h_{fe}} = \frac{-110}{1 + 110} = \mathbf{-0.991}$$

$$h_{ob} \cong \frac{h_{oe}}{1 + h_{fe}} = \frac{20 \mu\text{S}}{1 + 110} = \mathbf{0.18 \mu\text{S}}$$



**FIG. 5.122**

Small-signal equivalent for the network of Fig. 5.121.

Substituting the common-base hybrid equivalent circuit into the network of Fig. 5.121 results in the small-signal equivalent network of Fig. 5.122. The Thévenin network for the input circuit results in  $R_{Th} = 3 \text{ k}\Omega \parallel 1 \text{ k}\Omega = 0.75 \text{ k}\Omega$  for  $R_s$  in the equation for  $Z_o$ .

a. Eq. (5.169):

$$\begin{aligned} Z'_i &= \frac{V_i}{I'_i} = h_{ib} - \frac{h_{fb}h_{rb}R_L}{1 + h_{ob}R_L} \\ &= 14.41 \Omega - \frac{(-1.991)(0.883 \times 10^{-4})(2.2 \text{ k}\Omega)}{1 + (0.18 \mu\text{S})(2.2 \text{ k}\Omega)} \\ &= 14.41 \Omega + 0.19 \Omega \\ &= 14.60 \Omega \end{aligned}$$

versus 14.41 Ω using  $Z_i \equiv h_{ib}$ ; and

$$Z_i = 3 \text{ k}\Omega \parallel Z'_i \cong Z'_i = \mathbf{14.60 \Omega}$$

b. Eq. (5.167):

$$\begin{aligned} A'_i &= \frac{I_o}{I'_i} = \frac{h_{fb}}{1 + h_{ob}R_L} \\ &= \frac{-0.991}{1 + (0.18 \mu\text{S})(2.2 \text{ k}\Omega)} \\ &= -0.991 \end{aligned}$$

Because  $3 \text{ k}\Omega \gg Z'_i$ ,  $I_i \cong I'_i$  and  $A_i = I_o/I_i \cong -1$ .

c. Eq. (5.168):

$$\begin{aligned} A_v &= \frac{V_o}{V_i} = \frac{-h_{fb}R_L}{h_{ib} + (h_{ib}h_{ob} - h_{fb}h_{rb})R_L} \\ &= \frac{-(-0.991)(2.2 \text{ k}\Omega)}{14.41 \Omega + [(14.41 \Omega)(0.18 \mu\text{S}) - (-0.991)(0.883 \times 10^{-4})]2.2 \text{ k}\Omega} \\ &= \mathbf{149.25} \end{aligned}$$

versus 151.3 using  $A_v \cong -h_{fb}R_L/h_{ib}$ .

d. Eq. (5.170):

$$\begin{aligned} Z'_o &= \frac{1}{h_{ob} - [h_{fb}h_{rb}/(h_{ib} + R_s)]} \\ &= \frac{1}{0.18 \mu\text{S} - [(-0.991)(0.883 \times 10^{-4})/(14.41 \Omega + 0.75 \text{ k}\Omega)]} \\ &= \frac{1}{0.295 \mu\text{S}} \\ &= \mathbf{3.39 \text{ M}\Omega} \end{aligned}$$

versus 5.56 MΩ using  $Z'_o \cong 1/h_{ob}$ . For  $Z_o$  as defined by Fig. 5.122,

$$Z_o = R_C \parallel Z'_o = 2.2 \text{ k}\Omega \parallel 3.39 \text{ M}\Omega = \mathbf{2.199 \text{ k}\Omega}$$

versus 2.2 kΩ using  $Z_o \cong R_C$ .

The last transistor model to be introduced is the hybrid  $\pi$  model of Fig. 5.123 which includes parameters that do not appear in the other two models primarily to provide a more accurate model for high-frequency effects.

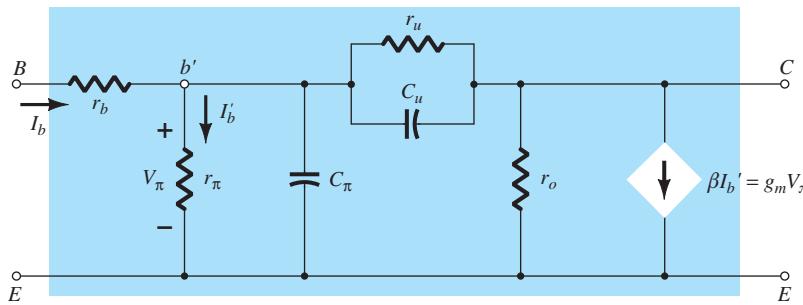


FIG. 5.123

Giacoletto (or hybrid  $\pi$ ) high-frequency transistor small-signal ac equivalent circuit.

### $r_\pi$ , $r_o$ , $r_b$ , and $r_u$

The resistors  $r_\pi$ ,  $r_o$ ,  $r_b$ , and  $r_u$  are the resistances between the indicated terminals of the device when the device is in the active region. The resistance  $r_\pi$  (using the symbol  $\pi$  to agree with the hybrid  $\pi$  terminology) is simply  $\beta r_e$  as introduced for the common-emitter  $r_e$  model.

That is,

$$r_\pi = \beta r_e \quad (5.171)$$

The output resistance  $r_o$  is the output resistance normally appearing across an applied load. Its value, which typically lies between 5 k $\Omega$  and 40 k $\Omega$ , is determined from the hybrid parameter  $h_{oe}$ , the Early voltage, or the output characteristics.

The resistance  $r_b$  includes the base contact, base bulk, and base spreading resistance levels. The first is due to the actual connection to the base. The second includes the resistance from the external terminal to the active region of the transistor, and the last is the actual resistance within the active base region. It is typically a few ohms to tens of ohms.

The resistance  $r_u$  (the subscript  $u$  refers to the *union* it provides between collector and base terminals) is a very large resistance and provides a feedback path from output to input circuits in the equivalent model. It is typically larger than  $\beta r_o$ , which places it in the megohm range.

### $C_\pi$ and $C_u$

All the capacitors that appear in Fig. 5.123 are stray parasitic capacitors between the various junctions of the device. They are all capacitive effects that really only come into play at high frequencies. For low to mid-frequencies their reactance is very large, and they can be considered open circuits. The capacitor  $C_\pi$  across the input terminals can range from a few pF to tens of pF. The capacitor  $C_u$  from base to collector is usually limited to a few pF but is magnified at the input and output by an effect called the Miller effect, to be introduced in Chapter 9.

### $\beta I_b'$ or $g_m V_\pi$

It is important to note in Fig. 5.123 that the controlled source can be a voltage-controlled current source (VCCS) or a current-controlled current source (CCCS), depending on the parameters employed.

Note the following parameter equivalence in Fig. 5.123:

$$g_m = \frac{1}{r_e} \quad (5.172)$$

and

$$r_o = \frac{1}{h_{oe}} \quad (5.173)$$

with

$$\frac{r_\pi}{r_\pi + r_u} \cong \frac{r_\pi}{r_u} \cong h_{re} \quad (5.174)$$

Take particular note of the fact that the equivalent sources  $\beta I'_b$  and  $g_m V_\pi$  are both controlled current sources. One is controlled by a current at another place in the network and the other by a voltage at the input side of the network. The equivalence between the two is defined by

$$\beta I'_b = \frac{1}{r_e} \cdot r_e \beta I'_b = g_m I'_b \beta r_e = g_m (I'_b r_\pi) = g_m V_\pi$$

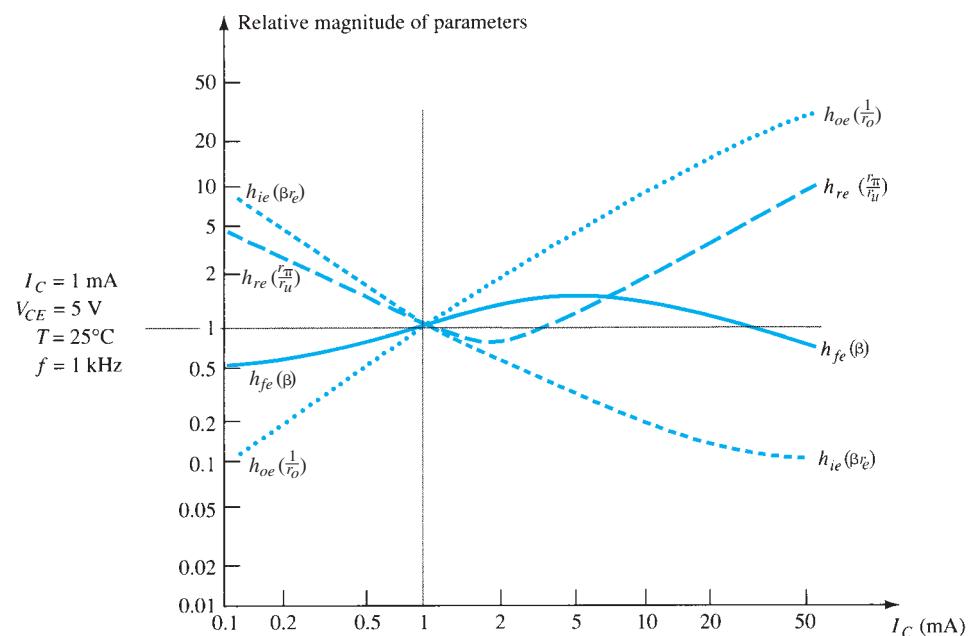
For the broad range of low- to mid-frequency analysis, the effect of the stray capacitive effects can be ignored due to the very high reactance levels associated with each. The resistance  $r_b$  is usually small enough with other series elements to be ignored while the resistance  $r_u$  is usually large enough compared to parallel elements to be ignored. The result is an equivalent network similar to the  $r_e$  model introduced and applied in this chapter.

In Chapter 9, when high-frequency effects are considered, the hybrid  $\pi$  model will be the model of choice.

## 5.23 VARIATIONS OF TRANSISTOR PARAMETERS

A variety of curves can be drawn to show the variations of the transistor parameters with temperature, frequency, voltage, and current. The most interesting and useful at this stage of the development include the variations with junction temperature and collector voltage and current.

The effect of the collector current on the  $r_e$  model and hybrid equivalent model is shown in Fig. 5.124. Take careful note of the logarithmic scale on the vertical and horizontal axes. Logarithmic scales will be examined in detail in Chapter 9. The parameters have all been normalized (a process described in detail in Section 9.5) to unity so that the relative change in magnitude with collector current can easily be determined. On each set of curves, such as in Figs. 5.124 to 5.126, the operating point at which the parameters were determined is always indicated. For this particular situation, the quiescent point is at the fairly typical values of  $V_{CE} = 5.0$  V and  $I_C = 1.0$  mA. Because the frequency and temperature of operation



**FIG. 5.124**  
Hybrid parameter variations with collector current.

also affect the parameters, these quantities are also indicated on the curves. Figure 5.124 shows the variation of the parameters with collector current. Note that at  $I_C = 1$  mA the value of all the parameters has been normalized to 1 on the vertical axis. The result is that the magnitude of each parameter is compared to the values at the defined operating point. Because manufacturers typically use the hybrid parameters for plots of this type, they are the curves of choice in Fig. 5.124. However, to broaden the use of the curves the  $r_e$  and hybrid  $\pi$  equivalent parameters have also been added.

At first glance it is particularly interesting to note that:

**The parameter  $h_{fe}(\beta)$  varies the least of all the parameters of a transistor equivalent circuit when plotted against variations in collector current.**

Figure 5.124 clearly reveals that for the full range of collector current the parameter  $h_{fe}(\beta)$  varies from 0.5 of its  $Q$ -point value to a peak of about 1.5 times that value at a current of about 6 mA. For a transistor with a  $\beta$  of 100, it therefore varies from about 50 to 150. This seems like quite a bit, but look at  $h_{oe}$ , which jumps to almost 40 times its  $Q$ -point value at a collector current of 50 mA.

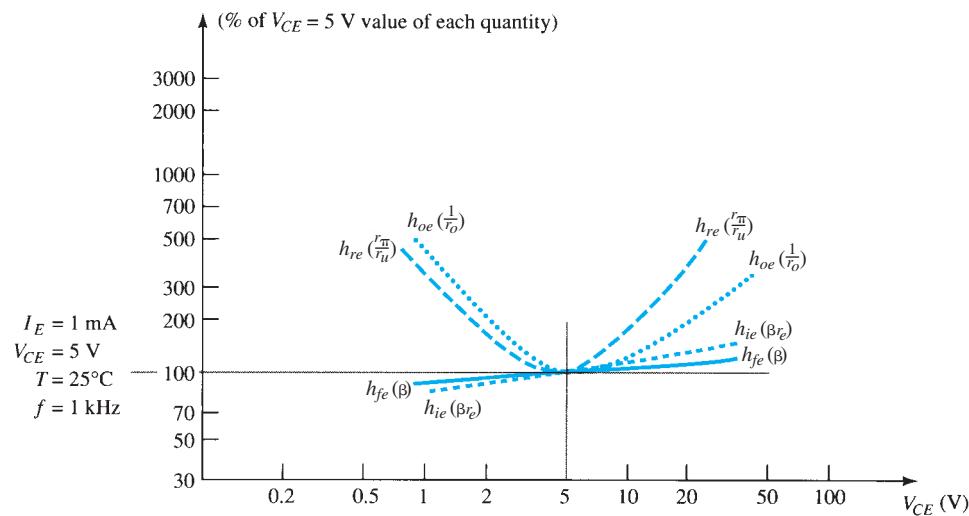
Figure 5.124 also shows that  $h_{oe}(1/r_o)$  and  $h_{ie}(\beta r_e)$  vary the most for the chosen current range. The parameter  $h_{ie}$  varies from about 10 times its  $Q$ -point value down to about one tenth the  $Q$  point value at 50 mA. This variation, however, should be expected because we know that the value of  $r_e$  is directly related to the emitter current by  $r_e = 26 \text{ mV}/I_E$ . As  $I_E (\equiv I_C)$  increases, the value of  $r_e$  and therefore  $\beta r_e$  will decrease, as shown in Fig. 5.124.

Keep in mind as you review the curve of  $h_{oe}$  versus current that the actual output resistance  $r_o$  is  $1/h_{oe}$ . Therefore, as the curve increases with current, the value of  $r_o$  becomes less and less. Because  $r_o$  is a parameter that normally appears in parallel with the applied load, decreasing values of  $r_o$  can become a critical problem. The fact that  $r_o$  has dropped to almost 1/40 of its value at the  $Q$ -point could spell a real reduction in gain at 50 mA.

The parameter  $h_{re}$  varies quite a bit, but because its  $Q$ -point value is usually small enough to permit ignoring its effect, it is a parameter that is only of concern for collector currents that are much less, or quite a bit more, than the  $Q$ -point level.

This may seem like an extensive description of a set of characteristic curves. However, experience has revealed that graphs of this nature are too often reviewed without taking the time to fully appreciate the broad impact of what they are providing. These plots reveal a lot of information that could be extremely useful in the design process.

Figure 5.125 shows the variation in magnitude of the parameters due to changes in collector-to-emitter voltage. This set of curves is normalized at the same operating point as the curves of Fig. 5.124 to permit comparisons between the two. In this case, however, the vertical scale is in percent rather than whole numbers. The 200% level defines a set of parameters twice that at the 100% level. A level of 1000% would reflect a 10:1 change. Note that  $h_{fe}$  and  $h_{ie}$  are relatively steady in magnitude with variations in collector-to-emitter voltage, whereas for changes in collector current the variation is a great deal more



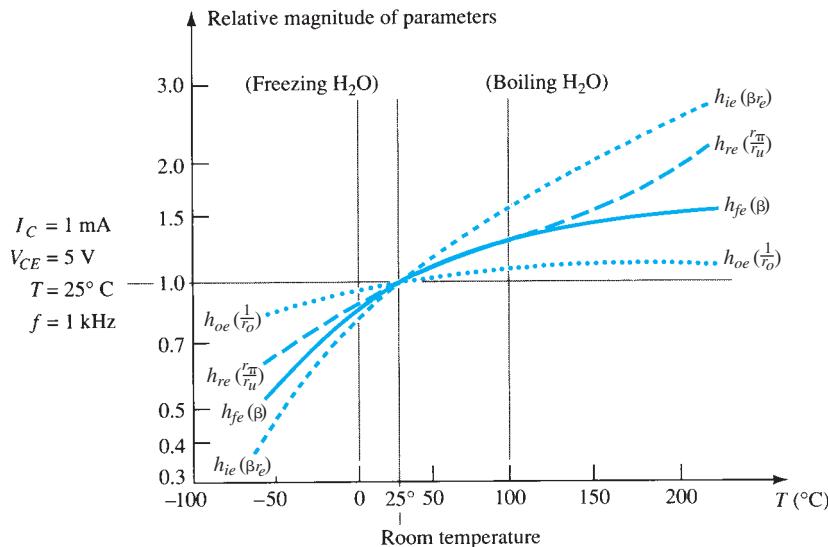
**FIG. 5.125**

Hybrid parameter variations with collector-emitter potential.

significant. In other words, if you want a parameter such as  $h_{ie}(\beta r_e)$  to remain fairly steady, keep the variation of  $I_C$  to a minimum while worrying less about variations in the collector-to-emitter voltage. The variation of  $h_{oe}$  and  $h_{ie}$  remains significant for the indicated range of collector-to-emitter voltage.

In Fig. 5.126, the variation in parameters is plotted for changes in junction temperature. The normalization value is taken to be room temperature,  $T = 25^\circ\text{C}$ . The horizontal scale is now a linear scale rather than the logarithmic scale employed in the two previous figures. In general:

**All the parameters of a hybrid transistor equivalent circuit increase with temperature.**



**FIG. 5.126**  
Hybrid parameter variations with temperature.

However, again keep in mind that the actual output resistance  $r_o$  is inversely related to  $h_{oe}$ , so its value drops with an increase in  $h_{oe}$ . The greatest change is in  $h_{ie}$ , although note that the range of the vertical scale is considerably less than in the other plots. At a temperature of  $200^\circ\text{C}$  the value of  $h_{ie}$  is almost 3 times its  $Q$ -point value, but in Fig. 5.124 parameters jumped to almost 40 times the  $Q$ -point value.

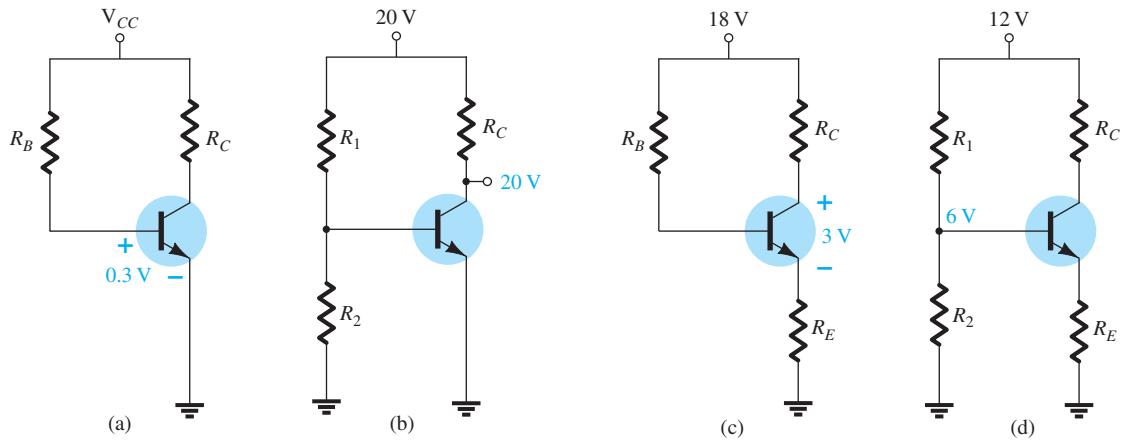
Of the three parameters, therefore, the variation in collector current has by far the greatest effect on the parameters of a transistor equivalent circuit. Temperature is always a factor, but the effect of the collector current can be significant.

## 5.24 TROUBLESHOOTING

Although the terminology *troubleshooting* suggests that the procedures to be described are designed simply to isolate a malfunction, it is important to realize that the same techniques can be applied to ensure that a system is operating properly. In any case, the testing, checking, and isolating procedures require an understanding of what to expect at various points in the network in both the dc and ac domains. In most cases, a network operating correctly in the dc mode will also behave properly in the ac domain.

***In general, therefore, if a system is not working properly, first disconnect the ac source and check the dc biasing levels.***

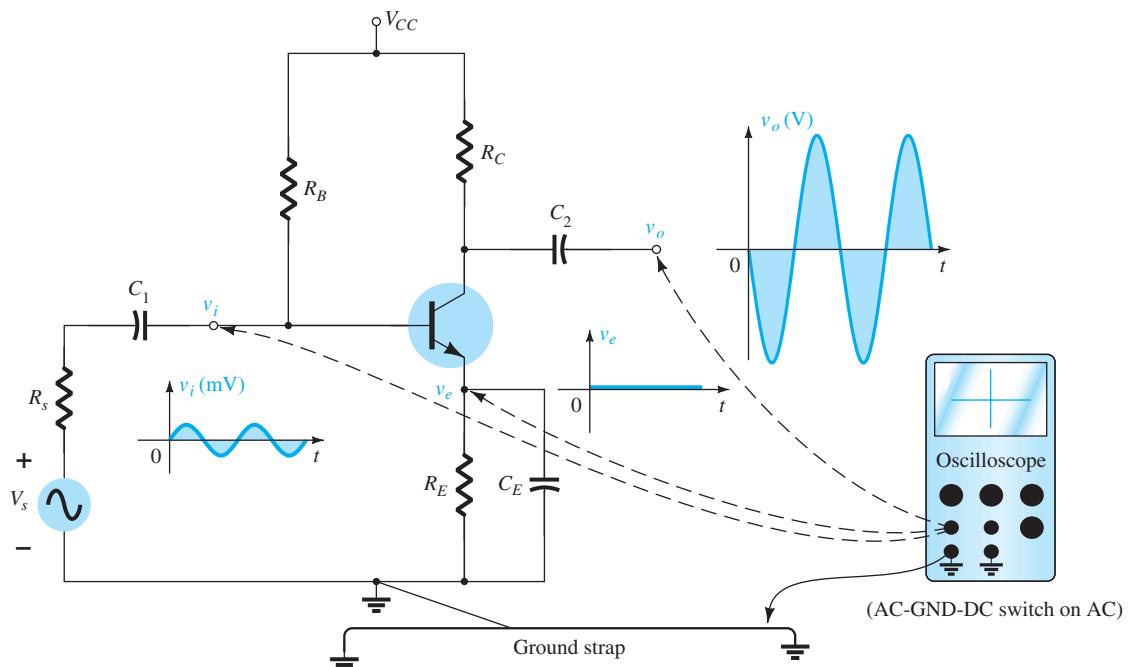
In Fig. 5.127 we have four transistor configurations with specific voltage levels provided as measured by a DMM in the dc mode. The first test of any transistor network is to simply measure the base-to-emitter voltage of the transistor. The fact that it is only 0.3 V in this case suggests that the transistor is not “on” and perhaps sitting in its saturation mode. If this is a switching design then the result is expected, but if in the amplifier mode there is an open connection preventing the base voltage from reaching an operating level.



**FIG. 5.127**  
Checking the dc levels to determine if a network is properly biased.

In Fig. 5.127b the fact that the voltage at the collector equals the supply voltage reveals that there is no drop across the resistor  $R_C$  and the collector current is zero. The resistor  $R_C$  is connected properly because it made the connection from the dc source to the collector. However, any one of the other elements may not have been connected properly, resulting in the absence of a base or collector current. In Fig. 5.127c the voltage drop across the collector-to-emitter voltage is too small compared with the applied dc voltage. Normally the voltage  $V_{CE}$  is in the mid-range of perhaps 6 V to 14 V. A reading of 18 V would cause the same concern as the reading of 3 V. The fact that the voltage levels exist at all suggests that all the elements are connected but the value of one or more of the resistive elements may be wrong. In Fig. 5.127d we find that the voltage at the base is exactly half the supply voltage. We know from this chapter that the resistance  $R_E$  will reflect back to the base by a factor of beta and appear in parallel with  $R_2$ . The result would be a base voltage less than half the supply voltage. The measurement suggests that the base lead is not connected to the voltage divider, causing an even split of the 20-V source.

In a typical laboratory setting, the ac response at various points in the network is checked with an oscilloscope as shown in Fig. 5.128. Note that the black (gnd) lead of the oscilloscope is connected directly to ground and the red lead is moved from point to point in the



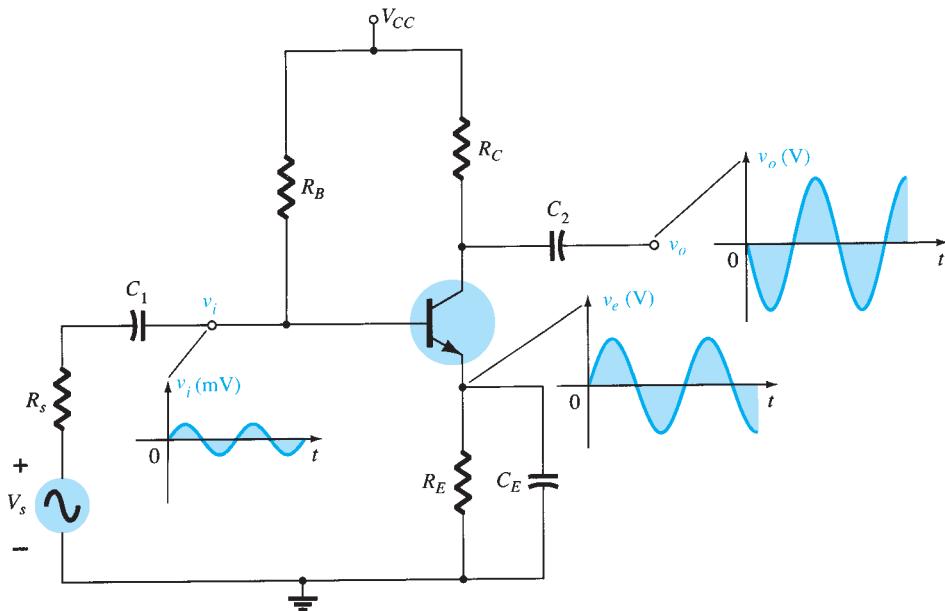
**FIG. 5.128**  
Using the oscilloscope to measure and display various voltages of a BJT amplifier.

network, providing the patterns appearing in Fig. 5.128. The vertical channels are set in the ac mode to remove any dc component associated with the voltage at a particular point. The small ac signal applied to the base is amplified to the level appearing from collector to ground. Note the difference in vertical scales for the two voltages. There is no ac response at the emitter terminal due to the short-circuit characteristics of the capacitor at the applied frequency. The fact that  $v_o$  is measured in volts and  $v_i$  in millivolts suggests a sizable gain for the amplifier. In general, the network appears to be operating properly. If desired, the dc mode of the multimeter could be used to check  $V_{BE}$  and the levels of  $V_B$ ,  $V_{CE}$ , and  $V_E$  to review whether they lie in the expected range. Of course, the oscilloscope can also be used to compare dc levels simply by switching to the dc mode for each channel.

A poor ac response can be due to a variety of reasons. In fact, there may be more than one problem area in the same system. Fortunately, however, with time and experience, the probability of malfunctions in some areas can be predicted, and an experienced person can isolate problem areas fairly quickly.

In general, there is nothing mysterious about the general troubleshooting process. If you decide to follow the ac response, it is good procedure to start with the applied signal and progress through the system toward the load, checking critical points along the way. An unexpected response at some point suggests that the network is fine up to that area, thereby defining the region that must be investigated further. The waveform obtained on the oscilloscope will certainly help in defining the possible problems with the system.

If the response for the network of Fig. 5.128 is as appears in Fig. 5.129, the network has a malfunction that is probably in the emitter area. An ac response across the emitter is unexpected, and the gain of the system as revealed by  $v_o$  is much lower. Recall for this configuration that the gain is much greater if  $R_E$  is bypassed. The response obtained suggests that  $R_E$  is not bypassed by the capacitor, and the terminal connections of the capacitor and the capacitor itself should be checked. In this case, a checking of the dc levels will probably not isolate the problem area because the capacitor has an “open-circuit” equivalent for dc. In general, prior knowledge of what to expect, familiarity with the instrumentation, and, most important, experience are all factors that contribute to the development of an effective approach to the art of troubleshooting.

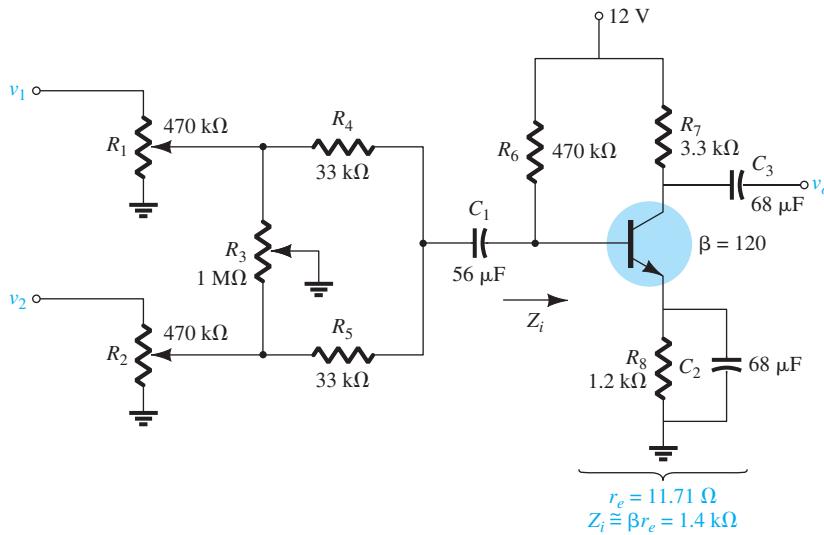


**FIG. 5.129**  
The waveforms resulting from a malfunction in the emitter area.

## 5.25 PRACTICAL APPLICATIONS

### Audio Mixer

When two or more signals are to be combined into a single audio output, mixers such as shown in Fig. 5.130 are employed. The potentiometers at the input are the volume controls for each channel, with potentiometer  $R_3$  included to provide additional balance between



**FIG. 5.130**  
Audio mixer.

the two signals. Resistors  $R_4$  and  $R_5$  are there to ensure that one channel does not load down the other, that is, to ensure that one signal does not appear as a load to the other, draw power, and affect the desired balance on the mixed signal.

The effect of resistors  $R_4$  and  $R_5$  is an important one that should be discussed in some detail. A dc analysis of the transistor configuration results in  $r_e = 11.71 \Omega$ , which will establish an input impedance to the transistor of about  $1.4 \text{ k}\Omega$ . The parallel combination of  $R_6 \parallel Z_i$  is also approximately  $1.4 \text{ k}\Omega$ . Setting both volume controls to their maximum value and the balance control  $R_3$  to its midpoint result in the equivalent network of Fig. 5.131a. The signal at  $v_1$  is assumed to be a low-impedance microphone with an internal resistance of  $1 \text{ k}\Omega$ . The signal at  $v_2$  is assumed to be a guitar amplifier with a higher internal impedance of  $10 \text{ k}\Omega$ . Because the  $470\text{-k}\Omega$  and  $500\text{-k}\Omega$  resistors are in parallel for the above conditions, they can be combined and replaced with a single resistor of about  $242 \text{ k}\Omega$ . Each source will then have an equivalent such as shown in Fig. 5.131b for the microphone. Applying Thévenin's theorem shows that it is an excellent approximation to simply drop the  $242 \text{ k}\Omega$  and assume that the equivalent network is as shown for each channel. The result is the equivalent network of Fig. 5.131c for the input section of the mixer. Applying the superposition theorem results in the following equation for the ac voltage at the base of the transistor:

$$v_b = \frac{(1.4 \text{ k}\Omega \parallel 43 \text{ k}\Omega)v_{s_1}}{34 \text{ k}\Omega + (1.4 \text{ k}\Omega \parallel 43 \text{ k}\Omega)} + \frac{(1.4 \text{ k}\Omega \parallel 34 \text{ k}\Omega)v_{s_2}}{43 \text{ k}\Omega + (1.4 \text{ k}\Omega \parallel 34 \text{ k}\Omega)}$$

$$= 38 \times 10^{-3}v_{s_1} + 30 \times 10^{-3}v_{s_2}$$

With  $r_e = 11.71 \Omega$ , the gain of the amplifier is  $-R_C/r_e = 3.3 \text{ k}\Omega/11.71 \Omega = -281.8$ , and the output voltage is

$$v_o = -10.7v_{s_1} - 8.45v_{s_2}$$

which provides a pretty good balance between the two signals, even though they have a 10:1 ratio in internal impedance. In general, the system will respond quite well. However, if we now remove the  $33\text{-k}\Omega$  resistors from the diagram of Fig. 5.131c, the equivalent network of Fig. 5.132 results, and the following equation for  $v_b$  is obtained using the superposition theorem:

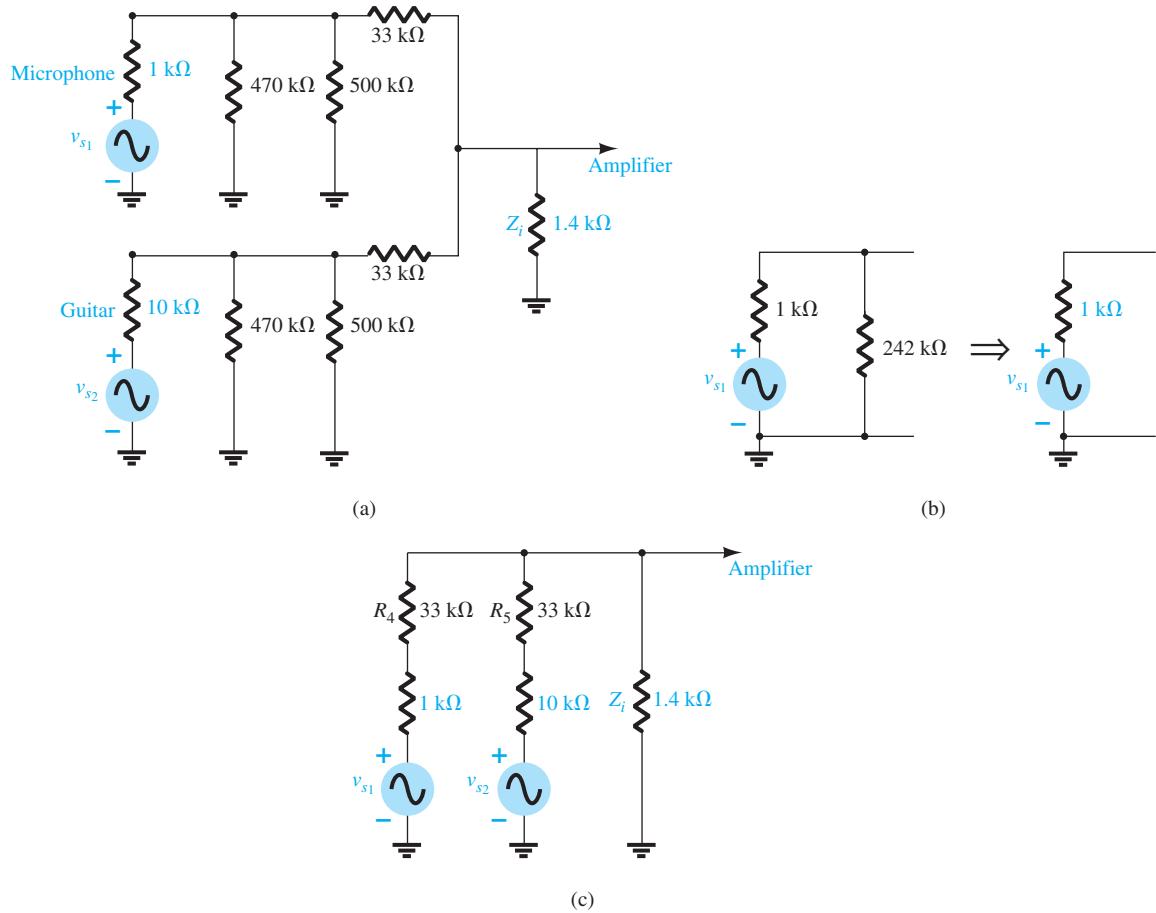
$$v_b = \frac{(1.4 \text{ k}\Omega \parallel 10 \text{ k}\Omega)v_{s_1}}{1 \text{ k}\Omega + 1.4 \text{ k}\Omega \parallel 10 \text{ k}\Omega} + \frac{(1.4 \text{ k}\Omega \parallel 1 \text{ k}\Omega)v_{s_2}}{10 \text{ k}\Omega + (1.4 \text{ k}\Omega \parallel 1 \text{ k}\Omega)}$$

$$= 0.55v_{s_1} + 0.055v_{s_2}$$

Using the same gain as before, we obtain the output voltage as

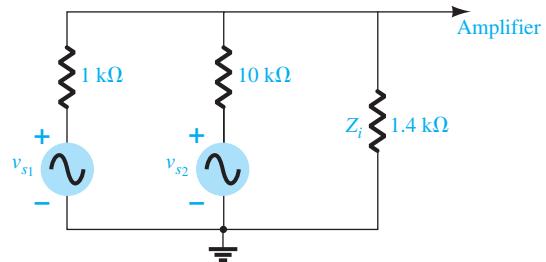
$$v_o = 155v_{s_1} + 15.5v_{s_2} \approx 155v_{s_1}$$

which indicates that the microphone will be quite loud and clear and the guitar input essentially lost.



**FIG. 5.131**

(a) Equivalent network with  $R_3$  set at the midpoint and the volume controls on their maximum settings;  
 (b) finding the Thévenin equivalent for channel 1; (c) substituting the Thévenin equivalent networks into Fig. 5.131a.



**FIG. 5.132**  
 Redrawing the network of Fig. 5.131c with the 33-k $\Omega$  resistors removed.

The importance of the 33-k $\Omega$  resistors is therefore defined. It makes each applied signal appear to have a similar impedance level so that there is good balance at the output. One might suggest that the larger resistor improves the balance. However, even though the balance at the base of the transistor may be better, the strength of the signal at the base of the transistor will be less, and the output level reduced accordingly. In other words, the choice of resistors  $R_4$  and  $R_5$  is a give-and-take situation between the input level at the base of the transistor and the balance of the output signal.

To demonstrate that the capacitors are truly short-circuit equivalents in the audio range, substitute a very low audio frequency of 100 Hz into the reactance equation of a 56- $\mu$ F capacitor:

$$X_C = \frac{1}{2\pi f C} = \frac{1}{2\pi(100 \text{ Hz})(56 \mu\text{F})} = 28.42 \Omega$$

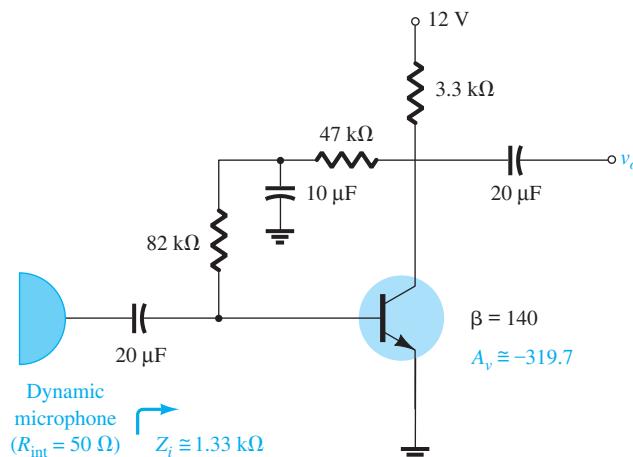
A level of  $28.42 \Omega$  compared to any of the neighboring impedances is certainly small enough to be ignored. Higher frequencies will have even less effect.

A similar mixer will be discussed in connection with the junction field effect transistor (JFET) in the following chapter. The major difference will be the fact that the input impedance of the JFET can be approximated by an open circuit rather than the rather low-level input impedance of the BJT configuration. The result will be a higher signal level at the input to the JFET amplifier. However, the gain of the FET is much less than that of the BJT transistor, resulting in output levels that are actually quite similar.

## Preamplifier

The primary function of a **preamplifier** is as its name implies: **an amplifier used to pick up the signal from its primary source and then operate on it in preparation for its passage into the amplifier section**. Typically, a preamplifier will amplify the signal, control its volume, perhaps change its input impedance characteristics, and if necessary determine its route through the stages to follow—in total, a stage of any system with a multitude of functions.

A preamplifier such as shown in Fig. 5.133 is often used with dynamic microphones to bring the signal level up to levels that are suitable for further amplification or power amplifiers. Typically, dynamic microphones are low-impedance microphones because their internal resistance is determined primarily by the winding of the voice coil. The basic construction consists of a voice coil attached to a small diaphragm that is free to move within a permanent magnet. When one speaks into the microphone, the diaphragm moves accordingly and causes the voice coil to move in the same manner within the magnetic field. In accord with Faraday's law, a voltage will be induced across the coil that will carry the audio signal.



**FIG. 5.133**  
Preamplifier for a dynamic microphone.

Because it is a low-impedance microphone, the input impedance of the transistor amplifier does not have to be that high to pick up most of the signal. Because the internal impedance of a dynamic microphone may be as low as  $20 \Omega$  to  $100 \Omega$ , most of the signal would be picked up with an amplifier having an input impedance as low as  $1$  to  $2 \text{ k}\Omega$ . This, in fact, is the case for the preamplifier of Fig. 5.133. For dc biasing conditions, the collector dc feedback configuration was chosen because of its high stability characteristics.

In the ac domain, the  $10\text{-}\mu\text{F}$  capacitor will assume a short-circuit state (on an approximate basis), placing the  $82\text{-k}\Omega$  resistor across the input impedance of the transistor and the  $47\text{ k}\Omega$  across the output of the transistor. A dc analysis of the transistor configuration results in  $r_e = 9.64 \Omega$ , giving an ac gain determined by

$$A_v = -\frac{(47\text{ k}\Omega \parallel 3.3\text{ k}\Omega)}{9.64 \Omega} = -319.7$$

which is excellent for this application. Of course, the gain will drop when this pickup stage of the design is connected to the input of the amplifier section. That is, the input resistance

of the next stage will appear in parallel with the  $47\text{-k}\Omega$  and  $3.3\text{-k}\Omega$  resistors and will drop the gain below the unloaded level of 319.7.

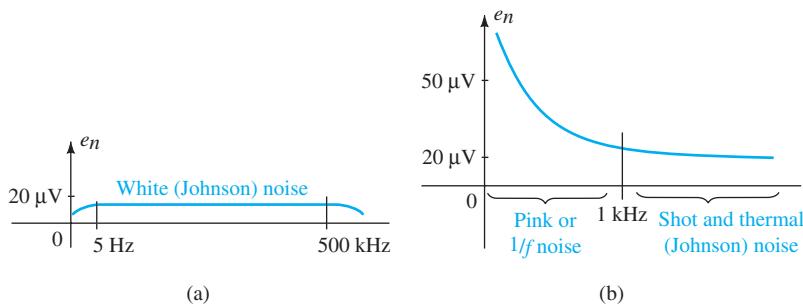
The input impedance of the preamplifier is determined by

$$Z_i = 82 \text{ k}\Omega \parallel \beta r_e = 82 \text{ k}\Omega \parallel (140)(9.64 \Omega) = 82 \text{ k}\Omega \parallel 1.34 \text{ k}\Omega = 1.33 \text{ k}\Omega$$

which is also fine for most low-impedance dynamic microphones. In fact, for a microphone with an internal impedance of  $50 \Omega$ , the signal at the base would be over 98% of that available. This discussion is important because if the impedance of the microphone is a great deal more, say,  $1 \text{k}\Omega$ , the preamplifier would have to be designed differently to ensure that the input impedance was at least  $10 \text{k}\Omega$  or more.

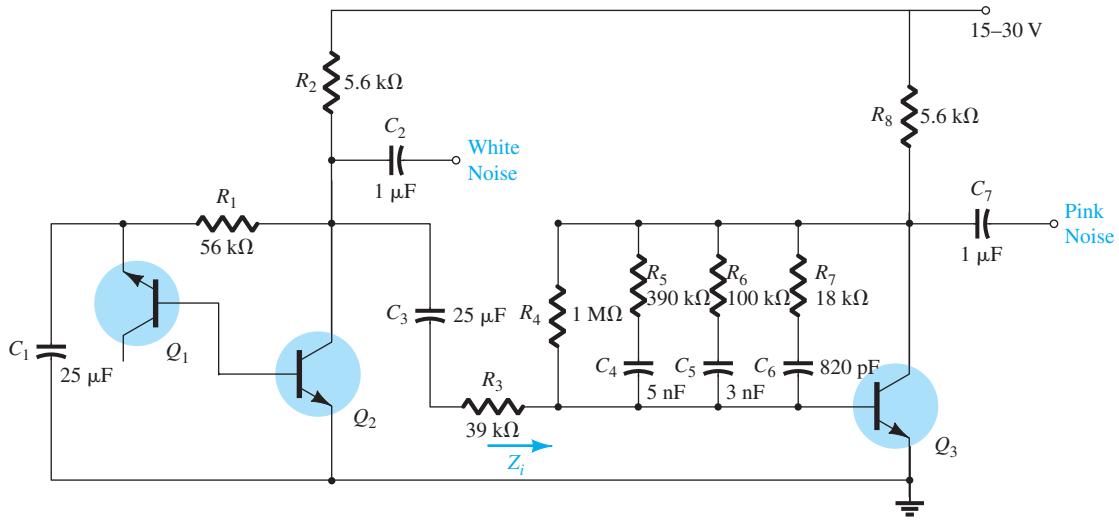
### Random-Noise Generator

There is often a need for a random-noise generator to test the response of a speaker, microphone, filter, and, in fact, any system designed to work over a wide range of frequencies. A **random-noise generator** is just as its name implies: a **generator that generates signals of random amplitude and frequency**. The fact that these signals are usually totally unintelligible and unpredictable is the reason that they are simply referred to as *noise*. **Thermal noise** is noise generated due to thermal effects resulting from the interaction between free electrons and the vibrating ions of a material in conduction. The result is an uneven flow of electrons through the medium, which will result in a varying potential across the medium. In most cases, these randomly generated signals are in the microvolt range, but with sufficient amplification they can wreak havoc on a system's response. This thermal noise is also called **Johnson noise** (named after the original researcher in the area) or **white noise** (because in optics, white light contains all frequencies). This type of noise has a fairly flat frequency response such as shown in Fig. 5.134a, that is, a plot of its power versus frequency from the very low to the very high end is fairly uniform. A second type of noise is called **shot noise**, a name derived from the fact that its noise sounds like a shower of lead shot hitting a solid surface or like heavy rain on a window. Its source is pockets of carriers passing through a medium at uneven rates. A third is **pink, flicker, or  $1/f$  noise**, which is due to the variation in transit times for carriers crossing various junctions of semiconductor devices. It is called  $1/f$  noise because its magnitude drops off with increase in frequency. **Its effect is usually the most dramatic for frequencies below 1 kHz**, as shown in Fig. 5.134b.



**FIG. 5.134**  
Typical noise frequency spectra: (a) white or Johnson; (b) pink, thermal, and shot.

The network of Fig. 5.135 is designed to generate both a white noise and a pink noise. Rather than a separate source for each, first white noise is developed (level across the entire frequency spectrum), and then a filter is applied to remove the mid- and high-frequency components, leaving only the low-frequency noise response. The filter is further designed to modify the flat response of the white noise in the low-frequency region (to create a  $1/f$  drop-off) by having sections of the filter “drop in” as the frequency increases. The white noise is created by leaving the collector terminal of transistor  $Q_1$  open and reverse-biasing the base-to-emitter junction. In essence, the transistor is being used as a diode biased in the Zener avalanche region. Biasing a transistor in this region creates a very unstable situation that is conducive to the generation of random white noise. The combination of the avalanche region with its rapidly changing charge levels, sensitivity of the current level to

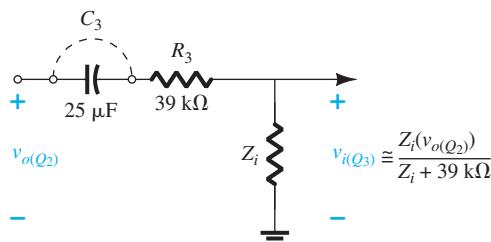


**FIG. 5.135**  
White- and pink-noise generator.

temperature, and quickly changing impedance levels contributes to the level of noise voltage and current generated by the transistor. Germanium transistors are often used because the avalanche region is less defined and less stable than in silicon transistors. In addition, there are diodes and transistors designed specifically for random-noise generation.

The source of the noise is not some specially designed generator. It is simply due to the fact that current flow is not an ideal phenomenon but actually varies with time at a level that generates unwanted variations in the terminal voltage across elements. In fact, that variation in flow is so broad that it can generate frequencies that extend across a wide spectrum—a very interesting phenomenon.

The generated noise current of  $Q_1$  will then be the base current for  $Q_2$ , which will be amplified to generate a white noise of perhaps 100 mV, which for this design would suggest an input noise voltage of about 170  $\mu$ V. Capacitor  $C_1$  will have a low impedance throughout the frequency range of interest to provide a “shorting effect” on any spurious signals in the air from contributing to the signal at the base of  $Q_1$ . The capacitor  $C_2$  is there to isolate the dc biasing of the white-noise generator from the dc levels of the filter network to follow. The 39 k $\Omega$  and the input impedance of the next stage create the simple voltage-divider network of Fig. 5.136. If the 39 k $\Omega$  were not present, the parallel combination of  $R_2$  and  $Z_i$  would load down the first stage and reduce the gain of  $Q_1$  considerably. In the gain equation,  $R_2$  and  $Z_i$  would appear in parallel (discussed in Chapter 9).



**FIG. 5.136**  
Input circuit for the second stage.

The filter network is actually part of the feedback loop from collector to base appearing in the collector feedback network of Section 5.10. To describe its behavior, let us first consider the extremes of the frequency spectrum. For very low frequencies all the capacitors can be approximated by an open circuit, and the only resistance from collector to base is the 1-M $\Omega$  resistor. Using a beta of 100, we find that the gain of the section is about 280 and the input impedance about 1.28 k $\Omega$ . At a sufficiently high frequency all the capacitors

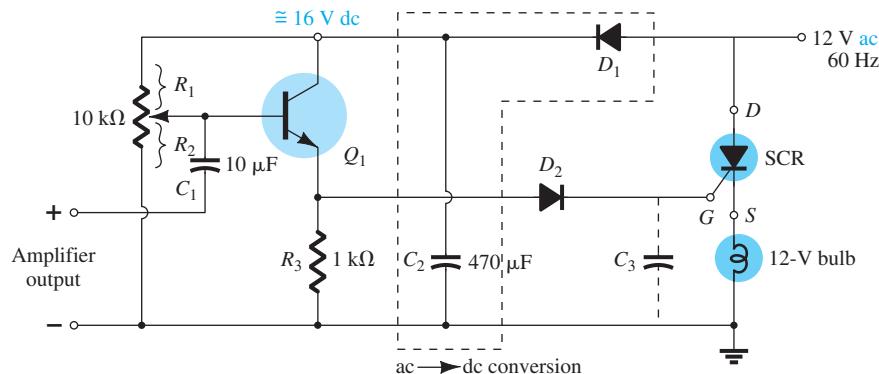
could be replaced by short circuits, and the total resistance combination between collector and base would be reduced to about  $14.5\text{ k}\Omega$ , which would result in a very high unloaded gain of about 731, more than twice that just obtained with  $R_F = 1\text{ M}\Omega$ . Because the  $1/f$  filter is supposed to reduce the gain at high frequencies, it initially appears as though there is an error in design. However, the input impedance has dropped to about  $19.33\text{ }\Omega$ , which is a 66-fold drop from the level obtained with  $R_F = 1\text{ M}\Omega$ . This would have a significant impact on the input voltage appearing at the second stage when we consider the voltage-divider action of Fig. 5.136. In fact, when compared to the series  $39\text{-k}\Omega$  resistor, the signal at the second stage can be assumed to be negligible or at a level where even a gain in excess of 700 cannot raise it to a level of any consequence. In total, therefore, the effect of doubling the gain is totally lost due to the tremendous drop in  $Z_i$ , and the output at very high frequencies can be ignored entirely.

For the range of frequencies between the very low and the very high, the three capacitors of the filter will cause the gain to drop off with increase in frequency. First, capacitor  $C_4$  will be dropped in and cause a reduction in gain (around 100 Hz). Then capacitor  $C_5$  will be included and will place the three branches in parallel (around 500 Hz). Finally, capacitor  $C_6$  will result in four parallel branches and the minimum feedback resistance (around 6 kHz).

The result is a network with an excellent random-noise signal for the full frequency spectrum (white) and the low-frequency spectrum (pink).

### Sound-Modulated Light Source

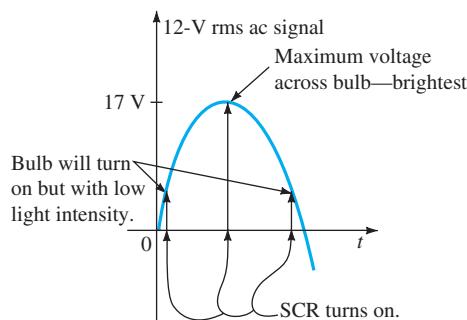
The light from the 12-V bulb of Fig. 5.137 will vary at a frequency and an intensity that are sensitive to the applied signal. The applied signal may be the output of an acoustical amplifier, a musical instrument, or even a microphone. Of particular interest is the fact that the applied voltage is 12 V ac rather than the typical dc biasing supply. The immediate question, in the absence of a dc supply, is how the dc biasing levels for the transistor will be established. In actuality, the dc level is obtained through the use of diode  $D_1$ , which rectifies the ac signal, and capacitor  $C_2$ , which acts as a power supply filter to generate a dc level across the output branch of the transistor. The peak value of a 12-V rms supply is about 17 V, resulting in a dc level after the capacitive filtering in the neighborhood of 16 V. If the potentiometer is set so that  $R_1$  is about  $320\text{ }\Omega$ , the voltage from base to emitter of the transistor will be about 0.5 V, and the transistor will be in the “off” state. In this state the collector and emitter currents are essentially 0 mA, and the voltage across resistor  $R_3$  is approximately 0 V. The voltage at the junction of the collector terminal and the diode is therefore 0 V, resulting in  $D_2$  being in the “off” state and 0 V at the gate terminal of the silicon-controlled rectifier (SCR). The SCR (see Section 17.3) is fundamentally a diode whose state is controlled by an applied voltage at the gate terminal. The absence of a voltage at the gate means that the SCR and bulb are off.



**FIG. 5.137**  
Sound-modulated light source. SCR, Silicon-controlled rectifier.

If a signal is now applied to the gate terminal, the combination of the established biasing level and the applied signal can establish the required 0.7-V turn-on voltage, and the transistor will be turned on for periods of time dependent on the applied signal. When the

transistor turns on, it will establish a collector current through resistor  $R_3$  that will establish a voltage from collector to ground. If the voltage is more than the required 0.7 V for diode  $D_2$ , a voltage will appear at the gate of the SCR that may be sufficient to turn it on and establish conduction from the drain to the source of the SCR. However, we must now examine one of the most interesting aspects of this design. Because the applied voltage across the SCR is ac, which will vary in magnitude with time as shown in Fig. 5.138, the conduction strength of the SCR will vary with time also. As shown in the figure, if the SCR is turned on when the sinusoidal voltage is a maximum, the resulting current through the SCR will be a maximum also, and the bulb will be its brightest. If the SCR should turn on when the sinusoidal voltage is near its minimum, the bulb may turn on, but the lower current will result in considerably less illumination. The result is that the lightbulb turns on in sync with when the input signal is peaking, but the strength of turn-on will be determined by where one is on the applied 12-V signal. One can imagine the interesting and varied responses of such a system. Each time one applies the same audio signal, the response will have a different character.



**FIG. 5.138**

*Demonstrating the effect of an ac voltage on the operation of the SCR of Fig. 5.137.*

In the above action, the potentiometer was set below the turn-on voltage of the transistor. The potentiometer can also be adjusted so that the transistor is “just on,” resulting in a low-level base current. The result is a low-level collector current and insufficient voltage to forward-bias diode  $D_2$  and turn on the SCR at the gate. However, when the system is set up in this manner, the resultant light output will be more sensitive to lower amplitude components of the applied signal. In the first case, the system acts more like a peak detector, whereas in the latter case it is sensitive to more components of the signal.

Diode  $D_2$  was included to be sure that there is sufficient voltage to turn on both the diode and the SCR, in other words, to eliminate the possibility of noise or some other low-level unexpected voltage on the line turning the SCR on. Capacitor  $C_3$  can be inserted to slow down the response by ensuring the voltage charge across the capacitor before the gate will reach sufficient voltage to turn on the SCR.

## 5.26 SUMMARY

### Important Conclusions and Concepts

1. Amplification in the ac domain cannot be obtained **without the application of dc biasing level**.
2. For most applications the BJT amplifier can be considered linear, permitting the use of the **superposition theorem** to separate the dc and ac analyses and designs.
3. When introducing the **ac model** for a BJT:
  - a. All **dc sources are set to zero** and replaced by a short-circuit connection to ground.
  - b. All **capacitors** are replaced by a **short-circuit equivalent**.
  - c. All elements **in parallel with** an introduced short-circuit equivalent should be removed from the network.
  - d. The network should be **redrawn** as often as possible.
4. The **input impedance** of an ac network **cannot be measured** with an ohmmeter.

5. The **output impedance** of an amplifier is measured with the **applied signal set to zero**. It cannot be measured with an ohmmeter.
6. The **output impedance** for the  $r_e$  model **can be included** only if obtained from a data sheet or from a graphical measurement from the characteristic curves.
7. Elements that were isolated by capacitors for the dc analysis **will appear in the ac analysis** due to the short-circuit equivalent for the capacitive elements.
8. The **amplification factor** ( $\beta$ , or  $h_{fe}$ ) is the least sensitive to changes **in collector current**, whereas the **output impedance** parameter is the most sensitive. The output impedance is also quite sensitive to changes in  $V_{CE}$ , whereas the **amplification** factor is the **least sensitive**. However, the **output impedance** is the **least sensitive** to changes in **temperature**, whereas the amplification factor is somewhat sensitive.
9. The  $r_e$  **model** for a BJT in the ac domain is sensitive to the **actual dc operating conditions of the network**. This parameter is normally not provided on a specification sheet, although  $h_{ie}$  of the normally provided hybrid parameters is equal to  $\beta r_e$ , but only under specific operating conditions.
10. Most **specification sheets** for BJTs include a **list of hybrid parameters** to establish an ac model for the transistor. One must be aware, however, that they are provided for a particular set of dc operating conditions.
11. The **CE fixed-bias configuration** can have a **significant voltage gain** characteristic, although its **input impedance can be relatively low**. The approximate **current gain** is given by simply **beta**, and the **output impedance** is normally assumed to be  **$R_C$** .
12. The **voltage-divider bias configuration** has a **higher stability** than the fixed-bias configuration, but it has about the **same voltage gain, current gain, and output impedance**. Due to the biasing resistors, its input impedance may be lower than that of the fixed-bias configuration.
13. The **CE emitter-bias configuration** with an unbypassed emitter resistor has a **larger input resistance** than the bypassed configuration, but it will have a **much smaller voltage gain** than the bypassed configuration. For the unbypassed or bypassed situation, the **output impedance** is normally assumed to be simply  **$R_C$** .
14. The **emitter-follower configuration** will always have an **output voltage slightly less than the input signal**. However, the **input impedance** can be **very large**, making it very useful for situations where a high-input first stage is needed to “pick up” as much of the applied signal as possible. Its **output impedance** is **extremely low**, making it an excellent signal source for the second stage of a multistage amplifier.
15. The **common-base configuration** has a **very low input impedance**, but it can have a **significant voltage gain**. The **current gain** is just **less than 1**, and the **output impedance** is simply  **$R_C$** .
16. The **collector feedback configuration** has an **input impedance** that is **sensitive to beta** and that can be quite low depending on the parameters of the configuration. However, the **voltage gain** can be **significant** and the **current gain of some magnitude** if the parameters are chosen properly. The **output impedance** is most often simply the collector resistance  **$R_C$** .
17. The **collector dc feedback configuration** uses the dc feedback to **increase its stability** and the changing state of a capacitor from dc to ac to establish a **higher voltage gain** than obtained with a straight feedback connection. The **output impedance** is usually close to  **$R_C$**  and the **input impedance** relatively close to that obtained with the **basic common-emitter configuration**.
18. The **approximate hybrid equivalent network** is very **similar** in composition to that used with the  $r_e$  **model**. In fact, the **same methods** of analysis can be applied to both models. For the hybrid model the results will be in terms of the network parameters and the hybrid parameters, whereas for the  $r_e$  model they will be in terms of the network parameters and  $\beta$ ,  $r_e$ , and  $r_o$ .
19. The **hybrid model** for common-emitter, common-base, and common-collector configurations **is the same**. The only difference will be the magnitude of the parameters of the equivalent network.
20. The total gain of a cascaded system is determined by the **product of the gains of each stage**. The gain of each stage, however, must be determined **under loaded conditions**.
21. Because the total gain is the product of the individual gains of a cascaded system, the **weakest link** can have a major effect on the total gain.

## Equations

$$r_e = \frac{26 \text{ mV}}{I_E}$$

Hybrid parameters:

$$h_{ie} = \beta r_e, \quad h_{fe} = \beta_{ac}, \quad h_{ib} = r_e, \quad h_{fb} = -\alpha \cong -1$$

CE fixed bias:

$$Z_i \cong \beta r_e, \quad Z_o \cong R_C$$

$$A_v = -\frac{R_C}{r_e}, \quad A_i = -A_v \frac{Z_i}{R_C} \cong \beta$$

Voltage-divider bias:

$$Z_i = R_1 \| R_2 \| \beta r_e, \quad Z_o \cong R_C$$

$$A_v = -\frac{R_C}{r_e}, \quad A_i = -A_v \frac{Z_i}{R_C} \cong \beta$$

CE emitter-bias:

$$Z_i \cong R_B \| \beta R_E, \quad Z_o \cong R_C$$

$$A_v \cong -\frac{R_C}{R_E}, \quad A_i \cong \frac{\beta R_B}{R_B + \beta R_E}$$

Emitter-follower:

$$Z_i \cong R_B \| \beta R_E, \quad Z_o \cong r_e$$

$$A_v \cong 1, \quad A_i = -A_v \frac{Z_i}{R_E}$$

Common-base:

$$Z_i \cong R_E \| r_e, \quad Z_o \cong R_C$$

$$A_v \cong \frac{R_C}{r_e}, \quad A_i \cong -1$$

Collector feedback:

$$Z_i \cong \frac{r_e}{\frac{1}{\beta} + \frac{R_C}{R_F}}, \quad Z_o \cong R_C \| R_F$$

$$A_v = -\frac{R_C}{r_e}, \quad A_i \cong \frac{R_F}{R_C}$$

Collector dc feedback:

$$Z_i \cong R_{F_1} \| \beta r_e, \quad Z_o \cong R_C \| R_{F_2}$$

$$A_v = -\frac{R_{F_2} \| R_C}{r_e}, \quad A_i = -A_v \frac{Z_i}{R_C}$$

Effect of load impedance:

$$A_{v_L} = \frac{V_o}{V_i} = \frac{R_L}{R_L + R_o} A_{v_{NL}}, \quad A_{i_L} = \frac{I_o}{I_i} = -A_{v_L} \frac{Z_i}{R_L}$$

Effect of source impedance:

$$V_i = \frac{R_i V_s}{R_i + R_s}, \quad A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} A_{v_{NL}}$$

$$I_s = \frac{V_s}{R_s + R_i}$$

Combined effect of load and source impedance:

$$A_{v_L} = \frac{V_o}{V_i} = \frac{R_L}{R_L + R_o} A_{v_{NL}}, \quad A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} \cdot \frac{R_L}{R_L + R_o} A_{v_{NL}}$$

$$A_{i_L} = \frac{I_o}{I_i} = -A_{v_L} \frac{R_i}{R_L}, \quad A_{i_s} = \frac{I_o}{I_s} = -A_{v_s} \frac{R_s + R_i}{R_L}$$

Cascode connection:

$$A_v = A_{v_1}A_{v_2}$$

Darlington connection (with  $R_E$ ):

$$\beta_D = \beta_1\beta_2,$$

$$Z_i = R_B \| (\beta_1\beta_2 R_E), \quad A_i = \frac{\beta_1\beta_2 R_B}{(R_B + \beta_1\beta_2 R_E)}$$

$$Z_o = \frac{r_{e_1}}{\beta_2} + r_{e_2} \quad A_v = \frac{V_o}{V_i} \approx 1$$

Darlington connection (without  $R_E$ ):

$$Z_i = R_1 \| R_2 \| \beta_1(r_{e_1} + \beta_1\beta_2 r_{e_2}) \quad A_i = \frac{\beta_1\beta_2(R_1 \| R_2)}{R_1 \| R_2 + Z'_i}$$

$$\text{where } Z'_i = \beta_1(r_{e_1} + \beta_2 r_{e_2})$$

$$Z_o \cong R_C \| r_{o_2} \quad A_v = \frac{V_o}{V_i} = \frac{\beta_1\beta_2 R_C}{Z'_i}$$

Feedback pair:

$$Z_i = R_B \| \beta_1\beta_2 R_C \quad A_i = \frac{-\beta_1\beta_2 R_B}{R_B + \beta_1\beta_2 R_C}$$

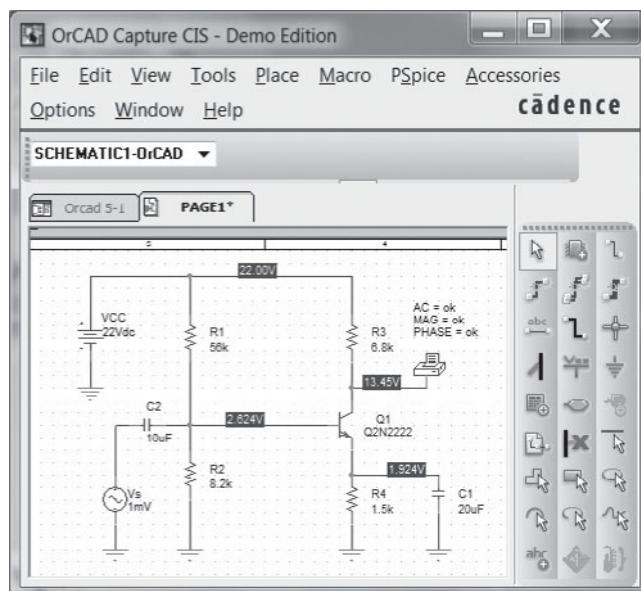
$$Z_o \approx \frac{r_{e_1}}{\beta_2} \quad A_v \cong 1$$

## 5.27 COMPUTER ANALYSIS

### PSpice Windows

**BJT Voltage-Divider Configuration** The last few chapters have been limited to the dc analysis of electronic networks using PSpice and Multisim. This section will consider the application of an ac source to a BJT network and describe how the results are obtained and interpreted.

Most of the construction of the network of Fig. 5.139 can be accomplished using the procedures introduced in earlier chapters. The ac source can be found in the **SOURCE** library as **VSIN**. You can scroll down the list of options or simply type in **VSIN** at the head of the listing. Once this is selected and placed, a number of labels will appear that define



**FIG. 5.139**  
Using PSpice Windows to analyze the network of Fig. 5.28  
(Example 5.2).

the parameters of the source. Double-clicking the source symbol or using the sequence **Edit-Properties** will result in the **Property Editor** dialog box, which lists all the parameters appearing on the screen and more. By scrolling all the way to the left, you will find a listing for **AC**. Select the blank rectangle under the heading and enter the **1 mV** value. Be aware that the entries can use prefixes such as m (milli) and k (kilo). Moving to the right, the heading **FREQ** will appear, in which you can enter **10 kHz**. Moving again to **PHASE**, you will find the default value is **0**, so it can be left alone. It represents the initial phase angle for the sinusoidal signal. Next you will find **VAMPL**, which is set at 1 mV, also followed by **VOFF** at **0 V**. Now that each of the properties has been set, we have to decide what to display on the screen to define the source. In Fig. 5.139 the only labels are **Vs** and **1 mV**, so a number of items have to be deleted and the name of the source has to be modified. For each quantity simply return to the heading and select it for modification. If you choose **AC**, select **Display** to obtain the **Display Properties** dialog box. Select **Value Only** because we prefer not to have the label **AC** appear. Leave all the other choices blank. An **OK**, and you can move to the other parameters within the **Property Editor** dialog box. We do not want the **FREQ**, **PHASE**, **VAMPL** and **VOFF** labels to appear with their values, so in each case select **Do Not Display**. To change **V1** to **Vs**, simply go to the **Part Reference**, and after selecting it, type in **Vs**. Then go to **Display** and select **Value Only**. Finally, to apply all the changes, select **Apply** and exit the dialog box; the source will appear as shown in Fig. 5.139.

The ac response for the voltage at a point in the network is obtained using the **VPRINT1** option found in the **SPECIAL** library. If the library does not appear, simply select **Add Library** followed by **special.olb**. When **VPRINT1** is chosen, it will appear on the screen as a printer with three labels: **AC**, **MAG**, and **PHASE**. Each has to be set to an **OK** status to reflect the fact that you desire this type of information about the voltage level. This is accomplished by simply clicking on the printer symbol to obtain the dialog box and setting each to **OK**. For each entry select **Display** and choose **Name and Label**. Finally, select **Apply** and exit the dialog box. The result appears in Fig. 5.139.

The transistor **Q2N2222** can be found under the **EVAL** library by typing it under the **Part** heading or simply scrolling through the possibilities. The levels of  $I_s$  and  $\beta$  can be set by first selecting the **Q2N2222** transistor to make it red and then applying the sequence **Edit-PSpice Model** to obtain the **PSpice Model Editor Lite** dialog box and changing **Is** to **2E-15A** and **Bf** to **90**. The level of **Is** is the result of numerous runs of the network to find the value that would result in  $V_{BE}$  being closest to **0.7 V**.

Now that all the components of the network have been set, it is time to ask the computer to analyze the network and provide some results. If improper entries were made, the computer will quickly respond with an error listing. First select the **New Simulation Profile** key to obtain the **New Simulation** dialog box. Then, after entering **Name** as **OrCAD 5-1**, select **Create** and the **Simulation Settings** dialog box will appear. Under **Analysis type**, select **AC Sweep/Noise** and then under **AC Sweep Type** choose **Linear**. The **Start Frequency** is **10 kHz**, the **End Frequency** is **10 kHz**, and the **Total Points** is **1**. An **OK**, and the simulation can be initiated by selecting the **Run PSpice** key (white arrow). A schematic will result with a graph that extends from 5 kHz to 15 kHz with no vertical scale. Through the sequence **View-Output File** the listing of Fig. 5.140 can be obtained. It starts with a list of all the elements of the network and their settings followed by all the parameters of the transistor. In particular, note the level of **IS** and **BF**. Next the dc levels are provided under the **SMALL SIGNAL BIAS SOLUTION**, which match those appearing on the schematic of Fig. 5.139. The dc levels appear on Fig. 5.139 due to the selection of the **V** option. Also note that  $V_{BE} = 2.624 \text{ V} - 1.924 \text{ V} = 0.7 \text{ V}$ , as stated above, due to the choice of **Is**.

The next listing, **OPERATING POINT INFORMATION**, reveals that even though beta of the **BJT MODEL PARAMETERS** listing was set at 90, the operating conditions of the network resulted in a dc beta of 48.3 and an ac beta of 55. Fortunately, however, the voltage-divider configuration is less sensitive to changes in beta in the dc mode, and the dc results are excellent. However, the drop in ac beta had an effect on the resulting level of  $V_o$ : 296.1 mV versus the handwritten solution (with  $r_o = 50 \text{ k}\Omega$ ) of 324.3 mV—a 9% difference. The results are certainly close, but probably not as close as one would like. A closer result (within 7%) could be obtained by setting all the parameters of the device except  $I_s$  and beta to zero. However, for the moment, the impact of the remaining parameters has been demonstrated, and the results will be accepted as sufficiently close to the handwritten levels. Later in this chapter, an ac model for the transistor will be introduced with results

```

***** CIRCUIT DESCRIPTION
*****
* Analysis directives:
.AC LIN 1 10kHz 10kHz
.OP
.PROBE V(alias(*)) I(alias(*)) W(alias(*)) D(alias(*)) NOISE(alias(*))
INC ".ASCHMATIC1.net"
* source ORCAD 5.1
Q_Q1 N00286 N00282 N00319 Q2N2222
R_R1 N00282 N00254 56k TC=0.0
R_R2 0 N00282 8.2k TC=0.0
R_R3 N00286 N00254 6.8k TC=0.0
R_R4 0 N00319 1.5k TC=0.0
V_VCC N00254 0 22Vdc
C_C1 0 N00319 200pF TC=0.0
V_Vs N00342 0 AC 1mV
+SIN 0V 1mV 10kHz 0 0 0
.PRINT AC
+ VM (N00286)
+ VP (N00286)
C_C2 N00342 N00282 10uF TC=0.0
.END

***** BJT MODEL PARAMETERS
*****
          Q2N2222
          NPN
LEVEL 1
IS 2.000000E-15
BF 90
NF 1
VAF 74.03
IKF .2847
ISE 14.340000E-15
NE 1.307
BR 6.092
NR 1
ISS 0
RB 10
RE 0
RC 1
CJE 22.010000E-12
VJE .75
MJE .377
CJC 7.306000E-12
VJC .75
MJC .3416
XCJC 1
CJS 0
VJS .75
TF 411.100000E-12
XTF 3
VTF 1.7
ITF .6
TR 46.910000E-09
XTB 1.5
KF 0
AF 1
CN 2.42
D .87

***** SMALL SIGNAL BIAS SOLUTION
TEMPERATURE = 27.000 DEG C
*****
NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE
(N00254) 22.0000 (N00282) 2.6239 (N00286) 13.4530 (N00319) 1.9244
(N00342) 0.0000

VOLTAGE SOURCE CURRENTS
NAME CURRENT
V_VCC -1.603E-03
V_Vs 0.0000E+00

TOTAL POWER DISSIPATION 3.53E-02 WATTS

***** OPERATING POINT INFORMATION
TEMPERATURE = 27.000 DEG C
*****
***** BIPOLAR JUNCTION TRANSISTORS
*****
NAME Q_Q1
MODEL Q2N2222
IB 2.60E-05
IC 1.26E-03
VBE 6.99E-01
VBC -1.08E+01
VCE 1.15E+01
BETADC 4.83E+01
GM 4.84E+02
RPI 1.14E+03
RX 1.00E+01
RO 6.75E+04
CBE 5.75E-11
CBC 2.87E-12
CIS 0.00E+00
BETAAC 5.50E+01
CBX/CBX2 0.00E+00
FT/FT2 1.27E+08

***** AC ANALYSIS
TEMPERATURE = 27.000 DEG C
*****
FREQ VM(N00286) VP(N00286)
1.000E+04 2.961E-01 -1.780E+02

```

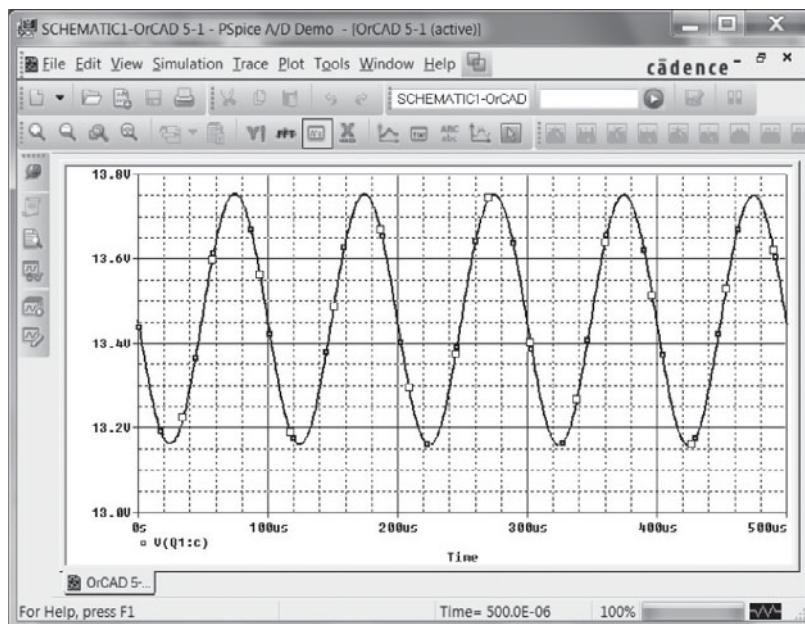
**FIG. 5.140**  
Output file for the network of Fig. 5.139.

that will be an exact match with the handwritten solution. The phase angle is  $-178^\circ$  versus the ideal of  $-180^\circ$ , a very close match.

A plot of the voltage at the collector of the transistor can be obtained by setting up a new simulation process to calculate the value of the desired voltage at a number of data points. The more points, the more accurate is the plot. The process is initiated by returning to the

**Simulation Settings** dialog box and under **Analysis type** selecting **Time Domain(Transient)**. Time domain is chosen because the horizontal axis will be a time axis, requiring that the collector voltage be determined at a specified time interval to permit the plot. Because the period of the waveform is  $1/10 \text{ kHz} = 0.1 \text{ ms} = 100 \mu\text{s}$ , and it would be convenient to display five cycles of the waveform, the **Run to time(TSTOP)** is set at  $500 \mu\text{s}$ . The **Start saving data after** point is left at 0 s and under **Transient option**, the **Maximum step size** is set at  $1 \mu\text{s}$  to ensure 100 data points for each cycle of the waveform. An **OK**, and a **SCHEMATIC** window will appear with a horizontal axis broken down in units of time but with no vertical axis defined. The desired waveform can then be added by first selecting **Trace** followed by **Add Trace** to obtain the **Add Trace** dialog box. In the provided listing **V(Q1:c)** is selected as the voltage at the collector of the transistor. The instant it is selected it will appear as the **Trace Expression** at the bottom of the dialog box. Referring to Fig. 5.139, we find that because the capacitor  $C_E$  will essentially be in the short-circuit state at 10 kHz, the voltage from collector to ground is the same as that across the output terminals of the transistor. An **OK**, and the simulation can be initiated by selecting the **Run PSpice** key.

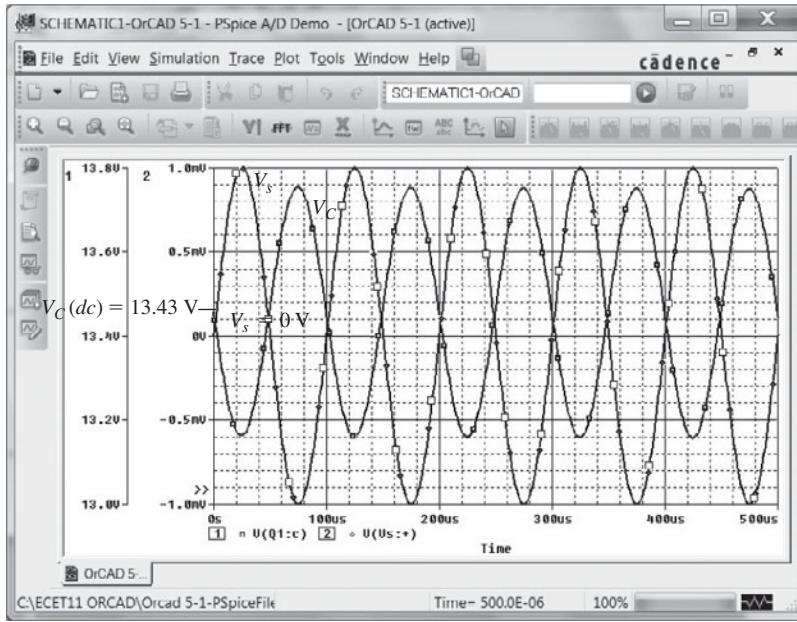
The result will be the waveform of Fig. 5.141 having an average value of about 13.45 V, which corresponds exactly with the bias level of the collector voltage in Fig. 5.139. The range of the vertical axis was chosen automatically by the computer. Five full cycles of the output voltage are displayed with 100 data points for each cycle. The data points appear in Fig. 5.139 because the sequence **Tools-Options-Mark Data Points** was applied. The data points appear as small dark circles on the plot curve. Using the scale of the graph, we see that the peak-to-peak value of the curve is approximately  $13.76 \text{ V} - 13.16 \text{ V} = 0.6 \text{ V} = 600 \text{ mV}$ , resulting in a peak value of 300 mV. Because a 1-mV signal was applied, the gain is 300, or very close to the calculator solution of 296.1.



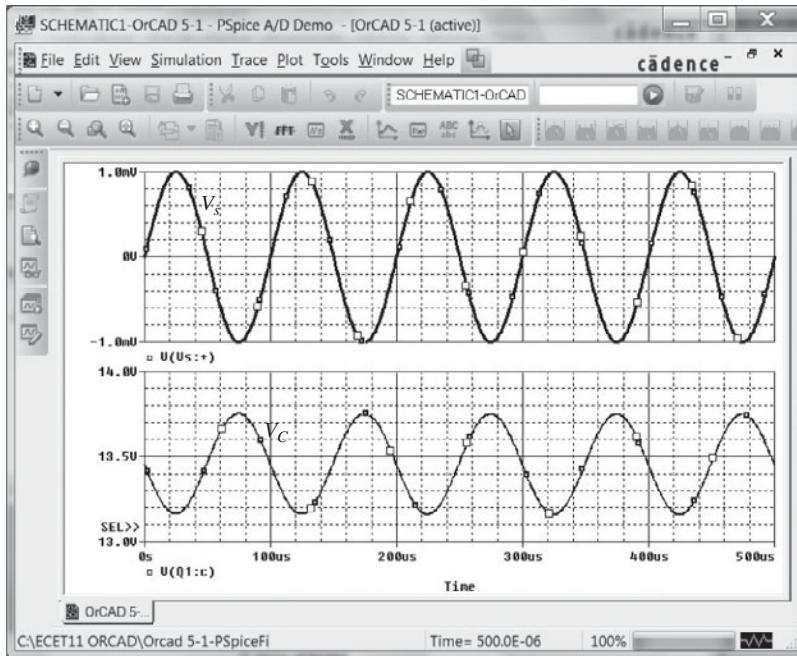
**FIG. 5.141**  
Voltage  $v_C$  for the network Fig. 5.139.

If a comparison is to be made between the input and output voltages on the same screen, the **Add Y-Axis** option under **Plot** can be used. After you select it, choose the **Add Trace** icon and select **V(Vs:+)** from the provided list. The result is that both waveforms will appear on the same screen as shown in Fig. 5.142, each with its own vertical scale.

If two separate graphs are preferred, we can start by selecting **Plot** followed by **Add Plot to Window** after the graph of Fig. 5.141 is in place. The result will be a second set of axes waiting for a decision about which curve to plot. Using **Trace-Add Trace-V(Vs:+)** will result in the graphs of Fig. 5.143. The **SEL >>** (from **SELECT**) appearing next to one of the plots defines the “active” plot.



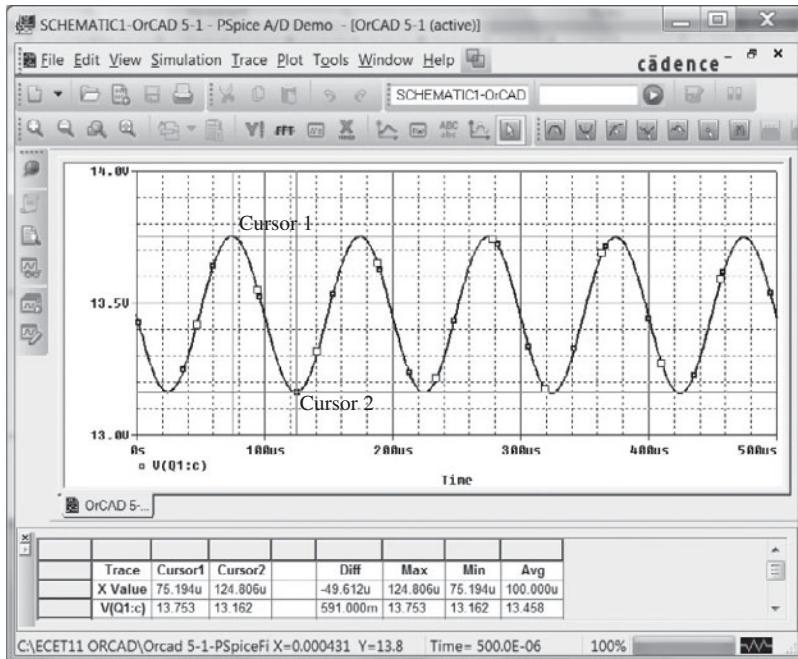
**FIG. 5.142**  
The voltages  $v_C$  and  $v_s$  for the network of Fig. 5.139.



**FIG. 5.143**  
Two separate plots of  $v_C$  and  $v_s$  in Fig. 5.139.

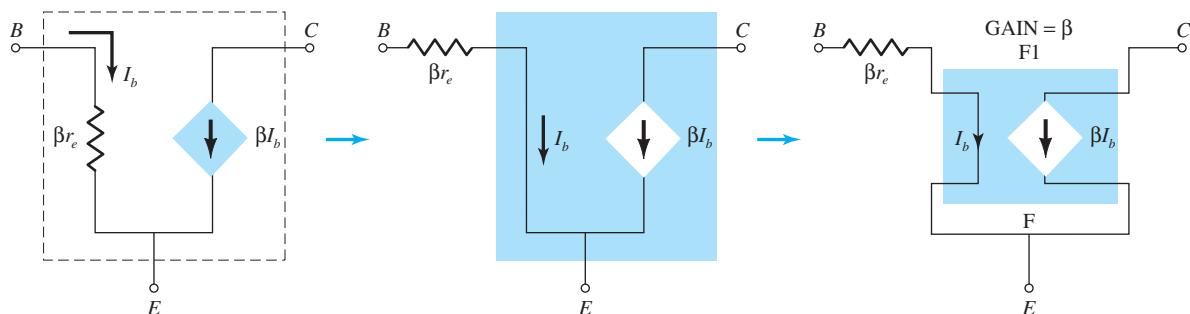
The last operation to be introduced in this coverage of graph displays is the use of the cursor option. The result of the sequence **Trace-Cursor-Display** is a line at the dc level of the graph of Fig. 5.144 intersecting with a vertical line. The level and time both appear in the small dialog box in the bottom right corner of the screen. The first number for **Cursor 1** is the time intersection and the second is the voltage level at that instant. A left-click of the mouse will provide control of the intersecting vertical and horizontal lines at this level. Clicking on the vertical line and holding down on the clicker will allow you to move the intersection horizontally along the curve, simultaneously displaying the time and

voltage level in the data box at the bottom right of the screen. If it is moved to the first peak of the waveform, the time appears as  $75.194 \mu s$  with a voltage level of 13.753 V, as shown in Fig. 5.144. On right-clicking of the mouse, a second intersection, defined by **Cursor 2**, will appear, which can be moved in the same way with its time and voltage appearing in the same dialog box. Note that if **Cursor 2** is placed close to the negative peak, the difference in time is  $49.61 \mu s$  (as displayed in the same box), which is very close to one-half the period of the waveform. The difference in magnitude is 591 mV, which is very close to the 600 mV obtained earlier.



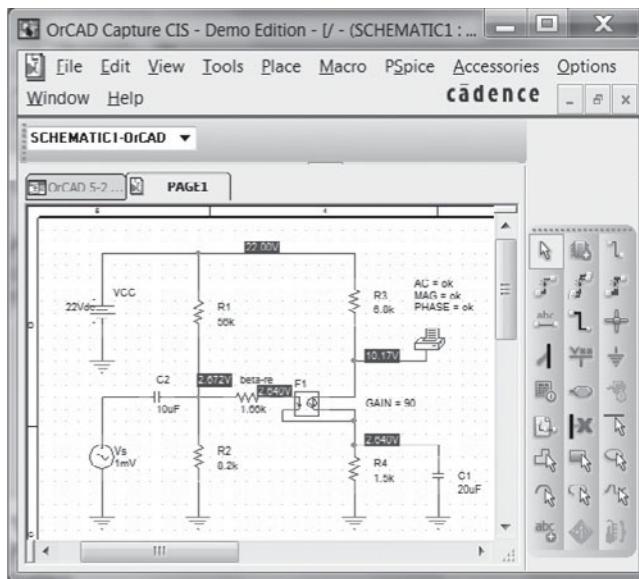
**FIG. 5.144**  
Demonstrating the use of cursors to read specific points on a plot.

**Voltage-Divider Configuration—Controlled Source Substitution** The results obtained for any analysis using the transistors provided in the PSpice listing will always be somewhat different from those obtained with an equivalent model that only includes the effect of beta and  $r_e$ . This was clearly demonstrated for the network of Fig. 5.139. If a solution is desired that is limited to the approximate model used in the hand calculations, then the transistor must be represented by a model such as appearing in Fig. 5.145.



**FIG. 5.145**  
Using a controlled source to represent the transistor of Fig. 5.139.

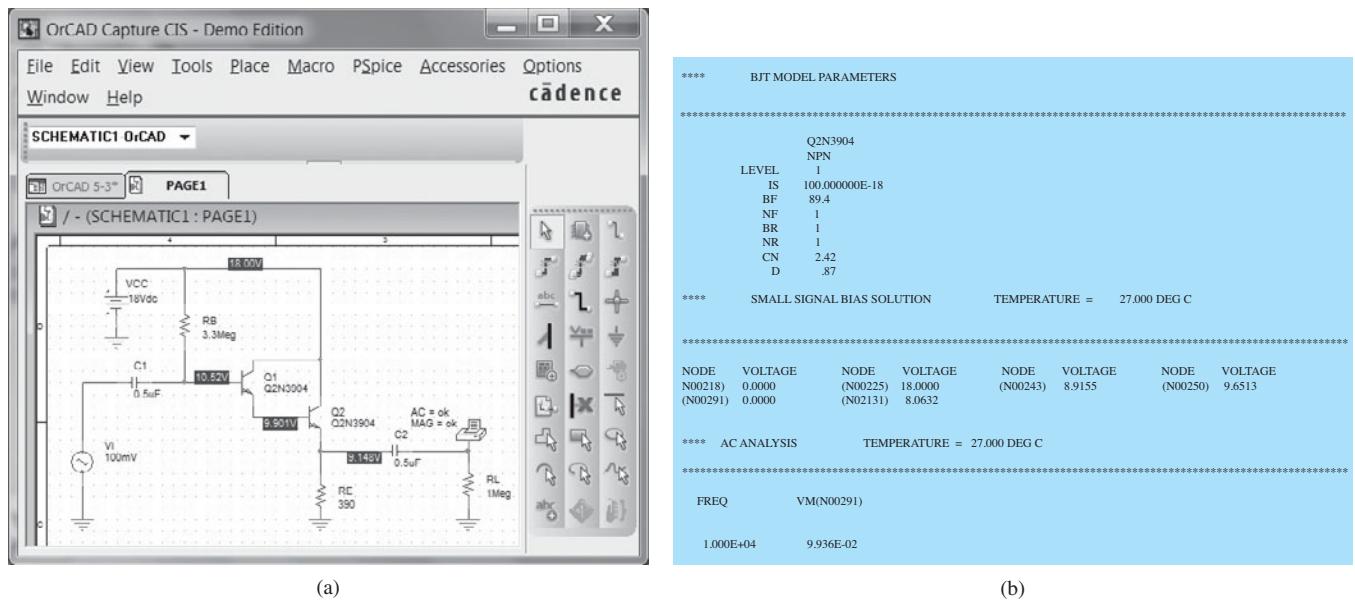
For Example 5.2,  $\beta$  is 90, with  $\beta r_e = 1.66 \text{ k}\Omega$ . The current-controlled current source (CCCS) is found in the ANALOG library as part F. After selection, an OK, and the graphical symbol for the CCCS will appear on the screen as shown in Fig. 5.146. Because it does not appear within the basic structure of the CCCS, it must be added in series with the controlling current that appears as an arrow in the symbol. Note the added 1.66-k $\Omega$  resistor, labeled **beta-re** in Fig. 5.146. Double-clicking on the CCCS symbol will result in the **Property Editor** dialog box, in which the **GAIN** can be set to 90. It is the only change to be made in the listing. Then select **Display** followed by **Name and Value** and exit (x) the dialog box. The result is the **GAIN = 90** label appearing in Fig. 5.146.



**FIG. 5.146**  
Substituting the controlled source of Fig. 5.145 for the transistor of Fig. 5.139.

A simulation and the dc levels of Fig. 5.146 will appear. The dc levels do not match the earlier results because the network is a mix of dc and ac parameters. The equivalent model substituted in Fig. 5.146 is a representation of the transistor under ac conditions, not dc biasing conditions. When the software package analyzes the network from an ac viewpoint it will work with an ac equivalent of Fig. 5.146, which will not include the dc parameters. The **Output File** will reveal that the output collector voltage is 368.3 mV, or a gain of 368.3, essentially an exact match with the handwritten solution of 368.76. The effects of  $r_o$  could be included by simply placing a resistor in parallel with the controlled source.

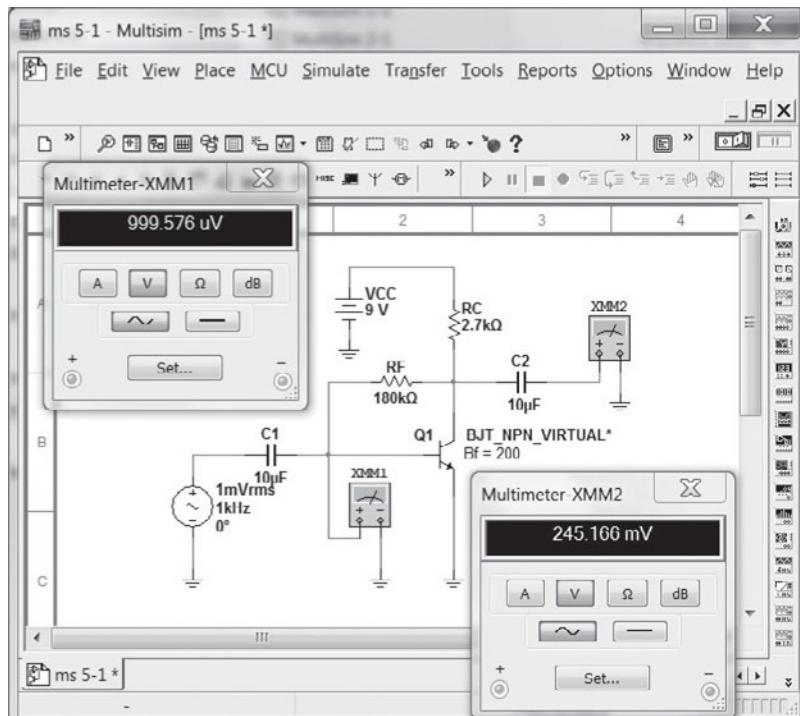
**Darlington Configuration** Although PSpice does have two Darlington pairs in the library, individual transistors are employed in Fig. 5.147 to test the solution to Example 5.17. The details of setting up the network have been covered in the preceding sections and chapters. For each transistor  $I_s$  is set to  $100E-18$  and  $\beta$  to 89.4. The applied frequency is 10 kHz. A simulation of the network results in the dc levels appearing in Fig. 5.147a and the **Output File** in Fig. 5.147b. In particular, note that the voltage drop between base and emitter for both transistors is  $10.52 \text{ V} - 9.148 \text{ V} = 1.37 \text{ V}$  compared to the 1.6 V assumed in the example. Recall that the drop across Darlington pairs is typically about 1.6 V and not simply twice that of a single transistor, or  $2(0.7 \text{ V}) = 1.4 \text{ V}$ . The output voltage of 99.36 mV is very close to the 99.80 mV obtained in Section 5.17.



**FIG. 5.147**  
(a) Design Center schematic of Darlington network; (b) output listing for circuit of part (a) (edited).

## Multisim

**Collector Feedback Configuration** Because the collector feedback configuration generated the most complex equations for the various parameters of a BJT network, it seems appropriate that Multisim be used to verify the conclusions of Example 5.9. The network appears as shown in Fig. 5.148 using the “virtual” transistor from the **Transistor family** toolbar. Recall from the previous chapter that transistors are obtained by first selecting the **Transistor** keypad appearing as the fourth option over on the **component**



**FIG. 5.148**  
Network of Example 5.9 redrawn using Multisim.

toolbar. Once chosen, the **Select a Component** dialog box will appear; under the **Family** heading, select **TRANSISTORS\_VIRTUAL** followed by **BJT\_NPN\_VIRTUAL**. Following an **OK** the symbols and labels will appear as shown in Fig. 5.148. We must now check that the beta value is 200 to match the example under investigation. This can be accomplished using one of two paths. In Chapter 4 we used the **EDIT-PROPERTIES** sequence, but here we will simply double-click on the symbol to obtain the **TRANSISTORS\_VIRTUAL** dialog box. Under **Value**, select **Edit Model** to obtain the **Edit Model** dialog box (the dialog box has a different appearance from that obtained with the other route and requires a different sequence to change its parameters). The value of **BF** appears as **100**, which must be changed to 200. First select the **BF** line to make it blue all the way across. Then place the cursor directly over the 100 value and select it to isolate it as the quantity to be changed. After deleting the 100, type in the desired 200 value. Then click the **BF** line directly under the **Name** heading and the entire line will be blue again, but now with the 200 value. Then choose **Change Part Model** at the bottom left of the dialog box and the **TRANSISTORS-VIRTUAL** dialog box will appear again. Select **OK** and  $\beta = 200$  will be set for the virtual transistor. Note the asterisk next to the BJT label to indicate the parameters of the device have been changed from the default values. The label **Bf = 100** was set using **Place-Text** as described in the previous chapter.

This will be the first opportunity to set up an ac source. First, it is important to realize that there are two types of ac sources available, one whose value is in rms units, the other with its peak value displayed. The option under **Power Sources** uses **rms** values, whereas the ac source under **Signal Sources** uses **peak** values. Because meters display rms values, the **Power Sources** option will be used here. Once **Source** is selected, the **Select a Component** dialog box will appear. Under the **Family** listing select **POWER\_SOURCES** and then select **AC\_POWER** under the **Component** listing. An **OK**, and the source will appear on the screen with four pieces of information. The label **V1** can be deleted by first double-clicking on the source symbol to obtain the **AC\_POWER** dialog box. Select **Display** and disengage **Use Schematic Global Settings**. To remove the label **V1**, disengage the **Show RefDes** option. An **OK**, and the **V1** will disappear from the screen. Next the value has to be set at 1 mV, a process initiated by selecting **Value** in the **AC\_POWER** dialog box and then changing the **Voltage (RMS)** to 1 mV. The units of mV can be set using the scroll keys to the right of the magnitude of the source. After you change the **Voltage** to **1 mV**, an **OK** will place this new value on the screen. The frequency of **1000 Hz** can be set in the same way. The **0-degree** phase shift happens to be the default value.

The label **Bf = 200** is set in the same way as described in Chapter 4. The two multimeters are obtained using the first option at the top of the right vertical toolbar. The meter faces appearing in Fig. 5.148 were obtained by simply double-clicking on the multimeter symbols on the schematic. Both were set to read voltages, the magnitudes of which will be in rms units.

After simulation the results of Fig. 5.148 appear. Note that the meter **XMM1** is not reading the 1 mV expected. This is due to the small drop in voltage across the input capacitor at 1 kHz. Certainly, however, it is very close to 1 mV. The output of 245.166 mV quickly reveals that the gain of the transistor configuration is about 245.2, which is a very close match with the 240 obtained in Example 5.9.

**Darlington Configuration** Applying Multisim to the network of Fig. 5.147 with a packaged Darlington amplifier results in the printout of Fig. 5.149. For each transistor the parameters were changed to **Is = 100E-18 A** and **Bf = 89.4** using the technique described earlier. For practice purposes the ac signal source was employed rather than the power source. The peak value of the applied signal is set at 100 mV, but note that the multimeter reads the effective or rms value of 99.991 mV. The indicators reveal that the base voltage of  $Q_1$  is 7.736 V, and the emitter voltage of  $Q_2$  is 6.193 V. The rms value of the output voltage is 99.163 mV, resulting in a gain of 0.99 as expected for the emitter follower configuration. The collector current is 16 mA with a base current of 1.952 mA, resulting in a  $\beta_D$  of about 8200.

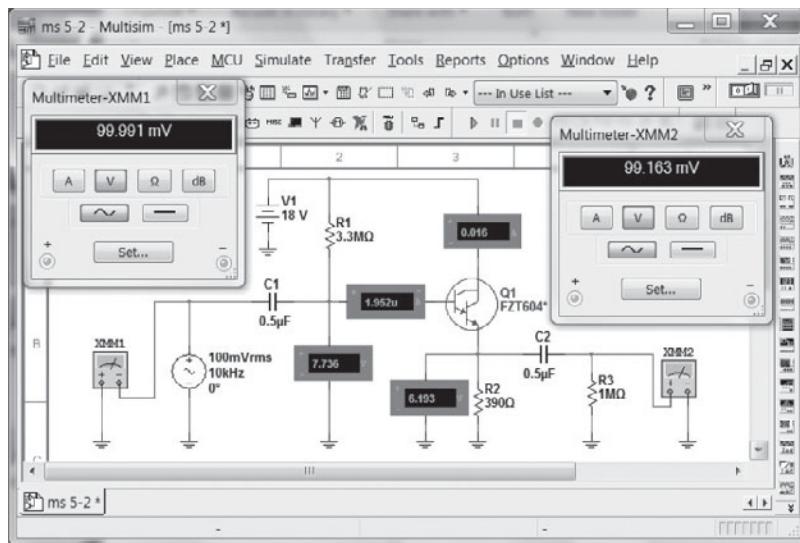


FIG. 5.149

Network of Example 5.9 redrawn using Multisim.

## PROBLEMS

\*Note: Asterisks indicate more difficult problems.

### 5.2 Amplification in the AC Domain

1. a. What is the expected amplification of a BJT transistor amplifier if the dc supply is set to zero volts?
- b. What will happen to the output ac signal if the dc level is insufficient? Sketch the effect on the waveform.
- c. What is the conversion efficiency of an amplifier in which the effective value of the current through a  $2.2\text{-k}\Omega$  load is 5 mA and the drain on the 18-V dc supply is 3.8 mA?
2. Can you think of an analogy that would explain the importance of the dc level on the resulting ac gain?
3. If a transistor amplifier has more than one dc source, can the superposition theorem be applied to obtain the response of each dc source and algebraically add the results?

### 5.3 BJT Transistor Modeling

4. What is the reactance of a  $10\text{-}\mu\text{F}$  capacitor at a frequency of 1 kHz? For networks in which the resistor levels are typically in the kilohm range, is it a good assumption to use the short-circuit equivalence for the conditions just described? How about at 100 kHz?
5. Given the common-base configuration of Fig. 5.150, sketch the ac equivalent using the notation for the transistor model appearing in Fig. 5.7.

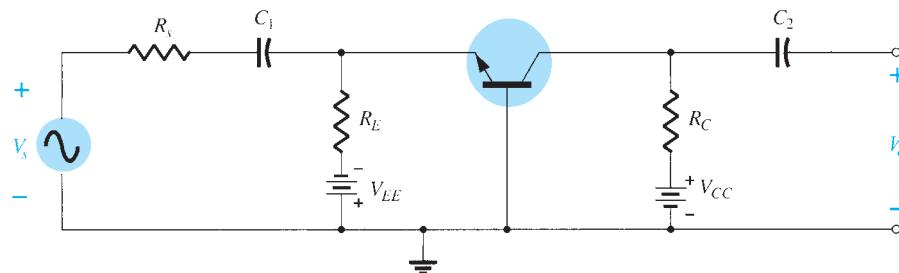


FIG. 5.150

Problem 5.

### 5.4 The $r_e$ Transistor Model

6. a. Given an Early voltage of  $V_A = 100$  V, determine  $r_o$  if  $V_{CEQ} = 8$  V and  $I_{CQ} = 4$  mA.
- b. Using the results of part (a), find the change in  $I_C$  for a change in  $V_{CE}$  of 6 V at the same  $Q$ -point as part (a).

7. For the common-base configuration of Fig. 5.18, an ac signal of 10 mV is applied, resulting in an ac emitter current of 0.5 mA. If  $\alpha = 0.980$ , determine:
- $Z_i$ .
  - $V_o$  if  $R_L = 1.2 \text{ k}\Omega$ .
  - $A_v = V_o/V_i$ .
  - $Z_o$  with  $r_o = \infty \Omega$ .
  - $A_i = I_o/I_i$ .
  - $I_b$ .
8. Using the model of Fig. 5.16, determine the following for a common-emitter amplifier if  $\beta = 80$ ,  $I_E(\text{dc}) = 2 \text{ mA}$ , and  $r_o = 40 \text{ k}\Omega$ .
- $Z_i$ .
  - $I_b$ .
  - $A_i = I_o/I_i = I_L/I_b$  if  $R_L = 1.2 \text{ k}\Omega$ .
  - $A_v$  if  $R_L = 1.2 \text{ k}\Omega$ .
9. The input impedance to a common-emitter transistor amplifier is  $1.2 \text{ k}\Omega$  with  $\beta = 140$ ,  $r_o = 50 \text{ k}\Omega$ , and  $R_L = 2.7 \text{ k}\Omega$ . Determine:
- $r_e$ .
  - $I_b$  if  $V_i = 30 \text{ mV}$ .
  - $I_c$ .
  - $A_i = I_o/I_i = I_L/I_b$ .
  - $A_v = V_o/V_i$ .
10. For the common-base configuration of Fig. 5.18, the dc emitter current is 3.2 mA and  $\alpha$  is 0.99. Determine the following if the applied voltage is 48 mV and the load is  $2.2 \text{ k}\Omega$ .
- $r_e$ .
  - $Z_i$ .
  - $I_c$ .
  - $V_o$ .
  - $A_v$ .
  - $I_b$ .

### 5.5 Common-Emitter Fixed-Bias Configuration

11. For the network of Fig. 5.151:
- Determine  $Z_i$  and  $Z_o$ .
  - Find  $A_v$ .
  - Repeat parts (a) and (b) with  $r_o = 20 \text{ k}\Omega$ .
12. For the network of Fig. 5.152, determine  $V_{CC}$  for a voltage gain of  $A_v = -160$ .

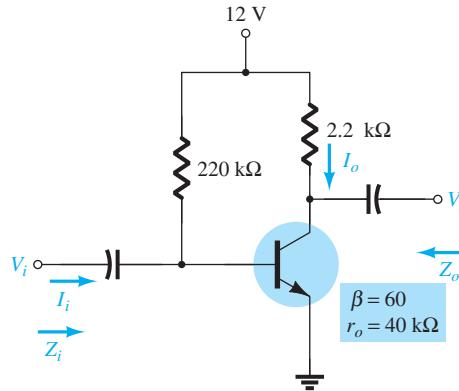


FIG. 5.151

Problem 11.

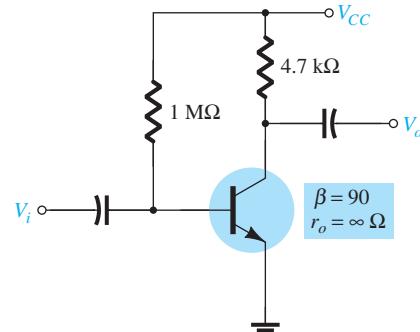
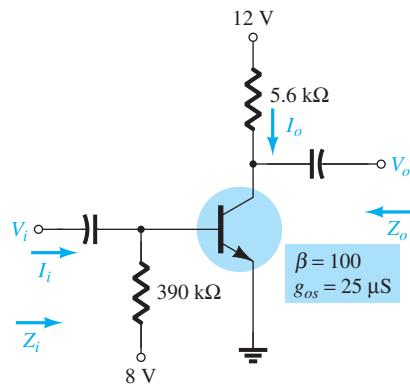


FIG. 5.152

Problem 12.

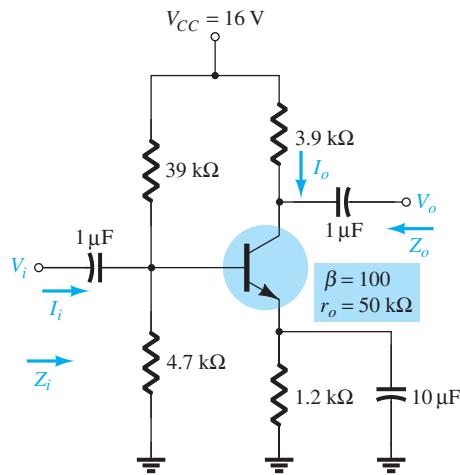
- \*13. For the network of Fig. 5.153:
- Calculate  $I_B$ ,  $I_C$ , and  $r_e$ .
  - Determine  $Z_i$  and  $Z_o$ .
  - Calculate  $A_v$ .
  - Determine the effect of  $r_o = 30 \text{ k}\Omega$  on  $A_v$ .
14. For the network of Fig. 5.153, what value of  $R_C$  will cut the voltage gain to half the value obtained in problem 13?



**FIG. 5.153**  
Problem 13.

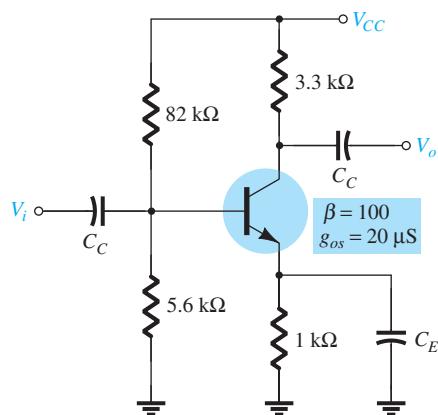
### 5.6 Voltage-Divider Bias

15. For the network of Fig. 5.154:
- Determine  $r_e$ .
  - Calculate  $Z_i$  and  $Z_o$ .
  - Find  $A_v$ .
  - Repeat parts (b) and (c) with  $r_o = 25 \text{ k}\Omega$ .

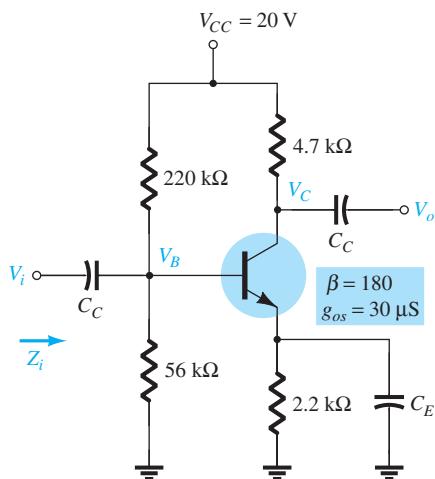


**FIG. 5.154**  
Problem 15.

16. Determine  $V_{CC}$  for the network of Fig. 5.155 if  $A_v = -160$  and  $r_o = 100 \text{ k}\Omega$ .
17. For the network of Fig. 5.156:
- Determine  $r_e$ .
  - Calculate  $V_B$  and  $V_C$ .
  - Determine  $Z_i$  and  $A_v = V_o/V_i$ .



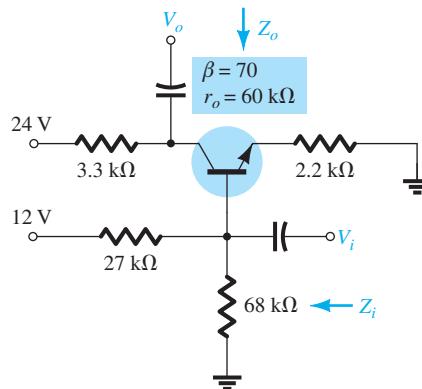
**FIG. 5.155**  
Problem 16.



**FIG. 5.156**  
Problem 17.

18. For the network of Fig. 5.157:

- Determine  $r_e$ .
- Find the dc voltages  $V_B$ ,  $V_{CB}$ , and  $V_{CE}$ .
- Determine  $Z_i$  and  $Z_o$ .
- Calculate  $A_v = V_o/V_i$ .



**FIG. 5.157**  
Problem 18.

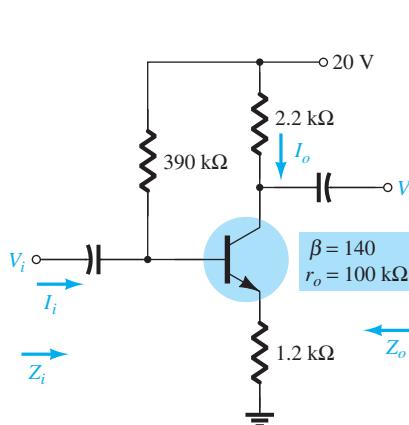
### 5.7 CE Emitter-Bias Configuration

19. For the network of Fig. 5.158:

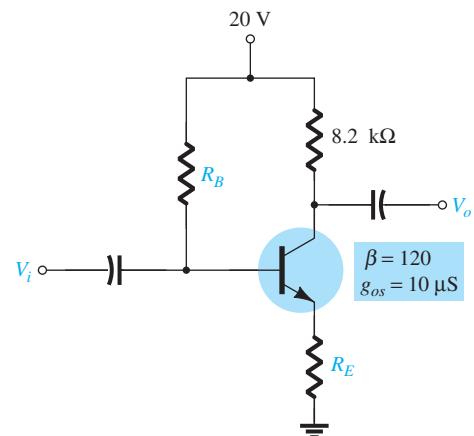
- Determine  $r_e$ .
- Find  $Z_i$  and  $Z_o$ .
- Calculate  $A_v$ .
- Repeat parts (b) and (c) with  $r_o = 20 \text{ k}\Omega$ .

20. Repeat Problem 19 with  $R_E$  bypassed. Compare results.

21. For the network of Fig. 5.159, determine  $R_E$  and  $R_B$  if  $A_v = -10$  and  $r_e = 3.8 \Omega$ . Assume that  $Z_b = \beta R_E$ .



**FIG. 5.158**  
Problems 19 and 20.



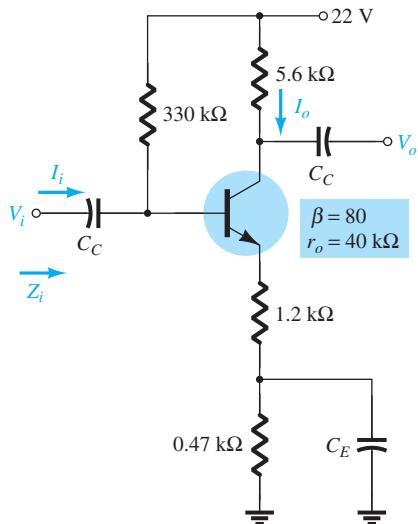
**FIG. 5.159**  
Problem 21.

- \*22. For the network of Fig. 5.160:

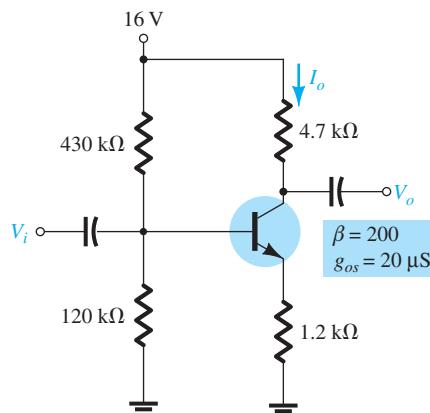
- Determine  $r_e$ .
- Find  $Z_i$  and  $A_v$ .

23. For the network of Fig. 5.161:

- Determine  $r_e$ .
- Calculate  $V_B$ ,  $V_{CE}$ , and  $V_{CB}$ .
- Determine  $Z_i$  and  $Z_o$ .
- Calculate  $A_v = V_o/V_i$ .
- Determine  $A_i = I_o/I_i$ .



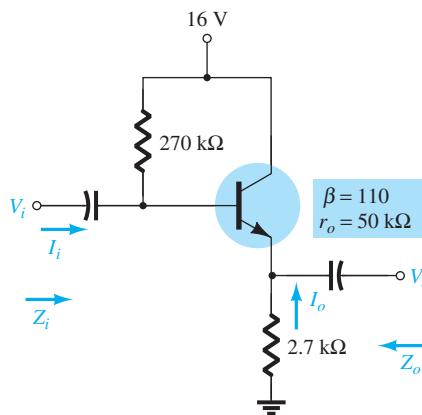
**FIG. 5.160**  
Problem 22.



**FIG. 5.161**  
Problem 23.

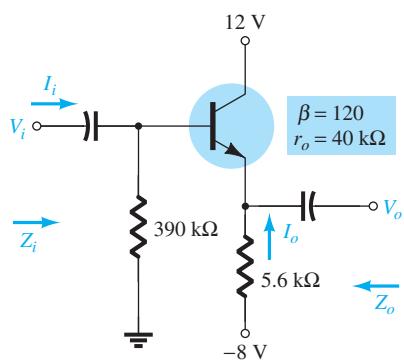
### 5.8 Emitter-Follower Configuration

24. For the network of Fig. 5.162:
- Determine  $r_e$  and  $\beta r_e$ .
  - Find  $Z_i$  and  $Z_o$ .
  - Calculate  $A_v$ .

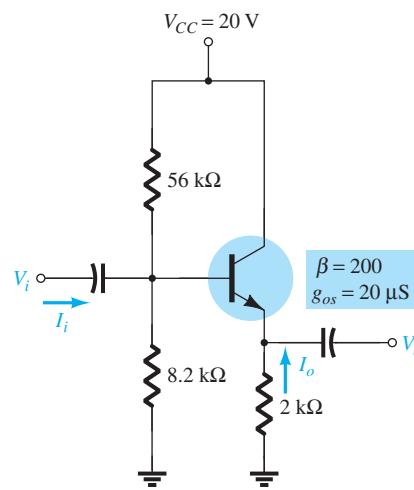


**FIG. 5.162**  
Problem 24.

- \*25. For the network of Fig. 5.163:
- Determine  $Z_i$  and  $Z_o$ .
  - Find  $A_v$ .
  - Calculate  $V_o$  if  $V_i = 1 \text{ mV}$ .
- \*26. For the network of Fig. 5.164:
- Calculate  $I_B$  and  $I_C$ .
  - Determine  $r_e$ .
  - Determine  $Z_i$  and  $Z_o$ .
  - Find  $A_v$ .



**FIG. 5.163**  
Problem 25.



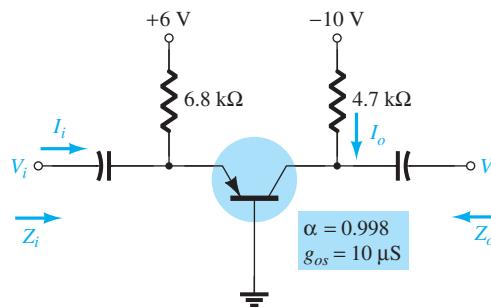
**FIG. 5.164**  
Problem 26.

### 5.9 Common-Base Configuration

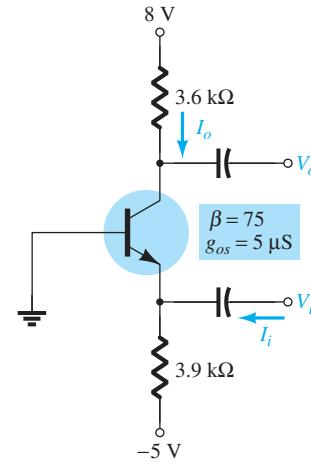
27. For the common-base configuration of Fig. 5.165:

- Determine  $r_e$ .
- Find  $Z_i$  and  $Z_o$ .
- Calculate  $A_v$ .

\*28. For the network of Fig. 5.166, determine  $A_v$ .



**FIG. 5.165**  
Problem 27.



**FIG. 5.166**  
Problem 28.

### 5.10 Collector Feedback Configuration

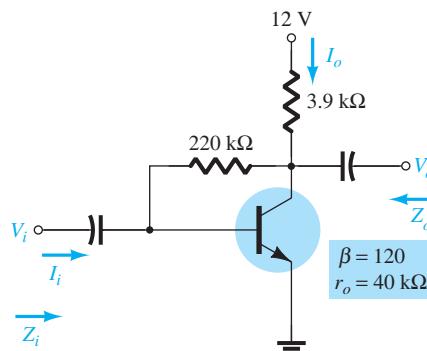
29. For the collector feedback configuration of Fig. 5.167:

- Determine  $r_e$ .
- Find  $Z_i$  and  $Z_o$ .
- Calculate  $A_v$ .

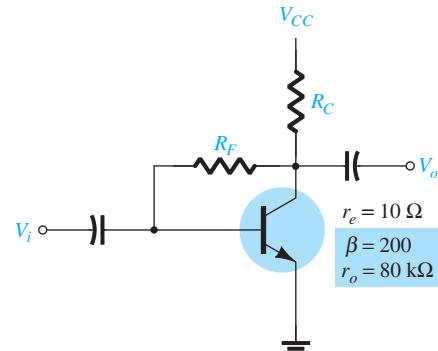
\*30. Given  $r_e = 10 \Omega$ ,  $\beta = 200$ ,  $A_v = -160$ , and  $A_i = 19$  for the network of Fig. 5.168, determine  $R_C$ ,  $R_F$ , and  $V_{CC}$ .

\*31. For the network of Fig. 5.49:

- Derive the approximate equation for  $A_v$ .
- Derive the approximate equations for  $Z_i$  and  $Z_o$ .
- Given  $R_C = 2.2 \text{ k}\Omega$ ,  $R_F = 120 \text{ k}\Omega$ ,  $R_E = 1.2 \text{ k}\Omega$ ,  $\beta = 90$ , and  $V_{CC} = 10 \text{ V}$ , calculate the magnitudes of  $A_v$ ,  $Z_i$ , and  $Z_o$  using the equations of parts (a) and (b).



**FIG. 5.167**  
Problem 29.

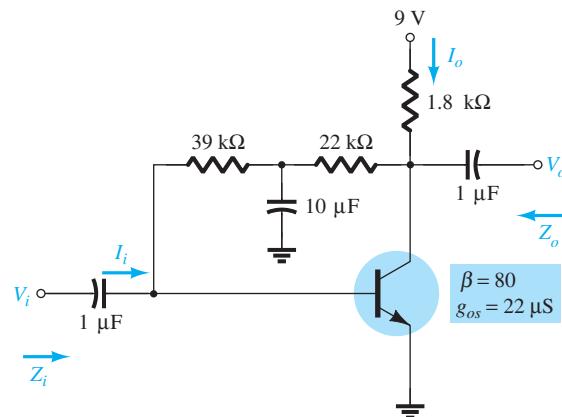


**FIG. 5.168**  
Problem 30.

### 5.11 Collector DC Feedback Configuration

32. For the network of Fig. 5.169:

- Determine  $Z_i$  and  $Z_o$ .
- Find  $A_v$ .



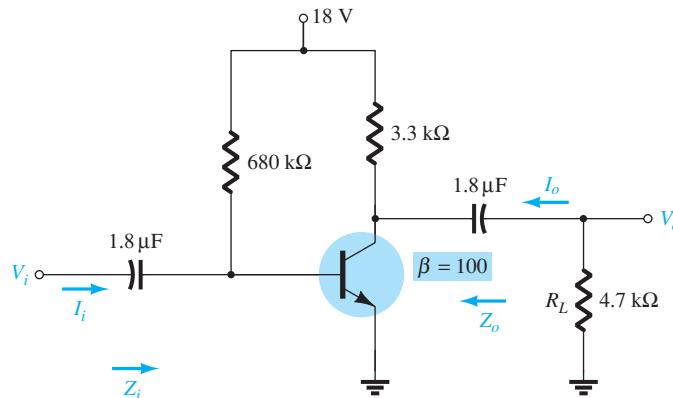
**FIG. 5.169**  
Problems 32 and 33.

33. Repeat problem 32 with the addition of an emitter resistor  $R_E = 0.68 \text{ k}\Omega$ .

#### 5.12–5.15 Effect of $R_L$ and $R_s$ and Two-Port Systems Approach

- \*34. For the fixed-bias configuration of Fig. 5.170:

- Determine  $A_{v_{NL}}$ ,  $Z_i$ , and  $Z_o$ .
- Sketch the two-port model of Fig. 5.63 with the parameters determined in part (a) in place.
- Calculate the gain  $A_{v_L} = V_o/V_i$ .
- Determine the current gain  $A_{i_L} = I_o/I_i$ .



**FIG. 5.170**  
Problems 34 and 35.

35. a. Determine the voltage gain  $A_{v_L}$  for the network of Fig. 5.170 for  $R_L = 4.7 \text{ k}\Omega$ ,  $2.2 \text{ k}\Omega$ , and  $0.5 \text{ k}\Omega$ . What is the effect of decreasing levels of  $R_L$  on the voltage gain?  
 b. How will  $Z_i$ ,  $Z_o$ , and  $A_{v_{NL}}$  change with decreasing values of  $R_L$ ?
- \*36. For the network of Fig. 5.171:  
 a. Determine  $A_{v_{NL}}$ ,  $Z_i$ , and  $Z_o$ .  
 b. Sketch the two-port model of Fig. 5.63 with the parameters determined in part (a) in place.  
 c. Determine  $A_v = V_o/V_i$ .  
 d. Determine  $A_{v_s} = V_o/V_s$ .  
 e. Change  $R_s$  to  $1 \text{ k}\Omega$  and determine  $A_v$ . How does  $A_v$  change with the level of  $R_s$ ?  
 f. Change  $R_s$  to  $1 \text{ k}\Omega$  and determine  $A_{v_s}$ . How does  $A_{v_s}$  change with the level of  $R_s$ ?  
 g. Change  $R_s$  to  $1 \text{ k}\Omega$  and determine  $A_{v_{NL}}$ ,  $Z_i$ , and  $Z_o$ . How do they change with the change in  $R_s$ ?  
 h. For the original network of Fig. 5.171 calculate  $A_i = I_o/I_i$ .

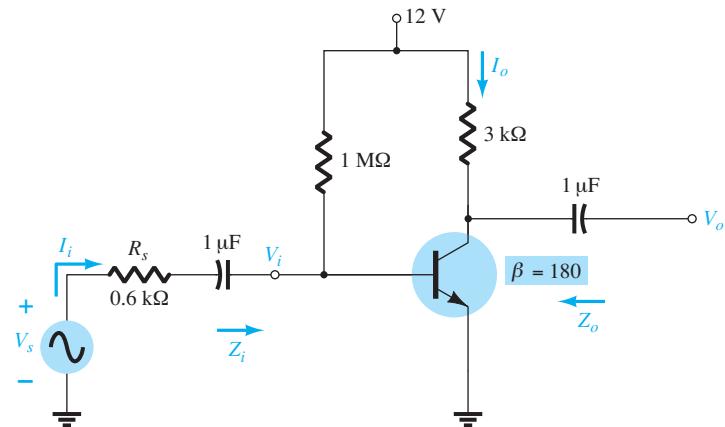


FIG. 5.171

Problem 36.

\*37. For the network of Fig. 5.172:

- Determine  $A_{v_{NL}}$ ,  $Z_i$ , and  $Z_o$ .
- Sketch the two-port model of Fig. 5.63 with the parameters determined in part (a) in place.
- Determine  $A_{v_L}$  and  $A_{v_s}$ .
- Calculate  $A_{i_L}$ .
- Change  $R_L$  to 5.6 kΩ and calculate  $A_{v_s}$ . What is the effect of increasing levels of  $R_L$  on the gain?
- Change  $R_s$  to 0.5 kΩ (with  $R_L$  at 2.7 kΩ) and comment on the effect of reducing  $R_s$  on  $A_{v_s}$ .
- Change  $R_L$  to 5.6 kΩ and  $R_s$  to 0.5 kΩ and determine the new levels of  $Z_i$  and  $Z_o$ . How are the impedance parameters affected by changing levels of  $R_L$  and  $R_s$ ?

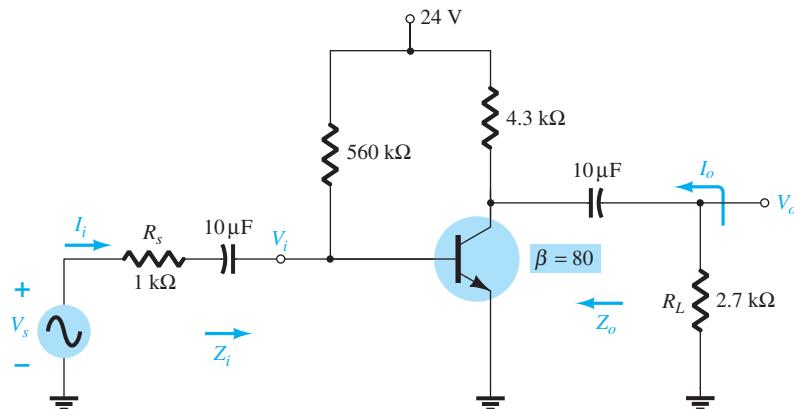
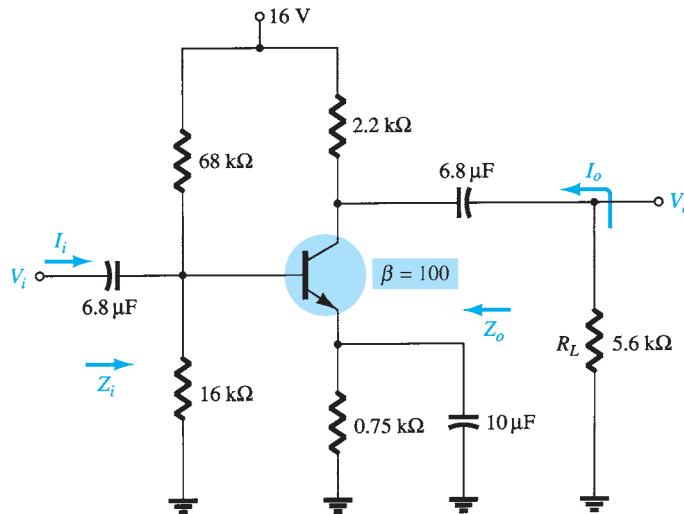


FIG. 5.172

Problem 37.

38. For the voltage-divider configuration of Fig. 5.173:

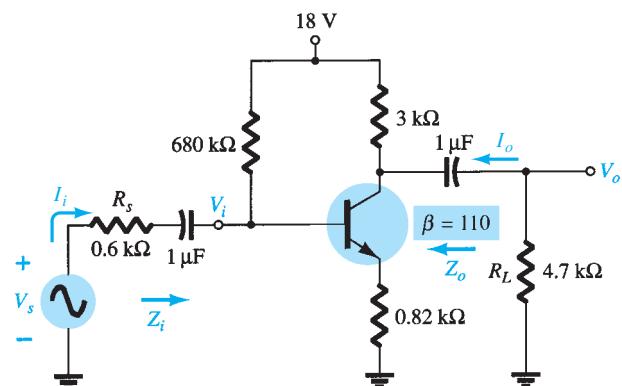
- Determine  $A_{v_{NL}}$ ,  $Z_i$ , and  $Z_o$ .
  - Sketch the two-port model of Fig. 5.63 with the parameters determined in part (a) in place.
  - Calculate the gain  $A_{v_L}$ .
  - Determine the current gain  $A_{i_L}$ .
  - Determine  $A_{v_L}$ ,  $A_{i_L}$ , and  $Z_o$  using the  $r_e$  model and compare solutions.
39. a. Determine the voltage gain  $A_{v_L}$  for the network of Fig. 5.173 with  $R_L = 4.7$  kΩ, 2.2 kΩ, and 0.5 kΩ. What is the effect of decreasing levels of  $R_L$  on the voltage gain?  
b. How will  $Z_i$ ,  $Z_o$ , and  $A_{v_{NL}}$  change with decreasing levels of  $R_L$ ?



**FIG. 5.173**  
Problems 38 and 39.

40. For the emitter-stabilized network of Fig. 5.174:

- Determine  $A_{v_{NL}}$ ,  $Z_i$ , and  $Z_o$ .
- Sketch the two-port model of Fig. 5.63 with the values determined in part (a).
- Determine  $A_{v_L}$  and  $A_{v_s}$ .
- Change  $R_s$  to 1 kΩ. What is the effect on  $A_{v_{NL}}$ ,  $Z_i$ , and  $Z_o$ ?
- Change  $R_s$  to 1 kΩ and determine  $A_{v_L}$  and  $A_{v_s}$ . What is the effect of increasing levels of  $R_s$  on  $A_{v_L}$  and  $A_{v_s}$ ?
- Determine  $A_i = I_o/I_i$ .



**FIG. 5.174**  
Problem 40.

- \*41. For the network of Fig. 5.175:

- Determine  $A_{v_{NL}}$ ,  $Z_i$ , and  $Z_o$ .
- Sketch the two-port model of Fig. 5.63 with the values determined in part (a).
- Determine  $A_{v_L}$  and  $A_{v_s}$ .
- Change  $R_s$  to 1 kΩ and determine  $A_{v_L}$  and  $A_{v_s}$ . What is the effect of increasing levels of  $R_s$  on the voltage gains?
- Change  $R_s$  to 1 kΩ and determine  $A_{v_{NL}}$ ,  $Z_i$ , and  $Z_o$ . What is the effect of increasing levels of  $R_s$  on the parameters?
- Change  $R_L$  to 5.6 kΩ and determine  $A_{v_L}$  and  $A_{v_s}$ . What is the effect of increasing levels of  $R_L$  on the voltage gains? Maintain  $R_s$  at its original level of 0.6 kΩ.
- Determine  $A_i = \frac{I_o}{I_i}$  with  $R_L = 2.7$  kΩ and  $R_s = 0.6$  kΩ.

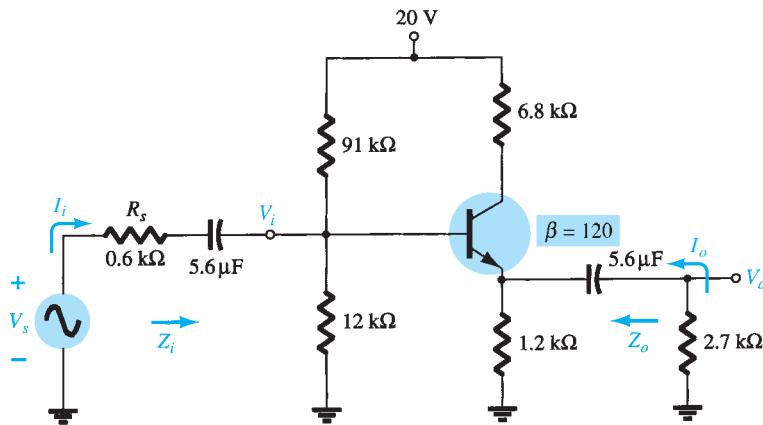


FIG. 5.175

Problem 41.

\*42. For the common-base network of Fig. 5.176:

- Determine  $Z_i$ ,  $Z_o$ , and  $A_{v_{NL}}$ .
- Sketch the two-port model of Fig. 5.63 with the parameters of part (a) in place.
- Determine  $A_{v_L}$  and  $A_{v_s}$ .
- Determine  $A_{v_L}$  and  $A_{v_s}$  using the  $r_e$  model and compare with the results of part (c).
- Change  $R_s$  to 0.5 k $\Omega$  and  $R_L$  to 2.2 k $\Omega$  and calculate  $A_{v_L}$  and  $A_{v_s}$ . What is the effect of changing levels of  $R_s$  and  $R_L$  on the voltage gains?
- Determine  $Z_o$  if  $R_s$  changed to 0.5 k $\Omega$  with all other parameters as appearing in Fig. 5.176. How is  $Z_o$  affected by changing levels of  $R_s$ ?
- Determine  $Z_i$  if  $R_L$  is reduced to 2.2 k $\Omega$ . What is the effect of changing levels of  $R_L$  on the input impedance?
- For the original network of Fig. 5.176 determine  $A_i = I_o/I_i$ .

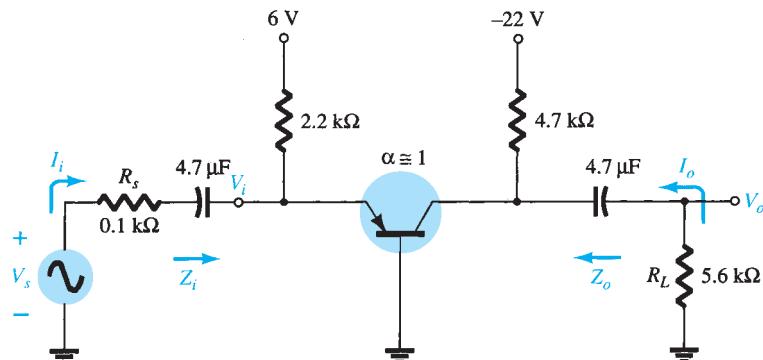


FIG. 5.176

Problem 42.

## 5.16 Cascaded Systems

\*43. For the cascaded system of Fig. 5.177 with two identical stages, determine:

- The loaded voltage gain of each stage.
- The total gain of the system,  $A_v$  and  $A_{v_s}$ .
- The loaded current gain of each stage.
- The total current gain of the system  $A_{i_L} = I_o/I_i$ .
- How  $Z_i$  is affected by the second stage and  $R_L$ .
- How  $Z_o$  is affected by the first stage and  $R_s$ .
- The phase relationship between  $V_o$  and  $V_i$ .

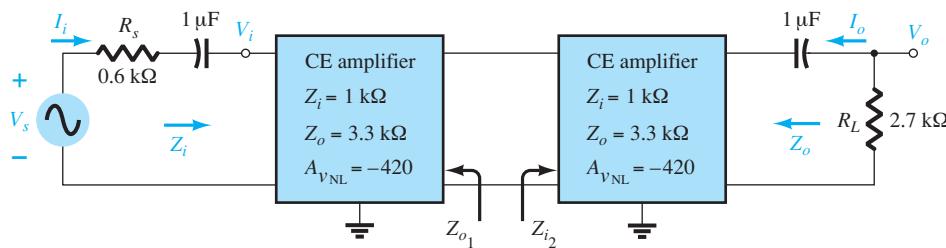


FIG. 5.177

Problem 43.

- \*44. For the cascaded system of Fig. 5.178, determine:

- The loaded voltage gain of each stage.
- The total gain of the system,  $A_{vL}$  and  $A_{vs}$ .
- The loaded current gain of each stage.
- The total current gain of the system.
- How  $Z_i$  is affected by the second stage and  $R_L$ .
- How  $Z_o$  is affected by the first stage and  $R_s$ .
- The phase relationship between  $V_o$  and  $V_i$ .

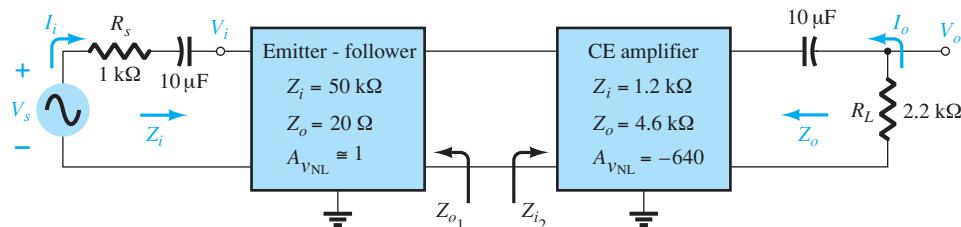


FIG. 5.178

Problem 44.

45. For the BJT cascade amplifier of Fig. 5.179, calculate the dc bias voltages and collector current for each stage.  
 46. a. Calculate the voltage gain of each stage and the overall ac voltage gain for the BJT cascade amplifier circuit of Fig. 5.179.  
 b. Find  $A_{iT} = I_o/I_i$ .

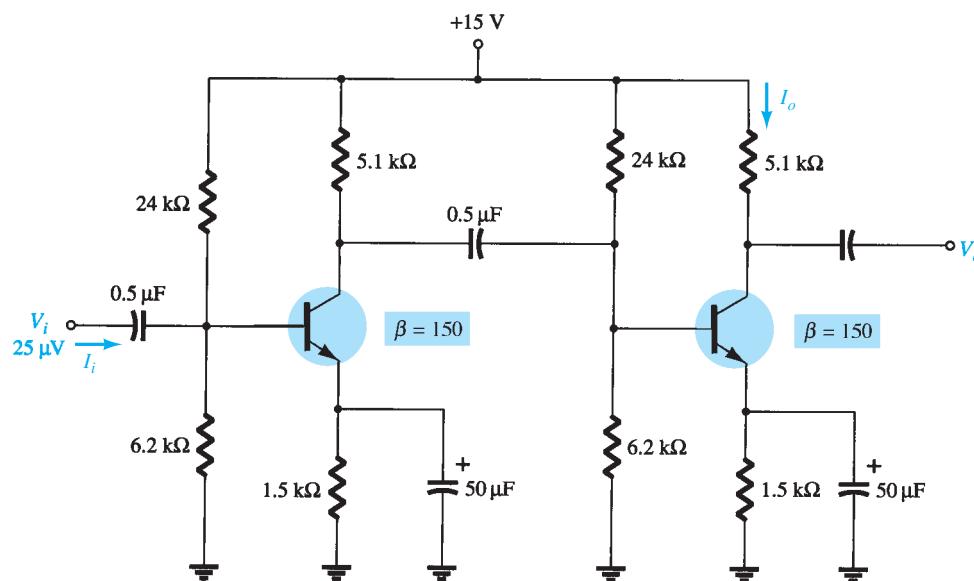


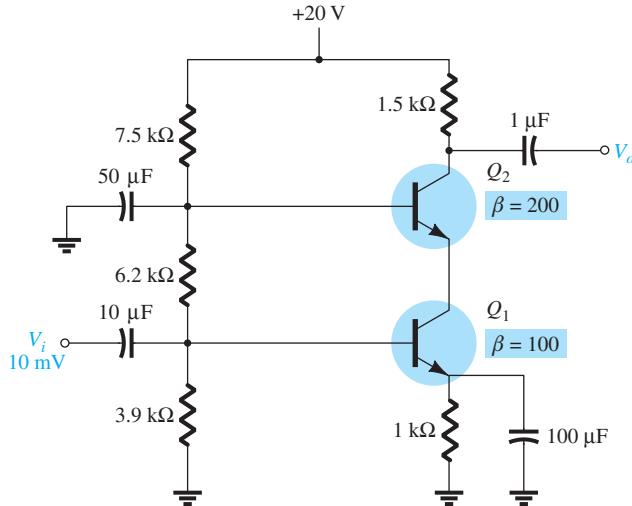
FIG. 5.179

Problems 45 and 46.

47. For the cascode amplifier circuit of Fig. 5.180, calculate the dc bias voltages  $V_{B_1}$ ,  $V_{B_2}$ , and  $V_{C_2}$ .

\*48. For the cascode amplifier circuit of Fig. 5.180, calculate the voltage gain  $A_v$  and output voltage  $V_o$ .

49. Calculate the ac voltage across a 10-k $\Omega$  load connected at the output of the circuit in Fig. 5.180.

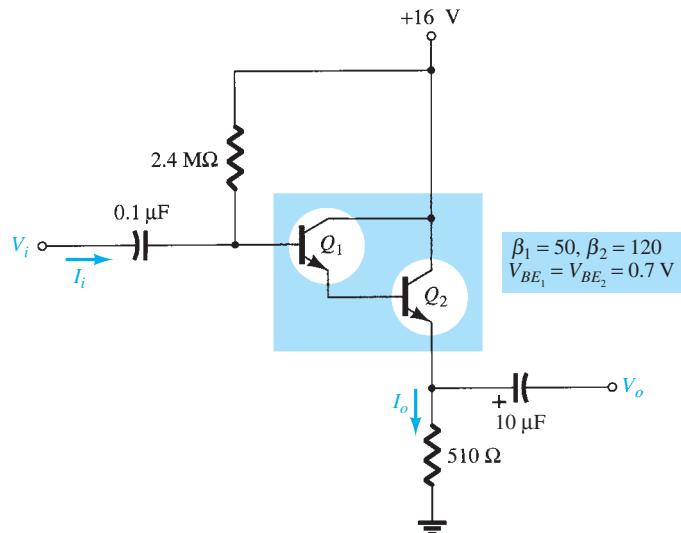


**FIG. 5.180**  
Problems 47 and 49.

### 5.17 Darlington Connection

50. For the Darlington network of Fig. 5.181:

- Determine the dc levels of  $V_{B_1}$ ,  $V_{C_1}$ ,  $V_{E_2}$ ,  $V_{CB_1}$ , and  $V_{CE_2}$ .
- Find the currents  $I_{B_1}$ ,  $I_{B_2}$ , and  $I_{E_2}$ .
- Calculate  $Z_i$  and  $Z_o$ .
- Determine the voltage gain  $A_v = V_o/V_i$  and current gain  $A_i = I_o/I_i$ .



**FIG. 5.181**  
Problems 50 through 53.

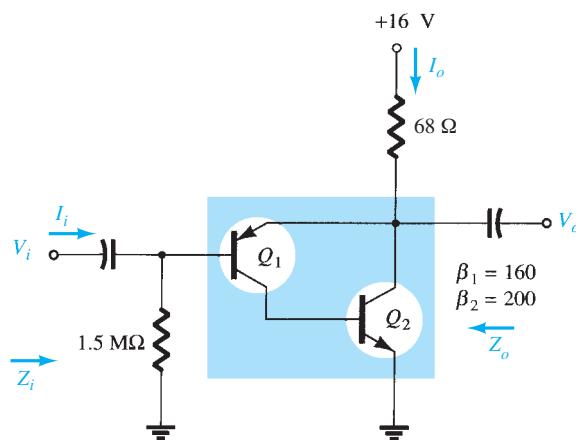
51. Repeat problem 50 with a load resistor of 1.2 k $\Omega$ .

52. Determine  $A_v = V_o/V_s$  for the network of Fig. 5.181 if the source has an internal resistance of 1.2 k $\Omega$  and the applied load is 10 k $\Omega$ .

53. A resistor  $R_C = 470 \Omega$  is added to the network of Fig. 5.181 along with a bypass capacitor  $C_E = 5 \mu\text{F}$  across the emitter resistor. If  $\beta_D = 4000$ ,  $V_{BE_T} = 1.6 \text{ V}$ , and  $r_{o_1} = r_{o_2} = 40 \text{ k}\Omega$  for a packaged Darlington amplifier:

- Find the dc levels of  $V_{B_1}$ ,  $V_{E_2}$ , and  $V_{CE_2}$ .
- Determine  $Z_i$  and  $Z_o$ .
- Determine the voltage gain  $A_v = V_o/V_i$  if the output voltage  $V_o$  is taken off the collector terminal via a coupling capacitor of 10  $\mu\text{F}$ .

54. For the feedback pair of Fig. 5.182:
- Calculate the dc voltages  $V_{B_1}$ ,  $V_{B_2}$ ,  $V_{C_1}$ ,  $V_{C_2}$ ,  $V_{E_1}$ , and  $V_{E_2}$ .
  - Determine the dc currents  $I_{B_1}$ ,  $I_{C_1}$ ,  $I_{B_2}$ ,  $I_{C_2}$ , and  $I_{E_2}$ .
  - Calculate the impedances  $Z_i$  and  $Z_o$ .
  - Find the voltage gain  $A_v = V_o/V_i$ .
  - Determine the current gain  $A_i = I_o/I_i$ .



**FIG. 5.182**  
Problems 54 and 55.

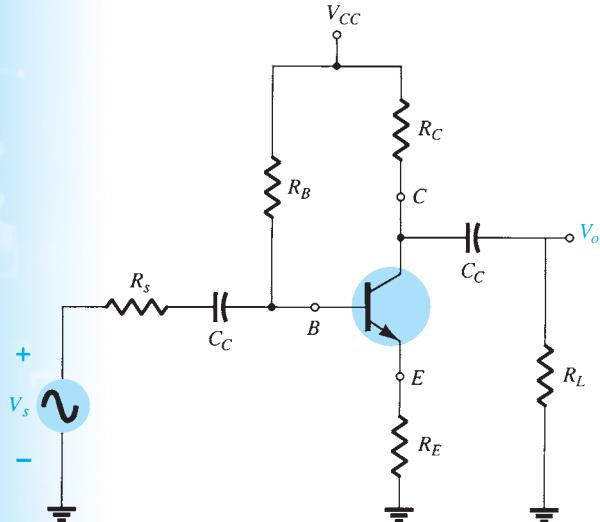
55. Repeat problem 54 if a 22-Ω resistor is added between  $V_{E_2}$  and ground.  
 56. Repeat problem 54 if a load resistance of 1.2 kΩ is introduced.

### 5.19 The Hybrid Equivalent Model

57. Given  $I_E(\text{dc}) = 1.2 \text{ mA}$ ,  $\beta = 120$ , and  $r_o = 40 \text{ k}\Omega$ , sketch the following:
- Common-emitter hybrid equivalent model.
  - Common-emitter  $r_e$  equivalent model.
  - Common-base hybrid equivalent model.
  - Common-base  $r_e$  equivalent model.
58. Given  $h_{ie} = 2.4 \text{ k}\Omega$ ,  $h_{fe} = 100$ ,  $h_{re} = 4 \times 10^{-4}$ , and  $h_{oe} = 25 \mu\text{S}$ , sketch the following:
- Common-emitter hybrid equivalent model.
  - Common-emitter  $r_e$  equivalent model.
  - Common-base hybrid equivalent model.
  - Common-base  $r_e$  equivalent model.
59. Redraw the common-emitter network of Fig. 5.3 for the ac response with the approximate hybrid equivalent model substituted between the appropriate terminals.
60. Redraw the network of Fig. 5.183 for the ac response with the  $r_e$  model inserted between the appropriate terminals. Include  $r_o$ .
61. Redraw the network of Fig. 5.184 for the ac response with the  $r_e$  model inserted between the appropriate terminals. Include  $r_o$ .
62. Given the typical values of  $h_{ie} = 1 \text{ k}\Omega$ ,  $h_{re} = 2 \times 10^{-4}$ , and  $A_v = -160$  for the input configuration of Fig. 5.185:
- Determine  $V_o$  in terms of  $V_i$ .
  - Calculate  $I_b$  in terms of  $V_i$ .
  - Calculate  $I_b$  if  $h_{re}V_o$  is ignored.
  - Determine the percentage difference in  $I_b$  using the following equation:

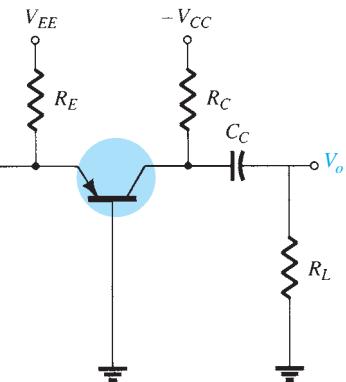
$$\% \text{ difference in } I_b = \frac{I_b(\text{without } h_{re}) - I_b(\text{with } h_{re})}{I_b(\text{without } h_{re})} \times 100\%$$

- e. Is it a valid approach to ignore the effects of  $h_{re}V_o$  for the typical values employed in this example?



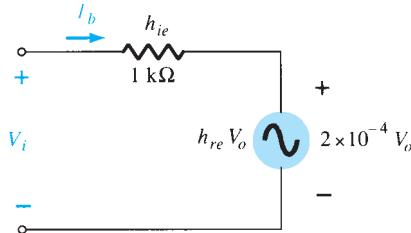
**FIG. 5.183**

Problem 60.



**FIG. 5.184**

Problem 61.



**FIG. 5.185**

Problems 62 and 64.

63. Given the typical values of  $R_L = 2.2 \text{ k}\Omega$  and  $h_{oe} = 20 \mu\text{S}$ , is it a good approximation to ignore the effects of  $1/h_{oe}$  on the total load impedance? What is the percentage difference in total loading on the transistor using the following equation?

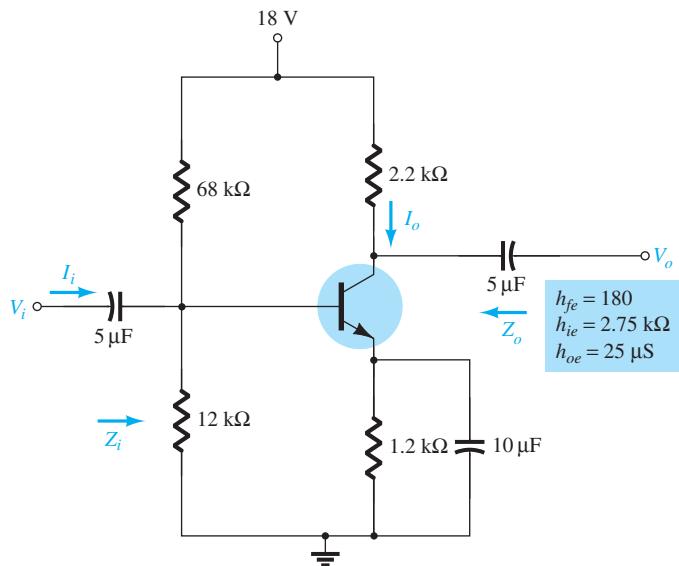
$$\% \text{ difference in total load} = \frac{R_L - R_L \parallel (1/h_{oe})}{R_L} \times 100\%$$

64. Repeat Problem 62 using the average values of the parameters of Fig. 5.92 with  $A_v = -180$ .

65. Repeat Problem 63 for  $R_L = 3.3 \text{ k}\Omega$  and the average value of  $h_{oe}$  in Fig. 5.92.

### 5.20 Approximate Hybrid Equivalent Circuit

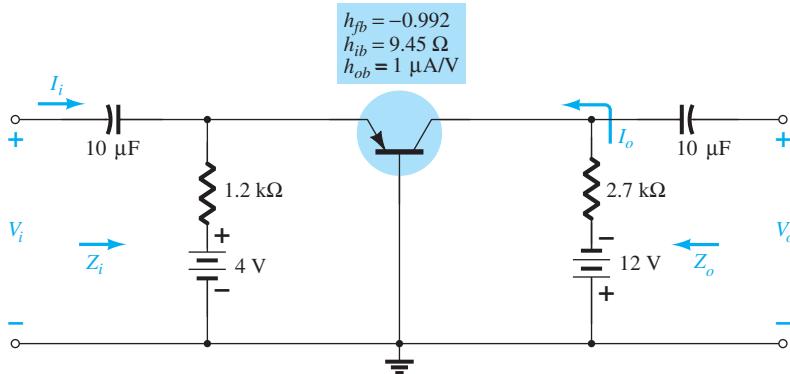
66. a. Given  $\beta = 120$ ,  $r_e = 4.5 \Omega$ , and  $r_o = 40 \text{ k}\Omega$ , sketch the approximate hybrid equivalent circuit.  
 b. Given  $h_{ie} = 1 \text{ k}\Omega$ ,  $h_{re} = 2 \times 10^{-4}$ ,  $h_{fe} = 90$ , and  $h_{oe} = 20 \mu\text{S}$ , sketch the  $r_e$  model.
67. For the network of Problem 11:  
 a. Determine  $r_e$ .  
 b. Find  $h_{fe}$  and  $h_{ie}$ .  
 c. Find  $Z_i$  and  $Z_o$  using the hybrid parameters.  
 d. Calculate  $A_v$  and  $A_i$  using the hybrid parameters.  
 e. Determine  $Z_i$  and  $Z_o$  if  $h_{oe} = 50 \mu\text{S}$ .  
 f. Determine  $A_v$  and  $A_i$  if  $h_{oe} = 50 \mu\text{S}$ .  
 g. Compare the solutions above with those of Problem 9. (Note: The solutions are available in Appendix E if Problem 11 was not performed.)
68. For the network of Fig. 5.186:  
 a. Determine  $Z_i$  and  $Z_o$ .  
 b. Calculate  $A_v$  and  $A_i$ .  
 c. Determine  $r_e$  and compare  $\beta r_e$  to  $h_{ie}$ .

**FIG. 5.186**

Problem 68.

- \*69. For the common-base network of Fig. 5.187:

- Determine  $Z_i$  and  $Z_o$ .
- Calculate  $A_v$  and  $A_i$ .
- Determine  $\alpha$ ,  $\beta$ ,  $r_e$ , and  $r_o$ .

**FIG. 5.187**

Problem 69.

### 5.21 Complete Hybrid Equivalent Model

- \*70. Repeat parts (a) and (b) of Problem 68 with  $h_{re} = 2 \times 10^{-4}$  and compare results.

- \*71. For the network of Fig. 5.188, determine:

- $Z_i$ .
- $A_v$ .
- $A_i = I_o/I_i$ .
- $Z_o$ .

- \*72. For the common-base amplifier of Fig. 5.189, determine:

- $Z_i$ .
- $A_i$ .
- $A_v$ .
- $Z_o$ .

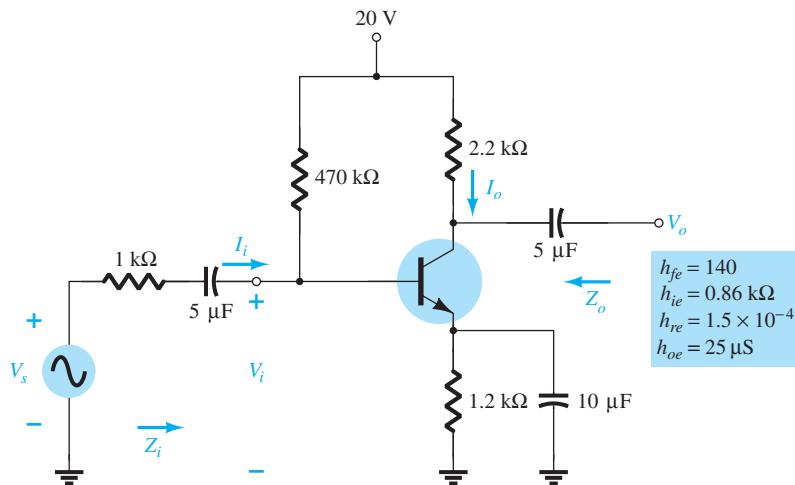


FIG. 5.188

Problem 71.

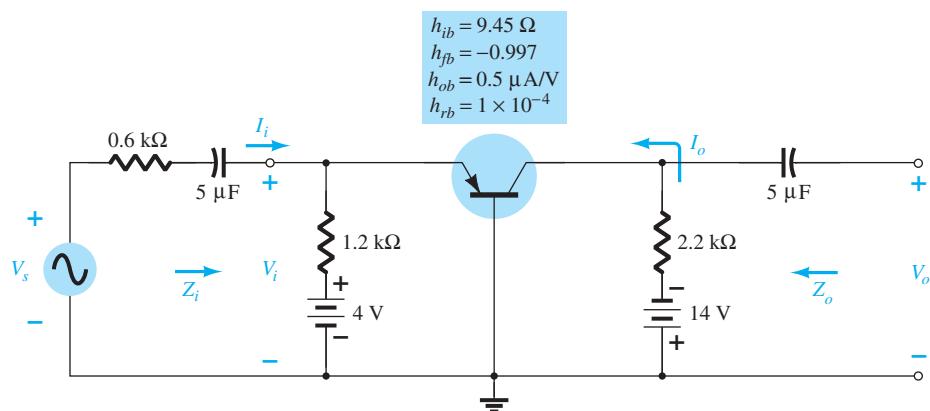


FIG. 5.189

Problem 72.

### 5.22 Hybrid $\pi$ Model

73. a. Sketch the Giacoletto (hybrid  $\pi$ ) model for a common-emitter transistor if  $r_b = 4 \Omega$ ,  $C_\pi = 5 \text{ pF}$ ,  $C_u = 1.5 \text{ pF}$ ,  $h_{oe} = 18 \mu\text{s}$ ,  $\beta = 120$ , and  $r_e = 14$ .  
b. If the applied load is  $1.2 \text{ k}\Omega$  and the source resistance is  $250 \Omega$ , draw the approximate hybrid  $\pi$  model for the low- and mid-frequency range.

### 5.23 Variations of Transistor Parameters

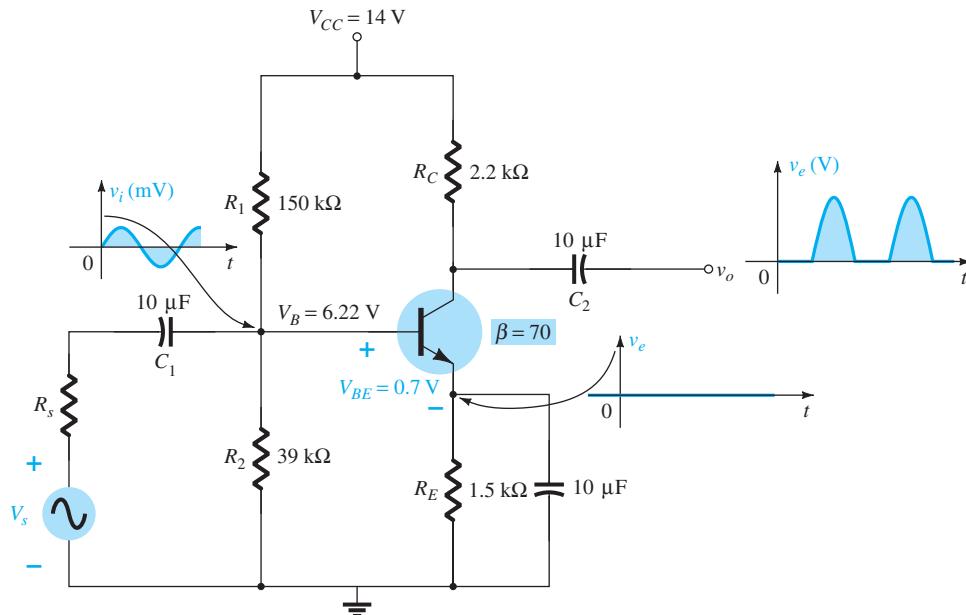
For Problems 74 through 80, use Figs. 5.124 through 5.126.

74. a. Using Fig. 5.124, determine the magnitude of the percentage change in  $h_{fe}$  for an  $I_C$  change from 0.2 mA to 1 mA using the equation
- $$\% \text{ change} = \left| \frac{h_{fe}(0.2 \text{ mA}) - h_{fe}(1 \text{ mA})}{h_{fe}(0.2 \text{ mA})} \right| \times 100\%$$
- b. Repeat part (a) for an  $I_C$  change from 1 mA to 5 mA.
75. Repeat Problem 74 for  $h_{ie}$  (same changes in  $I_C$ ).
76. a. If  $h_{oe} = 20 \mu\text{s}$  at  $I_C = 1 \text{ mA}$  on Fig. 5.124, what is the approximate value of  $h_{oe}$  at  $I_C = 0.2 \text{ mA}$ ?  
b. Determine its resistive value at 0.2 mA and compare to a resistive load of  $6.8 \text{ k}\Omega$ . Is it a good approximation to ignore the effects of  $1/h_{oe}$  in this case?
77. a. If  $h_{oe} = 20 \mu\text{s}$  at  $I_C = 1 \text{ mA}$  of Fig. 5.124, what is the approximate value of  $h_{oe}$  at  $I_C = 10 \text{ mA}$ ?  
b. Determine its resistive value at 10 mA and compare to a resistive load of  $6.8 \text{ k}\Omega$ . Is it a good approximation to ignore the effects of  $1/h_{oe}$  in this case?
78. a. If  $h_{re} = 2 \times 10^{-4}$  at  $I_C = 1 \text{ mA}$  on Fig. 5.124, determine the approximate value of  $h_{re}$  at 0.1 mA.  
b. For the value of  $h_{re}$  determined in part (a), can  $h_{re}$  be ignored as a good approximation if  $A_v = 210$ ?

79. a. Based on a review of the characteristics of Fig. 5.124, which parameter changed the least for the full range of collector current?  
 b. Which parameter changed the most?  
 c. What are the maximum and minimum values of  $1/h_{oe}$ ? Is the approximation  $1/h_{oe} \parallel R_L \approx R_L$  more appropriate at high or low levels of collector current?  
 d. In which region of current spectrum is the approximation  $h_{re}V_{ce} \approx 0$  the most appropriate?
80. a. Based on a review of the characteristics of Fig. 5.126, which parameter changed the most with increase in temperature?  
 b. Which changed the least?  
 c. What are the maximum and minimum values of  $h_{fe}$ ? Is the change in magnitude significant? Was it expected?  
 d. How does  $r_e$  vary with increase in temperature? Simply calculate its level at three or four points and compare their magnitudes.  
 e. In which temperature range do the parameters change the least?

### 5.24 Troubleshooting

- \*81. Given the network of Fig. 5.190:  
 a. Is the network properly biased?  
 b. What problem in the network construction could cause  $V_B$  to be 6.22 V and obtain the given waveform of Fig. 5.190?



**FIG. 5.190**  
Problem 81.

### 5.27 Computer Analysis

82. Using PSpice Windows, determine the voltage gain for the network of Fig. 5.25. Display the input and output waveforms.
83. Using PSpice Windows, determine the voltage gain for the network of Fig. 5.32. Display the input and output waveforms.
84. Using PSpice Windows, determine the voltage gain for the network of Fig. 5.44. Display the input and output waveforms.
85. Using Multisim, determine the voltage gain for the network of Fig. 5.28.
86. Using Multisim, determine the voltage gain for the network of Fig. 5.39.
87. Using PSpice Windows, determine the level of  $V_o$  for  $V_i = 1 \text{ mV}$  for the network of Fig. 5.69. For the capacitive elements assume a frequency of 1 kHz.
88. Repeat Problem 87 for the network of Fig. 5.71.
89. Repeat Problem 87 for the network of Fig. 5.82.
90. Repeat Problem 87 using Multisim.
91. Repeat Problem 87 using Multisim.

# 6

# Field-Effect Transistors

## CHAPTER OBJECTIVES

- Become familiar with the construction and operating characteristics of Junction Field Effect (JFET), Metal-Oxide Semiconductor FET (MOSFET), and Metal-Semiconductor FET (MESFET) transistors.
- Be able to sketch the transfer characteristics from the drain characteristics of a JFET, MOSFET, and MESFET transistor.
- Understand the vast amount of information provided on the specification sheet for each type of FET.
- Be aware of the differences between the dc analysis of the various types of FETs.

## 6.1 INTRODUCTION

The field-effect transistor (FET) is a three-terminal device used for a variety of applications that match, to a large extent, those of the BJT transistor described in Chapters 3 through 5. Although there are important differences between the two types of devices, there are also many similarities, which will be pointed out in the sections to follow.

The primary difference between the two types of transistors is the fact that:

*The BJT transistor is a current-controlled device as depicted in Fig. 6.1a, whereas the JFET transistor is a voltage-controlled device as shown in Fig. 6.1b.*

In other words, the current  $I_C$  in Fig. 6.1a is a direct function of the level of  $I_B$ . For the FET the current  $I_D$  will be a function of the voltage  $V_{GS}$  applied to the input circuit as shown in Fig. 6.1b. In each case the current of the output circuit is controlled by a parameter of the input circuit—in one case a current level and in the other an applied voltage.

Just as there are *npn* and *pnp* bipolar transistors, there are *n-channel* and *p-channel* field-effect transistors. However, it is important to keep in mind that the BJT transistor is a *bipolar* device—the prefix *bi* indicates that the conduction level is a function of two charge carriers, electrons and holes. The FET is a *unipolar* device depending solely on either electron (*n*-channel) or hole (*p*-channel) conduction.

The term *field effect* in the name deserves some explanation. We are all familiar with the ability of a permanent magnet to draw metal filings to itself without the need for actual contact. The magnetic field of the permanent magnet envelopes the filings and attracts them to the magnet along the shortest path provided by the magnetic flux lines. For the FET an *electric field* is established by the charges present, which controls the conduction path of the output circuit without the need for direct contact between the controlling and controlled quantities.

# 7

# FET Biasing

## CHAPTER OBJECTIVES

- Be able to perform a dc analysis of JFET, MOSFET, and MESFET networks.
- Become proficient in the use of load-line analysis to examine FET networks.
- Develop confidence in the dc analysis of networks with both FETs and BJTs.
- Understand how to use the Universal JFET Bias Curve to analyze the various FET configurations.

## 7.1 INTRODUCTION

In Chapter 4 we found that the biasing levels for a silicon transistor configuration can be obtained using the approximate characteristic equations  $V_{BE} = 0.7\text{ V}$ ,  $I_C = \beta I_B$ , and  $I_C \cong I_E$ . The link between input and output variables is provided by  $\beta$ , which is assumed to be fixed in magnitude for the analysis to be performed. The fact that beta is a constant establishes a *linear* relationship between  $I_C$  and  $I_B$ . Doubling the value of  $I_B$  will double the level of  $I_C$ , and so on.

For the field-effect transistor, the relationship between input and output quantities is *nonlinear* due to the squared term in Shockley's equation. Linear relationships result in straight lines when plotted on a graph of one variable versus the other, whereas nonlinear functions result in curves as obtained for the transfer characteristics of a JFET. The nonlinear relationship between  $I_D$  and  $V_{GS}$  can complicate the mathematical approach to the dc analysis of FET configurations. A graphical approach may limit solutions to tenths-place accuracy, but it is a quicker method for most FET amplifiers. Since the graphical approach is in general the most popular, the analysis of this chapter will have graphical solutions rather than mathematical solutions.

Another distinct difference between the analysis of BJT and FET transistors is that:

*The controlling variable for a BJT transistor is a current level, whereas for the FET a voltage is the controlling variable.*

In both cases, however, the controlled variable on the output side is a current level that also defines the important voltage levels of the output circuit.

The general relationships that can be applied to the dc analysis of all FET amplifiers are

$$I_G \approx 0 \text{ A} \quad (7.1)$$

and

$$I_D = I_S \quad (7.2)$$

For JFETs and depletion-type MOSFETs and MESFETs, Shockley's equation is applied to relate the input and output quantities:

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 \quad (7.3)$$

For enhancement-type MOSFETs and MESFETs, the following equation is applicable:

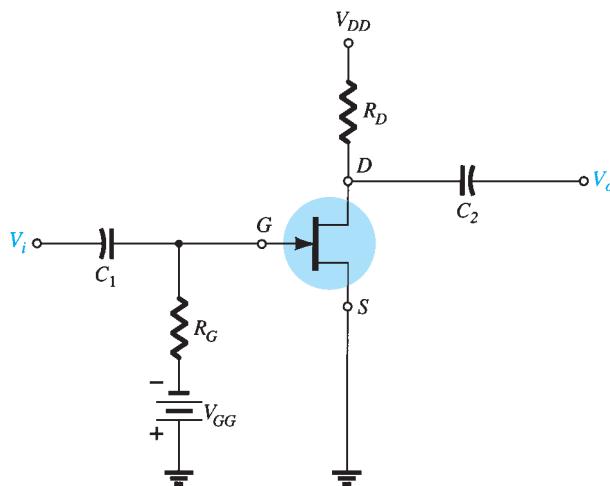
$$I_D = k(V_{GS} - V_T)^2 \quad (7.4)$$

It is particularly important to realize that all of the equations above are for the *field-effect transistor only!* They do not change with each network configuration so long as the device is in the active region. The network simply defines the level of current and voltage associated with the operating point through its own set of equations. In reality, the dc solution of BJT and FET networks is the solution of simultaneous equations established by the device and the network. The solution can be determined using a mathematical or graphical approach—a fact to be demonstrated by the first few networks to be analyzed. However, as noted earlier, the graphical approach is the most popular for FET networks and is employed in this book.

The first few sections of this chapter are limited to JFETs and the graphical approach to analysis. The depletion-type MOSFET will then be examined with its increased range of operating points, followed by the enhancement-type MOSFET. Finally, problems of a design nature are investigated to fully test the concepts and procedures introduced in the chapter.

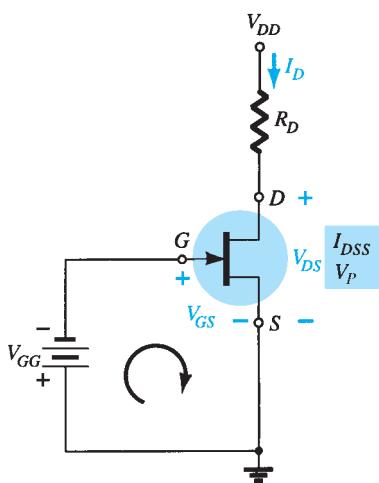
## 7.2 FIXED-BIAS CONFIGURATION

The simplest of biasing arrangements for the *n*-channel JFET appears in Fig. 7.1. Referred to as the fixed-bias configuration, it is one of the few FET configurations that can be solved just as directly using either a mathematical or a graphical approach. Both methods are included in this section to demonstrate the difference between the two methods and also to establish the fact that the same solution can be obtained using either approach.



**FIG. 7.1**  
*Fixed-bias configuration.*

The configuration of Fig. 7.1 includes the ac levels  $V_i$  and  $V_o$  and the coupling capacitors ( $C_1$  and  $C_2$ ). Recall that the coupling capacitors are “open circuits” for the dc analysis and low impedances (essentially short circuits) for the ac analysis. The resistor  $R_G$  is present to ensure that  $V_i$  appears at the input to the FET amplifier for the ac analysis (Chapter 8). For the dc analysis,



**FIG. 7.2**  
Network for dc analysis.

$$I_G \equiv 0 \text{ A}$$

and

$$V_{R_G} = I_G R_G = (0 \text{ A}) R_G = 0 \text{ V}$$

The zero-volt drop across  $R_G$  permits replacing  $R_G$  by a short-circuit equivalent, as appearing in the network of Fig. 7.2, specifically redrawn for the dc analysis.

The fact that the negative terminal of the battery is connected directly to the defined positive potential of  $V_{GS}$  clearly reveals that the polarity of  $V_{GS}$  is directly opposite to that of  $V_{GG}$ . Applying Kirchhoff's voltage law in the clockwise direction of the indicated loop of Fig. 7.2 results in

$$-V_{GG} - V_{GS} = 0$$

and

$$V_{GS} = -V_{GG} \quad (7.5)$$

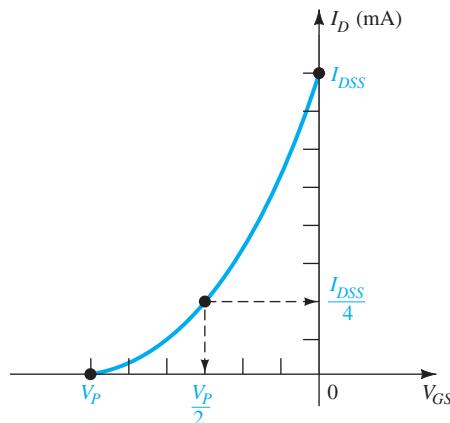
Since  $V_{GG}$  is a fixed dc supply, the voltage  $V_{GS}$  is fixed in magnitude, resulting in the designation “fixed-bias configuration.”

The resulting level of drain current  $I_D$  is now controlled by Shockley’s equation:

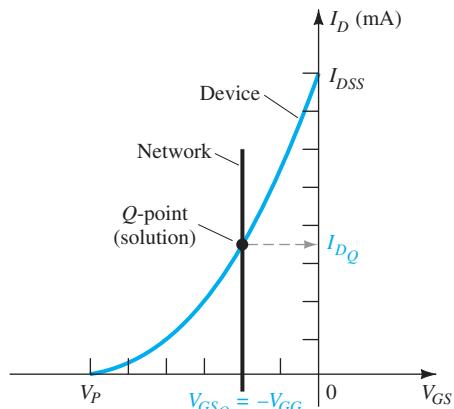
$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

Since  $V_{GS}$  is a fixed quantity for this configuration, its magnitude and sign can simply be substituted into Shockley’s equation and the resulting level of  $I_D$  calculated. This is one of the few instances in which a mathematical solution to a FET configuration is quite direct.

A graphical analysis would require a plot of Shockley’s equation as shown in Fig. 7.3. Recall that choosing  $V_{GS} = V_P/2$  will result in a drain current of  $I_{DSS}/4$  when plotting the equation. For the analysis of this chapter, the three points defined by  $I_{DSS}$ ,  $V_P$ , and the intersection just described will be sufficient for plotting the curve.



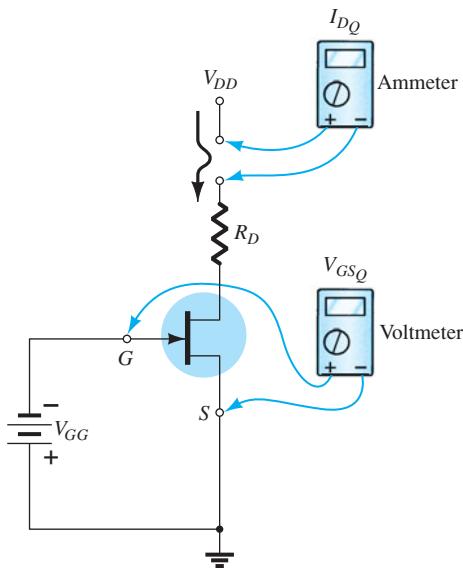
**FIG. 7.3**  
Plotting Shockley’s equation.



**FIG. 7.4**  
Finding the solution for the fixed-bias configuration.

In Fig. 7.4, the fixed level of  $V_{GS}$  has been superimposed as a vertical line at  $V_{GS} = -V_{GG}$ . At any point on the vertical line, the level of  $V_{GS}$  is  $-V_{GG}$ —the level of  $I_D$  must simply be determined on this vertical line. The point where the two curves intersect is the common solution to the configuration—commonly referred to as the *quiescent* or *operating point*. The subscript  $Q$  will be applied to the drain current and gate-to-source voltage to identify their levels at the  $Q$ -point. Note in Fig. 7.4 that the quiescent level of  $I_D$  is determined by drawing a horizontal line from the  $Q$ -point to the vertical  $I_D$  axis. It is important to realize

that once the network of Fig. 7.1 is constructed and operating, the dc levels of  $I_D$  and  $V_{GS}$  that will be measured by the meters of Fig. 7.5 are the quiescent values defined by Fig. 7.4.



**FIG. 7.5**  
Measuring the quiescent values of  $I_D$  and  $V_{GS}$ .

The drain-to-source voltage of the output section can be determined by applying Kirchhoff's voltage law as follows:

$$+V_{DS} + I_D R_D - V_{DD} = 0$$

and

$$V_{DS} = V_{DD} - I_D R_D \quad (7.6)$$

Recall that single-subscript voltages refer to the voltage at a point with respect to ground. For the configuration of Fig. 7.2,

$$V_S = 0 \text{ V} \quad (7.7)$$

Using double-subscript notation, we have

$$\begin{aligned} V_{DS} &= V_D - V_S \\ \text{or} \quad V_D &= V_{DS} + V_S = V_{DS} + 0 \text{ V} \end{aligned}$$

and

$$V_D = V_{DS} \quad (7.8)$$

In addition,

$$\begin{aligned} V_{GS} &= V_G - V_S \\ \text{or} \quad V_G &= V_{GS} + V_S = V_{GS} + 0 \text{ V} \end{aligned}$$

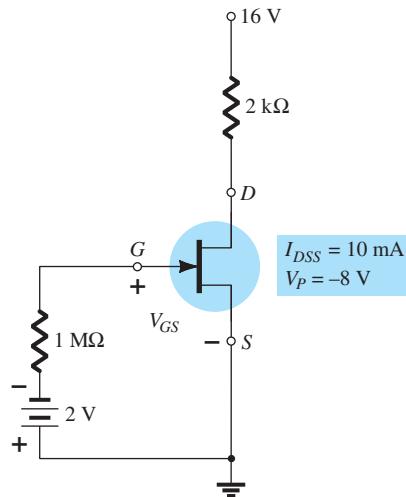
and

$$V_G = V_{GS} \quad (7.9)$$

The fact that  $V_D = V_{DS}$  and  $V_G = V_{GS}$  is fairly obvious from the fact that  $V_S = 0 \text{ V}$ , but the derivations above were included to emphasize the relationship that exists between double-subscript and single-subscript notation. Since the configuration requires two dc supplies, its use is limited and will not be included in the forthcoming list of the most common FET configurations.

**EXAMPLE 7.1** Determine the following for the network of Fig. 7.6:

- $V_{GSQ}$ .
- $I_{DQ}$ .
- $V_{DS}$ .
- $V_D$ .
- $V_G$ .
- $V_S$ .



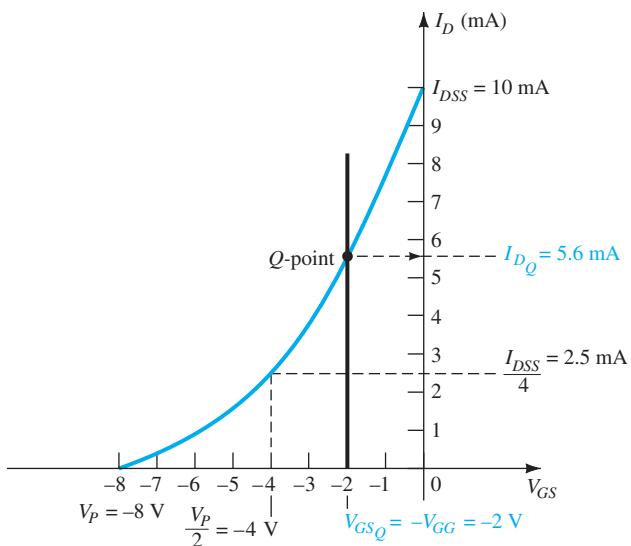
**FIG. 7.6**  
Example 7.1.

**Solution:**

**Mathematical Approach**

- $V_{GSQ} = -V_{GG} = -2 \text{ V}$
- $I_{DQ} = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10 \text{ mA} \left(1 - \frac{-2 \text{ V}}{-8 \text{ V}}\right)^2$   
 $= 10 \text{ mA}(1 - 0.25)^2 = 10 \text{ mA}(0.75)^2 = 10 \text{ mA}(0.5625)$   
 $= 5.625 \text{ mA}$
- $V_{DS} = V_{DD} - I_D R_D = 16 \text{ V} - (5.625 \text{ mA})(2 \text{ k}\Omega)$   
 $= 16 \text{ V} - 11.25 \text{ V} = 4.75 \text{ V}$
- $V_D = V_{DS} = 4.75 \text{ V}$
- $V_G = V_{GS} = -2 \text{ V}$
- $V_S = 0 \text{ V}$

**Graphical Approach** The resulting Shockley curve and the vertical line at  $V_{GS} = -2 \text{ V}$  are provided in Fig. 7.7. It is certainly difficult to read beyond the second place without



**FIG. 7.7**  
Graphical solution for the network of Fig. 7.6.

significantly increasing the size of the figure, but a solution of 5.6 mA from the graph of Fig. 7.7 is quite acceptable.

a. Therefore,

$$V_{GSQ} = -V_{GG} = -2 \text{ V}$$

b.  $I_{DQ} = 5.6 \text{ mA}$

$$\begin{aligned} c. \quad V_{DS} &= V_{DD} - I_D R_D = 16 \text{ V} - (5.6 \text{ mA})(2 \text{ k}\Omega) \\ &= 16 \text{ V} - 11.2 \text{ V} = 4.8 \text{ V} \end{aligned}$$

d.  $V_D = V_{DS} = 4.8 \text{ V}$

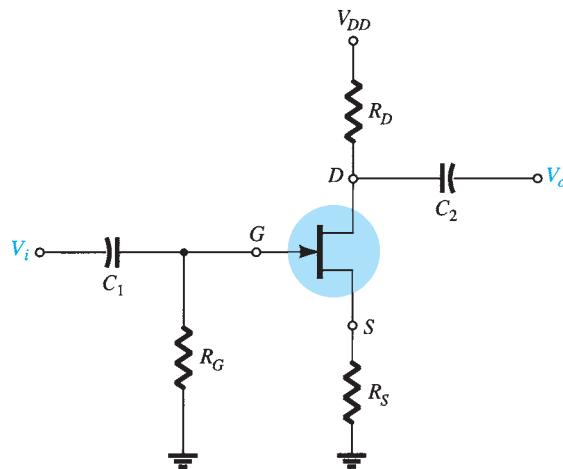
e.  $V_G = V_{GS} = -2 \text{ V}$

f.  $V_S = 0 \text{ V}$

The results clearly confirm the fact that the mathematical and graphical approaches generate solutions that are quite close.

### 7.3 SELF-BIAS CONFIGURATION

The self-bias configuration eliminates the need for two dc supplies. The controlling gate-to-source voltage is now determined by the voltage across a resistor  $R_S$  introduced in the source leg of the configuration as shown in Fig. 7.8.



**FIG. 7.8**  
JFET self-bias configuration.

For the dc analysis, the capacitors can again be replaced by “open circuits” and the resistor  $R_G$  replaced by a short-circuit equivalent since  $I_G = 0 \text{ A}$ . The result is the network of Fig. 7.9 for the important dc analysis.

The current through  $R_S$  is the source current  $I_S$ , but  $I_S = I_D$  and

$$V_{RS} = I_D R_S$$

For the indicated closed loop of Fig. 7.9, we find that

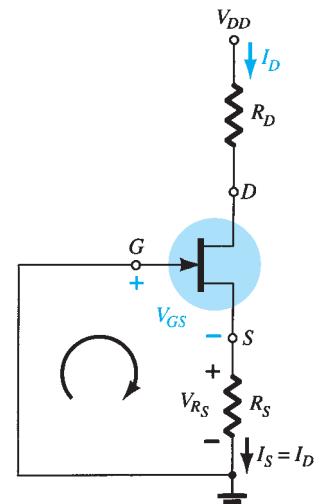
$$-V_{GS} - V_{RS} = 0$$

and

$$V_{GS} = -V_{RS}$$

or

$$V_{GS} = -I_D R_S \quad (7.10)$$



**FIG. 7.9**  
DC analysis of the self-bias configuration.

Note in this case that  $V_{GS}$  is a function of the output current  $I_D$  and not fixed in magnitude as occurred for the fixed-bias configuration.

Equation (7.10) is defined by the network configuration, and Shockley’s equation relates the input and output quantities of the device. Both equations relate the same two variables,  $I_D$  and  $V_{GS}$ , permitting either a mathematical or a graphical solution.

A mathematical solution could be obtained simply by substituting Eq. (7.10) into Shockley's equation as follows:

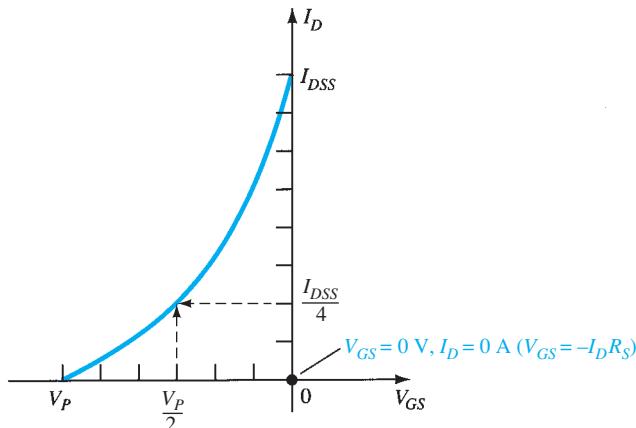
$$\begin{aligned} I_D &= I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 \\ &= I_{DSS} \left( 1 - \frac{-I_D R_S}{V_P} \right)^2 \\ \text{or} \quad I_D &= I_{DSS} \left( 1 + \frac{I_D R_S}{V_P} \right)^2 \end{aligned}$$

By performing the squaring process indicated and rearranging terms, we obtain an equation of the following form:

$$I_D^2 + K_1 I_D + K_2 = 0$$

The quadratic equation can then be solved for the appropriate solution for  $I_D$ .

The sequence above defines the mathematical approach. The graphical approach requires that we first establish the device transfer characteristics as shown in Fig. 7.10. Since Eq. (7.10) defines a straight line on the same graph, let us now identify two points on the graph that are on the line and simply draw a straight line between the two points. The most obvious condition to apply is  $I_D = 0$  A since it results in  $V_{GS} = -I_D R_S = (0 \text{ A})R_S = 0 \text{ V}$ . For Eq. (7.10), therefore, one point on the straight line is defined by  $I_D = 0 \text{ A}$  and  $V_{GS} = 0 \text{ V}$ , as appearing on Fig. 7.10.



**FIG. 7.10**  
Defining a point on the self-bias line.

The second point for Eq. (7.10) requires that a level of  $V_{GS}$  or  $I_D$  be chosen and the corresponding level of the other quantity be determined using Eq. (7.10). The resulting levels of  $I_D$  and  $V_{GS}$  will then define another point on the straight line and permit the drawing of the straight line. Suppose, for example, that we choose a level of  $I_D$  equal to one-half the saturation level. That is,

$$I_D = \frac{I_{DSS}}{2}$$

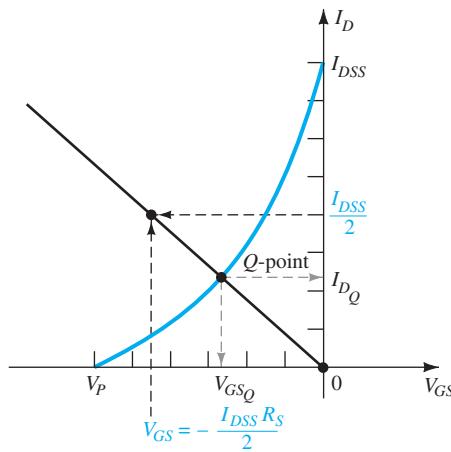
Then  $V_{GS} = -I_D R_S = -\frac{I_{DSS} R_S}{2}$

The result is a second point for the straight-line plot as shown in Fig. 7.11. The straight line as defined by Eq. (7.10) is then drawn and the quiescent point obtained at the intersection of the straight-line plot and the device characteristic curve. The quiescent values of  $I_D$  and  $V_{GS}$  can then be determined and used to find the other quantities of interest.

The level of  $V_{DS}$  can be determined by applying Kirchhoff's voltage law to the output circuit, with the result that

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

and  $V_{DS} = V_{DD} - V_{R_S} - V_{R_D} = V_{DD} - I_S R_S - I_D R_D$



**FIG. 7.11**  
Sketching the self-bias line.

but

$$I_D = I_S$$

and

$$V_{DS} = V_{DD} - I_D(R_S + R_D) \quad (7.11)$$

In addition,

$$V_S = I_D R_S \quad (7.12)$$

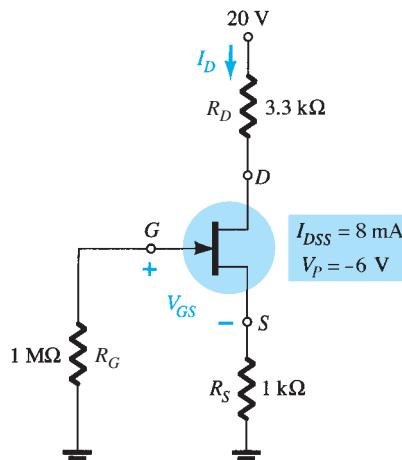
$$V_G = 0 \text{ V} \quad (7.13)$$

and

$$V_D = V_{DS} + V_S = V_{DD} - V_{R_D} \quad (7.14)$$

**EXAMPLE 7.2** Determine the following for the network of Fig. 7.12:

- a.  $V_{GSQ}$ .
- b.  $I_{DQ}$ .
- c.  $V_{DS}$ .
- d.  $V_S$ .
- e.  $V_G$ .
- f.  $V_D$ .



**FIG. 7.12**  
Example 7.2.

**Solution:**

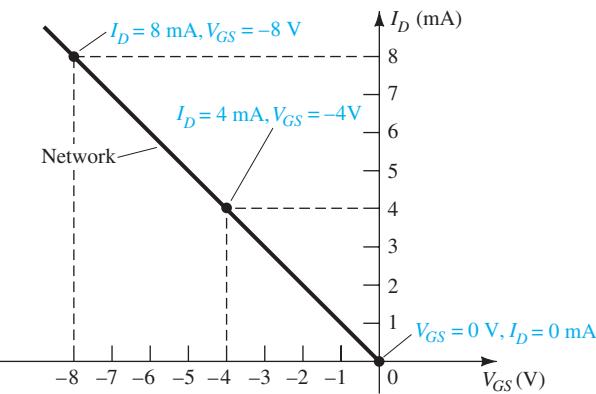
- a. The gate-to-source voltage is determined by

$$V_{GS} = -I_D R_S$$

Choosing  $I_D = 4 \text{ mA}$ , we obtain

$$V_{GS} = -(4 \text{ mA})(1 \text{ k}\Omega) = -4 \text{ V}$$

The result is the plot of Fig. 7.13 as defined by the network.

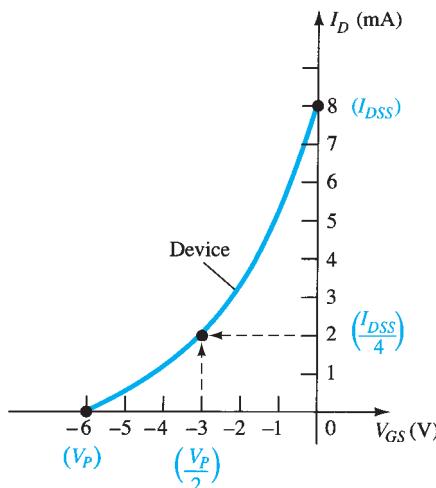


**FIG. 7.13**  
Sketching the self-bias line for the network of Fig. 7.12.

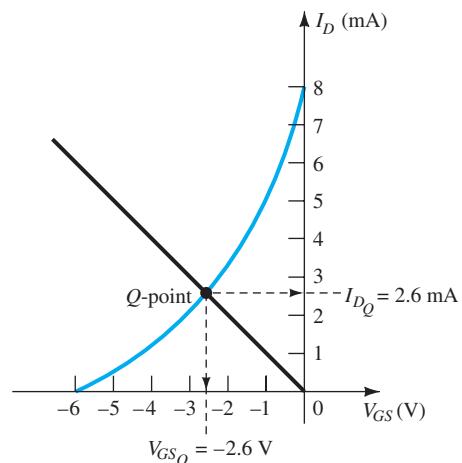
If we happen to choose  $I_D = 8 \text{ mA}$ , the resulting value of  $V_{GS}$  would be  $-8 \text{ V}$ , as shown on the same graph. In either case, the same straight line will result, clearly demonstrating that any appropriate value of  $I_D$  can be chosen as long as the corresponding value of  $V_{GS}$  as determined by Eq. (7.10) is employed. In addition, keep in mind that the value of  $V_{GS}$  could be chosen and the value of  $I_D$  determined graphically.

For Shockley's equation, if we choose  $V_{GS} = V_P/2 = -3 \text{ V}$ , we find that  $I_D = I_{DSS}/4 = 8 \text{ mA}/4 = 2 \text{ mA}$ , and the plot of Fig. 7.14 will result, representing the characteristics of the device. The solution is obtained by superimposing the network characteristics defined by Fig. 7.13 on the device characteristics of Fig. 7.14 and finding the point of intersection of the two as indicated on Fig. 7.15. The resulting operating point results in a quiescent value of gate-to-source voltage of

$$V_{GSQ} = -2.6 \text{ V}$$



**FIG. 7.14**  
Sketching the device characteristics for the JFET of Fig. 7.12.



**FIG. 7.15**  
Determining the *Q*-point for the network of Fig. 7.12.

b. At the quiescent point

$$I_{DQ} = 2.6 \text{ mA}$$

$$\begin{aligned} \text{c. Eq. (7.11): } V_{DS} &= V_{DD} - I_D(R_S + R_D) \\ &= 20 \text{ V} - (2.6 \text{ mA})(1 \text{ k}\Omega + 3.3 \text{ k}\Omega) \\ &= 20 \text{ V} - 11.18 \text{ V} \\ &= 8.82 \text{ V} \end{aligned}$$

d. Eq. (7.12):  $V_S = I_D R_S$   
 $= (2.6 \text{ mA})(1 \text{ k}\Omega)$   
 $= \mathbf{2.6 \text{ V}}$

e. Eq. (7.13):  $V_G = \mathbf{0 \text{ V}}$

f. Eq. (7.14):  $V_D = V_{DS} + V_S = 8.82 \text{ V} + 2.6 \text{ V} = \mathbf{11.42 \text{ V}}$   
or  $V_D = V_{DD} - I_D R_D = 20 \text{ V} - (2.6 \text{ mA})(3.3 \text{ k}\Omega) = \mathbf{11.42 \text{ V}}$

**EXAMPLE 7.3** Find the quiescent point for the network of Fig. 7.12 if:

- a.  $R_S = 100 \Omega$ .  
b.  $R_S = 10 \text{ k}\Omega$ .

**Solution:** Both  $R_S = 100 \Omega$  and  $R_S = 10 \text{ k}\Omega$  are plotted on Fig. 7.16.

- a. For  $R_S = 100 \Omega$ :

$$I_{DQ} \cong \mathbf{6.4 \text{ mA}}$$

and from Eq. (7.10),

$$V_{GSQ} \cong \mathbf{-0.64 \text{ V}}$$

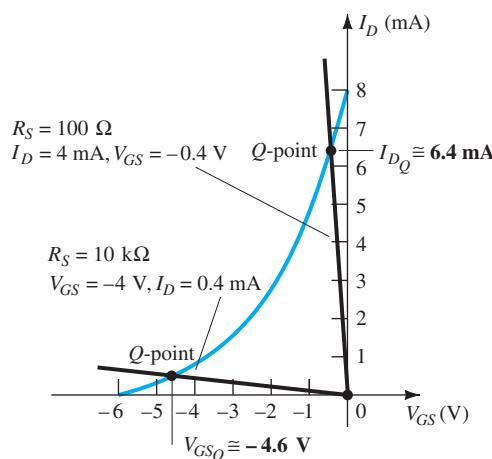
- b. For  $R_S = 10 \text{ k}\Omega$

$$V_{GSQ} \cong \mathbf{-4.6 \text{ V}}$$

and from Eq. (7.10),

$$I_{DQ} \cong \mathbf{0.46 \text{ mA}}$$

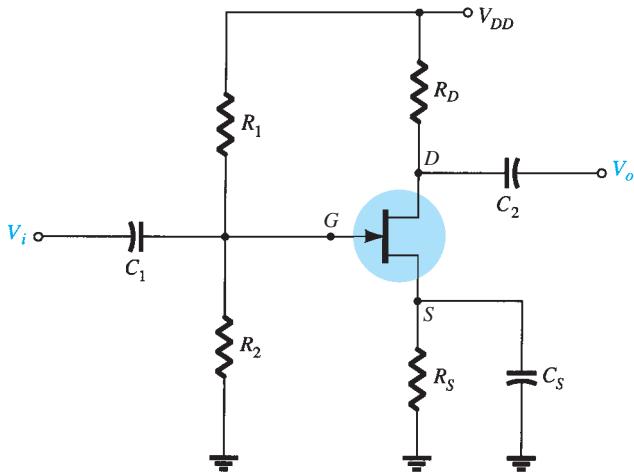
In particular, note how lower levels of  $R_S$  bring the load line of the network closer to the  $I_D$  axis, whereas increasing levels of  $R_S$  bring the load line closer to the  $V_{GS}$  axis.



**FIG. 7.16**  
Example 7.3.

## 7.4 VOLTAGE-DIVIDER BIASING

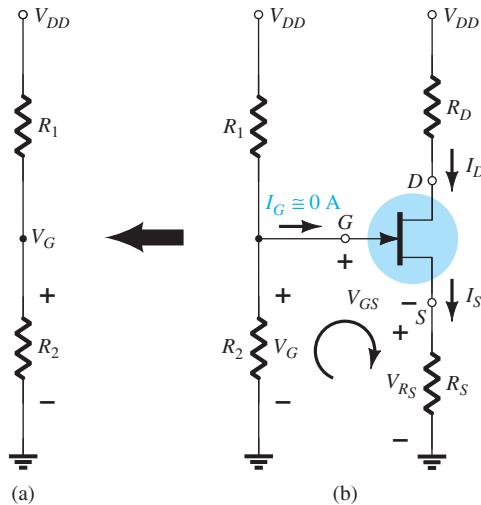
The voltage-divider bias arrangement applied to BJT transistor amplifiers is also applied to FET amplifiers as demonstrated by Fig. 7.17. The basic construction is exactly the same, but the dc analysis of each is quite different.  $I_G = 0 \text{ A}$  for FET amplifiers, but the magnitude of  $I_B$  for common-emitter BJT amplifiers can affect the dc levels of current and voltage in both the input and output circuits. Recall that  $I_B$  provides the link between input and output circuits for the BJT voltage-divider configuration, whereas  $V_{GS}$  does the same for the FET configuration.



**FIG. 7.17**  
Voltage-divider bias arrangement.

The network of Fig. 7.17 is redrawn as shown in Fig. 7.18 for the dc analysis. Note that all the capacitors, including the bypass capacitor  $C_S$ , have been replaced by an “open-circuit” equivalent in Fig. 7.18b. In addition, the source  $V_{DD}$  was separated into two equivalent sources to permit a further separation of the input and output regions of the network. Since  $I_G = 0 \text{ A}$ , Kirchhoff’s current law requires that  $I_{R_1} = I_{R_2}$ , and the series equivalent circuit appearing to the left of the figure can be used to find the level of  $V_G$ . The voltage  $V_G$ , equal to the voltage across  $R_2$ , can be found using the voltage-divider rule and Fig. 7.18a as follows:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} \quad (7.15)$$



**FIG. 7.18**  
Redrawn network of Fig. 7.17 for dc analysis.

Applying Kirchhoff’s voltage law in the clockwise direction to the indicated loop of Fig. 7.18 results in

$$V_G - V_{GS} - V_{RS} = 0$$

and

$$V_{GS} = V_G - V_{RS}$$

Substituting  $V_{RS} = I_S R_S = I_D R_S$ , we have

$$V_{GS} = V_G - I_D R_S \quad (7.16)$$

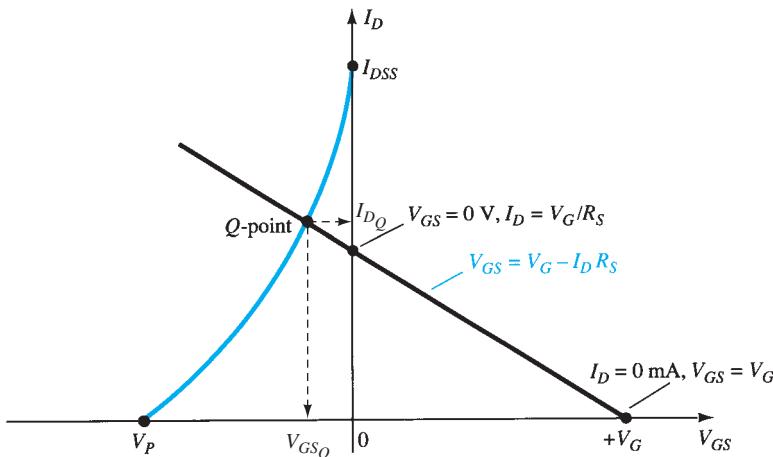
The result is an equation that continues to include the same two variables appearing in Shockley's equation:  $V_{GS}$  and  $I_D$ . The quantities  $V_G$  and  $R_S$  are fixed by the network construction. Equation (7.16) is still the equation for a straight line, but the origin is no longer a point in the plotting of the line. The procedure for plotting Eq. (7.16) is not a difficult one and will proceed as follows. Since any straight line requires two points to be defined, let us first use the fact that anywhere on the horizontal axis of Fig. 7.19 the current  $I_D = 0$  mA. If we therefore select  $I_D$  to be 0 mA, we are in essence stating that we are somewhere on the horizontal axis. The exact location can be determined simply by substituting  $I_D = 0$  mA into Eq. (7.16) and finding the resulting value of  $V_{GS}$  as follows:

$$\begin{aligned} V_{GS} &= V_G - I_D R_S \\ &= V_G - (0 \text{ mA}) R_S \end{aligned}$$

and

$$V_{GS} = V_G \Big|_{I_D=0 \text{ mA}} \quad (7.17)$$

The result specifies that whenever we plot Eq. (7.16), if we choose  $I_D = 0$  mA, the value of  $V_{GS}$  for the plot will be  $V_G$  volts. The point just determined appears in Fig. 7.19.



**FIG. 7.19**

Sketching the network equation for the voltage-divider configuration.

For the other point, let us now employ the fact that at any point on the vertical axis  $V_{GS} = 0$  V and solve for the resulting value of  $I_D$ :

$$\begin{aligned} V_{GS} &= V_G - I_D R_S \\ 0 \text{ V} &= V_G - I_D R_S \end{aligned}$$

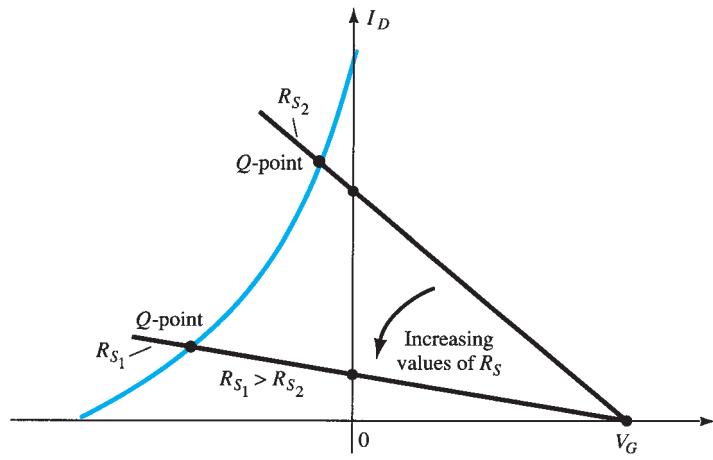
and

$$I_D = \frac{V_G}{R_S} \Big|_{V_{GS}=0 \text{ V}} \quad (7.18)$$

The result specifies that whenever we plot Eq. (7.16), if  $V_{GS} = 0$  V, the level of  $I_D$  is determined by Eq. (7.18). This intersection also appears on Fig. 7.19.

The two points defined above permit the drawing of a straight line to represent Eq. (7.16). The intersection of the straight line with the transfer curve in the region to the left of the vertical axis will define the operating point and the corresponding levels of  $I_D$  and  $V_{GS}$ .

Since the intersection on the vertical axis is determined by  $I_D = V_G / R_S$  and  $V_G$  is fixed by the input network, increasing values of  $R_S$  will reduce the level of the  $I_D$  intersection as



**FIG. 7.20**  
Effect of  $R_S$  on the resulting  $Q$ -point.

shown in Fig. 7.20. It is fairly obvious from Fig. 7.20 that:

**Increasing values of  $R_S$  result in lower quiescent values of  $I_D$  and declining values of  $V_{GS}$ .**

Once the quiescent values of  $I_{DQ}$  and  $V_{GSQ}$  are determined, the remaining network analysis can be performed in the usual manner. That is,

$$V_{DS} = V_{DD} - I_D(R_D + R_S) \quad (7.19)$$

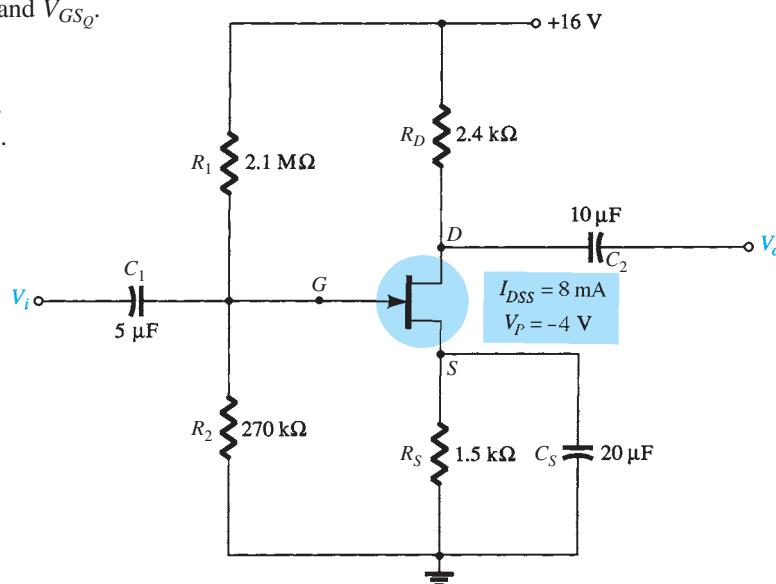
$$V_D = V_{DD} - I_D R_D \quad (7.20)$$

$$V_S = I_D R_S \quad (7.21)$$

$$I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2} \quad (7.22)$$

**EXAMPLE 7.4** Determine the following for the network of Fig. 7.21:

- a.  $I_{DQ}$  and  $V_{GSQ}$ .
- b.  $V_D$ .
- c.  $V_S$ .
- d.  $V_{DS}$ .
- e.  $V_{DG}$ .



**FIG. 7.21**  
Example 7.4.

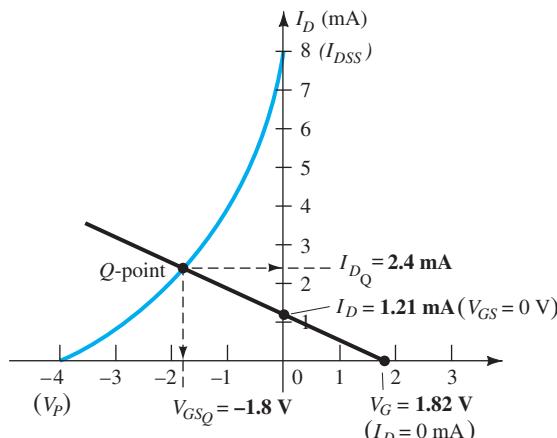
**Solution:**

- a. For the transfer characteristics, if  $I_D = I_{DSS}/4 = 8 \text{ mA}/4 = 2 \text{ mA}$ , then  $V_{GS} = V_P/2 = -4 \text{ V}/2 = -2 \text{ V}$ . The resulting curve representing Shockley's equation appears in Fig. 7.22. The network equation is defined by

$$\begin{aligned} V_G &= \frac{R_2 V_{DD}}{R_1 + R_2} \\ &= \frac{(270 \text{ k}\Omega)(16 \text{ V})}{2.1 \text{ M}\Omega + 0.27 \text{ M}\Omega} \\ &= 1.82 \text{ V} \end{aligned}$$

and

$$\begin{aligned} V_{GS} &= V_G - I_D R_S \\ &= 1.82 \text{ V} - I_D(1.5 \text{ k}\Omega) \end{aligned}$$



**FIG. 7.22**

Determining the *Q*-point for the network of Fig. 7.21.

When  $I_D = 0 \text{ mA}$ ,

$$V_{GS} = +1.82 \text{ V}$$

When  $V_{GS} = 0 \text{ V}$ ,

$$I_D = \frac{1.82 \text{ V}}{1.5 \text{ k}\Omega} = 1.21 \text{ mA}$$

The resulting bias line appears on Fig. 7.22 with quiescent values of

$$I_{DQ} = 2.4 \text{ mA}$$

and

$$V_{GSQ} = -1.8 \text{ V}$$

b.  $V_D = V_{DD} - I_D R_D$

$$= 16 \text{ V} - (2.4 \text{ mA})(2.4 \text{ k}\Omega)$$

$$= 10.24 \text{ V}$$

c.  $V_S = I_D R_S = (2.4 \text{ mA})(1.5 \text{ k}\Omega)$

$$= 3.6 \text{ V}$$

d.  $V_{DS} = V_{DD} - I_D(R_D + R_S)$

$$= 16 \text{ V} - (2.4 \text{ mA})(2.4 \text{ k}\Omega + 1.5 \text{ k}\Omega)$$

$$= 6.64 \text{ V}$$

or  $V_{DS} = V_D - V_S = 10.24 \text{ V} - 3.6 \text{ V}$

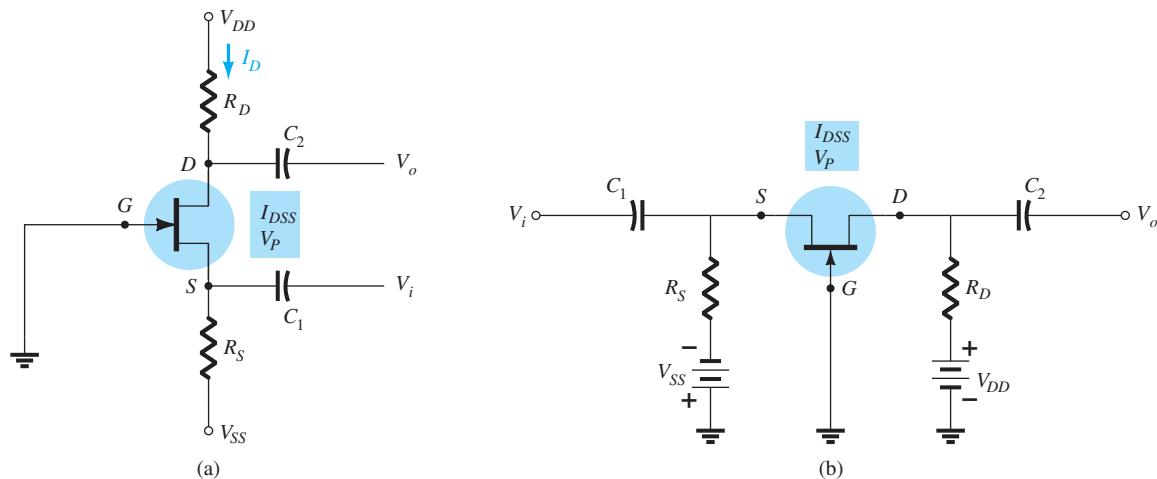
$$= 6.64 \text{ V}$$

e. Although seldom requested, the voltage  $V_{DG}$  can easily be determined using

$$\begin{aligned} V_{DG} &= V_D - V_G \\ &= 10.24 \text{ V} - 1.82 \text{ V} \\ &= \mathbf{8.42 \text{ V}} \end{aligned}$$

## 7.5 COMMON-GATE CONFIGURATION

The next configuration is one in which the gate terminal is grounded and the input signal typically applied to the source terminal and the output signal obtained at the drain terminal as shown in Fig. 7.23a. The network can also be drawn as shown in Fig. 7.23b.



**FIG. 7.23**  
Two versions of the common-gate configuration.

The network equation can be determined using Fig. 7.24.

Applying Kirchhoff's voltage law in the direction shown in Fig. 7.24 will result in

$$-V_{GS} - I_S R_S + V_{SS} = 0$$

$$V_{GS} = V_{SS} - I_S R_S$$

$$I_S = I_D$$

so

$$V_{GS} = V_{SS} - I_D R_S \quad (7.23)$$

Applying the condition  $I_D = 0 \text{ mA}$  to Eq. 7.23 will result in

$$V_{GS} = V_{SS} - (0)R_S$$

and

$$V_{GS} = V_{SS}|_{I_D=0\text{mA}} \quad (7.24)$$

Applying the condition  $V_{GS} = 0 \text{ V}$  to Eq. 7.23 will result in

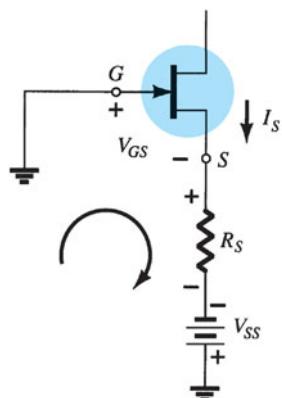
$$0 = V_{SS} - I_D R_S$$

and

$$I_D = \frac{V_{SS}}{R_S} \Big|_{V_{GS}=0\text{V}} \quad (7.25)$$

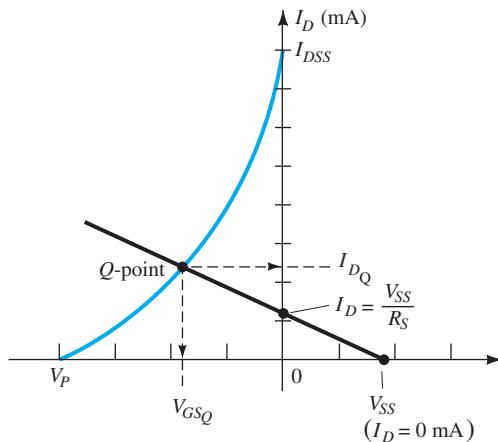
The resulting load-line appears in Fig. 7.25 intersecting the transfer curve for the JFET as shown in the figure.

The resulting intersection defines the operating current  $I_{DQ}$  and voltage  $V_{DQ}$  for the network as also indicated in the network.



**FIG. 7.24**

Determining the network equation for the configuration of Fig. 7.23.

**FIG. 7.25**

Determining the *Q*-point for the network of Fig. 7.24.

Applying Kirchhoff's voltage law around the loop containing the two sources, the JFET and the resistors  $R_D$  and  $R_S$  in Fig. 7.23a and Fig. 7.23b will result in

$$+V_{DD} - I_D R_D - V_{DS} - I_S R_S + V_{SS} = 0$$

Substituting  $I_S = I_D$  we have

$$+V_{DD} + V_{SS} - V_{DS} - I_D(R_D + R_S) = 0$$

so that

$$V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S) \quad (7.26)$$

with

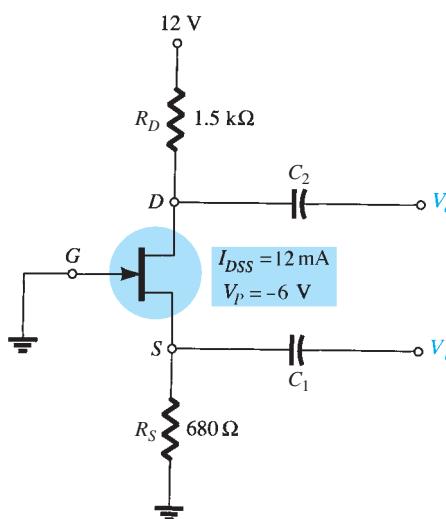
$$V_D = V_{DD} - I_D R_D \quad (7.27)$$

and

$$V_S = -V_{SS} + I_D R_S \quad (7.28)$$

**EXAMPLE 7.5** Determine the following for the common-gate configuration of Fig. 7.26:

- $V_{GSQ}$
- $I_{DQ}$
- $V_D$
- $V_G$
- $V_S$
- $V_{DS}$

**FIG. 7.26**

Example 7.5.

**Solution:** Even though  $V_{SS}$  is not present in this common-gate configuration the equations derived above can still be used by simply substituting  $V_{SS} = 0$  V into each equation in which it appears.

a. For the transfer characteristics Eq. 7.23 becomes

$$V_{GS} = 0 - I_D R_S$$

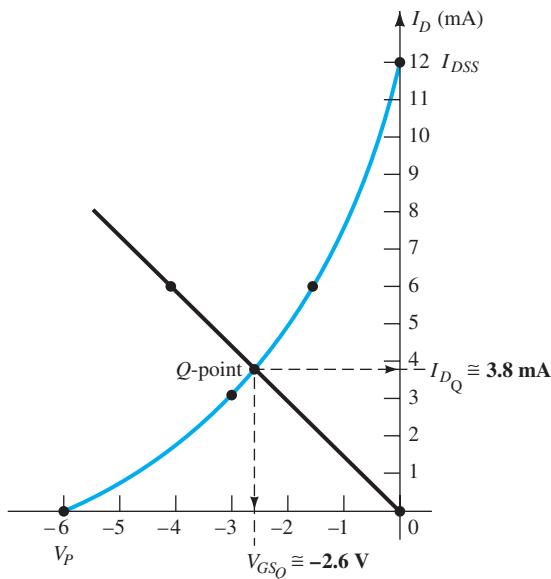
and

$$V_{GS} = -I_D R_S$$

For this equation the origin is one point on the load line while the other must be determined at some arbitrary point. Choosing  $I_D = 6$  mA and solving for  $V_{GS}$  will result in the following:

$$V_{GS} = -I_D R_S = -(6 \text{ mA})(680 \Omega) = -4.08 \text{ V}$$

as shown in Fig. 7.27.



**FIG. 7.27**  
Determining the  $Q$ -point for the network of Fig. 7.26.

The device transfer curve is sketched using

$$I_D = \frac{I_{DSS}}{4} = \frac{12 \text{ mA}}{4} = 3 \text{ mA} (\text{at } V_P/2)$$

and  $V_{GS} \cong 0.3V_P = 0.3(-6 \text{ V}) = -1.8 \text{ V}$  (at  $I_D = I_{DSS}/2$ )

The resulting solution is:

$$V_{GS_Q} \cong -2.6 \text{ V}$$

b. From Fig. 7.27,

$$I_{D_Q} \cong 3.8 \text{ mA}$$

c.  $V_D = V_{DD} - I_D R_D$

$$= 12 \text{ V} - (3.8 \text{ mA})(1.5 \text{ k}\Omega) = 12 \text{ V} - 5.7 \text{ V}$$

$$= 6.3 \text{ V}$$

d.  $V_G = 0 \text{ V}$

e.  $V_S = I_D R_S = (3.8 \text{ mA})(680 \Omega)$

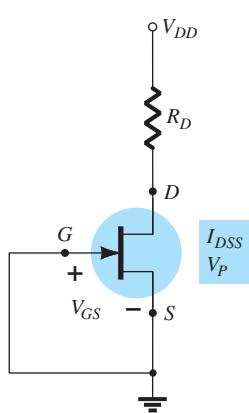
$$= 2.58 \text{ V}$$

f.  $V_{DS} = V_D - V_S$

$$= 6.3 \text{ V} - 2.58 \text{ V}$$

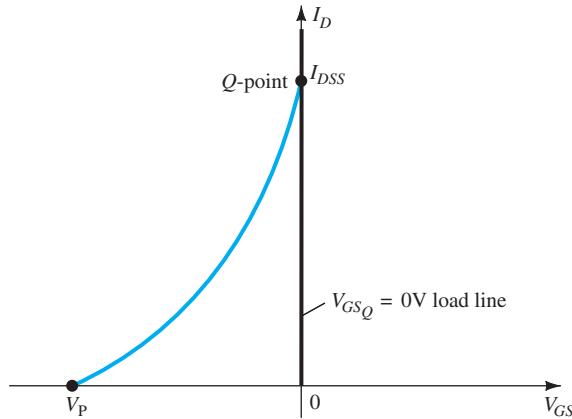
$$= 3.72 \text{ V}$$

A network of recurring practical value because of its relative simplicity is the configuration of Fig. 7.28. Note that direct connection of the gate and source terminals to ground resulting in  $V_{GS} = 0$  V. It specifies that for any dc condition the gate to source voltage must be zero volts. This will result in a vertical load line at  $V_{GSQ} = 0$  V as shown in Fig. 7.29.



**FIG. 7.28**

Special case  $V_{GSQ} = 0$  V configuration.



**FIG. 7.29**

Finding the Q-point for the network of Fig. 7.28.

Since the transfer curve of a JFET will cross the vertical axis at  $I_{DS}$  the drain current for the network is set at that level.

Therefore,

$$I_{DQ} = I_{DS} \quad (7.29)$$

Applying Kirchhoff's voltage law:

$$V_{DD} - I_D R_D - V_{DS} = 0$$

and

$$V_{DS} = V_{DD} - I_D R_D \quad (7.30)$$

with

$$V_D = V_{DS} \quad (7.31)$$

and

$$V_S = 0 \text{ V} \quad (7.32)$$

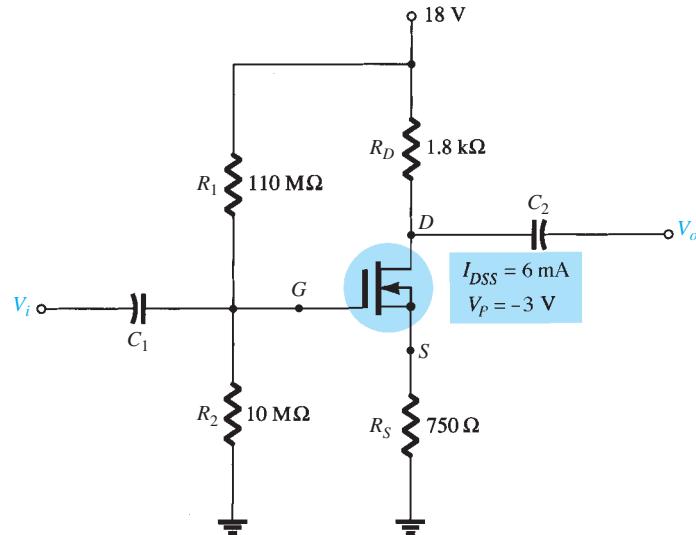
## 7.7 DEPLETION-TYPE MOSFETS

The similarities in appearance between the transfer curves of JFETs and depletion-type MOSFETs permit a similar analysis of each in the dc domain. The primary difference between the two is the fact that depletion-type MOSFETs permit operating points with positive values of  $V_{GS}$  and levels of  $I_D$  that exceed  $I_{DS}$ . In fact, for all the configurations discussed thus far, the analysis is the same if the JFET is replaced by a depletion-type MOSFET.

The only undefined part of the analysis is how to plot Shockley's equation for positive values of  $V_{GS}$ . How far into the region of positive values of  $V_{GS}$  and values of  $I_D$  greater than  $I_{DS}$  does the transfer curve have to extend? For most situations, this required range will be fairly well defined by the MOSFET parameters and the resulting bias line of the network. A few examples will reveal the effect of the change in device on the resulting analysis.

**EXAMPLE 7.6** For the *n*-channel depletion-type MOSFET of Fig. 7.30, determine:

- $I_{DQ}$  and  $V_{GSQ}$ .
- $V_{DS}$ .

**FIG. 7.30**

Example 7.6.

**Solution:**

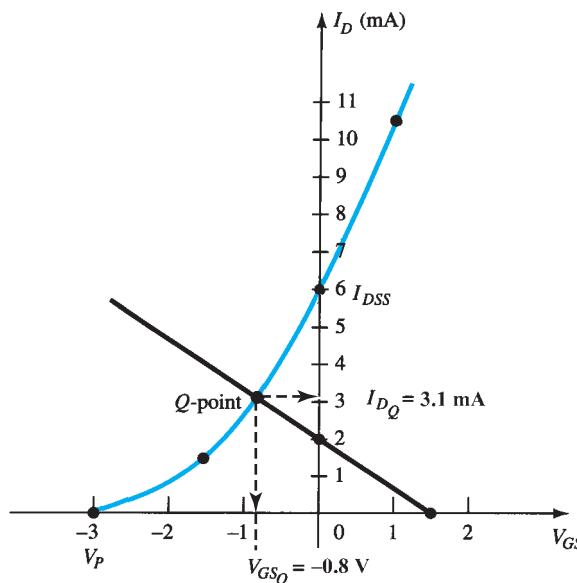
- a. For the transfer characteristics, a plot point is defined by  $I_D = I_{DSS}/4 = 6 \text{ mA}/4 = 1.5 \text{ mA}$  and  $V_{GS} = V_P/2 = -3 \text{ V}/2 = -1.5 \text{ V}$ . Considering the level of  $V_P$  and the fact that Shockley's equation defines a curve that rises more rapidly as  $V_{GS}$  becomes more positive, a plot point will be defined at  $V_{GS} = +1 \text{ V}$ . Substituting into Shockley's equation yields

$$\begin{aligned} I_D &= I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 \\ &= 6 \text{ mA} \left( 1 - \frac{+1 \text{ V}}{-3 \text{ V}} \right)^2 = 6 \text{ mA} \left( 1 + \frac{1}{3} \right)^2 = 6 \text{ mA} (1.778) \\ &= 10.67 \text{ mA} \end{aligned}$$

The resulting transfer curve appears in Fig. 7.31. Proceeding as described for JFETs, we have

$$\text{Eq. (7.15): } V_G = \frac{10 \text{ M}\Omega (18 \text{ V})}{10 \text{ M}\Omega + 110 \text{ M}\Omega} = 1.5 \text{ V}$$

$$\text{Eq. (7.16): } V_{GS} = V_G - I_D R_S = 1.5 \text{ V} - I_D (750 \Omega)$$

**FIG. 7.31**Determining the  $Q$ -point for the network of Fig. 7.30.

Setting  $I_D = 0$  mA results in

$$V_{GS} = V_G = 1.5 \text{ V}$$

Setting  $V_{GS} = 0$  V yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5 \text{ V}}{750 \Omega} = 2 \text{ mA}$$

The plot points and resulting bias line appear in Fig. 7.31. The resulting operating point is given by

$$I_{DQ} = 3.1 \text{ mA}$$

$$V_{GSQ} = -0.8 \text{ V}$$

b. Eq. (7.19):

$$\begin{aligned} V_{DS} &= V_{DD} - I_D(R_D + R_S) \\ &= 18 \text{ V} - (3.1 \text{ mA})(1.8 \text{ k}\Omega + 750 \Omega) \\ &\cong 10.1 \text{ V} \end{aligned}$$

**EXAMPLE 7.7** Repeat Example 7.6 with  $R_S = 150 \Omega$ .

**Solution:**

a. The plot points are the same for the transfer curve as shown in Fig. 7.32. For the bias line,

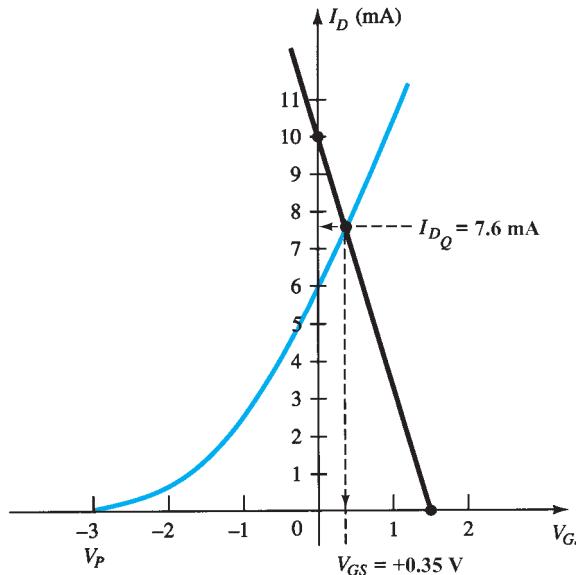
$$V_{GS} = V_G - I_D R_S = 1.5 \text{ V} - I_D(150 \Omega)$$

Setting  $I_D = 0$  mA results in

$$V_{GS} = 1.5 \text{ V}$$

Setting  $V_{GS} = 0$  V yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5 \text{ V}}{150 \Omega} = 10 \text{ mA}$$



**FIG. 7.32**  
Example 7.7.

The bias line is included on Fig. 7.32. Note in this case that the quiescent point results in a drain current that exceeds  $I_{DSS}$ , with a positive value for  $V_{GS}$ . The result is

$$I_{DQ} = 7.6 \text{ mA}$$

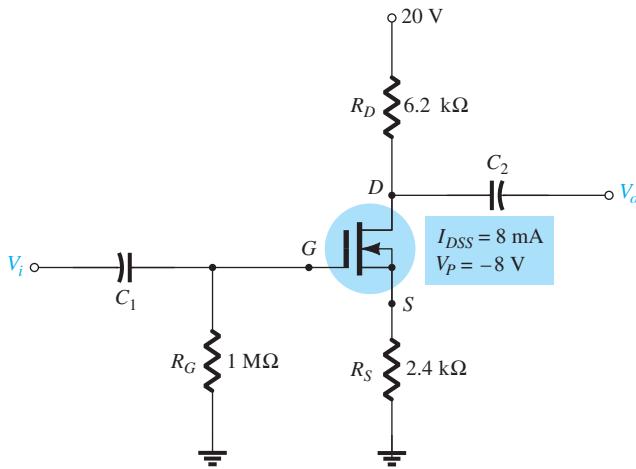
$$V_{GSQ} = +0.35 \text{ V}$$

b. Eq. (7.19):

$$\begin{aligned} V_{DS} &= V_{DD} - I_D(R_D + R_S) \\ &= 18 \text{ V} - (7.6 \text{ mA})(1.8 \text{ k}\Omega + 150 \Omega) \\ &= 3.18 \text{ V} \end{aligned}$$

**EXAMPLE 7.8** Determine the following for the network of Fig. 7.33:

- $I_{DQ}$  and  $V_{GSQ}$
- $V_D$ .



**FIG. 7.33**

Example 7.8.

**Solution:**

- The self-bias configuration results in

$$V_{GS} = -I_D R_S$$

as obtained for the JFET configuration, establishing the fact that  $V_{GS}$  must be less than 0 V. There is therefore no requirement to plot the transfer curve for positive values of  $V_{GS}$ , although it was done on this occasion to complete the transfer characteristics. A plot point for the transfer characteristics for  $V_{GS} < 0$  V is

$$I_D = \frac{I_{DSS}}{4} = \frac{8 \text{ mA}}{4} = 2 \text{ mA}$$

$$\text{and } V_{GS} = \frac{V_P}{2} = \frac{-8 \text{ V}}{2} = -4 \text{ V}$$

and for  $V_{GS} > 0$  V, since  $V_P = -8$  V, we will choose

$$V_{GS} = +2 \text{ V}$$

$$\begin{aligned} \text{and } I_D &= I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 = 8 \text{ mA} \left( 1 - \frac{+2 \text{ V}}{-8 \text{ V}} \right)^2 \\ &= 12.5 \text{ mA} \end{aligned}$$

The resulting transfer curve appears in Fig. 7.34. For the network bias line, at  $V_{GS} = 0$  V,  $I_D = 0$  mA. Choosing  $V_{GS} = -6$  V gives

$$I_D = -\frac{V_{GS}}{R_S} = -\frac{-6 \text{ V}}{2.4 \text{ k}\Omega} = 2.5 \text{ mA}$$

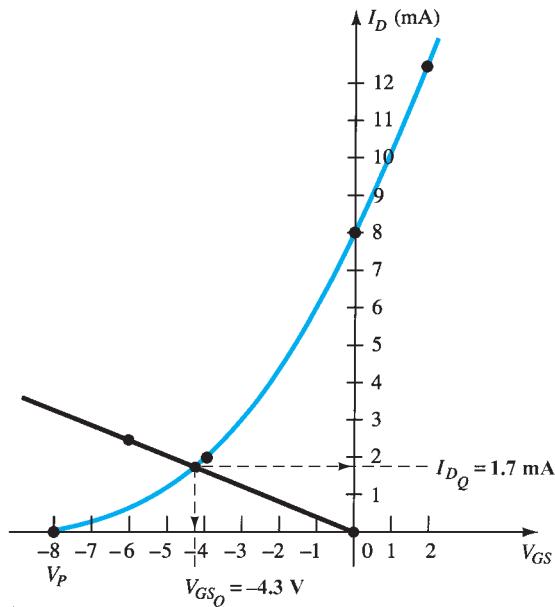
The resulting Q-point is given by

$$I_{DQ} = 1.7 \text{ mA}$$

$$V_{GSQ} = -4.3 \text{ V}$$

$$\begin{aligned} \text{b. } V_D &= V_{DD} - I_D R_D \\ &= 20 \text{ V} - (1.7 \text{ mA})(6.2 \text{ k}\Omega) \\ &= 9.46 \text{ V} \end{aligned}$$

The example to follow employs a design that can also be applied to JFET transistors. At first impression it appears rather simplistic, but in fact it often causes some confusion when first analyzed due to the special point of operation.



**FIG. 7.34**  
Determining the *Q*-point for the network of Fig. 7.33.

**EXAMPLE 7.9** Determine  $V_{DS}$  for the network of Fig. 7.35.

**Solution:** The direct connection between the gate and source terminals requires that

$$V_{GS} = 0 \text{ V}$$

Since  $V_{GS}$  is fixed at 0 V, the drain current must be  $I_{DSS}$  (by definition). In other words,

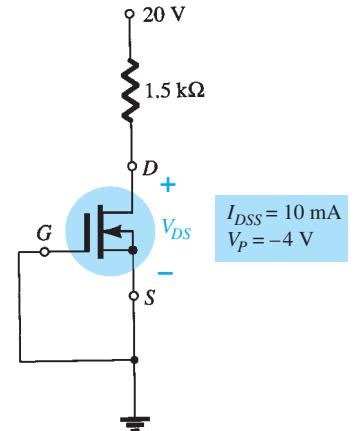
$$V_{GSQ} = 0 \text{ V}$$

and

$$I_{DQ} = 10 \text{ mA}$$

There is therefore no need to draw the transfer curve, and

$$\begin{aligned} V_D &= V_{DD} - I_D R_D = 20 \text{ V} - (10 \text{ mA})(1.5 \text{ k}\Omega) \\ &= 20 \text{ V} - 15 \text{ V} \\ &= 5 \text{ V} \end{aligned}$$



**FIG. 7.35**  
Example 7.9.

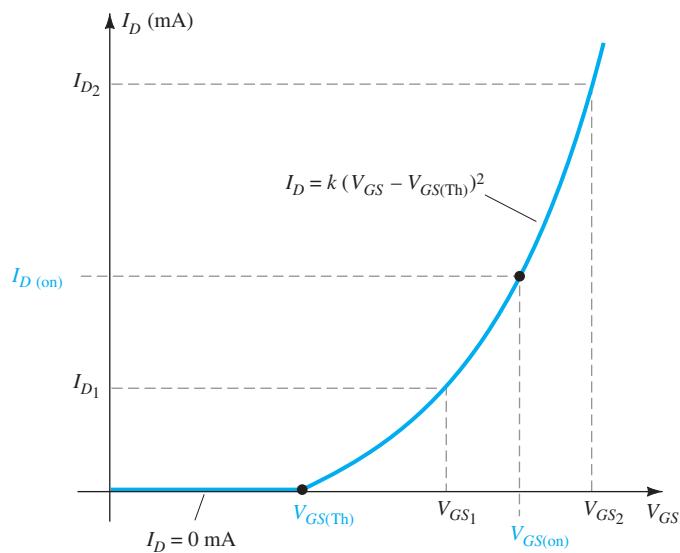
## 7.8 ENHANCEMENT-TYPE MOSFETS

The transfer characteristics of the enhancement-type MOSFET are quite different from those encountered for the JFET and depletion-type MOSFETs, resulting in a graphical solution quite different from those of the preceding sections. First and foremost, recall that for the *n*-channel enhancement-type MOSFET, the drain current is zero for levels of gate-to-source voltage less than the threshold level  $V_{GS(Th)}$ , as shown in Fig. 7.36. For levels of  $V_{GS}$  greater than  $V_{GS(Th)}$ , the drain current is defined by

$$I_D = k(V_{GS} - V_{GS(Th)})^2 \quad (7.33)$$

Since specification sheets typically provide the threshold voltage and a level of drain current ( $I_{D(on)}$ ) and its corresponding level of  $V_{GS(on)}$ , two points are defined immediately as shown in Fig. 7.36. To complete the curve, the constant  $k$  of Eq. (7.33) must be determined from the specification sheet data by substituting into Eq. (7.33) and solving for  $k$  as follows:

$$\begin{aligned} I_D &= k(V_{GS} - V_{GS(Th)})^2 \\ I_{D(on)} &= k(V_{GS(on)} - V_{GS(Th)})^2 \end{aligned}$$



**FIG. 7.36**  
Transfer characteristics of an n-channel enhancement-type MOSFET.

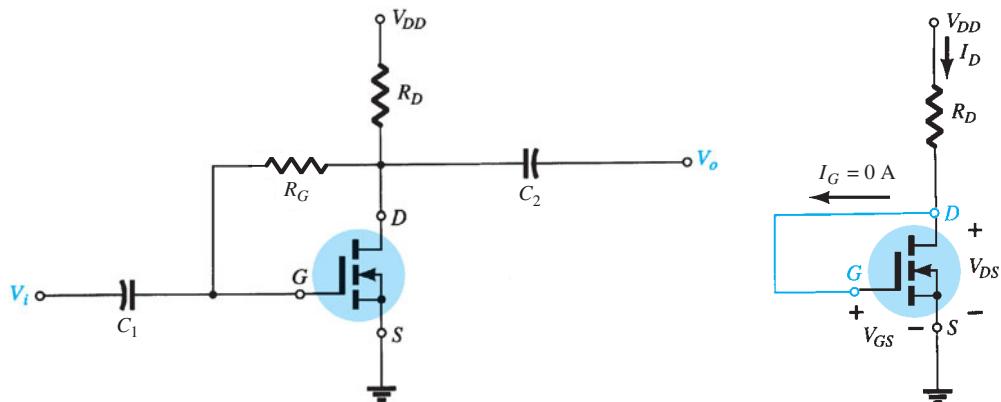
and

$$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2} \quad (7.34)$$

Once  $k$  is defined, other levels of  $I_D$  can be determined for chosen values of  $V_{GS}$ . Typically, a point between  $V_{GS(\text{Th})}$  and  $V_{GS(\text{on})}$  and one just greater than  $V_{GS(\text{on})}$  will provide a sufficient number of points to plot Eq. (7.33) (note  $I_{D_1}$  and  $I_{D_2}$  on Fig. 7.36).

### Feedback Biasing Arrangement

A popular biasing arrangement for enhancement-type MOSFETs is provided in Fig. 7.37. The resistor  $R_G$  brings a suitably large voltage to the gate to drive the MOSFET “on.” Since  $I_G = 0 \text{ mA}$ ,  $V_{R_G} = 0 \text{ V}$  and the dc equivalent network appears as shown in Fig. 7.38.



**FIG. 7.37**  
Feedback biasing arrangement.  
**FIG. 7.38**  
DC equivalent of the network of Fig. 7.37.

A direct connection now exists between drain and gate, resulting in

$$V_D = V_G$$

and

$$V_{DS} = V_{GS} \quad (7.35)$$

For the output circuit,

$$V_{DS} = V_{DD} - I_D R_D$$

which becomes the following after substituting Eq. (7.27):

$$V_{GS} = V_{DD} - I_D R_D \quad (7.36)$$

The result is an equation that relates  $I_D$  to  $V_{GS}$ , permitting the plot of both on the same set of axes.

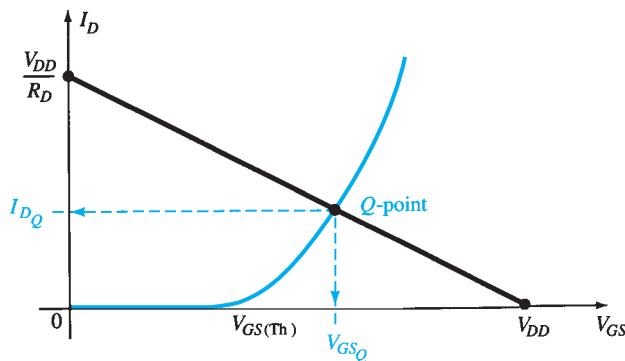
Since Eq. (7.36) is that of a straight line, the same procedure described earlier can be employed to determine the two points that will define the plot on the graph. Substituting  $I_D = 0$  mA into Eq. (7.36) gives

$$V_{GS} = V_{DD}|_{I_D=0 \text{ mA}} \quad (7.37)$$

Substituting  $V_{GS} = 0$  V into Eq. (7.36), we have

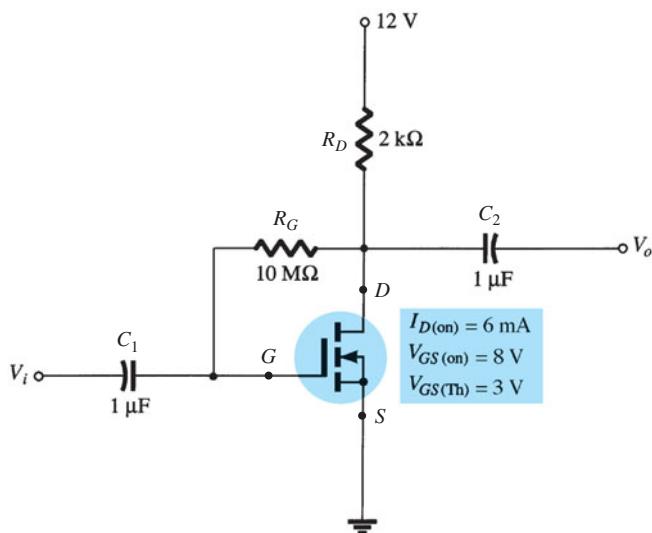
$$I_D = \frac{V_{DD}}{R_D} \Big|_{V_{GS}=0 \text{ V}} \quad (7.38)$$

The plots defined by Eqs. (7.33) and (7.36) appear in Fig. 7.39 with the resulting operating point.



**FIG. 7.39**  
Determining the *Q*-point for the network of Fig. 7.37.

**EXAMPLE 7.10** Determine  $I_{D_Q}$  and  $V_{DS_Q}$  for the enhancement-type MOSFET of Fig. 7.40.

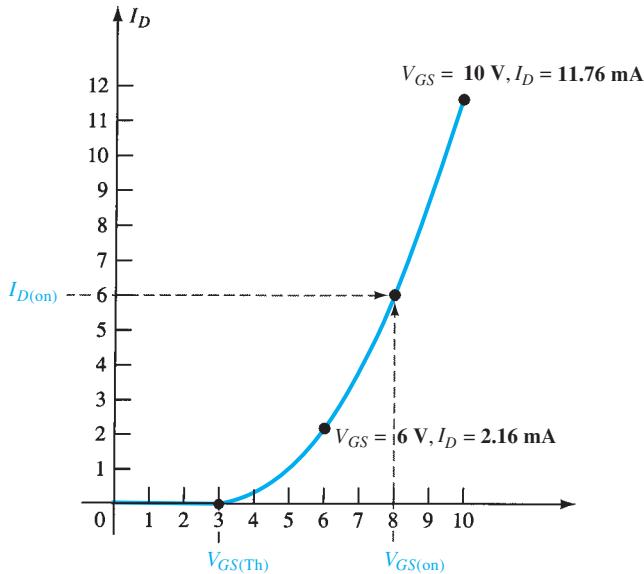


**FIG. 7.40**  
Example 7.10.

**Solution:**

**Plotting the Transfer Curve** Two points are defined immediately as shown in Fig. 7.41. Solving for  $k$ , we obtain

$$\begin{aligned} \text{Eq. (7.34): } k &= \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2} \\ &= \frac{6 \text{ mA}}{(8 \text{ V} - 3 \text{ V})^2} = \frac{6 \times 10^{-3}}{25} \text{ A/V}^2 \\ &= \mathbf{0.24 \times 10^{-3} \text{ A/V}^2} \end{aligned}$$



**FIG. 7.41**  
Plotting the transfer curve for the MOSFET of Fig. 7.40.

For  $V_{GS} = 6 \text{ V}$  (between 3 and 8 V):

$$\begin{aligned} I_D &= 0.24 \times 10^{-3}(6 \text{ V} - 3 \text{ V})^2 = 0.24 \times 10^{-3}(9) \\ &= 2.16 \text{ mA} \end{aligned}$$

as shown on Fig. 7.41. For  $V_{GS} = 10 \text{ V}$  (slightly greater than  $V_{GS(\text{Th})}$ ),

$$\begin{aligned} I_D &= 0.24 \times 10^{-3}(10 \text{ V} - 3 \text{ V})^2 = 0.24 \times 10^{-3}(49) \\ &= 11.76 \text{ mA} \end{aligned}$$

as also appearing on Fig. 7.41. The four points are sufficient to plot the full curve for the range of interest as shown in Fig. 7.41.

**For the Network Bias Line**

$$\begin{aligned} V_{GS} &= V_{DD} - I_D R_D \\ &= 12 \text{ V} - I_D(2 \text{ k}\Omega) \\ \text{Eq. (7.37): } V_{GS} &= V_{DD} = 12 \text{ V} |_{I_D=0 \text{ mA}} \end{aligned}$$

$$\text{Eq. (7.38): } I_D = \frac{V_{DD}}{R_D} = \frac{12 \text{ V}}{2 \text{ k}\Omega} = 6 \text{ mA} |_{V_{GS}=0 \text{ V}}$$

The resulting bias line appears in Fig. 7.42.

At the operating point,

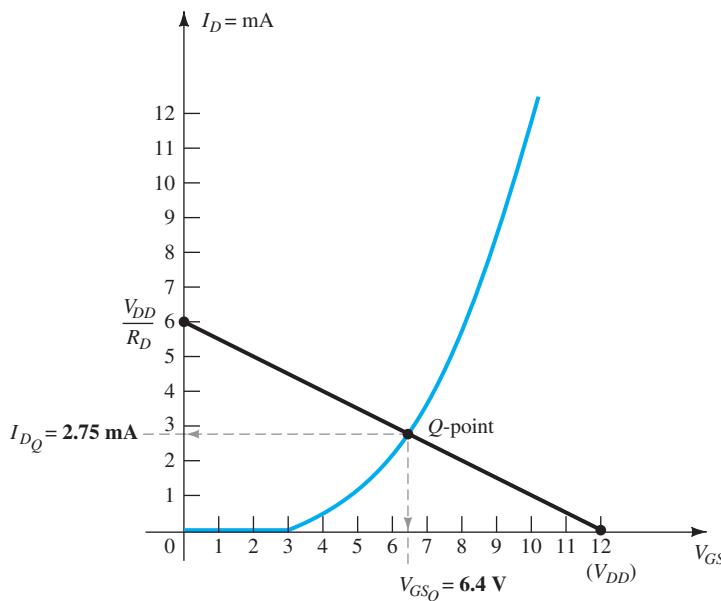
$$I_{D_Q} = \mathbf{2.75 \text{ mA}}$$

and

$$V_{GS_Q} = 6.4 \text{ V}$$

with

$$V_{DS_Q} = V_{GS_Q} = \mathbf{6.4 \text{ V}}$$



**FIG. 7.42**  
Determining the *Q*-point for the network of Fig. 7.40.

### Voltage-Divider Biasing Arrangement

A second popular biasing arrangement for the enhancement-type MOSFET appears in Fig. 7.43. The fact that  $I_G = 0$  mA results in the following equation for  $V_{GS}$  as derived from an application of the voltage-divider rule:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} \quad (7.39)$$

Applying Kirchhoff's voltage law around the indicated loop of Fig. 7.43 results in

$$+V_G - V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = V_G - V_{R_S}$$

or

$$V_{GS} = V_G - I_D R_S \quad (7.40)$$

For the output section,

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

and

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D}$$

or

$$V_{DS} = V_{DD} - I_D(R_S + R_D) \quad (7.41)$$

Since the characteristics are a plot of  $I_D$  versus  $V_{GS}$  and Eq. (7.40) relates the same two variables, the two curves can be plotted on the same graph and a solution determined at their intersection. Once  $I_{DQ}$  and  $V_{GSQ}$  are known, all the remaining quantities of the network such as  $V_{DS}$ ,  $V_D$ , and  $V_S$  can be determined.

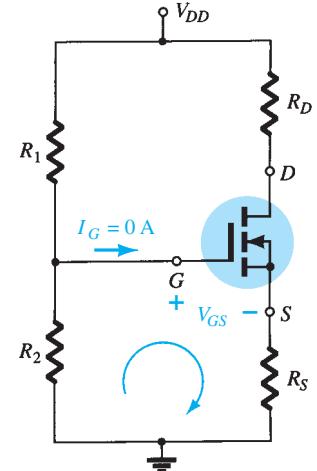
**EXAMPLE 7.11** Determine  $I_{DQ}$ ,  $V_{GSQ}$ , and  $V_{DS}$  for the network of Fig. 7.44.

**Solution:**

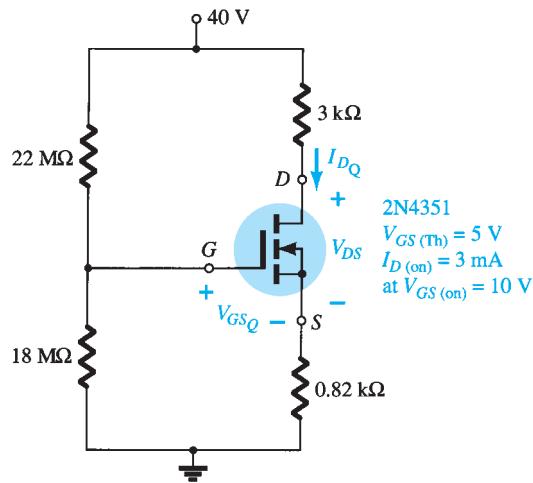
#### Network

$$\text{Eq. (7.39): } V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(18 \text{ M}\Omega)(40 \text{ V})}{22 \text{ M}\Omega + 18 \text{ M}\Omega} = 18 \text{ V}$$

$$\text{Eq. (7.40): } V_{GS} = V_G - I_D R_S = 18 \text{ V} - I_D(0.82 \text{ k}\Omega)$$



**FIG. 7.43**  
Voltage-divider biasing arrangement for an *n*-channel enhancement MOSFET.



**FIG. 7.44**  
Example 7.11.

When  $I_D = 0 \text{ mA}$ ,

$$V_{GS} = 18 \text{ V} - (0 \text{ mA})(0.82 \text{ k}\Omega) = 18 \text{ V}$$

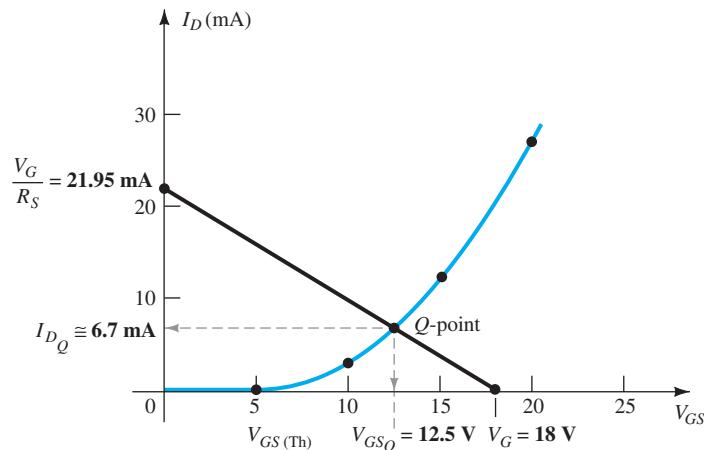
as appearing on Fig. 7.45. When  $V_{GS} = 0 \text{ V}$ ,

$$V_{GS} = 18 \text{ V} - I_D(0.82 \text{ k}\Omega)$$

$$0 = 18 \text{ V} - I_D(0.82 \text{ k}\Omega)$$

$$I_D = \frac{18 \text{ V}}{0.82 \text{ k}\Omega} = 21.95 \text{ mA}$$

as appearing on Fig. 7.45.



**FIG. 7.45**  
Determining the *Q*-point for the network of Example 7.11.

### Device

$$V_{GS(\text{Th})} = 5 \text{ V}, \quad I_{D(\text{on})} = 3 \text{ mA} \text{ with } V_{GS(\text{on})} = 10 \text{ V}$$

$$\begin{aligned} \text{Eq. (7.34): } k &= \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2} \\ &= \frac{3 \text{ mA}}{(10 \text{ V} - 5 \text{ V})^2} = 0.12 \times 10^{-3} \text{ A/V}^2 \end{aligned}$$

and

$$\begin{aligned} I_D &= k(V_{GS} - V_{GS(\text{Th})})^2 \\ &= 0.12 \times 10^{-3}(V_{GS} - 5)^2 \end{aligned}$$

which is plotted on the same graph (Fig. 7.45). From Fig. 7.45,

$$I_{DQ} \approx 6.7 \text{ mA}$$

$$V_{GSQ} = 12.5 \text{ V}$$

$$\begin{aligned} \text{Eq. (7.41): } V_{DS} &= V_{DD} - I_D(R_S + R_D) \\ &= 40 \text{ V} - (6.7 \text{ mA})(0.82 \text{ k}\Omega + 3.0 \text{ k}\Omega) \\ &= 40 \text{ V} - 25.6 \text{ V} \\ &= 14.4 \text{ V} \end{aligned}$$

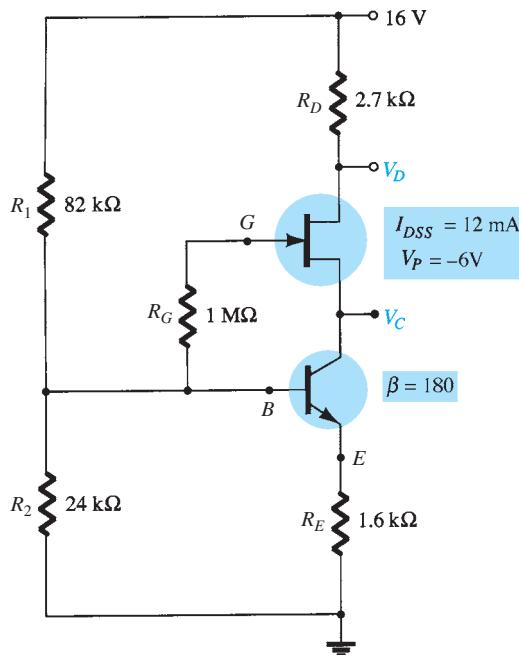
## 7.9 SUMMARY TABLE

Table 7.1 reviews the basic results and demonstrates the similarity in approach for a number of FET configurations. It also reveals that the analysis of dc configurations for FETs is fairly straightforward. Once the transfer characteristics are established, the network bias line can be drawn and the  $Q$ -point determined at the intersection of the device transfer characteristic and the network bias curve. The remaining analysis is simply an application of the basic laws of circuit analysis.

## 7.10 COMBINATION NETWORKS

Now that the dc analysis of a variety of BJT and FET configurations is established, the opportunity to analyze networks with both types of devices presents itself. Fundamentally, the analysis simply requires that we *first* approach the device that will provide a terminal voltage or current level. The door is then usually open to calculating other quantities and concentrating on the remaining unknowns. These are usually particularly interesting problems due to the challenge of finding the opening and then using the results of the past few sections and Chapter 4 to find the important quantities for each device. The equations and relationships used are simply those we have employed on more than one occasion—there is no need to develop any new methods of analysis.

**EXAMPLE 7.12** Determine the levels of  $V_D$  and  $V_C$  for the network of Fig. 7.46.



**FIG. 7.46**  
Example 7.12.

**TABLE 7.1**  
*FET Bias Configurations*

Type	Configuration	Pertinent Equations	Graphical Solution
JFET Fixed-bias		$V_{GSQ} = -V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
JFET Self-bias		$V_{GS} = -I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Common-gate		$V_{GS} = V_{SS} - I_D R_S$ $V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)$	
JFET ( $R_D = 0 \Omega$ )		$V_{GS} = -I_D R_S$ $V_D = V_{DD}$ $V_S = I_D R_S$ $V_{DS} = V_{DD} - I_S R_S$	
JFET Special case ( $V_{GSQ} = 0 \text{ V}$ )		$V_{GSQ} = 0 \text{ V}$ $I_{DQ} = I_{DSS}$	
Depletion-type MOSFET Fixed-bias (and MESFETs)		$V_{GSQ} = +V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
Depletion-type MOSFET Voltage-divider bias (and MESFETs)		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
Enhancement type MOSFET Feedback configuration (and MESFETs)		$V_{GS} = V_{DS}$ $V_{GS} = V_{DD} - I_D R_D$	
Enhancement type MOSFET Voltage-divider bias (and MESFETs)		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$	

**Solution:** From experience we now realize that  $V_{GS}$  is typically an important quantity to determine or write an equation for when analyzing JFET networks. Since  $V_{GS}$  is a level for which an immediate solution is not obvious, let us turn our attention to the transistor configuration. The voltage-divider configuration is one where the approximate technique can be applied ( $\beta R_E = 180 \times 1.6 \text{ k}\Omega = 288 \text{ k}\Omega > 10R_2 = 240 \text{ k}\Omega$ ), permitting a determination of  $V_B$  using the voltage-divider rule on the input circuit.

For  $V_B$ ,

$$V_B = \frac{24 \text{ k}\Omega(16 \text{ V})}{82 \text{ k}\Omega + 24 \text{ k}\Omega} = 3.62 \text{ V}$$

Using the fact that  $V_{BE} = 0.7 \text{ V}$  results in

$$\begin{aligned} V_E &= V_B - V_{BE} = 3.62 \text{ V} - 0.7 \text{ V} \\ &= 2.92 \text{ V} \end{aligned}$$

and

$$I_E = \frac{V_{RE}}{R_E} = \frac{V_E}{R_E} = \frac{2.92 \text{ V}}{1.6 \text{ k}\Omega} = 1.825 \text{ mA}$$

with

$$I_C \cong I_E = 1.825 \text{ mA}$$

Continuing, we find for this configuration that

$$I_D = I_S = I_C$$

and

$$\begin{aligned} V_D &= 16 \text{ V} - I_D(2.7 \text{ k}\Omega) \\ &= 16 \text{ V} - (1.825 \text{ mA})(2.7 \text{ k}\Omega) = 16 \text{ V} - 4.93 \text{ V} \\ &= \mathbf{11.07 \text{ V}} \end{aligned}$$

The question of how to determine  $V_C$  is not as obvious. Both  $V_{CE}$  and  $V_{DS}$  are unknown quantities, preventing us from establishing a link between  $V_D$  and  $V_C$  or from  $V_E$  to  $V_D$ . A more careful examination of Fig. 7.46 reveals that  $V_C$  is linked to  $V_B$  by  $V_{GS}$  (assuming that  $V_{RG} = 0 \text{ V}$ ). Since we know  $V_B$  if we can find  $V_{GS}$ ,  $V_C$  can be determined from

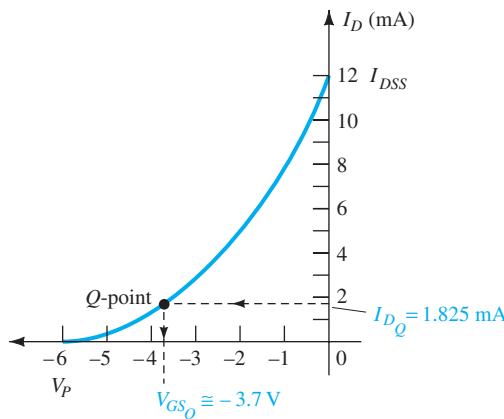
$$V_C = V_B - V_{GS}$$

The question then arises as to how to find the level of  $V_{GSQ}$  from the quiescent value of  $I_D$ . The two are related by Shockley's equation:

$$I_{DQ} = I_{DSS} \left( 1 - \frac{V_{GSQ}}{V_P} \right)^2$$

and  $V_{GSQ}$  could be found mathematically by solving for  $V_{GSQ}$  and substituting numerical values. However, let us turn to the graphical approach and simply work in the reverse order employed in the preceding sections. The JFET transfer characteristics are first sketched as shown in Fig. 7.47. The level of  $I_{DQ} = I_{SQ} = I_{CQ} = I_{EQ}$  is then established by a horizontal line as shown in the same figure.  $V_{GSQ}$  is then determined by dropping a line down from the operating point to the horizontal axis, resulting in

$$V_{GSQ} = -3.7 \text{ V}$$



**FIG. 7.47**

Determining the Q-point for the network of Fig. 7.46.

The level of  $V_C$  is given by

$$\begin{aligned} V_C &= V_B - V_{GS_Q} = 3.62 \text{ V} - (-3.7 \text{ V}) \\ &= 7.32 \text{ V} \end{aligned}$$

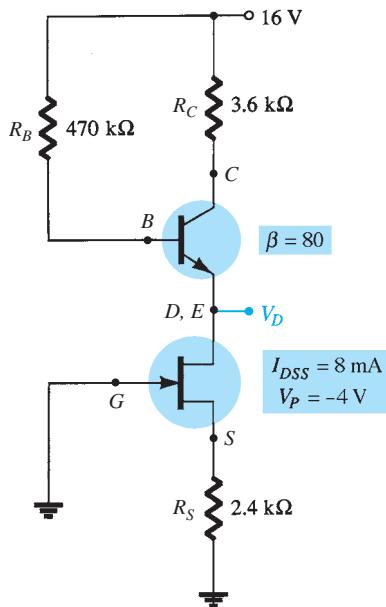


FIG. 7.48

Example 7.13.

**EXAMPLE 7.13** Determine  $V_D$  for the network of Fig. 7.48.

**Solution:** In this case, there is no obvious path for determining a voltage or current level for the transistor configuration. However, turning to the self-biased JFET, we can derive an equation for  $V_{GS}$  and determine the resulting quiescent point using graphical techniques. That is,

$$V_{GS} = -I_D R_S = -I_D(2.4 \text{ k}\Omega)$$

resulting in the self-bias line appearing in Fig. 7.49, which establishes a quiescent point at

$$V_{GS_Q} = -2.4 \text{ V}$$

$$I_{DQ} = 1 \text{ mA}$$

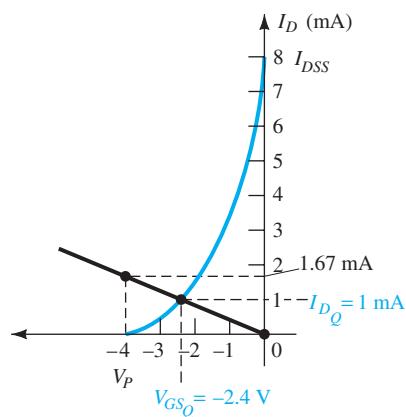


FIG. 7.49

Determining the  $Q$ -point for the network of Fig. 7.48.

For the transistor,

$$I_E \cong I_C = I_D = 1 \text{ mA}$$

$$\text{and } I_B = \frac{I_C}{\beta} = \frac{1 \text{ mA}}{80} = 12.5 \mu\text{A}$$

$$\begin{aligned} V_B &= 16 \text{ V} - I_B(470 \text{ k}\Omega) \\ &= 16 \text{ V} - (12.5 \mu\text{A})(470 \text{ k}\Omega) = 16 \text{ V} - 5.88 \text{ V} \\ &= 10.12 \text{ V} \end{aligned}$$

and

$$\begin{aligned} V_E &= V_D = V_B - V_{BE} \\ &= 10.12 \text{ V} - 0.7 \text{ V} \\ &= 9.42 \text{ V} \end{aligned}$$

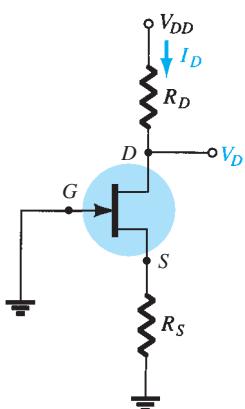


FIG. 7.50

Self-bias configuration to be designed.

## 7.11 DESIGN

The design process is a function of the area of application, level of amplification desired, signal strength, and operating conditions. The first step is normally to establish the proper dc levels of operation.

For example, if the levels of  $V_D$  and  $I_D$  are specified for the network of Fig. 7.50, the level of  $V_{GS_Q}$  can be determined from a plot of the transfer curve and  $R_S$  can then be determined from  $V_{GS} = -I_D R_S$ . If  $V_{DD}$  is specified, the level of  $R_D$  can then be calculated from  $R_D = (V_{DD} - V_D)/I_D$ . Of course, the values of  $R_S$  and  $R_D$  may not be standard commercial values, requiring that the nearest commercial values be employed. However, with the tolerance (range of values) normally specified for the parameters of a network,

the slight variation due to the choice of standard values will seldom cause a real concern in the design process.

The above is only one possibility for the design phase involving the network of Fig. 7.50. It is possible that only  $V_{DD}$  and  $R_D$  are specified together with the level of  $V_{DS}$ . The device to be employed may have to be specified along with the level of  $R_S$ . It appears logical that the device chosen should have a maximum  $V_{DS}$  greater than the specified value by a safe margin.

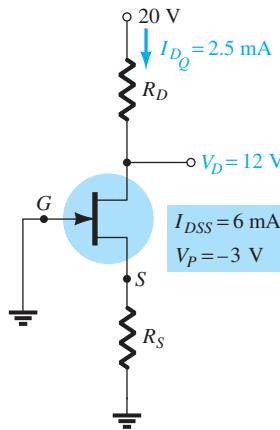
In general, it is good design practice for linear amplifiers to choose operating points that do not crowd the saturation level ( $I_{DSS}$ ) or cutoff ( $V_P$ ) regions. Levels of  $V_{GSQ}$  close to  $V_P/2$  or levels of  $I_{DQ}$  near  $I_{DSS}/2$  are certainly reasonable starting points in the design. Of course, in every design procedure the maximum levels of  $I_D$  and  $V_{DS}$  as appearing on the specification sheet must not be exceeded.

The examples to follow have a design or synthesis orientation in that specific levels are provided and network parameters such as  $R_D$ ,  $R_S$ ,  $V_{DD}$ , and so on, must be determined. In any case, the approach is in many ways the opposite of that described in previous sections. In some cases, it is just a matter of applying Ohm's law in its appropriate form. In particular, if resistive levels are requested, the result is often obtained simply by applying Ohm's law in the following form:

$$R_{\text{unknown}} = \frac{V_R}{I_R} \quad (7.42)$$

where  $V_R$  and  $I_R$  are often parameters that can be found directly from the specified voltage and current levels.

**EXAMPLE 7.14** For the network of Fig. 7.51, the levels of  $V_{DQ}$  and  $I_{DQ}$  are specified. Determine the required values of  $R_D$  and  $R_S$ . What are the closest standard commercial values?



**FIG. 7.51**  
Example 7.14.

**Solution:** As defined by Eq. (7.42),

$$R_D = \frac{V_{RD}}{I_{DQ}} = \frac{V_{DD} - V_{DQ}}{I_{DQ}}$$

$$\text{and} \quad = \frac{20 \text{ V} - 12 \text{ V}}{2.5 \text{ mA}} = \frac{8 \text{ V}}{2.5 \text{ mA}} = 3.2 \text{ k}\Omega$$

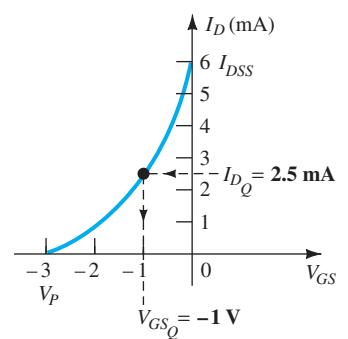
Plotting the transfer curve in Fig. 7.52 and drawing a horizontal line at  $I_{DQ} = 2.5 \text{ mA}$  results in  $V_{GSQ} = -1 \text{ V}$ , and applying  $V_{GS} = -I_{DQ}R_S$  establishes the level of  $R_S$ :

$$R_S = \frac{-(V_{GSQ})}{I_{DQ}} = \frac{-(-1 \text{ V})}{2.5 \text{ mA}} = 0.4 \text{ k}\Omega$$

The nearest standard commercial values are

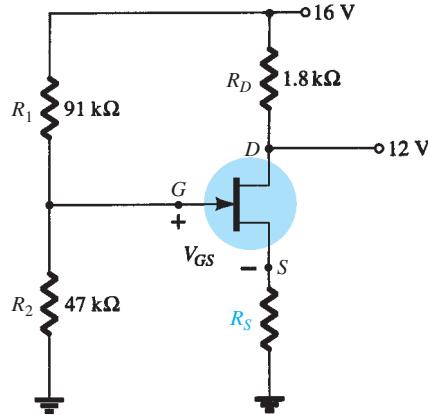
$$R_D = 3.2 \text{ k}\Omega \Rightarrow 3.3 \text{ k}\Omega$$

$$R_S = 0.4 \text{ k}\Omega \Rightarrow 0.39 \text{ k}\Omega$$



**FIG. 7.52**  
Determining  $V_{GSQ}$  for the network of Fig. 7.51.

**EXAMPLE 7.15** For the voltage-divider bias configuration of Fig. 7.53, if  $V_D = 12$  V and  $V_{GSQ} = -2$  V, determine the value of  $R_S$ .



**FIG. 7.53**  
Example 7.15.

**Solution:** The level of  $V_G$  is determined as follows:

$$V_G = \frac{47 \text{ k}\Omega(16 \text{ V})}{47 \text{ k}\Omega + 91 \text{ k}\Omega} = 5.44 \text{ V}$$

with

$$\begin{aligned} I_D &= \frac{V_{DD} - V_D}{R_D} \\ &= \frac{16 \text{ V} - 12 \text{ V}}{1.8 \text{ k}\Omega} = 2.22 \text{ mA} \end{aligned}$$

The equation for  $V_{GS}$  is then written and the known values substituted:

$$\begin{aligned} V_{GS} &= V_G - I_D R_S \\ -2 \text{ V} &= 5.44 \text{ V} - (2.22 \text{ mA}) R_S \\ -7.44 \text{ V} &= -(2.22 \text{ mA}) R_S \end{aligned}$$

and

$$R_S = \frac{7.44 \text{ V}}{2.22 \text{ mA}} = 3.35 \text{ k}\Omega$$

The nearest standard commercial value is 3.3 kΩ.

**EXAMPLE 7.16** The levels of  $V_{DS}$  and  $I_D$  are specified as  $V_{DS} = \frac{1}{2}V_{DD}$  and  $I_D = I_{D(\text{on})}$  for the network of Fig. 7.54. Determine the levels of  $V_{DD}$  and  $R_D$ .

**Solution:** Given  $I_D = I_{D(\text{on})} = 4$  mA and  $V_{GS} = V_{GS(\text{on})} = 6$  V, for this configuration,

$$V_{DS} = V_{GS} = \frac{1}{2}V_{DD}$$

and

$$6 \text{ V} = \frac{1}{2}V_{DD}$$

so that

$$V_{DD} = 12 \text{ V}$$

Applying Eq. (7.42) yields

$$R_D = \frac{V_{RD}}{I_D} = \frac{V_{DD} - V_{DS}}{I_{D(\text{on})}} = \frac{V_{DD} - \frac{1}{2}V_{DD}}{I_{D(\text{on})}} = \frac{\frac{1}{2}V_{DD}}{I_{D(\text{on})}}$$

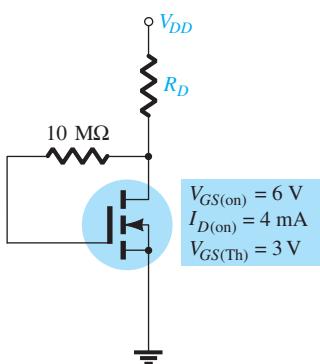
and

$$R_D = \frac{6 \text{ V}}{4 \text{ mA}} = 1.5 \text{ k}\Omega$$

which is a standard commercial value.

**FIG. 7.54**

Example 7.16.



How often has a network been carefully constructed only to find that when the power is applied, the response is totally unexpected and fails to match the theoretical calculations? What is the next step? Is it a bad connection? A misreading of the color code for a resistive element? An error in the construction process? The range of possibilities seems vast and often frustrating. The troubleshooting process first described in the analysis of BJT transistor configurations should narrow down the list of possibilities and isolate the problem area following a definite plan of attack. In general, the process begins with a rechecking of the network construction and the terminal connections. This is usually followed by the checking of voltage levels between specific terminals and ground or between terminals of the network. Seldom are current levels measured since such maneuvers require disturbing the network structure to insert the meter. Of course, once the voltage levels are obtained, current levels can be calculated using Ohm's law. In any case, some idea of the expected voltage or current level must be known for the measurement to have any importance. In total, therefore, the troubleshooting process can begin with some hope of success only if the basic operation of the network is understood along with some expected levels of voltage or current. For the *n*-channel JFET amplifier, it is clearly understood that the quiescent value of  $V_{GSQ}$  is limited to 0 V or a negative voltage. For the network of Fig. 7.55,  $V_{GSQ}$  is limited to negative values in the range 0 V to  $V_P$ . If a meter is hooked up as shown in Fig. 7.55, with the positive lead (normally red) to the gate and the negative lead (usually black) to the source, the resulting reading should have a negative sign and a magnitude of a few volts. Any other response should be considered suspicious and needs to be investigated.

The level of  $V_{DS}$  is typically between 25% and 75% of  $V_{DD}$ . A reading of 0 V for  $V_{DS}$  clearly indicates that either the output circuit has an "open" or the JFET is internally short-circuited between drain and source. If  $V_D = V_{DD}$  volts, there is obviously no drop across  $R_D$ , due to the lack of current through  $R_D$ , and the connections should be checked for continuity.

If the level of  $V_{DS}$  seems inappropriate, the continuity of the output circuit can easily be checked by grounding the negative lead of the voltmeter and measuring the voltage levels from  $V_{DD}$  to ground using the positive lead. If  $V_D = V_{DD}$ , the current through  $R_D$  may be zero, but there is continuity between  $V_D$  and  $V_{DD}$ . If  $V_S = V_{DD}$ , the device is not open between drain and source, but it is also not "on." The continuity through to  $V_S$  is confirmed, however. In this case, it is possible that there is a poor ground connection between  $R_S$  and ground that may not be obvious. The internal connection between the wire of the lead and the terminal connector may have separated. Other possibilities also exist, such as a shorted device from drain to source, but the troubleshooter will simply have to narrow down the possible causes for the malfunction.

The continuity of a network can also be checked simply by measuring the voltage across any resistor of the network (except for  $R_G$  in the JFET configuration). An indication of 0 V immediately reveals the lack of current through the element due to an open circuit in the network.

The most sensitive element in the BJT and JFET configurations is the amplifier itself. The application of excessive voltage during the construction or testing phase or the use of incorrect resistor values resulting in high current levels can destroy the device. If you question the condition of the amplifier, the best test for the FET is the curve tracer since it not only reveals whether the device is operable, but also its range of current and voltage levels. Some testers may reveal that the device is still fundamentally sound but do not reveal whether its range of operation has been severely reduced.

The development of good troubleshooting techniques comes primarily from experience and a level of confidence in what to expect and why. There are, of course, times when the reasons for a strange response seem to disappear mysteriously when you check a network. In such cases, it is best not to breathe a sigh of relief and continue with the construction. The cause for such a sensitive "make or break" situation should be found and corrected, or it may reoccur at the most inopportune moment.

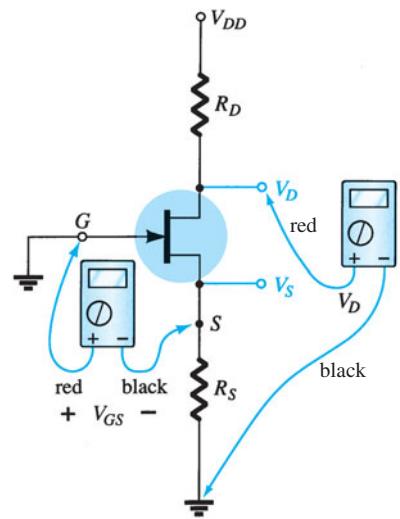
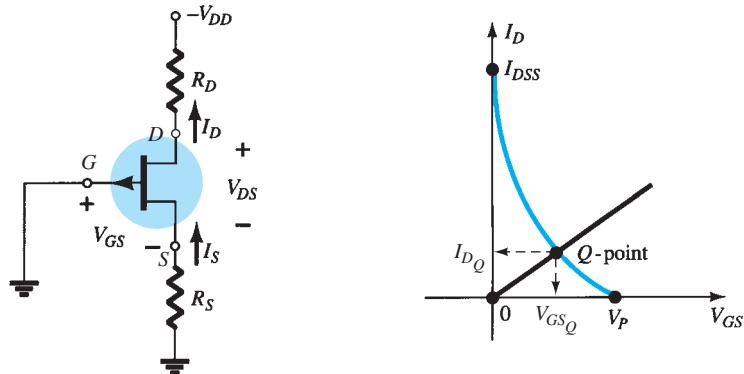


FIG. 7.55

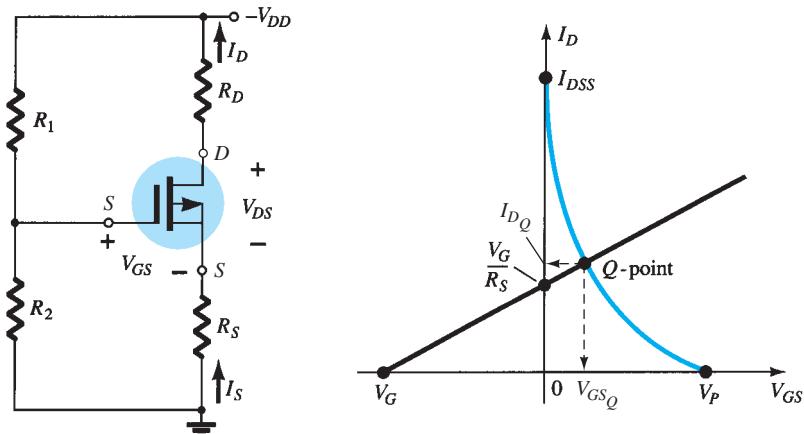
Checking the dc operation of the JFET self-bias configuration.

## 7.13 p-CHANNEL FETS

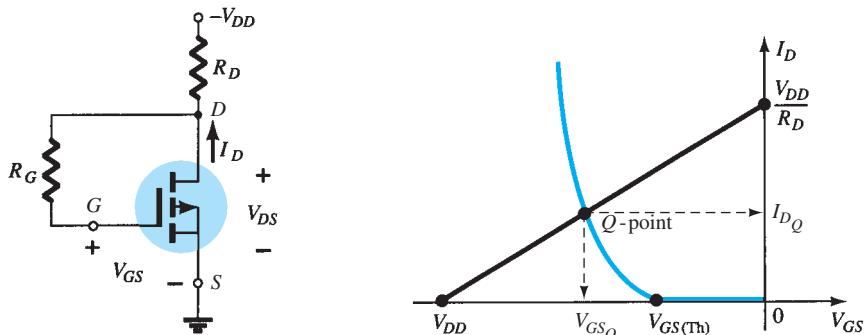
The analysis thus far has been limited solely to *n*-channel FETs. For *p*-channel FETs, a mirror image of the transfer curves is employed, and the defined current directions are reversed as shown in Fig. 7.56 for the various types of FETs.



(a)



(b)



(c)

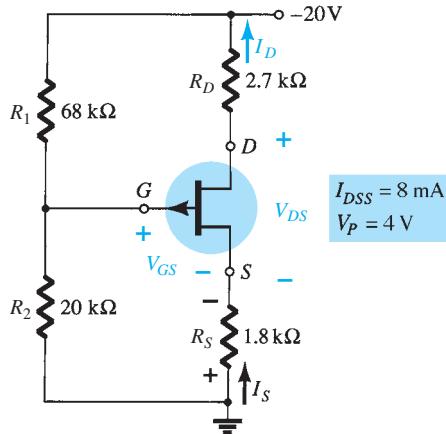
**FIG. 7.56**  
*p*-Channel configurations: (a) JFET; (b) depletion-type MOSFET;  
(c) enhancement-type MOSFET.

Note for each configuration of Fig. 7.56 that each supply voltage is now a negative voltage drawing current in the indicated direction. In particular, note that the double-subscript notation for voltages continues as defined for the *n*-channel device:  $V_{GS}$ ,  $V_{DS}$ , and so on. In this case, however,  $V_{GS}$  is positive (positive or negative for the depletion-type MOSFET) and  $V_{DS}$  negative.

Due to the similarities between the analysis of *n*-channel and *p*-channel devices, one can assume an *n*-channel device and reverse the supply voltage and perform the entire analysis. When the results are obtained, the magnitude of each quantity will be correct, although the current direction and voltage polarities will have to be reversed. However, the next example

will demonstrate that with the experience gained through the analysis of *n*-channel devices, the analysis of *p*-channel devices is quite straightforward.

**EXAMPLE 7.17** Determine  $I_{DQ}$ ,  $V_{GSQ}$ , and  $V_{DS}$  for the *p*-channel JFET of Fig. 7.57.



**FIG. 7.57**  
Example 7.17.

**Solution:** We have

$$V_G = \frac{20 \text{ k}\Omega(-20 \text{ V})}{20 \text{ k}\Omega + 68 \text{ k}\Omega} = -4.55 \text{ V}$$

Applying Kirchhoff's voltage law gives

$$V_G - V_{GS} + I_D R_S = 0$$

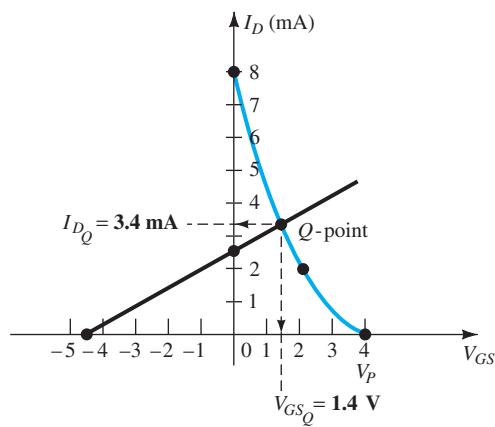
and

$$V_{GS} = V_G + I_D R_S$$

Choosing  $I_D = 0 \text{ mA}$  yields

$$V_{GS} = V_G = -4.55 \text{ V}$$

as appearing in Fig. 7.58.



**FIG. 7.58**  
Determining the *Q*-point for the JFET configuration of Fig. 7.57.

Choosing  $V_{GS} = 0 \text{ V}$ , we obtain

$$I_D = -\frac{V_G}{R_S} = -\frac{-4.55 \text{ V}}{1.8 \text{ k}\Omega} = 2.53 \text{ mA}$$

as also appearing in Fig. 7.58.

The resulting quiescent point from Fig. 7.58 is given by

$$I_{DQ} = 3.4 \text{ mA}$$

$$V_{GSQ} = 1.4 \text{ V}$$

For  $V_{DS}$ , Kirchhoff's voltage law results in

$$-I_D R_S + V_{DS} - I_D R_D + V_{DD} = 0$$

and

$$V_{DS} = -V_{DD} + I_D(R_D + R_S)$$

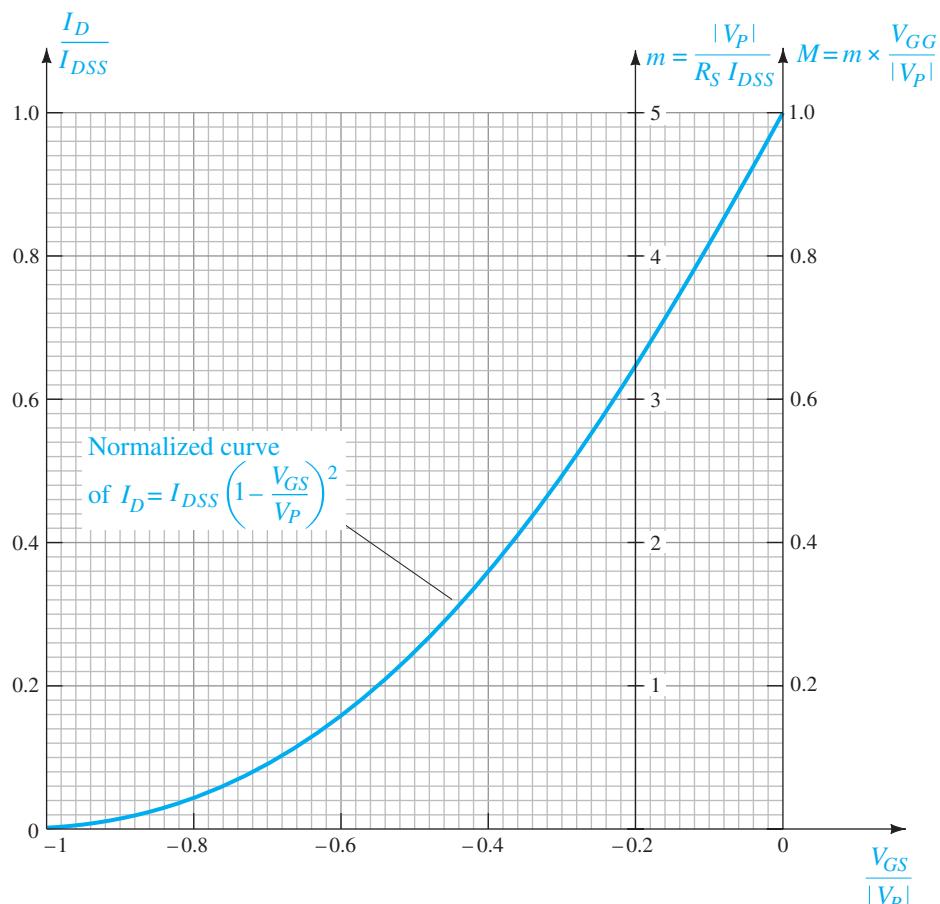
$$= -20 \text{ V} + (3.4 \text{ mA})(2.7 \text{ k}\Omega + 1.8 \text{ k}\Omega)$$

$$= -20 \text{ V} + 15.3 \text{ V}$$

$$= -4.7 \text{ V}$$

## 7.14 UNIVERSAL JFET BIAS CURVE

Since the dc solution of a FET configuration requires drawing the transfer curve for each analysis, a universal curve was developed that can be used for any level of  $I_{DSS}$  and  $V_P$ . The universal curve for an  $n$ -channel JFET or depletion-type MOSFET (for negative values of  $V_{GSQ}$ ) is provided in Fig. 7.59. Note that the horizontal axis is not that of  $V_{GS}$  but of a normalized level defined by  $V_{GS}/|V_P|$ , the  $|V_P|$  indicating that only the magnitude of  $V_P$  is to be employed, not its sign. For the vertical axis, the scale is also a normalized level of  $I_D/I_{DSS}$ . The result is that when  $I_D = I_{DSS}$ , the ratio is 1, and when  $V_{GS} = V_P$ , the ratio  $V_{GS}/|V_P|$  is -1. Note also that the scale for  $I_D/I_{DSS}$  is on the left rather than on the right as encountered for  $I_D$  in past exercises. The additional two scales on the right need an introduction. The vertical scale labeled  $m$  can in itself be used to find the solution to fixed-bias configurations. The other scale, labeled  $M$ , is employed along with the  $m$  scale to find the



**FIG. 7.59**

Universal JFET bias curve.

solution to voltage-divider configurations. The scaling for  $m$  and  $M$  come from a mathematical development involving the network equations and normalized scaling just introduced. The description to follow will not concentrate on why the  $m$  scale extends from 0 to 5 at  $V_{GS}/|V_P| = -0.2$  and the  $M$  scale ranges from 0 to 1 at  $V_{GS}/|V_P| = 0$ , but rather on how to use the resulting scales to obtain a solution for the configurations. The equations for  $m$  and  $M$  are the following, with  $V_G$  as defined by Eq. (7.15):

$$m = \frac{|V_P|}{I_{DSS}R_S} \quad (7.43)$$

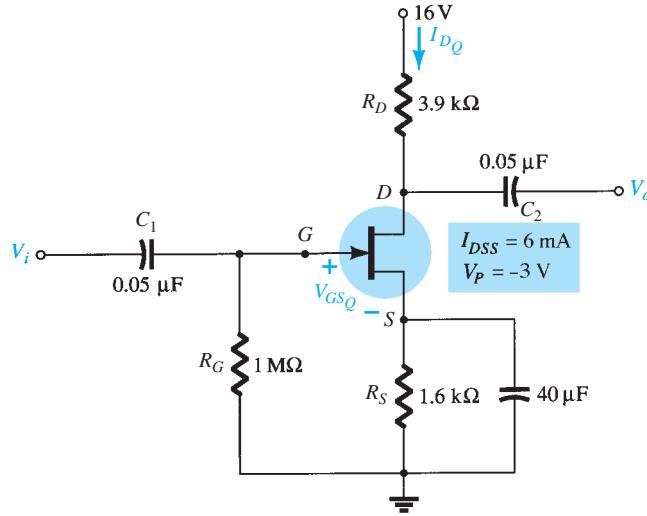
$$M = m \times \frac{V_G}{|V_P|} \quad (7.44)$$

with

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Keep in mind that the beauty of this approach is the elimination of the need to sketch the transfer curve for each analysis, that the superposition of the bias line is a great deal easier, and that the calculations are fewer. The use of the  $m$  and  $M$  axes is best described by examples employing the scales. Once the procedure is clearly understood, the analysis can be quite rapid, with a good measure of accuracy.

**EXAMPLE 7.18** Determine the quiescent values of  $I_D$  and  $V_{GS}$  for the network of Fig. 7.60.



**FIG. 7.60**  
Example 7.18.

**Solution:** Calculating the value of  $m$ , we obtain

$$m = \frac{|V_P|}{I_{DSS}R_S} = \frac{|-3 \text{ V}|}{(6 \text{ mA})(1.6 \text{ k}\Omega)} = 0.31$$

The self-bias line defined by  $R_S$  is plotted by drawing a straight line from the origin through a point defined by  $m = 0.31$ , as shown in Fig. 7.61.

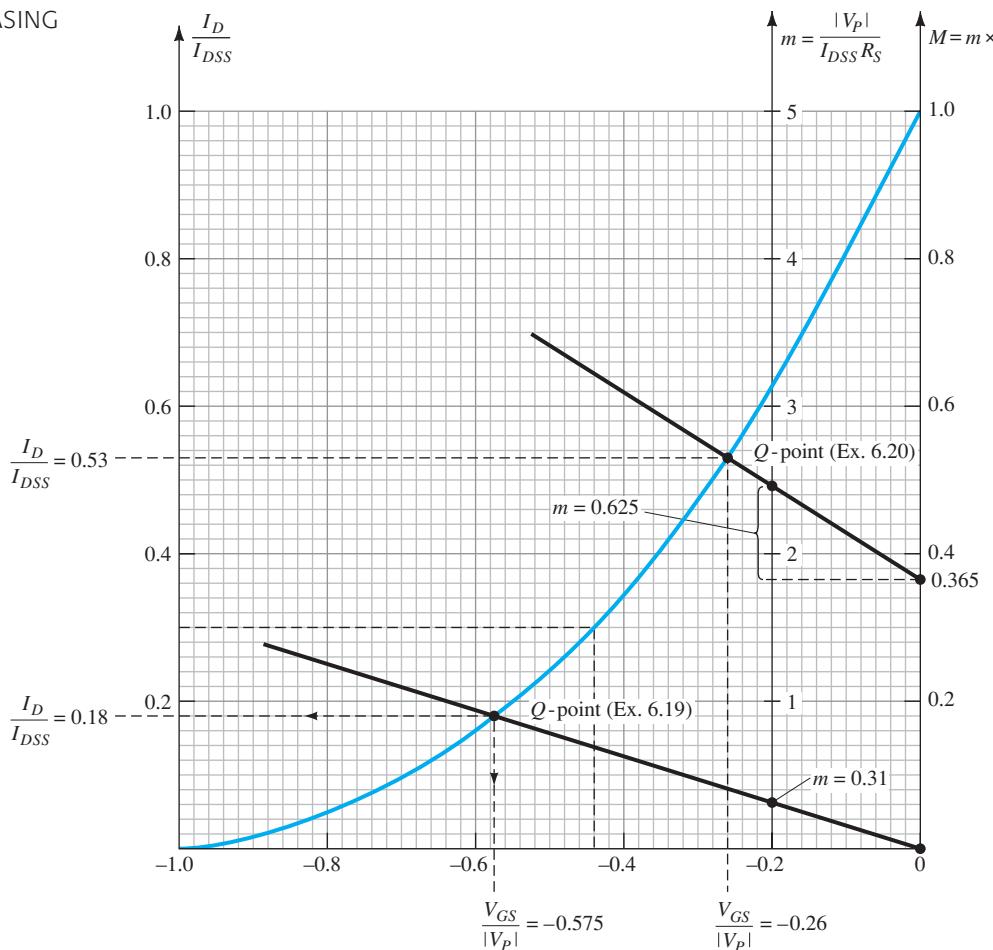
The resulting  $Q$ -point:

$$\frac{I_D}{I_{DSS}} = 0.18 \quad \text{and} \quad \frac{V_{GS}}{|V_P|} = -0.575$$

The quiescent values of  $I_D$  and  $V_{GS}$  can then be determined as follows:

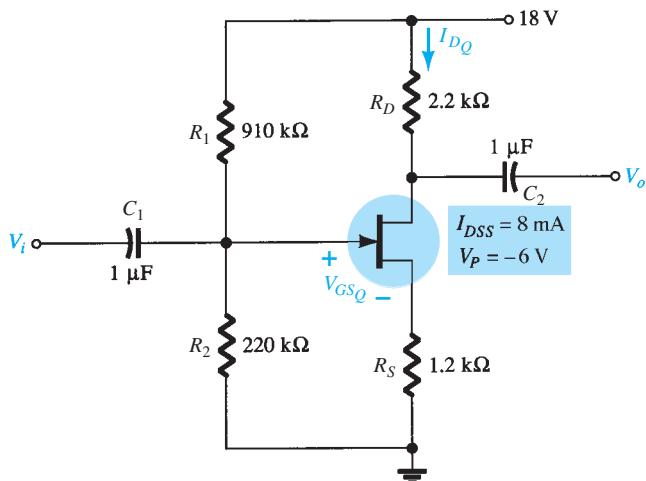
$$I_{DQ} = 0.18I_{DSS} = 0.18(6 \text{ mA}) = 1.08 \text{ mA}$$

$$\text{and} \quad V_{GSQ} = -0.575|V_P| = -0.575(3 \text{ V}) = -1.73 \text{ V}$$



**FIG. 7.61**  
Universal curve for Examples 7.18 and 7.19.

**EXAMPLE 7.19** Determine the quiescent values of  $I_D$  and  $V_{GS}$  for the network of Fig. 7.62.



**FIG. 7.62**  
Example 7.19.

**Solution:** Calculating  $m$  gives

$$m = \frac{|V_P|}{I_{DSS}R_S} = \frac{|-6\text{ V}|}{(8\text{ mA})(1.2\text{ k}\Omega)} = 0.625$$

Determining  $V_G$  yields

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(220 \text{ k}\Omega)(18 \text{ V})}{910 \text{ k}\Omega + 220 \text{ k}\Omega} = 3.5 \text{ V}$$

Finding  $M$ , we have

$$M = m \times \frac{V_G}{|V_P|} = 0.625 \left( \frac{3.5 \text{ V}}{6 \text{ V}} \right) = 0.365$$

Now that  $m$  and  $M$  are known, the bias line can be drawn on Fig. 7.61. In particular, note that even though the levels of  $I_{DSS}$  and  $V_P$  are different for the two networks, the same universal curve can be employed. First find  $M$  on the  $M$  axis as shown in Fig. 7.61. Then draw a horizontal line over to the  $m$  axis and, at the point of intersection, add the magnitude of  $m$  as shown in the figure. Using the resulting point on the  $m$  axis and the  $M$  intersection, draw the straight line to intersect with the transfer curve and define the  $Q$ -point. That is,

$$\frac{I_D}{I_{DSS}} = 0.53 \quad \text{and} \quad \frac{V_{GS}}{|V_P|} = -0.26$$

and

$$I_{DQ} = 0.53 I_{DSS} = 0.53(8 \text{ mA}) = 4.24 \text{ mA}$$

with

$$V_{GSQ} = -0.26 |V_P| = -0.26(6 \text{ V}) = -1.56 \text{ V}$$

## 7.15 PRACTICAL APPLICATIONS

The applications described here take full advantage of the high input impedance of field-effect transistors, the isolation that exists between the gate and drain circuits, and the linear region of JFET characteristics that permit approximating the device by a resistive element between the drain and source terminals.

### Voltage-Controlled Resistor (Noninverting Amplifier)

One of the most common applications of the JFET is as a variable resistor whose resistance value is controlled by the applied dc voltage at the gate terminal. In Fig. 7.63a, the linear region of a JFET transistor has been clearly indicated. Note that in this region the various curves all start at the origin and follow a fairly straight path as the drain-to-source voltage and drain current increase. Recall from your basic dc courses that **the plot of a fixed resistor is nothing more than a straight line with its origin at the intersection of the axes**.

In Fig. 7.63b, the linear region has been expanded to a maximum drain-to-source voltage of about 0.5 V. Note that even though the curves do have some curvature to them, they can easily be approximated by fairly straight lines, all having their origin at the intersection of the axes and a slope determined by the gate-to-source dc voltage. Recall from earlier discussions that **for an I-V plot where the current is the vertical axis and the voltage the horizontal axis, the steeper the slope, the less is the resistance; and the more horizontal the curve, the greater is the resistance**. The result is that a vertical line has  $0 \Omega$  resistance and a horizontal line has infinite resistance. At  $V_{GS} = 0 \text{ V}$ , the slope is the steepest and the resistance the least. As the gate-to-source voltage becomes increasingly negative, the slope decreases until it is almost horizontal near the pinch-off voltage.

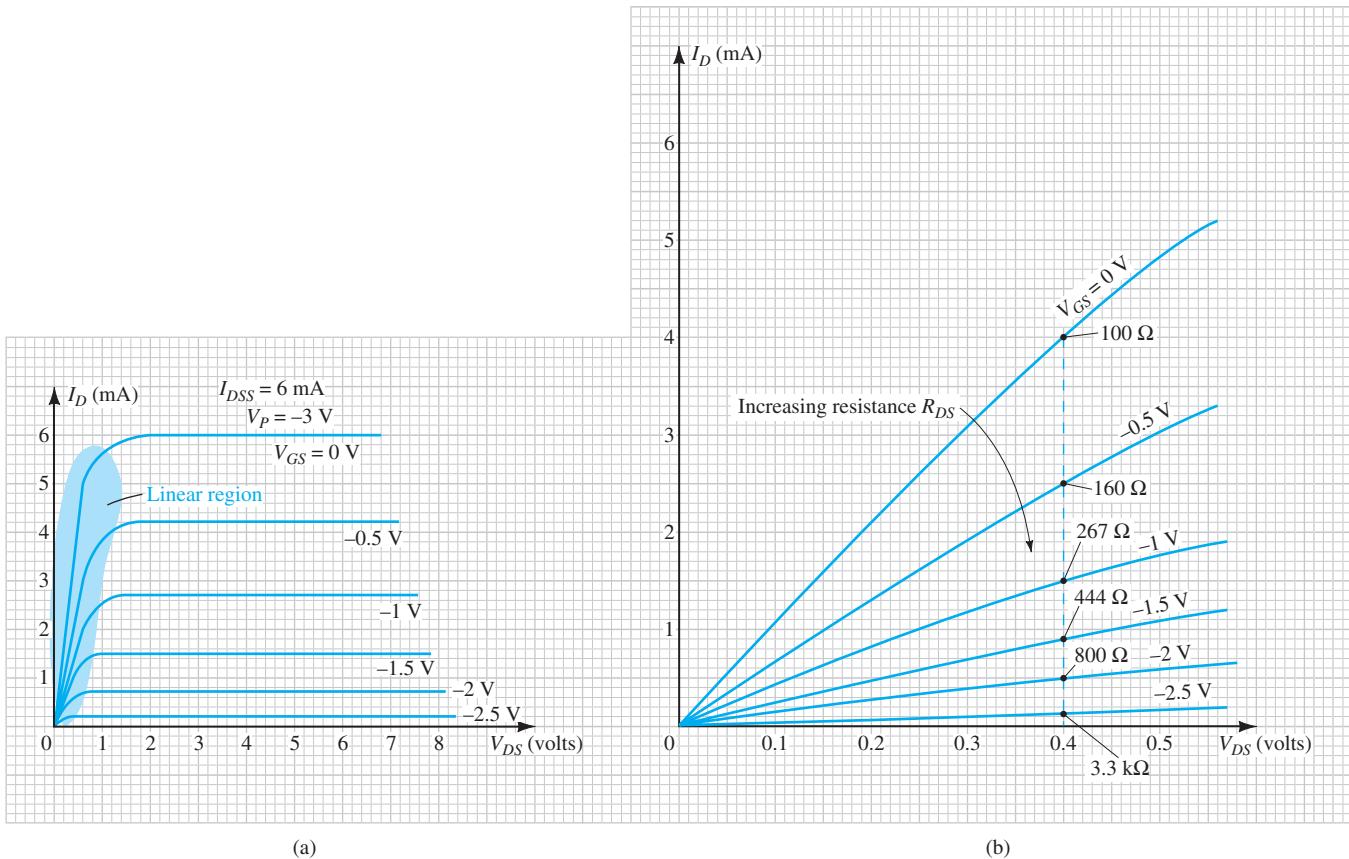
It is important to remember that this linear region is limited to levels of  $V_{DS}$  that are relatively small compared to the pinch-off voltage. In general, **the linear region of a JFET is defined by  $V_{DS} \ll V_{DS_{max}}$  and  $|V_{GS}| \ll |V_P|$** .

Using Ohm's law, let us calculate the resistance associated with each curve of Fig. 7.63b using the current that results at a drain-to-source voltage of 0.4 V.

$$V_{GS} = 0 \text{ V}: \quad R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{0.4 \text{ V}}{4 \text{ mA}} = 100 \Omega$$

$$V_{GS} = -0.5 \text{ V}: \quad R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{0.4 \text{ V}}{2.5 \text{ mA}} = 160 \Omega$$

$$V_{GS} = -1 \text{ V}: \quad R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{0.4 \text{ V}}{1.5 \text{ mA}} = 267 \Omega$$



(a)

(b)

**FIG. 7.63**  
JFET characteristics: (a) defining the linear region; (b) expanding the linear region.

$$V_{GS} = -1.5\text{ V}: \quad R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{0.4\text{ V}}{0.9\text{ mA}} = 444\Omega$$

$$V_{GS} = -2\text{ V}: \quad R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{0.4\text{ V}}{0.5\text{ mA}} = 800\Omega$$

$$V_{GS} = -2.5\text{ V}: \quad R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{0.4\text{ V}}{0.12\text{ mA}} = 3.3\text{ k}\Omega$$

In particular, note how the drain-to-source resistance increases as the gate-to-source voltage approaches the pinch-off value.

The results just obtained can be verified by Eq. (6.1) using the pinch-off voltage of  $-3\text{ V}$  and  $R_o = 100\Omega$  at  $V_{GS} = 0\text{ V}$ . We have

$$R_{DS} = \frac{R_o}{\left(1 - \frac{V_{GS}}{V_P}\right)^2} = \frac{100\Omega}{\left(1 - \frac{-V_{GS}}{-3\text{ V}}\right)^2}$$

$$V_{GS} = -0.5\text{ V}: \quad R_{DS} = \frac{100\Omega}{\left(1 - \frac{-0.5\text{ V}}{-3\text{ V}}\right)^2} = 144\Omega \quad (\text{versus } 160\Omega \text{ above})$$

$$V_{GS} = -1\text{ V}: \quad R_{DS} = \frac{100\Omega}{\left(1 - \frac{-1\text{ V}}{-3\text{ V}}\right)^2} = 225\Omega \quad (\text{versus } 267\Omega \text{ above})$$

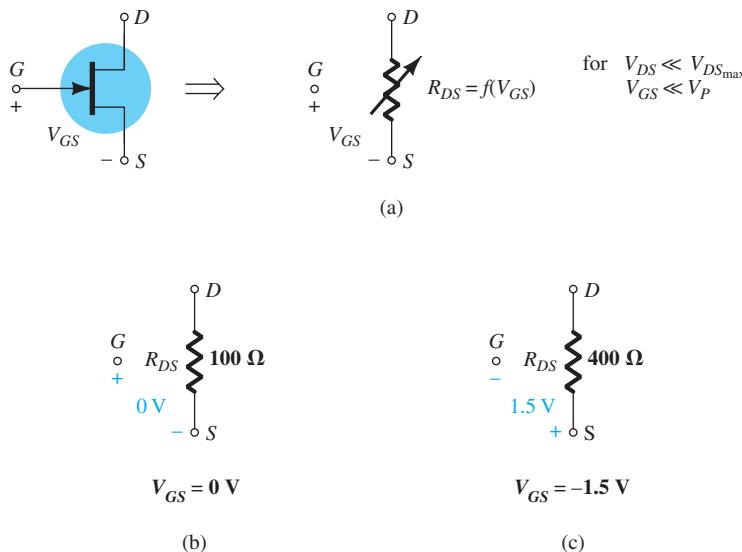
$$V_{GS} = -1.5\text{ V}: \quad R_{DS} = \frac{100\Omega}{\left(1 - \frac{-1.5\text{ V}}{-3\text{ V}}\right)^2} = 400\Omega \quad (\text{versus } 444\Omega \text{ above})$$

$$V_{GS} = -2 \text{ V}; R_{DS} = \frac{100 \Omega}{\left(1 - \frac{-2 \text{ V}}{-3 \text{ V}}\right)^2} = 900 \Omega \quad (\text{versus } 800 \Omega \text{ above})$$

$$V_{GS} = -2.5 \text{ V}; R_{DS} = \frac{100 \Omega}{\left(1 - \frac{-2.5 \text{ V}}{-3 \text{ V}}\right)^2} = 3.6 \text{ k}\Omega \quad (\text{versus } 3.3 \text{ k}\Omega \text{ above})$$

Although the results are not an exact match, for most applications Equation (6.1) provides an excellent approximation to the actual resistance level for  $R_{DS}$ .

Keep in mind that **the possible levels of  $V_{GS}$  between 0 V and pinch-off are infinite**, resulting in the full range of resistor values between  $100 \Omega$  and  $3.3 \text{ k}\Omega$ . In general, therefore, the above discussion is summarized by Fig. 7.64a. For  $V_{GS} = 0 \text{ V}$ , the equivalence of Fig. 7.64b would result; for  $V_{GS} = -1.5 \text{ V}$ , the equivalence of Fig. 7.64c; and so on.



**FIG. 7.64**

*JFET voltage-controlled drain resistance: (a) general equivalence; (b) with  $V_{GS} = 0 \text{ V}$ ; (c) with  $V_{GS} = -1.5 \text{ V}$ .*

Let us now investigate the use of this voltage-controlled drain resistance in the noninverting amplifier of Fig. 7.65a—**noninverting indicates that the input and output signals are in phase**. The op-amp of Fig. 7.65a is discussed in detail in Chapter 10, and the equation for the gain is derived in Section 10.4.

If  $R_f = R_1$ , the resulting gain is 2, as shown by the in-phase sinusoidal signals of Fig. 7.65a. In Fig. 7.65b, the variable resistor has been replaced by an *n*-channel JFET. If  $R_f = 3.3 \text{ k}\Omega$  and the transistor of Fig. 7.63 were employed, the gain could extend from  $1 + 3.3 \text{ k}\Omega / 3.3 \text{ k}\Omega = 2$  to  $1 + 3.3 \text{ k}\Omega / 100 \Omega = 34$  for  $V_{GS}$  varying from  $-2.5 \text{ V}$  to  $0 \text{ V}$ , respectively. In general, therefore, the gain of the amplifier can be set at any value between 2 and 34 by simply controlling the applied dc biasing voltage. The effect of this type of control can be extended to an extensive variety of applications. For instance, if the battery voltage of a radio should start to drop due to extended use, the dc level at the gate of the controlling JFET will drop, and the level of  $R_{DS}$  will decrease also. A drop in  $R_{DS}$  will result in an increase in gain for the same value of  $R_f$ , and the output volume of the radio can be maintained. A number of oscillators (networks designed to generate sinusoidal signals of specific frequencies) have a resistance factor in the equation for the frequency generated. If the frequency generated should start to drift, a feedback network can be designed that changes the dc level at the gate of a JFET and therefore its drain resistance. If that drain resistance is part of the resistance factor in the frequency equation, the frequency generated can be stabilized or maintained.

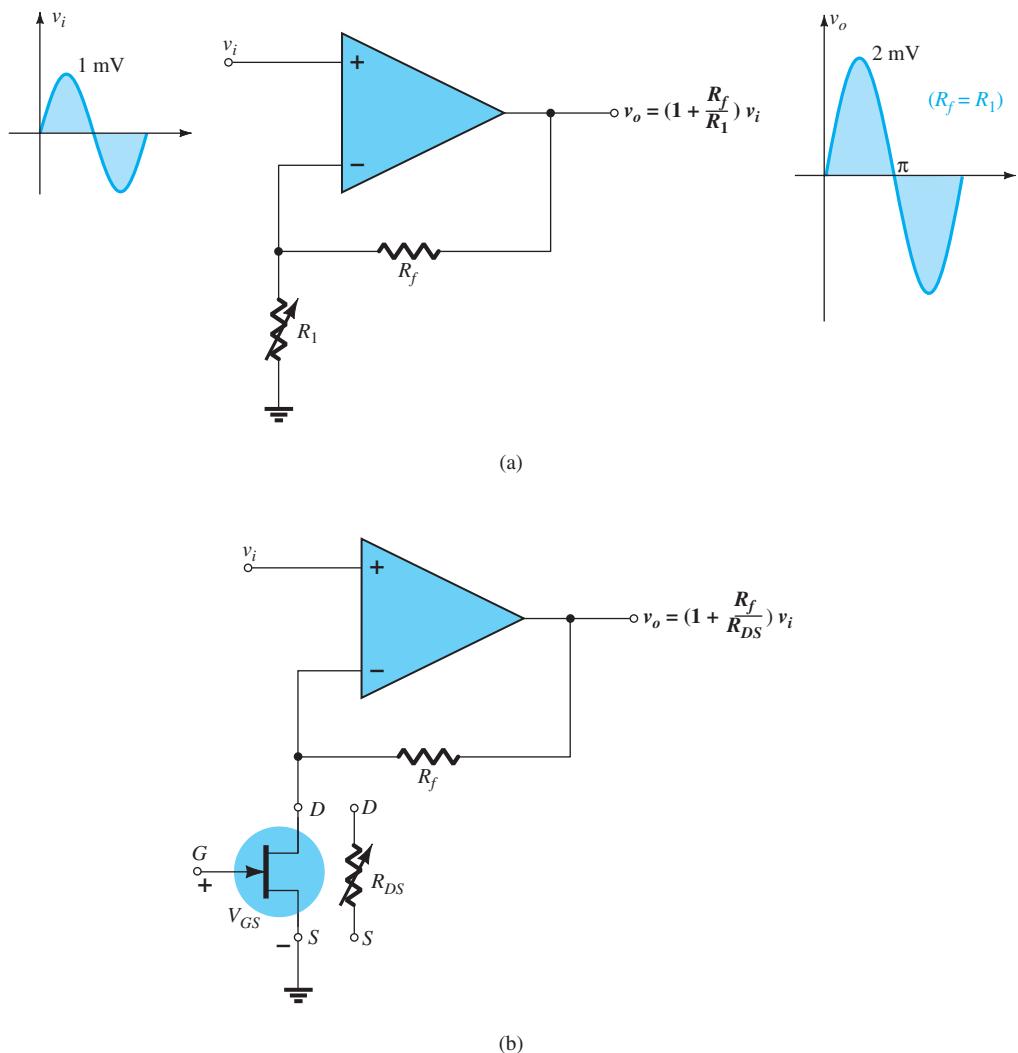


FIG. 7.65

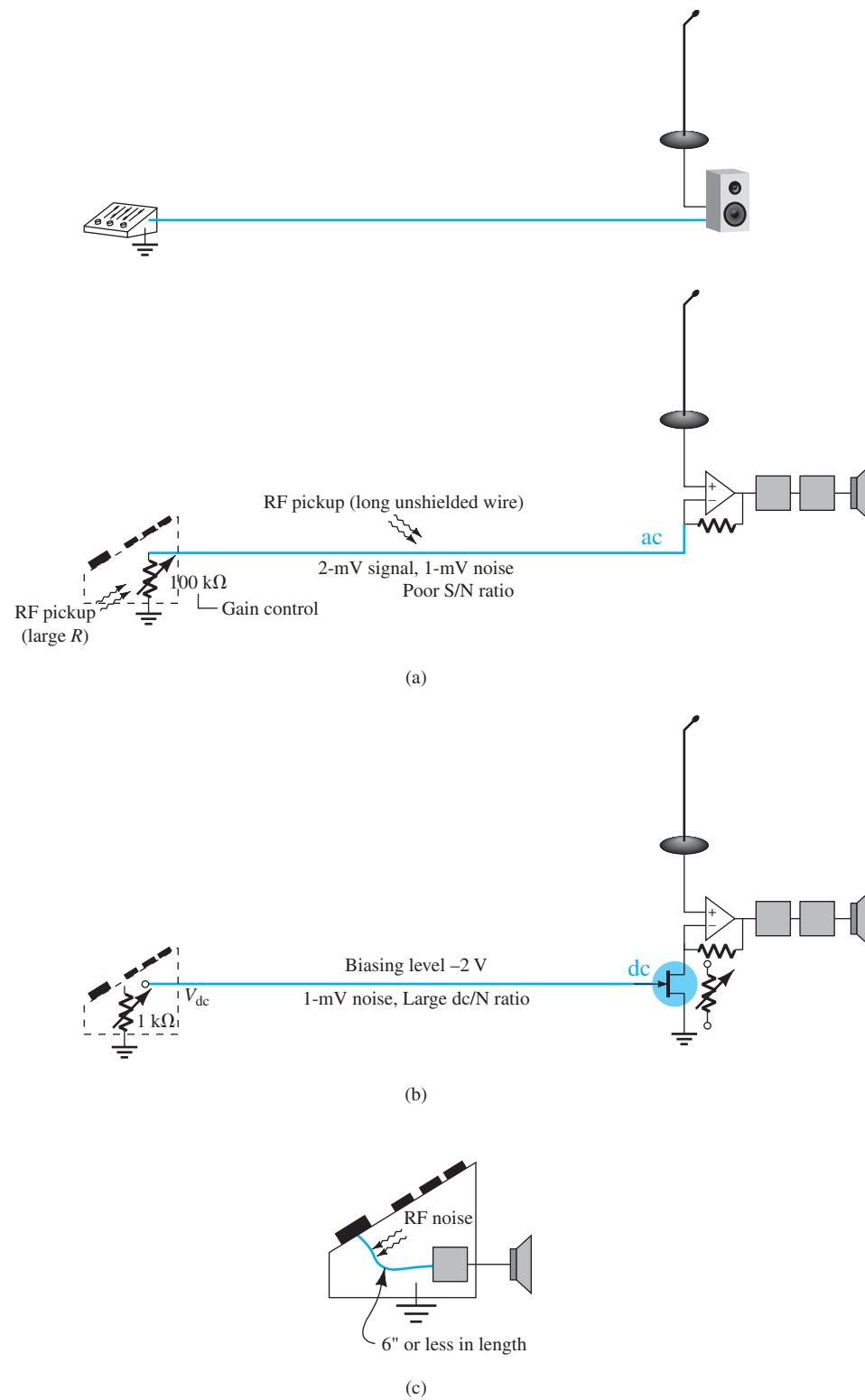
(a) Noninverting op-amp configuration; (b) using the voltage-controlled drain-to-source resistance of a JFET in the noninverting amplifier.

**One of the most important factors that affect the stability of a system is temperature variation.** As a system heats up, the usual tendency is for the gain to increase, which in turn will usually cause additional heating and may eventually result in a condition referred to as “thermal runaway.” Through proper design, a thermistor can be introduced that will affect the biasing level of a voltage-controlled variable JFET resistor. As the resistance of the thermistor drops with increase in heat, the biasing control of the JFET can be such that the drain resistance changes in the amplifier design to reduce the gain—establishing a balancing effect.

Before leaving the subject of thermal problems, note that some design specifications (often military type) require that systems that are overly sensitive to temperature variations be placed in a “chamber” or “oven” to establish a constant heat level. For instance, a 1-W resistor may be placed in an enclosed area with an oscillator network to establish a constant ambient heat level in the region. The design then centers on this heat level, which would be so high compared to the heat normally generated by the components that the variations in temperature levels of the elements could be ignored and a steady output frequency assured.

Other areas of application include any form of volume control, musical effects, meters, attenuators, filters, stability designs, and so on. One general advantage of this type of stability is that it avoids the need for expensive regulators (Chapter 15) in the overall design, although it should be understood that the purpose of this type of control mechanism is to “fine-tune” rather than to provide the primary source of stability.

For the noninverting amplifier, **one of the most important advantages associated with using a JFET for control is the fact that it is dc rather than ac control.** For most systems, dc control not only results in a reduced chance of adding unwanted noise to the system, but also lends itself well to remote control. For example, in Fig. 7.66a, a remote control panel controls the amplifier gain for the speaker by an ac line connected to the variable resistor.



**FIG. 7.66**

Demonstrating the benefits of dc control: system with (a) ac control; (b) dc control; (c) RF noise pickup.

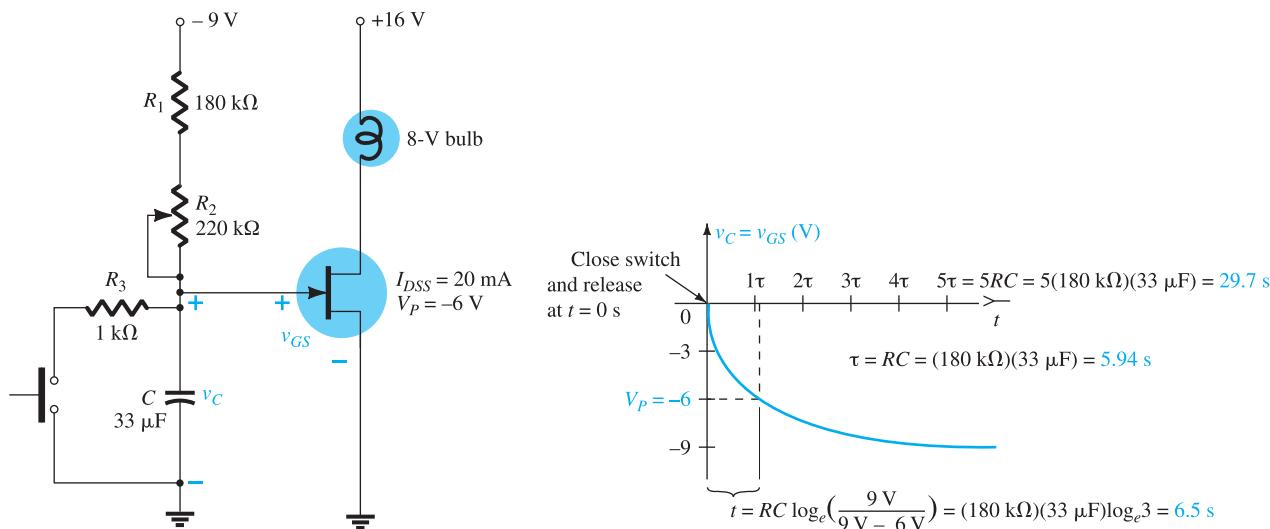
The long line from the amplifier can easily pick up noise from the surrounding air as generated by fluorescent lights, local radio stations, operating equipment (even computers), motors, generators, and so on. The result may be a 2-mV signal on the line with a 1-mV noise level—a terrible signal-to-noise ratio, which would only contribute to further deterioration of the signal coming in from the microphone due to the loop gain of the amplifier. In Fig. 7.66b, a dc line controls the gate voltage of the JFET and the variable resistance of the noninverting amplifier. Even though the dc line voltage on the line may be only  $-2\text{ V}$ , a ripple of 1 mV picked up by the long line will result in a very large signal-to-noise ratio, which could essentially be ignored in the distortion process. In other words, the noise on the dc line would simply move the dc operating point slightly on the device characteristics and would have almost no effect on the resulting drain resistance—isolation between the noise on the line and the amplifier response would be almost ideal.

Even though Figures 7.66a and 7.66b have a relatively long control line, the control line may only be 6" long, as shown in the control panel of Fig. 7.66c, where all the elements of the amplifier are housed in the same container. Consider, however, **that just 1" is enough to pick up RF noise**, so dc control is a favorable characteristic for almost any system. Furthermore, since the control resistance in Fig. 7.66a is usually quite large (hundreds of kilohms), whereas the dc voltage control resistors of the dc system of Fig. 7.66b are usually quite small (a few kilohms), the volume control resistor for the ac system will absorb a great deal more ac noise than the dc design. This phenomenon is a result of the fact that **RF noise signals in the air have a very high internal resistance, and therefore the larger the pickup resistance, the greater is the RF noise absorbed by the receiver**. Recall Thévenin's theorem, which states that for maximum power transfer, the load resistance should equal the internal resistance of the source.

As noted above, **dc control lends itself to computer and remote control systems** since they operate off specific fixed dc levels. For instance, when an infrared (IR) signal is sent out by a remote control to the receiver in a TV or VCR, the signal is passed through a decoder-counter sequence to define a particular dc voltage level on a staircase of voltage levels that can be fed into the gate of the JFET. For a volume control, that gate voltage may control the drain resistance of a noninverting amplifier controlling the volume of the system.

### Timer Network

The high isolation between gate and drain circuits permits the design of a relatively simple timer such as shown in Fig. 7.67. The switch is a normally open (NO) switch, which, when closed, will short out the capacitor and cause its terminal voltage to quickly drop to 0 V. The switching network can handle the rapid discharge of voltage across the capacitor



**FIG. 7.67**  
JFET timer network.

because the working voltages are relatively low and the discharge time is extremely short. Some would say it is a poor design, but in the practical world it is frequently used and not looked on as a terrible crime.

When power is first applied, the capacitor will respond with its short-circuit equivalence since the **voltage across the capacitor cannot change instantaneously**. The result is that the gate-to-source voltage of the JFET will immediately be set to 0 V, the drain current  $I_D$  will equal  $I_{DSS}$ , and the bulb will turn on. However, with the switch in the normally open position, the capacitor will begin to charge to  $-9$  V. **Because of the parallel high input impedance of the JFET, it has essentially no effect on the charging time constant of the capacitor.** Eventually, when the capacitor reaches the pinch-off level, the JFET and bulb will turn off. In general, therefore, when the system is first turned on, the bulb will light for a very short period of time and then turn off. It is now ready to perform its timing function.

When the switch is closed, it will short out the capacitor ( $R_3 \ll R_1, R_2$ ) and will set the voltage at the gate to 0 V. The resulting drain current is  $I_{DSS}$ , and the bulb will burn brightly. When the switch is released, the capacitor will charge toward  $-9$  V, and eventually when it reaches the pinch-off level, the JFET and bulb will turn off. The period during which the bulb is on will be determined by the time constant of the charging network, determined by  $\tau = (R_1 + R_2)C$  and the level of the pinch-off voltage. The more negative the pinch-off level, the longer the bulb will be on. Resistor  $R_1$  is included to be sure that there is some resistance in the charging circuit when the power is turned on. Otherwise, a very heavy current could result that might damage the network. Resistor  $R_2$  is a variable resistor, so the “on” time can be controlled. Resistor  $R_3$  was added to limit the discharge current when the switch is closed. When the switch across the capacitor is closed, the discharge time of the capacitor will be only  $5\tau = 5RC = 5(1\text{ k}\Omega)(33\text{ }\mu\text{F}) = 165\text{ }\mu\text{s} = 0.165\text{ ms} = 0.000165\text{ s}$ . In summary, therefore, when the switch is pressed and released, the bulb will come on brightly, and then, as time goes on, it will become dimmer until it shuts off after a period of time determined by the network time constant.

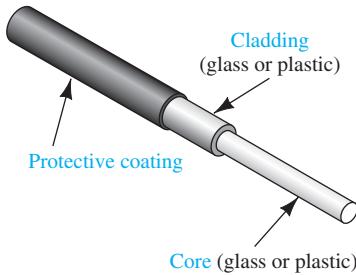
One of the most obvious applications of such a timing system is in a hallway or travel corridor where you want light for a short period of time so that you can pass safely but then want the system to turn off on its own. When you enter or leave a car, you may want a light on for a short period of time but don’t want to worry about turning it off. There are endless possibilities for a timing network such as just described. Just consider the variety of other electrical or electronic systems that you would like to turn on for specific periods of time, and the list of uses grows exponentially.

One might ask why a BJT would not be a good alternative to the JFET for the same application. First, the input resistance of the BJT may be only a few kilohms. That would affect not only the time constant of the charging network, but also the maximum voltage to which the capacitor could charge. Just draw an equivalent network with the transistor replaced by a 1-k $\Omega$  resistor, and the above will immediately become clear. In addition, the control levels will have to be designed with a great deal more care since the BJT transistor turns on at about 0.7 V. The voltage swing from off to on is only 0.7 V rather than 4 V for the JFET configuration. One final note: You might have noticed the absence of a series resistor in the drain circuit for the situation when the bulb is first turned on and the resistance of the bulb is very low. The resulting current could be quite high until the bulb reaches its rated intensity. However, again, as described above for the switch across the capacitor, if the energy levels are small and the duration of stress minimal, such designs are often accepted. If there were any concern, adding a resistor of 0.1 to 1  $\Omega$  in series with the bulb would provide some security.

## Fiber Optic Systems

The introduction of fiber optic technology has had a dramatic effect on the communications industry. The information-carrying capacity of fiber optic cable is significantly greater than that provided by conventional methods with individual pairs of wire. In addition, the cable size is reduced, the cable is less expensive, crosstalk due to electromagnetic effects between current-carrying conductors is eliminated, and noise pickup due to external disturbances such as lightning are eliminated.

The fiber optic industry is based on the fact that information can be transmitted on a beam of light. Although the speed of light through free space is  $3 \times 10^8$  meters per second,

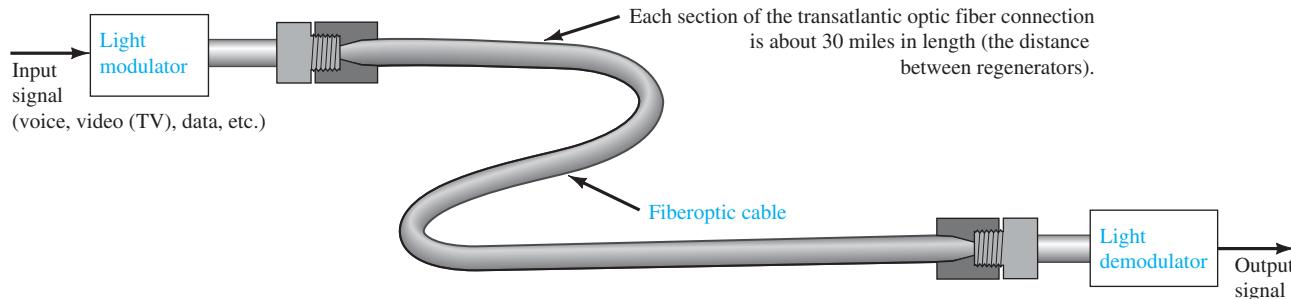
**FIG. 7.68**

Basic elements of a fiber optic cable.

or approximately 186,000 miles per second, its speed will be reduced by encounters with other media, causing reflection and refraction. When light information is passed through a fiber optic cable, it is expected to bounce off the walls of the cable. However, the angle at which the light is injected into the cable is critical, as is the actual design of the cable. In Fig. 7.68, the basic elements of a fiber optic cable are defined. The glass or plastic core of the cable can be as small as  $8 \mu\text{m}$ , which is close to 1/10 the diameter of a human hair. The core is surrounded by an outer layer called the *cladding*, which is also made of glass or plastic, but has a different refractive index to ensure that the light in the core that hits the outer surface of the core is reflected back into the core. A protective coating is then added to protect the two layers from outside environmental effects.

Most optical communication systems work in the infrared frequency range, which extends from  $3 \times 10^{11} \text{ Hz}$  to  $5 \times 10^{14} \text{ Hz}$ . This spectrum is just below the visible light spectrum, which extends from  $5 \times 10^{14} \text{ Hz}$  to  $7.7 \times 10^{14} \text{ Hz}$ . For most optical systems the frequency range of  $1.87 \times 10^{14} \text{ Hz}$  to  $3.75 \times 10^{14} \text{ Hz}$  is used. Because of the very high frequencies, each carrier can be modulated by hundreds or thousands of voice channels simultaneously. In addition, very high speed computer transmission is a possibility, although one must be sure that the electronic components of the modulators can also operate successfully at the same frequency. For distances over 30 nautical miles, repeaters (a combination receiver, amplifier, and transmitter) must be used, which require an additional electrical conductor in the cable that carries a current of about  $1.5 \text{ A}$  at  $2500 \text{ V}$ .

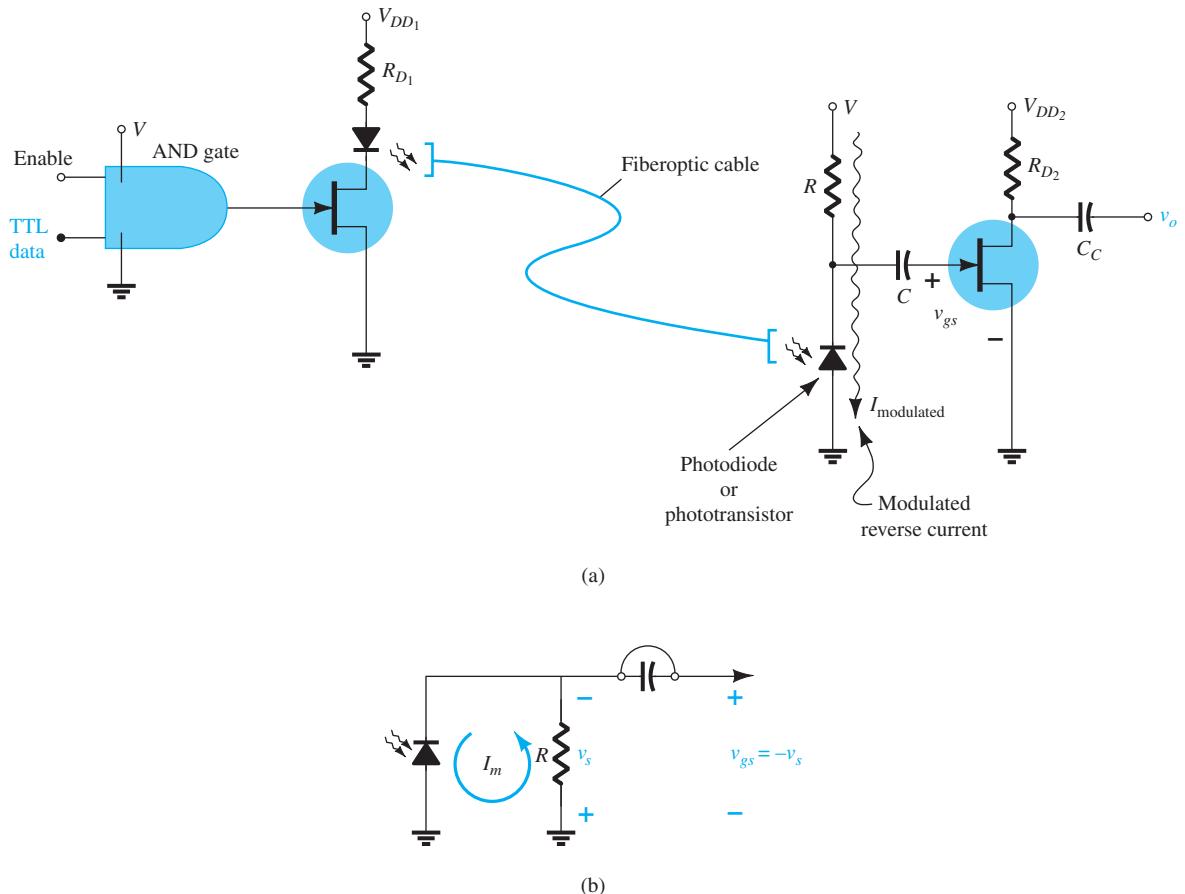
The basic components of an optical communication system are shown in Fig. 7.69. The input signal is applied to a light modulator whose sole purpose is to convert the input signal to one of corresponding levels of light intensity to be directed down the length of fiber optic cable. The information is then carried through the cable to the receiving station, where a light demodulator converts the varying light intensities back to voltage levels that match those of the original signal.



**FIG. 7.69**  
Basic components of an optical communication system.

An electronic equivalent for the transmission of computer transistor-transistor-logic (TTL) information is provided in Fig. 7.70a. With the Enable control in the “on” or 1-state, the TTL information at the input to the AND gate can pass through to the gate of the JFET configuration. The design is such that the discrete levels of voltage associated with the TTL logic will turn the JFET on and off (perhaps  $0 \text{ V}$  and  $-5 \text{ V}$ , respectively, for a JFET with  $V_P = -4 \text{ V}$ ). The resulting change in current levels will result in two distinct levels of light intensity from the LED (Section 1.16) in the drain circuit. That emitted light will then be directed through the cable to the receiving station, where a photodiode (Section 16.6) will react to the incident light and permit different levels of current to pass through as established by  $V$  and  $R$ . The current for photodiodes is a reverse current having the direction shown in Fig. 7.70a, but in the ac equivalent the photodiode and the resistor  $R$  are in parallel as shown in Fig. 7.70b, establishing the desired signal with the polarity shown at the gate of the JFET. Capacitor  $C$  is simply an open circuit to dc to isolate the biasing arrangement for the photodiode from the JFET and a short circuit as shown for the signal  $v_s$ . The incoming signal will then be amplified and will appear at the drain terminal of the output JFET.

As mentioned above, all the elements of the design, including the JFETs, LED, photodiode, capacitors, and so on, must be carefully chosen to ensure that they function properly



**FIG. 7.70**  
TTL fiber optic communication channel: (a) JFET design; (b) passing on the signal generated across the photodiode.

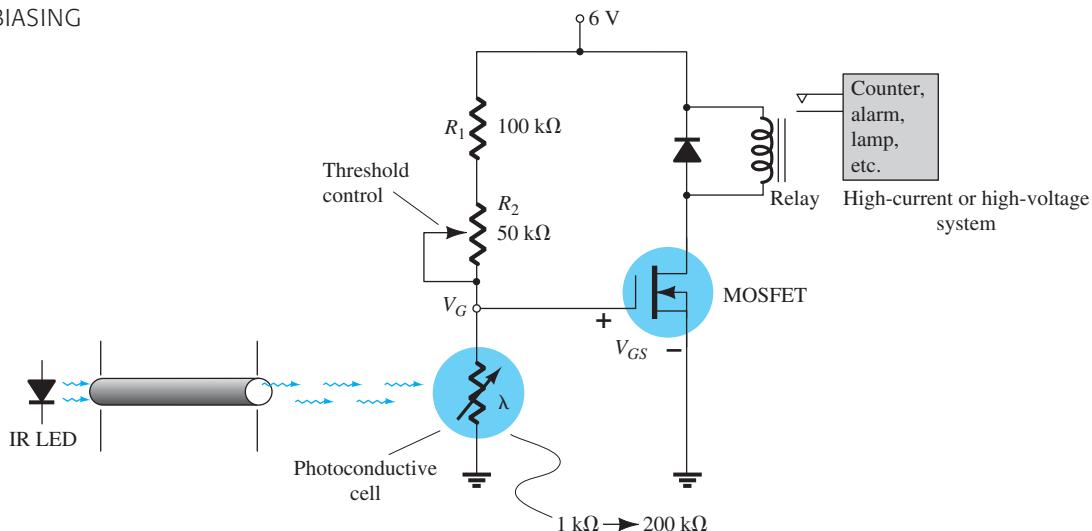
at the high frequency of transmission. In fact, laser diodes are frequently used instead of LEDs in the modulator because they work at higher information rates and higher powers and have lower coupling and transmission losses. However, laser diodes are a great deal more expensive and more temperature sensitive, and they typically have a shorter lifetime than LEDs. For the demodulator side, the photodiodes are either of the pin photodiode or the avalanche photodiode variety. The *pin* abbreviation comes from the *p-intrinsic-n* construction process, and the term *avalanche* from the rapidly growing ionization process that develops during operation.

In general, the JFET is excellent for this application because of its high isolation at the input side and its ability to quickly “snap” from one state to the other due to the TTL input. At the output side the isolation blocks any effect of the demodulator sensing circuit from affecting the ac response, and it provides some gain for the signal before it is passed on to the next stage.

### MOSFET Relay Driver

The MOSFET relay driver to be described in this section is an excellent example of how the FETs can be used to **drive high-current/high-voltage networks without drawing current or power from the driving circuit. The high input impedance of FETs essentially isolates the two parts of the network without the need for optical or electromagnetic linkages.** The network to be described can be used for a variety of applications, but our application will be limited to an alarm system activated when someone or something passes the plane of the transmitted light.

The IR (infrared—not visible) LED of Fig. 7.71 is directing its light through a directional funnel to hit the face of a photoconductive cell (Section 16.7) of the controlling network. The photoconductive cell has a range of resistance from about  $200\text{ k}\Omega$  as its dark



**FIG. 7.71**  
MOSFET relay driver.

resistance level down to less than  $1\text{ k}\Omega$  at high illumination levels. Resistor  $R_1$  is a variable resistance that can be used to set the threshold level of the depletion-type MOSFET. A medium-power MOSFET was employed because of the high level of drain current through the magnetizing coil. The diode is included as a protective device for reasons discussed in detail in Section 2.11.

When the system is on and the light consistently hitting the photoconductive cell, the resistance of the cell may drop to  $10\text{ k}\Omega$ . At this level an application of the voltage-divider rule will result in a voltage of about  $0.54\text{ V}$  at the gate terminal (with the  $50\text{-k}\Omega$  potentiometer set to  $0\text{ k}\Omega$ ). The MOSFET will be on, but not at a drain current level that will cause the relay to change state. When someone passes by, the light source will be cut off, and the resistance of the cell may quickly (in a few microseconds) rise to  $100\text{ k}\Omega$ . The voltage at the gate will then rise to  $3\text{ V}$ , turning on the MOSFET and activating the relay and turning on the system under control. An alarm circuit has its own control design to ensure that it will not turn off when light returns to the photoconductive cell.

In essence, therefore, we have controlled a high-current network with a relatively small dc voltage level and a rather inexpensive design. The only obvious flaw in the design is the fact that the MOSFET will be on even when there is no intrusion. This can be remedied through the use of a more sophisticated design, but keep in mind that **MOSFETs are typically low-power-consumption devices**, so the power loss, even over time, is not that great.

## 7.16 SUMMARY

### Important Conclusions and Concepts

1. A fixed-bias configuration has, as the label implies, a **fixed** dc voltage applied from gate to source to establish the operating point.
2. The **nonlinear** relationship between the gate-to-source voltage and the drain current of a JFET requires that a graphical or mathematical solution (involving the solution of two simultaneous equations) be used to determine the quiescent point of operation.
3. All voltages with a single subscript define a voltage from a specified point to **ground**.
4. The self-bias configuration is determined by an equation for  $V_{GS}$  that will *always* pass through the origin. Any other point determined by the biasing equation will establish a **straight** line to represent the biasing network.
5. For the voltage-divider biasing configuration, one can always assume that the gate current is  $0\text{ A}$  to permit an **isolation** of the voltage-divider network from the output section. The resulting gate-to-ground voltage will always be **positive for an *n*-channel JFET** and **negative for a *p*-channel JFET**. Increasing values of  $R_S$  result in **lower quiescent values of  $I_D$**  and more **negative values of  $V_{GS}$**  for an *n*-channel JFET.

6. The method of analysis applied to depletion-type MOSFETs is the same as applied to JFETs, with the only difference being a possible operating point with an  $I_D$  level **above** the  $I_{DSS}$  value.
7. The characteristics and method of analysis applied to enhancement-type MOSFETs are **entirely different** from those of JFETs and depletion-type MOSFETs. For values of  $V_{GS}$  less than the threshold value, the drain current is 0 A.
8. When analyzing networks with a variety of devices, first work with the region of the network that will provide a **voltage or current level** using the basic relationships associated with those devices. Then use that level and the appropriate equations to find other voltage or current levels of the network in the surrounding region of the system.
9. The design process often requires finding a resistance level to establish the desired voltage or current level. With this in mind, remember that a resistance level is defined by the **voltage across the resistor divided by the current** through the resistor. In the design process, both of these quantities are often available for a particular resistive element.
10. The ability to troubleshoot a network requires a **clear, firm understanding** of the terminal behavior of each of the devices in the network. That knowledge will provide an **estimate** of the working voltage levels of specific points of the network, which can be checked with a voltmeter. The ohmmeter section of a multimeter is particularly helpful in ensuring that there is a **true connection** between all the elements of the network.
11. The analysis of *p*-channel FETs is the same as that applied to *n*-channel FETs except for the fact that all the voltages will have the **opposite polarity** and the currents the **opposite direction**.

## Equations

JFETs/depletion-type MOSFETs:

$$\text{Fixed-bias configuration: } V_{GS} = -V_{GG} = V_G$$

$$\text{Self-bias configuration: } V_{GS} = -I_D R_S$$

$$\text{Voltage-divider biasing: } V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_{GS} = V_G - I_D R_S$$

Enhancement-type MOSFETs:

$$\text{Feedback biasing: } V_{DS} = V_{GS}$$

$$V_{GS} = V_{DD} - I_D R_D$$

$$\text{Voltage-divider biasing: } V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_{GS} = V_G - I_D R_S$$

## 7.17 COMPUTER ANALYSIS

### PSpice Windows

**JFET Voltage-Divider Configuration** The results of Example 7.19 will now be verified using PSpice Windows. The network of Fig. 7.72 is constructed using computer methods described in the previous chapters. The J2N3819 JFET is obtained from the **EVAL** library, and **Edit-PSpice model** is used to set **Beta** to 0.222 mA/V<sup>2</sup> and **Vto** to -6 V. The **Beta** value is determined using  $\beta = I_{DSS}/V_P^2$  Eq. (6.17) and the provided  $I_{DSS}$  and  $V_P$ . The results of the **Simulation** appear in Fig. 7.73 with the dc bias voltage and current levels. The resulting drain current is 4.225 mA, compared to the calculated level of 4.24 mA—an excellent match. The voltage  $V_{GS}$  is 3.504 V - 5.070 V = -1.57 V versus the calculated level of -1.56 V in Example 7.19—another excellent match.

**Combination Network** Next, the result of Example 7.12 with both a transistor and JFET will be verified. For the transistor **Bf** is set to 180, whereas for the JFET, **Beta** is set to 0.333 mA/V<sup>2</sup> and **Vto** to -6 V as called for in the example. The results for all the dc levels appear in Fig. 7.73. Note again the excellent comparison with the calculator solution, with  $V_D$  at 11.44 V compared to 11.07 V,  $V_S = V_C$  at 7.138 V compared to 7.32 V, and  $V_{GS}$  at 3.380 V - 7.138 V = -3.76 V compared to -3.7 V.

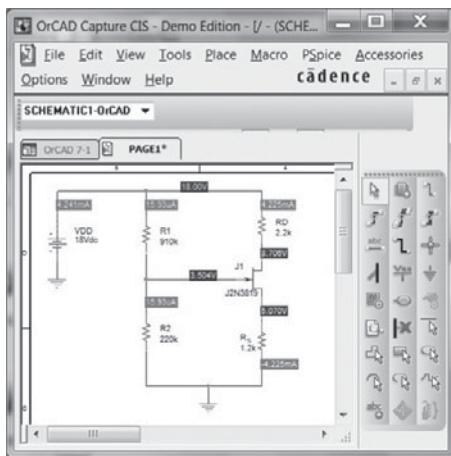


FIG. 7.72

JFET voltage-divider configuration with PSpice Windows results for current and voltage levels.

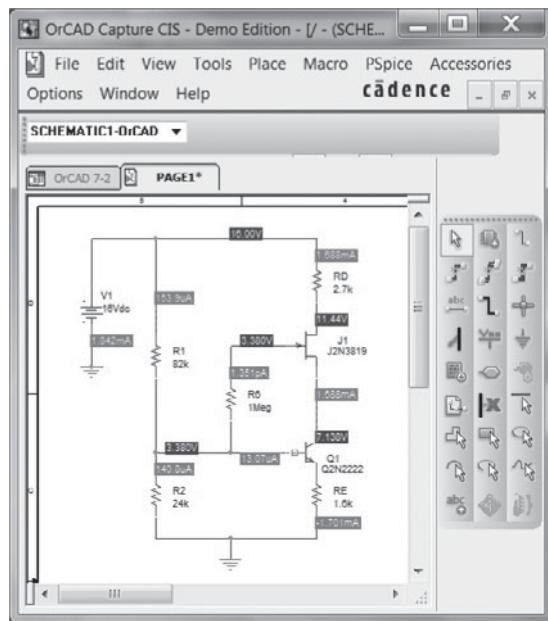


FIG. 7.73

Verifying the hand-calculated solution of Example 7.12 using PSpice Windows.

## Multisim

The results of Example 7.2 will now be verified using Multisim. The construction of the network of Fig. 7.74 is essentially the same as applied in the BJT chapters. The JFET is obtained by selecting **Transistor**, the fourth key down on the first vertical toolbar. A **Select a Component** dialog box will appear, in which **JFET\_N** can be selected under the **Family** listing. A long **Component** list appears, in which **2N3821** is selected for this application. An **OK**, and it can be placed on the screen. After double-clicking the symbol on the screen, a **JFET\_N** dialog box will appear in which **Value** can be selected, followed

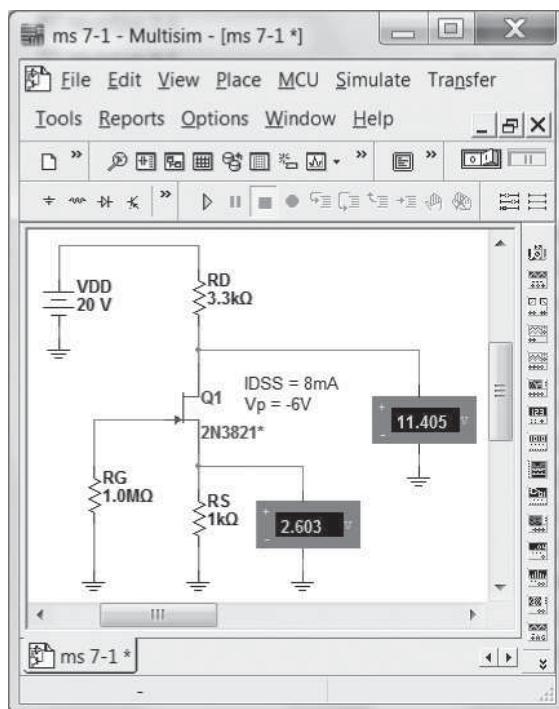


FIG. 7.74

Verifying the results of Example 7.2 using Multisim.

by **Edit Model**. An **Edit Model** dialog box will appear in which **Beta** and **V<sub>to</sub>** can be set to **0.222 mA/V<sup>2</sup>** and **-6 V**, respectively. The value of **Beta** is determined using Eq. (6.17) and the parameters of the network as follows:

$$\text{Beta} = \frac{I_{DSS}}{|V_P|^2} = \frac{8 \text{ mA}}{|-6 \text{ V}|^2} = \frac{8 \text{ mA}}{36 \text{ V}^2} = 0.222 \text{ mA/V}^2$$

Once the change is made, be sure to select **Change Part Model** before leaving the dialog box. The **JFET\_N** dialog box will appear again, but an **OK**, and the changes will be made. The labels **IDSS = 8 mA** and **V<sub>p</sub> = -6 V** are added using **Place-Text**. A blinking vertical bar will appear marking the place where the label can be entered. Once entered, it can easily be moved by simply clicking the area and dragging it to the desired position while holding the clicker down.

Using the **Indicator** option on the first vertical toolbar displays the drain and source voltages as shown in Fig. 7.74. In both cases the **VOLTMETER\_V** option was chosen in the **Select a Component** dialog box.

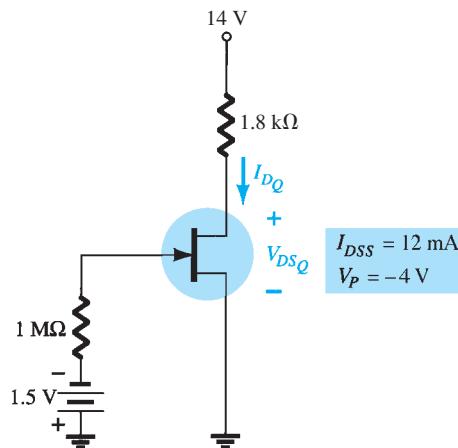
Selecting **Simulate-Run** or moving the switch to the **1** position results in the display of Fig. 7.74. Note that  $V_{GS}$  at  $-2.603 \text{ V}$  is an exact match with the hand-calculated solution of  $-2.6 \text{ V}$ . Although the indicator is connected from source to ground, be aware that this is also the gate-to-source voltage because the voltage drop across the  $1\text{-M}\Omega$  resistor is assumed to be  $0 \text{ V}$ . The level of  $11.405 \text{ V}$  at the drain is very close to the hand-calculated solution of  $11.42 \text{ V}$ —in all, a complete verification of the results of Example 7.2.

## PROBLEMS

\*Note: Asterisks indicate more difficult problems.

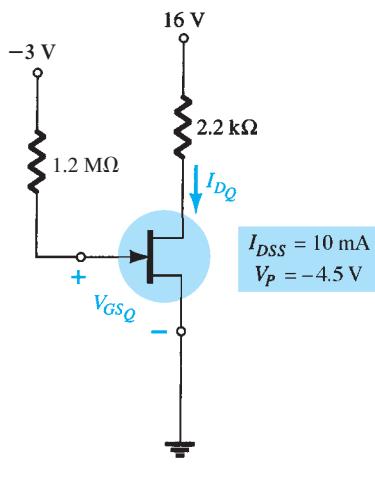
### 7.2 Fixed-Bias Configuration

1. For the fixed-bias configuration of Fig. 7.75:
  - a. Sketch the transfer characteristics of the device.
  - b. Superimpose the network equation on the same graph.
  - c. Determine  $I_{DQ}$  and  $V_{DSQ}$ .
  - d. Using Shockley's equation, solve for  $I_{DQ}$  and then find  $V_{DSQ}$ . Compare with the solutions of part (c).

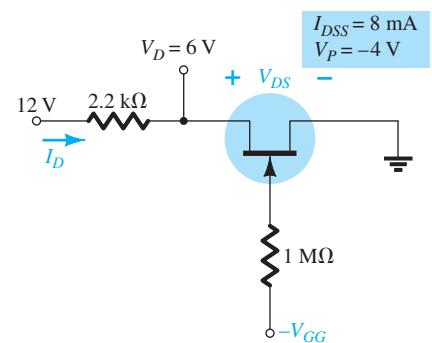


**FIG. 7.75**  
Problems 1 and 37.

2. For the fixed-bias configuration of Fig. 7.76, determine:
  - a.  $I_{DQ}$  and  $V_{GSQ}$  using a purely mathematical approach.
  - b. Repeat part (a) using a graphical approach and compare results.
  - c. Find  $V_{DS}$ ,  $V_D$ ,  $V_G$ , and  $V_S$  using the results of part (a).
3. Given the measured value of  $V_D$  in Fig. 7.77, determine:
  - a.  $I_D$ .
  - b.  $V_{DS}$ .
  - c.  $V_{GG}$ .

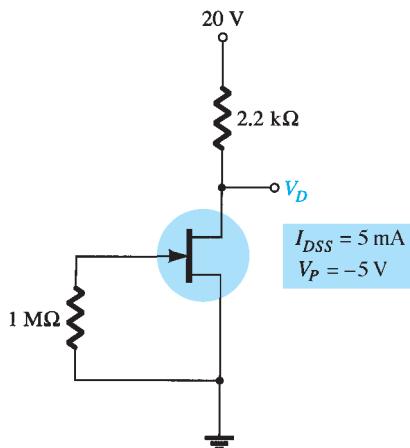


**FIG. 7.76**  
Problem 2.

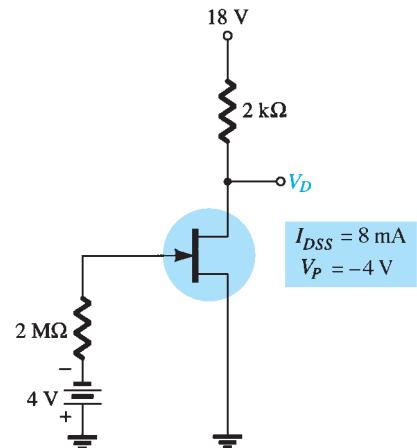


**FIG. 7.77**  
Problem 3.

4. Determine  $V_D$  and  $V_{GS}$  for the fixed-bias configuration of Fig. 7.78.
5. Determine  $V_D$  and  $V_{GS}$  for the fixed-bias configuration of Fig. 7.79.



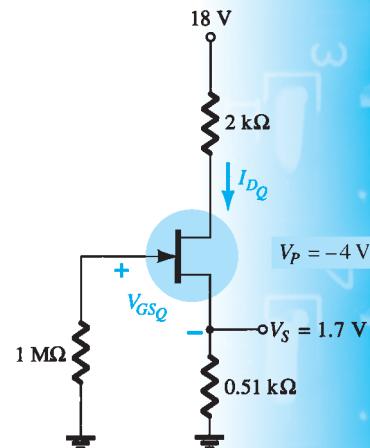
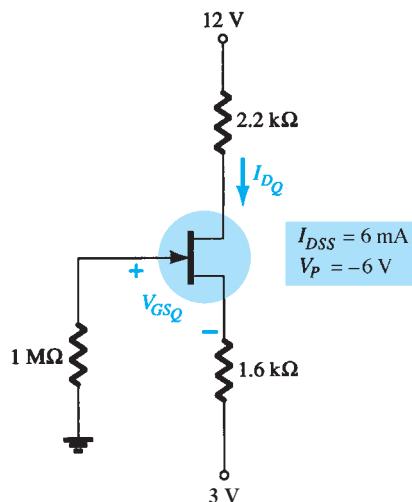
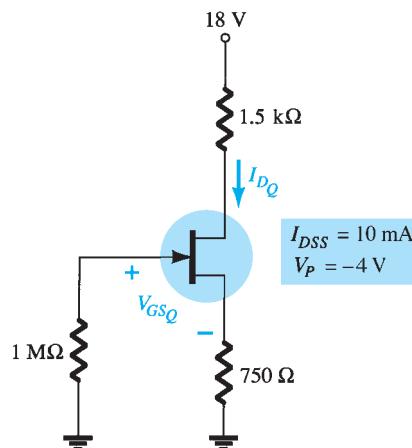
**FIG. 7.78**  
Problem 4.



**FIG. 7.79**  
Problem 5.

### 7.3 Self-Bias Configuration

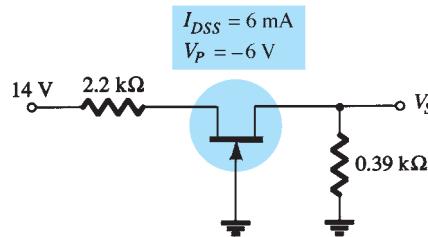
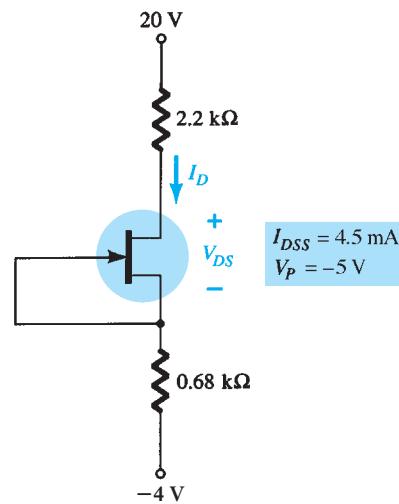
6. For the self-bias configuration of Fig. 7.80:
  - a. Sketch the transfer curve for the device.
  - b. Superimpose the network equation on the same graph.
  - c. Determine  $I_{DQ}$  and  $V_{GSQ}$ .
  - d. Calculate  $V_{DS}$ ,  $V_D$ ,  $V_G$ , and  $V_S$ .
- \*7. Determine  $I_{DQ}$  for the network of Fig. 7.80 using a purely mathematical approach. That is, establish a quadratic equation for  $I_D$  and choose the solution compatible with the network characteristics. Compare to the solution obtained in Problem 6.
8. For the network of Fig. 7.81, determine:
  - a.  $V_{GSQ}$  and  $I_{DQ}$ .
  - b.  $V_{DS}$ ,  $V_D$ ,  $V_G$ , and  $V_S$ .
9. Given the measurement  $V_S = 1.7 \text{ V}$  for the network of Fig. 7.82, determine:
  - a.  $I_{DQ}$ .
  - b.  $V_{GSQ}$ .
  - c.  $I_{DSS}$ .
  - d.  $V_D$ .
  - e.  $V_{DS}$ .



- \*10. For the network of Fig. 7.83, determine:

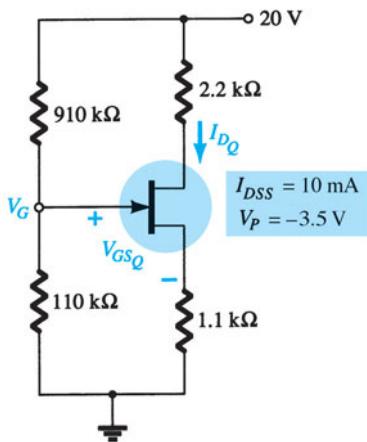
- $I_D$ .
- $V_{DS}$ .
- $V_D$ .
- $V_S$ .

- \*11. Find  $V_S$  for the network of Fig. 7.84.

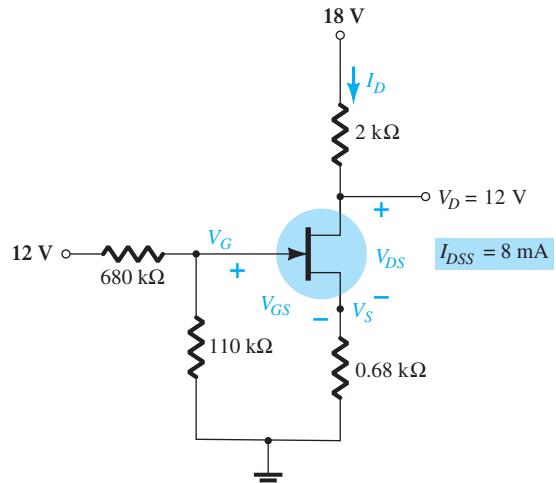


#### 7.4 Voltage-Divider Biasing

12. For the network of Fig. 7.85, determine:
- $V_G$ .
  - $I_DQ$  and  $V_{GSQ}$ .
  - $V_D$  and  $V_S$ .
  - $V_{DSQ}$ .
13. a. Repeat Problem 12 with  $R_S = 0.51 \text{ k}\Omega$  (about 50% of the value of that of Problem 12). What is the effect of a smaller  $R_S$  on  $I_{DQ}$  and  $V_{GSQ}$ ?  
b. What is the minimum possible value of  $R_S$  for the network of Fig. 7.85?
14. For the network of Fig. 7.86,  $V_D = 12 \text{ V}$ . Determine:
- $I_D$ .
  - $V_S$  and  $V_{DS}$ .
  - $V_G$  and  $V_{GS}$ .
  - $V_P$ .

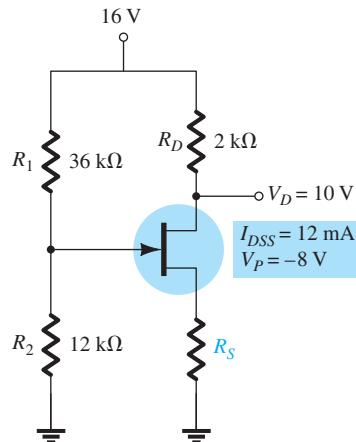


**FIG. 7.85**  
Problems 12 and 13.



**FIG. 7.86**  
Problem 14.

15. Determine the value of  $R_S$  for the network of Fig. 7.87 to establish  $V_D = 10 \text{ V}$ .



**FIG. 7.87**  
Problem 15.

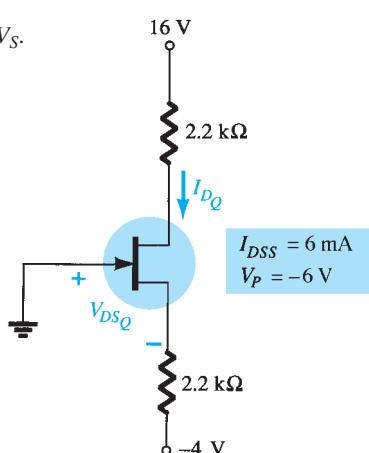
### 7.5 Common-Gate Configuration

- \*16. For the network of Fig. 7.88, determine:

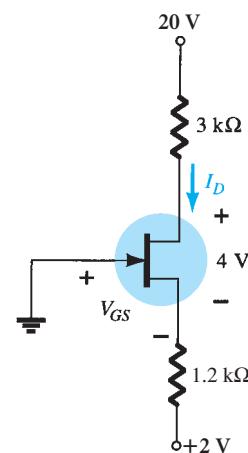
- $I_{DQ}$  and  $V_{GSQ}$ .
- $V_{DS}$  and  $V_S$ .

- \*17. Given  $V_{DS} = 4 \text{ V}$  for the network of Fig. 7.89, determine:

- $I_D$ .
- $V_D$  and  $V_S$ .
- $V_{GS}$ .



**FIG. 7.88**  
Problems 16 and 39.



**FIG. 7.89**  
Problem 17.

### 7.6 Special Case: $V_{GSQ} = 0 \text{ V}$

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18. For the network of Fig. 7.90.
  - a. Find  $I_{DQ}$ .
  - b. Determine  $V_{DQ}$  and  $V_{DSQ}$ .
  - c. Find the power supplied by the source and dissipated by the device.
19. Determine  $V_D$  and  $V_{GS}$  for the network of Fig. 7.91 using the provided information.

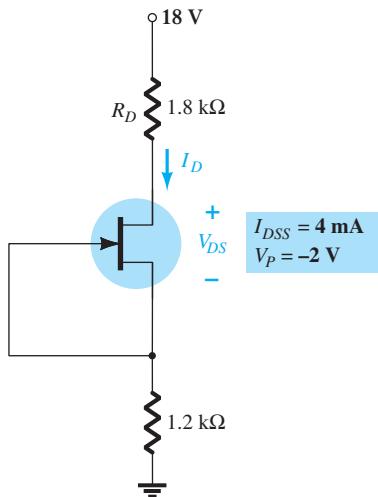


FIG. 7.90

Problem 18.

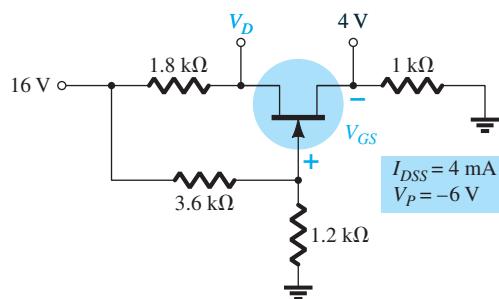


FIG. 7.91

Problem 19.

### 7.7 Depletion-Type MOSFETs

20. For the self-bias configuration of Fig. 7.92, determine:
  - a.  $I_{DQ}$  and  $V_{GSQ}$ .
  - b.  $V_{DS}$  and  $V_D$ .
- \*21. For the network of Fig. 7.93, determine:
  - a.  $I_{DQ}$  and  $V_{GSQ}$ .
  - b.  $V_{DS}$  and  $V_S$ .

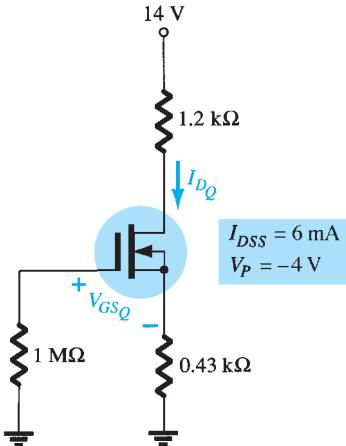


FIG. 7.92

Problem 20.

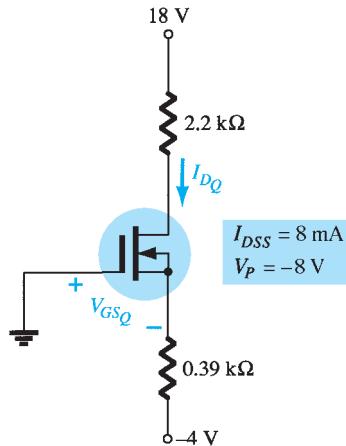
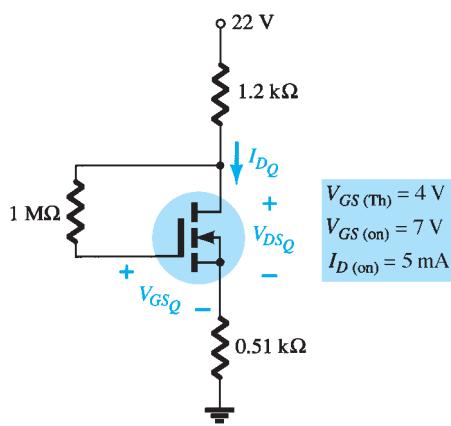
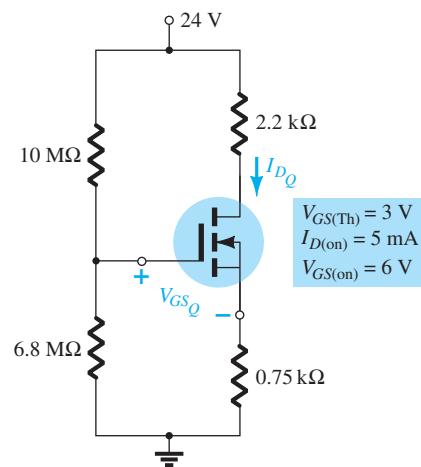


FIG. 7.93

Problem 21.

### 7.8 Enhancement-Type MOSFETs

22. For the network of Fig. 7.94, determine:
  - a.  $I_{DQ}$ .
  - b.  $V_{GSQ}$  and  $V_{DSQ}$ .
  - c.  $V_D$  and  $V_S$ .
  - d.  $V_{DS}$ .
23. For the voltage-divider configuration of Fig. 7.95, determine:
  - a.  $I_{DQ}$  and  $V_{GSQ}$ .
  - b.  $V_D$  and  $V_S$ .

FIG. 7.94  
Problem 22.FIG. 7.95  
Problem 23.

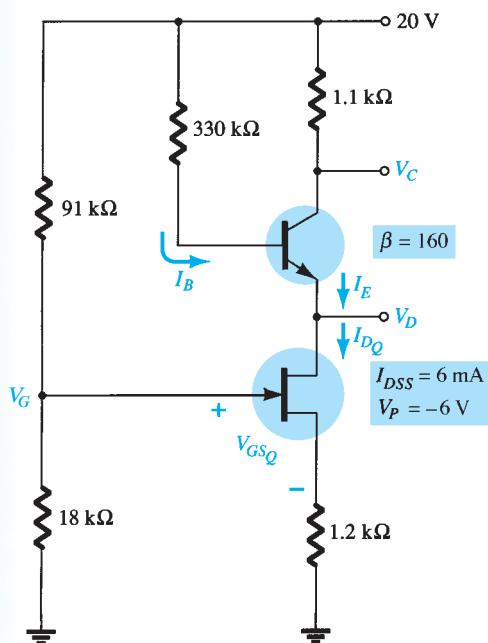
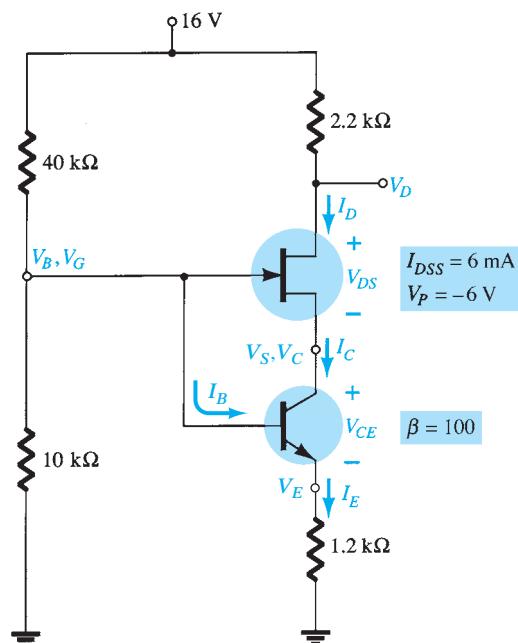
## 7.10 Combination Networks

\*24. For the network of Fig. 7.96, determine:

- a.  $V_G$ .
- b.  $V_{GSQ}$  and  $I_{DQ}$ .
- c.  $I_E$ .
- d.  $I_B$ .
- e.  $V_D$ .
- f.  $V_C$ .

\*25. For the combination network of Fig. 7.97, determine:

- a.  $V_B$  and  $V_G$ .
- b.  $V_E$ .
- c.  $I_E$ ,  $I_C$ , and  $I_D$ .
- d.  $I_B$ .
- e.  $V_C$ ,  $V_S$ , and  $V_D$ .
- f.  $V_{CE}$ .
- g.  $V_{DS}$ .

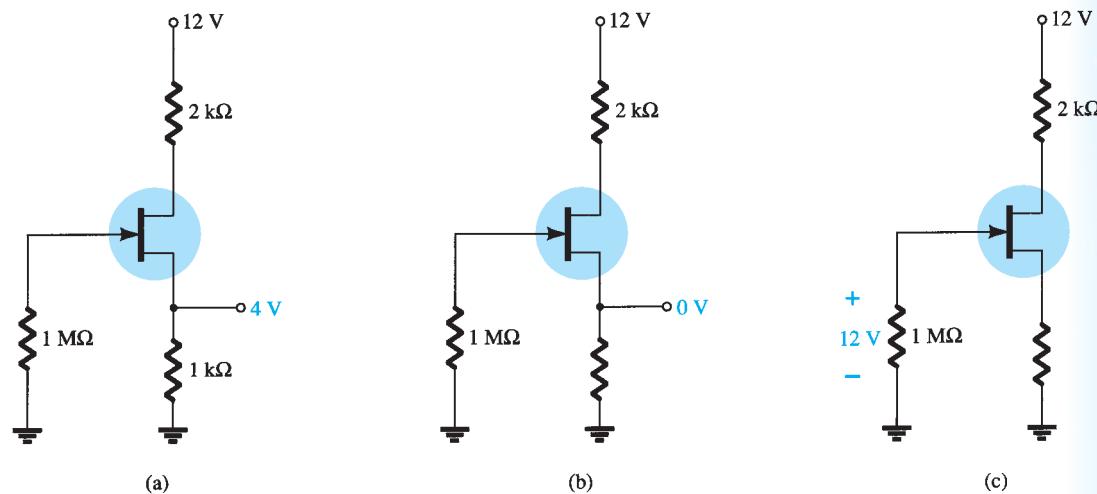
FIG. 7.96  
Problem 24.FIG. 7.97  
Problem 25.

**7.11 Design**

- \*26. Design a self-bias network using a JFET transistor with  $I_{DSS} = 8 \text{ mA}$  and  $V_P = -6 \text{ V}$  to have a  $Q$ -point at  $I_{DQ} = 4 \text{ mA}$  using a supply of 14 V. Assume that  $R_D = 3R_S$  and use standard values.
- \*27. Design a voltage-divider bias network using a depletion-type MOSFET with  $I_{DSS} = 10 \text{ mA}$  and  $V_P = -4 \text{ V}$  to have a  $Q$ -point at  $I_{DQ} = 2.5 \text{ mA}$  using a supply of 24 V. In addition, set  $V_G = 4 \text{ V}$  and use  $R_D = 2.5R_S$  with  $R_L = 22 \text{ M}\Omega$ . Use standard values.
28. Design a network such as appears in Fig. 7.39 using an enhancement-type MOSFET with  $V_{GS(\text{Th})} = 4 \text{ V}$  and  $k = 0.5 \times 10^{-3} \text{ A/V}^2$  to have a  $Q$ -point of  $I_{DQ} = 6 \text{ mA}$ . Use a supply of 16 V and standard values.

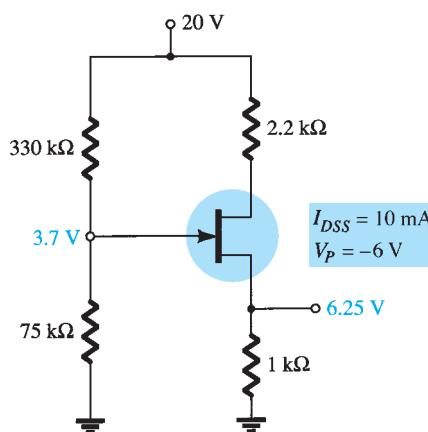
**7.12 Troubleshooting**

- \*29. What do the readings for each configuration of Fig. 7.98 suggest about the operation of the network?

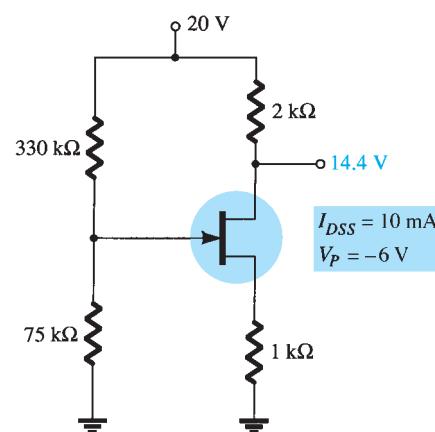


**FIG. 7.98**  
Problem 29.

- \*30. Although the readings of Fig. 7.99 initially suggest that the network is behaving properly, determine a possible cause for the undesirable state of the network.
- \*31. The network of Fig. 7.100 is not operating properly. What is the specific cause for its failure?



**FIG. 7.99**  
Problem 30.



**FIG. 7.100**  
Problem 31.

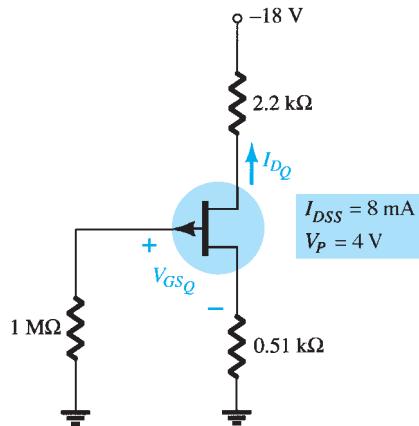
**7.13 p-Channel FETs**

32. For the network of Fig. 7.101, determine:

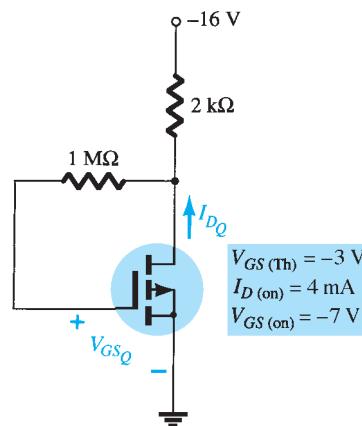
- $I_{DQ}$  and  $V_{GSQ}$ .
- $V_{DS}$ .
- $V_D$ .

33. For the network of Fig. 7.102, determine:

- $I_{DQ}$  and  $V_{GSQ}$ .
- $V_{DS}$ .
- $V_D$ .



**FIG. 7.101**  
Problem 32.



**FIG. 7.102**  
Problem 33.

**7.14 Universal JFET Bias Curve**

- Repeat Problem 1 using the universal JFET bias curve.
- Repeat Problem 6 using the universal JFET bias curve.
- Repeat Problem 12 using the universal JFET bias curve.
- Repeat Problem 16 using the universal JFET bias curve.

**7.15 Computer Analysis**

- Perform a PSpice Windows analysis of the network of Problem 1.
- Perform a PSpice Windows analysis of the network of Problem 6.
- Perform a Multisim analysis of the network of Problem 16.
- Perform a Multisim analysis of the network of Problem 33.

# 8

## FET Amplifiers

### CHAPTER OBJECTIVES

- Become acquainted with the small-signal ac model for a JFET and MOSFET.
- Be able to perform a small-signal ac analysis of a variety of JFET and MOSFET configurations.
- Begin to appreciate the design sequence applied to FET configurations.
- Understand the effects of a source resistor and load resistor on the input impedance, output impedance and overall gain.
- Be able to analyze cascaded configurations with FETs and/or BJT amplifiers.

### 8.1 INTRODUCTION

Field-effect transistor amplifiers provide an excellent voltage gain with the added feature of a high input impedance. They are also low-power-consumption configurations with good frequency range and minimal size and weight. JFETs, depletion MOSFETs, and MESFETs can be used to design amplifiers having similar voltage gains. The depletion MOSFET (MESFET) circuit, however, has a much higher input impedance than a similar JFET configuration.

Whereas a BJT device controls a large output (collector) current by means of a relatively small input (base) current, the FET device controls an output (drain) current by means of a small input (gate-voltage) voltage. In general, therefore, the BJT is a *current-controlled* device and the FET is a *voltage-controlled* device. In both cases, however, note that the output current is the controlled variable. Because of the high input characteristic of FETs, the ac equivalent model is somewhat simpler than that employed for BJTs. Whereas the BJT has an amplification factor,  $\beta$  (beta), the FET has a transconductance factor,  $g_m$ .

The FET can be used as a linear amplifier or as a digital device in logic circuits. In fact, the enhancement MOSFET is quite popular in digital circuitry, especially in CMOS circuits that require very low power consumption. FET devices are also widely used in high-frequency applications and in buffering (interfacing) applications. Table 8.1 in Section 8.13 provides a summary of FET small-signal amplifier circuits and related formulas.

Although the common-source configuration is the most popular one, providing an inverted, amplified signal, one also finds common-drain (source-follower) circuits providing unity gain with no inversion and common-gate circuits providing gain with no inversion. As with BJT amplifiers, the important circuit features described in this chapter include voltage gain, input impedance, and output impedance. Due to the very high input impedance, the input current is generally assumed to be 0  $\mu$ A and the current gain is an undefined quantity.

Whereas the voltage gain of an FET amplifier is generally less than that obtained using a BJT amplifier, the FET amplifier provides a much higher input impedance than that of a BJT configuration. Output impedance values are comparable for both BJT and FET circuits.

FET ac amplifier networks can also be analyzed using computer software. Using PSpice or Multisim, one can perform a dc analysis to obtain the circuit bias conditions and an ac analysis to determine the small-signal voltage gain. Using PSpice transistor models, one can analyze the circuit using specific transistor models. On the other hand, one can develop a program using a language such as C++ that can perform both the dc and ac analyses and provide the results in a very special format.

## 8.2 JFET SMALL-SIGNAL MODEL

The ac analysis of a JFET configuration requires that a small-signal ac model for the JFET be developed. A major component of the ac model will reflect the fact that an ac voltage applied to the input gate-to-source terminals will control the level of current from drain to source.

**The gate-to-source voltage controls the drain-to-source (channel) current of a JFET.**

Recall from Chapter 7 that a dc gate-to-source voltage controls the level of dc drain current through a relationship known as Shockley's equation:  $I_D = I_{DSS}(1 - V_{GS}/V_P)^2$ . The *change* in drain current that will result from a *change* in gate-to-source voltage can be determined using the transconductance factor  $g_m$  in the following manner:

$$\Delta I_D = g_m \Delta V_{GS} \quad (8.1)$$

The prefix *trans-* in the terminology applied to  $g_m$  reveals that it establishes a relationship between an output and an input quantity. The root word *conductance* was chosen because  $g_m$  is determined by a current-to-voltage ratio similar to the ratio that defines the conductance of a resistor,  $G = 1/R = I/V$ .

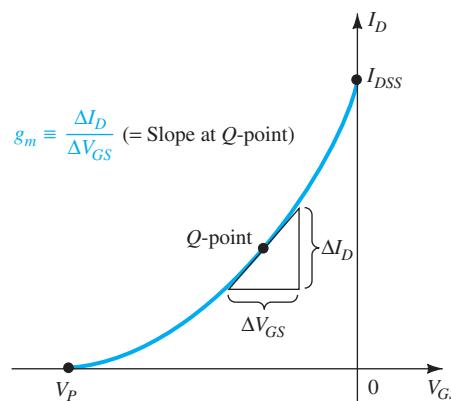
Solving for  $g_m$  in Eq. (8.1), we have

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \quad (8.2)$$

### Graphical Determination of $g_m$

If we now examine the transfer characteristics of Fig. 8.1, we find that  $g_m$  is actually the slope of the characteristics at the point of operation. That is,

$$g_m = m = \frac{\Delta y}{\Delta x} = \frac{\Delta I_D}{\Delta V_{GS}} \quad (8.3)$$



**FIG. 8.1**  
Definition of  $g_m$  using transfer characteristic.

Following the curvature of the transfer characteristics, it is reasonably clear that the slope and, therefore,  $g_m$  increase as we progress from  $V_P$  to  $I_{DSS}$ . In other words, as  $V_{GS}$  approaches 0 V, the magnitude of  $g_m$  increases.

Equation (8.2) reveals that  $g_m$  can be determined at any  $Q$ -point on the transfer characteristics by simply choosing a finite increment in  $V_{GS}$  (or in  $I_D$ ) about the  $Q$ -point and then finding the corresponding change in  $I_D$  (or  $V_{GS}$ , respectively). The resulting changes in each quantity are then substituted in Eq. (8.2) to determine  $g_m$ .

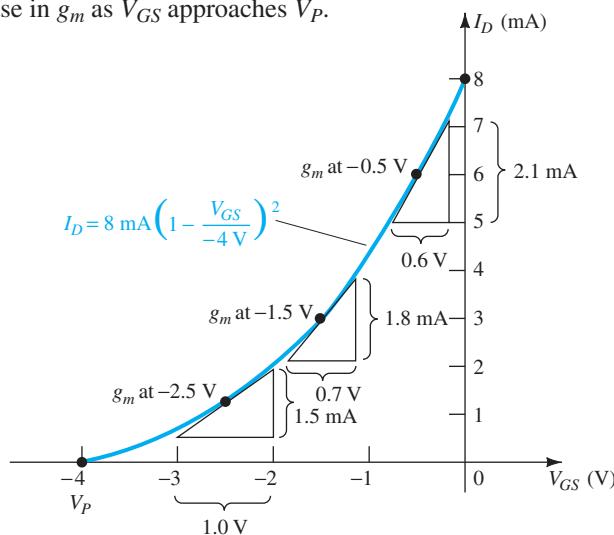
**EXAMPLE 8.1** Determine the magnitude of  $g_m$  for a JFET with  $I_{DSS} = 8 \text{ mA}$  and  $V_P = -4 \text{ V}$  at the following dc bias points:

- $V_{GS} = -0.5 \text{ V}$ .
- $V_{GS} = -1.5 \text{ V}$ .
- $V_{GS} = -2.5 \text{ V}$ .

**Solution:** The transfer characteristics are generated as Fig. 8.2 using the procedure defined in Chapter 7. Each operating point is then identified and a tangent line is drawn at each point to best reflect the slope of the transfer curve in this region. An appropriate increment is then chosen for  $V_{GS}$  to reflect a variation to either side of each  $Q$ -point. Equation (8.2) is then applied to determine  $g_m$ .

- $g_m = \frac{\Delta I_D}{\Delta V_{GS}} \cong \frac{2.1 \text{ mA}}{0.6 \text{ V}} = 3.5 \text{ mS}$
- $g_m = \frac{\Delta I_D}{\Delta V_{GS}} \cong \frac{1.8 \text{ mA}}{0.7 \text{ V}} \cong 2.57 \text{ mS}$
- $g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{1.5 \text{ mA}}{1.0 \text{ V}} = 1.5 \text{ mS}$

Note the decrease in  $g_m$  as  $V_{GS}$  approaches  $V_P$ .



**FIG. 8.2**  
Calculating  $g_m$  at various bias points.

### Mathematical Definition of $g_m$

The graphical procedure just described is limited by the accuracy of the transfer plot and the care with which the changes in each quantity can be determined. Naturally, the larger the graph, the better is the accuracy, but this can then become a cumbersome problem. An alternative approach to determining  $g_m$  employs the approach used to find the ac resistance of a diode in Chapter 1, where it was stated that:

*The derivative of a function at a point is equal to the slope of the tangent line drawn at that point.*

If we therefore take the derivative of  $I_D$  with respect to  $V_{GS}$  (differential calculus) using Shockley's equation, we can derive an equation for  $g_m$  as follows:

$$\begin{aligned} g_m &= \frac{dI_D}{dV_{GS}} \Big|_{Q\text{-pt.}} = \frac{d}{dV_{GS}} \left[ I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 \right] \\ &= I_{DSS} \frac{d}{dV_{GS}} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 = 2I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right] \frac{d}{dV_{GS}} \left( 1 - \frac{V_{GS}}{V_P} \right) \\ &= 2I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right] \left[ \frac{d}{dV_{GS}} (1) - \frac{1}{V_P} \frac{dV_{GS}}{dV_{GS}} \right] = 2I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right] \left[ 0 - \frac{1}{V_P} \right] \end{aligned}$$

and

$$g_m = \frac{2I_{DSS}}{|V_P|} \left[ 1 - \frac{V_{GS}}{V_P} \right] \quad (8.4)$$

where  $|V_P|$  denotes magnitude only, to ensure a positive value for  $g_m$ .

It was mentioned earlier that the slope of the transfer curve is a maximum at  $V_{GS} = 0$  V. Plugging in  $V_{GS} = 0$  V into Eq. (8.4) results in the following equation for the maximum value of  $g_m$  for a JFET in which  $I_{DSS}$  and  $V_P$  have been specified:

$$g_m = \frac{2I_{DSS}}{|V_P|} \left[ 1 - \frac{0}{V_P} \right]$$

and

$$g_{m0} = \frac{2I_{DSS}}{|V_P|} \quad (8.5)$$

where the added subscript 0 reminds us that it is the value of  $g_m$  when  $V_{GS} = 0$  V. Equation (8.4) then becomes

$$g_m = g_{m0} \left[ 1 - \frac{V_{GS}}{V_P} \right] \quad (8.6)$$

**EXAMPLE 8.2** For the JFET having the transfer characteristics of Example 8.1:

- Find the maximum value of  $g_m$ .
- Find the value of  $g_m$  at each operating point of Example 8.1 using Eq. (8.6) and compare with the graphical results.

**Solution:**

a.  $g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(8 \text{ mA})}{4 \text{ V}} = 4 \text{ mS}$  (maximum possible value of  $g_m$ )

b. At  $V_{GS} = -0.5$  V,

$$g_m = g_{m0} \left[ 1 - \frac{V_{GS}}{V_P} \right] = 4 \text{ mS} \left[ 1 - \frac{-0.5 \text{ V}}{-4 \text{ V}} \right] = 3.5 \text{ mS} \quad (\text{vs. } 3.5 \text{ mS graphically})$$

At  $V_{GS} = -1.5$  V,

$$g_m = g_{m0} \left[ 1 - \frac{V_{GS}}{V_P} \right] = 4 \text{ mS} \left[ 1 - \frac{-1.5 \text{ V}}{-4 \text{ V}} \right] = 2.5 \text{ mS} \quad (\text{vs. } 2.57 \text{ mS graphically})$$

At  $V_{GS} = -2.5$  V,

$$g_m = g_{m0} \left[ 1 - \frac{V_{GS}}{V_P} \right] = 4 \text{ mS} \left[ 1 - \frac{-2.5 \text{ V}}{-4 \text{ V}} \right] = 1.5 \text{ mS} \quad (\text{vs. } 1.5 \text{ mS graphically})$$

The results of Example 8.2 are certainly sufficiently close to validate Eq. (8.4) through (8.6) for future use when  $g_m$  is required.

On specification sheets,  $g_m$  is often provided as  $g_{fs}$  or  $y_{fs}$ , where  $y$  indicates it is part of an admittance equivalent circuit. The  $f$  signifies forward transfer conductance, and the  $s$  indicates that it is connected to the source terminal.

In equation form,

$$g_m = g_{fs} = y_{fs} \quad (8.7)$$

For the JFET of Fig. 6.20,  $g_{fs}$  ranges from  $1000 \mu\text{S}$  to  $5000 \mu\text{S}$ , or  $1 \text{ mS}$  to  $5 \text{ mS}$ .

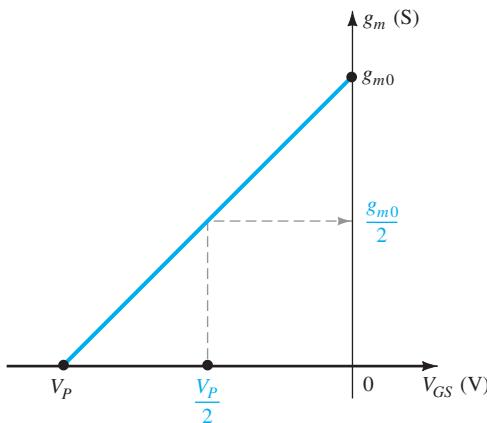
### Plotting $g_m$ versus $V_{GS}$

Since the factor  $\left(1 - \frac{V_{GS}}{V_P}\right)$  of Eq. (8.6) is less than 1 for any value of  $V_{GS}$  other than 0 V, the magnitude of  $g_m$  will decrease as  $V_{GS}$  approaches  $V_P$  and the ratio  $\frac{V_{GS}}{V_P}$  increases in magnitude. At  $V_{GS} = V_P$ ,  $g_m = g_{m0}(1 - 1) = 0$ . Equation (8.6) defines a straight line with a minimum value of 0 and a maximum value of  $g_m$ , as shown by the plot of Fig. 8.3.

In general, therefore

**the maximum value of  $g_m$  occurs where  $V_{GS} = 0 \text{ V}$  and the minimum value at  $V_{GS} = V_P$ . The more negative the value of  $V_{GS}$  the less the value of  $g_m$ .**

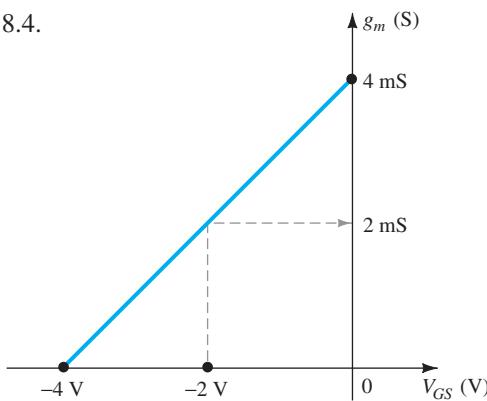
Figure 8.3 also shows that when  $V_{GS}$  is one-half the pinch-off value,  $g_m$  is one-half the maximum value.



**FIG. 8.3**  
Plot of  $g_m$  versus  $V_{GS}$

**EXAMPLE 8.3** Plot  $g_m$  versus  $V_{GS}$  for the JFET of Examples 8.1 and 8.2.

**Solution:** Note Fig. 8.4.



**FIG. 8.4**  
Plot of  $g_m$  versus  $V_{GS}$  for a JFET with  $I_{DSS} = 8 \text{ mA}$  and  $V_p = -4 \text{ V}$ .

### Effect of $I_D$ on $g_m$

A mathematical relationship between  $g_m$  and the dc bias current  $I_D$  can be derived by noting that Shockley's equation can be written in the following form:

$$1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}} \quad (8.8)$$

Substituting Eq. (8.8) into Eq. (8.6) results in

$$g_m = g_{m0} \left( 1 - \frac{V_{GS}}{V_P} \right) = g_{m0} \sqrt{\frac{I_D}{I_{DSS}}} \quad (8.9)$$

Using Eq. (8.9) to determine  $g_m$  for a few specific values of  $I_D$ , we obtain the following results:

- a. If  $I_D = I_{DSS}$ ,

$$g_m = g_{m0} \sqrt{\frac{I_{DSS}}{I_{DSS}}} = g_{m0}$$

- b. If  $I_D = I_{DSS}/2$ ,

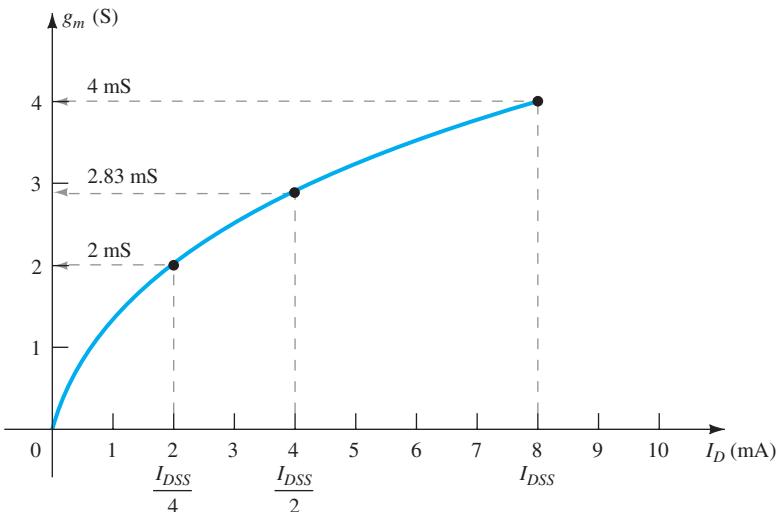
$$g_m = g_{m0} \sqrt{\frac{I_{DSS}/2}{I_{DSS}}} = 0.707g_{m0}$$

- c. If  $I_D = I_{DSS}/4$ ,

$$g_m = g_{m0} \sqrt{\frac{I_{DSS}/4}{I_{DSS}}} = \frac{g_{m0}}{2} = 0.5g_{m0}$$

**EXAMPLE 8.4** Plot  $g_m$  versus  $I_D$  for the JFET of Examples 8.1 through 8.3.

**Solution:** See Fig. 8.5.



**FIG. 8.5**  
Plot of  $g_m$  versus  $I_D$  for a JFET with  $I_{DSS} = 8$  mA and  $V_{GS} = -4$  V.

The plots of Examples 8.3 and 8.4 clearly reveal that

**the highest values of  $g_m$  are obtained when  $V_{GS}$  approaches 0 V and  $I_D$  approaches its maximum value of  $I_{DSS}$ .**

The input impedance of all commercially available JFETs is sufficiently large to assume that the input terminals approximate an open circuit. In equation form,

$$Z_i (\text{JFET}) = \infty \Omega \quad (8.10)$$

For a JFET a practical value of  $10^9 \Omega$  (1000 M $\Omega$ ) is typical, whereas a value of  $10^{12} \Omega$  to  $10^{15} \Omega$  is typical for MOSFETs and MESFETs.

### JFET Output Impedance $Z_o$

The output impedance of JFETs is similar in magnitude to that of conventional BJTs. On JFET specification sheets, the output impedance will typically appear as  $g_{os}$  or  $y_{os}$  with the units of  $\mu\text{S}$ . The parameter  $y_{os}$  is a component of an *admittance equivalent circuit*, with the subscript  $o$  signifying an *output* network parameter and  $s$  the terminal (source) to which it is attached in the model. For the JFET of Fig. 6.20,  $g_{os}$  has a range of  $10 \mu\text{S}$  to  $50 \mu\text{S}$  or  $20 \text{k}\Omega (R = 1/G = 1/50 \mu\text{S})$  to  $100 \text{k}\Omega (R = 1/G = 1/10 \mu\text{S})$ .

In equation form,

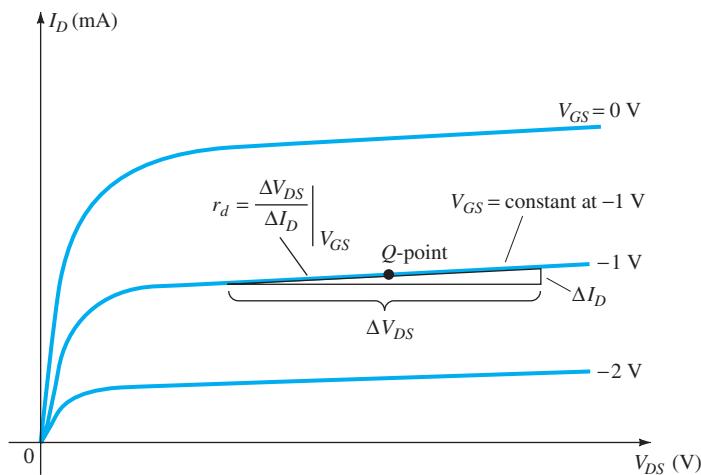
$$Z_o (\text{JFET}) = r_d = \frac{1}{g_{os}} = \frac{1}{y_{os}} \quad (8.11)$$

The output impedance is defined on the characteristics of Fig. 8.6 as the slope of the horizontal characteristic curve at the point of operation. The more horizontal the curve, the greater is the output impedance. If it is perfectly horizontal, the ideal situation is on hand with the output impedance being infinite (an open circuit)—an often applied approximation.

In equation form,

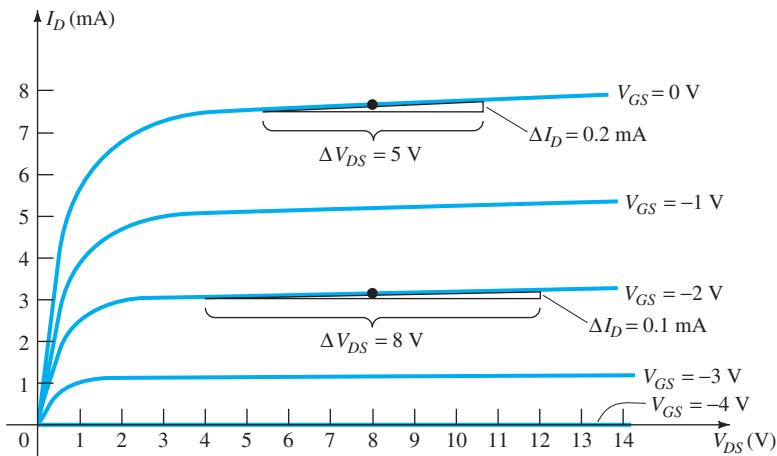
$$r_d = \left. \frac{\Delta V_{DS}}{\Delta I_D} \right|_{V_{GS}=\text{constant}} \quad (8.12)$$

Note the requirement when applying Eq. (8.12) that the voltage  $V_{GS}$  remain constant when  $r_d$  is determined. This is accomplished by drawing a straight line approximating the  $V_{GS}$  line at the point of operation. A  $\Delta V_{DS}$  or  $\Delta I_D$  is then chosen and the other quantity measured off for use in the equation.



**FIG. 8.6**  
Definition of  $r_d$  using JFET drain characteristics.

**EXAMPLE 8.5** Determine the output impedance for the JFET of Fig. 8.7 for  $V_{GS} = 0 \text{ V}$  and  $V_{GS} = -2 \text{ V}$  at  $V_{DS} = 8 \text{ V}$ .



**FIG. 8.7**  
Drain characteristics used to calculate  $r_d$  in Example 8.5.

**Solution:** For  $V_{GS} = 0\text{ V}$ , a tangent line is drawn and  $\Delta V_{DS}$  is chosen as  $5\text{ V}$ , resulting in a  $\Delta I_D$  of  $0.2\text{ mA}$ . Substituting into Eq. (8.12), we find

$$r_d = \left. \frac{\Delta V_{DS}}{\Delta I_D} \right|_{V_{GS}=0\text{ V}} = \frac{5\text{ V}}{0.2\text{ mA}} = 25\text{ k}\Omega$$

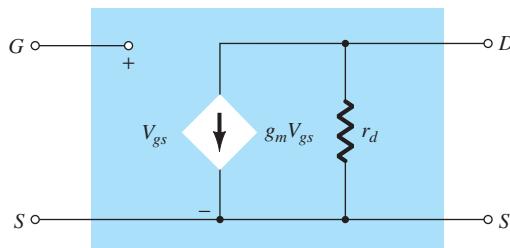
For  $V_{GS} = -2\text{ V}$ , a tangent line is drawn and  $\Delta V_{DS}$  is chosen as  $8\text{ V}$ , resulting in a  $\Delta I_D$  of  $0.1\text{ mA}$ . Substituting into Eq. (8.12), we find

$$r_d = \left. \frac{\Delta V_{DS}}{\Delta I_D} \right|_{V_{GS}=-2\text{ V}} = \frac{8\text{ V}}{0.1\text{ mA}} = 80\text{ k}\Omega$$

which shows that  $r_d$  does change from one operating region to another, with lower values typically occurring at lower levels of  $V_{GS}$  (closer to  $0\text{ V}$ ).

### JFET AC Equivalent Circuit

Now that the important parameters of an ac equivalent circuit have been introduced and discussed, a model for the JFET transistor in the ac domain can be constructed. The control of  $I_d$  by  $V_{gs}$  is included as a current source  $g_m V_{gs}$  connected from drain to source as shown in Fig. 8.8. The current source has its arrow pointing from drain to source to establish a  $180^\circ$  phase shift between output and input voltages as will occur in actual operation.



**FIG. 8.8**  
JFET ac equivalent circuit.

The input impedance is represented by the open circuit at the input terminals and the output impedance by the resistor  $r_d$  from drain to source. Note that the gate-to-source voltage is now represented by  $V_{gs}$  (lowercase subscripts) to distinguish it from dc levels. In addition, note that the source is common to both input and output circuits, whereas the gate and drain terminals are only in “touch” through the controlled current source  $g_m V_{gs}$ .

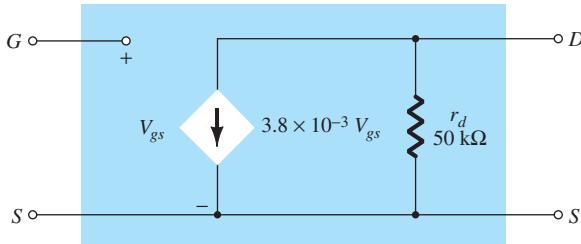
In situations where  $r_d$  is ignored (assumed sufficiently large in relation to other elements of the network to be approximated by an open circuit), the equivalent circuit is simply a current source whose magnitude is controlled by the signal  $V_{gs}$  and parameter  $g_m$ —clearly a voltage-controlled current source.

**EXAMPLE 8.6** Given  $g_{fs} = 3.8 \text{ mS}$  and  $g_{os} = 20 \mu\text{S}$ , sketch the FET ac equivalent model.

**Solution:**

$$g_m = g_{fs} = 3.8 \text{ mS} \quad \text{and} \quad r_d = \frac{1}{g_{os}} = \frac{1}{20 \mu\text{S}} = 50 \text{ k}\Omega$$

resulting in the ac equivalent model of Fig. 8.9.

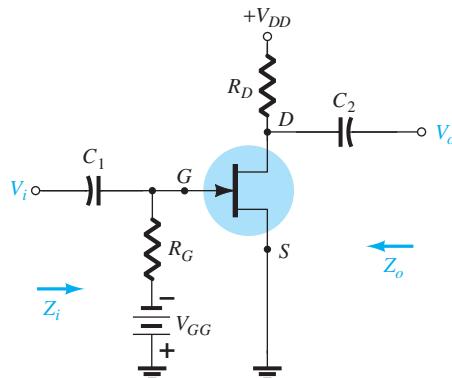


**FIG. 8.9**  
JFET ac equivalent model for Example 8.6.

### 8.3 FIXED-BIAS CONFIGURATION

Now that the JFET equivalent circuit has been defined, a number of fundamental JFET small-signal configurations are investigated. The approach parallels the ac analysis of BJT amplifiers with a determination of the important parameters of  $Z_i$ ,  $Z_o$ , and  $A_v$  for each configuration.

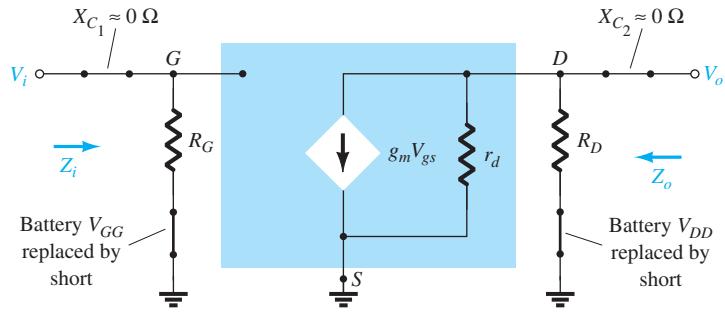
The *fixed-bias* configuration of Fig. 8.10 includes the coupling capacitors  $C_1$  and  $C_2$ , which isolate the dc biasing arrangement from the applied signal and load; they act as short-circuit equivalents for the ac analysis.



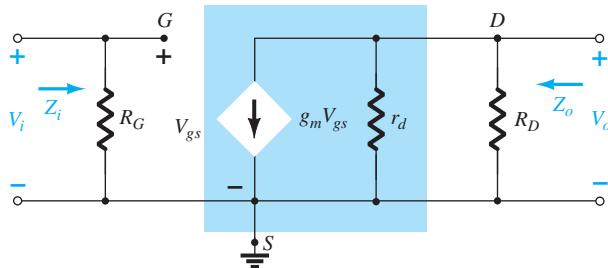
**FIG. 8.10**  
JFET fixed-bias configuration.

Once the levels of  $g_m$  and  $r_d$  are determined from the dc biasing arrangement, specification sheet, or characteristics, the ac equivalent model can be substituted between the appropriate terminals as shown in Fig. 8.11. Note that both capacitors have the short-circuit equivalent because the reactance  $X_C = 1/(2\pi fC)$  is sufficiently small compared to other impedance levels of the network, and the dc batteries  $V_{GG}$  and  $V_{DD}$  are set to 0 V by a short-circuit equivalent.

The network of Fig. 8.11 is then carefully redrawn as shown in Fig. 8.12. Note the defined polarity of  $V_{gs}$ , which defines the direction of  $g_m V_{gs}$ . If  $V_{gs}$  is negative, the direction of the current source reverses. The applied signal is represented by  $V_i$  and the output signal across  $R_D \parallel r_d$  by  $V_o$ .



**FIG. 8.11**  
Substituting the JFET ac equivalent circuit unit into the network of Fig. 8.10.



**FIG. 8.12**  
Redrawn network of Fig. 8.11.

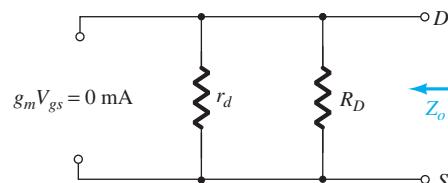
**Z<sub>i</sub>** Figure 8.12 clearly reveals that

$$Z_i = R_G \quad (8.13)$$

because of the infinite input impedance at the input terminals of the JFET.

**Z<sub>o</sub>** Setting  $V_i = 0$  V as required by the definition of  $Z_o$  will establish  $V_{gs}$  as 0 V also. The result is  $g_m V_{gs} = 0$  mA, and the current source can be replaced by an open-circuit equivalent as shown in Fig. 8.13. The output impedance is

$$Z_o = R_D \| r_d \quad (8.14)$$



**FIG. 8.13**  
Determining  $Z_o$ .

If the resistance  $r_d$  is sufficiently large (at least 10:1) compared to  $R_D$ , the approximation  $r_d \| R_D \approx R_D$  can often be applied and

$$Z_o \approx R_D \quad r_d \geq 10R_D \quad (8.15)$$

**A<sub>v</sub>** Solving for  $V_o$  in Fig. 8.12, we find

$$V_o = -g_m V_{gs} (r_d \| R_D)$$

but

$$V_{gs} = V_i$$

and

$$V_o = -g_m V_i (r_d \| R_D)$$

so that

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D) \quad (8.16)$$

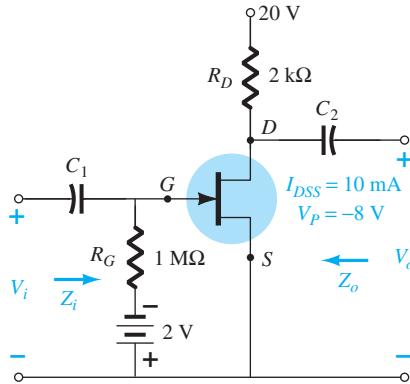
If  $r_d \geq 10R_D$ ,

$$A_v = \frac{V_o}{V_i} = -g_m R_D \quad r_d \geq 10R_D \quad (8.17)$$

**Phase Relationship** The negative sign in the resulting equation for  $A_v$  clearly reveals a phase shift of  $180^\circ$  between input and output voltages.

**EXAMPLE 8.7** The fixed-bias configuration of Example 7.1 had an operating point defined by  $V_{GSQ} = -2\text{ V}$  and  $I_{DQ} = 5.625\text{ mA}$ , with  $I_{DSS} = 10\text{ mA}$  and  $V_P = -8\text{ V}$ . The network is redrawn as Fig. 8.14 with an applied signal  $V_i$ . The value of  $y_{os}$  is provided as  $40\text{ }\mu\text{S}$ .

- Determine  $g_m$ .
- Find  $r_d$ .
- Determine  $Z_i$ .
- Calculate  $Z_o$ .
- Determine the voltage gain  $A_v$ .
- Determine  $A_v$  ignoring the effects of  $r_d$ .



**FIG. 8.14**  
JFET configuration for Example 8.7.

**Solution:**

$$\text{a. } g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10\text{ mA})}{8\text{ V}} = 2.5\text{ mS}$$

$$g_m = g_{m0} \left(1 - \frac{V_{GSQ}}{V_P}\right) = 2.5\text{ mS} \left(1 - \frac{(-2\text{ V})}{(-8\text{ V})}\right) = 1.88\text{ mS}$$

$$\text{b. } r_d = \frac{1}{y_{os}} = \frac{1}{40\text{ }\mu\text{S}} = 25\text{ k}\Omega$$

$$\text{c. } Z_i = R_G = 1\text{ M}\Omega$$

$$\text{d. } Z_o = R_D \| r_d = 2\text{ k}\Omega \| 25\text{ k}\Omega = 1.85\text{ k}\Omega$$

$$\begin{aligned} \text{e. } A_v &= -g_m(R_D \| r_d) = -(1.88\text{ mS})(1.85\text{ k}\Omega) \\ &= -3.48 \end{aligned}$$

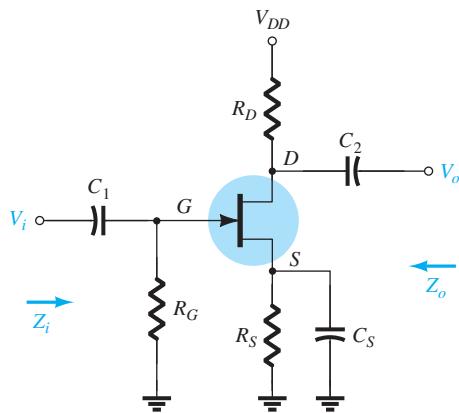
$$\text{f. } A_v = -g_m R_D = -(1.88\text{ mS})(2\text{ k}\Omega) = -3.76$$

As demonstrated in part (f), a ratio of  $25\text{ k}\Omega : 2\text{ k}\Omega = 12.5:1$  between  $r_d$  and  $R_D$  results in a difference of 8% in the solution.

## 8.4 SELF-BIAS CONFIGURATION

### Bypassed $R_S$

The fixed-bias configuration has the distinct disadvantage of requiring two dc voltage sources. The *self-bias* configuration of Fig. 8.15 requires only one dc supply to establish the desired operating point.

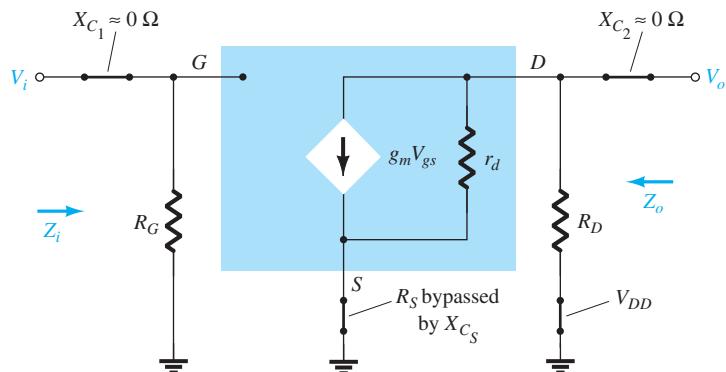


**FIG. 8.15**  
Self-bias JFET configuration.

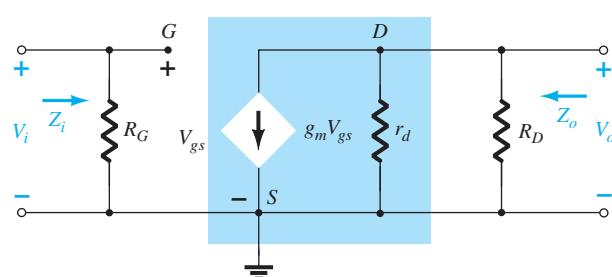
The capacitor  $C_S$  across the source resistance assumes its open-circuit equivalence for dc, allowing  $R_S$  to define the operating point. Under ac conditions, the capacitor assumes the short-circuit state and “short circuits” the effects of  $R_S$ . If left in the ac, gain will be reduced, as will be shown in the paragraphs to follow.

The JFET equivalent circuit is established in Fig. 8.16 and carefully redrawn in Fig. 8.17.

Since the resulting configuration is the same as appearing in Fig. 8.12, the resulting equations for  $Z_i$ ,  $Z_o$ , and  $A_v$  will be the same.



**FIG. 8.16**  
Network of Fig. 8.15 following the substitution of  
the JFET ac equivalent circuit.



**FIG. 8.17**  
Redrawn network of Fig. 8.16.

**Z<sub>i</sub>**

$$Z_i = R_G$$

(8.18)

**Z<sub>o</sub>**

$$Z_o = r_d \| R_D$$

(8.19)

If  $r_d \geq 10R_D$ ,

$$Z_o \cong R_D \quad |_{r_d \geq 10R_D}$$

(8.20)

**A<sub>v</sub>**

$$A_v = -g_m(r_d \| R_D)$$

(8.21)

If  $r_d \geq 10R_D$ ,

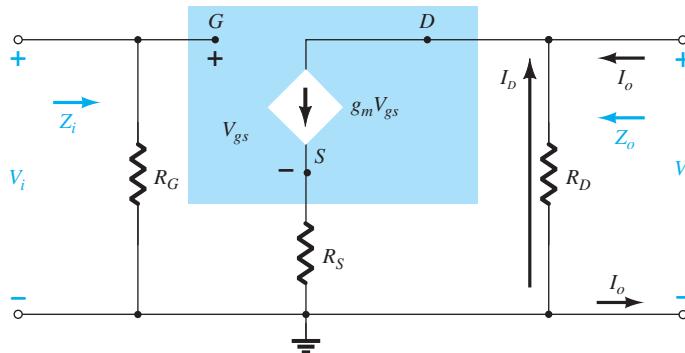
$$A_v = -g_m R_D \quad |_{r_d \geq 10R_D}$$

(8.22)

**Phase Relationship** The negative sign in the solutions for  $A_v$  again indicates a phase shift of  $180^\circ$  between  $V_i$  and  $V_o$ .

### Unbypassed $R_S$

If  $C_S$  is removed from Fig. 8.15, the resistor  $R_S$  will be part of the ac equivalent circuit as shown in Fig. 8.18. In this case, there is no obvious way to reduce the network to lower its level of complexity. In determining the levels of  $Z_i$ ,  $Z_o$ , and  $A_v$ , one must be very careful with notation and defined polarities and direction. Initially, the resistance  $r_d$  will be left out of the analysis to form a basis for comparison.



**FIG. 8.18**  
Self-bias JFET configuration including the effects of  $R_S$  with  
 $r_d = \infty\Omega$ .

**Z<sub>i</sub>** Due to the open-circuit condition between the gate and the output network, the input remains the following:

$$Z_i = R_G$$

(8.23)

**Z<sub>o</sub>** The output impedance is defined by

$$Z_o = \left. \frac{V_o}{I_o} \right|_{V_i=0}$$

Setting  $V_i = 0$  V in Fig. 8.18 results in the gate terminal being at ground potential (0 V). The voltage across  $R_G$  is then 0 V, and  $R_G$  has been effectively “shorted out” of the picture.

Applying Kirchhoff's current law results in

$$I_o + I_D = g_m V_{gs}$$

with

$$V_{gs} = -(I_o + I_D) R_S$$

so that

$$I_o + I_D = -g_m(I_o + I_D)R_S = -g_mI_oR_S - g_mI_DR_S$$

or

$$I_o[1 + g_mR_S] = -I_D[1 + g_mR_S]$$

and

$I_o = -I_D$  (the controlled current source  $g_mV_{gs} = 0$  A  
for the applied conditions)

Since

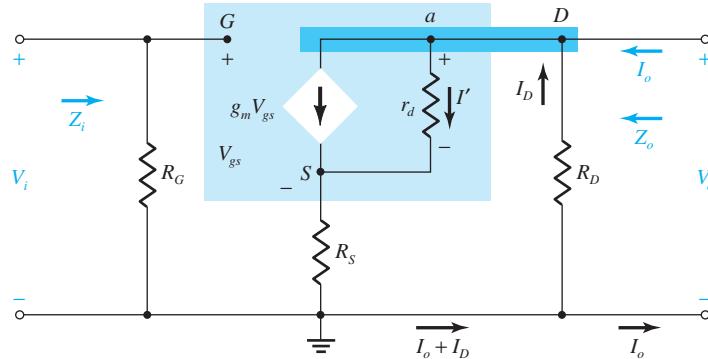
$$V_o = -I_DR_D$$

then

$$V_o = -(-I_o)R_D = I_oR_D$$

and

$$Z_o = \frac{V_o}{I_o} = R_D \quad r_d = \infty \Omega \quad (8.24)$$

If  $r_d$  is included in the network, the equivalent will appear as shown in Fig. 8.19.

**FIG. 8.19**  
Including the effects of  $r_d$  in the self-bias JFET configuration.

Since

$$Z_o = \left. \frac{V_o}{I_o} \right|_{V_i=0 \text{ V}} = -\frac{I_DR_D}{I_o}$$

we should try to find an expression for  $I_o$  in terms of  $I_D$ .

Applying Kirchhoff's current law, we have

$$I_o = g_mV_{gs} + I_{r_d} - I_D$$

but

$$V_{r_d} = V_o + V_{gs}$$

and

$$I_o = g_mV_{gs} + \frac{V_o + V_{gs}}{r_d} - I_D$$

or

$$I_o = \left( g_m + \frac{1}{r_d} \right) V_{gs} - \frac{I_DR_D}{r_d} - I_D \text{ using } V_o = -I_DR_D$$

Now,

$$V_{gs} = -(I_D + I_o)R_S$$

so that

$$I_o = -\left( g_m + \frac{1}{r_d} \right) (I_D + I_o)R_S - \frac{I_DR_D}{r_d} - I_D$$

with the result that

$$I_o \left[ 1 + g_mR_S + \frac{R_S}{r_d} \right] = -I_D \left[ 1 + g_mR_S + \frac{R_S}{r_d} + \frac{R_D}{r_d} \right]$$

or

$$I_o = \frac{-I_D \left[ 1 + g_mR_S + \frac{R_S}{r_d} + \frac{R_D}{r_d} \right]}{1 + g_mR_S + \frac{R_S}{r_d}}$$

and

$$Z_o = \frac{V_o}{I_o} = \frac{-I_DR_D}{-I_D \left( 1 + g_mR_S + \frac{R_S}{r_d} + \frac{R_D}{r_d} \right)} = \frac{R_S}{1 + g_mR_S + \frac{R_S}{r_d}}$$

and finally,

$$Z_o = \frac{\left[ 1 + g_m R_S + \frac{R_S}{r_d} \right]}{\left[ 1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d} \right]} R_D \quad (8.25a)$$

For  $r_d \geq 10R_D$ ,

$$\left( 1 + g_m R_S + \frac{R_S}{r_d} \right) \gg \frac{R_D}{r_d}$$

and  $1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d} \cong 1 + g_m R_S + \frac{R_S}{r_d}$

resulting in

$$Z_o \cong R_D \quad r_d \geq 10R_D \quad (8.25b)$$

**A<sub>v</sub>** For the network of Fig. 8.19, application of Kirchhoff's voltage law to the input circuit results in

$$V_i - V_{gs} - V_{R_S} = 0$$

$$V_{gs} = V_i - I_D R_S$$

The voltage across  $r_d$  using Kirchhoff's voltage law is

$$V_{r_d} = V_o - V_{R_S}$$

and

$$I' = \frac{V_{r_d}}{r_d} = \frac{V_o - V_{R_S}}{r_d}$$

so that application of Kirchhoff's current law results in

$$I_D = g_m V_{gs} + \frac{V_o - V_{R_S}}{r_d}$$

Substituting for  $V_{gs}$  from above and substituting for  $V_o$  and  $V_{R_S}$ , we have

$$I_D = g_m [V_i - I_D R_S] + \frac{(-I_D R_D) - (I_D R_S)}{r_d}$$

so that

$$I_D \left[ 1 + g_m R_S + \frac{R_D + R_S}{r_d} \right] = g_m V_i$$

or

$$I_D = \frac{g_m V_i}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$$

The output voltage is then

$$V_o = -I_D R_D = -\frac{g_m R_D V_i}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$$

and

$$A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}} \quad (8.26)$$

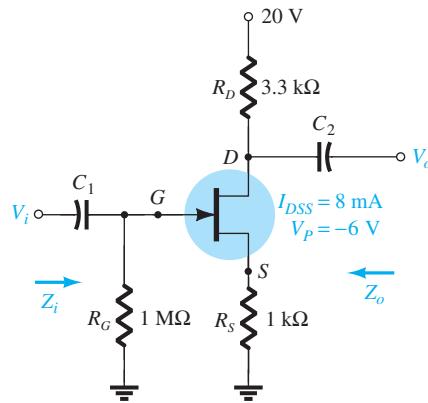
Again, if  $r_d \geq 10(R_D + R_S)$ ,

$$A_v = \frac{V_o}{V_i} \cong -\frac{g_m R_D}{1 + g_m R_S} \quad r_d \geq 10(R_D + R_S) \quad (8.27)$$

**Phase Relationship** The negative sign in Eq. (8.26) again reveals that a  $180^\circ$  phase shift will exist between  $V_i$  and  $V_o$ .

**EXAMPLE 8.8** The self-bias configuration of Example 7.2 has an operating point defined by  $V_{GSQ} = -2.6$  V and  $I_{DQ} = 2.6$  mA, with  $I_{DSS} = 8$  mA and  $V_P = -6$  V. The network is redrawn as Fig. 8.20 with an applied signal  $V_i$ . The value of  $g_{os}$  is given as  $20 \mu\text{S}$ .

- Determine  $g_m$ .
- Find  $r_d$ .
- Find  $Z_i$ .
- Calculate  $Z_o$  with and without the effects of  $r_d$ . Compare the results.
- Calculate  $A_v$  with and without the effects of  $r_d$ . Compare the results.



**FIG. 8.20**  
Network for Example 8.8.

**Solution:**

$$\text{a. } g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(8 \text{ mA})}{6 \text{ V}} = 2.67 \text{ mS}$$

$$g_m = g_{m0} \left( 1 - \frac{V_{GSQ}}{V_P} \right) = 2.67 \text{ mS} \left( 1 - \frac{(-2.6 \text{ V})}{(-6 \text{ V})} \right) = 1.51 \text{ mS}$$

$$\text{b. } r_d = \frac{1}{y_{os}} = \frac{1}{20 \mu\text{S}} = 50 \text{ k}\Omega$$

$$\text{c. } Z_i = R_G = 1 \text{ M}\Omega$$

$$\text{d. With } r_d,$$

$$r_d = 50 \text{ k}\Omega > 10R_D = 33 \text{ k}\Omega$$

Therefore,

$$Z_o = R_D = 3.3 \text{ k}\Omega$$

If  $r_d = \infty \Omega$ ,

$$Z_o = R_D = 3.3 \text{ k}\Omega$$

$$\text{e. With } r_d,$$

$$\begin{aligned} A_v &= \frac{-g_m R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}} = \frac{-(1.51 \text{ mS})(3.3 \text{ k}\Omega)}{1 + (1.51 \text{ mS})(1 \text{ k}\Omega) + \frac{3.3 \text{ k}\Omega + 1 \text{ k}\Omega}{50 \text{ k}\Omega}} \\ &= -1.92 \end{aligned}$$

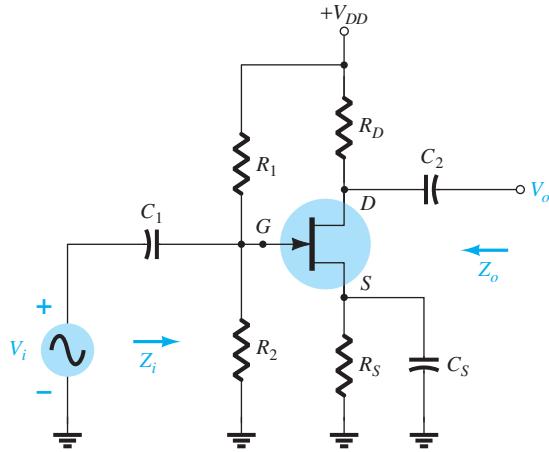
With  $r_d = \infty \Omega$  (open-circuit equivalence),

$$A_v = \frac{-g_m R_D}{1 + g_m R_S} = \frac{-(1.51 \text{ mS})(3.3 \text{ k}\Omega)}{1 + (1.51 \text{ mS})(1 \text{ k}\Omega)} = -1.98$$

As above, the effect of  $r_d$  is minimal because the condition  $r_d \geq 10(R_D + R_S)$  is satisfied.

Note also that the typical gain of a JFET amplifier is less than that generally encountered for BJTs of similar configurations. Keep in mind, however, that  $Z_i$  is magnitudes greater than the typical  $Z_i$  of a BJT, which will have a very positive effect on the overall gain of a system.

The popular voltage-divider configuration for BJTs can also be applied to JFETs as demonstrated in Fig. 8.21.



**FIG. 8.21**

JFET voltage-divider configuration.

Substituting the ac equivalent model for the JFET results in the configuration of Fig. 8.22. Replacing the dc supply  $V_{DD}$  by a short-circuit equivalent has grounded one end of  $R_1$  and  $R_D$ . Since each network has a common ground,  $R_1$  can be brought down in parallel with  $R_2$  as shown in Fig. 8.23.  $R_D$  can also be brought down to ground, but in the output circuit across  $r_d$ . The resulting ac equivalent network now has the basic format of some of the networks already analyzed.

**Z<sub>i</sub>**  $R_1$  and  $R_2$  are in parallel with the open-circuit equivalence of the JFET, resulting in

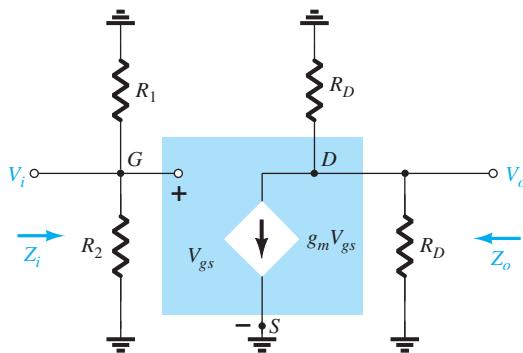
$$Z_i = R_1 \parallel R_2 \quad (8.28)$$

**Z<sub>o</sub>** Setting  $V_i = 0$  sets  $V_{gs}$  and  $g_m V_{gs}$  to zero, and

$$Z_o = r_d \parallel R_D \quad (8.29)$$

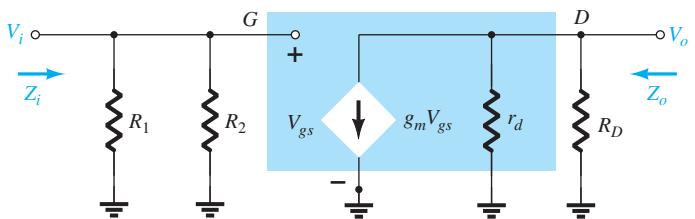
For  $r_d \geq 10R_D$ ,

$$Z_o \cong R_D \quad |_{r_d \geq 10R_D} \quad (8.30)$$



**FIG. 8.22**

Network of Fig. 8.21 under ac conditions.



**FIG. 8.23**

Redrawn network of Fig. 8.22.

**A<sub>v</sub>**

$$V_{gs} = V_i$$

and

$$V_o = -g_m V_{gs} (r_d \| R_D)$$

so that

$$A_v = \frac{V_o}{V_i} = \frac{-g_m V_{gs} (r_d \| R_D)}{V_{gs}}$$

and

$$A_v = \frac{V_o}{V_i} = -g_m (r_d \| R_D) \quad (8.31)$$

If  $r_d \geq 10R_D$ ,

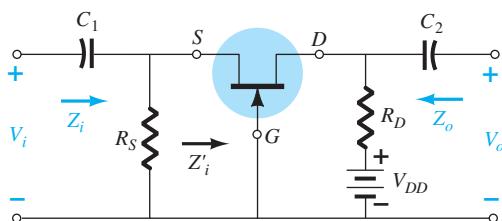
$$A_v = \frac{V_o}{V_i} \cong -g_m R_D \quad r_d \geq 10R_D \quad (8.32)$$

Note that the equations for  $Z_o$  and  $A_v$  are the same as obtained for the fixed-bias and self-bias (with bypassed  $R_S$ ) configurations. The only difference is the equation for  $Z_i$ , which is now sensitive to the parallel combination of  $R_1$  and  $R_2$ .

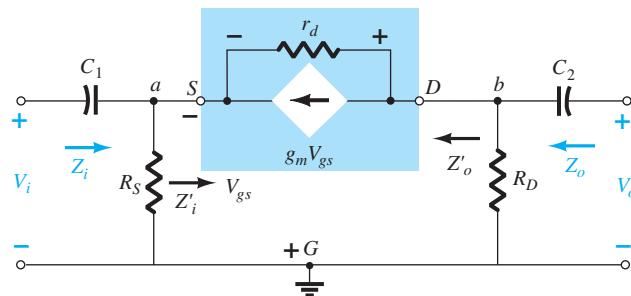
## 8.6 COMMON-GATE CONFIGURATION

The last JFET configuration to be analyzed in detail is the common-gate configuration of Fig. 8.24, which parallels the common-base configuration employed with BJT transistors.

Substituting the JFET equivalent circuit results in Fig. 8.25. Note the continuing requirement that the controlled source  $g_m V_{gs}$  be connected from drain to source with  $r_d$  in parallel. The isolation between input and output circuits has obviously been lost since the gate terminal is now connected to the common ground of the network and the controlled current source is connected directly from drain to source. In addition, the resistor connected between input terminals is no longer  $R_G$ , but the resistor  $R_S$  connected from source to ground. Note also the location of the controlling voltage  $V_{gs}$  and the fact that it appears directly across the resistor  $R_S$ .



**FIG. 8.24**  
JFET common-gate configuration.



**FIG. 8.25**  
Network of Fig. 8.24 following substitution of JFET ac equivalent model.

**Z<sub>i</sub>** The resistor  $R_S$  is directly across the terminals defining  $Z_i$ . Let us therefore find the impedance  $Z'_i$  of Fig. 8.24, which will simply be in parallel with  $R_S$  when  $Z_i$  is defined.

The network of interest is redrawn as Fig. 8.26. The voltage  $V' = -V_{gs}$ . Applying Kirchhoff's voltage law around the output perimeter of the network results in

$$V' - V_{r_d} - V_{R_D} = 0$$

and

$$V_{r_d} = V' - V_{R_D} = V' - I' R_D$$

Applying Kirchhoff's current law at node  $a$  results in

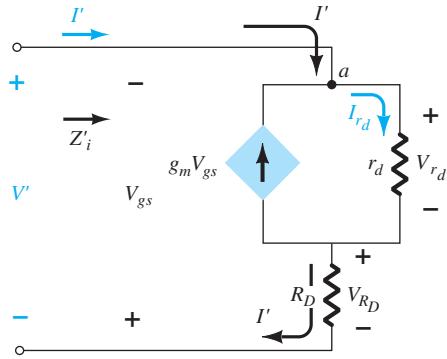
$$I' + g_m V_{gs} = I_{r_d}$$

and

$$I' = I_{r_d} - g_m V_{gs} = \frac{(V' - I' R_D)}{r_d} - g_m V_{gs}$$

or

$$I' = \frac{V'}{r_d} - \frac{I' R_D}{r_d} - g_m [-V']$$



**FIG. 8.26**  
Determining  $Z'_i$  for the network of Fig. 8.24.

so that

$$I' \left[ 1 + \frac{R_D}{r_d} \right] = V' \left[ \frac{1}{r_d} + g_m \right]$$

and

$$Z'_i = \frac{V'}{I'} = \frac{\left[ 1 + \frac{R_D}{r_d} \right]}{\left[ g_m + \frac{1}{r_d} \right]} \quad (8.33)$$

or

$$Z'_i = \frac{V'}{I'} = \frac{r_d + R_D}{1 + g_m r_d}$$

and

$$Z_i = R_S \| Z'_i$$

which results in

$$Z_i = R_S \| \left[ \frac{r_d + R_D}{1 + g_m r_d} \right] \quad (8.34)$$

If  $r_d \geq 10R_D$ , Eq. (8.33) permits the following approximation since  $R_D/r_d \ll 1$  and  $1/r_d \ll g_m$ :

$$Z'_i = \frac{\left[ 1 + \frac{R_D}{r_d} \right]}{\left[ g_m + \frac{1}{r_d} \right]} \cong \frac{1}{g_m}$$

and

$$Z_i \cong R_S \| 1/g_m \quad r_d \geq 10R_D \quad (8.35)$$

**Z<sub>o</sub>** Substituting  $V_i = 0$  V in Fig. 8.25 will “short-out” the effects of  $R_S$  and set  $V_{gs}$  to 0 V. The result is  $g_m V_{gs} = 0$ , and  $r_d$  will be in parallel with  $R_D$ . Therefore,

$$Z_o = R_D \| r_d \quad (8.36)$$

For  $r_d \geq 10R_D$ ,

$$Z_o \cong R_D \quad r_d \geq 10R_D \quad (8.37)$$

**A<sub>v</sub>** Figure 8.25 reveals that

$$V_i = -V_{gs}$$

and

$$V_o = I_D R_D$$

The voltage across  $r_d$  is

$$V_{rd} = V_o - V_i$$

and

$$I_{r_d} = \frac{V_o - V_i}{r_d}$$

Applying Kirchhoff's current law at node  $b$  in Fig. 8.25 results in

$$I_{r_d} + I_D + g_m V_{gs} = 0$$

and

$$\begin{aligned} I_D &= -I_{r_d} - g_m V_{gs} \\ &= -\left[\frac{V_o - V_i}{r_d}\right] - g_m[-V_i] \\ I_D &= \frac{V_i - V_o}{r_d} + g_m V_i \end{aligned}$$

so that

$$\begin{aligned} V_o &= I_D R_D = \left[\frac{V_i - V_o}{r_d} + g_m V_i\right] R_D \\ &= \frac{V_i R_D}{r_d} - \frac{V_o R_D}{r_d} + g_m \\ \text{and } &V_o \left[1 + \frac{R_D}{r_d}\right] = V_i \left[\frac{R_D}{r_d} + g_m R_D\right] \end{aligned}$$

with

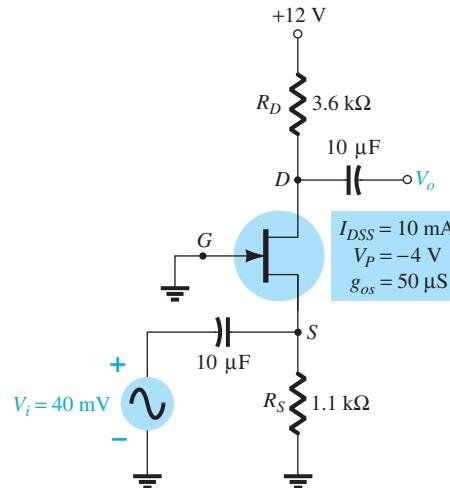
$$A_v = \frac{V_o}{V_i} = \frac{\left[g_m R_D + \frac{R_D}{r_d}\right]}{\left[1 + \frac{R_D}{r_d}\right]} \quad (8.38)$$

For  $r_d \geq 10R_D$ , the factor  $R_D/r_d$  of Eq. (8.38) can be dropped as a good approximation, and

$$A_v \cong g_m R_D \quad r_d \geq 10R_D \quad (8.39)$$

**Phase Relationship** The fact that  $A_v$  is a positive number will result in an *in-phase* relationship between  $V_o$  and  $V_i$  for the common-gate configuration.**EXAMPLE 8.9** Although the network of Fig. 8.27 may not initially appear to be of the common-gate variety, a close examination will reveal that it has all the characteristics of Fig. 8.24. If  $V_{GSQ} = -2.2$  V and  $I_{DQ} = 2.03$  mA:

- Determine  $g_m$ .
- Find  $r_d$ .
- Calculate  $Z_i$  with and without  $r_d$ . Compare results.
- Find  $Z_o$  with and without  $r_d$ . Compare results.
- Determine  $V_o$  with and without  $r_d$ . Compare results.



**FIG. 8.27**  
Network for Example 8.9.

**Solution:**

a.  $g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10 \text{ mA})}{4 \text{ V}} = 5 \text{ mS}$

$$g_m = g_{m0} \left(1 - \frac{V_{GSQ}}{V_P}\right) = 5 \text{ mS} \left(1 - \frac{(-2.2 \text{ V})}{(-4 \text{ V})}\right) = 2.25 \text{ mS}$$

b.  $r_d = \frac{1}{g_{os}} = \frac{1}{50 \mu\text{S}} = 20 \text{ k}\Omega$

c. With  $r_d$ ,

$$\begin{aligned} Z_i &= R_S \parallel \left[ \frac{r_d + R_D}{1 + g_m r_d} \right] = 1.1 \text{ k}\Omega \parallel \left[ \frac{20 \text{ k}\Omega + 3.6 \text{ k}\Omega}{1 + (2.25 \text{ mS})(20 \text{ k}\Omega)} \right] \\ &= 1.1 \text{ k}\Omega \parallel 0.51 \text{ k}\Omega = 0.35 \text{ k}\Omega \end{aligned}$$

Without  $r_d$ ,

$$\begin{aligned} Z_i &= R_S \parallel 1/g_m = 1.1 \text{ k}\Omega \parallel 1/2.25 \text{ ms} = 1.1 \text{ k}\Omega \parallel 0.44 \text{ k}\Omega \\ &= 0.31 \text{ k}\Omega \end{aligned}$$

Even though the condition  $r_d \geq 10R_D$  is not satisfied with  $r_d = 20 \text{ k}\Omega$  and  $10R_D = 36 \text{ k}\Omega$ , both equations result in essentially the same level of impedance. In this case,  $1/g_m$  was the predominant factor.

d. With  $r_d$ ,

$$Z_o = R_D \parallel r_d = 3.6 \text{ k}\Omega \parallel 20 \text{ k}\Omega = 3.05 \text{ k}\Omega$$

Without  $r_d$ ,

$$Z_o = R_D = 3.6 \text{ k}\Omega$$

Again the condition  $r_d \geq 10R_D$  is not satisfied, but both results are reasonably close.  $R_D$  is certainly the predominant factor in this example.

e. With  $r_d$ ,

$$\begin{aligned} A_v &= \frac{\left[ g_m R_D + \frac{R_D}{r_d} \right]}{\left[ 1 + \frac{R_D}{r_d} \right]} = \frac{\left[ (2.25 \text{ mS})(3.6 \text{ k}\Omega) + \frac{3.6 \text{ k}\Omega}{20 \text{ k}\Omega} \right]}{\left[ 1 + \frac{3.6 \text{ k}\Omega}{20 \text{ k}\Omega} \right]} \\ &= \frac{8.1 + 0.18}{1 + 0.18} = 7.02 \end{aligned}$$

and  $A_v = \frac{V_o}{V_i} \Rightarrow V_o = A_v V_i = (7.02)(40 \text{ mV}) = 280.8 \text{ mV}$

Without  $r_d$ ,

$$A_v = g_m R_D = (2.25 \text{ mS})(3.6 \text{ k}\Omega) = 8.1$$

with  $V_o = A_v V_i = (8.1)(40 \text{ mV}) = 324 \text{ mV}$

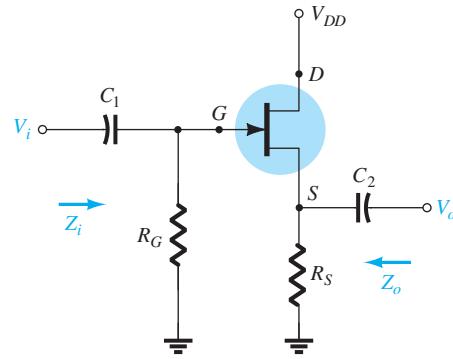
In this case, the difference is a little more noticeable, but not dramatically so.

Example 8.9 demonstrates that even though the condition  $r_d \geq 10R_D$  was not satisfied, the results for the parameters given were not significantly different using the exact and approximate equations. In fact, in most cases, the approximate equations can be used to find a reasonable idea of particular levels with a reduced amount of effort.

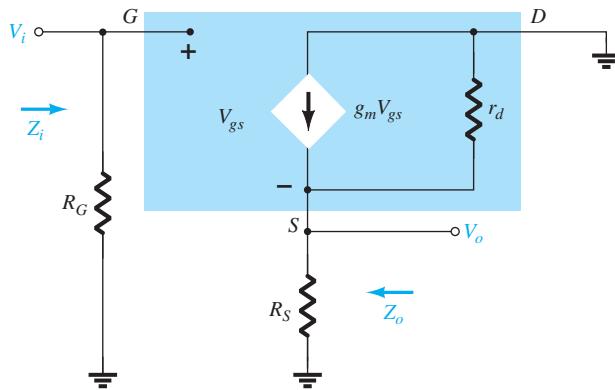
## 8.7 SOURCE-FOLLOWER (COMMON-DRAIN) CONFIGURATION

The JFET equivalent of the BJT emitter-follower configuration is the source-follower configuration of Fig. 8.28. Note that the output is taken off the source terminal and, when the dc supply is replaced by its short-circuit equivalent, the drain is grounded (hence, the terminology *common-drain*).

Substituting the JFET equivalent circuit results in the configuration of Fig. 8.29. The controlled source and the internal output impedance of the JFET are tied to ground at one end and  $R_S$  on the other, with  $V_o$  across  $R_S$ . Since  $g_m V_{gs}$ ,  $r_d$ , and  $R_S$  are connected to

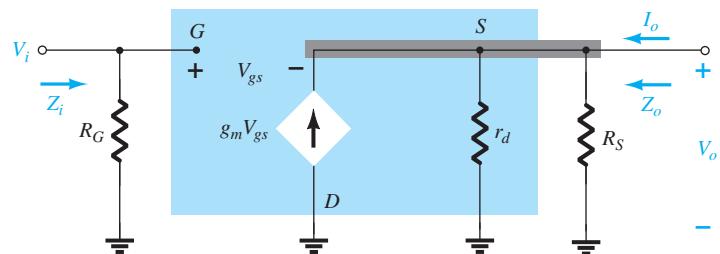


**FIG. 8.28**  
JFET source-follower configuration.



**FIG. 8.29**  
Network of Fig. 8.28 following the substitution of the JFET ac equivalent model.

the same terminal and ground, they can all be placed in parallel as shown in Fig. 8.30. The current source reversed direction, but  $V_{gs}$  is still defined between the gate and source terminals.



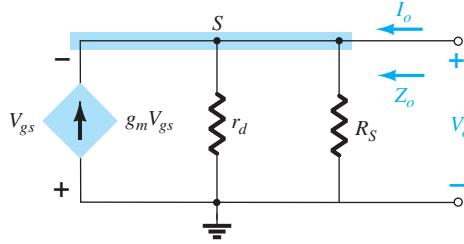
**FIG. 8.30**  
Network of Fig. 8.29 redrawn.

**Z<sub>i</sub>** Figure 8.30 clearly reveals that  $Z_i$  is defined by

$$Z_i = R_G \quad (8.40)$$

**Z<sub>o</sub>** Setting  $V_i = 0$  V results in the gate terminal being connected directly to the ground as shown in Fig. 8.31.

The fact that  $V_{gs}$  and  $V_o$  are across the same parallel network results in  $V_o = -V_{gs}$ .



**FIG. 8.31**  
*Determining  $Z_o$  for the network of Fig. 8.30.*

Applying Kirchhoff's current law at node  $S$ , we obtain

$$\begin{aligned} I_o + g_m V_{gs} &= I_{r_d} + I_{R_s} \\ &= \frac{V_o}{r_d} + \frac{V_o}{R_s} \end{aligned}$$

The result is

$$\begin{aligned} I_o &= V_o \left[ \frac{1}{r_d} + \frac{1}{R_s} \right] - g_m V_{gs} \\ &= V_o \left[ \frac{1}{r_d} + \frac{1}{R_s} \right] - g_m [-V_o] \\ &= V_o \left[ \frac{1}{r_d} + \frac{1}{R_s} + g_m \right] \end{aligned}$$

and  $Z_o = \frac{V_o}{I_o} = \frac{V_o}{V_o \left[ \frac{1}{r_d} + \frac{1}{R_s} + g_m \right]} = \frac{1}{\frac{1}{r_d} + \frac{1}{R_s} + g_m} = \frac{1}{\frac{1}{r_d} + \frac{1}{R_s} + \frac{1}{g_m}}$

which has the same format as the total resistance of three parallel resistors. Therefore,

$$Z_o = r_d \| R_s \| 1/g_m \quad (8.41)$$

For  $r_d \geq 10 R_s$ ,

$$Z_o \approx R_s \| 1/g_m \quad r_d \geq 10 R_s \quad (8.42)$$

**A<sub>v</sub>** The output voltage  $V_o$  is determined by

$$V_o = g_m V_{gs} (r_d \| R_s)$$

and applying Kirchhoff's voltage law around the perimeter of the network of Fig. 8.30 results in

$$V_i = V_{gs} + V_o$$

and

$$V_{gs} = V_i - V_o$$

so that

$$V_o = g_m (V_i - V_o) (r_d \| R_s)$$

or

$$V_o = g_m V_i (r_d \| R_s) - g_m V_o (r_d \| R_s)$$

and

$$V_o [1 + g_m (r_d \| R_s)] = g_m V_i (r_d \| R_s)$$

so that

$$A_v = \frac{V_o}{V_i} = \frac{g_m (r_d \| R_s)}{1 + g_m (r_d \| R_s)} \quad (8.43)$$

In the absence of  $r_d$  or if  $r_d \geq 10 R_s$ ,

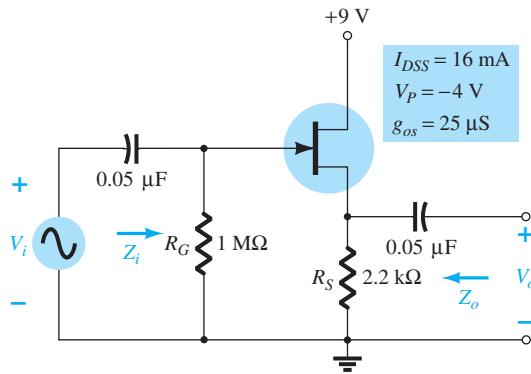
$$A_v = \frac{V_o}{V_i} \cong \frac{g_m R_s}{1 + g_m R_s} \quad r_d \geq 10 R_s \quad (8.44)$$

Since the denominator of Eq. (8.43) is larger than the numerator by a factor of one, the gain can never be equal to or greater than one (as encountered for the emitter-follower BJT network).

**Phase Relationship** Since  $A_v$  of Eq. (8.43) is a positive quantity,  $V_o$  and  $V_i$  are in phase for the JFET source-follower configuration.

**EXAMPLE 8.10** A dc analysis of the source-follower network of Fig. 8.32 results in  $V_{GSQ} = -2.86$  V and  $I_{DQ} = 4.56$  mA.

- Determine  $g_m$ .
- Find  $r_d$ .
- Determine  $Z_i$ .
- Calculate  $Z_o$  with and without  $r_d$ . Compare results.
- Determine  $A_v$  with and without  $r_d$ . Compare results.



**FIG. 8.32**  
Network to be analyzed in Example 8.10.

**Solution:**

$$\text{a. } g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(16 \text{ mA})}{4 \text{ V}} = 8 \text{ mS}$$

$$g_m = g_{m0} \left( 1 - \frac{V_{GSQ}}{V_P} \right) = 8 \text{ mS} \left( 1 - \frac{(-2.86 \text{ V})}{(-4 \text{ V})} \right) = 2.28 \text{ mS}$$

$$\text{b. } r_d = \frac{1}{g_{os}} = \frac{1}{25 \mu\text{S}} = 40 \text{ k}\Omega$$

$$\text{c. } Z_i = R_G = 1 \text{ M}\Omega$$

d. With  $r_d$ ,

$$\begin{aligned} Z_o &= r_d \| R_S \| 1/g_m = 40 \text{ k}\Omega \| 2.2 \text{ k}\Omega \| 1/2.28 \text{ mS} \\ &= 40 \text{ k}\Omega \| 2.2 \text{ k}\Omega \| 438.6 \Omega \\ &= 362.52 \Omega \end{aligned}$$

which shows that  $Z_o$  is often relatively small and determined primarily by  $1/g_m$ . Without  $r_d$ ,

$$Z_o = R_S \| 1/g_m = 2.2 \text{ k}\Omega \| 438.6 \Omega = 365.69 \Omega$$

which shows that  $r_d$  typically has little effect on  $Z_o$ .

e. With  $r_d$ ,

$$\begin{aligned} A_v &= \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)} = \frac{(2.28 \text{ mS})(40 \text{ k}\Omega \| 2.2 \text{ k}\Omega)}{1 + (2.28 \text{ mS})(40 \text{ k}\Omega \| 2.2 \text{ k}\Omega)} \\ &= \frac{(2.28 \text{ mS})(2.09 \text{ k}\Omega)}{1 + (2.28 \text{ mS})(2.09 \text{ k}\Omega)} = \frac{4.77}{1 + 4.77} = 0.83 \end{aligned}$$

which is less than 1, as predicted above.

Without  $r_d$ ,

$$A_v = \frac{g_m R_S}{1 + g_m R_S} = \frac{(2.28 \text{ mS})(2.2 \text{ k}\Omega)}{1 + (2.28 \text{ mS})(2.2 \text{ k}\Omega)}$$

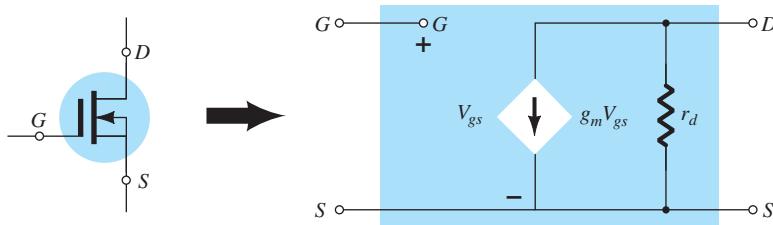
$$= \frac{5.02}{1 + 5.02} = \mathbf{0.83}$$

which shows that  $r_d$  usually has little effect on the gain of the configuration.

## 8.8 DEPLETION-TYPE MOSFETS

The fact that Shockley's equation is also applicable to depletion-type MOSFETs (D-MOSFETs) results in the same equation for  $g_m$ . In fact, the ac equivalent model for D-MOSFETs shown in Fig. 8.33 is exactly the same as that employed for JFETs, as shown in Fig. 8.8.

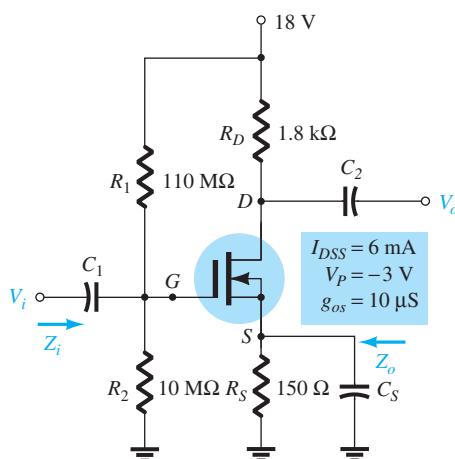
The only difference offered by D-MOSFETs is that  $V_{GSQ}$  can be positive for *n*-channel devices and negative for *p*-channel units. The result is that  $g_m$  can be greater than  $g_{m0}$ , as demonstrated by the example to follow. The range of  $r_d$  is very similar to that encountered for JFETs.



**FIG. 8.33**  
D-MOSFET ac equivalent model.

**EXAMPLE 8.11** The network of Fig. 8.34 was analyzed as Example 7.7, resulting in  $V_{GSQ} = 0.35 \text{ V}$  and  $I_{DQ} = 7.6 \text{ mA}$ .

- Determine  $g_m$  and compare to  $g_{m0}$ .
- Find  $r_d$ .
- Sketch the ac equivalent network for Fig. 8.34.
- Find  $Z_i$ .
- Calculate  $Z_o$ .
- Find  $A_v$ .



**FIG. 8.34**  
Network for Example 8.11.

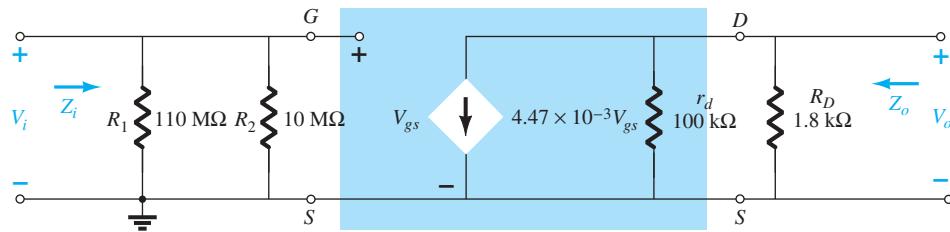
**Solution:**

$$\text{a. } g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(6 \text{ mA})}{3 \text{ V}} = 4 \text{ mS}$$

$$g_m = g_{m0} \left( 1 - \frac{V_{GS0}}{V_P} \right) = 4 \text{ mS} \left( 1 - \frac{(0.35 \text{ V})}{(-3 \text{ V})} \right) = 4 \text{ mS}(1 + 0.117) = 4.47 \text{ mS}$$

$$\text{b. } r_d = \frac{1}{y_{os}} = \frac{1}{10 \mu\text{S}} = 100 \text{ k}\Omega$$

c. See Fig. 8.35. Note the similarities with the network of Fig. 8.23. Equations (8.28) through (8.32) are therefore applicable.



**FIG. 8.35**  
AC equivalent circuit for Fig. 8.34.

d. Eq. (8.28):  $Z_i = R_1 \parallel R_2 = 10 \text{ M}\Omega \parallel 110 \text{ M}\Omega = 9.17 \text{ M}\Omega$

e. Eq. (8.29):  $Z_o = r_d \parallel R_D = 100 \text{ k}\Omega \parallel 1.8 \text{ k}\Omega = 1.77 \text{ k}\Omega \approx R_D = 1.8 \text{ k}\Omega$

f.  $r_d \geq 10R_D \rightarrow 100 \text{ k}\Omega \geq 18 \text{ k}\Omega$

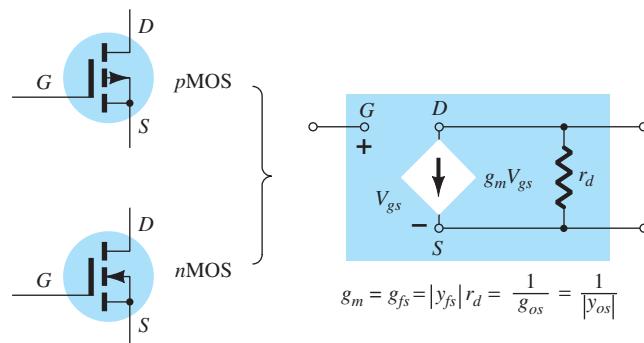
Eq. (8.32):  $A_v = -g_m R_D = -(4.47 \text{ mS})(1.8 \text{ k}\Omega) = 8.05$

## 8.9 ENHANCEMENT-TYPE MOSFETS

The enhancement-type MOSFET (E-MOSFET) can be either an *n*-channel (*n*MOS) or *p*-channel (*p*MOS) device, as shown in Fig. 8.36. The ac small-signal equivalent circuit of either device is shown in Fig. 8.36, revealing an open-circuit between gate and drain–source channel and a current source from drain to source having a magnitude dependent on the gate-to-source voltage. There is an output impedance from drain to source  $r_d$ , which is usually provided on specification sheets as a conductance  $g_{os}$  or admittance  $y_{os}$ . The device transconductance  $g_m$  is provided on specification sheets as the forward transfer admittance  $y_{fs}$ .

In our analysis of JFETs, an equation for  $g_m$  was derived from Shockley's equation. For E-MOSFETs, the relationship between output current and controlling voltage is defined by

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$



**FIG. 8.36**  
Enhancement MOSFET ac small-signal model.

Since  $g_m$  is still defined by

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

we can take the derivative of the transfer equation to determine  $g_m$  as an operating point. That is,

$$\begin{aligned} g_m &= \frac{dI_D}{dV_{GS}} = \frac{d}{dV_{GS}} k(V_{GS} - V_{GS(\text{Th})})^2 = k \frac{d}{dV_{GS}} (V_{GS} - V_{GS(\text{Th})})^2 \\ &= 2k(V_{GS} - V_{GS(\text{Th})}) \frac{d}{dV_{GS}} (V_{GS} - V_{GS(\text{Th})}) = 2k(V_{GS} - V_{GS(\text{Th})})(1 - 0) \end{aligned}$$

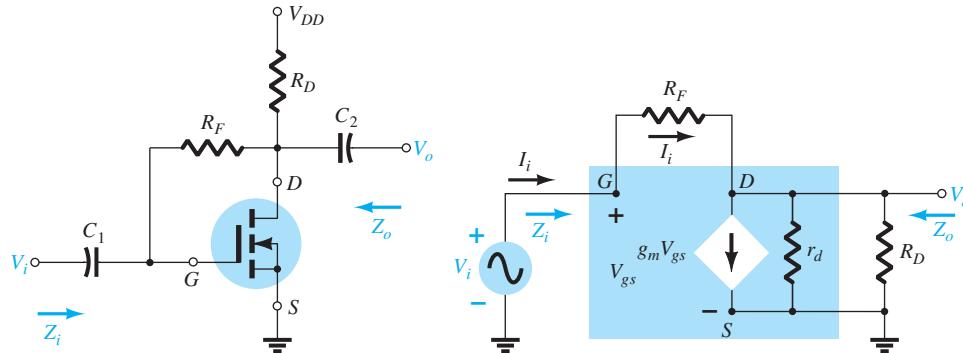
and

$$g_m = 2k(V_{GS_Q} - V_{GS(\text{Th})}) \quad (8.45)$$

Recall that the constant  $k$  can be determined from a given typical operating point on a specification sheet. In every other respect, the ac analysis is the same as that employed for JFETs or D-MOSFETs. Be aware, however, that the characteristics of an E-MOSFET are such that the biasing arrangements are somewhat limited.

## 8.10 E-MOSFET DRAIN-FEEDBACK CONFIGURATION

The E-MOSFET drain-feedback configuration appears in Fig. 8.37. Recall from dc calculations that  $R_G$  could be replaced by a short-circuit equivalent since  $I_G = 0$  A and therefore  $V_{R_G} = 0$  V. However, for ac situations it provides an important high impedance between  $V_o$  and  $V_i$ . Otherwise, the input and output terminals would be connected directly and  $V_o = V_i$ .



**FIG. 8.37**

E-MOSFET drain-feedback configuration.

**FIG. 8.38**

AC equivalent of the network of Fig. 8.37.

Substituting the ac equivalent model for the device results in the network of Fig. 8.38. Note that  $R_F$  is not within the shaded area defining the equivalent model of the device, but does provide a direct connection between input and output circuits.

**Z1** Applying Kirchhoff's current law to the output circuit (at node D in Fig. 8.38) results in

$$I_i = g_m V_{gs} + \frac{V_o}{r_d \| R_D}$$

and

$$V_{gs} = V_i$$

so that

$$I_i = g_m V_i + \frac{V_o}{r_d \| R_D}$$

or

$$I_i - g_m V_i = \frac{V_o}{r_d \| R_D}$$

Therefore,

$$V_o = (r_d \| R_D)(I_i - g_m V_i)$$

with

$$I_i = \frac{V_i - V_o}{R_F} = \frac{V_i - (r_d \| R_D)(I_i - g_m V_i)}{R_F}$$

and

so that

$$I_i R_F = V_i - (r_d \| R_D) I_i + (r_d \| R_D) g_m V_i \\ V_i [1 + g_m (r_d \| R_D)] = I_i [R_F + r_d \| R_D]$$

and finally,

$$Z_i = \frac{V_i}{I_i} = \frac{R_F + r_d \| R_D}{1 + g_m (r_d \| R_D)} \quad (8.46)$$

Typically,  $R_F \gg r_d \| R_D$ , so that

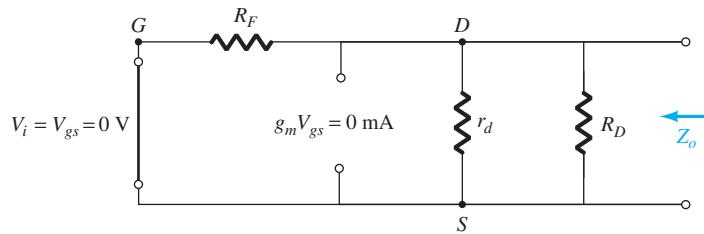
$$Z_i \approx \frac{R_F}{1 + g_m (r_d \| R_D)}$$

For  $r_d \geq 10R_D$ ,

$$Z_i \approx \frac{R_F}{1 + g_m R_D} \quad R_F \gg r_d \| R_D, r_d \geq 10R_D \quad (8.47)$$

**Z<sub>o</sub>** Substituting  $V_i = 0$  V results in  $V_{gs} = 0$  V and  $g_m V_{gs} = 0$ , with a short-circuit path from gate to ground as shown in Fig. 8.39.  $R_F$ ,  $r_d$ , and  $R_D$  are then in parallel and

$$Z_o = R_F \| r_d \| R_D \quad (8.48)$$



**FIG. 8.39**  
Determining  $Z_o$  for the network of Fig. 8.37.

Normally,  $R_F$  is so much larger than  $r_d \| R_D$  that

$$Z_o \approx r_d \| R_D$$

and with  $r_d \geq 10R_D$ ,

$$Z_o \approx R_D \quad R_F \gg r_d \| R_D, r_d \geq 10R_D \quad (8.49)$$

**A<sub>v</sub>** Applying Kirchhoff's current law at node D of Fig. 8.38 results in

$$I_i = g_m V_{gs} + \frac{V_o}{r_d \| R_D}$$

$$\text{but } V_{gs} = V_i \quad \text{and} \quad I_i = \frac{V_i - V_o}{R_F}$$

$$\text{so that } \frac{V_i - V_o}{R_F} = g_m V_i + \frac{V_o}{r_d \| R_D}$$

$$\text{and } \frac{V_i}{R_F} - \frac{V_o}{R_F} = g_m V_i + \frac{V_o}{r_d \| R_D}$$

$$\text{so that } V_o \left[ \frac{1}{r_d \| R_D} + \frac{1}{R_F} \right] = V_i \left[ \frac{1}{R_F} - g_m \right]$$

$$\text{and } A_v = \frac{V_o}{V_i} = \frac{\left[ \frac{1}{R_F} - g_m \right]}{\left[ \frac{1}{r_d \| R_D} + \frac{1}{R_F} \right]}$$

$$\text{but } \frac{1}{r_d \| R_D} + \frac{1}{R_F} = \frac{1}{R_F \| r_d \| R_D}$$

and

$$g_m \gg \frac{1}{R_F}$$

so that

$$A_v = -g_m(R_F \| R_d \| R_D) \quad (8.50)$$

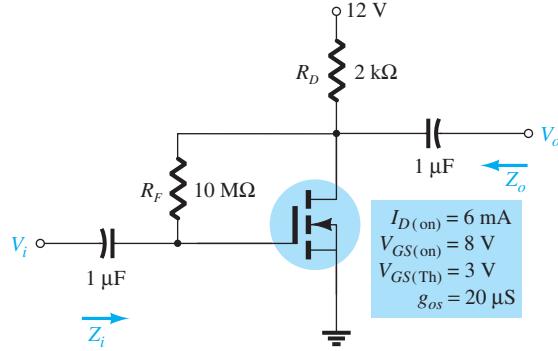
Since  $R_F$  is usually  $\gg r_d \| R_D$  and if  $r_d \geq 10R_D$ ,

$$A_v \cong -g_m R_D \quad R_F \gg r_d \| R_D, r_d \geq 10R_D \quad (8.51)$$

**Phase Relationship** The negative sign for  $A_v$  reveals that  $V_o$  and  $V_i$  are out of phase by  $180^\circ$ .

**EXAMPLE 8.12** The E-MOSFET of Fig. 8.40 was analyzed in Example 7.10, with the result that  $k = 0.24 \times 10^{-3} \text{ A/V}^2$ ,  $V_{GSQ} = 6.4 \text{ V}$ , and  $I_{DQ} = 2.75 \text{ mA}$ .

- Determine  $g_m$ .
- Find  $r_d$ .
- Calculate  $Z_i$  with and without  $r_d$ . Compare results.
- Find  $Z_o$  with and without  $r_d$ . Compare results.
- Find  $A_v$  with and without  $r_d$ . Compare results.



**FIG. 8.40**  
Drain-feedback amplifier from Example 8.11.

**Solution:**

a.  $g_m = 2k(V_{GSQ} - V_{GS(\text{Th})}) = 2(0.24 \times 10^{-3} \text{ A/V}^2)(6.4 \text{ V} - 3 \text{ V}) = 1.63 \text{ mS}$

b.  $r_d = \frac{1}{g_{os}} = \frac{1}{20 \mu\text{S}} = 50 \text{ k}\Omega$

c. With  $r_d$ ,

$$\begin{aligned} Z_i &= \frac{R_F + r_d \| R_D}{1 + g_m(r_d \| R_D)} = \frac{10 \text{ M}\Omega + 50 \text{ k}\Omega \| 2 \text{ k}\Omega}{1 + (1.63 \text{ mS})(50 \text{ k}\Omega \| 2 \text{ k}\Omega)} \\ &= \frac{10 \text{ M}\Omega + 1.92 \text{ k}\Omega}{1 + 3.13} = 2.42 \text{ M}\Omega \end{aligned}$$

Without  $r_d$ ,

$$Z_i \cong \frac{R_F}{1 + g_m R_D} = \frac{10 \text{ M}\Omega}{1 + (1.63 \text{ mS})(2 \text{ k}\Omega)} = 2.53 \text{ M}\Omega$$

which shows that since the condition  $r_d \geq 10R_D = 50 \text{ k}\Omega \geq 40 \text{ k}\Omega$  is satisfied, the results for  $Z_o$  with or without  $r_d$  will be quite close.

d. With  $r_d$ ,

$$\begin{aligned} Z_o &= R_F \| r_d \| R_D = 10 \text{ M}\Omega \| 50 \text{ k}\Omega \| 2 \text{ k}\Omega = 49.75 \text{ k}\Omega \| 2 \text{ k}\Omega \\ &= 1.92 \text{ k}\Omega \end{aligned}$$

Without  $r_d$ ,

$$Z_o \cong R_D = 2 \text{ k}\Omega$$

again providing very close results.

e. With  $r_d$ ,

$$\begin{aligned} A_v &= -g_m(R_F \parallel r_d \parallel R_D) \\ &= -(1.63 \text{ mS})(10 \text{ M}\Omega \parallel 50 \text{ k}\Omega \parallel 2 \text{ k}\Omega) \\ &= -(1.63 \text{ mS})(1.92 \text{ k}\Omega) \\ &= -3.21 \end{aligned}$$

Without  $r_d$ ,

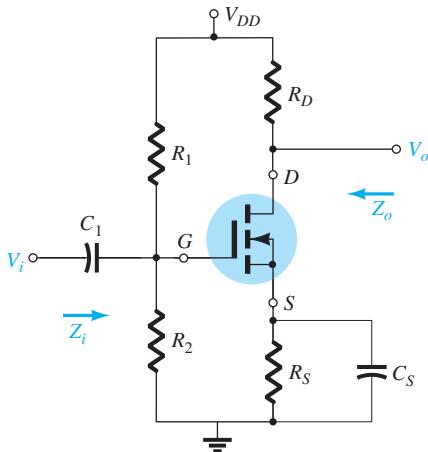
$$\begin{aligned} A_v &= -g_m R_D = -(1.63 \text{ mS})(2 \text{ k}\Omega) \\ &= -3.26 \end{aligned}$$

which is very close to the above result.

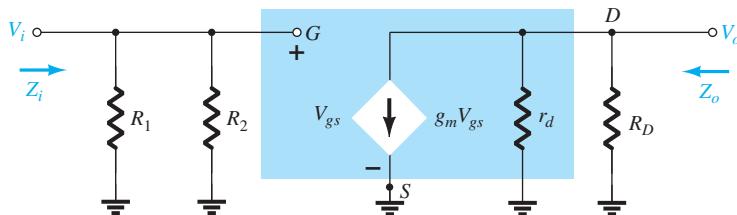
## 8.11 E-MOSFET VOLTAGE-DIVIDER CONFIGURATION

The last E-MOSFET configuration to be examined in detail is the voltage-divider network of Fig. 8.41. The format is exactly the same as appearing in a number of earlier discussions.

Substituting the ac equivalent network for the E-MOSFET results in the configuration of Fig. 8.42, which is exactly the same as Fig. 8.23. The result is that Eqs. (8.28) through (8.32) are applicable, as listed below for the E-MOSFET.

**FIG. 8.41**

E-MOSFET voltage-divider configuration.

**FIG. 8.42**

AC equivalent network for the configuration of Fig. 8.41.

**Z<sub>i</sub>**

$$Z_i = R_1 \parallel R_2 \quad (8.52)$$

**Z<sub>o</sub>**

$$Z_o = r_d \parallel R_D \quad (8.53)$$

For  $r_d \geq 10R_D$ ,

$$Z_o \cong R_d \quad r_d \geq 10R_D \quad (8.54)$$

**A<sub>v</sub>**

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \parallel R_D) \quad (8.55)$$

and if  $r_d \geq 10R_D$ ,

$$A_v = \frac{V_o}{V_i} \cong -g_m R_D \quad (8.56)$$

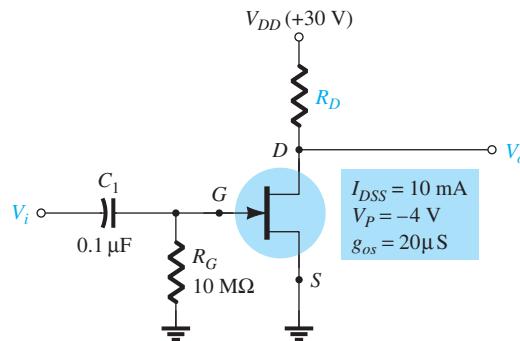
## 8.12 DESIGNING FET AMPLIFIER NETWORKS

Design problems at this stage are limited to obtaining a desired dc bias condition or ac voltage gain. In most cases, the various equations developed are used “in reverse” to define the parameters necessary to obtain the desired gain, input impedance, or output impedance. To avoid unnecessary complexity during the initial stages of the design, the approximate equations are often employed because some variation will occur when calculated resistors are replaced by standard values. Once the initial design is completed, the results can be tested and refinements made using the complete equations.

Throughout the design procedure be aware that although superposition permits a separate analysis and design of the network from a dc and an ac viewpoint, a parameter chosen in the dc environment will often play an important role in the ac response. In particular, recall that the resistance  $R_G$  could be replaced by a short-circuit equivalent in the feedback configuration because  $I_G \cong 0$  A for dc conditions, but for the ac analysis, it presents an important high-impedance path between  $V_o$  and  $V_i$ . In addition, recall that  $g_m$  is larger for operating points closer to the  $I_D$  axis ( $V_{GS} = 0$  V), requiring that  $R_S$  be relatively small. In the unbypassed  $R_S$  network, a small  $R_S$  will also contribute to a higher gain, but for the source-follower, the gain is reduced from its maximum value of 1. In total, simply keep in mind that network parameters can affect the dc and ac levels in different ways. Often a balance must be made between a particular operating point and its effect on the ac response.

In most situations, the available dc supply voltage is known, the FET to be employed has been determined, and the capacitors to be employed at the chosen frequency are defined. It is then necessary to determine the resistive elements necessary to establish the desired gain or impedance level. The next three examples determine the required parameters for a specific gain.

**EXAMPLE 8.13** Design the fixed-bias network of Fig. 8.43 to have an ac gain of 10. That is, determine the value of  $R_D$ .



**FIG. 8.43**  
Circuit for desired voltage gain in Example 8.13.

**Solution:** Since  $V_{GSQ} = 0$  V, the level of  $g_m$  is  $g_{m0}$ . The gain is therefore determined by

$$A_v = -g_m(R_D \| r_d) = -g_{m0}(R_D \| r_d)$$

with

$$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10 \text{ mA})}{4 \text{ V}} = 5 \text{ mS}$$

The result is

$$-10 = -5 \text{ mS}(R_D \| r_d)$$

and

$$R_D \| r_d = \frac{10}{5 \text{ mS}} = 2 \text{ kΩ}$$

From the device specifications,

$$r_d = \frac{1}{g_{os}} = \frac{1}{20 \times 10^{-6} \text{ S}} = 50 \text{ k}\Omega$$

Substituting, we find

$$R_D \| r_d = R_D \| 50 \text{ k}\Omega = 2 \text{ k}\Omega$$

and

$$\frac{R_D(50 \text{ k}\Omega)}{R_D + 50 \text{ k}\Omega} = 2 \text{ k}\Omega$$

or

$$50R_D = 2(R_D + 50 \text{ k}\Omega) = 2R_D + 100 \text{ k}\Omega$$

with

$$48R_D = 100 \text{ k}\Omega$$

and

$$R_D = \frac{100 \text{ k}\Omega}{48} \approx 2.08 \text{ k}\Omega$$

The closest standard value is **2 kΩ** (Appendix D), which would be employed for this design.

The resulting level of  $V_{DSQ}$  is then determined as follows:

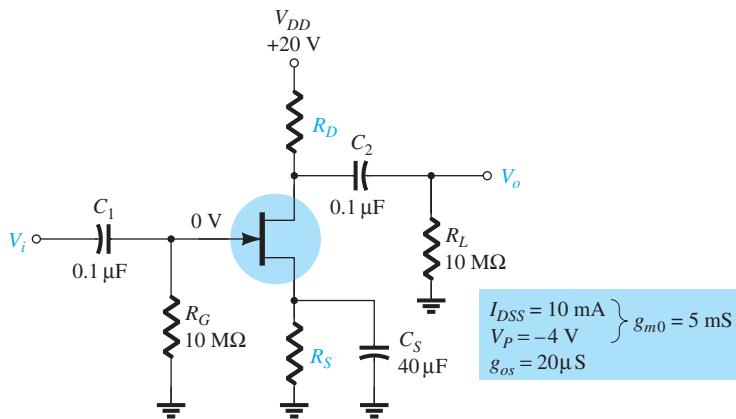
$$V_{DSQ} = V_{DD} - I_{DQ}R_D = 30 \text{ V} - (10 \text{ mA})(2 \text{ k}\Omega) = 10 \text{ V}$$

The levels of  $Z_i$  and  $Z_o$  are set by the levels of  $R_G$  and  $R_D$ , respectively. That is,

$$Z_i = R_G = 10 \text{ M}\Omega$$

$$Z_o = R_D \| r_d = 2 \text{ k}\Omega \| 50 \text{ k}\Omega = 1.92 \text{ k}\Omega \approx R_D = 2 \text{ k}\Omega$$

**EXAMPLE 8.14** Choose the values of  $R_D$  and  $R_S$  for the network of Fig. 8.44 that will result in a gain of 8 using a relatively high level of  $g_m$  for this device defined at  $V_{GSQ} = \frac{1}{4}V_P$ .



**FIG. 8.44**  
Network for desired voltage gain in Example 8.14.

**Solution:** The operating point is defined by

$$V_{GSQ} = \frac{1}{4}V_P = \frac{1}{4}(-4 \text{ V}) = -1 \text{ V}$$

$$\text{and } I_D = I_{DSS} \left( 1 - \frac{V_{GSQ}}{V_P} \right)^2 = 10 \text{ mA} \left( 1 - \frac{(-1 \text{ V})}{(-4 \text{ V})} \right)^2 = 5.625 \text{ mA}$$

Determining  $g_m$ , we obtain

$$\begin{aligned} g_m &= g_{m0} \left( 1 - \frac{V_{GSQ}}{V_P} \right) \\ &= 5 \text{ mS} \left( 1 - \frac{(-1 \text{ V})}{(-4 \text{ V})} \right) = 3.75 \text{ mS} \end{aligned}$$

The magnitude of the ac voltage gain is determined by

$$|A_v| = g_m(R_D \| r_d)$$

Substituting known values results in

$$8 = (3.75 \text{ mS})(R_D \| r_d)$$

so that  $R_D \| r_d = \frac{8}{3.75 \text{ mS}} = 2.13 \text{ k}\Omega$

The level of  $r_d$  is defined by

$$r_d = \frac{1}{g_{os}} = \frac{1}{20 \mu\text{S}} = 50 \text{ k}\Omega$$

and

$$R_D \| 50 \text{ k}\Omega = 2.13 \text{ k}\Omega$$

with the result that

$$R_D = 2.2 \text{ k}\Omega$$

which is a standard value.

The level of  $R_S$  is determined by the dc operating conditions as follows:

$$\begin{aligned} V_{GS_Q} &= -I_D R_S \\ -1 \text{ V} &= -(5.625 \text{ mA}) R_S \end{aligned}$$

and

$$R_S = \frac{1 \text{ V}}{5.625 \text{ mA}} = 177.8 \Omega$$

The closest standard value is **180 Ω**. In this example,  $R_S$  does not appear in the ac design because of the shorting effect of  $C_S$ .

In the next example,  $R_S$  is unbypassed and the design becomes a bit more complicated.

**EXAMPLE 8.15** Determine  $R_D$  and  $R_S$  for the network of Fig. 8.44 to establish a gain of 8 if the bypass capacitor  $C_S$  is removed.

**Solution:**  $V_{GS_Q}$  and  $I_{DQ}$  are still  $-1 \text{ V}$  and  $5.625 \text{ mA}$ , respectively, and since the equation  $V_{GS} = -I_D R_S$  has not changed,  $R_S$  continues to equal the standard value of **180 Ω** obtained in Example 8.14.

The gain of an unbypassed self-bias configuration is

$$A_v = -\frac{g_m R_D}{1 + g_m R_S}$$

For the moment it is assumed that  $r_d \geq 10(R_D + R_S)$ . Using the full equation for  $A_v$  at this stage of the design would simply complicate the process unnecessarily.

Substituting (for the specified magnitude of 8 for the gain), we obtain

$$|8| = \left| \frac{-(3.75 \text{ mS}) R_D}{1 + (3.75 \text{ mS})(180 \Omega)} \right| = \frac{(3.75 \text{ mS}) R_D}{1 + 0.675}$$

and

$$8(1 + 0.675) = (3.75 \text{ mS}) R_D$$

so that

$$R_D = \frac{13.4}{3.75 \text{ mS}} = 3.573 \text{ k}\Omega$$

with the closest standard value at **3.6 kΩ**.

We can now test the condition

$$r_d \geq 10(R_D + R_S)$$

We have  $50 \text{ k}\Omega \geq 10(3.6 \text{ k}\Omega + 0.18 \text{ k}\Omega) = 10(3.78 \text{ k}\Omega)$

and

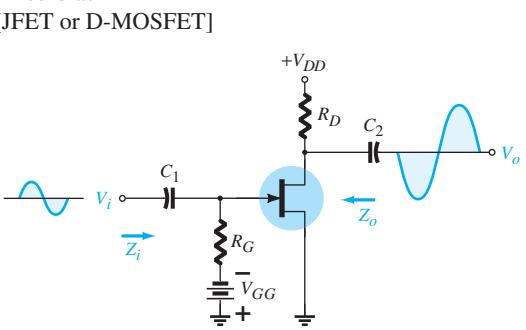
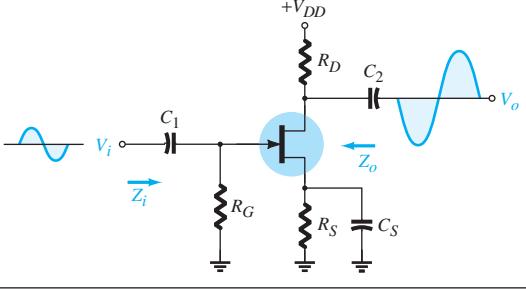
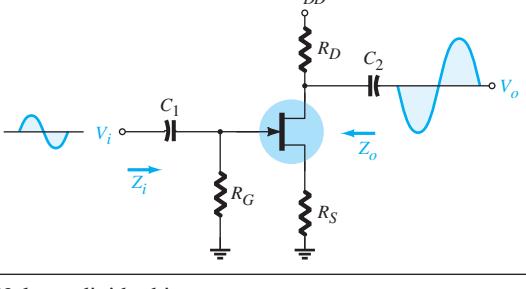
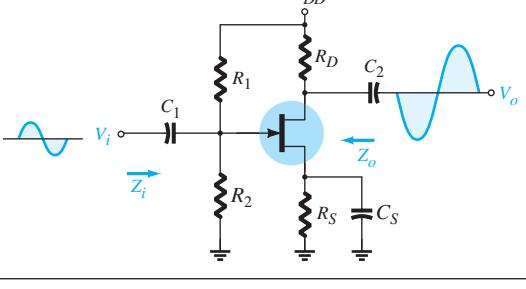
$$50 \text{ k}\Omega \geq 37.8 \text{ k}\Omega$$

which is satisfied—the solution stands!

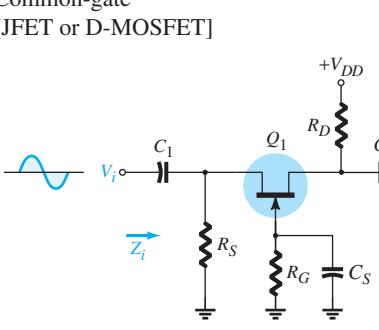
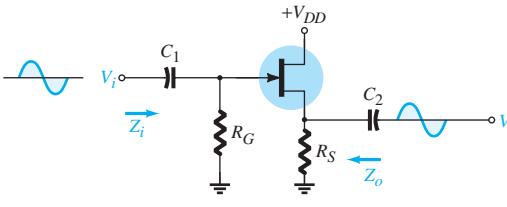
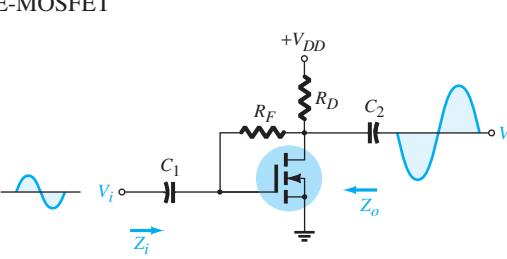
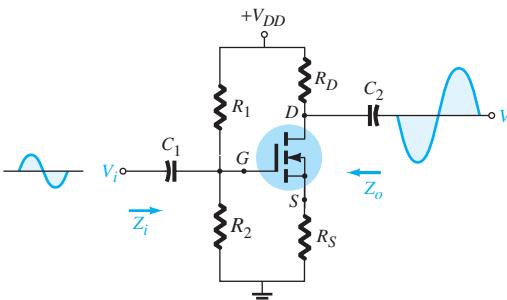
### 8.13 SUMMARY TABLE

To provide a quick comparison between configurations and offer a listing that can be helpful for a variety of reasons, Table 8.1 was developed. The exact and approximate equations for each important parameter are provided with a typical range of values for each. Although

**TABLE 8.1**  
 $Z_i$ ,  $Z_o$ , and  $A_v$  for various FET configurations

Configuration	$Z_i$	$Z_o$	$A_v = \frac{V_o}{V_i}$
Fixed-bias [JFET or D-MOSFET]	 <p>High (10 MΩ)  <math>= R_G</math></p>	<p>Medium (2 kΩ)  <math>= R_D \  r_d</math>  <math>\cong R_D</math> (<math>r_d \geq 10 R_D</math>)</p>	<p>Medium (-10)  <math>= -g_m(r_d \  R_D)</math>  <math>\cong -g_m R_D</math> (<math>r_d \geq 10 R_D</math>)</p>
Self-bias bypassed $R_S$ [JFET or D-MOSFET]	 <p>High (10 MΩ)  <math>= R_G</math></p>	<p>Medium (2 kΩ)  <math>= R_D \  r_d</math>  <math>\cong R_D</math> (<math>r_d \geq 10 R_D</math>)</p>	<p>Medium (-10)  <math>= -g_m(r_d \  R_D)</math>  <math>\cong -g_m R_D</math> (<math>r_d \geq 10 R_D</math>)</p>
Self-bias unbypassed $R_S$ [JFET or D-MOSFET]	 <p>High (10 MΩ)  <math>= R_G</math></p>	$= \frac{\left[ 1 + g_m R_S + \frac{R_S}{r_d} \right] R_D}{\left[ 1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d} \right]}$ $= R_D \quad r_d \geq 10 R_D \text{ or } r_d \approx \infty \Omega$	<p>Low (-2)  <math>= \frac{g_m R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}</math>  <math>\cong -\frac{g_m R_D}{1 + g_m R_S} \quad [r_d \geq 10 (R_D + R_S)]</math></p>
Voltage-divider bias [JFET or D-MOSFET]	 <p>High (10 MΩ)  <math>= R_1 \  R_2</math></p>	<p>Medium (2 kΩ)  <math>= R_D \  r_d</math>  <math>\cong R_D</math> (<math>r_d \geq 10 R_D</math>)</p>	<p>Medium (-10)  <math>= -g_m(r_d \  R_D)</math>  <math>\cong -g_m R_D</math> (<math>r_d \geq 10 R_D</math>)</p>

**TABLE 8.1**  
(Continued)

Configuration	$Z_i$	$Z_o$	$A_v = \frac{V_o}{V_i}$
Common-gate [JFET or D-MOSFET]		<p>Low (<math>1\text{ k}\Omega</math>)</p> $= R_S \parallel \left[ \frac{r_d + R_D}{1 + g_m r_d} \right]$ $\cong R_S \parallel \frac{1}{g_m} \quad (r_d \geq 10 R_D)$ <p>Medium (<math>2\text{ k}\Omega</math>)</p> $= R_D \parallel r_d$ $\cong R_D \quad (R_d \geq 10 R_D)$	<p>Medium (+10)</p> $= \frac{g_m R_D + \frac{R_D}{r_d}}{1 + \frac{R_D}{r_d}}$ $\cong g_m R_D \quad (r_d \geq 10 R_D)$
Source-follower [JFET or D-MOSFET]		<p>High (<math>10\text{ M}\Omega</math>)</p> $= R_G$	<p>Low (&lt;1)</p> $= \frac{g_m(r_d \parallel R_S)}{1 + g_m(r_d \parallel R_S)}$ $\cong \frac{g_m R_S}{1 + g_m R_S} \quad (r_d \geq 10 R_S)$
Drain-feedback bias E-MOSFET		<p>Medium (<math>1\text{ M}\Omega</math>)</p> $= \frac{R_F + r_d \parallel R_D}{1 + g_m(r_d \parallel R_D)}$ $\cong \frac{R_F}{1 + g_m R_D} \quad (r_d \geq 10 R_D)$	<p>Medium (2 kΩ)</p> $= R_F \parallel r_d \parallel R_D$ $\cong R_D \quad (R_F, r_d \geq 10 R_D)$ <p>Medium (-10)</p> $= -g_m(R_F \parallel r_d \parallel R_D)$ $\cong -g_m R_D \quad (R_F, r_d \geq 10 R_D)$
Voltage-divider bias E-MOSFET		<p>Medium (1 MΩ)</p> $= R_1 \parallel R_2$	<p>Medium (2 kΩ)</p> $= R_D \parallel r_d$ $\cong R_D \quad (r_d \geq 10 R_D)$ <p>Medium (-10)</p> $= -g_m(r_d \parallel R_D)$ $\cong -g_m R_D \quad (r_d \geq 10 R_D)$

all the possible configurations are not present, the majority of the most frequently encountered are included. In fact, any configuration not listed will probably be some variation of those appearing in the table, so at the very least, the listing will provide some insight as to what expected levels should be and which path will probably generate the desired equations. The format chosen was designed to permit a duplication of the entire table on the front and back of one  $8\frac{1}{2}$  by 11 inch page.

## 8.14 EFFECT OF $R_L$ AND $R_{sig}$

This section will parallel Sections 5.16 and 5.17 of the BJT small-signal ac analysis chapter dealing with the effect of the source resistance and load resistance on the ac gain of an amplifier. There are again two approaches to the analysis. One can simply substitute the ac model for the FET of interest and perform a detailed analysis similar to the unloaded situation, or apply the two-port equations introduced in Section 5.17.

*All of the two-port equations developed for the BJT transistor apply to FET networks also because the quantities of interest are defined at the input and output terminals and not the components of the system.*

A few of the most important equations are repeated below to provide an easy reference for the analysis of this chapter and to refresh your memory about the conclusions:

$$A_{v_L} = \frac{R_L}{R_L + R_o} A_{v_{NL}} \quad (8.57)$$

$$A_i = -A_{v_L} \frac{Z_i}{R_L} \quad (8.58)$$

$$A_{v_s} = \frac{V_o}{V_s} = \frac{V_i}{V_s} \cdot \frac{V_o}{V_i} = \left( \frac{R_i}{R_i + R_{sig}} \right) \left( \frac{R_L}{R_L + R_o} \right) A_{v_{NL}} \quad (8.59)$$

Some of the important conclusions about the gain of BJT transistor configurations are also applicable to FET networks. They include the following facts:

*The greatest gain of an amplifier is the no-load gain.*

*The loaded gain is always less than the no-load gain.*

*A source impedance will always reduce the overall gain below the no-load or loaded level.*

In general, therefore,

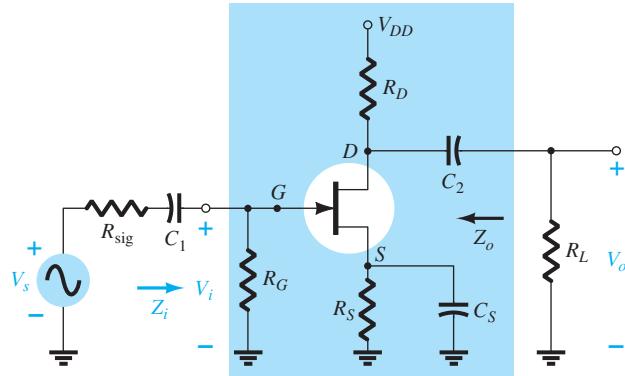
$$A_{v_{NL}} > A_{v_L} > A_{v_s} \quad (8.60)$$

Recall from Chapter 5 that some BJT configurations are such that the output impedance is sensitive to the source impedance or the input impedance is sensitive to the applied load. For FET networks, however:

*Due to the high impedance between the gate terminal and the channel, one can generally assume that the input impedance is unaffected by the load resistor and the output impedance is unaffected by the source resistance.*

One must always be aware, however, that there are special situations where the above may not be totally true. Take, for instance, the feedback configuration that results in a direct connection between input and output networks. Although the feedback resistor is usually many times that of the source resistance, permitting the approximation that the source resistance is essentially  $0 \Omega$ , it does present a situation where the source resistance could possibly affect the output resistance or the load resistance could affect the input impedance. In general, however, due to the high isolation provided between the gate and the drain or source terminals, the general equations for the loaded gain are less complex than those encountered for BJT transistors. Recall that the base current provided a direct link between input and output circuits of any BJT transistor configuration.

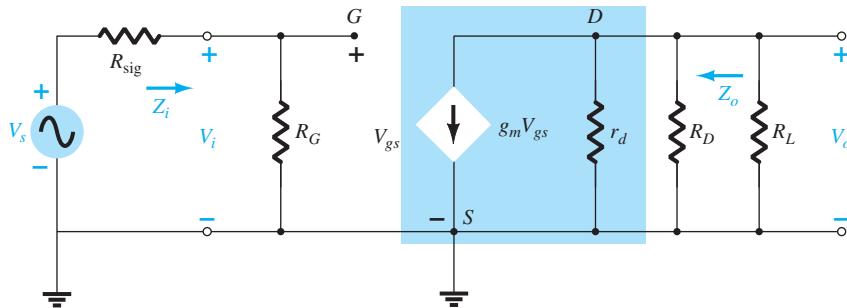
To demonstrate each approach, let us examine the self-bias configuration of Fig. 8.45 with a bypassed source resistance. Substituting the ac equivalent model for the JFET results in the configuration of Fig. 8.46.



**FIG. 8.45**  
JFET amplifier with  $R_{\text{sig}}$  and  $R_L$ .

Note that the load resistance appears in parallel with the drain resistance and the source resistance  $R_{\text{sig}}$  appears in series with the gate resistance  $R_G$ . For the overall voltage gain the result is a modified form of Eq. (8.21):

$$A_{vL} = \frac{V_o}{V_i} = -g_m(r_d \| R_D \| R_L) \quad (8.61)$$



**FIG. 8.46**  
Network of Fig. 8.45 following the substitution of the ac equivalent circuit for the JFET.

The output impedance is the same as obtained for the unloaded situation without a source resistance:

$$Z_o = r_d \| R_D \quad (8.62)$$

The input impedance remains as

$$Z_i = R_G \quad (8.63)$$

For the overall gain  $A_{vS}$ ,

$$V_i = \frac{R_G V_S}{R_G + R_{\text{sig}}}$$

and

$$A_{v_s} = \frac{V_o}{V_s} = \frac{V_i}{V_s} \cdot \frac{V_o}{V_i} = \left[ \frac{R_G}{R_G + R_{\text{sig}}} \right] [-g_m(r_d \| R_D \| R_L)] \quad (8.64)$$

which for most applications where  $R_G \gg R_{\text{sig}}$  and  $R_D \| R_L \ll r_d$  results in

$$A_{v_s} \cong -g_m(R_D \| R_L) \quad (8.65)$$

If we now turn to the two-port approach for the same network, the equation for the overall gain becomes

$$A_{v_L} = \frac{R_L}{R_L + R_o} A_{v_{NL}} = \frac{R_L}{R_L + R_o} [-g_m(r_d \| R_D)]$$

but

$$R_o = R_D \| r_d,$$

$$\text{so that } A_{v_L} = \frac{R_L}{R_L + R_D \| r_d} [-g_m(r_d \| R_D)] = -g_m \frac{(r_d \| R_D)(R_L)}{(r_d + R_D) + R_L}$$

and

$$A_{v_L} = -g_m(r_d \| R_D \| R_L)$$

matching the previous result.

The above derivation was included to demonstrate that the same result will be obtained using either approach. If numerical values for  $R_i$ ,  $R_o$ , and  $A_{v_{NL}}$  were available, it would simply be a matter of substituting the values into Eq. (8.57).

Continuing in the same manner for the most common configurations results in the equations of Table 8.2.

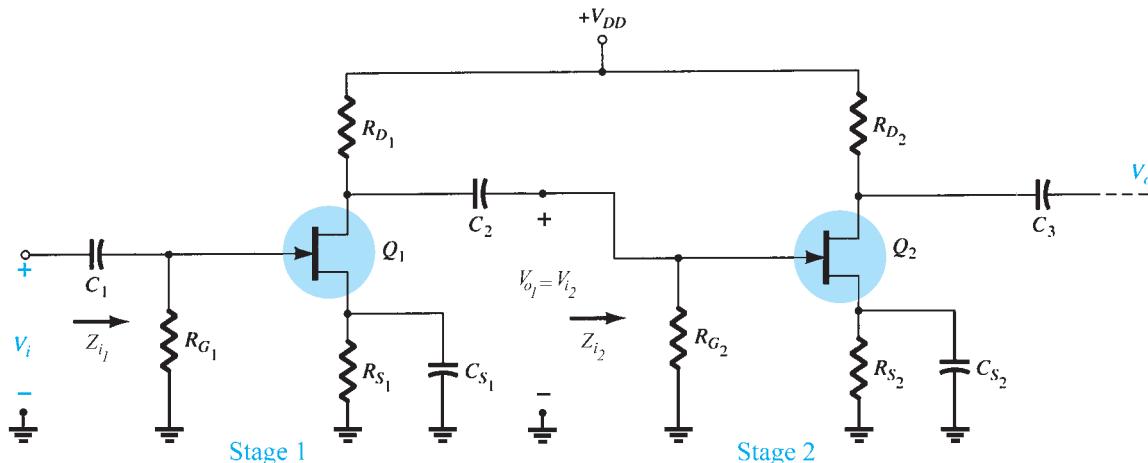
## 8.15 CASCADE CONFIGURATION

The cascade configuration introduced in Chapter 5 for BJTs can also be used with JFETs or MOSFETs, as shown for JFETs in Fig. 8.47. Recall that the output of one stage appears as the input for the following stage. The input impedance for the second stage is the load impedance for the first stage.

*The total gain is the product of the gain of each stage including the loading effects of the following stage.*

Too often, the no-load gain is employed and the overall gain is an unrealistic result. For each stage the loading effect of the following stage must be included in the gain calculations. Using the results of the previous sections of this chapter results in the following equation for the overall gain of the configuration of Fig. 8.47:

$$A_v = A_{v_1} A_{v_2} = (-g_{m1} R_{D1})(-g_{m2} R_{D2}) = g_{m1} g_{m2} R_{D1} R_{D2} \quad (8.66)$$



**FIG. 8.47**  
Cascaded FET amplifier.

TABLE 8.2

Configuration	$A_{v_L} = V_o \parallel V_i$	$Z_i$	$Z_o$
	$-g_m(R_D \parallel R_L)$  Including $r_d$ : $-g_m(R_D \parallel R_L \parallel r_d)$	$R_G$	$R_D$
	$\frac{-g_m(R_D \parallel R_L)}{1 + g_m R_S}$  Including $r_d$ : $\frac{-g_m(R_D \parallel R_L)}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$	$R_G$	$\frac{R_D}{1 + g_m R_S} \cong \frac{R_D}{1 + g_m R_S}$
	$-g_m(R_D \parallel R_L)$  Including $r_d$ : $-g_m(R_D \parallel R_L \parallel r_d)$	$R_1 \parallel R_2$	$R_D$
	$\frac{g_m(R_S \parallel R_L)}{1 + g_m(R_S \parallel R_L)}$  Including $r_d$ : $= \frac{g_m r_d (R_S \parallel R_L)}{r_d + R_D + g_m r_d (R_S \parallel R_L)}$	$R_G$	$R_S \parallel 1/g_m$
	$g_m(R_D \parallel R_L)$  Including $r_d$ : $\cong g_m(R_D \parallel R_L)$	$Z_i = \frac{R_S}{1 + \frac{g_m r_d R_S}{r_d + R_D \parallel R_L}}$	$R_D \parallel r_d$

The input impedance of the cascade amplifier is that of stage 1,

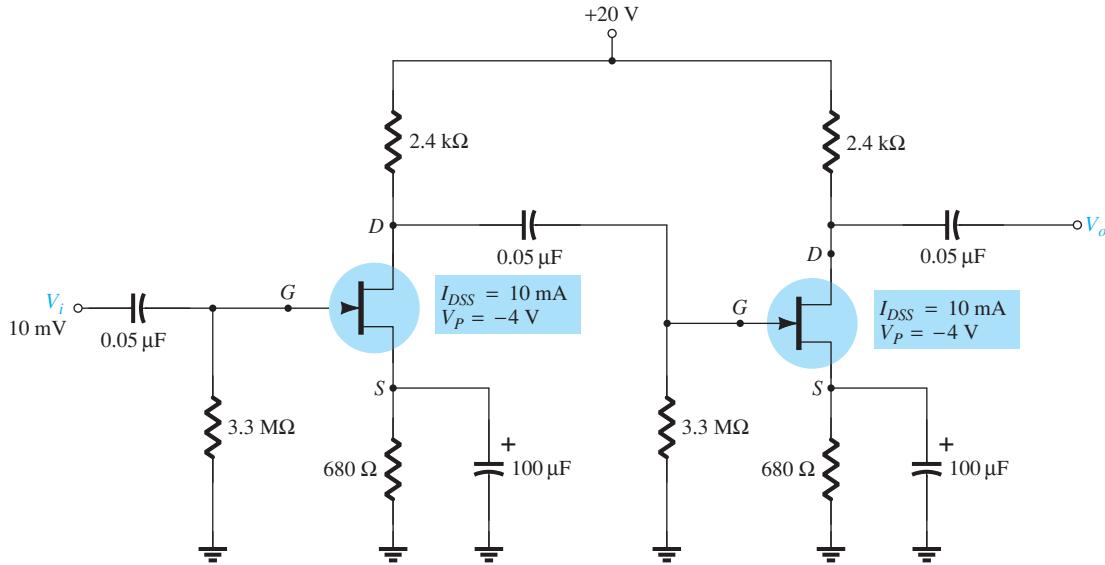
$$Z_i = R_{G_1} \quad (8.67)$$

and the output impedance is that of stage 2,

$$Z_o = R_{D_2} \quad (8.68)$$

The main function of cascading stages is the larger overall gain achieved. Since dc bias and ac calculations for a cascade amplifier follow those derived for the individual stages, an example will demonstrate the various calculations to determine dc bias and ac operation.

**EXAMPLE 8.16** Calculate the dc bias, voltage gain, input impedance, output impedance, and resulting output voltage for the cascade amplifier shown in Fig. 8.48.



**FIG. 8.48**  
Cascade amplifier circuit for Example 8.16.

**Solution:** Both amplifier stages have the same dc bias. Using dc bias techniques from Chapter 7 results in

$$V_{GSQ} = -1.9 \text{ V}, \quad I_{DQ} = 2.8 \text{ mA} \quad g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10 \text{ mA})}{|-4 \text{ V}|} = 5 \text{ mS}$$

and at the dc bias point,

$$g_m = g_{m0} \left( 1 - \frac{V_{GSQ}}{V_P} \right) = (5 \text{ mS}) \left( 1 - \frac{-1.9 \text{ V}}{-4 \text{ V}} \right) = 2.6 \text{ mS}$$

Since the second stage is unloaded

$$A_{v2} = -g_m R_D = -(2.6 \text{ mS})(2.4 \text{ kΩ}) = -6.24$$

For the first stage  $2.4 \text{ kΩ} \parallel 3.3 \text{ MΩ} \approx 2.4 \text{ kΩ}$  resulting in the same gain.  
The cascade amplifier voltage gain is

$$\text{Eq. (8.66): } A_v = A_{v1} A_{v2} = (-6.2)(-6.2) = 38.4$$

Take special note of the fact that the total gain is positive.

The output voltage is then

$$V_o = A_v V_i = (38.4)(10 \text{ mV}) = 384 \text{ mV}$$

The cascade amplifier input impedance is

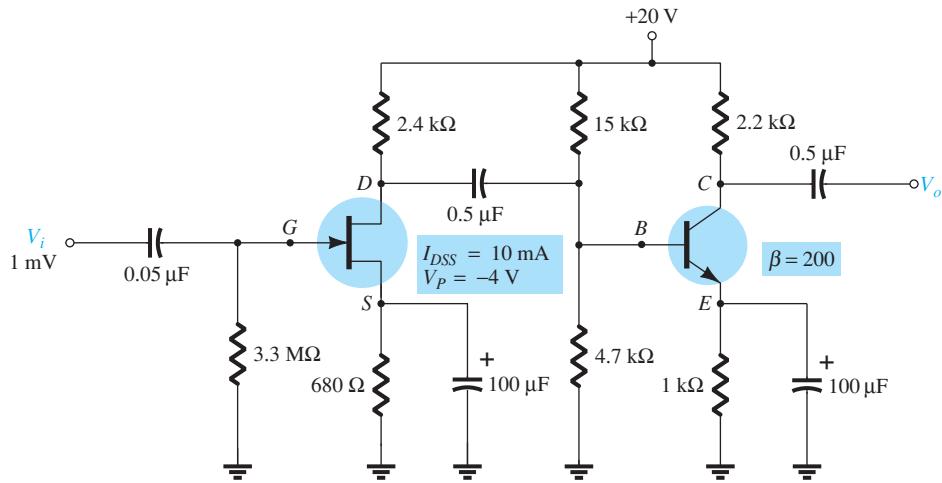
$$Z_i = R_G = 3.3 \text{ M}\Omega$$

The cascade amplifier output impedance (assuming that  $r_d = \infty\Omega$ ) is

$$Z_o = R_D = 2.4 \text{ k}\Omega$$

A combination of FET and BJT stages can also be used to provide high voltage gain and high input impedance, as demonstrated by the next example.

**EXAMPLE 8.17** For the cascade amplifier of Fig. 8.49, use the dc bias calculated in Examples 5.15 and 8.16 to calculate input impedance, output impedance, voltage gain, and resulting output voltage.



**FIG. 8.49**

Cascaded JFET-BJT amplifier for Example 8.17.

**Solution:** Since  $R_i$  (stage 2) =  $15 \text{ k}\Omega \parallel 4.7 \text{ k}\Omega \parallel 200(6.5 \Omega) = 953.6 \Omega$ , the gain of stage 1 (when loaded by stage 2) is

$$\begin{aligned} A_{v_1} &= -g_m[R_D \parallel R_i \text{ (stage 2)}] \\ &= -2.6 \text{ mS}(2.4 \text{ k}\Omega \parallel 953.6 \Omega) = -1.77 \end{aligned}$$

From Example 5.18, the voltage gain of stage 2 is  $A_{v_2} = -338.46$ . The overall voltage gain is then

$$A_v = A_{v_1}A_{v_2} = (-1.77)(-338.46) = 599.1$$

The output voltage is then

$$V_o = A_v V_i = (599.1)(1 \text{ mV}) \approx 0.6 \text{ V}$$

The input impedance of the amplifier is that of stage 1,

$$Z_i = 3.3 \text{ M}\Omega$$

and the output impedance is that of stage 2,

$$Z_o = R_D = 2.2 \text{ k}\Omega$$

## 8.16 TROUBLESHOOTING

As mentioned before, troubleshooting a circuit is a combination of knowing the theory and having experience using meters and an oscilloscope to check the operation of the circuit. A good troubleshooter has a sense for what to check based on the behavior of the networks. This ability is developed through building, testing, and repairing a wide

variety of configurations. For any small-signal amplifier one might consider the following steps:

1. Look at the circuit board to see if any obvious problems can be seen: an area charred by excess heating of a component; a component that feels or seems too hot to touch; what appears to be a poor solder joint; any connection that appears to have come loose.
2. Use a dc meter: make some measurements as marked in a repair manual containing the circuit schematic diagram and a listing of test dc voltages.
3. Apply a test ac signal: measure the ac voltages starting at the input and work along toward the output.
4. If the problem is identified at a particular stage, the ac signal at various points should be checked using an oscilloscope to see the waveform, its polarity, amplitude, and frequency, as well as any unusual waveform “glitches” that may be present. In particular, observe that the signal is present for the full signal cycle.

### Possible Symptoms and Actions

In the absence of an output ac voltage:

1. Check whether the supply voltage is properly connected.
2. Check whether the output voltage at  $V_D$  is in the midrange between 0 V and  $V_{DD}$ .
3. Check whether there is any input ac signal at the gate terminal.
4. Check the ac voltage at each side of the coupling capacitor terminals.

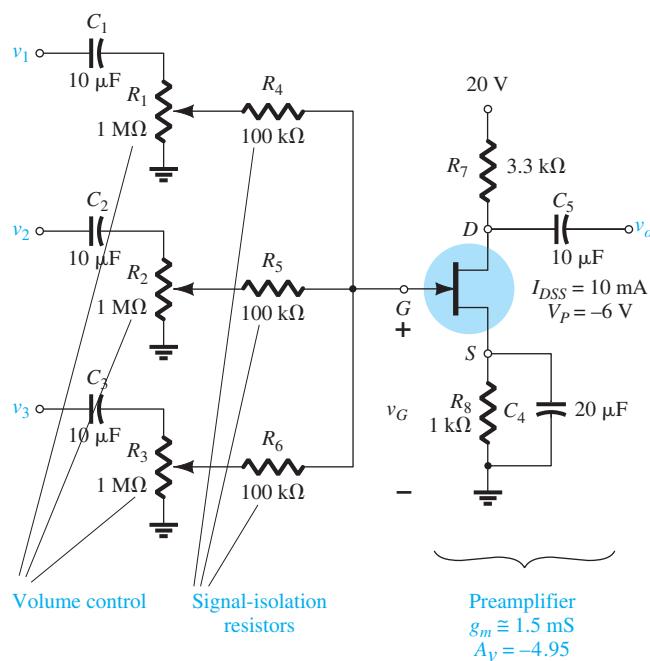
When building and testing an FET amplifier circuit in the laboratory:

1. Check the color code of resistor values to be sure that they are correct. Even better, measure the resistor values because components used repeatedly may get overheated when used incorrectly, causing the nominal value to change.
2. Check that all dc voltages are present at the component terminals. Be sure that all ground connections are made common.
3. Measure the ac input signal to be sure the expected value is provided to the circuit.

## 8.17 PRACTICAL APPLICATIONS

### Three-Channel Audio Mixer

The basic components of a three-channel JFET audio mixer are shown in Fig. 8.50. The three input signals can come from different sources such as a microphone, a musical instrument, background sound generators, and so on. All signals can be applied to the same gate terminal because the input impedance of the JFET is so high that it can be approximated by

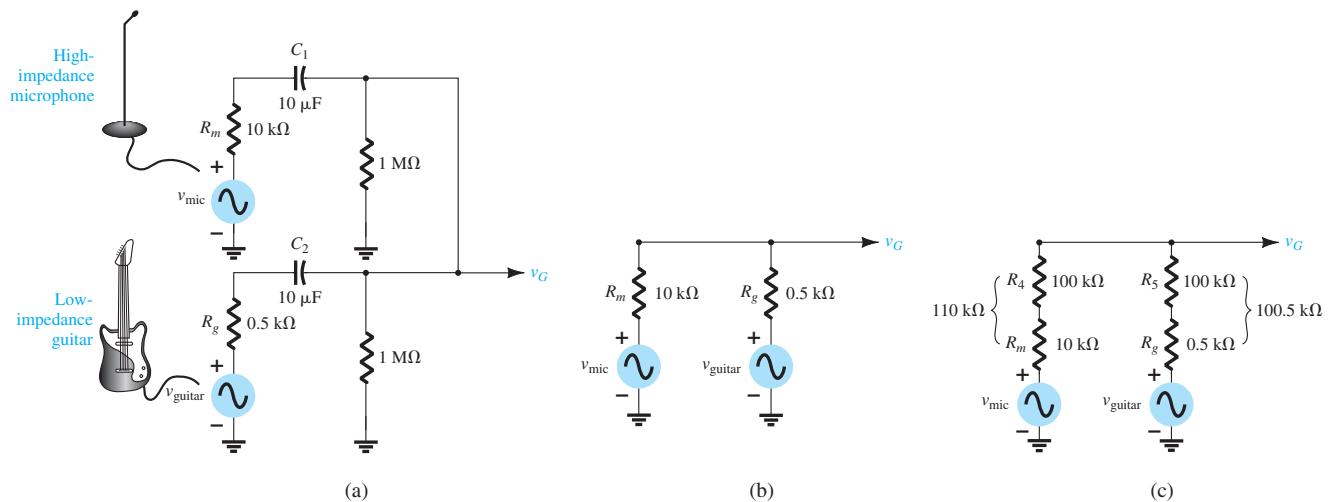


**FIG. 8.50**  
Basic components of a three-channel JFET audio mixer.

an open circuit. In general, the input impedance is  $1000 \text{ M}\Omega$  ( $10^9 \Omega$ ) or better for JFETs and  $100 \text{ million M}\Omega$  ( $10^{14} \Omega$ ) or better for MOSFETs. If BJTs were employed instead of JFETs, the lower input impedance would require a transistor amplifier for each channel or at least an emitter-follower as the first stage to provide a higher input impedance.

The  $10-\mu\text{F}$  capacitors are there to prevent any dc biasing levels on the input signal from appearing at the gate of the JFET, and the  $1-\text{M}\Omega$  potentiometers are the volume controls for each channel. The need for the  $100-\text{k}\Omega$  resistors for each channel is less obvious. Their purpose is to ensure that one channel does not load down the other channels and severely reduce or distort the signal at the gate. For instance, in Fig. 8.51a, one channel has a high-impedance ( $10-\text{k}\Omega$ ) microphone, whereas another channel has a low-impedance ( $0.5-\text{k}\Omega$ ) guitar amplifier. Channel 3 is left open, and the  $100-\text{k}\Omega$  isolation resistors have been removed for the moment. Replacing the capacitors by their short-circuit equivalent for the frequency range of interest and ignoring the effects of the parallel  $1-\text{M}\Omega$  potentiometers (set at their maximum value) result in the equivalent circuit of Fig. 8.51b at the gate of the JFET amplifier. Using the superposition theorem, we determine the voltage at the gate of the JFET by

$$\begin{aligned} v_G &= \frac{0.5 \text{ k}\Omega(v_{\text{mic}})}{10.5 \text{ k}\Omega} + \frac{10 \text{ k}\Omega(v_{\text{guitar}})}{10.5 \text{ k}\Omega} \\ &= 0.047v_{\text{mic}} + 0.95v_{\text{guitar}} \approx v_{\text{guitar}} \end{aligned}$$



(a) Application of a high- and a low-impedance source to the mixer of Fig. 8.50; (b) reduced equivalent without the  $100-\text{k}\Omega$  isolation resistors; (c) reduced equivalent with the  $100-\text{k}\Omega$  resistors.

clearly showing that the guitar has swamped the signal of the microphone. The only response of the amplifier of Fig. 8.51 will be to the guitar. Now, with the  $100-\text{k}\Omega$  resistors in place, the situation of Fig. 8.51c results. Using the superposition theorem again, we obtain the following equation for the voltage at the gate:

$$\begin{aligned} v_G &= \frac{101 \text{ k}\Omega(v_{\text{mic}})}{211 \text{ k}\Omega} + \frac{110 \text{ k}\Omega(v_{\text{guitar}})}{211 \text{ k}\Omega} \\ &\approx 0.48v_{\text{mic}} + 0.52v_{\text{guitar}} \end{aligned}$$

showing an even balance in the signals at the gate of the JFET. In general, therefore, the **100-kΩ resistors compensate for any difference in signal impedance to ensure that one does not load down the other and develop a mixed level of signals at the amplifier. Technically, they are often called “signal isolation resistors.”**

An interesting consequence of a situation such as described in Fig. 8.51b is depicted in Fig. 8.52, where a guitar of low impedance has a signal level of about  $150 \text{ mV}$ , whereas the microphone, having a larger internal impedance, has a signal strength of only  $50 \text{ mV}$ . As pointed out above, the major part of the signal at the “feed” point ( $v_G$ ) is that of the guitar. The resulting direction of current and power flow is unquestionably from the guitar to the microphone. Furthermore, since the basic construction of a microphone and a speaker is quite similar, the microphone may be forced to act like a speaker and broadcast the guitar signal. New acoustic bands often face this problem as they learn the rudiments of

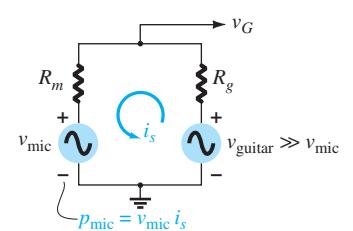


FIG. 8.52

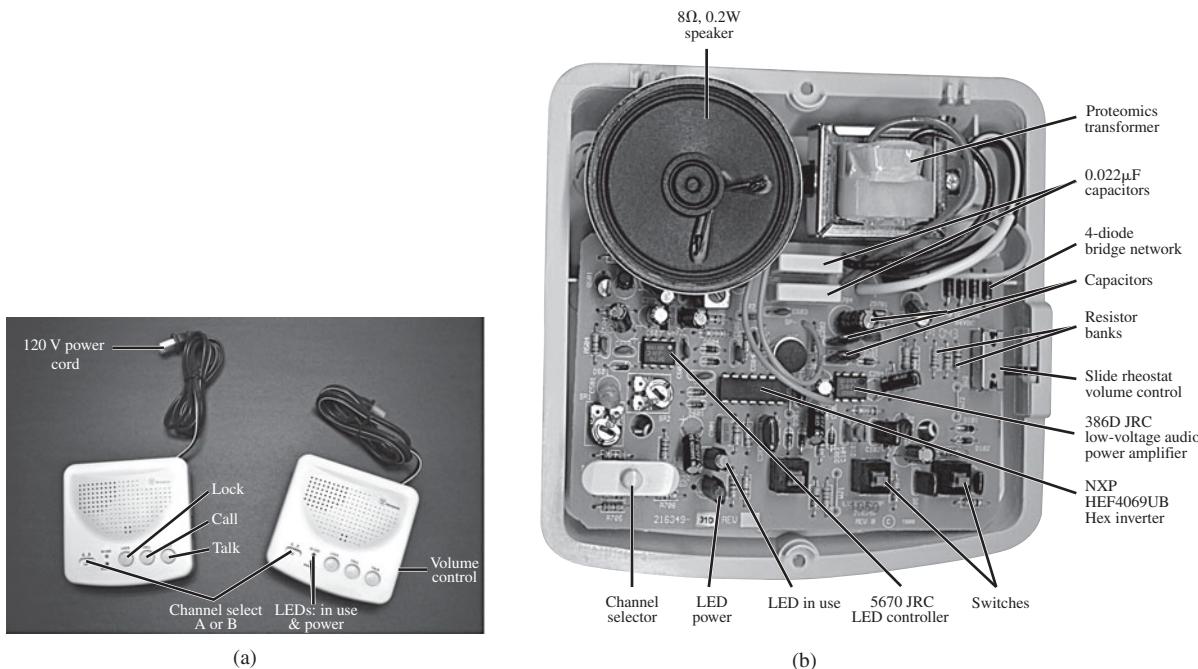
Demonstrating that for parallel signals, the channel with the least internal impedance and most power controls the situation.

good amplifier basics. In general, for parallel signals, the channel with the least internal impedance controls the situation.

In Fig. 8.50, the gain of the self-biased JFET is determined by  $-g_m R_D$ , which for this situation is

$$-g_m R_D = (-1.5 \text{ mS})(3.3 \text{ k}\Omega) = -4.95$$

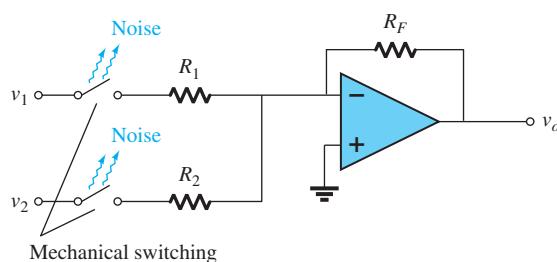
For some it may come as quite a surprise that a microphone can actually behave like a speaker. However, the classical example of the use of one voice cone to act as a microphone and a speaker is in the typical intercom system such as appearing in Fig. 8.53a. The 8 Ω, 0.2 W speaker of Fig. 8.53b can be used as a microphone or a speaker, depending on the position of the activation switch. It is important to note, however, as in the microphone–guitar example above, that most speakers are designed to handle reasonable power levels, but most microphones are designed to simply accept the voice-activated input, and they cannot handle the power levels normally associated with speakers. Just compare the size of each in any audio system. In general, a situation such as described above, where the guitar signal is heard over the microphone, will ultimately damage the microphone. For an intercom system the speaker is designed to handle both types of excitation without difficulty.



**FIG. 8.53**  
Two-station, two channel intercom: (a) external appearance; (b) internal construction.  
(Photos by Dan Trudden/Pearson).

### Silent Switching

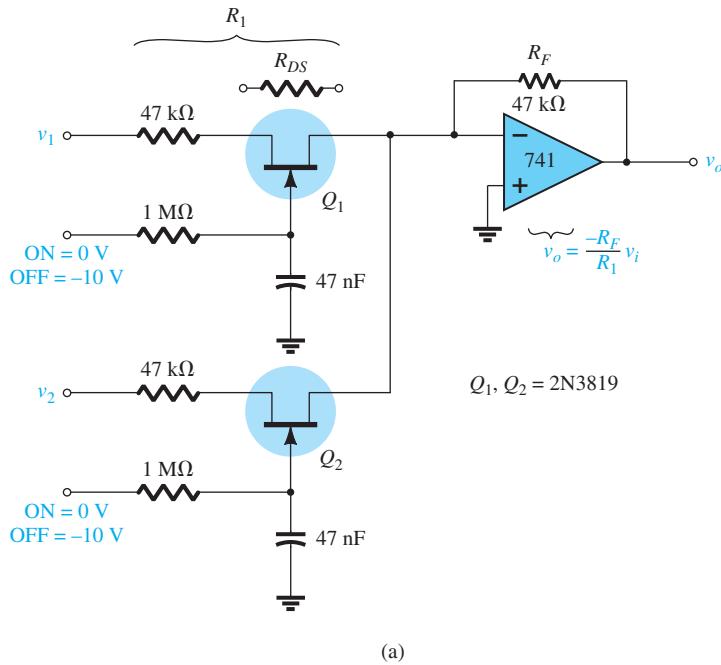
Any electronic system that incorporates mechanical switching such as shown in Fig. 8.54 is prone to developing noise on the line that will reduce the signal-to-noise ratio. When the switch of Fig. 8.54 is opened and closed, one often gets an annoying “pfft, pfft” sound as part of the output signal. In addition, the longer wires normally associated with



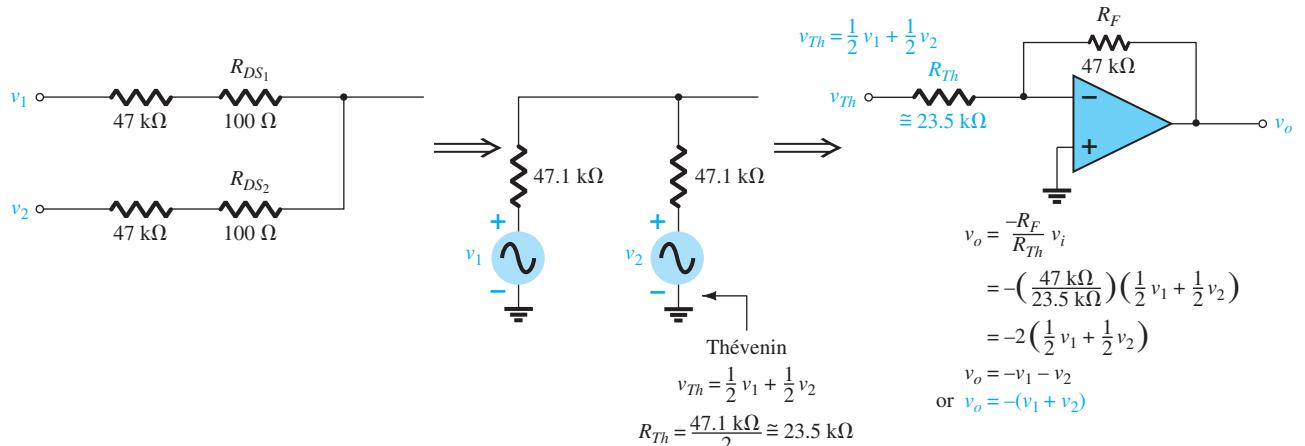
**FIG. 8.54**  
Noise development due to mechanical switching.

mechanical switches will require that the switch be as close to the amplifier as possible to reduce the noise pickup on the line.

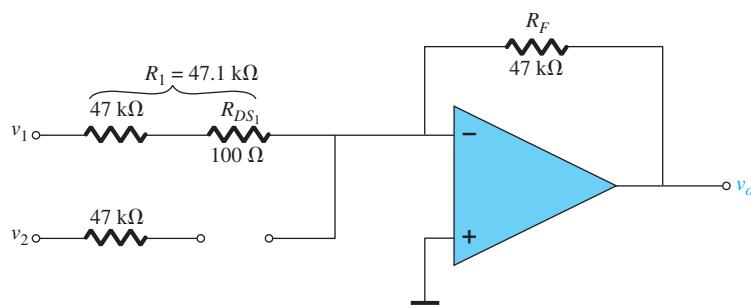
**One effective method to essentially eliminate this source of noise is to use electronic switching such as shown in Fig. 8.55a for a two-channel mixing network. Recall from Chapter 7 that the drain to source of a JFET for low values of  $V_{DS}$  can be looked on as a**



(a)



(b)



(c)

**FIG. 8.55**

Silent switching audio network: (a) JFET configuration; (b) with both signals present; (c) with one signal on.

resistance whose value is determined by the applied gate-to-source voltage as described in detail in Section 7.13. In addition, recall that the resistance is the least at  $V_{GS} = 0$  V and the highest near pinch-off. In Fig. 8.55a, the signals to be mixed are applied to the drain side of each JFET, and the dc control is connected directly to the gate terminal of each JFET. With 0 V at each control terminal, both JFETs are heavily “on,” and the resistance from  $D_1$  to  $S_1$  and from  $D_2$  to  $S_2$  is relatively small, say,  $100\ \Omega$  for this discussion. Although  $100\ \Omega$  is not the  $0\ \Omega$  assumed with an ideal switch, it is so small compared to the series  $47\text{-k}\Omega$  resistor that it can often be ignored. Both switches are therefore in the “on” position, and both input signals can make their way to the input of the inverting amplifier (to be introduced in Chapter 10) as shown in Fig. 8.55b. In particular, note that the chosen resistor values result in an output signal that is simply an inversion of the sum of the two signals. The amplifier stage to follow will then raise the summation to audio levels.

Both electronic switches can be put in the “off” state by applying a voltage that is more negative than the pinch-off level as indicated by the 10 V in Fig. 8.55a. The level of “off” resistance can approach  $10,000\text{ M}\Omega$ , which certainly can be approximated by an open circuit for most applications. Since both channels are isolated, one can be “on” while the other is “off.” The speed of operation of a JFET switch is controlled by the substrate (those due to the device construction) and stray capacitance levels and the low “on” resistance of the JFET. **Maximum speeds for JFETs are about 100 MHz, with 10 MHz being more typical.** However, this speed is critically reduced by the input resistance and capacitance of the design. In Fig. 8.55a, the  $1\text{-M}\Omega$  resistor and the  $47\text{-nF}$  capacitors have a time constant of  $\tau = RC = 47\text{ ms} = 0.047\text{ s}$  for the dc charging network that is controlling the voltage at the gate. If we assume two time constants to charge to the pinch-off level, the total time is  $0.094\text{ s}$ , or a switching speed of  $1/0.094\text{ s} \cong 10.6$  per second. Compared to the typical switching speed of the JFET at 10 million times in 1 s, this number is extremely small. Keep in mind, however, that the application is the important consideration, and for a typical mixer, switching is not going to occur at speeds greater than 10.6 per second unless we have some radical input signals. One might ask why it is necessary to have the  $RC$  time constant at the gate at all. Why not let the applied dc level at the gate simply control the state of the JFET? In general, the  $RC$  time constant ensures that the control signal is not a spurious one generated by noise or “ringing” due to the sharply rising and falling applied pulses at the gate. By using a charging network, we ensure that the dc level must be present for a period of time before the pinch-off level is reached. Any spike on the line will not be present long enough to charge the capacitor and switch the state of the JFET.

It is important to realize that the JFET switch is a **bilateral switch**. That is, signals in the “on” state can pass through the drain–source region in either direction. This, of course, is the way ordinary mechanical switches work, which makes it that much easier to replace mechanical switch designs with electronic switches. Remember that the diode is not a bilateral switch because it can conduct current at low voltages in only one direction.

It should be noted that because the state of the JFETs can be controlled by a dc level, the design of Fig. 8.55a lends itself to remote and computer control for the same reasons described in Chapter 7 when dc control was discussed.

The data sheet for a low-cost JFET analog switch is provided in Fig. 8.56. Note under the heading Drain Cutoff Current that the pinch-off voltage  $V_{GS} = V_P$  is typically about  $-10\text{ V}$  at a drain-to-source voltage of  $12\text{ V}$ . In addition, a current level of  $10\text{ nA}$  is used to define the pinch-off level. The level of  $I_{DSS}$  is  $15\text{ mA}$ , whereas the drain-to-source resistance is quite low at  $150\ \Omega$  with  $V_{GS} = 0\text{ V}$ . The turn-on time is quite small at  $10\text{ ns}$  ( $t_d + t_r$ ), whereas the turn-off time is  $25\text{ ns}$ .

## Phase-Shift Networks

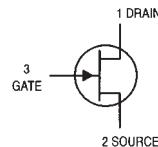
Using the voltage-controlled drain-to-source resistance characteristic of a JFET, we can control the phase angle of a signal using the configurations of Fig. 8.57. The network of Fig. 8.57a is a phase-advance network, which adds an angle to the applied signal, whereas the network of Fig. 8.57b is a phase-retard configuration, which creates a negative phase shift.

## JFET Switching

### N-Channel — Depletion

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	25	Vdc
Drain-Gate Voltage	$V_{DG}$	25	Vdc
Gate-Source Voltage	$V_{GS}$	25	Vdc
Forward Gate Current	$I_{GF}$	10	mAdc
Total Device Dissipation @ $T_c = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	350 2.8	mW mW/ $^\circ\text{C}$
Junction Temperature Range	$T_J$	-65 to +150	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Gate-Source Breakdown Voltage ( $I_G = 10 \mu\text{Adc}, V_{DS} = 0$ )	$V_{(BR)GSS}$	25	—	Vdc
Gate Reverse Current ( $V_{GS} = 15 \text{ Vdc}, V_{DS} = 0$ )	$I_{GSS}$	—	1.0	nAdc
Drain Cutoff Current ( $V_{DS} = 12 \text{ Vdc}, V_{GS} = -10 \text{ V}$ ) ( $V_{DS} = 12 \text{ Vdc}, V_{GS} = -10 \text{ V}, T_A = 100^\circ\text{C}$ )	$I_{D(off)}$	—	10 2.0	nAdc $\mu\text{Adc}$

## ON CHARACTERISTICS

Zero-Gate-Voltage Drain Current <sup>(1)</sup> ( $V_{DS} = 15 \text{ Vdc}, V_{GS} = 0$ )	$I_{DSS}$	15	—	mAdc
Gate-Source Forward Voltage ( $I_{Gf} = 1.0 \text{ mAdc}, V_{DS} = 0$ )	$V_{GS(f)}$	—	1.0	Vdc
Drain-Source On-Voltage ( $I_D = 7.0 \text{ mAdc}, V_{GS} = 0$ )	$V_{DS(on)}$	—	1.5	Vdc
Static Drain-Source On Resistance ( $I_D = 0.1 \text{ mAdc}, V_{GS} = 0$ )	$r_{DS(on)}$	—	150	Ohms

1. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty Cycle < 3.0%.

Characteristic	Symbol	Min	Max	Unit
<b>SMALL-SIGNAL CHARACTERISTICS</b>				
Small-Signal Drain-Source "ON" Resistance ( $V_{GS} = 0, I_D = 0, f = 1.0 \text{ kHz}$ )	$r_{ds(on)}$	—	150	Ohms
Input Capacitance ( $V_{DS} = 15 \text{ Vdc}, V_{GS} = 0, f = 1.0 \text{ MHz}$ )	$C_{iss}$	—	5.0	pF
Reverse Transfer Capacitance ( $V_{DS} = 0, V_{GS} = 10 \text{ Vdc}, f = 1.0 \text{ MHz}$ )	$C_{rss}$	—	1.2	pF

## SWITCHING CHARACTERISTICS

Turn-On Delay Time	( $V_{DD} = 10 \text{ Vdc}, I_D(on) = 7.0 \text{ mAdc}, V_{GS(on)} = 0, V_{GS(off)} = -10 \text{ Vdc}$ )	$t_{d(on)}$	—	5.0	ns
Rise Time		$t_r$	—	5.0	ns
Turn-Off Delay Time	( $V_{DD} = 10 \text{ Vdc}, I_D(on) = 7.0 \text{ mAdc}, V_{GS(on)} = 0, V_{GS(off)} = -10 \text{ Vdc}$ )	$t_{d(off)}$	—	15	ns
Fall Time		$t_f$	—	10	ns

FIG. 8.56

Specification sheet for a low-cost analog JFET current switch.  
(Copyright of Semiconductor Components Industries, LLC. Used by permission.)

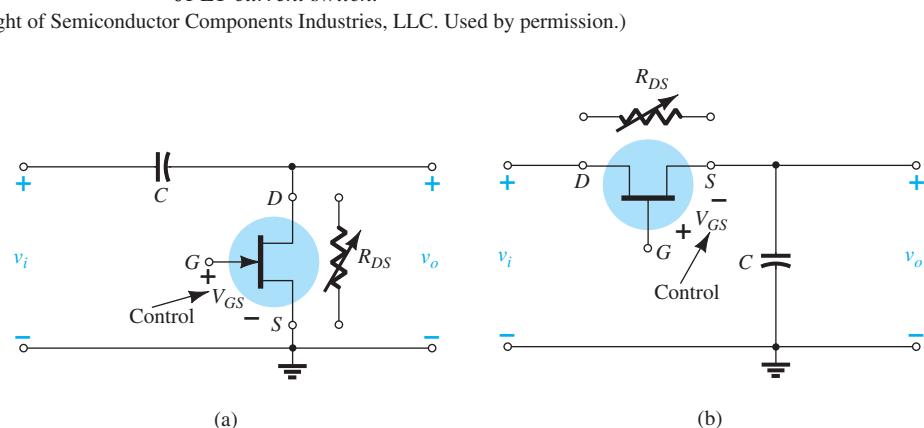


FIG. 8.57

Phase-shift networks: (a) advance; (b) retard.

For example, let us consider the effect of  $R_{DS}$  on an input signal having a frequency such as 10 kHz if we apply it to the network of Fig. 8.57a. For discussion, let us assume that the drain-to-source resistance is  $2 \text{ k}\Omega$  due to an applied gate-to-source voltage of  $-3 \text{ V}$ . Drawing the equivalent network results in the general configuration of Fig. 8.58. Solving for the output voltage results in

$$\begin{aligned} V_o &= \frac{R_{DS}\angle 0^\circ V_i\angle 0^\circ}{R_{DS} - jX_C} = \frac{R_{DS}V_i\angle 0^\circ}{\sqrt{R_{DS}^2 + X_C^2} - \tan^{-1}\frac{X_C}{R_{DS}}} \\ &= \frac{R_{DS}V_i}{\sqrt{R_{DS}^2 + X_C^2}}\angle \tan^{-1}\frac{X_C}{R_{DS}} = \left(\frac{R_{DS}}{\sqrt{R_{DS}^2 + X_C^2}}\right)V_i\angle \tan^{-1}\frac{X_C}{R_{DS}} \end{aligned}$$

so that

$$V_o = k_1 V_i \angle \theta_1$$

where

$$k_1 = \frac{R_{DS}}{\sqrt{R_{DS}^2 + X_C^2}} \quad \text{and} \quad \theta_1 = \tan^{-1}\frac{X_C}{R_{DS}} \quad (8.69)$$

Substituting the numerical values from above results in

$$X_C = \frac{1}{2\pi f C} = \frac{1}{2\pi(10 \text{ kHz})(0.01 \mu\text{F})} = 1.592 \text{ k}\Omega$$

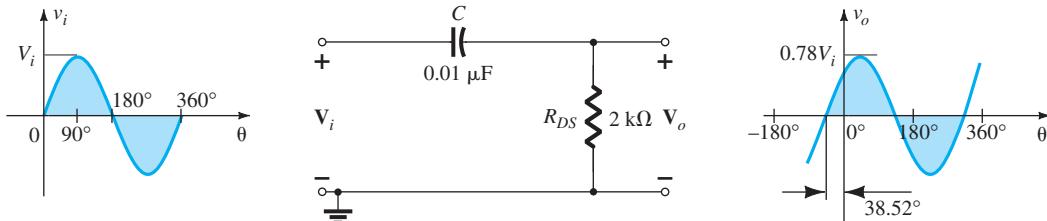
$$\text{and} \quad k_1 = \frac{R_{DS}}{\sqrt{R_{DS}^2 + X_C^2}} = \frac{2 \text{ k}\Omega}{\sqrt{(2 \text{ k}\Omega)^2 + (1.592 \text{ k}\Omega)^2}} = 0.782$$

$$\text{with} \quad \theta_1 = \tan^{-1}\frac{X_C}{R_{DS}} = \tan^{-1}\frac{1.592 \text{ k}\Omega}{2 \text{ k}\Omega} = \tan^{-1} 0.796 = 38.52^\circ$$

so that

$$V_o = 0.782V_i \angle 38.52^\circ$$

and an output signal that is 78.2% of its applied signal but with a phase shift of  $38.52^\circ$ .



**FIG. 8.58**  
RC phase-advance network.

In general, therefore, the network of Fig. 8.57a can introduce a positive phase shift extending from a few degrees (with  $X_C$  relatively small compared to  $R_{DS}$ ) to almost  $90^\circ$  (with  $X_C$  relatively large compared to  $R_{DS}$ ). Keep in mind, however, that for fixed values of  $R_{DS}$ , as the frequency increases,  $X_C$  will decrease and the phase shift will approach  $0^\circ$ . For decreasing frequencies and a fixed  $R_{DS}$ , the phase shift will approach  $90^\circ$ . It is also important to realize that for a fixed  $R_{DS}$ , an increasing level of  $X_C$  results in diminishing magnitude for  $V_o$ . For such a network, a balance between gain and desired phase shift will have to be made.

For the network of Fig. 8.57b, the resulting equation is

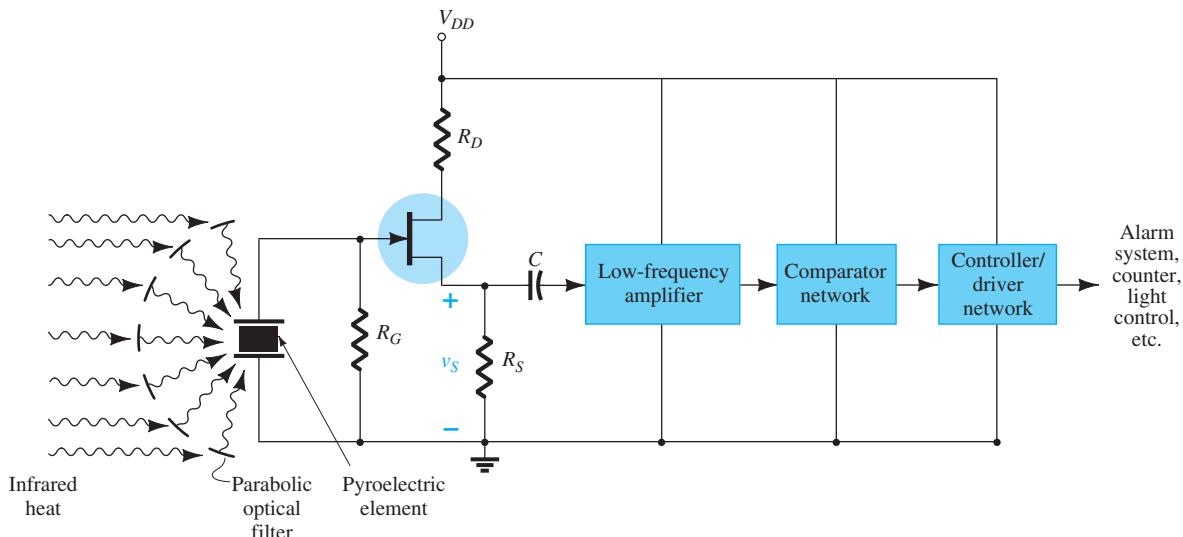
$$V_o = k_2 V_i \angle \theta_2 \quad (8.70)$$

where

$$k_2 = \frac{X_C}{\sqrt{R_{DS}^2 + X_C^2}} \quad \text{and} \quad \theta_2 = -\tan^{-1}\frac{R_{DS}}{X_C}$$

## Motion-Detection System

The basic components of a passive infrared (PIR) motion-detection system are shown in Fig. 8.59. The heart of the system is the **pyroelectric detector**, which generates a voltage that varies with the amount of incident heat. It filters out all but the infrared radiation from a particular area and focuses the energy onto a temperature-sensing element. Recall from Chapter 7, Section 7.13, that the infrared band is a nonvisible band just below the visible light spectrum. **Passive detectors do not emit a signal of any kind but simply respond to the energy flow of the environment.**



**FIG. 8.59**  
*Passive infrared (PIR) motion-detection system.*

An external and an internal view of a commercially available unit are provided in Fig. 8.60a and b, respectively. Four interchangeable lens are provided for different coverage areas. For our purposes the “pet” option was selected with the coverage indicated in Fig. 8.60c. The unit is mounted at a height of 7'6" and operates at a dc voltage of 8.5 V to 15.4 V, drawing a current of 17 mA at 12 V dc. The range of coverage is 35' perpendicular to the sensor and 20' to each side. In the lowest sensitivity setting the combined weight of the animals cannot exceed 80 lbs.

To focus the incident ambient heat on the pyroelectric detector, the unit of Fig. 8.60 uses a parabolic deflector. As a person walks past a sensor, he or she will cut the various fields appearing in Fig. 8.60c, and the detector will sense the **rapid changes** in heat level. **The result is a changing dc level akin to a low-frequency ac signal of relatively high internal impedance appearing at the gate of the JFET.** One might then ask why turning a heating system on or turning on a lamp doesn’t generate an alarm signal since heat will be generated. The answer is that both will generate a voltage at the detector that grows steadily with increasing heat level from the heating system or the burning bulb. Remember that for the lamp, the detector is heat sensitive and not light sensitive. The resulting voltage is not oscillating between levels, but simply climbing in level and will not set off the alarm—a varying ac voltage will not be generated by the pyroelectric detector!

Note in Fig. 8.59 that a JFET source-follower configuration was employed to ensure a very high input impedance to capture most of the pyroelectric signal. It is then passed through a low-frequency amplifier, followed by a peak-detecting network and a comparator to determine whether the alarm should be set off. The dc voltage comparator is a network that “captures” the peak value of the generated ac voltage and compares it to a known dc voltage level. The output processor determines whether the difference between the two levels is sufficient to tell the driver to energize the alarm.

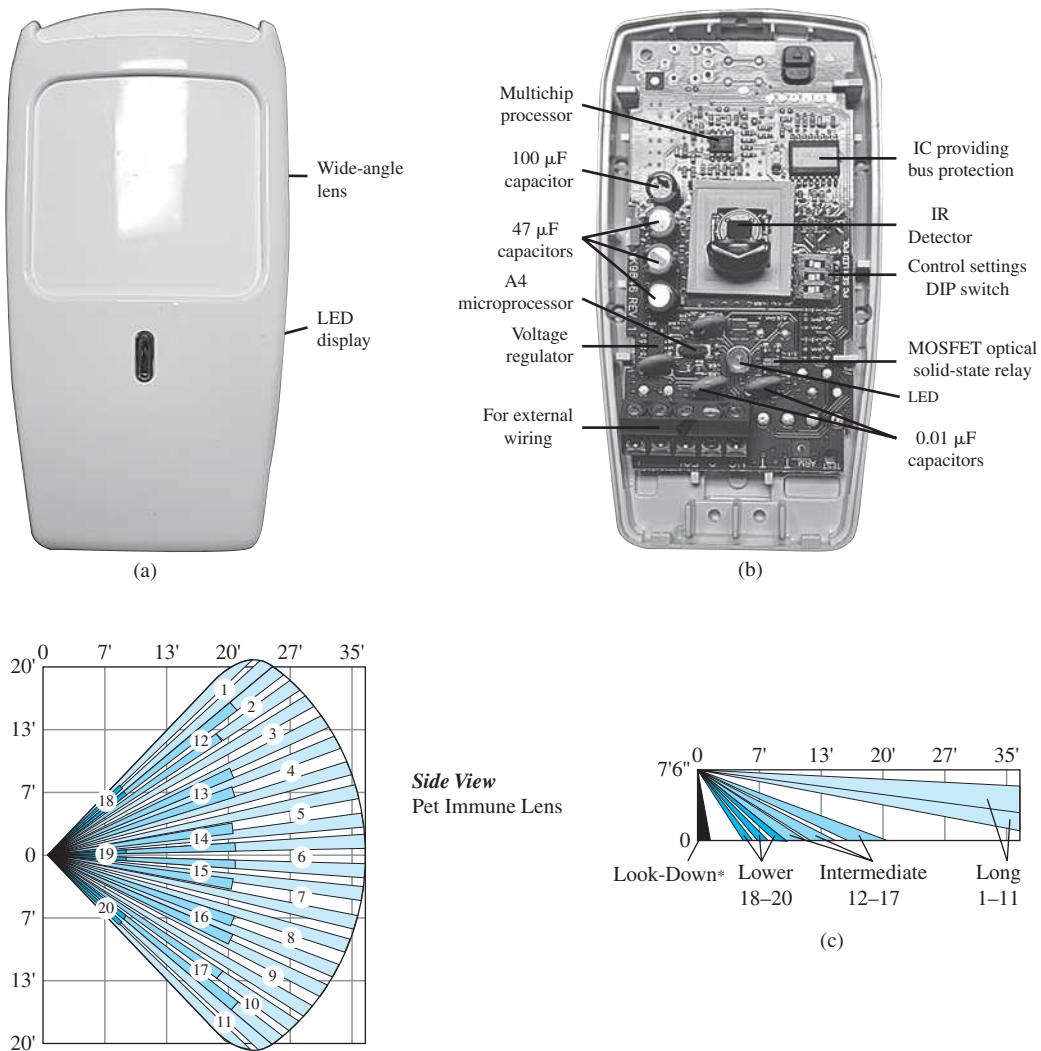


FIG. 8.60

Commercially available PIR motion-detection unit: (a) external appearance; (b) internal construction; (c) pet option coverage.  
[Photos (a) and (b) by Dan Trudden/Pearson.]

## 8.18 SUMMARY

### Important Conclusions and Concepts

1. The transconductance parameter  $g_m$  is determined by the ratio of the change in drain current associated with a particular change in gate-to-source voltage in the region of interest. The steeper the slope of the  $I_D$ -versus- $V_{GS}$  curve, the greater is the level of  $g_m$ . In addition, the closer the point or region of interest to the saturation current  $I_{DSS}$ , the greater is the transconductance parameter.
2. On specification sheets,  $g_m$  is provided as  $y_{fs}$ .
3. When  $V_{GS}$  is one-half the pinch-off value,  $g_m$  is one-half the maximum value.
4. When  $I_D$  is one-fourth the saturation level of  $I_{DSS}$ ,  $g_m$  is one-half the value at saturation.
5. The output impedance of FETs is similar in magnitude to that of conventional BJTs.
6. On specification sheets the output impedance  $r_d$  is provided as  $1/y_{os}$ . The more horizontal the characteristic curves on the drain characteristics, the greater is the output impedance.

7. The **voltage gain** for the fixed-bias and self-bias JFET configurations (with a bypassed source capacitance) **is the same**.
8. The **ac analysis** of JFETs and depletion-type MOSFETs **is the same**.
9. The **ac equivalent network** for an enhancement-type MOSFET **is the same** as that employed for JFETs and depletion-type MOSFETs. The only difference is the equation for  $g_m$ .
10. The **magnitude of the gain** of FET networks is typically **between 2 and 20**. The **self-bias configuration** (without a bypass source capacitance) and the **source-follower** are **low-gain configurations**.
11. There is **no phase shift** between input and output for the **source-follower** and **common-gate configurations**. Most others have a  $180^\circ$  phase shift.
12. The **output impedance** for most FET configurations is **determined primarily by  $R_D$** . For the **source-follower** configuration it is determined by  $R_S$  and  $g_m$ .
13. The **input impedance** for most FET configurations is **quite high**. However, it is **quite low** for the **common-gate configuration**.
14. When **troubleshooting any electronic or mechanical system**, always check the **most obvious causes first**.

## Equations

$$g_m = y_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}$$

$$g_{m0} = \frac{2I_{DSS}}{|V_P|}$$

$$g_m = g_{m0} \left[ 1 - \frac{V_{GS}}{V_P} \right]$$

$$g_m = g_{m0} \sqrt{\frac{I_D}{I_{DSS}}}$$

$$r_d = \frac{1}{y_{os}} = \frac{\Delta V_{DS}}{\Delta I_D} \Big|_{V_{GS}=\text{constant}}$$

For JFET and depletion-type MOSFET configurations, see Tables 8.1 and 8.2.

## 8.19 COMPUTER ANALYSIS

### PSpice Windows

**JFET Fixed-Bias Configuration** The first JFET configuration to be analyzed in the ac domain will be the fixed-bias configuration of Fig. 8.61, using a JFET with  $V_P = -4$  V and  $I_{DSS} = 10$  mA. The  $10\text{-M}\Omega$  resistor was added to act as a path to ground for the capacitor but is essentially an open circuit for the ac analysis. The **J2N3819** *n*-channel JFET from the **EVAL** library was used, and the ac voltage is to be determined at four different points for comparison and review.

The constant **Beta** is determined by

$$\text{Beta} = \frac{I_{DSS}}{|V_P|^2} = \frac{10 \text{ mA}}{4^2 \text{ V}^2} = 0.625 \text{ mA/V}^2$$

and is inserted in the **Edit Model** dialog box obtained by the sequence **EDIT-PROPERTIES**. **V<sub>t0</sub>** is also changed to  $-4$  V. The remaining elements of the network are set as described for the transistor in Chapter 5.

An analysis of the network results in the printout of Fig. 8.62. The **CIRCUIT DESCRIPTION** includes all the elements of the network along with their assigned nodes. In particular, note that **Vi** is set at **10 mV** at a frequency of **10 kHz** and a phase angle of **0**

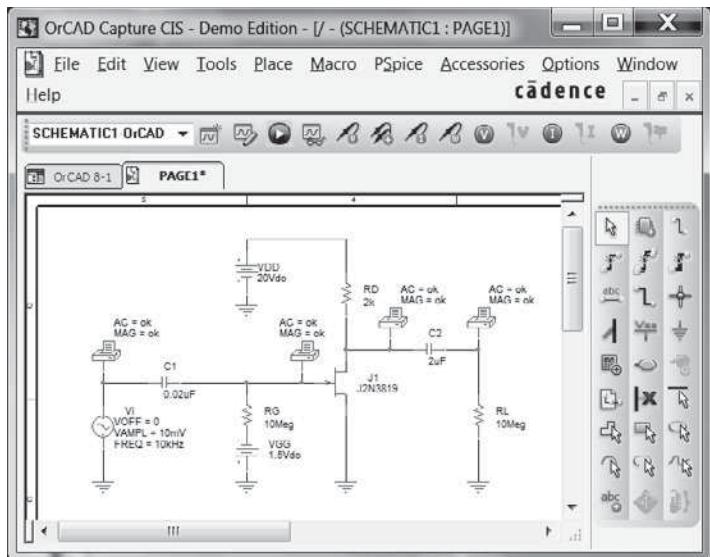


FIG. 8.61

Fixed-bias JFET configuration with an ac source.

```
*****
CIRCUIT DESCRIPTION
*****
*Analysis directives:
.AC LIN 1 10kHz 10kHz
.OP
.PROBE V(alias(*)) I(alias(*)) W(alias(*)) D(alias(*)) NOISE(alias(*))
INC ".SCHEMATIC1.net"
**** INCLUDING SCHEMATIC1.net ****
* source ORCAD 8-1
V_Vi N00344 0 AC 10mV
+SIN 0 10mV 10kHz 0 0 0
C_C1 N00344 N00351 0.02uF TC=0.0
C_C2 N00315 N00321 2uF TC=0.0
R_RG N00358 N00351 10Meg TC=0.0
R_RD N00315 N00303 2k TC=0.0
R_RL 0 N00326 10Meg TC=0.0
V_VDD N00303 0 20Vdc
V_VGG 0 N00358 1.5Vdc
J_J1 N00315 N00351 0 J2N3819
.PRINT AC
+VM(N00344)
.PRINT AC
+VM(N00351)
.PRINT AC
+VM(N00315)
.PRINT AC
+VM(N00326)
.END

*****
Junction FET MODEL PARAMETERS
*****
J2N3819
NJF
VTO -4
BETA 625.000000E-06
LAMBDAB 2.250000E-03
IS 33.570000E-15
ISR 322.400000E-15
ALPHA 311.700000E-06
VK 243.6
RD 1
RS 1
CGD 1.600000E-12
CGS 2.414000E-12
M .3622
VTOTC -2.500000E-03
BETATCE -.5
KF 9.882000E-18

*****
SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C
*****
NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE
(N00303) 20.0000 (N00315) 12.0020 (N00326) 0.0000
(N00344) 0.0000 (N00351) -1.5000 (N00358) -1.5000

VOLTAGE SOURCE CURRENTS
NAME CURRENT
V_Vi 0.000E+00
V_VDD -3.999E-03
V_VGG -1.366E-12

*****
OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C
*****
JFETS
NAME J_J1
MODEL J2N3819
ID 4.00E-03
VGS -1.50E+00
VDS 1.20E+01
GM 3.20E-03
GDS 8.76E-06
CGS 1.73E-12
CGD 6.07E-13

*****
AC ANALYSIS TEMPERATURE = 27.000 DEG C
*****
FREQ VM(N00344)
1.000E+04 1.000E-02

FREQ VM(N00351)
1.000E+04 9.997E-03

FREQ VM(N00315)
1.000E+04 6.275E-02

FREQ VM(N00326)
1.000E+04 6.275E-02
```

FIG. 8.62

Output file for the network of Fig. 8.61.

degrees. In the following list of **Junction FET MODEL PARAMETERS** note that **VTO** is  $-4$  V and **BETA** is  $625E-6$  A/V $^2$  =  $0.625$  mA/V $^2$ , as entered earlier. The **SMALL SIGNAL BIAS SOLUTION** reveals that the voltage at both ends of  $R_G$  is  $-1.5$  V, resulting in  $V_{GS} = -1.5$  V. The voltage levels of this section can be related to the original network by simply noting the assigned node list in the **CIRCUIT DESCRIPTION**. The voltage from drain to source (ground) is  $12$  V, leaving a drop of  $8$  V across  $R_D$ . The **AC ANALYSIS** listing reveals that the voltage at the source (N01707) is  $10$  mV as set, but the voltage at the other end of the capacitor is  $3 \mu$ V less due to the impedance of the capacitor at  $10$  kHz—certainly a drop to be ignored. The choice of  $0.02 \mu$ F for this frequency was obviously a good one. The voltages before and after the capacitor on the output side are exactly the same (to three places), revealing that the larger the capacitor, the closer are the characteristics to those of a short circuit. The output of  $6.275E-2 = 62.75$  mV reflects a gain of  $6.275$ .

The **OPERATING POINT INFORMATION** reveals that  $I_D$  is 4 mA and  $g_m$  is 3.2 mS. We calculate the value of  $g_m$  from

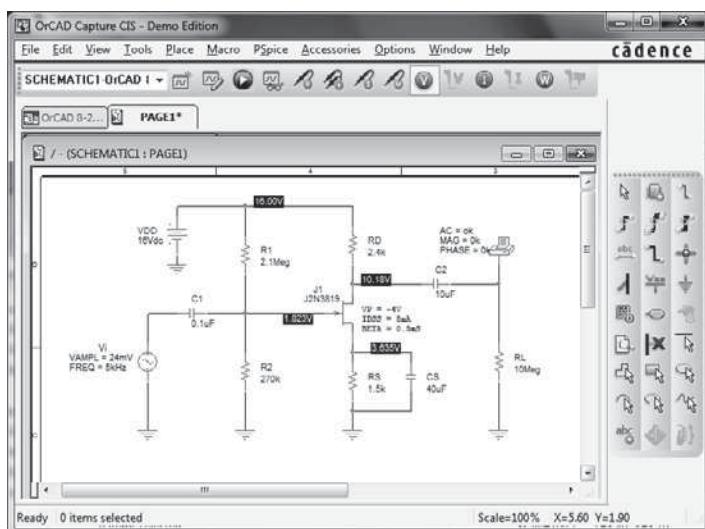
$$g_m = \frac{2I_{DSS}}{|V_P|} \left(1 - \frac{V_{GSQ}}{V_P}\right)$$

$$g_m = \frac{2(10 \text{ mA})}{4 \text{ V}} \left[1 - \frac{(-1.5 \text{ V})}{(-4 \text{ V})}\right]$$

$$= 3.125 \text{ mS}$$

which confirms our analysis.

**JFET Voltage-Divider Configuration** The next network to be analyzed in the ac domain is the voltage-divider bias configuration of Fig. 8.63. Note that the parameters chosen are different from those employed in earlier examples, with  $V_i$  at 24 mV and a frequency of 5 kHz. In addition, the dc levels are displayed, and a plot of the output and input voltages are displayed on the same screen.

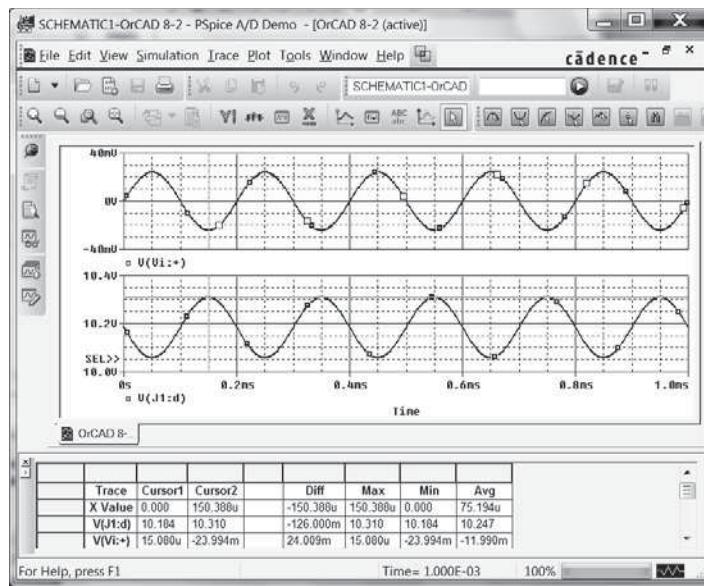


**FIG. 8.63**  
JFET voltage-divider configuration with an ac source.

To run the analysis, select the **New Simulation Profile** key to obtain the **New Simulation** dialog box. After entering **Name of OrCAD 8-2**, select **Create**, and the **Simulation Settings** dialog box will appear. Under **Analysis type**, select **AC/Sweep/Noise**, and then under **AC Sweep** choose **Linear**. The **Start Frequency** is **5 kHz**, the **End Frequency** is **5 kHz** and the **Total Points** is **1**. An **OK**, and the simulation can be initiated by selecting the **Run PSpice** key. A schematic will appear, which can be exited to result in the display of Fig. 8.63 with all the voltage levels displayed as controlled by the **V** option. The resulting dc levels reveal that  $V_{GS}$  is 1.823 V – 3.635 V = –1.812 V, comparing very well with the –1.8 V calculated in Example 7.4.  $V_D$  is 10.18 V, compared to the calculated level of 10.24 V, and  $V_{DS}$  is 10.18 V – 3.635 V = 6.545 V, compared to 6.64 V.

For the ac solution, we can select **View-Output File** and find under **OPERATING POINT INFORMATION** that  $g_m$  is 2.22 mS, comparing very well with the hand-calculated value of 2.2 mS, and under **AC ANALYSIS** that the output ac voltage is 125.8 mV, resulting in a gain of 125.8 mV/24 mV = 5.24. The hand-calculated level is  $g_m R_D = (2.2 \text{ mS})(2.4 \text{ k}\Omega) = 5.28$ .

The ac waveform for the output voltage can be obtained by returning to the **Simulation Settings** dialog box and under **Analysis type** choosing **Time Domain (Transient)**. Then, since the period of a 5-kHz signal is 200  $\mu$ s, select a **Run to** time of 1 ms, so that five cycles of the waveform will appear. Leave the **Start saving data after** option at 0 s, and under **Transient options** enter a **Maximum step size** of 2  $\mu$ s, so that we have at least 100 plot points for each cycle of the waveform. An **OK**, and the **SCHEMATIC** screen will appear. Select **Trace-Add Trace-V(J1:d)** and the waveform at the bottom of Fig 8.64 appears. If you then choose

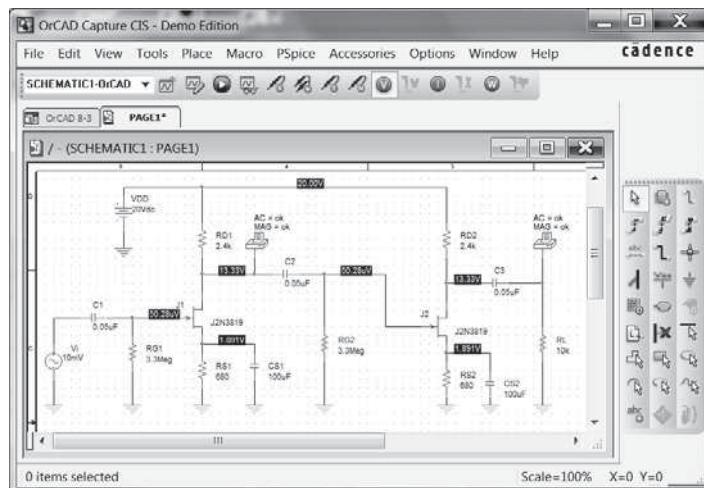


**FIG. 8.64**  
The ac drain and gate voltage for the voltage-divider JFET configuration of Fig. 8.63.

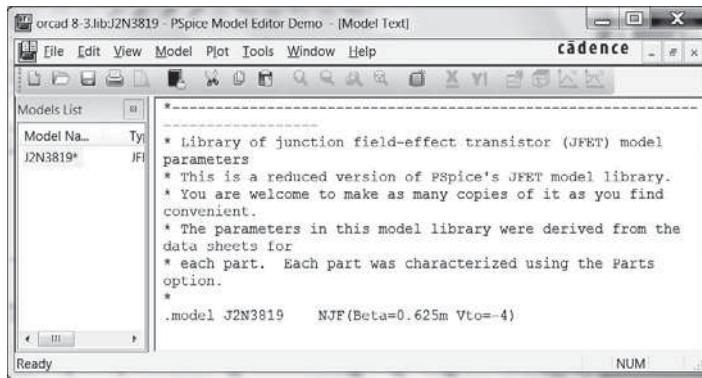
**Plot-Add Plot to Window-Trace-Add Trace-V(Vi:+)**, the waveform of the applied voltage appears at the top of Fig. 8.64. Now shift SEL >> to the bottom waveform by simply bringing the cursor down to the left of the other waveform and left clicking the mouse once. Now select **Trace-Cursor-Display**, and a horizontal line will appear at the dc level of the output voltage at 10.184 V (note the level of **V(J1:d)** in the **Probe Cursor** dialog box in the bottom right of the screen). A right click of the mouse, and a second set of intersecting lines will appear. Choose the **Cursor Peak** icon in the toolbar above the display, and the intersection will automatically go to the peak value of the waveform [(**V(Vi:+)** in the dialog box)]. Note that **Cursor 2** indicates that the peak value occurs at about 150  $\mu$ s and the instantaneous peak value is 10.31 V. The **Diff** is simply the difference between **Cursor 1** and **Cursor 2** intersections for time and amplitude.

**Cascaded JFET Amplifier** The extensive two-stage JFET amplifier of Fig. 8.65 can be created using the same procedures described in the previous examples using PSpice. For both JFETs, **Beta** was set at 0.625 mA/V<sup>2</sup> and **Vto** at -4 V as shown in Fig. 8.66. The applied frequency is 10 kHz to ensure that the capacitors take on a short-circuit approximation. The ac output at the output of each stage is requested.

After simulation, the output file of Fig. 8.67 results, revealing that the gain is 63.23 mV / 10 mV = 6.3 after the first stage and 322.6 mV / 10 mV = 32.3 after both stages. The gain



**FIG. 8.65**  
Design Center network for analyzing cascaded JFET amplifiers.



**FIG. 8.66**  
Display of resulting JFET model definition.

```
***** CIRCUIT DESCRIPTION
*****
*Libraries:
* Profile Libraries :
* Local Libraries :
.LIB ".../orcad 8-3-pspicefiles/orcad 8-3.lib"
* From [PSPIKE NETLIST] section of C:\OrCAD\OrCAD_16.3_Demo\tools\PSpice\PSpice.ini file:
.lib "nomd.lib"
*Analysis directives:
.AC LIN 1 10kHz 10kHz
.OP
.PROBE V(alias(*)) I(alias(*)) W(alias(*)) D(alias(*)) NOISE(alias(*))
.INC "...SCHEMATIC1.net"

**** INCLUDING SCHEMATIC1.net ****
* source ORCAD 8-3
J_J1 N00328 N00336 N00332 J2N3819
J_J2 N00340 N00416 N00344 J2N3819
V_VDD N00308 0 20Vdc
R_RD1 N00328 N00308 2.4k TC=0,0
R_RS1 0 N00332 680 TC=0,0
R_RG1 0 N00336 3.3Meg TC=0,0
R_RD2 N00340 N00308 2.4k TC=0,0
R_RS2 0 N00344 680 TC=0,0
R_RG2 0 N00416 3.3Meg TC=0,0
R_RL 0 N00361 10 TC=0,0
C_C1 N01393 N00336 0.05uF TC=0,0
C_C2 N00328 N00416 0.05uF TC=0,0
C_C3 N00340 N00361 0.05uF TC=0,0
C_CS1 0 N00332 100uF TC=0,0
C_CS2 0 N00344 100uF TC=0,0

.PRINT AC
+ VM([N00361])
.PRINT AC
+ VM([N00328])
V_Vi N01393 0 DC 0Vdc AC 10mV

**** RESUMING "OrCAD 8-3.cir" ****
.END

**** Junction FET MODEL PARAMETERS
*****
J2N3819
NJF
VTO -4
BETA 625.000000E-06

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C
*****
NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE
(N00308) 20.0000 (N00328) 13.3270 (N00332) 1.8908 (N00336) 50.28E-06
(N00340) 13.3270 (N00344) 1.8908 (N00361) 0.0000 (N00416) 50.28E-06
(N01393) 0.0000

VOLTAGE SOURCE CURRENTS
NAME CURRENT
V_VDD -5.561E-03
V_Vi 0.000E+00

**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C
*****
**** JFETS
NAME J_J1 J_J2
MODEL J2N3819 J2N3819
ID 2.78E-03 2.78E-03
VGS -1.89E+00 -1.89E+00
VDS 1.14E+01 1.14E+01
GM 2.64E-03 2.64E-03
GDS 0.00E+00 0.00E+00
CGS 0.00E+00 0.00E+00
CGD 0.00E+00 0.00E+00

**** AC ANALYSIS TEMPERATURE = 27.000 DEG C
*****
FREQ VM([N00361])
1.000E+04 3.226E-01

**** AC ANALYSIS TEMPERATURE = 27.000 DEG C
*****
FREQ VM([N00328])
1.000E+04 6.323E-02
```

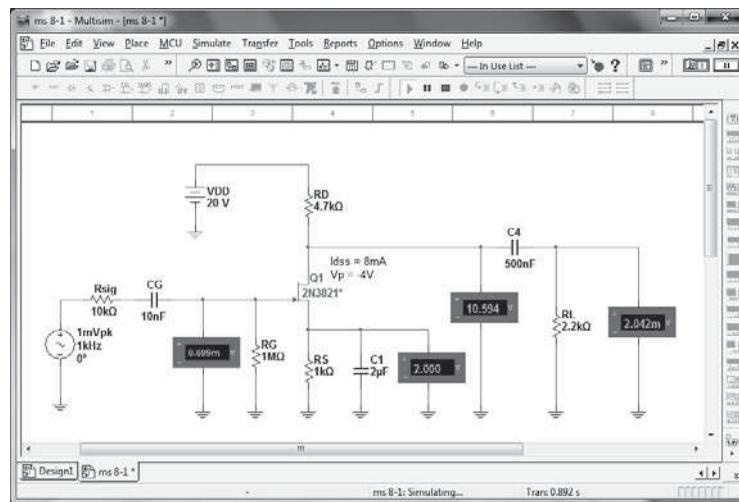
**FIG. 8.67**  
PSpice output for the network of Fig. 8.65.

for the second stage is  $322.6 \text{ mV} / 63.23 \text{ mV} = 5.1$ . The gains and output voltage are very close to the results obtained in Example 8.1.

In Fig. 8.67 the **V** option is selected to obtain the dc levels of the network. In particular, note how close the gate voltages are to 0 V, ensuring that the gate-to-source bias voltage is essentially the same as that across the source resistor. In fact, due to the isolation offered by the **C2** capacitor, the bias levels of each configuration are exactly the same.

## Multisim

The ac gain for the JFET self-bias network of Fig. 8.68 will now be determined using Multisim. The entire procedure for setting up the network and obtaining the desired readings was described for BJT ac networks in Chapter 5. This particular network will appear again



**FIG. 8.68**  
Analysis of a JFET self-bias network using Multisim.

in Chapter 9 as Fig. 9.70 when we turn our attention to the frequency response of a loaded JFET amplifier. A detailed analysis is provided in Chapter 9, including determining the dc levels, the value of  $g_m$ , and the loaded gain. The drain current of Example 9.12 is 2 mA, resulting in a drain voltage of 10.6 V and a source voltage of 2 V, which compare very well with the 10.594 V and 2.0 V respectively, of Fig. 8.68. When a load such as  $R_L$  is added to the network, it will appear in parallel with  $R_D$  of the network, changing the gain equation to  $-g_m R_D \parallel R_L$ . For Example 9.12,  $g_m$  is 2 mS, resulting in a gain  $V_o/V_i$  of  $(-2 \text{ mS}) (2.2 \text{ k}\Omega \parallel 4.7 \text{ k}\Omega) = -2.997$ . The meters of Fig. 8.68 provide the effective values of the voltages at those points. Since we used a power source, the reading of the meter XMM1 is very close to that of the applied source. The difference is due solely to the ac drop of voltage across  $R_{\text{sig}}$  and  $\text{CG}$ . The magnitude of the ac gain ( $V_o/V_i$ ) of the configuration is  $2.042 \text{ mV}/0.699 \text{ mV} = 2.921$ , which is very close to the hand-calculated solution.

## PROBLEMS

Note: Asterisks indicate more difficult questions.

### 8.2 FET Small-Signal Model

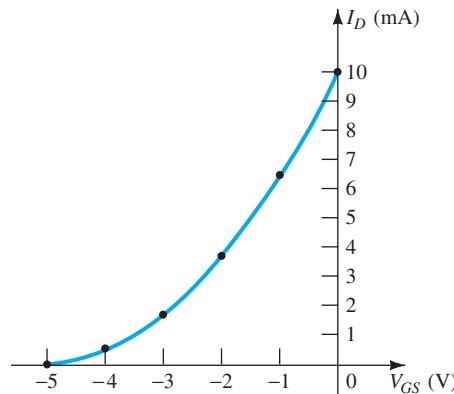
- Calculate  $g_{m0}$  for a JFET having device parameters  $I_{DSS} = 12 \text{ mA}$  and  $V_p = -4 \text{ V}$ .
- Determine the pinch-off voltage of a JFET with  $g_{m0} = 10 \text{ mS}$  and  $I_{DSS} = 12 \text{ mA}$ .
- For a JFET having device parameters  $g_{m0} = 5 \text{ mS}$  and  $V_p = -4 \text{ V}$ , what is the device current at  $V_{GS} = 0 \text{ V}$ ?
- Calculate the value of  $g_m$  for a JFET ( $I_{DSS} = 12 \text{ mA}$ ,  $V_p = -3 \text{ V}$ ) at a bias point of  $V_{GS} = -0.5 \text{ V}$ .
- For a JFET having  $g_m = 6 \text{ mS}$  at  $V_{GSQ} = -1 \text{ V}$ , what is the value of  $I_{DSS}$  if  $V_p = -2.5 \text{ V}$ ?
- A JFET ( $I_{DSS} = 10 \text{ mA}$ ,  $V_p = -5 \text{ V}$ ) is biased at  $I_D = I_{DSS}/4$ . What is the value of  $g_m$  at that bias point?
- Determine the value of  $g_m$  for a JFET ( $I_{DSS} = 8 \text{ mA}$ ,  $V_p = -5 \text{ V}$ ) when biased at  $V_{GSQ} = V_p/4$ .
- A specification sheet provides the following data (at a listed drain-source current):

$$g_{fs} = 4.5 \text{ mS}, \quad g_{os} = 25 \mu\text{S}$$

At the listed drain-source current, determine:

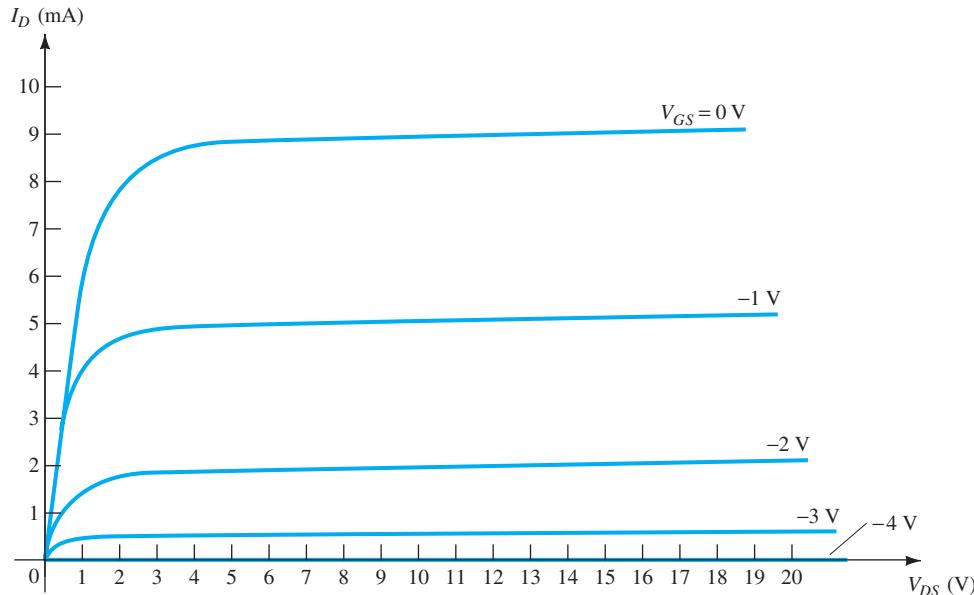
- $g_m$
- $r_d$

- For a JFET having specified values of  $g_{fs} = 4.5 \text{ mS}$  and  $g_{os} = 25 \mu\text{S}$ , determine the device output impedance  $Z_o(\text{FET})$  and device ideal voltage gain  $A_v(\text{FET})$ .
- If a JFET having a specified value of  $r_d = 100 \text{ k}\Omega$  has an ideal voltage gain of  $A_v(\text{FET}) = -200$ , what is the value of  $g_m$ ?

**FIG. 8.69**

JFET transfer characteristic for Problem 11.

11. Using the transfer characteristic of Fig. 8.69:
  - a. What is the value of  $g_{m0}$ ?
  - b. Determine  $g_m$  at  $V_{GS} = -0.5$  V graphically.
  - c. What is the value of  $g_m$  at  $V_{GS_Q} = -0.5$  V using Eq. (8.6)? Compare with the solution to part (b).
  - d. Graphically determine  $g_m$  at  $V_{GS} = -1$  V.
  - e. What is the value of  $g_m$  at  $V_{GS_Q} = -1$  V using Eq. (8.6)? Compare with the solution to part (d).
12. Using the drain characteristic of Fig. 8.70:
  - a. What is the value of  $r_d$  for  $V_{GS} = 0$  V?
  - b. What is the value of  $g_{m0}$  at  $V_{DS} = 10$  V?

**FIG. 8.70**

JFET drain characteristic for Problem 12.

13. For a 2N4220 n-channel JFET [ $g_{fs}$ (minimum) = 750  $\mu$ S,  $g_{os}$ (maximum) = 10  $\mu$ S]:
  - a. What is the value of  $g_m$ ?
  - b. What is the value of  $r_d$ ?
14. a. Plot  $g_m$  versus  $V_{GS}$  for an n-channel JFET with  $I_{DSS} = 12$  mA and  $V_P = -6$  V.  
b. Plot  $g_m$  versus  $I_D$  for the same n-channel JFET as part (a).
15. Sketch the ac equivalent model for a JFET if  $g_{fs} = 5.6$  mS and  $g_{os} = 15$   $\mu$ S.
16. Sketch the ac equivalent model for a JFET if  $I_{DSS} = 10$  mA,  $V_P = -4$  V,  $V_{GS_Q} = -2$  V, and  $g_{os} = 25$   $\mu$ S.

### 8.3 Fixed-Bias Configuration

17. Determine  $Z_i$ ,  $Z_o$ , and  $A_v$  for the network of Fig. 8.71 if  $I_{DSS} = 10 \text{ mA}$ ,  $V_P = -6 \text{ V}$ , and  $r_d = 40 \text{ k}\Omega$ .
18. a. Determine  $Z_i$ ,  $Z_o$ , and  $A_v$  for the network of Fig. 8.71 if  $I_{DSS}$  and  $V_P$  are one-half the values of Problems 17. This is  $I_{DSS} = 5 \text{ mA}$  and  $V_P = -3 \text{ V}$ .  
b. Compare the solutions to that of Problem 17.
19. a. Determine  $Z_i$ ,  $Z_o$ , and  $A_v$  for the network of Fig. 8.72 if  $I_{DSS} = 10 \text{ mA}$ ,  $V_P = -4 \text{ V}$ , and  $r_d = 20 \text{ k}\Omega$ .  
b. Repeat part (a) with  $r_d = 40 \text{ k}\Omega$ . What was the impact on the results?

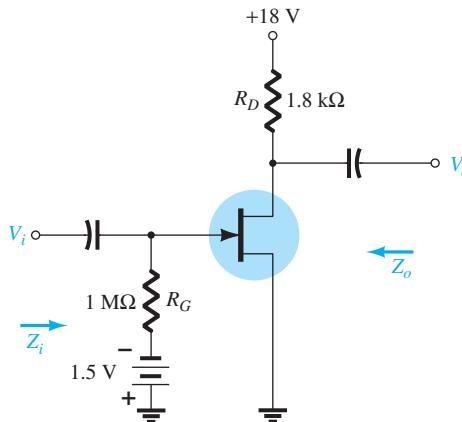


FIG. 8.71

Fixed-bias amplifier for Problems 17 and 18.

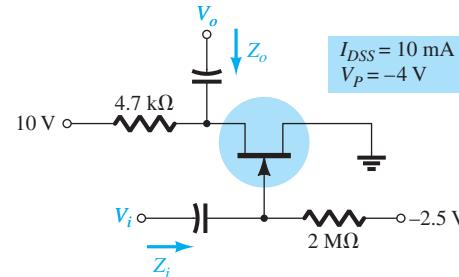


FIG. 8.72

Problem 19.

### 8.4 Self-Bias Configuration

20. Determine  $Z_i$ ,  $Z_o$ , and  $A_v$  for the network of Fig. 8.73 if  $g_{fs} = 3000 \mu\text{S}$  and  $g_{os} = 50 \mu\text{s}$ .
21. Determine  $Z_i$ ,  $Z_o$ , and  $A_v$  for the network of Fig. 8.73 if the 20-μF capacitor is removed and the parameters of the network are the same as in Problem 20. Compare results with those of Problem 20.
22. Repeat Problem 20 if  $g_{os}$  is 10 μS. Compare the results to those of Problem 20.
23. a. Find the value of  $R_S$  to obtain a voltage gain of 2 for the network of Fig. 8.74 using  $r_d = \infty \Omega$ .  
b. Repeat part (a) with  $r_d = 30 \text{ k}\Omega$ . What was the impact of the change in  $r_d$  on the gain and the analysis?

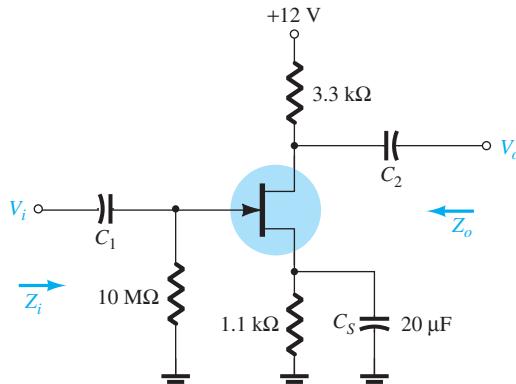


FIG. 8.73

Problems 20, 21, 22, and 59.

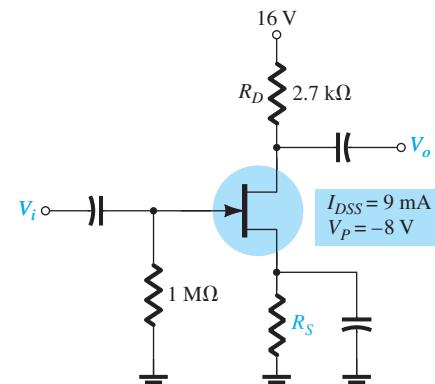


FIG. 8.74

Problem 23.

24. Determine  $Z_i$ ,  $Z_o$ , and  $A_v$  for the network of Fig. 8.75 if  $I_{DSS} = 6 \text{ mA}$ ,  $V_P = -6 \text{ V}$ , and  $g_{os} = 40 \mu\text{S}$ .

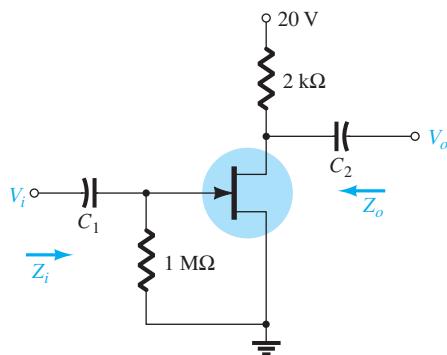


FIG. 8.75

Self-bias configuration for Problems 24 and 60.

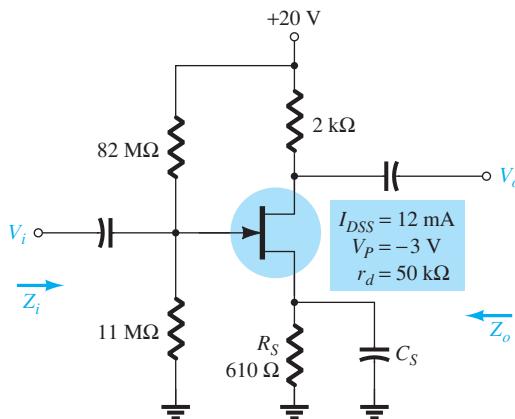


FIG. 8.76

Problems 25 to 28 and 61.

### 8.5 Voltage-Divider Configuration

25. Determine  $Z_i$ ,  $Z_o$ , and  $V_o$  for the network of Fig. 8.76 if  $V_i = 20 \text{ mV}$ .
26. Repeat Problem 25 with the capacitor  $C_S$  removed and compare results.
27. Repeat Problem 25 if  $r_d = 20 \text{ k}\Omega$  and compare results.
28. Repeat Problem 26 if  $r_d = 20 \text{ k}\Omega$  and compare results.

### 8.6 JFET Common-Gate Configuration

29. Determine  $Z_i$ ,  $Z_o$ , and  $V_o$  for the network of Fig. 8.77 if  $V_i = 4 \text{ mV}$ .
30. Repeat Problem 29 if  $r_d = 20 \text{ k}\Omega$  and compare results.
31. Determine  $Z_i$ ,  $Z_o$ , and  $A_v$  for the network of Fig. 8.78 if  $r_d = 30 \text{ k}\Omega$ .

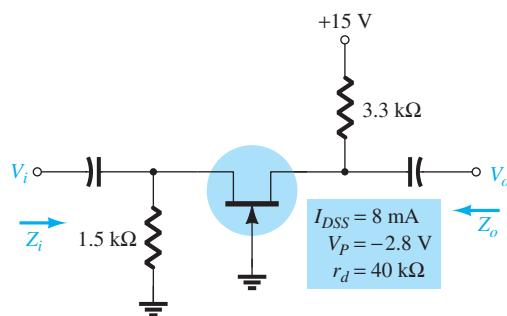


FIG. 8.77

Problems 29, 30, and 62.

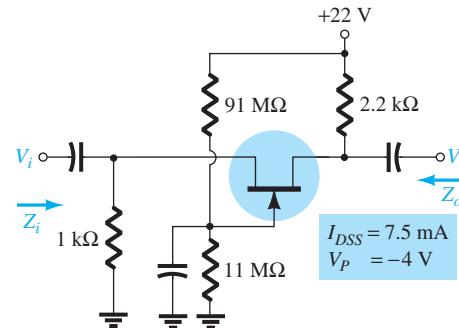


FIG. 8.78

Problem 31.

### 8.7 JFET Source-Follower Configuration

32. Determine  $Z_i$ ,  $Z_o$ , and  $A_v$  for the network of Fig. 8.79.
33. Repeat Problem 32 if  $r_d = 20 \text{ k}\Omega$  and compare results.
34. Determine  $Z_i$ ,  $Z_o$ , and  $A_v$  for the network of Fig. 8.80.

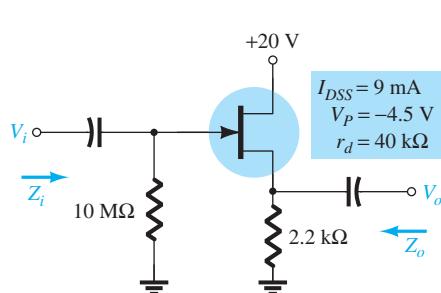


FIG. 8.79

Problems 32 and 33.

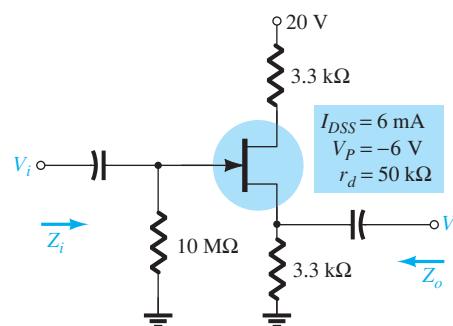


FIG. 8.80

Problem 34.

## 8.8 Depletion-Type MOSFETs

35. Determine  $V_o$  for the network of Fig. 8.81 if  $g_{os} = 20 \mu\text{S}$ .  
 36. Determine  $Z_i$ ,  $Z_o$ , and  $A_v$  for the network of Fig. 8.82 if  $r_d = 60 \text{ k}\Omega$ .  
 37. Repeat Problem 36 if  $r_d = 25 \text{ k}\Omega$  and compare results.

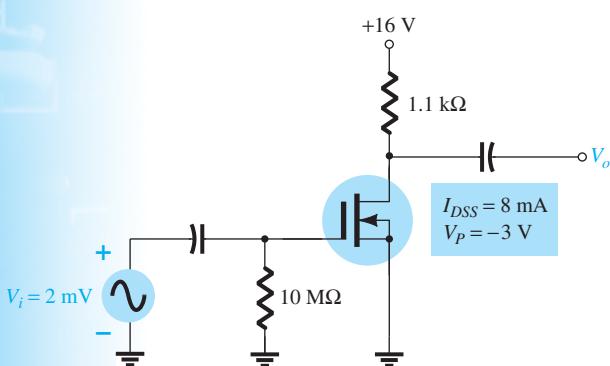


FIG. 8.81

Problem 35.

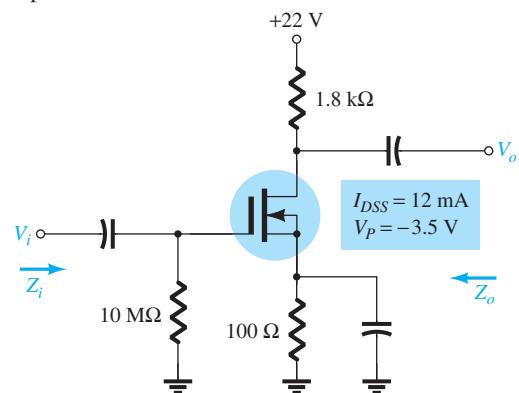


FIG. 8.82

Problems 36, 37, and 63.

38. Determine  $V_o$  for the network of Fig. 8.83 if  $V_i = 1.8 \text{ mV}$ .  
 39. Determine  $Z_i$ ,  $Z_o$ , and  $A_v$  for the network of Fig. 8.84.

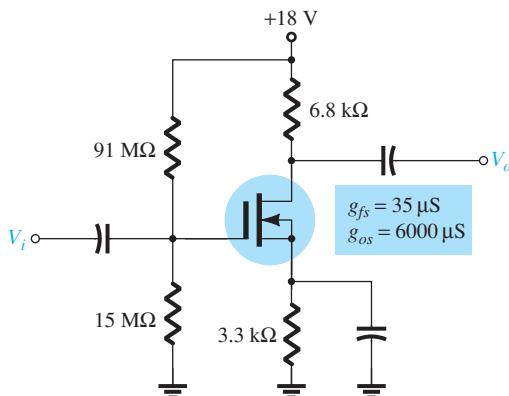


FIG. 8.83

Problem 38.

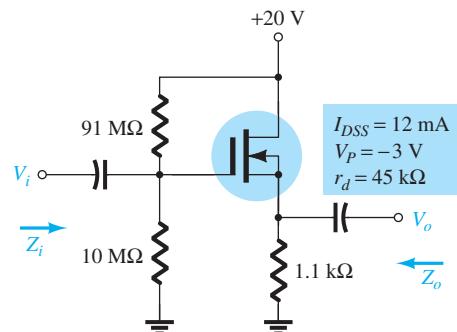


FIG. 8.84

Problem 39.

## 8.10 E-MOSFET Drain-Feedback Configuration

40. Determine  $g_m$  for a MOSFET if  $V_{GS(\text{Th})} = 3 \text{ V}$  and it is biased at  $V_{GS} = 8 \text{ V}$ . Assume  $k = 0.3 \times 10^{-3}$ .  
 41. Determine  $Z_i$ ,  $Z_o$ , and  $A_v$  for the amplifier of Fig. 8.85 if  $k = 0.3 \times 10^{-3}$ .  
 42. Repeat Problem 41 if  $k$  drops to  $0.2 \times 10^{-3}$ . Compare results.

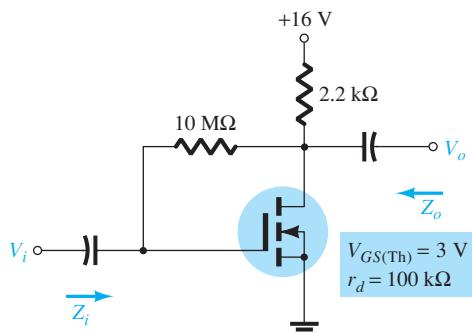
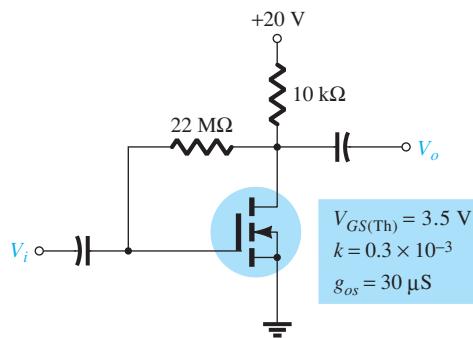


FIG. 8.85

Problems 41, 42, and 64.

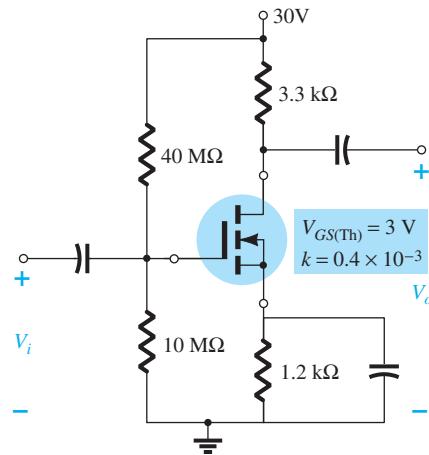
43. Determine  $V_o$  for the network of Fig. 8.86 if  $V_i = 20 \text{ mV}$ .
44. Determine  $V_o$  for the network of Fig. 8.86 if  $V_i = 4 \text{ mV}$ ,  $V_{GS(\text{Th})} = 4 \text{ V}$ , and  $I_{D(\text{on})} = 4 \text{ mA}$ , with  $V_{GS(\text{on})} = 7 \text{ V}$  and  $g_{os} = 20 \mu\text{S}$ .



**FIG. 8.86**  
Problems 43 and 44.

### 8.11 E-MOSFET Voltage-Divider Configuration

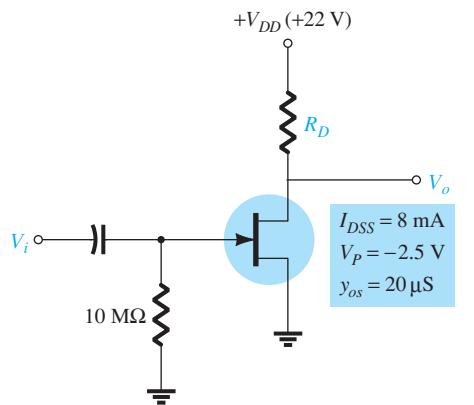
45. Determine the output voltage for the network of Fig. 8.87 if  $V_i = 0.8 \text{ mV}$  and  $r_d = 40 \text{ k}\Omega$ .



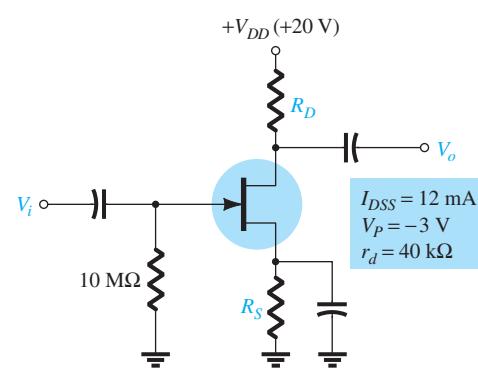
**FIG. 8.87**  
Problem 45.

### 8.12 Designing FET Amplifier Networks

46. Design the fixed-bias network of Fig. 8.88 to have a gain of 8.
47. Design the self-bias network of Fig. 8.89 to have a gain of 10. The device should be biased at  $V_{GSQ} = \frac{1}{3}V_P$ .



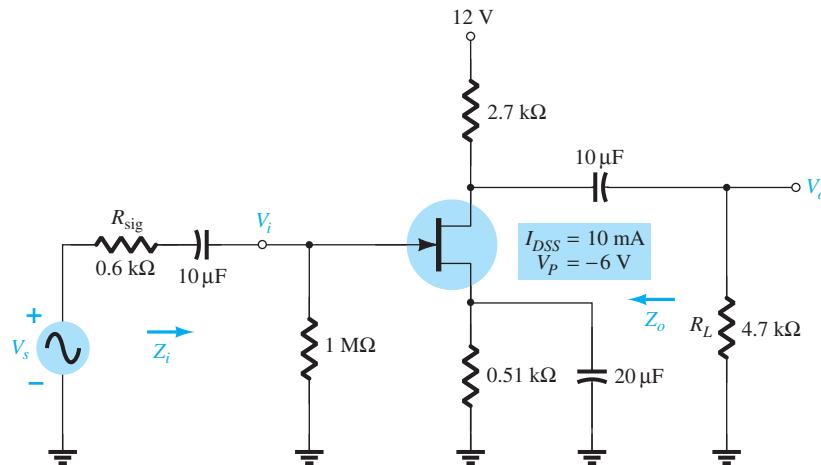
**FIG. 8.88**  
Problem 46.



**FIG. 8.89**  
Problem 47.

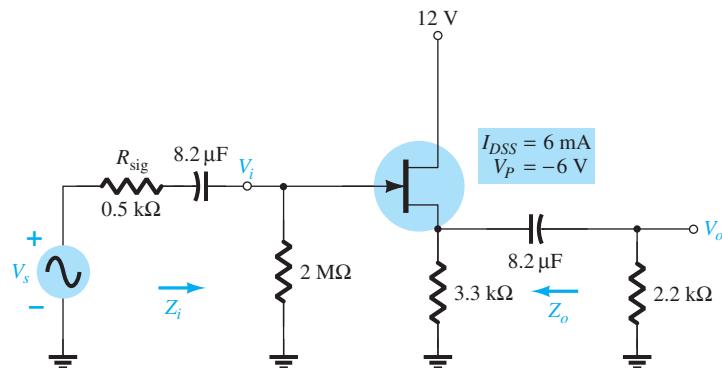
8.14 Effect of  $R_L$  and  $R_{\text{sig}}$ 

48. For the self-bias JFET network of Fig. 8.90:
- Determine  $A_{v_{NL}}$ ,  $Z_i$ , and  $Z_o$ .
  - Sketch the two-port model of Fig. 5.75 with the parameters determined in part (a) in place.
  - Determine  $A_{v_L}$  and  $A_{v_s}$ .
  - Change  $R_{\text{sig}}$  to  $10 \text{ k}\Omega$  and calculate the new levels of  $A_{v_L}$  and  $A_{v_s}$ . How is the voltage gain affected by an increase in  $R_s$ ?
  - For the change of part (d), determine  $Z_i$  and  $Z_o$ . What was the effect on both impedances?



**FIG. 8.90**  
Problem 48.

49. For the source-follower network of Fig. 8.91:
- Determine  $A_{v_{NL}}$ ,  $Z_i$ , and  $Z_o$ .
  - Sketch the two-port model of Fig. 5.75 with the parameters determined in part (a) in place.
  - Determine  $A_{v_L}$  and  $A_{v_s}$ .
  - Change  $R_L$  to  $4.7 \text{ k}\Omega$  and calculate  $A_{v_L}$  and  $A_{v_s}$ . What was the effect of increasing levels of  $R_L$  on both voltage gains?
  - Change  $R_{\text{sig}}$  to  $20 \text{ k}\Omega$  (with  $R_L$  at  $2.2 \text{ k}\Omega$ ) and calculate  $A_{v_L}$  and  $A_{v_s}$ . What was the effect of increasing levels of  $R_{\text{sig}}$  on both voltage gains?
  - Change  $R_L$  to  $4.7 \text{ k}\Omega$  and  $R_{\text{sig}}$  to  $20 \text{ k}\Omega$  and calculate  $Z_i$  and  $Z_o$ . What was the effect on both impedance parameters?



**FIG. 8.91**  
Problem 49.

50. For the common-gate configuration of Fig. 8.92:
- Determine  $A_{v_{NL}}$ ,  $Z_i$ , and  $Z_o$ .
  - Sketch the two-port model of Fig. 5.75 with the parameters determined in part (a) in place.
  - Determine  $A_{v_L}$  and  $A_{v_s}$ .
  - Change  $R_L$  to  $2.2 \text{ k}\Omega$  and calculate  $A_{v_L}$  and  $A_{v_s}$ . What was the effect of changing  $R_L$  on the voltage gains?

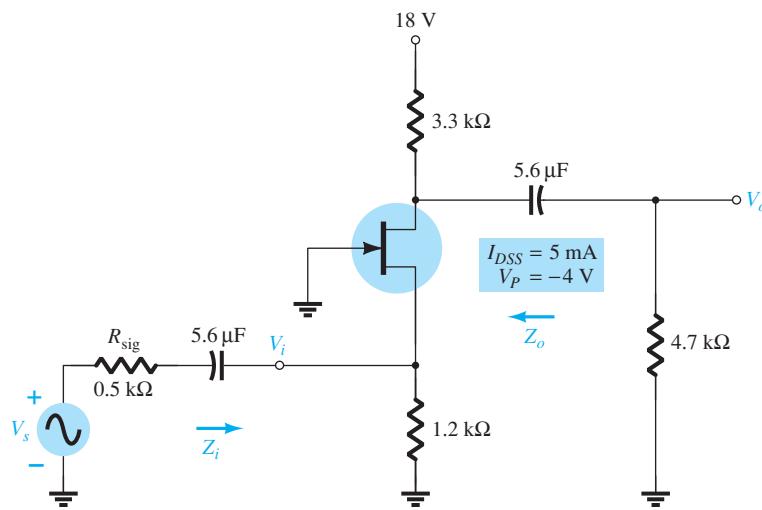


FIG. 8.92

Problem 50.

- e. Change  $R_{\text{sig}}$  to  $0.1 \text{ k}\Omega$  (with  $R_L$  at  $4.7 \text{ k}\Omega$ ) and calculate  $A_{v_L}$  and  $A_{v_s}$ . What was the effect of changing  $R_{\text{sig}}$  on the voltage gains?
- f. Change  $R_L$  to  $2.2 \text{ k}\Omega$  and  $R_{\text{sig}}$  to  $0.1 \text{ k}\Omega$  and calculate  $Z_i$  and  $Z_o$ . What was the effect on both parameters?
- g. What general conclusions can you draw from the above calculations?

### 8.15 Cascade Configuration

51. For the JFET cascade amplifier in Fig. 8.93, calculate the dc bias conditions for the two identical stages, using JFETs with  $I_{DSS} = 8 \text{ mA}$  and  $V_P = -4.5 \text{ V}$ .
52. For the JFET cascade amplifier of Fig. 8.93, using identical JFETs with  $I_{DSS} = 8 \text{ mA}$  and  $V_P = -4.5 \text{ V}$ , calculate the voltage gain of each stage, the overall gain of the amplifier, and the output voltage  $V_o$ .
53. If both JFETs in the cascade amplifier of Fig. 8.93 are changed to those having specifications  $I_{DSS} = 12 \text{ mA}$  and  $V_P = -3 \text{ V}$ , calculate the resulting dc bias of each stage.
54. If both JFETs in the cascade amplifier of Fig. 8.93 are changed to those having the specifications  $I_{DSS} = 12 \text{ mA}$ ,  $V_P = -3 \text{ V}$ , and  $g_{os} = 25 \mu\text{S}$ , calculate the resulting voltage gain for each stage, the overall voltage gain, and the output voltage,  $V_o$ .

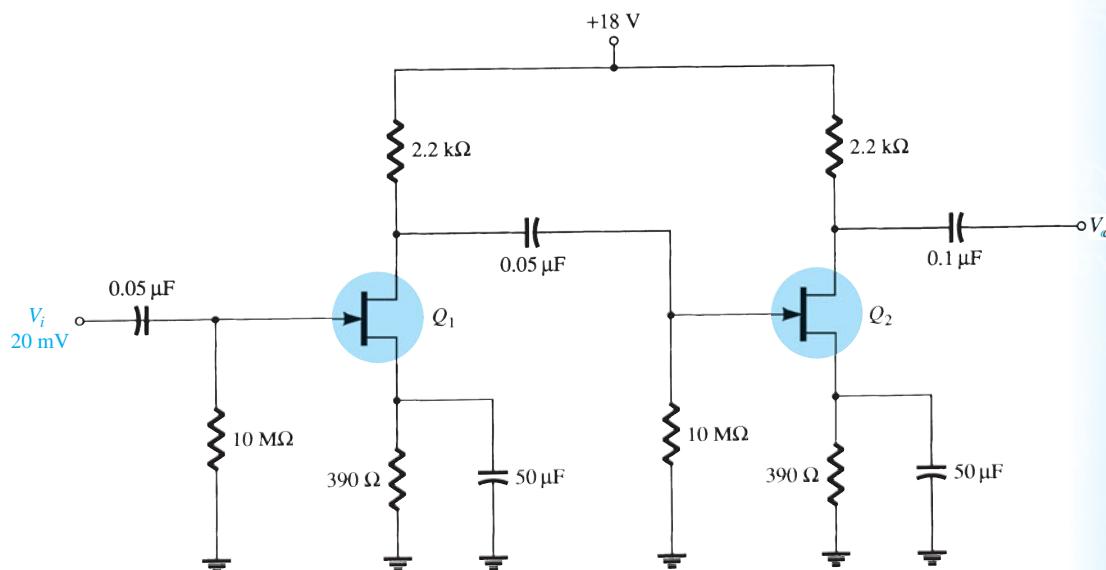
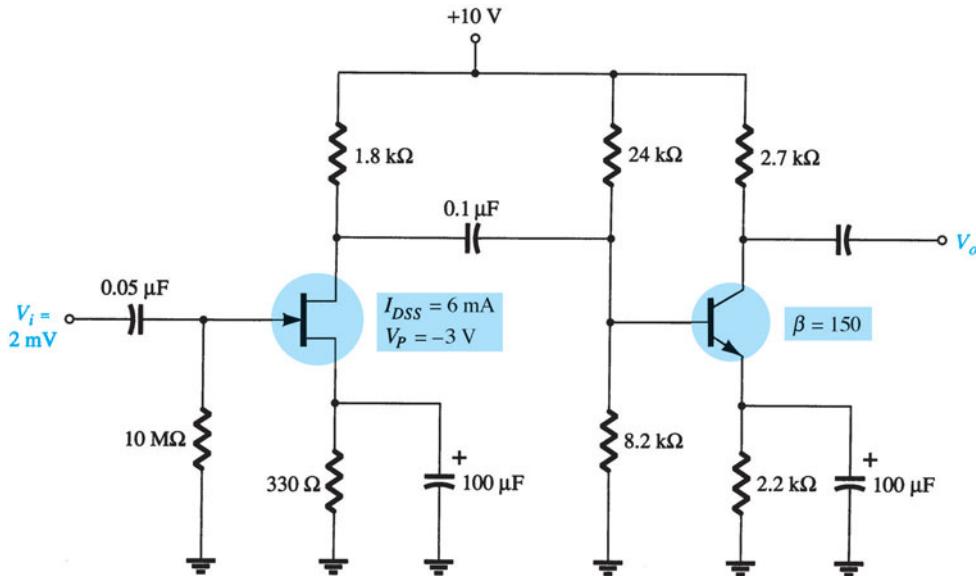


FIG. 8.93

Problems 51 to 55, 65, and 66.

55. For the cascade amplifier of Fig. 8.93, using JFETs with specifications  $I_{DSS} = 12 \text{ mA}$ ,  $V_P = -3 \text{ V}$ , and  $g_{os} = 25 \mu\text{S}$ , calculate the circuit input impedance ( $Z_i$ ) and output impedance ( $Z_o$ ).
56. For the cascade amplifier of Fig. 8.94, calculate the dc bias voltages currents of each stage.
57. For the amplifier circuit of Fig. 8.94, calculate the voltage gain of each stage and the overall amplifier voltage gain.
58. Calculate the input impedance ( $Z_i$ ) and output impedance ( $Z_o$ ) for the amplifier circuit of Fig. 8.94.



**FIG. 8.94**  
Problems 56 to 58.

### 8.19 Computer Analysis

59. Using PSpice Windows, determine the voltage gain for the network of Fig. 8.73.
60. Using Multisim, determine the voltage gain for the network of Fig. 8.75.
61. Using PSpice Windows, determine the voltage gain for the network of Fig. 8.76.
62. Using Multisim, determine the voltage gain for the network of Fig. 8.77.
63. Using PSpice Windows, determine the voltage gain for the network of Fig. 8.82.
64. Using PSpice Windows, determine the voltage gain for the network of Fig. 8.85.
- \*65. Use the Design Center to draw a schematic circuit of the cascade JFET amplifier as in Fig. 8.93. Set the JFET parameters for  $I_{DSS} = 12 \text{ mA}$  and  $V_P = 3 \text{ V}$ , and have the analysis determine the dc bias.
- \*66. Use the Design Center to draw a schematic circuit for a cascade JFET amplifier as shown in Fig. 8.93. Set the analysis to calculate the ac output voltage  $V_o$  for  $I_{DSS} = 12 \text{ mA}$  and  $V_P = -3 \text{ V}$ .

# 9

## BJT and JFET Frequency Response

### CHAPTER OBJECTIVES

- Develop confidence in the use of logarithms, understand the concept of decibels, and be able to accurately read a logarithmic plot.
- Become acquainted with the frequency response of a BJT and FET amplifier.
- Be able to normalize a frequency plot, establish the dB plot, and find the cutoff frequencies and bandwidth.
- Understand how straight-line segments and cutoff frequencies can result in a Bode plot that will define the frequency response of an amplifier.
- Be able to find the Miller effect capacitance at the input and output of an amplifier due to a feedback capacitor.
- Become familiar with square-wave testing to determine the frequency response of an amplifier.

### 9.1 INTRODUCTION

The analysis thus far has been limited to a particular frequency. For the amplifier, it was a frequency that normally permitted ignoring the effects of the capacitive elements, reducing the analysis to one that included only resistive elements and sources of the independent and controlled variety. We will now investigate the frequency effects introduced by the larger capacitive elements of the network at low frequencies and the smaller capacitive elements of the active device at high frequencies. Because the analysis will extend through a wide frequency range, the logarithmic scale will be defined and used throughout the analysis. In addition, because industry typically uses a decibel scale on its frequency plots, the concept of the decibel is introduced in some detail. The similarities between the frequency response analyses of both BJTs and FETs permit the coverage of both in the same chapter.

### 9.2 LOGARITHMS

In this field, there is no escaping the need to become comfortable with the logarithmic function. The plotting of a variable between wide limits, comparing levels without having to deal with unwieldy numbers, and identifying levels of particular importance in the design, review, and analysis procedures are all positive features of using the logarithmic function.

As a first step in clarifying the relationship between the variables of a logarithmic function, consider the following mathematical equations:

$$a = b^x, \quad x = \log_b a \quad (9.1)$$

The variables  $a$ ,  $b$ , and  $x$  are the same in each equation. If  $a$  is determined by taking the base  $b$  to the  $x$  power, the same  $x$  will result if the log of  $a$  is taken to the base  $b$ . For instance, if  $b = 10$  and  $x = 2$ ,

$$a = b^x = (10)^2 = 100$$

but

$$x = \log_b a = \log_{10} 100 = 2$$

In other words, if you were asked to find the power of a number that would result in a particular level such as

$$10,000 = 10^x$$

you could determine the level of  $x$  using logarithms. That is,

$$x = \log_{10} 10,000 = 4$$

For the electrical/electronics industry and in fact for the vast majority of scientific research, the base in the logarithmic equation is chosen as either 10 or the number  $e = 2.71828 \dots$

Logarithms taken to the base 10 are referred to as *common logarithms*, whereas logarithms taken to the base  $e$  are referred to as *natural logarithms*. In summary:

$$\text{Common logarithm: } x = \log_{10} a \quad (9.2)$$

$$\text{Natural logarithm: } y = \log_e a \quad (9.3)$$

The two are related by

$$\log_e a = 2.3 \log_{10} a \quad (9.4)$$

On scientific calculators, the common logarithm is typically denoted by the **log** key and the natural logarithm by the **ln** key.

**EXAMPLE 9.1** Using the calculator, determine the logarithm of the following numbers to the base indicated:

- a.  $\log_{10} 10^6$ .
- b.  $\log_e e^3$ .
- c.  $\log_{10} 10^{-2}$ .
- d.  $\log_e e^{-1}$ .

**Solution:**

- a. 6      b. 3      c. -2      d. -1

The results in Example 9.1 clearly reveal that

*the logarithm of a number taken to a power is simply the power of the number if the number matches the base of the logarithm.*

In the next example, the base and the variable  $x$  are not related by an integer power of the base.

**EXAMPLE 9.2** Using the calculator, determine the logarithm of the following numbers:

- a.  $\log_{10} 64$ .
- b.  $\log_e 64$ .
- c.  $\log_{10} 1600$ .
- d.  $\log_{10} 8000$ .

- a. 1.806    b. 4.159    c. 3.204    d. 3.903

Note in parts (a) and (b) of Example 9.2 that the logarithms  $\log_{10} a$  and  $\log_e a$  are indeed related as defined by Eq. (9.4). In addition, note that the logarithm of a number does not increase in the same linear fashion as the number. That is, 8000 is 125 times larger than 64, but the logarithm of 8000 is only about 2.16 times larger than the magnitude of the logarithm of 64, revealing a very nonlinear relationship. In fact, Table 9.1 clearly shows how the logarithm of a number increases only as the exponent of the number. If the antilogarithm of a number is desired, the  $10^x$  or  $e^x$  calculator function is employed.

TABLE 9.1

$\log_{10} 10^0$	= 0
$\log_{10} 10$	= 1
$\log_{10} 100$	= 2
$\log_{10} 1,000$	= 3
$\log_{10} 10,000$	= 4
$\log_{10} 100,000$	= 5
$\log_{10} 1,000,000$	= 6
$\log_{10} 10,000,000$	= 7
$\log_{10} 100,000,000$	= 8
etc.	

**EXAMPLE 9.3** Using a calculator, determine the antilogarithm of the following expressions:

- a.  $1.6 = \log_{10} a$ .  
b.  $0.04 = \log_e a$ .

**Solution:**

- a.  $a = 10^{1.6}$   
Using the  $10^x$  key:  $a = 39.81$   
b.  $a = e^{0.04}$   
Using the  $e^x$  key:  $a = 1.0408$

Because the remaining analysis of this chapter employs the common logarithm, we review a few properties of logarithms using solely the common logarithm. In general, however, the same relationships hold true for logarithms to any base. First, note that

$$\boxed{\log_{10} 1 = 0} \quad (9.5)$$

as clearly revealed by Table 9.1, because  $10^0 = 1$ . Next,

$$\boxed{\log_{10} \frac{a}{b} = \log_{10} a - \log_{10} b} \quad (9.6)$$

which for the special case of  $a = 1$  becomes

$$\boxed{\log_{10} \frac{1}{b} = -\log_{10} b} \quad (9.7)$$

which shows that for any  $b$  greater than 1, the logarithm of a number less than 1 is always negative. Finally,

$$\boxed{\log_{10} ab = \log_{10} a + \log_{10} b} \quad (9.8)$$

In each case, the equations employing natural logarithms have the same format.

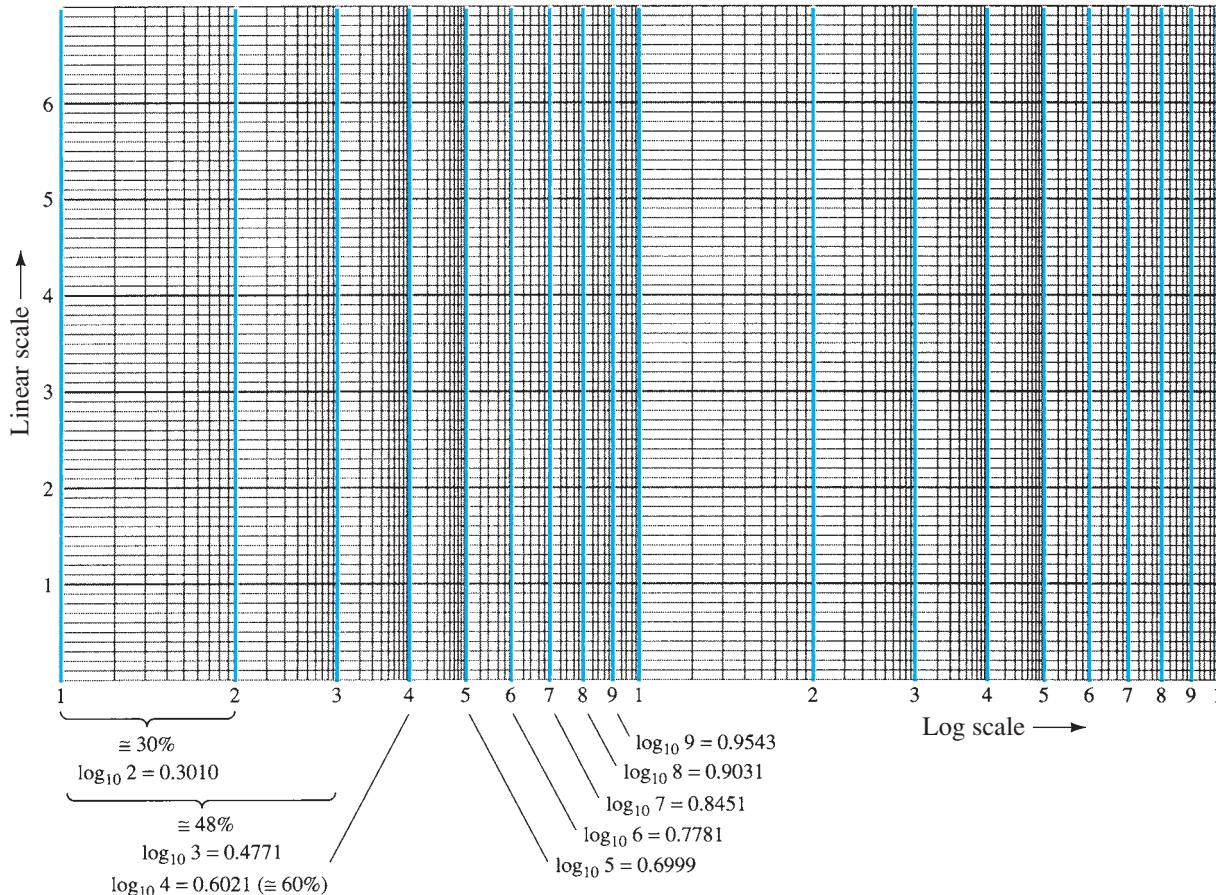
**EXAMPLE 9.4** Using a calculator, determine the logarithm of the following numbers:

- $\log_{10} 0.5$ .
- $\log_{10} \frac{4000}{250}$ .
- $\log_{10} (0.6 \times 30)$ .

**Solution:**

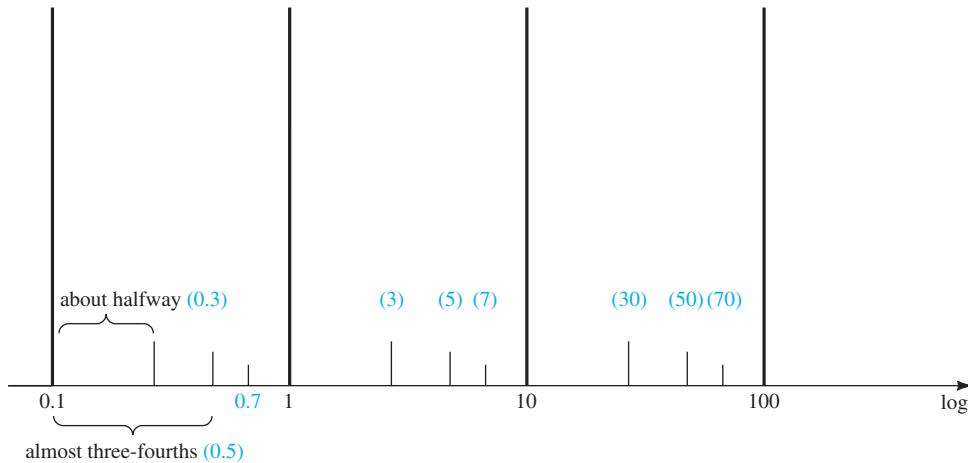
- 0.3**
- $\log_{10} 4000 - \log_{10} 250 = 3.602 - 2.398 = \mathbf{1.204}$   
Check:  $\log_{10} \frac{4000}{250} = \log_{10} 16 = \mathbf{1.204}$
- $\log_{10} 0.6 + \log_{10} 30 = -0.2218 + 1.477 = \mathbf{1.255}$   
Check:  $\log_{10} (0.6 \times 30) = \log_{10} 18 = \mathbf{1.255}$

The use of log scales can significantly expand the range of variation of a particular variable on a graph. Most graph paper available is of the semilog or double-log (log-log) variety. The term *semi* (meaning one-half) indicates that only one of the two scales is a log scale, whereas double-log indicates that both scales are log scales. A semilog scale appears in Fig. 9.1. Note that the vertical scale is a linear scale with equal divisions. The spacing between the lines of the log plot is shown on the graph. The log of 2 to the base 10 is approximately 0.3. The distance from 1 ( $\log_{10} 1 = 0$ ) to 2 is therefore 30% of the span. The log of 3 to the base 10 is 0.4771 or almost 48% of the span (very close to one-half



**FIG. 9.1**  
Semilog graph paper.

the distance between power-of-10 increments on the log scale). Because  $\log_{10} 5 \approx 0.7$ , it is marked off at a point 70% of the distance. Note that between any two digits the same compression of the lines appears as you progress from the left to the right. It is important to note the resulting numerical value and the spacing, because plots will typically only have the tic marks indicated in Fig. 9.2 due to a lack of space. The longer bars for this figure have the numerical values of 0.3, 3, and 30 associated with them, whereas the next-shorter bars have values of 0.5, 5, and 50 and the shortest bars 0.7, 7, and 70.



**FIG. 9.2**  
Identifying the numerical values of the tic marks on a log scale.

On many log plots, the tick marks for most of the intermediate levels are left off because of space constraints. The following equation can be used to determine the logarithmic level at a particular point between known levels using a ruler or simply estimating the distances. The parameters are defined by Fig. 9.3.

$$\text{Value} = 10^x \times 10^{d_1/d_2} \quad (9.9)$$

The derivation of Eq. (9.9) is simply an extension of the details regarding distance appearing in Fig. 9.1.

**EXAMPLE 9.5** Determine the value of the point appearing on the logarithmic plot in Fig. 9.4 using the measurements made by a ruler (linear).

**Solution:**

$$\frac{d_1}{d_2} = \frac{7/16''}{3/4''} = \frac{0.438''}{0.750''} = 0.584$$

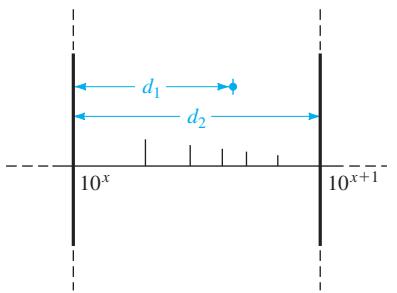
Using a calculator:

$$10^{d_1/d_2} = 10^{0.584} = 3.837$$

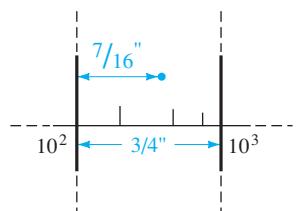
Applying Eq. (9.9):

$$\begin{aligned} \text{Value} &= 10^x \times 10^{d_1/d_2} = 10^2 \times 3.837 \\ &= 383.7 \end{aligned}$$

Plotting a function on a log scale can change the general appearance of the waveform as compared to a plot on a linear scale. A straight-line plot on a linear scale can develop a curve on a log scale, and a nonlinear plot on a linear scale can take on the appearance of a straight line on a log plot. The important point is that the results extracted at each level should be correctly labeled by developing a familiarity with the spacing of Figs. 9.1 and 9.2. This is particularly true for some of the log-log plots that appear later in this book.



**FIG. 9.3**  
Finding a value on a log plot.



**FIG. 9.4**  
Example 9.5.

### 9.3 DECIBELS

#### Power Levels

The concept of the decibel (dB) and the associated calculations will become increasingly important in the remaining sections of this chapter. The term *decibel* has its origin in the fact that power and audio levels are related on a logarithmic basis. That is, an increase in power level from, say, 4 W to 16 W does not result in an audio level increase by a factor of  $16/4 = 4$ , but by a factor of 2, as derived from the power of 4 in the following manner:  $(4)^2 = 16$ . For a change of 4 W to 64 W, the audio level will increase by a factor of 3 because  $(4)^3 = 64$ . In logarithmic form, the relationship can be written as  $\log_4 64 = 3$ .

The term *bel* is derived from the surname of Alexander Graham Bell. For standardization, the bel (B) is defined by the following equation relating two power levels,  $P_1$  and  $P_2$ :

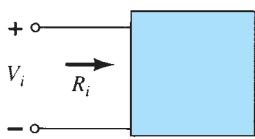
$$G = \log_{10} \frac{P_2}{P_1} \text{ bel} \quad (9.10)$$

It was found, however, that the bel was too large a unit of measurement for practical purposes, so the decibel (dB) is defined such that 10 decibels = 1 bel. Therefore,

$$G_{\text{dB}} = 10 \log_{10} \frac{P_2}{P_1} \text{ dB} \quad (9.11)$$

The terminal rating of electronic communication equipment (amplifiers, microphones, etc.) is commonly in decibels. Equation (9.11) indicates clearly, however, that the decibel rating is a measure of the difference in magnitude between *two* power levels. For a specified terminal (output) power ( $P_2$ ) there must be a reference power level ( $P_1$ ). The reference level is generally accepted to be 1 mW, although on occasion, the 6-mW standard of earlier years is applied. The resistance associated with the 1-mW power level is  $600 \Omega$ , chosen because it is the characteristic impedance of audio transmission lines. When the 1-mW level is employed as the reference level, the decibel symbol frequently appears as dBm. In equation form,

$$G_{\text{dBm}} = 10 \log_{10} \frac{P_2}{1 \text{ mW}} \Big|_{600 \Omega} \text{ dBm} \quad (9.12)$$



**FIG. 9.5**

Configuration employed in the discussion of Eq. (9.13).

There exists a second equation for decibels that is applied frequently. It can be best described through the system of Fig. 9.5. For  $V_i$  equal to some value  $V_1$ ,  $P_1 = V_1^2/R_i$ , where  $R_i$  is the input resistance of the system of Fig. 9.5. If  $V_i$  should be increased (or decreased) to some other level,  $V_2$  then  $P_2 = V_2^2/R_i$ . If we substitute into Eq. (9.11) to determine the resulting difference in decibels between the power levels, we obtain

$$G_{\text{dB}} = 10 \log_{10} \frac{P_2}{P_1} = 10 \log_{10} \frac{V_2^2/R_i}{V_1^2/R_i} = 10 \log_{10} \left( \frac{V_2}{V_1} \right)^2$$

and

$$G_{\text{dB}} = 20 \log_{10} \frac{V_2}{V_1} \text{ dB} \quad (9.13)$$

Frequently, the effect of different impedances ( $R_1 \neq R_2$ ) is ignored and Eq. (9.13) applied simply to establish a basis of comparison between levels—voltage or current. For situations of this type, the decibel gain should more correctly be referred to as the voltage or current gain in decibels to differentiate it from the common usage of decibel as applied to power levels.

In particular note the multiplying factor of 20 rather than the 10 of earlier equations.

#### Cascaded Stages

One of the advantages of the logarithmic relationship is the manner in which it can be applied to cascaded stages. For example, the magnitude of the overall voltage gain of a cascaded system is given by

$$|A_{v_T}| = |A_{v_1}| \cdot |A_{v_2}| \cdot |A_{v_3}| \cdots |A_{v_n}| \quad (9.14)$$

Applying the proper logarithmic relationship results in

$$G_v = 20 \log_{10} |A_{v_T}| = 20 \log_{10} |A_{v_1}| + 20 \log_{10} |A_{v_2}| + 20 \log_{10} |A_{v_3}| + \dots + 20 \log_{10} |A_{v_n}| \quad (\text{db}) \quad (9.15)$$

In words, the equation states that the decibel gain of a cascaded system is simply the sum of the decibel gains of each stage, that is,

$$G_{\text{dB}_T} = G_{\text{dB}_1} + G_{\text{dB}_2} + G_{\text{dB}_3} + \dots + G_{\text{dB}_n} \quad \text{dB} \quad (9.16)$$

### Voltage Gains versus dB Levels

Table 9.2 shows the association between dB levels and voltage gains. First note that a gain of 2 results in a dB level of +6 dB, whereas a drop to  $\frac{1}{2}$  results in a -6-dB level. A change in  $V_o/V_i$  from 1 to 10, 10 to 100, or 100 to 1000 results in the same 20-dB change in level. When  $V_o = V_i$ ,  $V_o/V_i = 1$ , and the dB level is 0. At a very high gain of 1000, the dB level is 60, whereas at the much higher gain of 10,000, the dB level is 80 dB, an increase of only 20 dB—a result of the logarithmic relationship. Table 9.2 clearly reveals that voltage gains of 50 dB or higher should immediately be recognized as being quite high.

**EXAMPLE 9.6** Find the magnitude gain corresponding to a voltage gain of 100 dB.

**Solution:** By Eq. (9.13),

$$G_{\text{dB}} = 20 \log_{10} \frac{V_2}{V_1} = 100 \text{ dB} \Rightarrow \log_{10} \frac{V_2}{V_1} = 5$$

so that

$$\frac{V_2}{V_1} = 10^5 = 100,000$$

**EXAMPLE 9.7** The input power to a device is 10,000 W at a voltage of 1000 V. The output power is 500 W and the output impedance is  $20 \Omega$ .

- Find the power gain in decibels.
- Find the voltage gain in decibels.
- Explain why parts (a) and (b) agree or disagree.

**Solution:**

$$\begin{aligned} \text{a. } G_{\text{dB}} &= 10 \log_{10} \frac{P_o}{P_i} = 10 \log_{10} \frac{500 \text{ W}}{10 \text{ kW}} = 10 \log_{10} \frac{1}{20} = -10 \log_{10} 20 \\ &= -10(1.301) = \mathbf{-13.01 \text{ dB}} \end{aligned}$$

$$\begin{aligned} \text{b. } G_v &= 20 \log_{10} \frac{V_o}{V_i} = 20 \log_{10} \frac{\sqrt{PR}}{1000} = 20 \log_{10} \frac{\sqrt{(500 \text{ W})(20 \Omega)}}{1000 \text{ V}} \\ &= 20 \log_{10} \frac{100}{1000} = 20 \log_{10} \frac{1}{10} = -20 \log_{10} 10 = \mathbf{-20 \text{ dB}} \end{aligned}$$

$$\text{c. } R_i = \frac{V_i^2}{P_i} = \frac{(1 \text{ kV})^2}{10 \text{ kW}} = \frac{10^6}{10^4} = \mathbf{100 \Omega \neq R_o = 20 \Omega}$$

**EXAMPLE 9.8** An amplifier rated at 40-W output is connected to a  $10\Omega$  speaker.

- Calculate the input power required for full power output if the power gain is 25 dB.
- Calculate the input voltage for rated output if the amplifier voltage gain is 40 dB.

**Solution:**

$$\begin{aligned} \text{a. Eq. (9.11): } 25 &= 10 \log_{10} \frac{40 \text{ W}}{P_i} \Rightarrow P_i = \frac{40 \text{ W}}{\text{antilog}(2.5)} = \frac{40 \text{ W}}{3.16 \times 10^2} \\ &= \frac{40 \text{ W}}{316} \cong \mathbf{126.5 \text{ mW}} \end{aligned}$$

TABLE 9.2

Comparing  $A_v = \frac{V_o}{V_i}$  to  $\text{dB}$

Voltage Gain, $V_o/V_i$	dB Level
0.5	-6
0.707	-3
1	0
2	6
10	20
40	32
100	40
1000	60
10,000	80
etc.	

b.  $G_v = 20 \log_{10} \frac{V_o}{V_i} \Rightarrow 40 = 20 \log_{10} \frac{V_o}{V_i}$

$$\frac{V_o}{V_i} = \text{antilog } 2 = 100$$

$$V_o = \sqrt{PR} = \sqrt{(40 \text{ W})(10 \text{ V})} = 20 \text{ V}$$

$$V_i = \frac{V_o}{100} = \frac{20 \text{ V}}{100} = 0.2 \text{ V} = 200 \text{ mV}$$

## Human Auditory Response

One of the most frequent applications of the decibel scale is in the communication and entertainment industries. The human ear does not respond in a linear fashion to changes in source power level, that is, a doubling of the audio power level from 1/2 W to 1 W does not result in a doubling of the loudness level for the human ear. In addition, a change from 5 W to 10 W is received by the ear as the same change in sound intensity as experienced from 1/2 W to 1 W. In other words, the ratio between levels is the same in each case ( $1 \text{ W}/0.5 \text{ W} = 10 \text{ W}/5 \text{ W} = 2$ ), resulting in the same decibel or logarithmic change defined by Eq. (9.11). The ear, therefore, responds in a logarithmic fashion to changes in audio power levels.

To establish a basis for comparison between audio levels, a reference level of 0.0002 **microbar** ( $\mu\text{bar}$ ) was chosen, where 1  $\mu\text{bar}$  is equal to the sound pressure of 1 dyne per square centimeter, or about 1 millionth of the normal atmospheric pressure at sea level. The 0.0002  $\mu\text{bar}$  level is the threshold level of hearing. Using this reference level, the sound pressure level in decibels is defined by the following equation:

$$\text{dB}_s = 20 \log_{10} \frac{P}{0.0002 \mu\text{bar}} \quad (9.17)$$

where  $P$  is the sound pressure in microbars.

The decibel levels in Table 9.3 are defined by Eq. (9.17). Meters designed to measure audio levels are calibrated to the levels defined by Eq. (9.17) and shown in Table 9.3.

In particular take note of the sound level for iPods and MP3 players, for which it is suggested, based on research, that they should not be used for more than 1 hour a day at 60% volume to prevent permanent hearing damage. Always remember that hearing damage is usually not reversible, so that any loss is for the long term.

A common question regarding audio levels is how much the power level of an acoustical source must be increased to double the sound level received by the human ear. The question is not as simple as it first seems due to considerations such as the frequency content of the sound, the acoustical conditions of the surrounding area, the physical characteristics of the surrounding medium, and—of course—the unique characteristics of the human ear. However, a general conclusion can be formulated that has practical value if we note the power levels of an acoustical source appearing to the left in Table 9.3. Each power level is associated with a particular decibel level, and a change of 10 dB in the scale corresponds to an increase or a decrease in power by a factor of 10. For instance, a change from 90 dB to 100 dB is associated with a change in wattage from 3 W to 30 W. Through experimentation, it has been found that on an average basis the loudness level doubles for every 10 dB change in audio level—a conclusion somewhat verified by the examples to the right in Table 9.3.

***To double the sound level received by the human ear, the power rating of the acoustical source (in watts) must be increased by a factor of 10.***

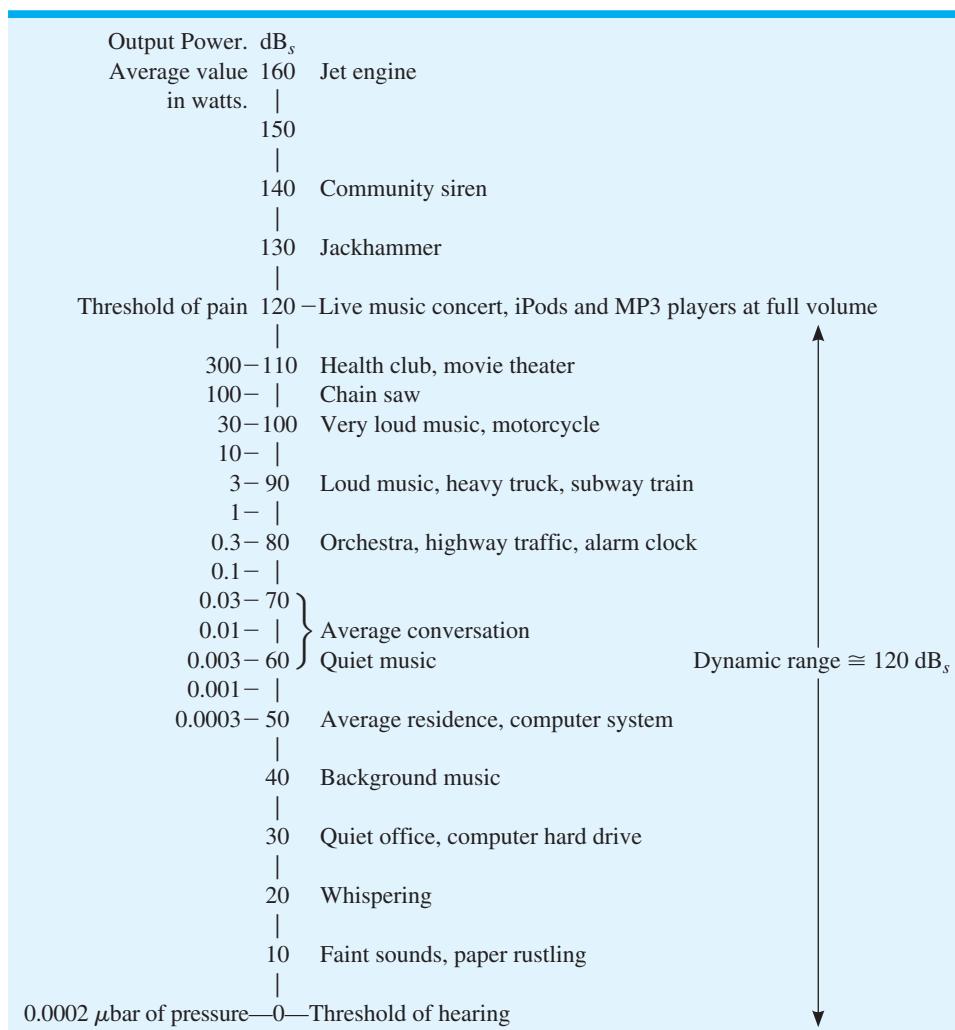
In other words, doubling the sound level available from a 1 W acoustical source requires moving up to a 10 W source.

Further:

***At normal hearing levels, it would take a change of about 3 dB (twice the power level) for the change to be noticeable to the human ear.***

***At low levels of sound, a change of 2 dB may be noticeable, but it may take a 6 dB (four times the power level) change for much higher levels of sound.***

**TABLE 9.3**  
*Typical sound levels and their decibel levels.*



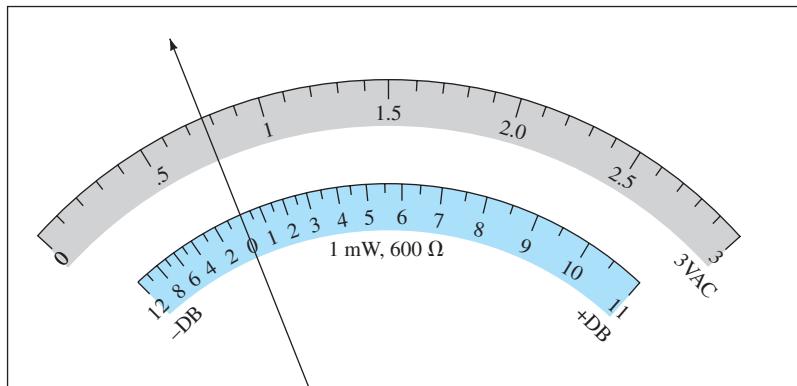
One final example of the use of dB as a unit of measurement is the LRAD (Long Range Acoustic Device) appearing in Fig. 9.6. It emits a tone between 2100 Hz and 3100 Hz at 145 dB that is effective at up to 500 m, or almost two football fields. The sound at its peak is thousands of times louder than a smoke alarm. It can be used to transmit critical information and instructions and is capable of strong deterrent tones against intruders.



**FIG. 9.6**  
*LRAD (Long Range Acoustic Device) 1000X. (Courtesy of LRAD Corporation.)*

## Instrumentation

A number of modern VOMs and DMMs have a dB scale designed to provide an indication of power ratios referenced to a standard level of 1 mW at 600 Ω. Since the reading is accurate only if the load has a characteristic impedance of 600 Ω, the 1 mW, 600 Ω reference level is normally printed somewhere on the face of the meter, as shown in Fig. 9.7. The dB scale is usually calibrated to the lowest ac scale of the meter. In other words, when making the dB measurement, choose the lowest ac voltage scale, but read the dB scale. If a higher voltage scale is chosen, a correction factor must be used, which is sometimes printed on the face of the meter but is always available in the meter manual. If the impedance is other than 600 Ω or not purely resistive, other correction factors must be used that are normally included in the meter manual. Using the basic power equation  $P = V^2/R$  reveals that 1 mW across a 600 Ω load is the same as applying 0.775 V rms across a 600 Ω load; that is,  $V = \sqrt{PR} = \sqrt{(1 \text{ mW})(600 \Omega)} = 0.775 \text{ V}$ . The result is that an analog display will have 0 dB [defining the reference point of 1 mW,  $\text{dB} = 10 \log_{10} P_2/P_1 = 10 \log_{10} (1\text{mW}/1 \text{mW}(\text{ref}) = 0 \text{ dB}]$  and 0.775 V rms on the same pointer projection, as shown in Fig. 9.7. A voltage of 2.5 V across a 600 Ω load results in a dB level of  $\text{dB} = 20 \log_{10} V_2/V_1 = 20 \log_{10} 2.5 \text{ V}/0.775 = 10.17 \text{ dB}$ , resulting in 2.5 V and 10.17 dB appearing along the same pointer projection. A voltage of less than 0.775 V, such as 0.5 V, results in a dB level of  $\text{dB} = 20 \log_{10} V_2/V_1 = 20 \log_{10} 0.5 \text{ V}/0.775 \text{ V} = -3.8 \text{ dB}$ , also shown on the scale in Fig. 9.7. Although a reading of 10 dB reveals that the power level is 10 times the reference, don't assume that a reading of 5 dB means that the output level is 5 mW. The 10 : 1 ratio is a special one in logarithmic use. For the 5 dB level, the power level must be found using the antilogarithm (3.126), which reveals that the power level associated with 5 dB is about 3.1 times the reference or 3.1 mW. A conversion table is usually provided in the manual for such conversions.



**FIG. 9.7**  
Defining the relationship between a dB scale referenced to  
1 mW, 600 Ω and a 3 V rms voltage scale.

## 9.4 GENERAL FREQUENCY CONSIDERATIONS

The frequency of the applied signal can have a pronounced effect on the response of a single-stage or multistage network. The analysis thus far has been for the midfrequency spectrum. At low frequencies, we shall find that the coupling and bypass capacitors can no longer be replaced by the short-circuit approximation because of the increase in reactance of these elements. The frequency-dependent parameters of the small-signal equivalent circuits and the stray capacitive elements associated with the active device and the network will limit the high-frequency response of the system. An increase in the number of stages of a cascaded system will also limit both the high- and low-frequency responses.

### Low-Frequency Range

To demonstrate how the larger coupling and bypass capacitors of a network will affect the frequency response of a system, the reactance of a 1- $\mu\text{F}$  (typical value for such applications) capacitor is tabulated in Table 9.4 for a wide range of frequencies.

**TABLE 9.4**

*Variation in  $X_C = \frac{1}{2\pi f C}$  with frequency for a 1- $\mu F$  capacitor*

<i>f</i>	<i>X<sub>C</sub></i>	
10 Hz	15.91 k $\Omega$	Range of possible effect
100 Hz	1.59 k $\Omega$	
1 kHz	159 $\Omega$	
10 kHz	15.9 $\Omega$	
100 kHz	1.59 $\Omega$	Range of lesser concern ( $\cong$ short-circuit equivalence)
1 MHz	0.159 $\Omega$	
10 MHz	15.9 m $\Omega$	
100 MHz	1.59 m $\Omega$	

Two regions have been defined in Table 9.4. For the range of 10 Hz to 10 kHz the magnitude of the reactance is sufficiently large that it may have an impact on the response of the system. However, for much higher frequencies it appears as though the capacitor is behaving much like the short-circuit equivalent it is designed to match.

Clearly, therefore,

*the larger capacitors of a system will have an important impact on the response of a system in the low-frequency range and can be ignored for the high-frequency region.*

## High-Frequency Range

For the smaller capacitors that come into play due to the parasitic capacitances of the device or network, the frequency range of concern will be the higher frequencies. Consider a 5-pF capacitor, typical of a parasitic capacitance of a transistor or the level of capacitance introduced simply by the wiring of the network, and the level of reactance that results for the same frequency range appearing in Table 9.4. The results appear in Table 9.5 and clearly reveal that at low frequencies they have a very large impedance matching the desired open-circuit equivalence. However, at higher frequencies they are approaching a short-circuit equivalence that can severely affect the response of a network.

**TABLE 9.5**

*Variation in  $X_C = \frac{1}{2\pi f C}$  with frequency for a 5 pF capacitor*

<i>f</i>	<i>X<sub>C</sub></i>	
10 Hz	3,183 M $\Omega$	Range of lesser concern ( $\cong$ open-circuit equivalent)
100 Hz	318.3 M $\Omega$	
1 kHz	31.83 M $\Omega$	
10 kHz	3.183 M $\Omega$	
100 kHz	318.3 k $\Omega$	Range of possible effect
1 MHz	31.83 k $\Omega$	
10 MHz	3.183 k $\Omega$	
100 MHz	318.3 $\Omega$	

Clearly, therefore,

*the smaller capacitors of a system will have an important impact on the response of a system in the high-frequency range and can be ignored for the low-frequency region.*

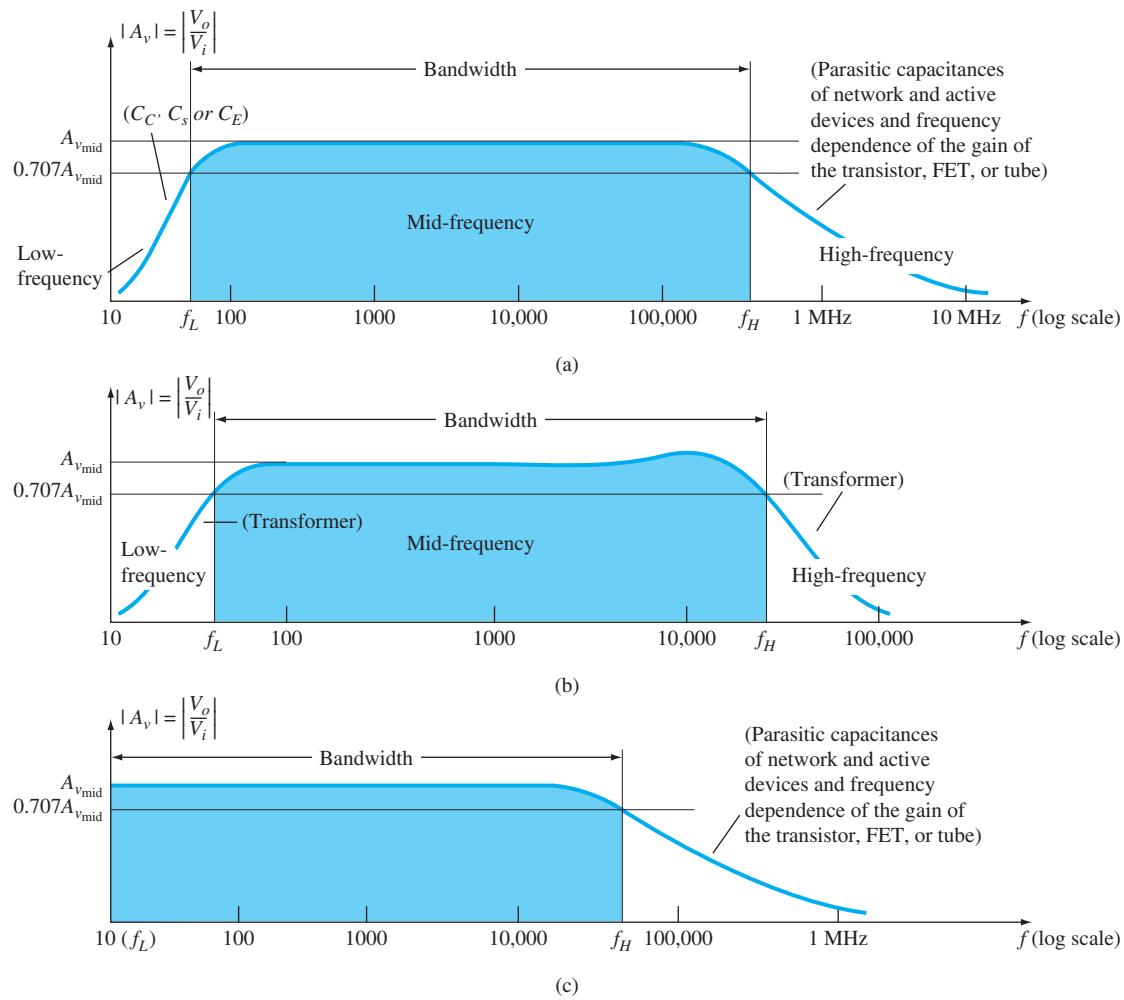
## Mid-Frequency Range

In the mid-frequency range the effect of the capacitive elements is largely ignored and the amplifier considered ideal and composed simply of resistive elements and controlled sources.

The result is that  
*the effect of the capacitive elements in an amplifier are ignored for the mid-frequency range when important quantities such as the gain and impedance levels are determined.*

### Typical Frequency Response

The magnitudes of the gain response curves of an *RC*-coupled, direct-coupled, and transformer-coupled amplifier system are provided in Fig. 9.8. Note that the horizontal scale is a logarithmic scale to permit a plot extending from the low- to the high-frequency regions. For each plot, a low-, a high-, and a mid-frequency region has been defined. In addition, the primary reasons for the drop in gain at low and high frequencies have also been indicated within the parentheses. For the *RC*-coupled amplifier, the drop at low frequencies is due to the increasing reactance of  $C_C$ ,  $C_s$ , or  $C_E$ , whereas its upper frequency limit is determined by either the parasitic capacitive elements of the network or the frequency dependence of the gain of the active device. An explanation of the drop in gain for the transformer-coupled system requires a basic understanding of “transformer action” and the transformer equivalent circuit. For the moment, let us say that it is simply due to the “shorting effect” (across the input terminals of the transformer) of the magnetizing inductive reactance at low frequencies ( $X_L = 2\pi fL$ ). The gain must obviously be zero at  $f = 0$  because at this point there is no longer a changing flux established through the core to induce a secondary or output voltage. As indicated in Fig. 9.8, the high-frequency response is controlled primarily by the stray capacitance between the turns of the primary and secondary windings. For the direct-coupled amplifier, there are no coupling or bypass capacitors to cause a drop in gain at low frequencies. As the figure indicates, it is a flat response to the upper cutoff



**FIG. 9.8**

Gain versus frequency: (a) *RC*-coupled amplifiers; (b) transformer-coupled amplifiers; (c) direct-coupled amplifiers.

frequency, which is determined by either the parasitic capacitances of the circuit or the frequency dependence of the gain of the active device.

For each system of Fig. 9.8, there is a band of frequencies in which the magnitude of the gain is either equal or relatively close to the midband value. To fix the frequency boundaries of relatively high gain,  $0.707A_{v\text{mid}}$  was chosen to be the gain at the cutoff levels. The corresponding frequencies  $f_L$  and  $f_H$  are generally called the *corner, cutoff, band, break, or half-power frequencies*. The multiplier 0.707 was chosen because at this level the output power is half the midband power output, that is, at midfrequencies,

$$P_{o\text{mid}} = \frac{|V_o|^2}{R_o} = \frac{|A_{v\text{mid}} V_i|^2}{R_o}$$

and at the half-power frequencies,

$$P_{o\text{HPF}} = \frac{|0.707 A_{v\text{mid}} V_i|^2}{R_o} = 0.5 \frac{|A_{v\text{mid}} V_i|^2}{R_o}$$

and

$$P_{o\text{HPF}} = 0.5 P_{o\text{mid}} \quad (9.18)$$

The bandwidth (or passband) of each system is determined by  $f_H$  and  $f_L$ , that is,

$$\text{bandwidth (BW)} = f_H - f_L \quad (9.19)$$

with  $f_H$  and  $f_L$  defined in each curve of Fig. 9.8.

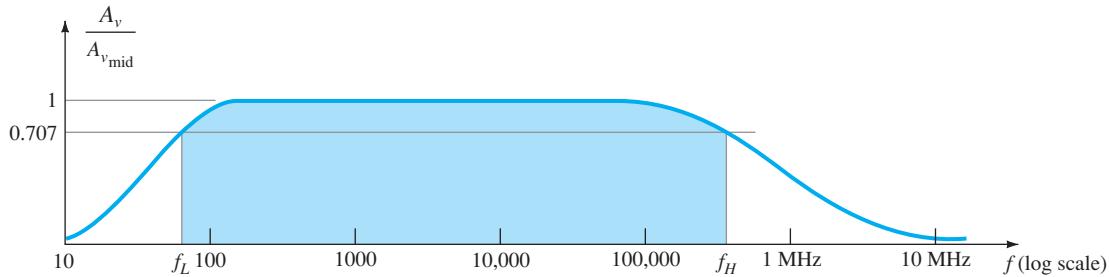
## 9.5 NORMALIZATION PROCESS

For applications of a communication nature (audio, video) a decibel plot versus frequency is normally provided rather than the gain versus frequency plot of Fig. 9.8. In other words, when you pick up a specification sheet on a particular amplifier or system, the plot will typically be of dB versus frequency rather than gain versus frequency.

To obtain such a dB plot the curve is first *normalized*—a process whereby the vertical parameter is divided by a specific level or quantity sensitive to a combination of variables of the system. For this area of investigation, it is usually the midband or maximum gain for the frequency range of interest.

For example, in Fig. 9.9 the curve of Fig. 9.8a is normalized by dividing the output voltage gain at each frequency by the midband level. Note that the curve has the same shape, but the band frequencies are now defined by simply the 0.707 level and not linked to the actual midband level. It clearly reveals that

***The band frequencies define a level where the gain or quantity of interest will be 70.7% or its maximum value.***



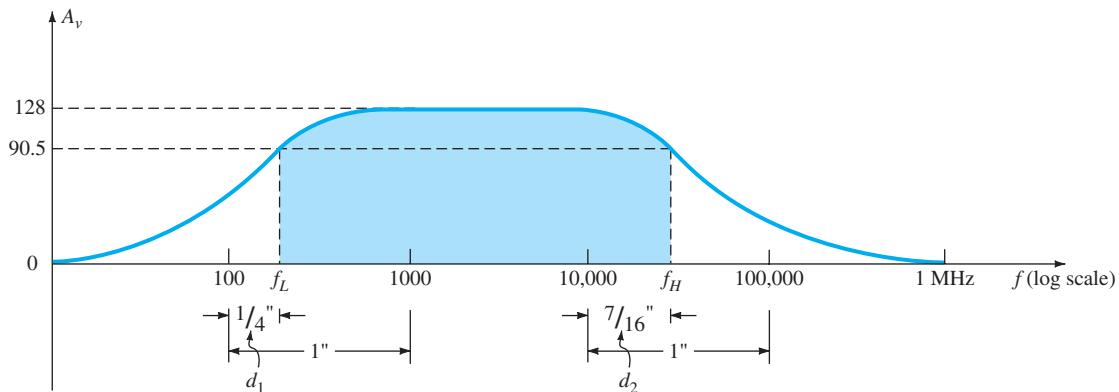
**FIG. 9.9**  
*Normalized gain versus frequency plot.*

Consider also that the plot of Fig. 9.9 is not sensitive to the actual level of the midband gain. The midband gain could be 50, 100, or even 200, and the resulting plot of Fig. 9.9 would be the same. The plot of Fig. 9.9 is now defining frequencies where the relative gain is defined rather than concerning itself with the “actual gain.”

The next example will demonstrate the normalization process for a typical amplifier response.

**EXAMPLE 9.9** Given the frequency response of Fig. 9.10:

- Find the cutoff frequencies  $f_L$  and  $f_H$  using the measurements provided.
- Find the bandwidth of the response.
- Sketch the normalized response.



**FIG. 9.10**  
Gain plot for Example 9.8.

**Solution:**

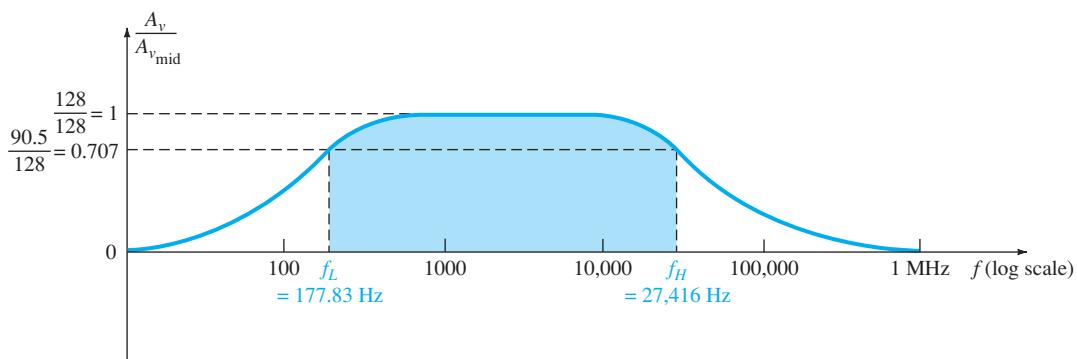
a. For  $f_L$ :  $\frac{d_1}{d_2} = \frac{1/4''}{1''} = 0.25$   
 $10^{d_1/d_2} = 10^{0.25} = 1.7783$   
 Value =  $10^x \times 10^{d_1/d_2} = 10^2 \times 1.7783 = 177.83 \text{ Hz}$

For  $f_H$ :  $\frac{d_1}{d_2} = \frac{7/16''}{1''} = 0.438$   
 $10^{d_1/d_2} = 10^{0.438} = 2.7416$   
 Value =  $10^x \times 10^{d_1/d_2} = 10^4 \times 2.7416 = 27,416 \text{ Hz}$

b. The bandwidth:

BW =  $f_H - f_L = 27,416 \text{ Hz} - 177.83 \text{ Hz} \approx 27.24 \text{ KHz}$

- c. The normalized response is determined by simply dividing each level of Fig. 9.10 by the midband level of 128, as shown in Fig. 9.11. The result is a maximum value of 1 and cutoff levels of 0.707.



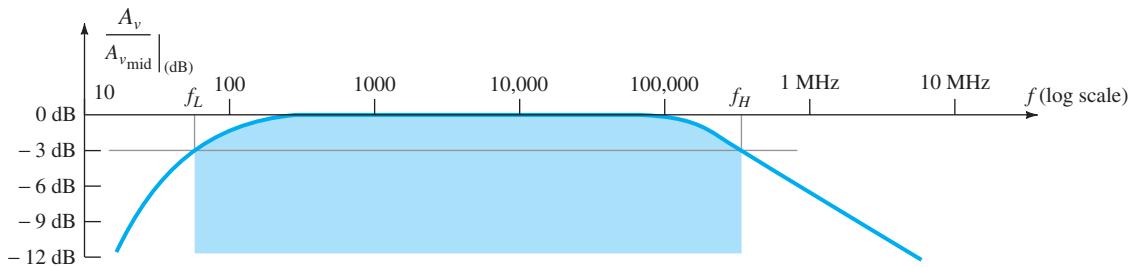
**FIG. 9.11**  
Normalized plot of Fig. 9.10.

A decibel plot of Fig. 9.11 can be obtained by applying Eq. (9.13) in the following manner:

$$\left| \frac{A_v}{A_{v\text{mid}}} \right|_{\text{dB}} = 20 \log_{10} \frac{A_v}{A_{v\text{mid}}}$$

(9.20)

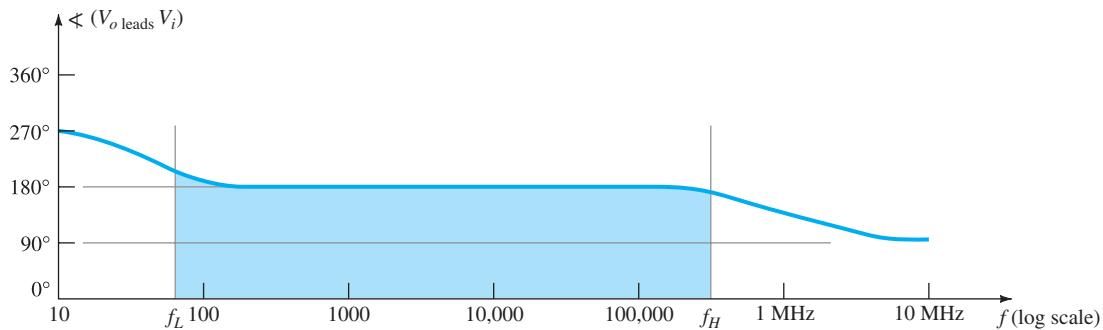
At midband frequencies,  $20 \log_{10} 1 = 0$ , and at the cutoff frequencies,  $20 \log_{10} 1/\sqrt{2} = -3$  dB. Both values are clearly indicated in the resulting decibel plot of Fig. 9.12. The smaller the fraction ratio, the more negative is the decibel level.



**FIG. 9.12**  
Decibel plot of the normalized gain versus frequency plot of Fig. 9.9.

For the greater part of the discussion to follow, a decibel plot will be made only for the low- and high-frequency regions. Keep Fig. 9.12 in mind, therefore, to permit a visualization of the broad system response.

Most amplifiers introduce a  $180^\circ$  phase shift between input and output signals. This fact must now be expanded to indicate that this is the case only in the midband region. At low frequencies, there is a phase shift such that  $V_o$  lags  $V_i$  by an increased angle. At high frequencies, the phase shift drops below  $180^\circ$ . Figure 9.13 is a standard phase plot for an *RC*-coupled amplifier.



**FIG. 9.13**  
Phase plot for an *RC*-coupled amplifier system.

## 9.6 LOW-FREQUENCY ANALYSIS—BODE PLOT

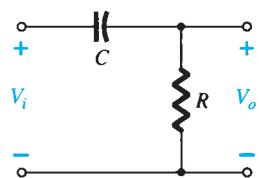
In the low-frequency region of the single-stage BJT or FET amplifier, it is the *RC* combinations formed by the network capacitors  $C_C$ ,  $C_E$ , and  $C_s$  and the network resistive parameters that determine the cutoff frequencies. In fact, an *RC* network similar to Fig. 9.14 can be established for each capacitive element, and the frequency at which the output voltage drops to 0.707 of its maximum value can be determined. Once the cutoff frequencies due to each capacitor are determined, they can be compared to establish which will determine the low-cutoff frequency for the system.

Consider, for example, the voltage-divider BJT network of Fig. 9.15 that was analyzed in detail in Section 5.6. The analysis of that section resulted in an input impedance of

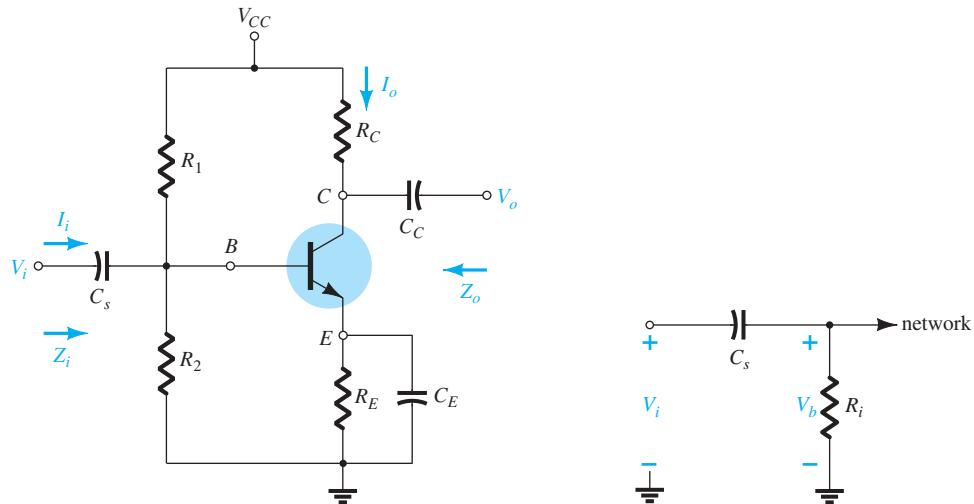
$$Z_i = R_i = R_1 \parallel R_2 \parallel \beta r_e$$

and an equivalent circuit at the input as shown in Fig. 9.16.

For the mid-frequency range the capacitor  $C_s$  is assumed to be an equivalent short-circuit state, and  $V_b = V_i$ . The result is a high midband gain for the amplifier that is not affected by the coupling or bypass capacitors. However, as we lower the applied frequency the reactance of the capacitor will increase and take an increasing share of the applied voltage  $V_i$ . Neglecting the effects of the coupling capacitor  $C_C$  and bypass capacitor  $C_E$  for the moment, if the voltage  $V_b$  should decrease, it will result in the same decrease in overall gain  $V_o/V_i$ .

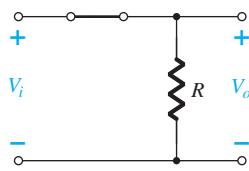


**FIG. 9.14**  
*RC* combination that will define a low-cutoff frequency.



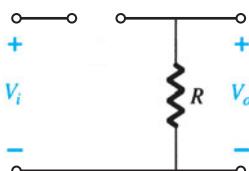
**FIG. 9.15**

Voltage-divider bias configuration.



**FIG. 9.17**

RC circuit of Fig. 9.14 at very high frequencies.



**FIG. 9.18**

RC circuit of Fig. 9.14 at  $f = 0 \text{ Hz}$ .

Less of the applied voltage is reaching the base of the transistor reducing the output voltage  $V_o$ . In fact if the  $V_b$  should drop to 0.707 of the peak possible value of  $V_i$  the overall gain will drop the same amount. In total, therefore, if we find the frequency that will result in  $V_b$  being only 0.707  $V_i$ , we will have the low-cut-off frequency for the full amplifier response.

Finding this frequency will now be examined by analyzing the generic  $RC$  network of Fig. 9.14 introduced above. Once the results are obtained it can be applied to any  $RC$  combination that may develop due to the other coupling capacitors or bypass capacitors. At high frequencies, the reactance of the capacitor of Fig. 9.14 is

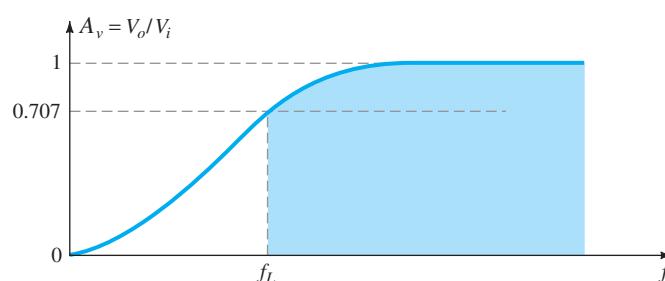
$$X_C = \frac{1}{2\pi f C} \approx 0 \Omega$$

and the short-circuit equivalent can be substituted for the capacitor as shown in Fig. 9.17. The result is that  $V_o \equiv V_i$  at high frequencies. At  $f = 0 \text{ Hz}$ ,

$$X_C = \frac{1}{2\pi f C} = \frac{1}{2\pi(0)C} = \infty \Omega$$

and the open-circuit approximation can be applied as shown in Fig. 9.18, with the result that  $V_o = 0 \text{ V}$ .

Between the two extremes, the ratio  $A_v = V_o/V_i$  will vary as shown in Fig. 9.19. As the frequency increases, the capacitive reactance decreases, and more of the input voltage appears across the output terminals.



**FIG. 9.19**  
Low-frequency response for the RC circuit of Fig. 9.14.

The output and input voltages are related by the voltage-divider rule in the following manner:

$$V_o = \frac{RV_i}{R + X_C}$$

where the boldface roman characters represent magnitude and angle of each quantity.

The magnitude of  $V_o$  is determined as follows:

$$V_o = \frac{RV_i}{\sqrt{R^2 + X_C^2}}$$

For the special case where  $X_C = R$ ,

$$V_o = \frac{RV_i}{\sqrt{R^2 + X_C^2}} = \frac{RV_i}{\sqrt{R^2 + R^2}} = \frac{RV_i}{\sqrt{2R^2}} = \frac{RV_i}{\sqrt{2}R} = \frac{1}{\sqrt{2}}V_i$$

and

$$|A_v| = \frac{V_o}{V_i} = \frac{1}{\sqrt{2}} = 0.707|_{X_C=R} \quad (9.21)$$

the level of which is indicated on Fig. 9.19. In other words, at the frequency for which  $X_C = R$ , the output will be 70.7% of the input for the network of Fig. 9.14.

The frequency at which this occurs is determined from

$$X_C = \frac{1}{2\pi f_L C} = R$$

and

$$f_L = \frac{1}{2\pi RC} \quad (9.22)$$

In terms of logs,

$$G_v = 20 \log_{10} A_v = 20 \log_{10} \frac{1}{\sqrt{2}} = -3 \text{ dB}$$

whereas at  $A_v = V_o/V_i = 1$  or  $V_o = V_i$  (the maximum value),

$$G_v = 20 \log_{10} 1 = 20(0) = 0 \text{ dB}$$

In Fig. 9.8, we recognize that there is a 3-dB drop in gain from the midband level when  $f = f_L$ . In a moment, we will find that an  $RC$  network will determine the low-frequency cutoff for a BJT transistor and  $f_L$  will be determined by Eq. (9.22).

If the gain equation is written as

$$A_v = \frac{V_o}{V_i} = \frac{R}{R - jX_C} = \frac{1}{1 - j(X_C/R)} = \frac{1}{1 - j(1/\omega CR)} = \frac{1}{1 - j(1/2\pi fCR)}$$

we obtain, using the frequency defined above,

$$A_v = \frac{1}{1 - j(f_L/f)} \quad (9.23)$$

In the magnitude and phase form,

$$A_v = \frac{V_o}{V_i} = \underbrace{\frac{1}{\sqrt{1 + (f_L/f)^2}}}_{\text{magnitude of } A_v} \underbrace{\tan^{-1}(f_L/f)}_{\substack{\text{phase by which} \\ V_o \text{ leads } V_i}} \quad (9.24)$$

For the magnitude when  $f = f_L$ ,

$$|A_v| = \frac{1}{\sqrt{1 + (1)^2}} = \frac{1}{\sqrt{2}} = 0.707 \Rightarrow -3 \text{ dB}$$

In the logarithmic form, the gain in dB is

$$A_{v(\text{dB})} = 20 \log_{10} \frac{1}{\sqrt{1 + (f_L/f)^2}} \quad (9.25)$$

Expanding Eq. (9.25):

$$\begin{aligned} A_{v(\text{dB})} &= -20 \log_{10} \left[ 1 + \left( \frac{f_L}{f} \right)^2 \right]^{1/2} \\ &= -\left(\frac{1}{2}\right)(20) \log_{10} \left[ 1 + \left( \frac{f_L}{f} \right)^2 \right] \\ &= -10 \log_{10} \left[ 1 + \left( \frac{f_L}{f} \right)^2 \right] \end{aligned}$$

For frequencies where  $f \ll f_L$  or  $(f_L/f)^2 \gg 1$ , the equation above can be approximated by

$$A_{v(\text{dB})} = -10 \log_{10} \left( \frac{f_L}{f} \right)^2$$

and finally,

$$A_{v(\text{dB})} = -20 \log_{10} \frac{f_L}{f} \quad f \ll f_L$$

(9.26)

Ignoring the condition  $f \ll f_L$  for a moment, we find that a plot of Eq. (9.26) on a frequency log scale yields a result very useful for future decibel plots.

$$\text{At } f = f_L: \frac{f_L}{f} = 1 \text{ and } -20 \log_{10} 1 = 0 \text{ dB}$$

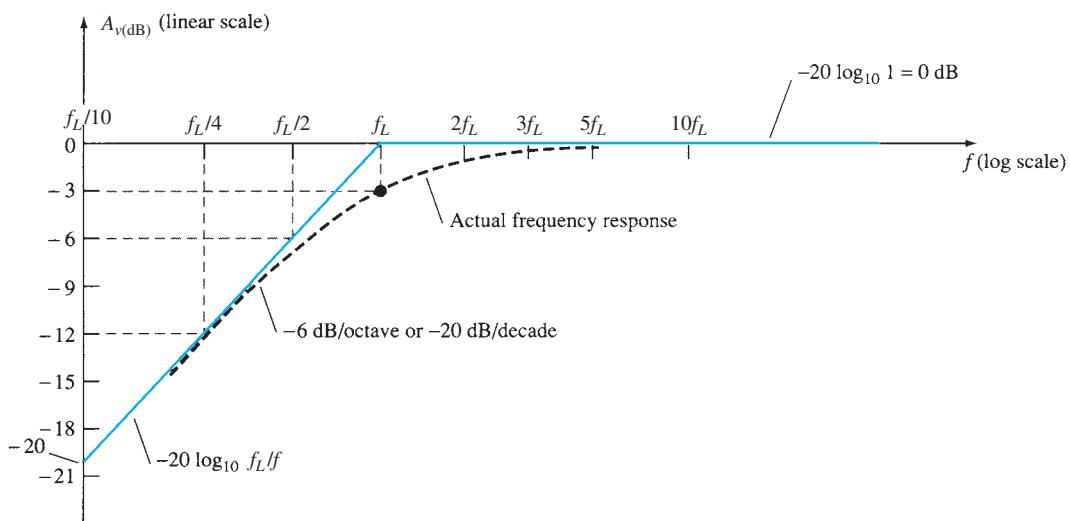
$$\text{At } f = \frac{1}{2}f_L: \frac{f_L}{f} = 2 \text{ and } -20 \log_{10} 2 \approx -6 \text{ dB}$$

$$\text{At } f = \frac{1}{4}f_L: \frac{f_L}{f} = 4 \text{ and } -20 \log_{10} 4 \approx -12 \text{ dB}$$

$$\text{At } f = \frac{1}{10}f_L: \frac{f_L}{f} = 10 \text{ and } -20 \log_{10} 10 = -20 \text{ dB}$$

A plot of these points is indicated in Fig. 9.20 from  $0.1f_L$  to  $f_L$  with a dark blue straight line. In the same figure, a straight line is also drawn for the condition of 0 dB for  $f \gg f_L$ . As stated earlier, the straight-line segments (asymptotes) are only accurate for 0 dB when  $f \gg f_L$  and the sloped line when  $f_L \gg f$ . We know, however, that when  $f = f_L$ , there is a 3-dB drop from the midband level. Employing this information in association with the straight-line segments permits a fairly accurate plot of the frequency response as indicated in the same figure.

*The piecewise linear plot of the asymptotes and associated breakpoints is called a Bode plot of the magnitude versus frequency.*



**FIG. 9.20**  
Bode plot for the low-frequency region.

The approach was developed by Professor Hendrik Bode in the 1940s (Fig. 9.21).

The calculations above and the curve itself demonstrate clearly that:

**A change in frequency by a factor of two, equivalent to one octave, results in a 6-dB change in the ratio, as shown by the change in gain from  $f_L/2$  to  $f_L$ .**

As noted by the change in gain from  $f_L/2$  to  $f_L$ :

**For a 10:1 change in frequency, equivalent to one decade, there is a 20-dB change in the ratio, as demonstrated between the frequencies of  $f_L/10$  and  $f_L$ .**

Therefore, a decibel plot can easily be obtained for a function having the format of Eq. (9.26). First, simply find  $f_L$  from the circuit parameters and then sketch two asymptotes—one along the 0-dB line and the other drawn through  $f_L$  sloped at 6 dB/octave or 20 dB/decade. Then, find the 3-dB point corresponding to  $f_L$  and sketch the curve.

The gain at any frequency can be determined from the frequency plot in the following manner:

$$A_{v(\text{dB})} = 20 \log_{10} \frac{V_o}{V_i}$$

but

$$\frac{A_{v(\text{dB})}}{20} = \log_{10} \frac{V_o}{V_i}$$

and

$$A_v = \frac{V_o}{V_i} = 10^{A_{v(\text{dB})}/20} \quad (9.27)$$

For example, if  $A_{v(\text{dB})} = -3$  dB,

$$A_v = \frac{V_o}{V_i} = 10^{(-3/20)} = 10^{(-0.15)} \approx 0.707 \quad \text{as expected}$$

The quantity  $10^{-0.15}$  is determined using the  $10^x$  function found on most scientific calculators.

The phase angle of  $\theta$  is determined from

$$\theta = \tan^{-1} \frac{f_L}{f} \quad (9.28)$$

from Eq. (9.24).

For frequencies  $f \ll f_L$ ,

$$\theta = \tan^{-1} \frac{f_L}{f} \rightarrow 90^\circ$$

For instance, if  $f_L = 100f$ ,

$$\theta = \tan^{-1} \frac{f_L}{f} = \tan^{-1}(100) = 89.4^\circ$$

For  $f = f_L$ ,

$$\theta = \tan^{-1} \frac{f_L}{f} = \tan^{-1} 1 = 45^\circ$$

For  $f \gg f_L$ ,

$$\theta = \tan^{-1} \frac{f_L}{f} \rightarrow 0^\circ$$

For instance, if  $f = 100f_L$ ,

$$\theta = \tan^{-1} \frac{f_L}{f} = \tan^{-1} 0.01 = 0.573^\circ$$

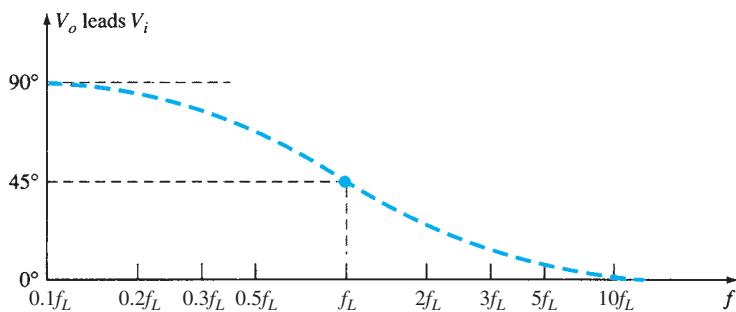
A plot of  $\theta = \tan^{-1}(f_L/f)$  is provided in Fig. 9.22. If we add the additional  $180^\circ$  phase shift introduced by an amplifier, the phase plot of Fig. 9.13 is obtained. The magnitude and phase response for an *RC* combination have now been established. In Section 9.7, each capacitor of importance in the low-frequency region will be redrawn in an *RC* format and the cutoff frequency for each determined to establish the low-frequency response for the BJT amplifier.



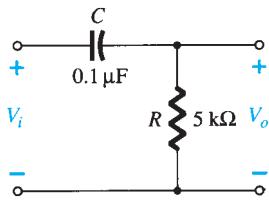
**American** (Madison, WI; Summit, NJ; Cambridge, MA)  
**(1905–1981)**  
**V.P. at Bell Laboratories**  
**Professor of Systems Engineering,**  
Harvard University

In his early years at Bell Laboratories, Hendrik Bode was involved with *electric filter* and *equalizer design*. He then transferred to the Mathematics Research Group, where he specialized in research pertaining to electrical networks theory and its application to long distance communication facilities. In 1948 he was awarded the Presidential Certificate of Merit for his work in electronic fire control devices. In addition to the publication of the book *Network Analysis and Feedback Amplifier Design* in 1945, which is considered a classic in its field, he has been granted 25 patents in electrical engineering and systems design. Upon retirement, Bode was elected Gordon McKay Professor of Systems Engineering at Harvard University. He was a fellow of the IEEE and American Academy of Arts and Sciences.

**FIG. 9.21**  
*Hendrik Wade Bode.*  
(Courtesy of AT&T Archives and History Center.)



**FIG. 9.22**  
Phase response for the RC circuit of Fig. 9.14.



**FIG. 9.23**  
Example 9.10.

**EXAMPLE 9.10** For the network of Fig. 9.23:

- Determine the break frequency.
- Sketch the asymptotes and locate the  $-3\text{-dB}$  point.
- Sketch the frequency response curve.
- Find the gain at  $A_{v(\text{dB})} = -6 \text{ dB}$ .

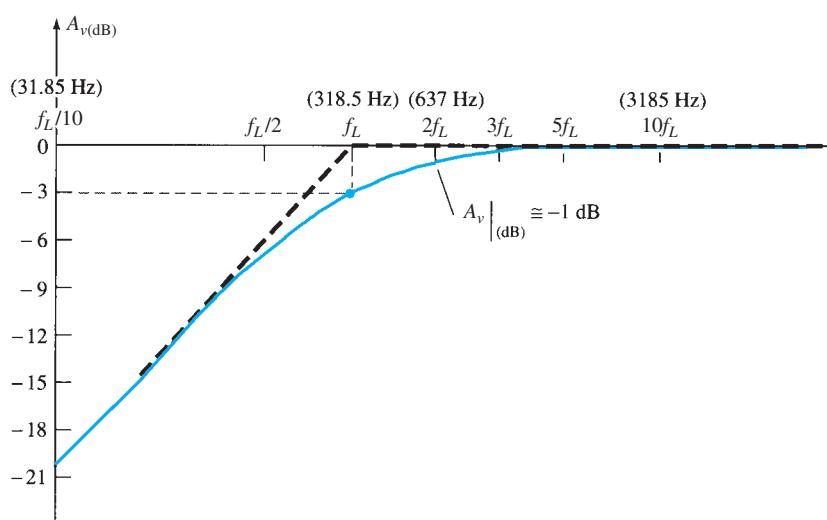
**Solution:**

$$\text{a. } f_L = \frac{1}{2\pi RC} = \frac{1}{(6.28)(5 \times 10^3 \Omega)(0.1 \times 10^{-6} \text{ F})} \cong 318.5 \text{ Hz}$$

b. and c. See Fig. 9.24.

$$\text{d. Eq. (9.27): } A_v = \frac{V_o}{V_i} = 10^{A_{v(\text{dB})}/20} = 10^{(-6/20)} = 10^{-0.3} = 0.501$$

and  $V_o = 0.501 V_i$  or approximately 50% of  $V_i$ .

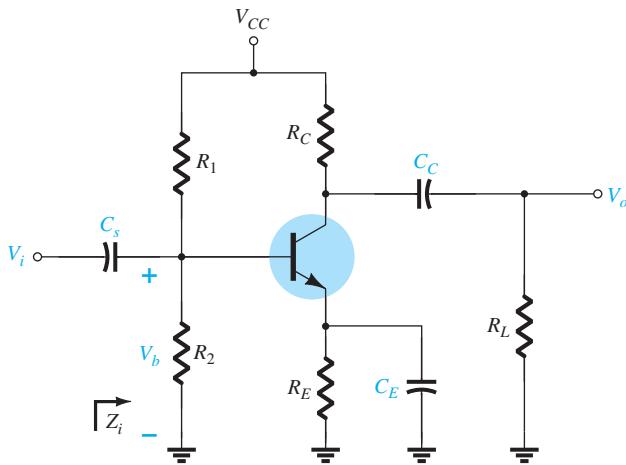


**FIG. 9.24**  
Frequency response for the RC circuit of Fig. 9.23.

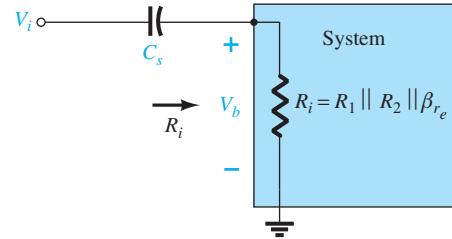
## 9.7 LOW-FREQUENCY RESPONSE—BJT AMPLIFIER WITH $R_L$

The analysis of this section will employ the loaded ( $R_L$ ) voltage-divider BJT bias configuration introduced earlier in Section 9.6. For the network of Fig. 9.25, the capacitors  $C_s$ ,  $C_C$ , and  $C_E$  will determine the low-frequency response. We will now examine the impact of each independently in the order listed.

**C<sub>s</sub>** Because  $C_s$  is normally connected between the applied source and the active device, the general form of the  $RC$  configuration is established by the network of Fig. 9.26, matching that of Fig. 9.16 with  $R_i = R_1 \parallel R_2 \parallel \beta r_e$ .



**FIG. 9.25**  
Loaded BJT amplifier with capacitors that affect the low-frequency response.



**FIG. 9.26**  
Determining the effect of  $C_s$  on the low-frequency response.

Applying the voltage-divider rule:

$$V_b = \frac{R_i V_i}{R_i - jX_{C_s}} \quad (9.29)$$

The cutoff frequency defined by  $C_s$  can be determined by manipulating the above equation into a standard form or simply using the results of Section 9.6. As a verification of the results of Section 9.6 the manipulation process is defined in detail below. For future RC networks, the results of Section 9.6 will simply be applied.

Rewriting Eq. (9.29):

$$\frac{V_b}{V_i} = \frac{R_i}{R_i - jX_{C_s}} = \frac{1}{1 - j\frac{X_{C_s}}{R_i}}$$

The factor

$$\frac{X_{C_s}}{R_i} = \left( \frac{1}{2\pi f C_s} \right) \left( \frac{1}{R_i} \right) = \frac{1}{2\pi f R_i C_s}$$

Defining

$$f_{L_s} = \frac{1}{2\pi R_i C_s} \quad (9.30)$$

we have

$$A_v = \frac{V_b}{V_i} = \frac{1}{1 - j(f_{L_s}/f)} \quad (9.31)$$

At  $f_{L_s}$  the voltage  $V_b$  will be 70.7% of the mid band value assuming  $C_s$  is the only capacitive element controlling the low-frequency response.

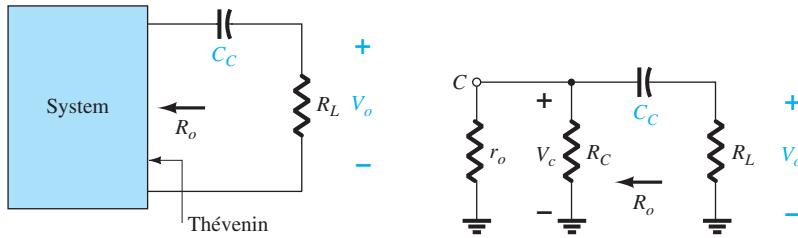
For the network of Fig. 9.25, when we analyze the effects of  $C_s$  we must make the assumption that  $C_E$  and  $C_C$  are performing their designed function or the analysis becomes too unwieldy, that is, that the magnitudes of the reactances of  $C_E$  and  $C_C$  permit employing a short-circuit equivalent in comparison to the magnitude of the other series impedances.

**C<sub>c</sub>** Because the coupling capacitor is normally connected between the output of the active device and the applied load, the *RC* configuration that determines the low-cut-off frequency due to  $C_C$  appears in Fig. 9.27. The total series resistance is now  $R_o + R_L$ , and the cutoff frequency due to  $C_C$  is determined by

$$f_{LC} = \frac{1}{2\pi(R_o + R_L)C_C} \quad (9.32)$$

Ignoring the effects of  $C_s$  and  $C_E$ , we find that the output voltage  $V_o$  will be 70.7% of its midband value at  $f_{LC}$ . For the network of Fig. 9.25, the ac equivalent network for the output section with  $V_i = 0$  V appears in Fig. 9.28. The resulting value for  $R_o$  in Eq. (9.32) is then simply

$$R_o = R_C \| r_o \quad (9.33)$$



**FIG. 9.27**  
Determining the effect of  $C_C$  on the low-frequency response.

**FIG. 9.28**  
Localized ac equivalent for  $C_C$  with  $V_i = 0$  V.

**C<sub>E</sub>** To determine  $f_{LE}$ , the network “seen” by  $C_E$  must be determined as shown in Fig. 9.29. Once the level of  $R_e$  is established, the cutoff frequency due to  $C_E$  can be determined using the following equation:

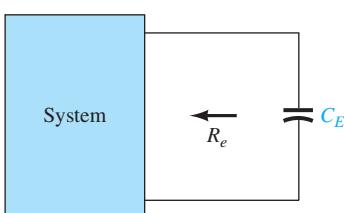
$$f_{LE} = \frac{1}{2\pi R_e C_E} \quad (9.34)$$

For the network of Fig. 9.25, the ac equivalent as “seen” by  $C_E$  appears in Fig. 9.30 as derived from Fig. 5.38. The value of  $R_e$  is therefore determined by

$$R_e = R_E \| \left( \frac{R_1 \| R_2}{\beta} + r_e \right) \quad (9.35)$$

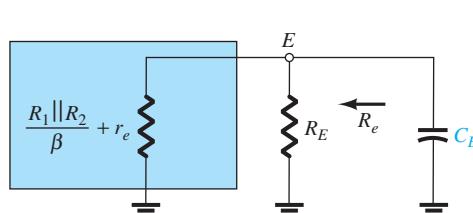
The effect of  $C_E$  on the gain is best described in a quantitative manner by recalling that the gain for the configuration of Fig. 9.31 is given by

$$A_v = \frac{-R_C}{r_e + R_E}$$



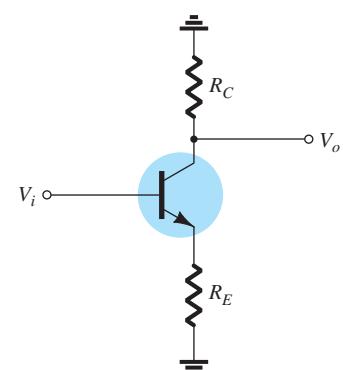
**FIG. 9.29**

Determining the effect of  $C_E$  on the low-frequency response.



**FIG. 9.30**

Localized ac equivalent of  $C_E$ .



**FIG. 9.31**

Network employed to describe the effect of  $C_E$  on the amplifier gain.

The maximum gain is obviously available where  $R_E$  is  $0\ \Omega$ . At low frequencies, with the bypass capacitor  $C_E$  in its “open-circuit” equivalent state, all of  $R_E$  appears in the gain equation above, resulting in the minimum gain. As the frequency increases, the reactance of the capacitor  $C_E$  will decrease, reducing the parallel impedance of  $R_E$  and  $C_E$  until the resistor  $R_E$  is effectively “shorted out” by  $C_E$ . The result is a maximum or midband gain determined by  $A_v = -R_C/r_e$ . At  $f_{LE}$  the gain will be 3 dB below the midband value determined with  $R_E$  “shorted out.”

Before continuing, keep in mind that  $C_s$ ,  $C_C$ , and  $C_E$  will affect only the low-frequency response. At the midband frequency level, the short-circuit equivalents for the capacitors can be inserted. Although each will affect the gain  $A_v = V_o/V_i$  in a similar frequency range, the highest low-frequency cutoff determined by  $C_s$ ,  $C_C$ , or  $C_E$  will have the greatest impact because it will be the last encountered before the midband level. If the frequencies are relatively far apart, the highest cutoff frequency will essentially determine the lower cutoff frequency for the entire system. If there are two or more “high” cutoff frequencies, the effect will be to raise the lower cutoff frequency and reduce the resulting bandwidth of the system. In other words, there is an interaction between capacitive elements that can affect the resulting low-cutoff frequency. However, if the cutoff frequencies established by each capacitor are sufficiently separated, the effect of one on the other can be ignored with a high degree of accuracy—a fact that will be demonstrated by the printouts to appear in the following example.

**EXAMPLE 9.11** Determine the cutoff frequencies for the network of Fig. 9.25 using the following parameters:

$$\begin{aligned} C_s &= 10\ \mu\text{F}, & C_E &= 20\ \mu\text{F}, & C_C &= 1\ \mu\text{F} \\ R_1 &= 40\ \text{k}\Omega, & R_2 &= 10\ \text{k}\Omega, & R_E &= 2\ \text{k}\Omega, & R_C &= 4\ \text{k}\Omega, \\ R_L &= 2.2\ \text{k}\Omega \\ \beta &= 100, & r_o &= \infty\ \Omega, & V_{CC} &= 20\ \text{V} \end{aligned}$$

**Solution:** To determine  $r_e$  for dc conditions, we first apply the test equation:

$$\beta R_E = (100)(2\ \text{k}\Omega) = 200\ \text{k}\Omega \gg 10R_2 = 100\ \text{k}\Omega$$

Since satisfied the dc base voltage is determined by

$$V_B \cong \frac{R_2 V_{CC}}{R_2 + R_1} = \frac{10\ \text{k}\Omega(20\ \text{V})}{10\ \text{k}\Omega + 40\ \text{k}\Omega} = \frac{200\ \text{V}}{50} = 4\ \text{V}$$

with  $I_E = \frac{V_E}{R_E} = \frac{4\ \text{V} - 0.7\ \text{V}}{2\ \text{k}\Omega} = \frac{3.3\ \text{V}}{2\ \text{k}\Omega} = 1.65\ \text{mA}$

so that  $r_e = \frac{26\ \text{mV}}{1.65\ \text{mA}} \cong \mathbf{15.76\ \Omega}$

and  $\beta r_e = 100(15.76\ \Omega) = 1576\ \Omega = \mathbf{1.576\ k\Omega}$

**Midband Gain**  $A_v = \frac{V_o}{V_i} = \frac{-R_C \| R_L}{r_e} = -\frac{(4\ \text{k}\Omega) \| (2.2\ \text{k}\Omega)}{15.76\ \Omega} \cong -90$

**C<sub>s</sub>**  $R_i = R_1 \| R_2 \| \beta r_e = 40\ \text{k}\Omega \| 10\ \text{k}\Omega \| 1.576\ \text{k}\Omega \cong 1.32\ \text{k}\Omega$

$$f_{LS} = \frac{1}{2\pi R_i C_s} = \frac{1}{(6.28)(1.32\ \text{k}\Omega)(10\ \mu\text{F})}$$

$$f_{LS} \cong \mathbf{12.06\ Hz}$$

**C<sub>c</sub>** 
$$\begin{aligned} f_{LC} &= \frac{1}{2\pi(R_o + R_L)C_C} \quad \text{with} \quad R_o = R_C \| r_o \cong R_C \\ &= \frac{1}{(6.28)(4\ \text{k}\Omega + 2.2\ \text{k}\Omega)(1\ \mu\text{F})} \\ &\cong \mathbf{25.68\ Hz} \end{aligned}$$

C<sub>E</sub>

$$\begin{aligned}
 R_e &= R_E \parallel \left( \frac{R_1 \parallel R_2}{\beta} + r_e \right) \\
 &= 2 \text{k}\Omega \parallel \left( \frac{40 \text{k}\Omega \parallel 10 \text{k}\Omega}{100} + 15.76 \Omega \right) \\
 &= 2 \text{k}\Omega \parallel \left( \frac{8 \text{k}\Omega}{100} + 15.76 \Omega \right) \\
 &= 2 \text{k}\Omega \parallel (80 \Omega + 15.76 \Omega) \\
 &= 2 \text{k}\Omega \parallel 95.76 \Omega \\
 &= 91.38 \Omega
 \end{aligned}$$

$$f_{L_E} = \frac{1}{2\pi R_e C_E} = \frac{1}{(6.28)(91.38 \Omega)(20 \mu\text{F})} = \frac{10^6}{11,477.73} \approx 87.13 \text{ Hz}$$

Since  $f_{L_E} \gg f_{L_C}$  or  $f_{L_S}$  the bypass capacitor  $C_E$  is determining the lower cutoff frequency of the amplifier.

## 9.8 IMPACT OF $R_s$ ON THE BJT LOW-FREQUENCY RESPONSE

In this section we will investigate the impact of the source resistance on the various cutoff frequencies. In Fig. 9.32 a signal source and associated resistance have been added to the configuration of Fig. 9.25. The gain will now be between the output voltage  $V_o$  and the signal source  $V_s$ .

**C<sub>s</sub>** The equivalent circuit at the input is now as shown in Fig. 9.33, with  $R_i$  continuing to be equal to  $R_1 \parallel R_2 \parallel \beta r_e$ .

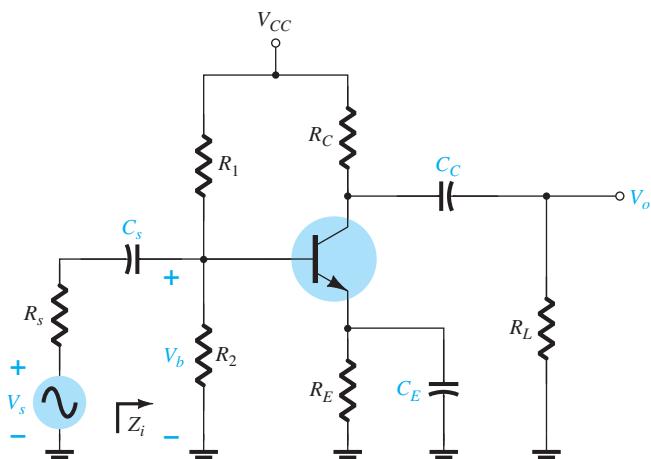


FIG. 9.32

Determining the effect of  $R_s$  on the low-frequency response of a BJT amplifier.

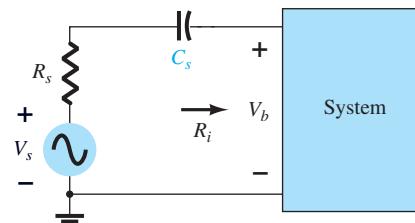


FIG. 9.33

Determining the effect of  $C_s$  on the low-frequency response.

Using the results of the last section it would appear we could simply find the total sum of the series resistors and plug it into Eq. (9.22). Doing so would result in the following equation for the cutoff frequency:

$$f_{L_s} = \frac{1}{2\pi(R_i + R_s)C_s} \quad (9.36)$$

However, it would be best to validate our assumption by first applying the voltage-divider rule in the following manner:

$$\frac{\mathbf{V}_b}{\mathbf{V}_s} = \frac{R_i \mathbf{V}_s}{R_s + R_i - jX_{C_s}} \quad (9.37)$$

The cutoff frequency defined by  $C_s$  can be determined by manipulating the above equation into a standard form, as demonstrated below.

Rewriting Eq. (9.37):

$$\begin{aligned} \frac{\mathbf{V}_b}{\mathbf{V}_s} &= \frac{R_i}{R_s + R_i - jX_{C_s}} = \frac{1}{1 + \frac{R_s}{R_i} - j\frac{X_{C_s}}{R_i}} \\ &= \frac{1}{\left(1 + \frac{R_s}{R_i}\right) \left[1 - j\frac{X_{C_s}}{R_i} \left(\frac{1}{1 + \frac{R_s}{R_i}}\right)\right]} = \frac{1}{\left(1 + \frac{R_s}{R_i}\right) \left(1 - j\frac{X_{C_s}}{R_i + R_s}\right)} \end{aligned}$$

The factor

$$\frac{X_{C_s}}{R_i + R_s} = \left(\frac{1}{2\pi f C_s}\right) \left(\frac{1}{R_i + R_s}\right) = \frac{1}{2\pi f (R_i + R_s) C_s}$$

Defining

$$f_{L_s} = \frac{1}{2\pi(R_i + R_s)C_s}$$

we have

$$\frac{\mathbf{V}_b}{\mathbf{V}_s} = \frac{1}{\left(1 + \frac{R_s}{R_i}\right) \left(1 - \frac{1}{1 - j(f_{L_s}/f)}\right)}$$

and finally

$$\mathbf{A}_v = \frac{\mathbf{V}_b}{\mathbf{V}_s} = \left[\frac{R_i}{R_i + R_s}\right] \left[\frac{1}{1 - j(f_{L_s}/f)}\right]$$

For the midband frequencies, the input network will appear as shown in Fig. 9.34.

so that

$$A_{v_{\text{mid}}} = \frac{\mathbf{V}_b}{\mathbf{V}_s} = \frac{R_i}{R_i + R_s} \quad (9.38)$$

and

$$\frac{A_v}{A_{v_{\text{mid}}}} = \frac{1}{1 - j(f_{L_s}/f)}$$

Noting the similarities with Eq. (9.23) the cutoff frequency is defined by  $f_{L_s}$  above and

$$f_{L_s} = \frac{1}{2\pi(R_s + R_i)C_s} \quad (9.39)$$

as assumed in the derivation of Eq. (9.36).

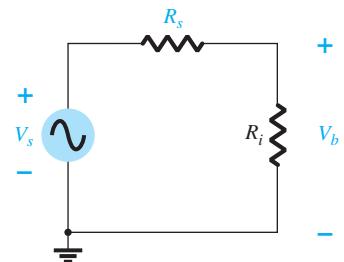
At  $f_{L_s}$ , the voltage  $V_o$  will be 70.7% of the midband value determined by Eq. (9.38), assuming the  $C_s$  is the only capacitive element controlling the low-frequency response.

**C<sub>c</sub>** Reviewing the analysis of Section 9.7 for the coupling capacitor  $C_C$ , we find that the derivation of the equation for the cutoff frequency remains the same. That is,

$$f_{L_C} = \frac{1}{2\pi(R_o + R_L)C_C} \quad (9.40)$$

**C<sub>E</sub>** Again, following the analysis of Section 9.7 for the same capacitor, we find that  $R_s$  will affect the resistance level substituted into the cutoff equation so that

$$f_{L_E} = \frac{1}{2\pi R_e C_E} \quad (9.41)$$



**FIG. 9.34**  
Determining the effect of  $R_s$  on the gain  $A_{v_s}$ .

with

$$R_e = R_E \left\| \left( \frac{R'_s}{\beta} + r_e \right) \right\| \text{ and } R'_s = R_s \left\| R_1 \right\| R_2$$

In total, therefore, the introduction of the resistance  $R_s$  reduced the cutoff frequency defined by  $C_s$  and raised the cutoff frequency defined by  $C_E$ . The cutoff frequency defined by  $C_C$  remained the same. It is also important to note that the gain can be severely affected by the loss in signal voltage across the source resistance. This last factor will be demonstrated in the next example.

### EXAMPLE 9.12

- Repeat the analysis of Example 9.11 but with a source resistance  $R_s$  of  $1\text{k}\Omega$ . The gain of interest will now be  $V_o/V_s$  rather than  $V_o/V_i$ . Compare results.
- Sketch the frequency response using a Bode plot.
- Verify the results using PSpice.

**Solution:** a. The dc conditions remain the same:

$$r_e = 15.76 \Omega \text{ and } \beta r_e = 1.576 \text{ k}\Omega$$

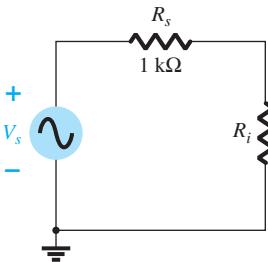
**Midband Gain**  $A_v = \frac{V_o}{V_i} = \frac{-R_C \parallel R_L}{r_e} \cong -90$  as before

The input impedance is given by

$$\begin{aligned} Z_i &= R_i = R_1 \parallel R_2 \parallel \beta r_e \\ &= 40 \text{ k}\Omega \parallel 10 \text{ k}\Omega \parallel 1.576 \text{ k}\Omega \\ &\cong 1.32 \text{ k}\Omega \end{aligned}$$

and from Fig. 9.35,

$$\begin{aligned} V_b &= \frac{R_i V_s}{R_i + R_s} \\ \frac{V_b}{V_s} &= \frac{R_i}{R_i + R_s} = \frac{1.32 \text{ k}\Omega}{1.32 \text{ k}\Omega + 1 \text{ k}\Omega} = 0.569 \\ A_{v_s} &= \frac{V_o}{V_s} = \frac{V_o}{V_i} \cdot \frac{V_b}{V_s} = (-90)(0.569) \\ &= \mathbf{-51.21} \end{aligned}$$



**FIG. 9.35**

Determining the effect of  $R_s$  on the gain  $A_{v_s}$ .

**C<sub>s</sub>**

$$R_i = R_1 \parallel R_2 \parallel \beta r_e = 40 \text{ k}\Omega \parallel 10 \text{ k}\Omega \parallel 1.576 \text{ k}\Omega \cong 1.32 \text{ k}\Omega$$

$$\begin{aligned} f_{L_s} &= \frac{1}{2\pi(R_s + R_i)C_s} = \frac{1}{(6.28)(1 \text{ k}\Omega + 1.32 \text{ k}\Omega)(10 \mu\text{F})} \\ f_{L_s} &\cong 6.86 \text{ Hz vs. } 12.06 \text{ Hz without } R_s \end{aligned}$$

**C<sub>c</sub>**

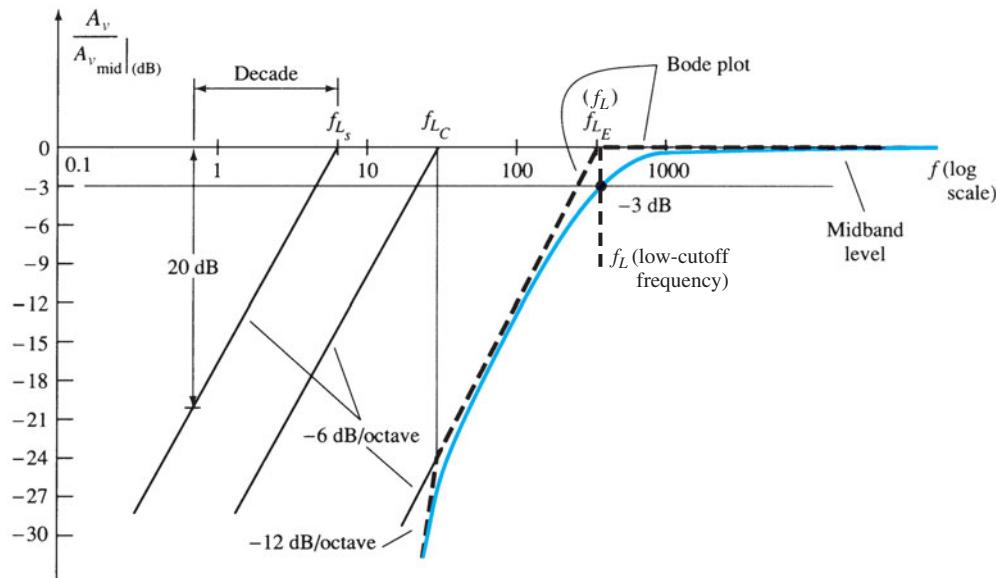
$$\begin{aligned} f_{L_C} &= \frac{1}{2\pi(R_C + R_L)C_C} \\ &= \frac{1}{(6.28)(4 \text{ k}\Omega + 2.2 \text{ k}\Omega)(1 \mu\text{F})} \\ &\cong \mathbf{25.68 \text{ Hz}} \text{ as before} \end{aligned}$$

**C<sub>E</sub>**

$$\begin{aligned} R'_s &= R_s \parallel R_1 \parallel R_2 = 1 \text{ k}\Omega \parallel 40 \text{ k}\Omega \parallel 10 \text{ k}\Omega \cong 0.889 \text{ k}\Omega \\ R_e &= R_E \left\| \left( \frac{R'_s}{\beta} + r_e \right) \right\| = 2 \text{ k}\Omega \left\| \left( \frac{0.889 \text{ k}\Omega}{100} + 15.76 \Omega \right) \right\| \\ &= 2 \text{ k}\Omega \parallel (8.89 \Omega + 15.76 \Omega) = 2 \text{ k}\Omega \parallel 24.65 \Omega \cong 24.35 \Omega \\ f_{L_E} &= \frac{1}{2\pi R_e C_E} = \frac{1}{(6.28)(24.35 \Omega)(20 \mu\text{F})} = \frac{10^6}{3058.36} \\ &\cong \mathbf{327 \text{ Hz}} \text{ vs. } 87.13 \text{ Hz without } R_s. \end{aligned}$$

The net result is a severe reduction in overall gain (almost 43%) but a corresponding reduction in the lower cutoff frequency. Recall that the highest of the low cutoff frequencies will determine the overall low cutoff frequency for the amplifier. The results point out that the internal series resistance can have a very strong impact on the midband gain, but on the other side of the coin it can improve the overall bandwidth. In this case it is clear that the loss in gain far outweighs any gain in bandwidth.

- b. It was mentioned earlier that dB plots are usually normalized by dividing the voltage gain  $A_v$  by the magnitude of the midband gain. For Fig. 9.32, the magnitude of the midband gain is 51.21, and naturally the ratio  $|A_v/A_{v\text{mid}}|$  will be 1 in the midband region. The result is a 0-dB asymptote in the midband region as shown in Fig. 9.36. Defining  $f_{L_E}$  as our lower cutoff frequency  $f_L$ , we can draw an asymptote at  $-6 \text{ dB/octave}$  as shown in Fig. 9.36 to form the Bode plot and our envelope for the actual response. At  $f_L$ , the actual curve is  $-3 \text{ dB}$  down from the midband level as defined by the  $0.707A_{v\text{mid}}$  level, permitting a sketch of the actual frequency response curve as shown in Fig. 9.36. A  $-6 \text{ dB/octave}$  asymptote was drawn at each frequency defined in the analysis above to demonstrate clearly that it is  $f_{L_E}$  for this network that will determine the  $-3 \text{ dB}$  point. It is not until about  $-24 \text{ dB}$  that  $f_{L_C}$  begins to affect the shape of the envelope. The magnitude plot shows that the slope of the resultant asymptote is the sum of the asymptotes having the same sloping direction in the same frequency interval. Note in Fig. 9.36 that the slope has dropped to  $-12 \text{ dB/octave}$  for frequencies less than  $f_{L_C}$  and could drop to  $-18 \text{ dB/octave}$  if the three defined cutoff frequencies of Fig. 9.36 were closer together. Using Eq. (9.9), the cutoff frequency for the low-frequency region is about 325 Hz.



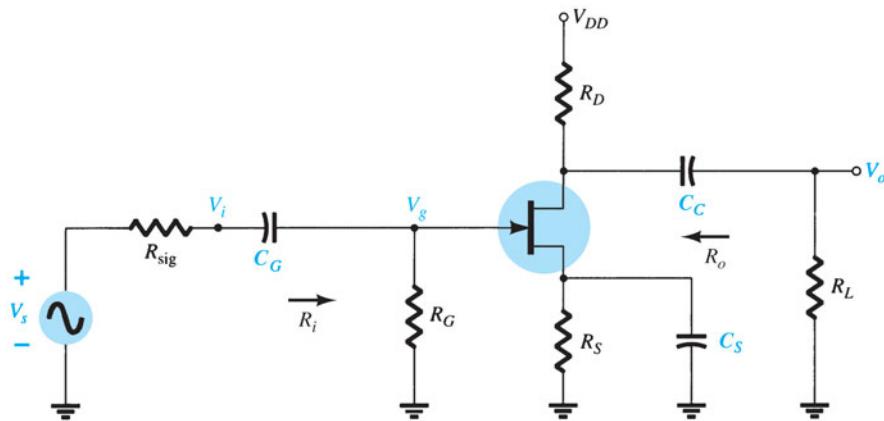
**FIG. 9.36**  
Low-frequency plot for the network of Example 9.12.

- c. The PSpice solution can be found in Section 9.15.

Keep in mind as we proceed to the next section that the analysis of this section is not limited to the networks of Figs. 9.25 and 9.32. For any transistor configuration it is simply necessary to isolate each  $RC$  combination formed by a capacitive element and determine the break frequencies. The resulting frequencies will then determine whether there is a strong interaction between capacitive elements in determining the overall response and which element will have the greatest effect on establishing the lower cutoff frequency. In fact, the analysis of the next section will parallel this section as we determine the low-cutoff frequencies for the FET amplifier.

## 9.9 LOW-FREQUENCY RESPONSE—FET AMPLIFIER

The analysis of the FET amplifier in the low-frequency region will be quite similar to that of the BJT amplifier of Section 9.7. There are again three capacitors of primary concern as appearing in the network of Fig. 9.37:  $C_G$ ,  $C_C$ , and  $C_S$ . Although Fig. 9.37

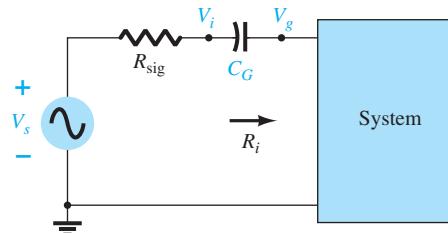


**FIG. 9.37**  
Capacitive elements that affect the low-frequency response of a JFET amplifier.

will be used to establish the fundamental equations, the procedure and conclusions can be applied to any FET configuration. Most of the equations for impedance levels can be found in Table 8.2.

**C<sub>G</sub>** For the coupling capacitor between the source and the active device, the ac equivalent network is as shown in Fig. 9.38. The cutoff frequency determined by  $C_G$  is

$$f_{L_G} = \frac{1}{2\pi(R_{\text{sig}} + R_i)C_G} \quad (9.42)$$

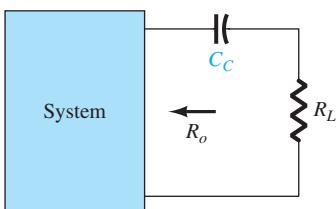


**FIG. 9.38**  
Determining the effect of  $C_G$  on the low-frequency response.

which is an exact match of Eq. (9.39). For the network of Fig. 9.37,

$$R_i = R_G \quad (9.43)$$

Typically,  $R_G \gg R_{\text{sig}}$ , and the lower cutoff frequency is determined primarily by  $R_G$  and  $C_G$ . The fact that  $R_G$  is so large permits a relatively low level of  $C_G$  while maintaining a low cutoff frequency level for  $f_{L_G}$ .



**FIG. 9.39**

Determining the effect of  $C_C$  on the low-frequency response.

**C<sub>C</sub>** For the coupling capacitor between the active device and the load the network of Fig. 9.39 results, which is also an exact match of Fig. 9.27. The resulting cutoff frequency is

$$f_{L_C} = \frac{1}{2\pi(R_o + R_L)C_C} \quad (9.44)$$

For the network of Fig. 9.37,

$$R_o = R_D \| r_d \quad (9.45)$$

**C<sub>s</sub>** For the source capacitor  $C_S$ , the resistance level of importance is defined by Fig. 9.40. The cutoff frequency is defined by

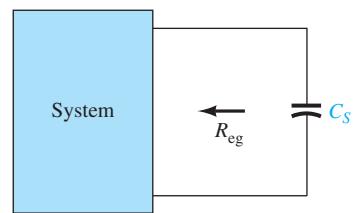
$$f_{L_s} = \frac{1}{2\pi R_{eq} C_S} \quad (9.46)$$

For Fig. 9.37, the resulting value of  $R_{eq}$  is

$$R_{eq} = \frac{R_S}{1 + R_S(1 + g_m r_d)/(r_d + R_D \| R_L)} \quad (9.47)$$

which for  $r_d \equiv \infty \Omega$  becomes

$$R_{eq} = R_S \| \frac{1}{g_m} \quad r_d \equiv \infty \Omega \quad (9.48)$$

**FIG. 9.40**

Determining the effect of  $C_S$  on the low-frequency response.

### EXAMPLE 9.13

- Determine the lower cutoff frequency for the network of Fig. 9.37 using the following parameters:  
 $C_G = 0.01 \mu\text{F}$ ,  $C_C = 0.5 \mu\text{F}$ ,  $C_S = 2 \mu\text{F}$   
 $R_{sig} = 10 \text{ k}\Omega$ ,  $R_G = 1 \text{ M}\Omega$ ,  $R_D = 4.7 \text{ k}\Omega$ ,  $R_S = 1 \text{ k}\Omega$ ,  $R_L = 2.2 \text{ k}\Omega$   
 $I_{DSS} = 8 \text{ mA}$ ,  $V_P = -4 \text{ V}$ ,  $r_d = \infty \Omega$ ,  $V_{DD} = 20 \text{ V}$
- Sketch the frequency response using a Bode plot.
- Verify the results of part (b) using PSpice.
- Perform a complete analysis of the network of Fig. 9.37 using Multisim.

#### Solution:

- DC analysis: Plotting the transfer curve of  $I_D = I_{DSS}(1 - V_{GS}/V_P)^2$  and superimposing the curve defined by  $V_{GS} = -I_D R_S$  results in an intersection at  $V_{GS_Q} = -2 \text{ V}$  and  $I_{D_Q} = 2 \text{ mA}$ . In addition,

$$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(8 \text{ mA})}{4 \text{ V}} = 4 \text{ mS}$$

$$g_m = g_{m0} \left( 1 - \frac{V_{GS_Q}}{V_P} \right) = 4 \text{ mS} \left( 1 - \frac{-2 \text{ V}}{-4 \text{ V}} \right) = 2 \text{ mS}$$

**C<sub>G</sub>** Eq. (9.36):  $f_{L_G} = \frac{1}{2\pi(R_{sig} + R_i)C_G} = \frac{1}{2\pi(10 \text{ k}\Omega + 1 \text{ M}\Omega)(0.01 \mu\text{F})} \cong 15.8 \text{ Hz}$

**C<sub>C</sub>** Eq. (9.38):  $f_{L_C} = \frac{1}{2\pi(R_o + R_L)C_C} = \frac{1}{2\pi(4.7 \text{ k}\Omega + 2.2 \text{ k}\Omega)(0.5 \mu\text{F})} \cong 46.13 \text{ Hz}$

**C<sub>S</sub>**  $R_{eq} = R_S \| \frac{1}{g_m} = 1 \text{ k}\Omega \| \frac{1}{2 \text{ mS}} = 1 \text{ k}\Omega \| 0.5 \text{ k}\Omega = 333.33 \Omega$

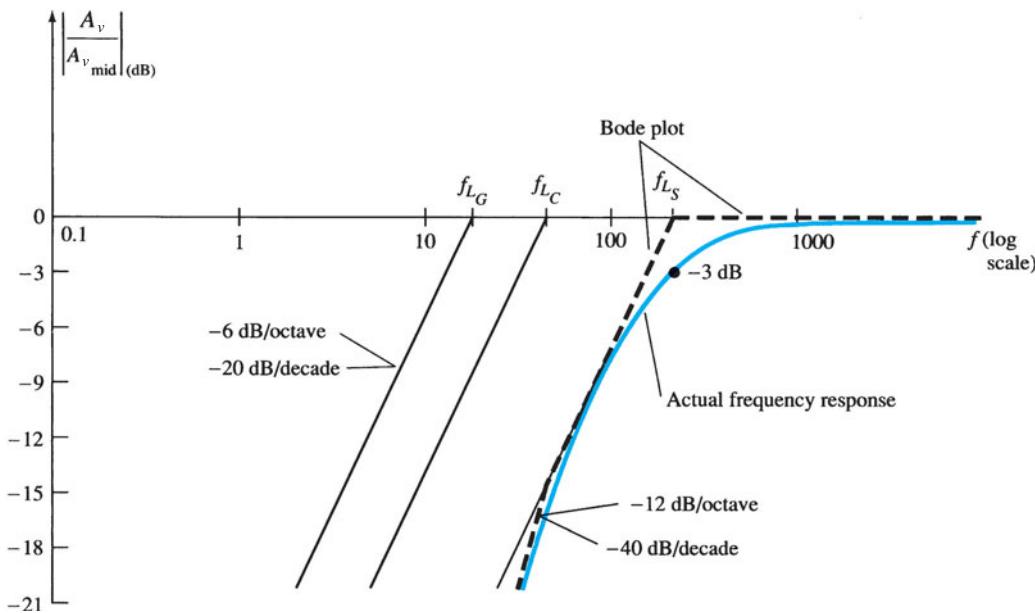
Eq. (9.40):  $f_{L_s} = \frac{1}{2\pi R_{eq} C_S} = \frac{1}{2\pi(333.33 \Omega)(2 \mu\text{F})} = 238.73 \text{ Hz}$

Because  $f_{L_s}$  is the largest of the three cutoff frequencies, it defines the low-cutoff frequency for the network of Fig. 9.37.

- The midband gain of the system is determined by

$$\begin{aligned} A_{v_{mid}} &= \frac{V_o}{V_i} = -g_m(R_D \| R_L) = -(2 \text{ mS})(4.7 \text{ k}\Omega \| 2.2 \text{ k}\Omega) \\ &= -(2 \text{ mS})(1.499 \text{ k}\Omega) \\ &\cong -3 \end{aligned}$$

Using the midband gain to normalize the response for the network of Fig. 9.37 results in the frequency plot of Fig. 9.41.



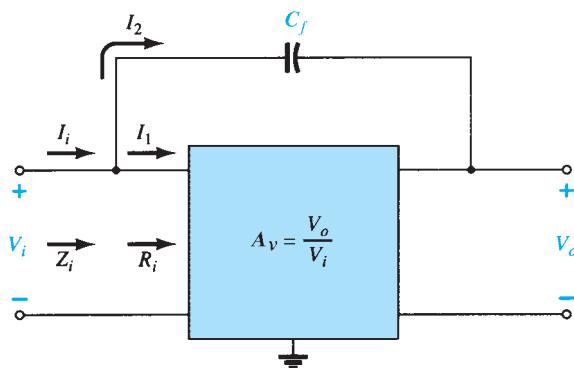
**FIG. 9.41**  
Low-frequency response for the JFET configuration of Example 9.13.

c. and d. The computer solutions can be found in Section 9.15.

## 9.10 MILLER EFFECT CAPACITANCE

In the high-frequency region, the capacitive elements of importance are the interelectrode (between-terminals) capacitances internal to the active device and the wiring capacitance between leads of the network. The large capacitors of the network that controlled the low-frequency response are all replaced by their short-circuit equivalent due to their very low reactance levels.

For *inverting* amplifiers (phase shift of  $180^\circ$  between input and output, resulting in a negative value for  $A_v$ ), the input and output capacitance is increased by a capacitance level sensitive to the interelectrode capacitance between the input and output terminals of the device and the gain of the amplifier. In Fig. 9.42, this “feedback” capacitance is defined by  $C_f$ .



**FIG. 9.42**  
Network employed in the derivation of an equation for the Miller input capacitance.

Applying Kirchhoff's current law gives

$$I_i = I_1 + I_2$$

Using Ohm's law yields

$$I_i = \frac{V_i}{Z_i}, \quad I_1 = \frac{V_i}{R_i}$$

and

$$I_2 = \frac{V_i - V_o}{X_{C_f}} = \frac{V_i - A_v V_i}{X_{C_f}} = \frac{(1 - A_v) V_i}{X_{C_f}}$$

Substituting, we obtain

$$\frac{V_i}{Z_i} = \frac{V_i}{R_i} + \frac{(1 - A_v) V_i}{X_{C_f}}$$

and

$$\frac{1}{Z_i} = \frac{1}{R_i} + \frac{1}{X_{C_f}/(1 - A_v)}$$

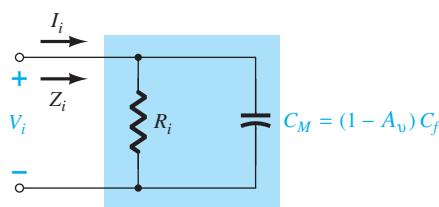
but

$$\frac{X_{C_f}}{1 - A_v} = \underbrace{\frac{1}{\omega(1 - A_v) C_f}}_{C_M} = X_{C_M}$$

and

$$\frac{1}{Z_i} = \frac{1}{R_i} + \frac{1}{X_{C_M}}$$

establishing the equivalent network of Fig. 9.43. The result is an equivalent input impedance to the amplifier of Fig. 9.44 that includes the same  $R_i$  that we dealt with in previous chapters, with the addition of a feedback capacitor magnified by the gain of the amplifier. Any interelectrode capacitance at the input terminals to the amplifier will simply be added in parallel with the elements of Fig. 9.43.



**FIG. 9.43**  
Demonstrating the effect of the Miller effect capacitance.

In general, therefore, the Miller effect input capacitance is defined by

$$C_{M_i} = (1 - A_v) C_f \quad (9.49)$$

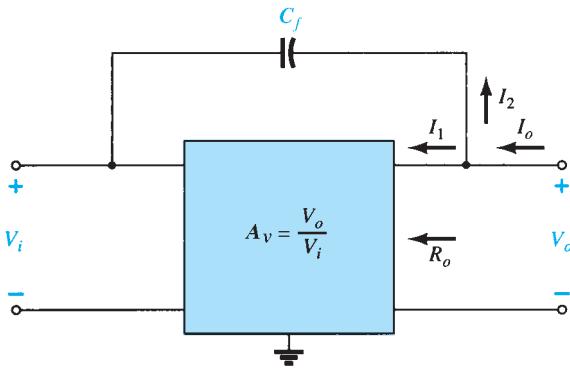
This shows us that:

**For any inverting amplifier, the input capacitance will be increased by a Miller effect capacitance sensitive to the gain of the amplifier and the interelectrode (parasitic) capacitance between the input and output terminals of the active device.**

The dilemma of an equation such as Eq. (9.49) is that at high frequencies the gain  $A_v$  will be a function of the level of  $C_{M_i}$ . However, because the maximum gain is the midband value, using the midband value will result in the highest level of  $C_{M_i}$  and the worst-case scenario. In general, therefore, the midband value is typically employed for  $A_v$  in Eq. (9.49).

The reason for the constraint that the amplifier be of the inverting variety is now more apparent when one examines Eq. (9.49). A positive value for  $A_v$  would result in a negative capacitance (for  $A_v > 1$ ).

The Miller effect will also increase the level of output capacitance, which must also be considered when the high-frequency cutoff is determined. In Fig. 9.44, the parameters of



**FIG. 9.44**  
Network employed in the derivation of an equation for the Miller output capacitance.

importance to determine the output Miller effect are in place. Applying Kirchhoff's current law results in

$$I_o = I_1 + I_2$$

$$\text{with } I_1 = \frac{V_o}{R_o} \quad \text{and} \quad I_2 = \frac{V_o - V_i}{X_{C_f}}$$

The resistance  $R_o$  is usually sufficiently large to permit ignoring the first term of the equation compared to the second term and assuming that

$$I_o \cong \frac{V_o - V_i}{X_{C_f}}$$

Substituting  $V_i = V_o/A_v$  from  $A_v = V_o/V_i$  results in

$$I_o = \frac{V_o - V_o/A_v}{X_{C_f}} = \frac{V_o(1 - 1/A_v)}{X_{C_f}}$$

$$\text{and } \frac{I_o}{V_o} = \frac{1 - 1/A_v}{X_{C_f}}$$

$$\text{or } \frac{V_o}{I_o} = \frac{X_{C_f}}{1 - 1/A_v} = \frac{1}{\omega C_f(1 - 1/A_v)} = \frac{1}{\omega C_{M_o}}$$

resulting in the following equation for the Miller output capacitance:

$$C_{M_o} = \left(1 - \frac{1}{A_v}\right) C_f \quad (9.50)$$

For the usual situation where  $A_v \gg 1$ , Eq. (9.50) reduces to

$$C_{M_o} \cong C_f \quad |_{A_v \gg 1} \quad (9.51)$$

Examples of the use of Eq. (9.50) appear in the next two sections as we investigate the high-frequency responses of BJT and FET amplifiers.

**For noninverting amplifiers such as the common-base and emitter-follower configurations, the Miller effect capacitance is not a contributing concern for high-frequency applications.**

## 9.11 HIGH-FREQUENCY RESPONSE—BJT AMPLIFIER

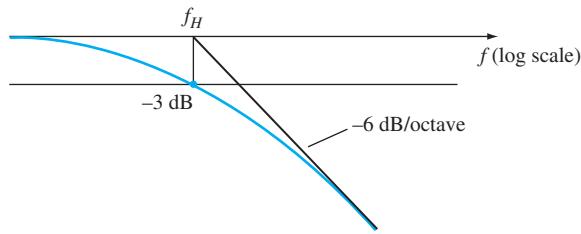
**At the high-frequency end, there are two factors that define the  $-3\text{-dB}$  cutoff point: the network capacitance (parasitic and introduced) and the frequency dependence of  $h_{fe}(\beta)$ .**

## Network Parameters

In the high-frequency region, the  $RC$  network of concern has the configuration appearing in Fig. 9.45. At increasing frequencies, the reactance  $X_C$  will decrease in magnitude, resulting in a shorting effect across the output and a decrease in gain. The derivation leading to the corner frequency for this  $R_C$  configuration follows along similar lines to that encountered for the low-frequency region. The most significant difference is in the following general form of  $A_v$ :

$$A_v = \frac{1}{1 + j(f/f_H)} \quad (9.52)$$

This results in a magnitude plot such as shown in Fig. 9.46 that drops off at 6 dB/octave with increasing frequency. Note that  $f_H$  is in the denominator of the frequency ratio rather than the numerator as occurred for  $f_L$  in Eq. (9.23).



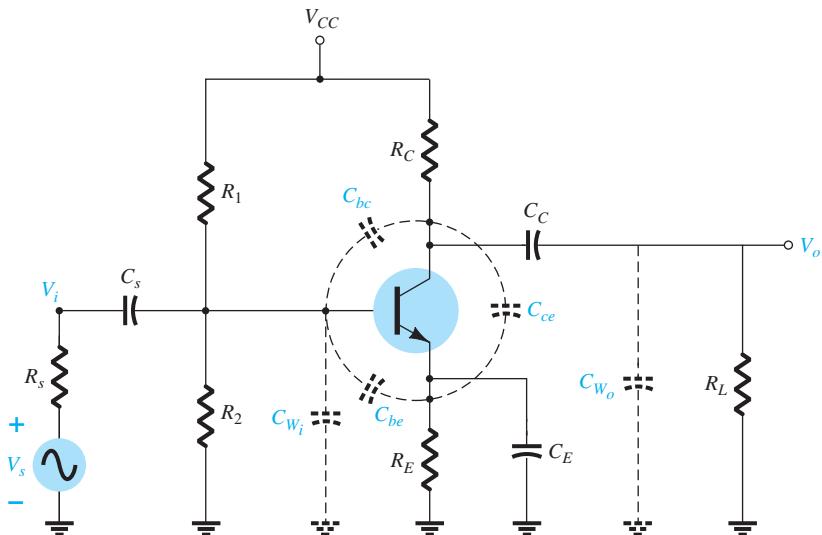
**FIG. 9.45**

RC combination that will define a high-cutoff frequency.

**FIG. 9.46**

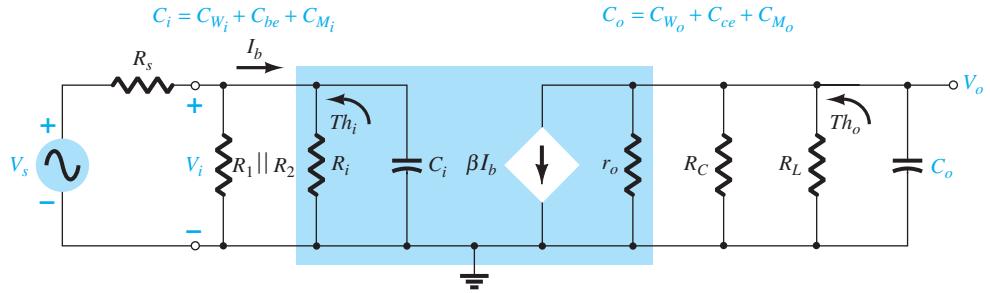
Asymptotic plot as defined by Eq. (9.52).

In Fig. 9.47, the various parasitic capacitances ( $C_{be}$ ,  $C_{bc}$ ,  $C_{ce}$ ) of the transistor are included with the wiring capacitances ( $C_{Wi}$ ,  $C_{Wo}$ ) introduced during construction. The high-frequency equivalent model for the network of Fig. 9.47 appears in Fig. 9.48. Note the absence of the capacitors  $C_s$ ,  $C_C$ , and  $C_E$ , which are all assumed to be in the short-circuit state at these frequencies. The capacitance  $C_i$  includes the input wiring capacitance  $C_{Wi}$ , the transition capacitance  $C_{be}$ , and the Miller capacitance  $C_{Mi}$ . The capacitance  $C_o$  includes the output wiring capacitance  $C_{Wo}$ , the parasitic capacitance  $C_{ce}$ , and the output Miller capacitance  $C_{Mo}$ . In general, the capacitance  $C_{be}$  is the largest of the parasitic capacitances, with  $C_{ce}$  the smallest. In fact, most specification sheets simply provide the levels of  $C_{be}$  and  $C_{bc}$  and do not include  $C_{ce}$  unless it will affect the response of a particular type of transistor in a specific area of application.



**FIG. 9.47**

Network of Fig. 9.25 with the capacitors that affect the high-frequency response.



**FIG. 9.48**

High-frequency ac equivalent model for the network of Fig. 9.47.

Determining the Thévenin equivalent circuit for the input and output networks of Fig. 9.48 results in the configurations of Fig. 9.49. For the input network, the  $-3\text{-dB}$  frequency is defined by

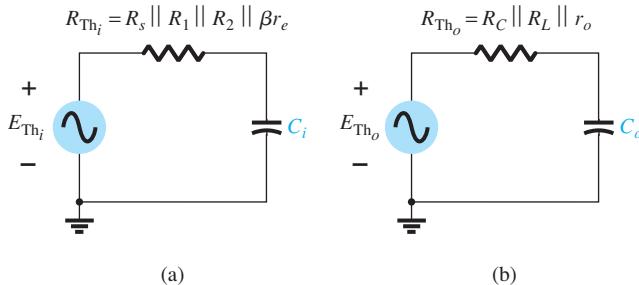
$$f_{H_i} = \frac{1}{2\pi R_{Th_i} C_i} \quad (9.53)$$

with

$$R_{Th_i} = R_s \| R_1 \| R_2 \| \beta r_e \quad (9.54)$$

and

$$C_i = C_{W_i} + C_{be} + C_{M_i} = C_{W_i} + C_{be} + (1 - A_v)C_{bc} \quad (9.55)$$



**FIG. 9.49**  
Thévenin circuits for the input and output networks of the network of Fig. 9.48.

At very high frequencies, the effect of  $C_i$  is to reduce the total impedance of the parallel combination of  $R_1$ ,  $R_2$ ,  $\beta r_e$ , and  $C_i$  in Fig. 9.48. The result is a reduced level of voltage across  $C_i$ , a reduction in  $I_b$ , and a gain for the system.

For the output network,

$$f_{H_o} = \frac{1}{2\pi R_{Th_o} C_o} \quad (9.56)$$

with

$$R_{Th_o} = R_C \| R_L \| r_o \quad (9.57)$$

and

$$C_o = C_{W_o} + C_{ce} + C_{M_o} \quad (9.58)$$

or

$$C_o = C_{W_o} + C_{ce} + (1 - 1/A_v)C_{bc}$$

For  $A_v$  large (typical):

$$1 \gg 1/A_v$$

and

$$C_o \approx C_{W_o} + C_{ce} + C_{bc} \quad (9.59)$$

At very high frequencies, the capacitive reactance of  $C_o$  will decrease and consequently reduce the total impedance of the output parallel branches of Fig. 9.48. The net result is that  $V_o$  will also decline toward zero as the reactance  $X_C$  becomes smaller. The frequencies

$f_{H_i}$  and  $f_{H_o}$  will each define a  $-6\text{-dB/octave}$  asymptote such as depicted in Fig. 9.46. If the parasitic capacitors were the only elements to determine the high-cutoff frequency, the lowest frequency would be the determining factor. However, the decrease in  $h_{fe}$  (or  $\beta$ ) with frequency must also be considered as to whether its break frequency is lower than  $f_{H_i}$  or  $f_{H_o}$ .

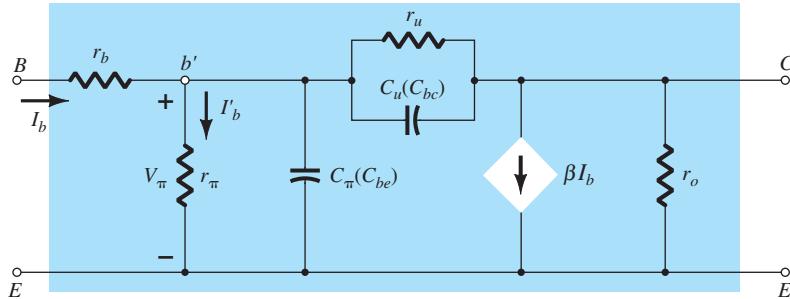
### **$h_{fe}$ (or $\beta$ ) Variation**

The variation of  $h_{fe}$  (or  $\beta$ ) with frequency will approach, with some degree of accuracy, the following relationship:

$$h_{fe} = \frac{h_{fe\text{mid}}}{1 + j(f/f_\beta)} \quad (9.60)$$

The use of  $h_{fe}$  rather than  $\beta$  in some of this descriptive material is due primarily to the fact that manufacturers typically use the hybrid parameters when covering this issue in their specification sheets and so on.

The only undefined quantity,  $f_\beta$ , is determined by a set of parameters employed in the *hybrid  $\pi$*  or *Giacoleotto* model of Fig. 9.50 introduced in Section 5.22. The resistance  $r_b$  includes the base contact, base bulk, and base spreading resistance. The first is due to the actual connection to the base. The second includes the resistance from the external terminal to the active region of the transistors, and the last is the actual resistance within the active base region. The resistances  $r_\pi$ ,  $r_o$ , and  $r_u$  are the resistances between the indicated terminals when the device is in the active region. The same is true for the capacitances  $C_{bc}$  and  $C_{be}$ , although the former is a transition capacitance, whereas the latter is a diffusion capacitance. A more detailed explanation of the frequency dependence of each can be found in a number of readily available texts.



**FIG. 9.50**

*Giacoleotto (or hybrid  $\pi$ ) high-frequency transistor small-signal ac equivalent circuit.*

If we remove the base resistance  $r_b$ , the base-to-collector resistance  $r_u$ , and all the parasitic capacitances, the result is an ac equivalent circuit that matches the small-signal equivalent for the common-emitter configuration used in Chapter 5. The base-to-emitter resistance  $r_\pi$  is  $\beta r_e$  and the output resistance  $r_o$  is simply a value provided through the hybrid parameter  $h_{oe}$ . The controlled source is also  $\beta I_b$  as used in Chapter 5. However, if we include the resistance  $r_u$  (usually quite large) between base and collector, there is a feedback loop between output and input circuits to match the contribution of  $h_{re}$  for the hybrid equivalent circuit. Recall from Chapter 5 that the feedback term is normally inconsequential for most applications, but if a particular application puts it at the forefront, then the model of Fig. 9.50 will bring it into play. The resistance  $r_u$  is a result of the fact that the base current is somewhat sensitive to the collector-to-base voltage. Because the base-to-emitter voltage is linearly related to the base current through Ohm's law and the output voltage is equal to the difference between the base-to-emitter voltage and collector-to-base voltage, we can conclude that the base current is sensitive to the changes in output voltage as revealed by the hybrid parameter  $h_{re}$ .

In terms of these parameters,

$$f_\beta(\text{often appearing as } f_{h_{fe}}) = \frac{1}{2\pi r_\pi(C_\pi + C_u)} \quad (9.61)$$

or, because  $r_\pi = \beta r_e = h_{fe_{mid}} r_e$ ,

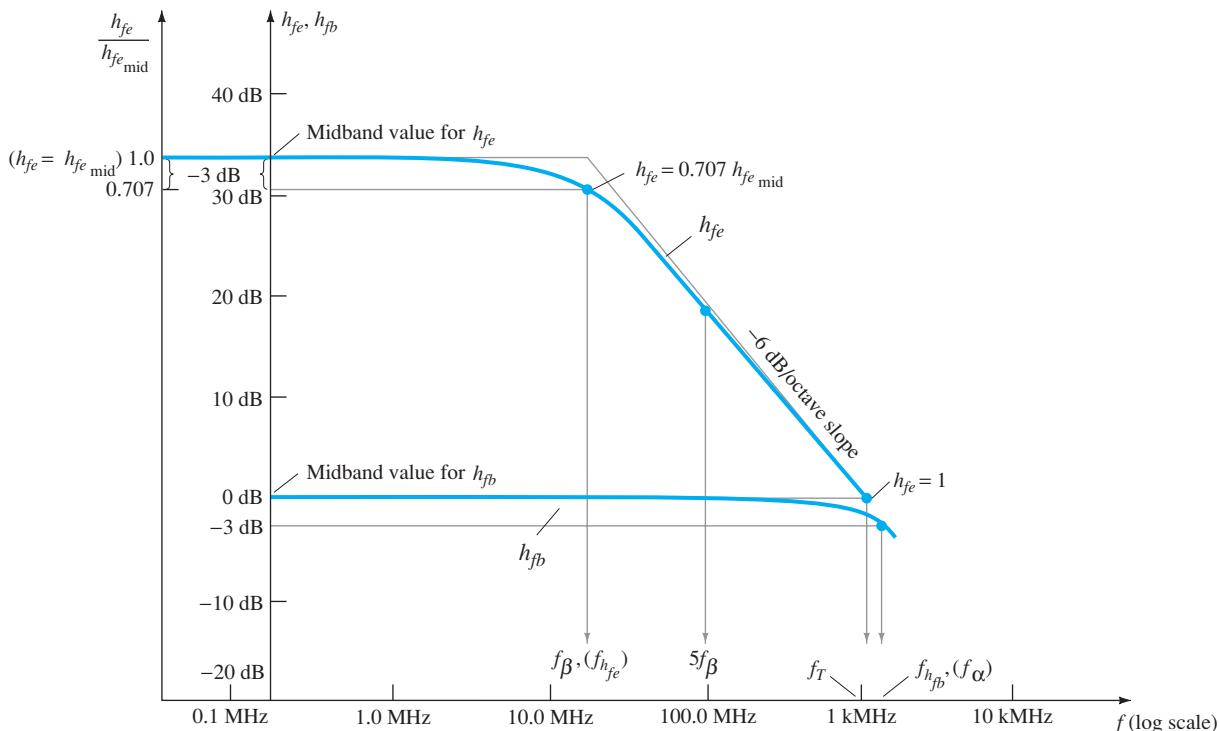
$$f_\beta = \frac{1}{h_{fe_{mid}}} \frac{1}{2\pi r_e(C_\pi + C_u)} \quad (9.62)$$

or

Equation (9.62) clearly reveals that because  $r_e$  is a function of the network design:

**f<sub>β</sub> is a function of the bias configuration.**

The basic format of Eq. (9.60) is exactly the same as Eq. (9.52) if we extract the multiplying factor  $h_{fe_{mid}}$ , revealing that  $h_{fe}$  will drop off from its midband value with a 6-dB/octave slope as shown in Fig. 9.51. The same figure has a plot of  $h_{fb}$  (or  $\alpha$ ) versus frequency. Note the small change in  $h_{fb}$  for the chosen frequency range, revealing that the common-base configuration displays improved high-frequency characteristics over the common-emitter configuration. Recall also the absence of the Miller effect capacitance due to the noninverting characteristics of the common-base configuration. For this very reason, common-base high-frequency parameters rather than common-emitter parameters are often specified for a transistor—especially those designed specifically to operate in the high-frequency regions.



**FIG. 9.51**  
 $h_{fe}$  and  $h_{fb}$  versus frequency in the high-frequency region.

The following equation permits a direct conversion for determining  $f_\beta$  if  $f_\alpha$  and  $\alpha$  are specified:

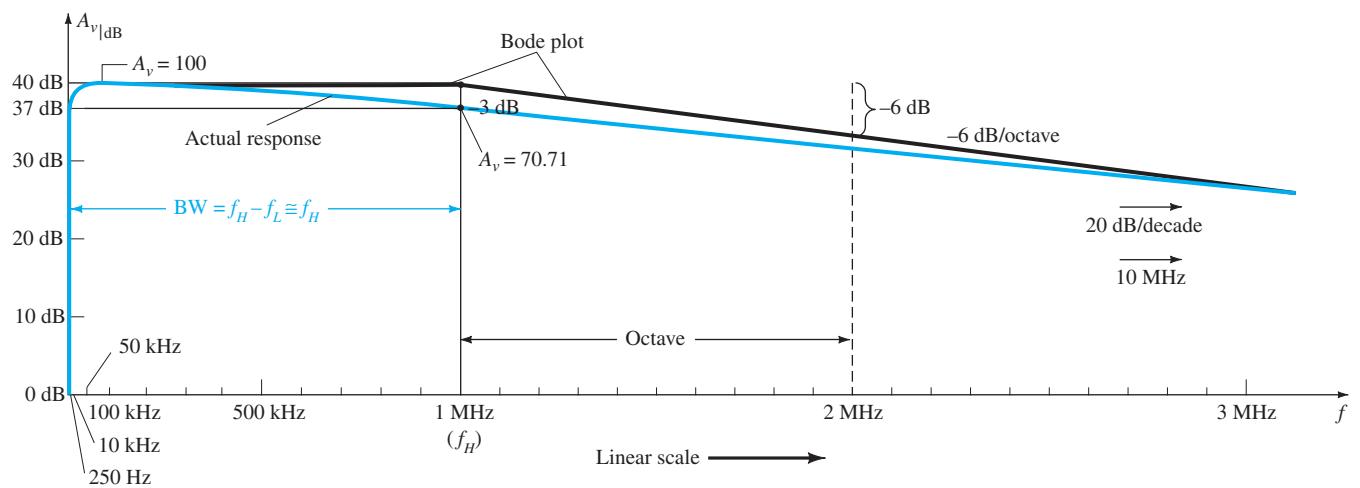
$$f_\beta = f_\alpha(1 - \alpha) \quad (9.63)$$

### Gain-Bandwidth Product

There is a **Figure of Merit** applied to amplifiers called the **Gain-Bandwidth Product (GBP)** that is commonly used to initiate the design process of an amplifier. It provides

important information about the relationship between the gain of the amplifier and the expected operating frequency range.

In Fig. 9.52 the frequency response of an amplifier with a gain of 100, a low cutoff frequency of 250 Hz, and an upper cutoff frequency of 1 MHz has been plotted on a linear scale rather than the typical log scale. Note that because a linear scale was chosen for the horizontal axis it is impossible to show the low cutoff frequency, and the curve appears as essentially a straight vertical line at  $f = 0$  Hz. Because  $f = 0$  Hz represents a dc situation,



**FIG. 9.52**  
Plotting the dB gain of an amplifier in a linear-frequency plot.

**the gain at the low end of an amplifier is often called the DC gain.**

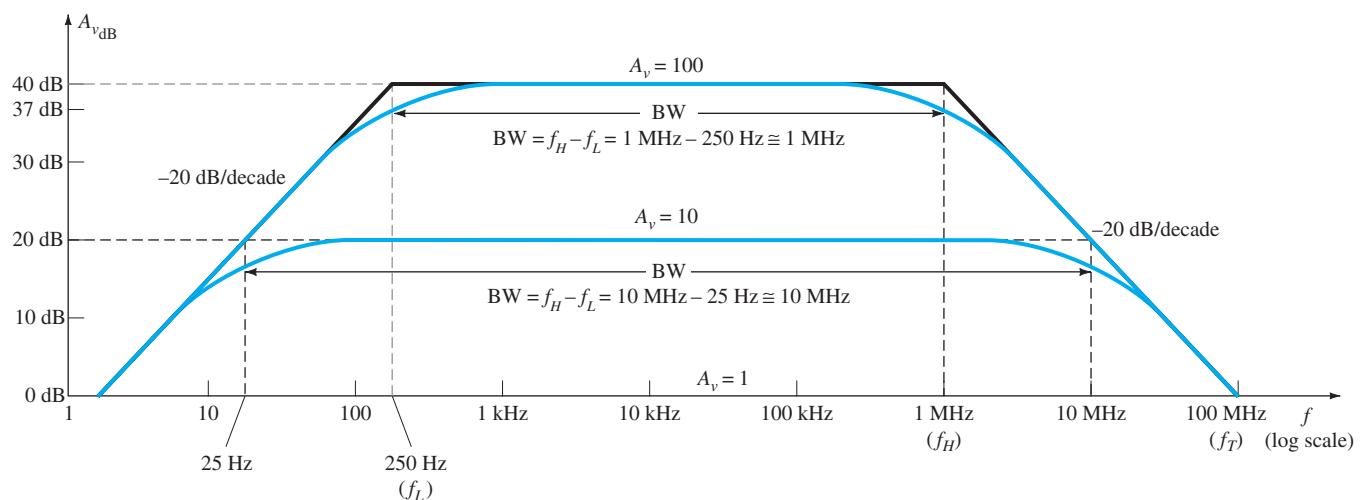
Note also that the use of a linear horizontal axis results in a very slow decline in gain with frequency past the breakpoint. It would take many pages to show the full frequency plot at the high end.

It is also clear from Fig. 9.52 that the bandwidth is essentially defined by the upper cutoff frequency because the low cutoff frequency is so small in comparison.

If Fig. 9.52 were plotted using a log scale for the horizontal axis, the plot of Fig. 9.53 would result.

The low end is expanded and the frequency response at the upper end is complete with a boundary defined by the 20-dB drop per decade slope. The upper breakpoint frequency is labeled  $f_H$  with the lower breakpoint frequency labeled  $f_L$ .

At  $A_v = A_{v_{mid}} = 100$  the bandwidth as shown in Fig. 9.53 is approximately 1 MHz.



**FIG. 9.53**  
Finding the bandwidth at two different gain levels.

The gain-bandwidth product is

$$\text{GBP} = A_{v_{\text{mid}}} \text{BW} \quad (9.64)$$

which for this example is

$$\text{GBP} = (100)(1 \text{ MHz}) = 100 \text{ MHz}$$

At  $A_v = 10$ ,  $20 \log_{10} 10 = 20$  and the bandwidth as shown in Fig. 9.53 is approximately 10 MHz.

The resulting gain-bandwidth product is now

$$\text{GBP} = (10)(10 \text{ MHz}) = 100 \text{ MHz}$$

*In fact, at any level of gain the product of the two remains a constant.*

At  $A_v = 1$  or  $A_v|_{dB} = 0$  bandwidth is defined as  $f_T$  in Fig. 9.53.

In general,

*the frequency  $f_T$  is called the unity-gain frequency and is always equal to the product of the midband gain of an amplifier and the bandwidth at any level of gain.*

That is,

$$f_T = A_{v_{\text{mid}}} f_H \quad (\text{Hz}) \quad (9.65a)$$

The result is that the expected bandwidth of an amplifier for any level of gain can be found quite directly. Consider an amplifier with a given  $f_T$  of 120 MHz. At a gain of 80 the expected  $f_H$  or bandwidth is  $f_T/A_{v_{\text{mid}}} = 120 \text{ MHz}/80 = 1.5 \text{ MHz}$ . At a gain of 60 the bandwidth is  $120 \text{ MHz}/60 = 2 \text{ MHz}$  and so on—a very useful tool.

For transistors themselves, where a voltage gain has not been defined by a configuration, specification sheets will provide a value of  $f_T$  that relates to the transistor only. That is,

$$f_T = h_{f_e_{\text{mid}}} f_\beta \quad (\text{Hz}) \quad (9.65b)$$

The dB plot would appear as shown in Fig. 9.49.

The general equation for the  $h_{f_e}$  variation with frequency is defined by Eq. 9.60. For the amplifier it is defined by

$$A_v = \frac{A_{v_{\text{mid}}}}{1 + j(f/f_H)} \quad (9.66)$$

Note that in each case the frequency  $f_H$  defines the corner frequency.

Substituting Eq. (9.62) for  $f_\beta$  in Eq. (9.65) gives

$$f_T = h_{f_e_{\text{mid}}} \frac{1}{2\pi h_{f_e_{\text{mid}}} r_e (C_\pi + C_u)}$$

and

$$f_T \cong \frac{1}{2\pi r_e (C_\pi + C_u)} \quad (9.67)$$

**EXAMPLE 9.14** Use the network of Fig. 9.47 with the same parameters as in Example 9.12, that is,

$$R_s = 1 \text{ k}\Omega, R_1 = 40 \text{ k}\Omega, R_2 = 10 \text{ k}\Omega, R_E = 2 \text{ k}\Omega, R_C = 4 \text{ k}\Omega, R_L = 2.2 \text{ k}\Omega$$

$$C_s = 10 \text{ }\mu\text{F}, C_C = 1 \text{ }\mu\text{F}, C_E = 20 \text{ }\mu\text{F}$$

$$h_{f_e} = 100, r_o = \infty \text{ }\Omega, V_{CC} = 20 \text{ V}$$

with the addition of

$$C_\pi(C_{be}) = 36 \text{ pF}, C_u(C_{bc}) = 4 \text{ pF}, C_{ce} = 1 \text{ pF}, C_{W_i} = 6 \text{ pF}, C_{W_o} = 8 \text{ pF}$$

- Determine  $f_{H_i}$  and  $f_{H_o}$ .
- Find  $f_\beta$  and  $f_T$ .

- c. Sketch the frequency response for the low- and high-frequency regions using the results of Example 9.12 and the results of parts (a) and (b).
- d. Obtain the PSpice response for the full frequency spectrum and compare with the results of part (c).

**Solution:**

- a. From Example 9.12:

$$\beta r_e = 1.576 \text{ k}\Omega, \quad A_{v_{\text{mid}}}(\text{amplifier—not including effects of } R_s) = -90$$

and  $R_{\text{Th}_i} = R_s \| R_1 \| R_2 \| \beta r_e = 1 \text{ k}\Omega \| 40 \text{ k}\Omega \| 10 \text{ k}\Omega \| 1.576 \text{ k}\Omega \cong 0.57 \text{ k}\Omega$

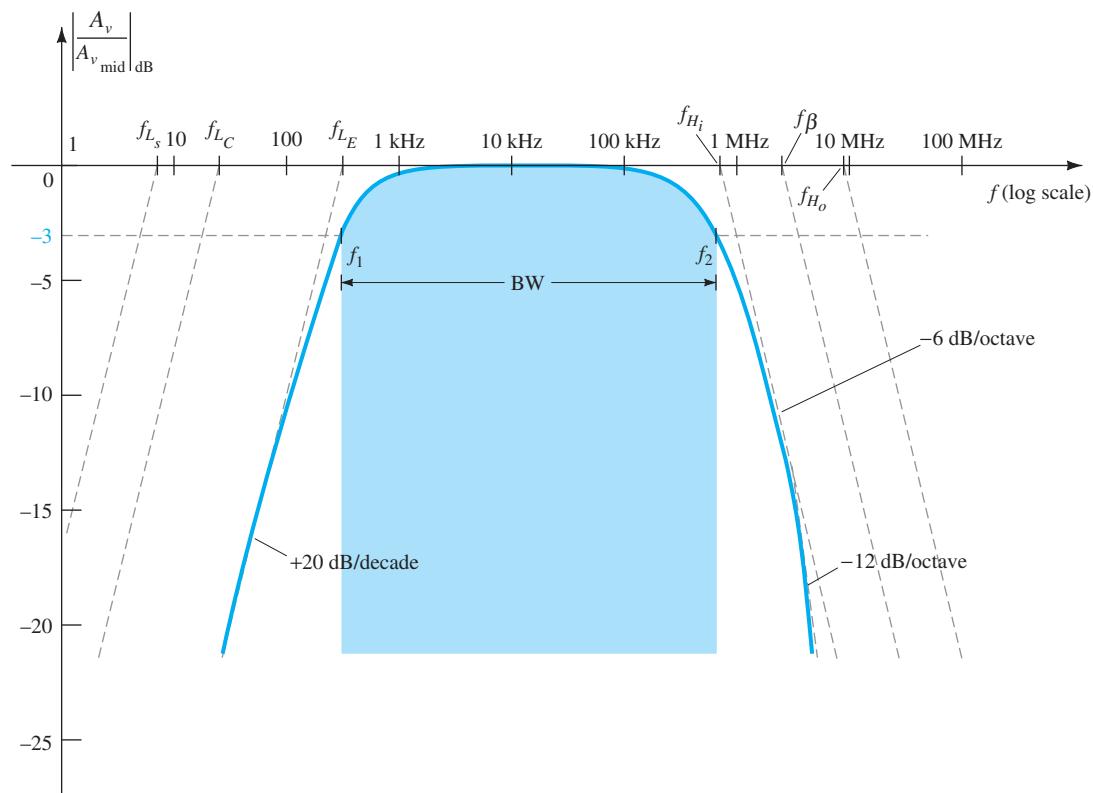
with  $C_i = C_{W_i} + C_{be} + (1 - A_v)C_{bc}$   
 $= 6 \text{ pF} + 36 \text{ pF} + [1 - (-90)]4 \text{ pF}$   
 $= 406 \text{ pF}$

$$f_{H_i} = \frac{1}{2\pi R_{\text{Th}_i} C_i} = \frac{1}{2\pi(0.57 \text{ k}\Omega)(406 \text{ pF})}$$
 $= 687.73 \text{ kHz}$

$$R_{\text{Th}_o} = R_C \| R_L = 4 \text{ k}\Omega \| 2.2 \text{ k}\Omega = 1.419 \text{ k}\Omega$$

$$C_o = C_{W_o} + C_{ce} + C_{M_o} = 8 \text{ pF} + 1 \text{ pF} + \left(1 - \frac{1}{-90}\right)4 \text{ pF}$$
 $= 13.04 \text{ pF}$

$$f_{H_o} = \frac{1}{2\pi R_{\text{Th}_o} C_o} = \frac{1}{2\pi(1.419 \text{ k}\Omega)(13.04 \text{ pF})}$$
 $= 8.6 \text{ MHz}$



**FIG. 9.54**  
Full frequency response for the network of Fig. 9.47.

b. Applying Eq. (9.63) gives

$$\begin{aligned} f_\beta &= \frac{1}{2\pi h_{fe_{mid}} r_e (C_{be} + C_{bc})} \\ &= \frac{1}{2\pi(100)(15.76 \Omega)(36 \text{ pF} + 4 \text{ pF})} = \frac{1}{2\pi(100)(15.76 \Omega)(40 \text{ pF})} \\ &= \mathbf{2.52 \text{ MHz}} \end{aligned}$$

$$\begin{aligned} f_T &= h_{fe_{mid}} f_\beta = (100)(2.52 \text{ MHz}) \\ &= \mathbf{252 \text{ MHz}} \end{aligned}$$

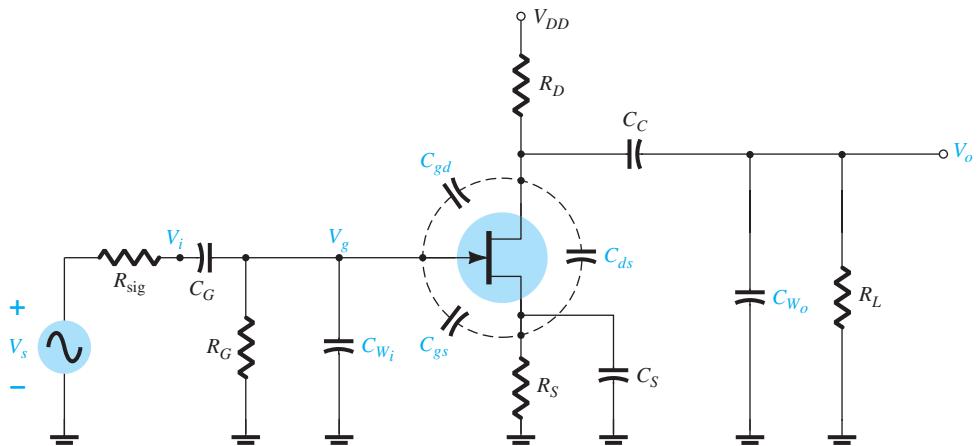
c. See Fig. 9.54. The corner frequency  $f_{H_i}$  will determine the high cutoff frequency and the bandwidth of the amplifier. The upper cutoff frequency is very close to 600 kHz.

d. The PSpice analysis will appear in Section 9.15.

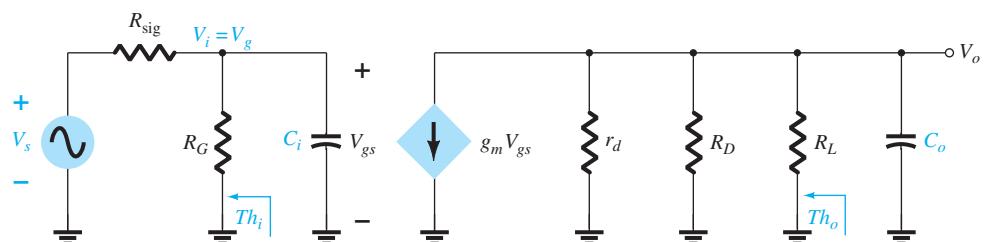
## 9.12 HIGH-FREQUENCY RESPONSE—FET AMPLIFIER

The analysis of the high-frequency response of the FET amplifier will proceed in a very similar manner to that encountered for the BJT amplifier. As shown in Fig. 9.55, there are interelectrode and wiring capacitances that will determine the high-frequency characteristics of the amplifier. The capacitors  $C_{gs}$  and  $C_{gd}$  typically vary from 1 pF to 10 pF, whereas the capacitance  $C_{ds}$  is usually quite a bit smaller, ranging from 0.1 pF to 1 pF.

Because the network of Fig. 9.55 is an inverting amplifier, a Miller effect capacitance will appear in the high-frequency ac equivalent network appearing in Fig. 9.56. At high frequencies,  $C_i$  will approach a short-circuit equivalent and  $V_{gs}$  will drop in value and reduce the overall gain. At frequencies where  $C_o$  approaches its short-circuit equivalent, the parallel output voltage  $V_o$  will drop in magnitude.



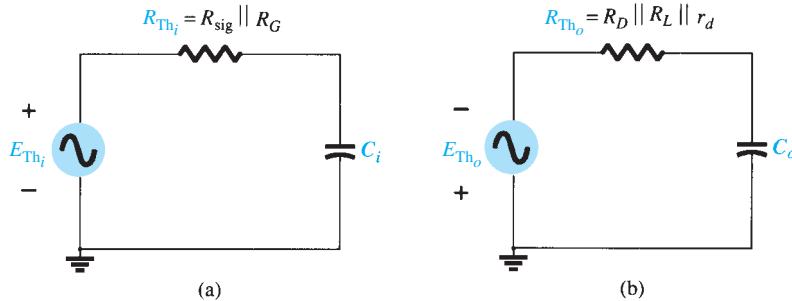
**FIG. 9.55**  
Capacitive elements that affect the high-frequency response of a JFET amplifier.



**FIG. 9.56**  
High-frequency ac equivalent circuit for Fig. 9.55.

The cutoff frequencies defined by the input and output circuits can be obtained by first finding the Thévenin equivalent circuits for each section as shown in Fig. 9.57. For the input circuit,

$$f_{H_i} = \frac{1}{2\pi R_{Th_i} C_i} \quad (9.68)$$



**FIG. 9.57**

The Thévenin equivalent circuits for: (a) the input circuit and (b) the output circuit.

and

$$R_{Th_i} = R_{sig} \parallel R_G \quad (9.69)$$

with

$$C_i = C_{W_i} + C_{gs} + C_{M_i} \quad (9.70)$$

and

$$C_{M_i} = (1 - A_v)C_{gd} \quad (9.71)$$

for the output circuit,

$$f_{H_o} = \frac{1}{2\pi R_{Th_o} C_o} \quad (9.72)$$

with

$$R_{Th_o} = R_D \parallel R_L \parallel r_d \quad (9.73)$$

and

$$C_o = C_{W_o} + C_{ds} + C_{M_o} \quad (9.74)$$

and

$$C_{M_o} = \left(1 - \frac{1}{A_v}\right)C_{gd} \quad (9.75)$$

### EXAMPLE 9.15

- a. Determine the high-cutoff frequencies for the network of Fig. 9.55 using the same parameters as Example 9.13:

$$C_G = 0.01 \mu F, \quad C_C = 0.5 \mu F, \quad C_S = 2 \mu F$$

$$R_{sig} = 10 k\Omega, \quad R_G = 1 M\Omega, \quad R_D = 4.7 k\Omega, \quad R_S = 1 k\Omega, \quad R_L = 2.2 k\Omega$$

$$I_{DSS} = 8 mA, \quad V_P = -4 V, \quad r_d = \infty \Omega, \quad V_{DD} = 20 V$$

with the addition of

$$C_{gd} = 2 pF, \quad C_{gs} = 4 pF, \quad C_{ds} = 0.5 pF, \quad C_{W_i} = 5 pF, \quad C_{W_o} = 6 pF$$

- b. Obtain a PSpice response for the full frequency range and note whether it supports the conclusions of Example 9.13 and the calculations above.

**Solution:**

a.  $R_{Th_i} = R_{sig} \parallel R_G = 10 \text{ k}\Omega \parallel 1 \text{ M}\Omega = 9.9 \text{ k}\Omega$

From Example 9.13,  $A_v = -3$ . We have

$$\begin{aligned} C_i &= C_{W_i} + C_{gs} + (1 - A_v)C_{gd} \\ &= 5 \text{ pF} + 4 \text{ pF} + (1 + 3)2 \text{ pF} \\ &= 9 \text{ pF} + 8 \text{ pF} \\ &= 17 \text{ pF} \end{aligned}$$

$$\begin{aligned} f_{H_1} &= \frac{1}{2\pi R_{Th_i} C_i} \\ &= \frac{1}{2\pi(9.9 \text{ k}\Omega)(17 \text{ pF})} = 945.67 \text{ kHz} \end{aligned}$$

$$\begin{aligned} R_{Th_o} &= R_D \parallel R_L \\ &= 4.7 \text{ k}\Omega \parallel 2.2 \text{ k}\Omega \\ &\approx 1.5 \text{ k}\Omega \end{aligned}$$

$$C_o = C_{W_o} + C_{ds} + C_{M_o} = 6 \text{ pF} + 0.5 \text{ pF} + \left(1 - \frac{1}{-3}\right)2 \text{ pF} = 9.17 \text{ pF}$$

$$f_{H_o} = \frac{1}{2\pi(1.5 \text{ k}\Omega)(9.17 \text{ pF})} = 11.57 \text{ MHz}$$

The results above clearly indicate that the input capacitance with its Miller effect capacitance will determine the upper cutoff frequency. This is typically the case due to the smaller value of  $C_{ds}$  and the resistance levels encountered in the output circuit.

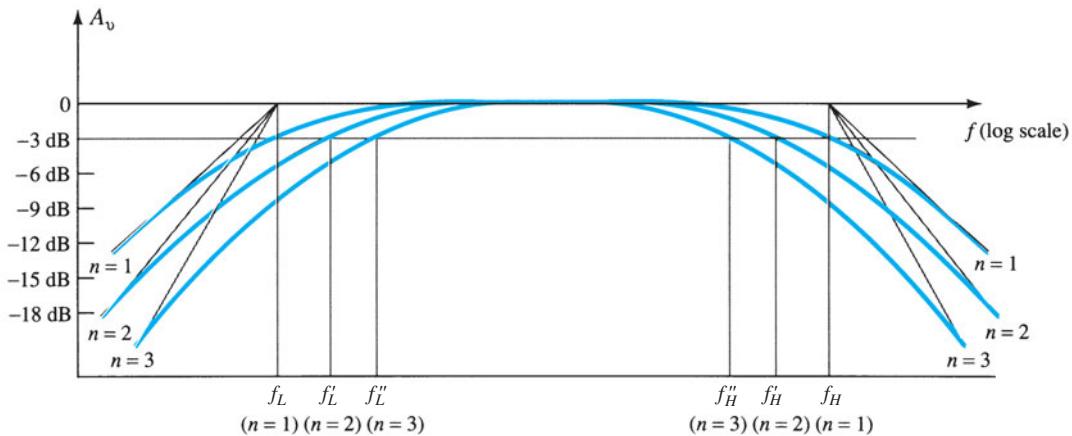
b. The PSpice analysis will appear in Section 9.15.

Even though the analysis of the last few sections has been limited to two configurations, the general procedure for determining the cutoff frequencies should support the analysis of any other transistor configuration. Keep in mind that the Miller capacitance is limited to inverting amplifiers and that  $f_\alpha$  is significantly greater than  $f_\beta$  if the common-base configuration is encountered. There is a great deal more literature on the analysis of single-stage amplifiers that goes beyond the coverage of this chapter. However, the content of this chapter should provide a firm foundation for any analysis of frequency effects.

### 9.13 MULTISTAGE FREQUENCY EFFECTS

For a second transistor stage connected directly to the output of a first stage, there will be a significant change in the overall frequency response. In the high-frequency region, the output capacitance  $C_o$  must now include the wiring capacitance ( $C_{W_i}$ ), parasitic capacitance ( $C_{be}$ ), and Miller capacitance ( $C_{M_i}$ ) of the following stage. Furthermore, there will be additional low-frequency cutoff levels due to the second stage, which will further reduce the overall gain of the system in this region. For each additional stage, the upper cutoff frequency will be determined primarily by the stage having the lowest cutoff frequency. The low-frequency cutoff is primarily determined by that stage having the highest low-frequency cutoff frequency. Obviously, therefore, one poorly designed stage can offset an otherwise well-designed cascaded system.

The effect of increasing the number of *identical* stages can be clearly demonstrated by considering the situations indicated in Fig. 9.58. In each case, the upper and lower cutoff frequencies of each of the cascaded stages are identical. For a single stage, the cutoff frequencies are  $f_L$  and  $f_H$  as indicated. For two identical stages in cascade, the drop-off rate in the high- and low-frequency regions has increased to  $-12 \text{ dB/octave}$  or  $-40 \text{ dB/decade}$ . At  $f_L$  and  $f_H$ , therefore, the decibel drop is now  $-6 \text{ dB}$  rather than the defined band frequency gain level of  $-3 \text{ dB}$ . The  $-3\text{-dB}$  point has shifted to  $f'_L$  and  $f'_H$  as indicated, with a resulting drop in the bandwidth. A  $-18\text{-dB/octave}$  or  $-60\text{-dB/decade}$  slope will result for a three-stage system of identical stages with the indicated reduction in bandwidth ( $f''_L$  and  $f''_H$ ).



**FIG. 9.58**  
Effect of an increased number of stages on the cutoff frequencies and the bandwidth.

Assuming identical stages, we can determine an equation for each band frequency as a function of the number of stages ( $n$ ) in the following manner: For the low-frequency region,

$$A_{v_{\text{low, (overall)}}} = A_{v_{1_{\text{low}}}} A_{v_{2_{\text{low}}}} A_{v_{3_{\text{low}}}} \cdots A_{v_{n_{\text{low}}}}$$

but because all stages are identical,  $A_{v_{1_{\text{low}}}} = A_{v_{2_{\text{low}}}} = \text{etc.}$ , and

$$A_{v_{\text{low, (overall)}}} = (A_{v_{1_{\text{low}}}})^n$$

$$\text{or } \frac{A_{v_{\text{low}}}}{A_{v_{\text{mid}}}} (\text{overall}) = \left( \frac{A_{v_{\text{low}}}}{A_{v_{\text{mid}}}} \right)^n = \frac{1}{(1 - jf_L/f)^n}$$

Setting the magnitude of this result equal to  $1/\sqrt{2}$  (-3 dB level) results in

$$\frac{1}{\sqrt{[1 + (f_L/f'_L)^2]^n}} = \frac{1}{\sqrt{2}}$$

$$\text{or } \left\{ \left[ 1 + \left( \frac{f_L}{f'_L} \right)^2 \right]^{1/2} \right\}^n = \left\{ \left[ 1 + \left( \frac{f_L}{f'_L} \right)^2 \right]^n \right\}^{1/2} = (2)^{1/2}$$

$$\text{so that } \left[ 1 + \left( \frac{f_L}{f'_L} \right)^2 \right]^n = 2$$

$$\text{and } 1 + \left( \frac{f_L}{f'_L} \right)^2 = 2^{1/n}$$

with the result that

$$f'_L = \frac{f_L}{\sqrt{2^{1/n} - 1}} \quad (9.76)$$

In a similar manner, it can be shown that for the high-frequency region,

$$f'_H = (\sqrt{2^{1/n} - 1})f_H \quad (9.77)$$

Note the presence of the same factor  $\sqrt{2^{1/n} - 1}$  in each equation. The magnitude of this factor for various values of  $n$  is listed below.

$n$	$\sqrt{2^{1/n} - 1}$
2	0.64
3	0.51
4	0.43
5	0.39

For  $n = 2$ , consider that the upper cutoff frequency  $f'_H = 0.64f_H$ , or 64% of the value obtained for a single stage, whereas  $f'_L = (1/0.64)f_L = 1.56f_L$ . For  $n = 3$ ,  $f'_H = 0.51f_H$ , or approximately one-half the value of a single stage, and  $f'_L = (1/0.51)f_L = 1.96f_L$ , or approximately *twice* the single-stage value.

For the *RC*-coupled transistor amplifier, if  $f_H = f_\beta$ , or if they are close enough in magnitude for both to affect the upper 3-dB frequency, the number of stages must be increased by a factor of 2 when determining  $f'_H$  due to the increased number of factors  $1/(1 + jf/f_x)$ .

A decrease in bandwidth is not always associated with an increase in the number of stages if the midband gain can remain fixed and independent of the number of stages. For instance, if a single-stage amplifier produces a gain of 100 with a bandwidth of 10,000 Hz, the resulting gain-bandwidth product is  $10^2 \times 10^4 = 10^6$ . For a two-stage system the same gain can be obtained by having two stages with a gain of 10 ( $10 \times 10 = 100$ ). The bandwidth of each stage would then increase by a factor of 10 to 100,000 due to the lower gain requirement and fixed gain-bandwidth product of  $10^6$ . Of course, the design must be such as to permit the increased bandwidth and establish the lower gain level.

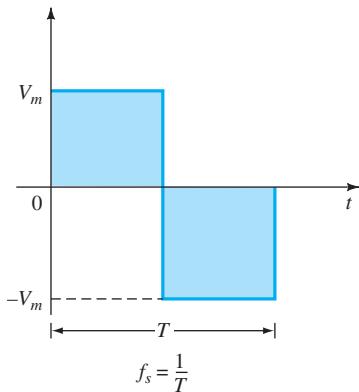
## 9.14 SQUARE-WAVE TESTING

A sense for the frequency response of an amplifier can be determined experimentally by applying a square-wave signal to the amplifier and noting the output response. The shape of the output waveform will reveal whether the high or low frequencies are being properly amplified. Using *square-wave testing* is significantly less time consuming than applying a series of sinusoidal signals at different frequencies and magnitudes to test the frequency response of the amplifier.

The reason for choosing a square-wave signal for the testing process is best described by examining the *Fourier series expansion* of a square wave composed of a series of sinusoidal components of different magnitudes and frequencies. The summation of all the terms of the series will result in the original waveform. In other words, even though a waveform may not be sinusoidal, it can be reproduced by a series of sinusoidal terms of different frequencies and magnitudes.

The Fourier series expansion for the square wave of Fig. 9.59 is

$$v = \frac{4}{\pi} V_m \left( \underbrace{\sin 2\pi f_s t}_{\text{fundamental}} + \underbrace{\frac{1}{3} \sin 2\pi(3f_s)t}_{\text{third harmonic}} + \underbrace{\frac{1}{5} \sin 2\pi(5f_s)t}_{\text{fifth harmonic}} + \underbrace{\frac{1}{7} \sin 2\pi(7f_s)t}_{\text{seventh harmonic}} + \cdots + \underbrace{\frac{1}{9} \sin 2\pi(9f_s)t}_{\text{ninth harmonic}} + \cdots + \underbrace{\frac{1}{n} \sin 2\pi(nf_s)t}_{\text{nth harmonic}} \right) \quad (9.78)$$



**FIG. 9.59**  
Square wave.

The first term of the series is called the *fundamental* term and in this case has the same frequency,  $f_s$ , as the square wave. The next term has a frequency equal to three times the fundamental and is referred to as the *third harmonic*. Its magnitude is one-third the magnitude of the fundamental term. The frequencies of the succeeding terms are odd multiples of the fundamental term, and the magnitude decreases with each higher harmonic. Figure 9.58 demonstrates how the summation of terms of a Fourier series can result in a nonsinusoidal waveform. The generation of the square wave of Fig. 9.59 would require an infinite number of terms. However, the summation of just the fundamental term and the third harmonic in Fig. 9.60a clearly results in a waveform that is beginning to take on the appearance of a square wave. Including the fifth and seventh harmonics as in Fig. 9.60b takes us a step closer to the waveform of Fig. 9.59.

Because the ninth harmonic has a magnitude greater than 10% of the fundamental term [ $\frac{1}{9}(100\%) = 11.1\%$ ], the terms from the fundamental term through the ninth harmonic are the major contributors to the Fourier series expansion of the square-wave function. It is therefore reasonable to assume that if the application of a square wave of a particular frequency results in a nice clean square wave at the output, then the terms from the fundamental through the ninth harmonic are being amplified without visual distortion by the amplifier. For instance, if an audio amplifier with a bandwidth of 20 kHz (audio range is from 20 Hz to 20 kHz) is to be tested, the frequency of the applied signal should be at least  $20 \text{ kHz}/9 = 2.22 \text{ kHz}$ .

If the response of an amplifier to an applied square wave is an undistorted replica of the input, the frequency response (or BW) of the amplifier is obviously sufficient for the applied frequency. If the response is as shown in Fig. 9.61a and b, the low frequencies are not being amplified properly and the low cutoff frequency has to be investigated. If the waveform has the appearance of Fig. 9.61c and d, the high-frequency components are not receiving sufficient amplification and the high-cutoff frequency (or BW) has to be reviewed.

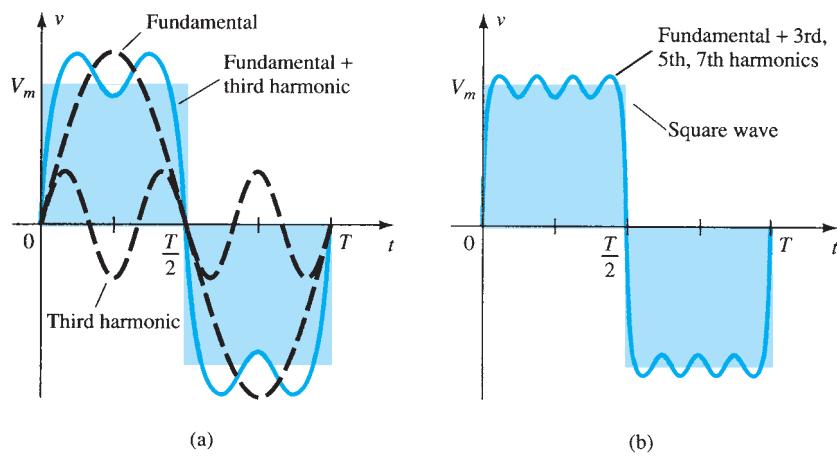


FIG. 9.60

Harmonic content of a square wave.

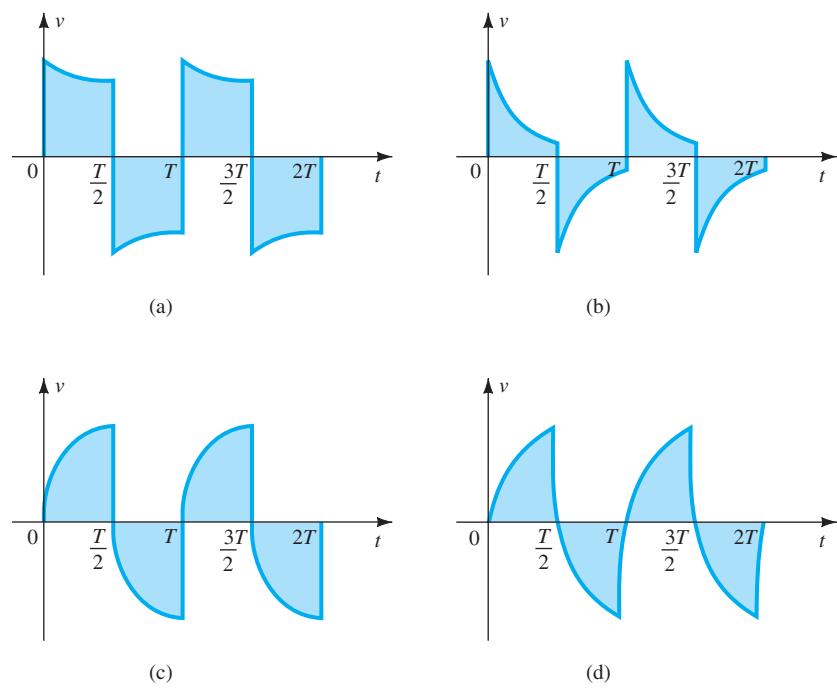


FIG. 9.61

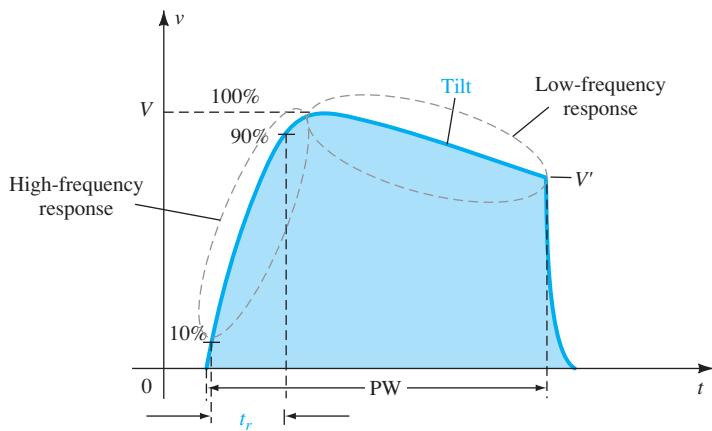
(a) Poor low-frequency response; (b) very poor low-frequency response; (c) poor high-frequency response; (d) very poor high-frequency response.

The actual high-cutoff frequency (or BW) can be determined from the output waveform by carefully measuring the rise time defined between 10% and 90% of the peak value, as shown in Fig. 9.62. Substituting into the following equation will provide the upper cutoff frequency, and because  $BW = f_{H_i} - f_{L_o} \cong f_{H_i}$ , the equation also provides an indication of the BW of the amplifier:

$$BW \cong f_{H_i} = \frac{0.35}{t_r} \quad (9.79)$$

The low-cutoff frequency can be determined from the output response by carefully measuring the tilt of Fig. 9.62 and substituting into one of the following equations:

$$\% \text{ tilt} = P\% = \frac{V - V'}{V} \times 100\% \quad (9.80)$$



**FIG. 9.62**  
Defining the rise time and tilt of a square wave response.

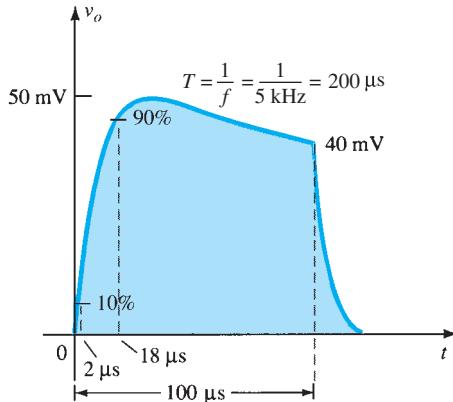
$$\text{tilt} = P = \frac{V - V'}{V} \quad (\text{decimal form}) \quad (9.81)$$

The low-cut-off frequency is then determined from

$$f_{L_o} = \frac{P}{\pi} f_s \quad (9.82)$$

**EXAMPLE 9.16** The application of a 1-mV, 5-kHz square wave to an amplifier resulted in the output waveform of Fig. 9.63.

- Write the Fourier series expansion for the square wave through the ninth harmonic.
- Determine the bandwidth of the amplifier.
- Calculate the low-cut-off frequency.



**FIG. 9.63**  
Example 9.16.

**Solution:**

$$\begin{aligned} \text{a. } v_i &= \frac{4 \text{ mV}}{\pi} \left( \sin 2\pi (5 \times 10^3)t + \frac{1}{3} \sin 2\pi(15 \times 10^3)t + \frac{1}{5} \sin 2\pi(25 \times 10^3)t \right. \\ &\quad \left. + \frac{1}{7} \sin 2\pi(35 \times 10^3)t + \frac{1}{9} \sin 2\pi(45 \times 10^3)t \right) \end{aligned}$$

$$\text{b. } t_r = 18 \mu\text{s} - 2 \mu\text{s} = 16 \mu\text{s}$$

$$\text{BW} \cong \frac{0.35}{t_r} = \frac{0.35}{16 \mu\text{s}} = 21,875 \text{ Hz} \cong 4.4f_s$$

$$c. P = \frac{V - V'}{V} = \frac{50 \text{ mV} - 40 \text{ mV}}{50 \text{ mV}} = 0.2$$

$$f_{L_o} = \frac{P}{\pi} f_s = \left( \frac{0.2}{\pi} \right) (5 \text{ kHz}) = 318.31 \text{ Hz}$$

## 9.15 SUMMARY

### Important Conclusions and Concepts

1. The logarithm of a number gives the **power to which the base must be brought to obtain the same number**. If the base is 10, it is referred to as the **common logarithm**; if the base is  $e = 2.71828\dots$ , it is called the **natural logarithm**.
2. Because the decibel rating of any piece of equipment is a **comparison between levels**, a reference level must be selected for each area of application. For audio systems the reference level is generally accepted as **1 mW**. When using voltage levels to determine the gain in dB between two points, any difference in resistance level is generally ignored.
3. The dB gain of cascaded systems is simply the **sum** of the dB gains of each stage.
4. It is the **capacitive elements** of a network that determine the **bandwidth** of a system. The **larger** capacitive elements of the basic design determine the **low-cutoff frequency**, whereas the **smaller** parasitic capacitors determine the **high-cutoff frequencies**.
5. The frequencies at which the gain drops to 70.7% of the midband value are called the **cutoff, corner, band, break, or half-power frequencies**.
6. The **narrower** the bandwidth, the **smaller** is the range of frequencies that will permit a transfer of power to the load that is at least 50% of the midband level.
7. A change in frequency by a factor of **two**, equivalent to **one octave**, results in a **6-dB change in gain**. For a **10:1** change in frequency, equivalent to **one decade**, there is a **20-dB change in gain**.
8. For any **inverting** amplifier, the input capacitance will be increased by a **Miller effect** capacitance determined by the **gain** of the amplifier and the **interelectrode** (parasitic) capacitance between the input and output terminals of the active device.
9. A **3-dB drop in beta** ( $h_{fe}$ ) will occur at a frequency defined by  $f_B$  that is sensitive to the **dc operating conditions** of the transistor. This variation in beta can define the upper cutoff frequency of the design.
10. The **high- and low-cutoff frequencies** of an amplifier can be determined by the response of the system to a **square-wave input**. The general appearance will immediately reveal whether the low- or high-frequency response of the system is too limited for the applied frequency, whereas a more detailed examination of the response will reveal the actual bandwidth of the amplifier.

### Equations

Logarithms:

$$a = b^x, \quad x = \log_b a, \quad \log_{10} \frac{a}{b} = \log_{10} a - \log_{10} b$$

$$\log_{10} ab = \log_{10} a + \log_{10} b, \quad G_{\text{dB}} = 10 \log_{10} \frac{P_2}{P_1} = 20 \log_{10} \frac{V_2}{V_1}$$

$$G_{\text{dB}_T} = G_{\text{dB}_1} + G_{\text{dB}_2} + G_{\text{dB}_3} + \dots + G_{\text{dB}_n}$$

Low-frequency response:

$$A_v = \frac{1}{1 - j(f_L/f)}, \quad f_L = \frac{1}{2\pi RC}$$

BJT low-frequency response:

$$f_{L_s} = \frac{1}{2\pi(R_s + R_i)C_s}, \quad R_i = R_1 \| R_2 \| \beta r_e$$

$$f_{L_C} = \frac{1}{2\pi(R_o + R_L)C_C}, \quad R_o = R_C \| r_o$$

# 12

## Power Amplifiers

### CHAPTER OBJECTIVES

- The differences between classes A, AB, and C amplifiers
- What causes amplifier distortion
- Efficiency of various classes of amplifiers
- Power calculations for various class amplifiers

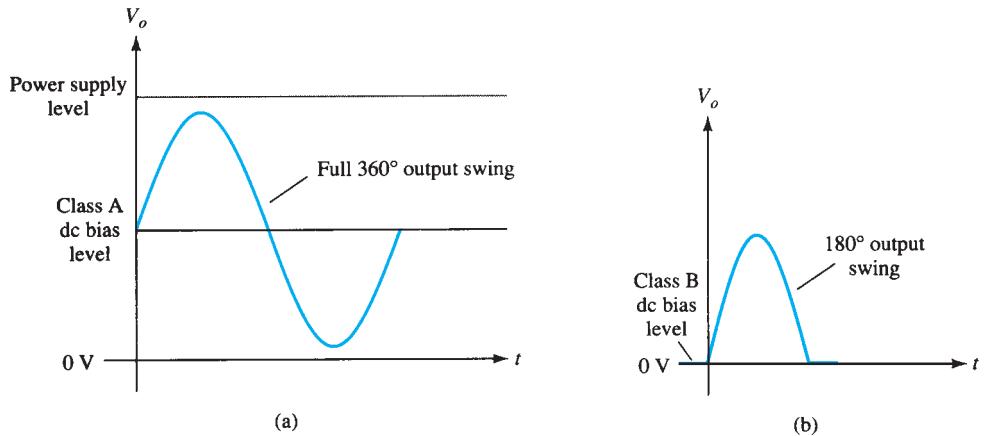
### 12.1 INTRODUCTION—DEFINITIONS AND AMPLIFIER TYPES

An amplifier receives a signal from some pickup transducer or other input source and provides a larger version of the signal to some output device or to another amplifier stage. An input transducer signal is generally small (a few millivolts from a cassette or CD input, or a few microvolts from an antenna) and needs to be amplified sufficiently to operate an output device (speaker or other power-handling device). In small-signal amplifiers, the main factors are usually amplification linearity and magnitude of gain. Since signal voltage and current are small in a small-signal amplifier, the amount of power-handling capacity and power efficiency are of little concern. A voltage amplifier provides voltage amplification primarily to increase the voltage of the input signal. Large-signal or power amplifiers, on the other hand, primarily provide sufficient power to an output load to drive a speaker or other power device, typically a few watts to tens of watts. In Chapter 12, we concentrate on amplifier circuits used to handle large-voltage signals at moderate to high current levels. The main features of a large-signal amplifier are the circuit's power efficiency, the maximum amount of power that the circuit is capable of handling, and the impedance matching to the output device.

One method used to categorize amplifiers is by class. Basically, amplifier classes represent the amount the output signal varies over one cycle of operation for a full cycle of input signal. A brief description of amplifier classes is provided next.

**Class A:** The output signal varies for a full  $360^\circ$  of the input signal. Figure 12.1a shows that this requires the *Q*-point to be biased at a level so that at least half the signal swing of the output may vary up and down without going to a high enough voltage to be limited by the supply voltage level or too low to approach the lower supply level, or 0 V in this description.

**Class B:** A class B circuit provides an output signal varying over one-half the input signal cycle, or for  $180^\circ$  of signal, as shown in Fig. 12.1b. The dc bias point for class B is at 0 V, with the output then varying from this bias point for a half-cycle. Obviously, the



**FIG. 12.1**  
Amplifier operating classes.

output is not a faithful reproduction of the input if only one half-cycle is present. Two class B operations—one to provide output on the positive-output half-cycle and another to provide operation on the negative-output half-cycle—are necessary. The combined half-cycles then provide an output for a full  $360^\circ$  of operation. This type of connection is referred to as *push-pull operation*, which is discussed later in this chapter. Note that class B operation by itself creates a very distorted output signal since reproduction of the input takes place for only  $180^\circ$  of the output signal swing.

**Class AB:** An amplifier may be biased at a dc level above the zero-base-current level of class B and above one-half the supply voltage level of class A; this bias condition is class AB. Class AB operation still requires a push-pull connection to achieve a full output cycle, but the dc bias level is usually closer to the zero-base-current level for better power efficiency, as described shortly. For class AB operation, the output signal swing occurs between  $180^\circ$  and  $360^\circ$  and is neither class A nor class B operation.

**Class C:** The output of a class C amplifier is biased for operation at less than  $180^\circ$  of the cycle and will operate only with a tuned (resonant) circuit, which provides a full cycle of operation for the tuned or resonant frequency. This operating class is therefore used in special areas of tuned circuits, such as radio or communications.

**Class D:** This operating class is a form of amplifier operation using pulse (digital) signals, which are on for a short interval and off for a longer interval. Using digital techniques makes it possible to obtain a signal that varies over the full cycle (using sample-and-hold circuitry) to recreate the output from many pieces of input signal. The major advantage of class D operation is that the amplifier is “on” (using power) only for short intervals and the overall efficiency can practically be very high, as described next.

### Amplifier Efficiency

The power efficiency of an amplifier, defined as the ratio of power output to power input, improves (gets higher) going from class A to class D. In general terms, we see that a class A amplifier, with dc bias at one-half the supply voltage level, uses a good amount of power to maintain bias, even with no input signal applied. This results in very poor efficiency, especially with small input signals, when very little ac power is delivered to the load. In fact, the maximum efficiency of a class A circuit, occurring for the largest output voltage and current swing, is only 25% with a direct or series-fed load connection and 50% with a transformer connection to the load. Class B operation, with no dc bias power for no input signal, can be shown to provide a maximum efficiency that reaches 78.5%. Class D operation can achieve power efficiency over 90% and provides the most efficient operation of all the operating classes. Since class AB falls between class A and class B in bias, it also falls between their efficiency ratings—between 25% (or 50%) and 78.5%. Table 12.1 summarizes the operation of the various amplifier classes. This table provides a relative comparison of the output cycle operation and power efficiency for the various class types. In class B operation, a push-pull connection is obtained using either a transformer coupling

**TABLE 12.1**  
Comparison of Amplifier Classes

	A	AB	Class B	C <sup>a</sup>	D
Operating cycle	360°	180° to 360°	180°	Less than 180°	Pulse operation
Power efficiency	25% to 50%	Between 25% (50%) and 78.5%	78.5%		Typically over 90%

<sup>a</sup>Class C is usually not used for delivering large amounts of power, and thus the efficiency is not given here.

or by using complementary (or quasi-complementary) operation with *npn* and *pnp* transistors to provide operation on opposite-polarity cycles. Although transformer operation can provide opposite-cycle signals, the transformer itself is quite large in many applications. A transformerless circuit using complementary transistors provides the same operation in a much smaller package. Circuits and examples are provided later in this chapter.

## 12.2 SERIES-FED CLASS A AMPLIFIER

The simple fixed-bias circuit connection shown in Fig. 12.2 can be used to discuss the main features of a class A series-fed amplifier. The only differences between this circuit and the small-signal version considered previously is that the signals handled by the large-signal circuit are in the range of volts, and the transistor used is a power transistor that is capable of operating in the range of a few to tens of watts. As will be shown in this section, this circuit is not the best to use as a large-signal amplifier because of its poor power efficiency. The beta of a power transistor is generally less than 100, the overall amplifier circuit using power transistors that are capable of handling large power or current while not providing much voltage gain.

### DC Bias Operation

The dc bias set by  $V_{CC}$  and  $R_B$  fixes the dc base-bias current at

$$I_B = \frac{V_{CC} - 0.7}{R_B} \quad (12.1)$$

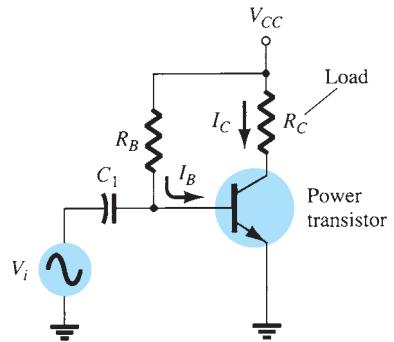
with the collector current then being

$$I_C = \beta I_B \quad (12.2)$$

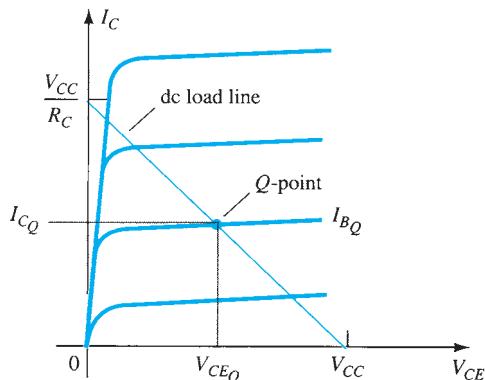
with the collector-emitter voltage then

$$V_{CE} = V_{CC} - I_C R_C \quad (12.3)$$

To appreciate the importance of the dc bias on the operation of the power amplifier, consider the collector characteristic shown in Fig. 12.3. A dc load line is drawn using the



**FIG. 12.2**  
Series-fed class A large-signal amplifier.

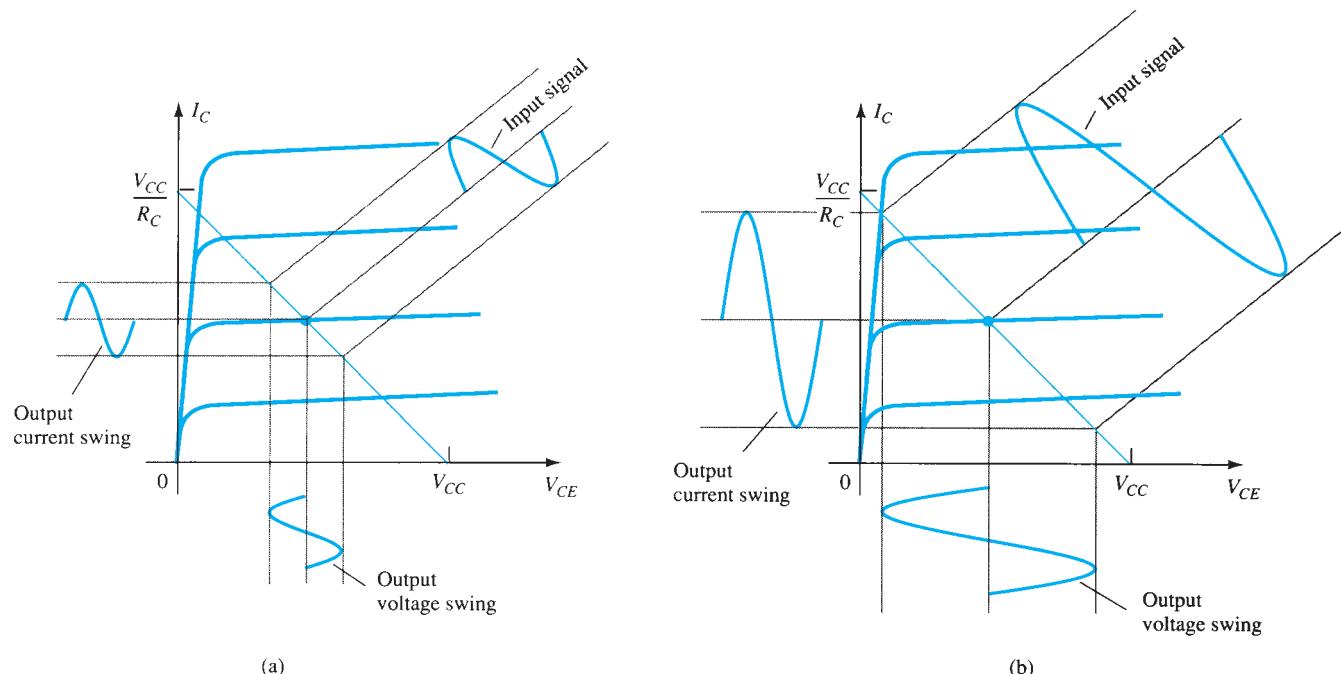


**FIG. 12.3**  
Transistor characteristic showing load line and Q-point.

values of  $V_{CC}$  and  $R_C$ . The intersection of the dc bias value of  $I_B$  with the dc load line then determines the operating point ( $Q$ -point) for the circuit. The quiescent-point values are those calculated using Eqs. (12.1) through (12.3). If the dc bias collector current is set at one-half the possible signal swing (between 0 and  $V_{CC}/R_C$ ), the largest collector current swing will be possible. Additionally, if the quiescent collector-emitter voltage is set at one-half the supply voltage, the largest voltage swing will be possible. With the  $Q$ -point set at this optimum bias point, the power considerations for the circuit of Fig. 12.2 are determined as described next.

### AC Operation

When an input ac signal is applied to the amplifier of Fig. 12.2, the output will vary from its dc bias operating voltage and current. A small input signal, as shown in Fig. 12.4, will cause the base current to vary above and below the dc bias point, which will then cause the collector current (output) to vary from the dc bias point set as well as the collector-emitter voltage to vary around its dc bias value. As the input signal is made larger, the output will vary further around the established dc bias point until either the current or the voltage reaches a limiting condition. For the current this limiting condition is either zero current at the low end or  $V_{CC}/R_C$  at the high end of its swing. For the collector-emitter voltage, the limit is either 0 V or the supply voltage,  $V_{CC}$ .



**FIG. 12.4**  
Amplifier input and output signal variation.

### Power Considerations

The power into an amplifier is provided by the supply voltage. With no input signal, the dc current drawn is the collector bias current  $I_{CQ}$ . The power then drawn from the supply is

$$P_i(\text{dc}) = V_{CC}I_{CQ} \quad (12.4)$$

Even with an ac signal applied, the average current drawn from the supply remains equal to the quiescent current  $I_{CQ}$ , so that Eq. (12.4) represents the input power supplied to the class A series-fed amplifier.

**Output Power** The output voltage and current varying around the bias point provide ac power to the load. This ac power is delivered to the load  $R_C$  in the circuit of Fig. 12.2. The ac signal  $V_i$  causes the base current to vary around the dc bias current and the collector current around its quiescent level  $I_{CQ}$ . As shown in Fig. 12.4, the ac input signal results in ac current and ac voltage signals. The larger the input signal, the larger is the output swing, up to the maximum set by the circuit. The ac power delivered to the load ( $R_C$ ) can be expressed in a number of ways.

**Using RMS signals.** The ac power delivered to the load ( $R_C$ ) may be expressed using

$$P_o(\text{ac}) = V_{CE}(\text{rms})I_C(\text{rms}) \quad (12.5)$$

$$P_o(\text{ac}) = I_C^2(\text{rms})R_C \quad (12.6)$$

$$P_o(\text{ac}) = \frac{V_C^2(\text{rms})}{R_C} \quad (12.7)$$

## Efficiency

The efficiency of an amplifier represents the amount of ac power delivered (transferred) from the dc source. The efficiency of the amplifier is calculated using

$$\% \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% \quad (12.8)$$

**Maximum Efficiency** For the class A series-fed amplifier, the maximum efficiency can be determined using the maximum voltage and current swings. For the voltage swing it is

$$\text{maximum } V_{CE}(\text{p-p}) = V_{CC}$$

For the current swing it is

$$\text{maximum } I_C(\text{p-p}) = \frac{V_{CC}}{R_C}$$

Using the maximum voltage swing in Eq. (12.7) yields

$$\begin{aligned} \text{maximum } P_o(\text{ac}) &= \frac{V_{CC}(V_{CC}/R_C)}{8} \\ &= \frac{V_{CC}^2}{8R_C} \end{aligned}$$

The maximum power input can be calculated using the dc bias current set to one-half the maximum value:

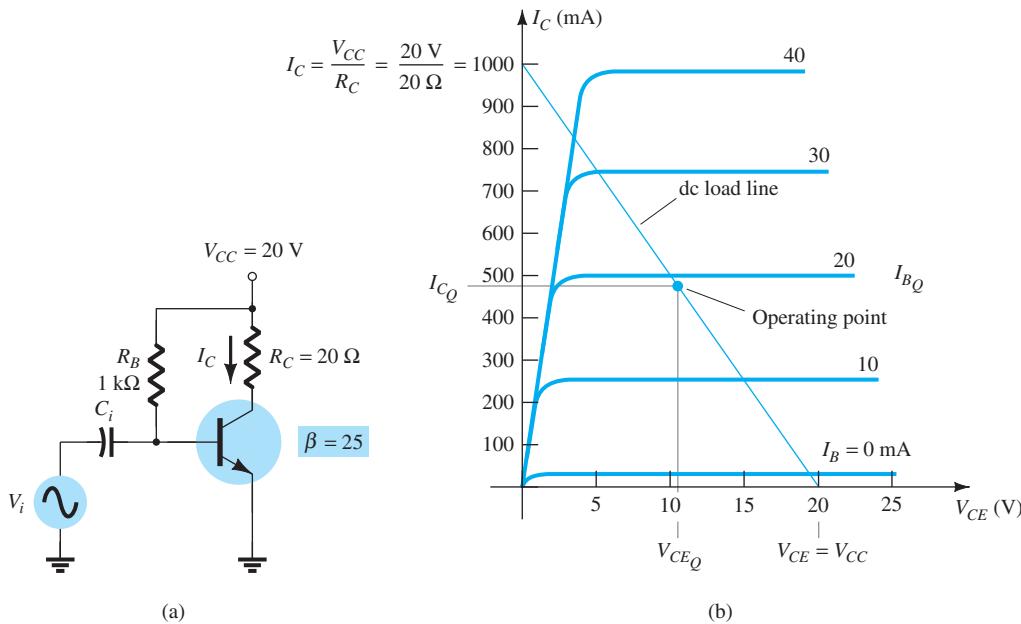
$$\begin{aligned} \text{maximum } P_i(\text{dc}) &= V_{CC}(\text{maximum } I_C) = V_{CC} \frac{V_{CC}/R_C}{2} \\ &= \frac{V_{CC}^2}{2R_C} \end{aligned}$$

We can then use Eq. (12.8) to calculate the maximum efficiency:

$$\begin{aligned} \text{maximum } \% \eta &= \frac{\text{maximum } P_o(\text{ac})}{\text{maximum } P_i(\text{dc})} \times 100\% \\ &= \frac{V_{CC}^2/8R_C}{V_{CC}^2/2R_C} \times 100\% \\ &= 25\% \end{aligned}$$

The maximum efficiency of a class A series-fed amplifier is thus seen to be 25%. Since this maximum efficiency will occur only for ideal conditions of both voltage swing and current swing, most series-fed circuits will provide efficiencies of much less than 25%.

**EXAMPLE 12.1** Calculate the input power, output power, and efficiency of the amplifier circuit in Fig. 12.5 for an input voltage that results in a base current of 10 mA peak.



**FIG. 12.5**  
Operation of a series-fed circuit for Example 12.1.

**Solution:** Using Eqs. (12.1) through (12.3), we can determine the *Q*-point to be

$$I_{BQ} = \frac{V_{CC} - 0.7 \text{ V}}{R_B} = \frac{20 \text{ V} - 0.7 \text{ V}}{1 \text{ k}\Omega} = 19.3 \text{ mA}$$

$$I_{CQ} = \beta I_{BQ} = 25(19.3 \text{ mA}) = 482.5 \text{ mA} \approx 0.48 \text{ A}$$

$$V_{CEQ} = V_{CC} - I_{CQ} R_C = 20 \text{ V} - (0.48 \text{ A})(20 \Omega) = 10.4 \text{ V}$$

This bias point is marked on the transistor collector characteristic of Fig. 12.5b. The ac variation of the output signal can be obtained graphically using the dc load line drawn on Fig. 12.5b by connecting  $V_{CE} = V_{CC} = 20 \text{ V}$  with  $I_C = V_{CC}/R_C = 1000 \text{ mA} = 1 \text{ A}$ , as shown. When the input ac base current increases from its dc bias level, the collector current rises by

$$I_C(p) = \beta I_B(p) = 25(10 \text{ mA peak}) = 250 \text{ mA peak}$$

Using Eq. (12.6) yields

$$P_o(\text{ac}) = I_C^2(\text{rms}) R_C = \frac{I_C^2(\text{p})}{2} R_C = \frac{(250 \times 10^{-3} \text{ A})^2}{2} (20 \Omega) = \mathbf{0.625 \text{ W}}$$

Using Eq. (12.4) results in

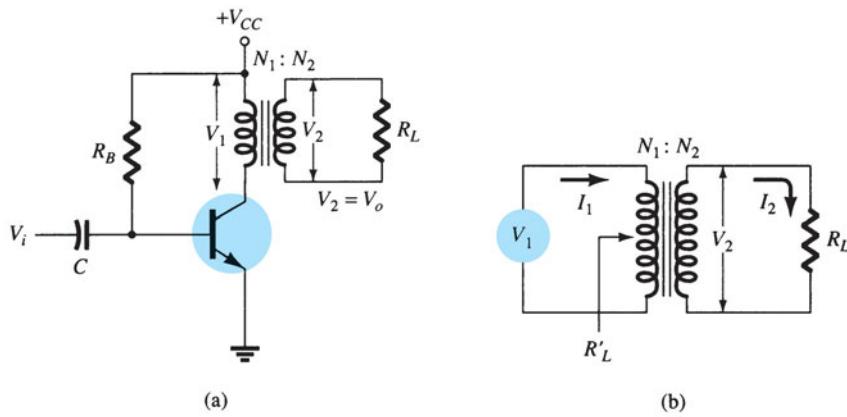
$$P_i(\text{dc}) = V_{CC} I_{CQ} = (20 \text{ V})(0.48 \text{ A}) = \mathbf{9.6 \text{ W}}$$

The amplifier's power efficiency can then be calculated using Eq. (12.8):

$$\% \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{0.625 \text{ W}}{9.6 \text{ W}} \times 100\% = \mathbf{6.5\%}$$

### 12.3 TRANSFORMER-COUPLED CLASS A AMPLIFIER

A form of class A amplifier having maximum efficiency of 50% uses a transformer to couple the output signal to the load as shown in Fig. 12.6. This is a simple circuit form to use in presenting a few basic concepts. More practical circuit versions are covered later.



**FIG. 12.6**  
Transformer-coupled audio power amplifier.

Since the circuit uses a transformer to step voltage or current, a review of voltage and current step-up and step-down is presented next.

### Transformer Action

A transformer can increase or decrease voltage or current levels according to the turns ratio, as explained below. In addition, the impedance connected to one side of a transformer can be made to appear either larger or smaller (step up or step down) at the other side of the transformer, depending on the square of the transformer winding turns ratio. The following discussion assumes ideal (100%) power transfer from primary to secondary, that is, no power losses are considered.

**Voltage Transformation** As shown in Fig. 12.7a, the transformer can step up or step down a voltage applied to one side directly as the ratio of the turns (or number of windings) on each side. The voltage transformation is given by

$$\frac{V_2}{V_1} = \frac{N_2}{N_1} \quad (12.9)$$

Equation (12.9) shows that if the number of turns of wire on the secondary side is larger than the number on the primary, the voltage at the secondary side is larger than the voltage at the primary side.

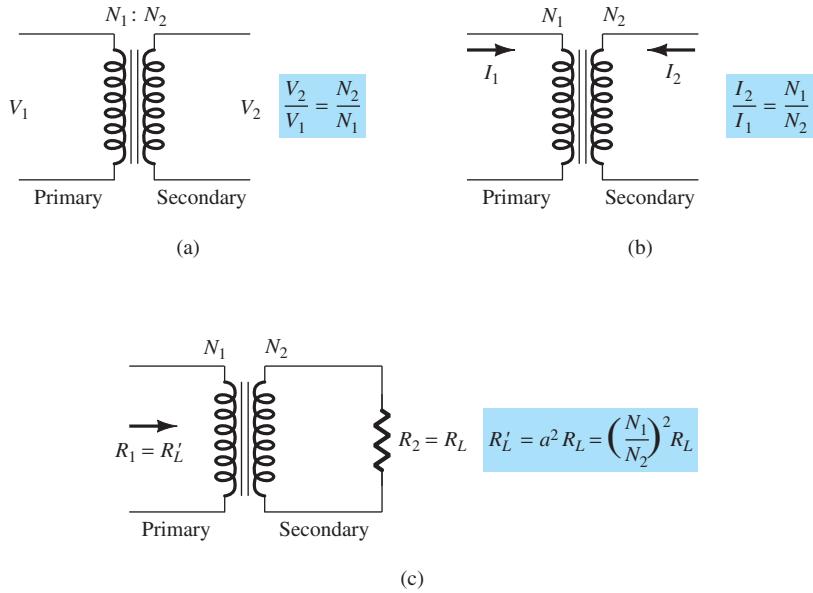
**Current Transformation** The current in the secondary winding is inversely proportional to the number of turns in the windings. The current transformation is given by

$$\frac{I_2}{I_1} = \frac{N_1}{N_2} \quad (12.10)$$

This relationship is shown in Fig. 12.7b. If the number of turns of wire on the secondary is greater than that on the primary, the secondary current will be less than the current in the primary.

**Impedance Transformation** Since the voltage and current can be changed by a transformer, an impedance “seen” from either side (primary or secondary) can also be changed. As shown in Fig. 12.7c, an impedance  $R_L$  is connected across the transformer secondary. This impedance is changed by the transformer when viewed at the primary side ( $R'_L$ ). This can be shown as follows:

$$\frac{R_L}{R'_L} = \frac{R_2}{R_1} = \frac{V_2/I_2}{V_1/I_1} = \frac{V_2 I_1}{I_2 V_1} = \frac{V_2 I_1}{V_1 I_2} = \frac{N_2 N_2}{N_1 N_1} = \left(\frac{N_2}{N_1}\right)^2$$



**FIG. 12.7**  
Transformer operation: (a) voltage transformation; (b) current transformation; (c) impedance transformation.

If we define  $a = N_1/N_2$ , where  $a$  is the turns ratio of the transformer, the above equation becomes

$$\frac{R'_L}{R_L} = \frac{R_1}{R_2} = \left(\frac{N_1}{N_2}\right)^2 = a^2 \quad (12.11)$$

We can express the load resistance reflected to the primary side as

$$R_1 = a^2 R_2 \quad \text{or} \quad R'_L = a^2 R_L \quad (12.12)$$

where  $R'_L$  is the reflected impedance. As shown in Eq. (12.12), the reflected impedance is related directly to the square of the turns ratio. If the number of turns of the secondary is smaller than that of the primary, the impedance seen looking into the primary is larger than that of the secondary by the square of the turns ratio.

**EXAMPLE 12.2** Calculate the effective resistance seen looking into the primary of a 15:1 transformer connected to an 8-Ω load.

**Solution:** Eq. (12.22):

$$R'_L = a^2 R_L = (15)^2 (8 \Omega) = 1800 \Omega = 1.8 \text{ k}\Omega$$

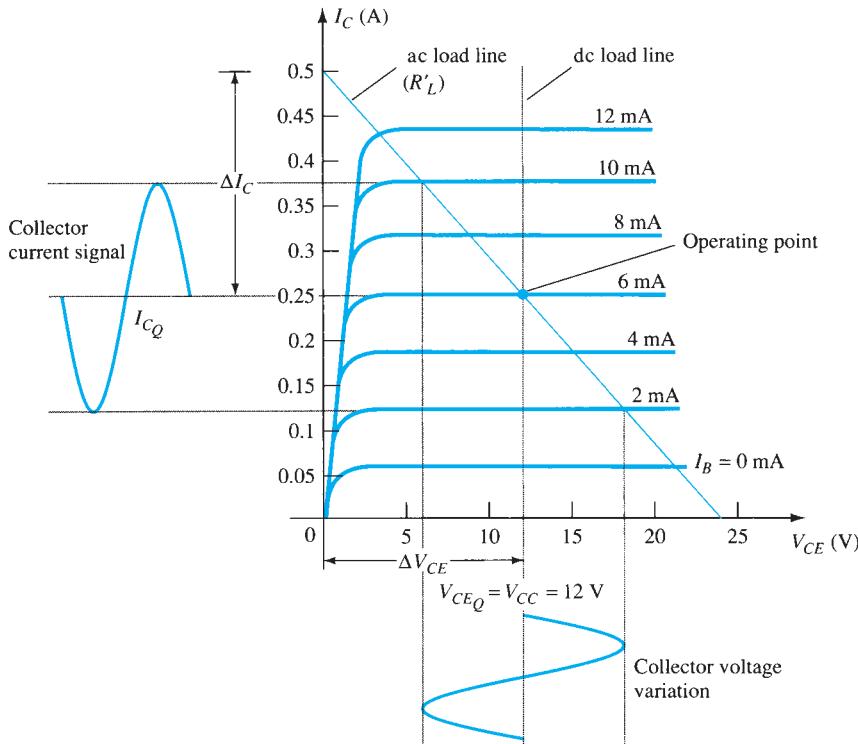
**EXAMPLE 12.3** What transformer turns ratio is required to match a 16-Ω speaker load so that the effective load resistance seen at the primary is 10 kΩ?

**Solution:** Eq. (12.11):

$$\left(\frac{N_1}{N_2}\right)^2 = \frac{R'_L}{R_L} = \frac{10 \text{ k}\Omega}{16 \Omega} = 625$$

$$\frac{N_1}{N_2} = \sqrt{625} = 25:1$$

**DC Load Line** The transformer (dc) winding resistance determines the dc load line for the circuit of Fig. 12.6. Typically, this dc resistance is small (ideally  $0 \Omega$ ) and, as shown in Fig. 12.8, a  $0\text{-}\Omega$  dc load line is a straight vertical line. A practical transformer winding resistance would be a few ohms, but only the ideal case will be considered in this discussion. There is no dc voltage drop across the  $0\text{-}\Omega$  dc load resistance, and the load line is drawn straight vertically from the voltage point,  $V_{CEQ} = V_{CC}$ .



**FIG. 12.8**  
Load lines for class A transformer-coupled amplifier.

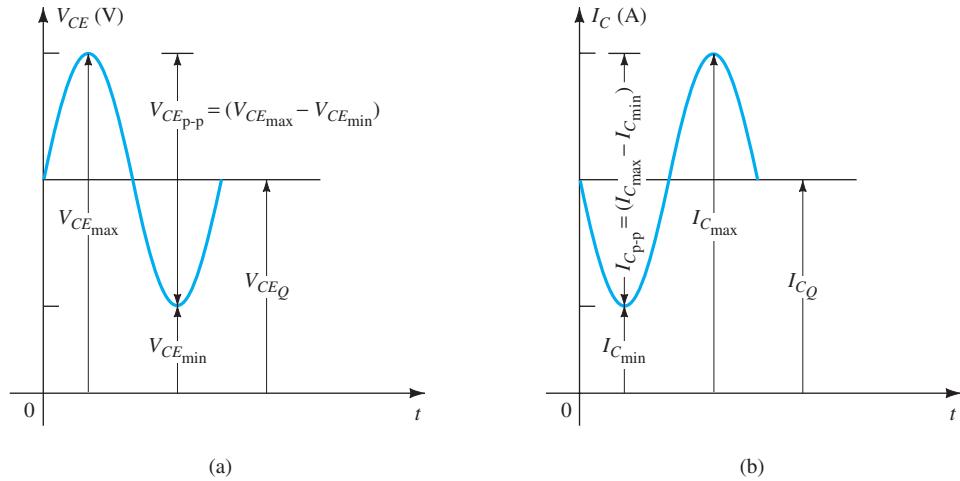
**Quiescent Operating Point** The operating point in the characteristic curve of Fig. 12.8 can be obtained graphically at the point of intersection of the dc load line and the base current set by the circuit. The collector quiescent current can then be obtained from the operating point. In class A operation, keep in mind that the dc bias point sets the conditions for the maximum undistorted signal swing for both collector current and collector-emitter voltage. If the input signal produces a voltage swing less than the maximum possible, the efficiency of the circuit at that time will be less than the maximum of 50%. The dc bias point is therefore important in setting the operation of a class A series-fed amplifier.

**AC Load Line** To carry out ac analysis, it is necessary to calculate the ac load resistance “seen” looking into the primary side of the transformer, then draw the ac load line on the collector characteristic. The reflected load resistance ( $R'_L$ ) is calculated using Eq. (12.12) using the value of the load connected across the secondary ( $R_L$ ) and the turns ratio of the transformer. The graphical analysis technique then proceeds as follows. Draw the ac load line so that it passes through the operating point and has a slope equal to  $-1/R'_L$  (the reflected load resistance), the load line slope being the negative reciprocal of the ac load resistance. Notice that the ac load line shows that the output signal swing can exceed the value of  $V_{CC}$ . In fact, the voltage developed across the transformer primary can be quite large. It is therefore necessary after obtaining the ac load line to check that the possible voltage swing does not exceed transistor maximum ratings.

**Signal Swing and Output AC Power** Figure 12.9 shows the voltage and current signal swings from the circuit of Fig. 12.6. From the signal variations shown in Fig. 12.9, the values of the peak-to-peak signal swings are

$$V_{CE}(\text{p-p}) = V_{CE_{\max}} - V_{CE_{\min}}$$

$$I_C(\text{p-p}) = I_{C_{\max}} - I_{C_{\min}}$$



**FIG. 12.9**  
Graphical operation of transformer-coupled class A amplifier.

The ac power developed across the transformer primary can then be calculated using

$$P_o(\text{ac}) = \frac{(V_{CE_{\max}} - V_{CE_{\min}})(I_{C_{\max}} - I_{C_{\min}})}{8} \quad (12.13)$$

The ac power calculated is that developed across the primary of the transformer. Assuming an ideal transformer (a highly efficient transformer has an efficiency of well over 90%), we find that the power delivered by the secondary to the load is approximately that calculated using Eq. (12.13). The output ac power can also be determined using the voltage delivered to the load.

For the ideal transformer, the voltage delivered to the load can be calculated using Eq. (12.9):

$$V_L = V_2 = \frac{N_2}{N_1} V_1$$

The power across the load can then be expressed as

$$P_L = \frac{V_L^2(\text{rms})}{R_L}$$

and equals the power calculated using Eq. (12.5c).

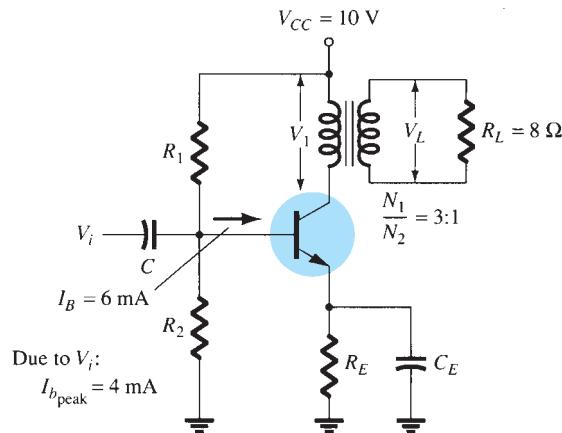
Using Eq. (12.10) to calculate the load current yields

$$I_L = I_2 = \frac{N_1}{N_2} I_C$$

with the output ac power then calculated using

$$P_L = I_L^2(\text{rms}) R_L$$

**EXAMPLE 12.4** Calculate the ac power delivered to the 8-Ω speaker for the circuit of Fig. 12.10. The circuit component values result in a dc base current of 6 mA, and the input signal ( $V_i$ ) results in a peak base current swing of 4 mA.


**FIG. 12.10**

Transformer-coupled class A amplifier for Example 12.4.

**Solution:** The dc load line is drawn vertically (see Fig. 12.11) from the voltage point:

$$V_{CEQ} = V_{CC} = 10 \text{ V}$$

For  $I_B = 6 \text{ mA}$ , the operating point on Fig. 12.11 is

$$V_{CEQ} = 10 \text{ V} \quad \text{and} \quad I_{CQ} = 140 \text{ mA}$$

The effective ac resistance seen at the primary is

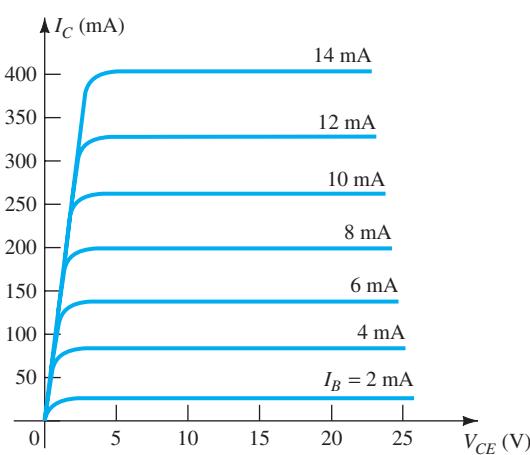
$$R'_L = \left(\frac{N_1}{N_2}\right)^2 R_L = (3)^2(8) = 72 \Omega$$

The ac load line can then be drawn of slope  $-1/72$  going through the indicated operating point. To help draw the load line, consider the following procedure. For a current swing of

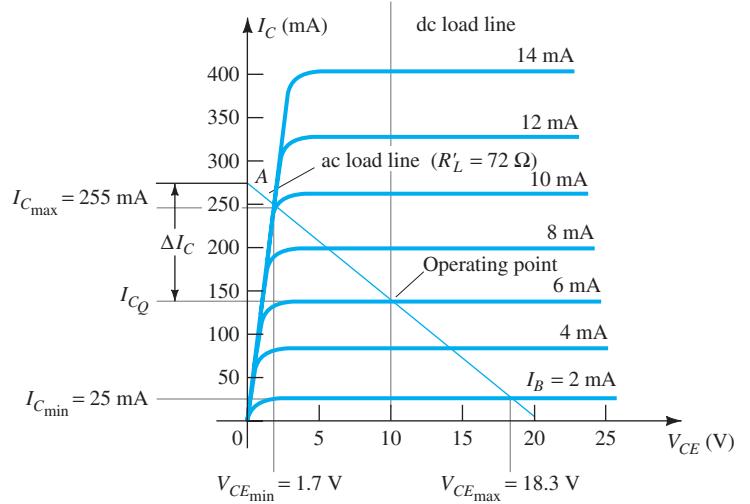
$$I_C = \frac{V_{CE}}{R'_L} = \frac{10 \text{ V}}{72 \Omega} = 139 \text{ mA}$$

mark a point A:

$$I_{CEQ} + I_C = 140 \text{ mA} + 139 \text{ mA} = 279 \text{ mA} \text{ along the } y\text{-axis}$$



(a)


**FIG. 12.11**

Transformer-coupled class A transistor characteristic for Examples 12.4 and 12.5: (a) device characteristic; (b) dc and ac load lines.

Connect point A through the  $Q$ -point to obtain the ac load line. For the given base current swing of 4 mA peak, the maximum and minimum collector current and collector-emitter voltage obtained from Fig. 12.11 are, respectively,

$$\begin{aligned} V_{CE\min} &= 1.7 \text{ V} & I_{C\min} &= 25 \text{ mA} \\ V_{CE\max} &= 18.3 \text{ V} & I_{C\max} &= 255 \text{ mA} \end{aligned}$$

The ac power delivered to the load can then be calculated using Eq. (12.13):

$$\begin{aligned} P_o(\text{ac}) &= \frac{(V_{CE\max} - V_{CE\min})(I_{C\max} - I_{C\min})}{8} \\ &= \frac{(18.3 \text{ V} - 1.7 \text{ V})(255 \text{ mA} - 25 \text{ mA})}{8} = \mathbf{0.477 \text{ W}} \end{aligned}$$


---

## Efficiency

So far we have considered calculating the ac power delivered to the load. We next consider the input power from the battery, power losses in the amplifier, and the overall power efficiency of the transformer-coupled class A amplifier.

The input (dc) power obtained from the supply is calculated from the supply dc voltage and the average power drawn from the supply:

$$P_i(\text{dc}) = V_{CC}I_{C_Q} \quad (12.14)$$

For the transformer-coupled amplifier, the power dissipated by the transformer is small (due to the small dc resistance of a coil) and will be ignored in the present calculations. Thus the only power loss considered here is that dissipated by the power transistor and calculated using

$$P_Q = P_i(\text{dc}) - P_o(\text{ac}) \quad (12.15)$$

where  $P_Q$  is the power dissipated as heat. Although the equation is simple, it is nevertheless significant when operating a class A amplifier. The amount of power dissipated by the transistor is the difference between that drawn from the dc supply (set by the bias point) and the amount delivered to the ac load. When the input signal is very small, with very little ac power delivered to the load, the maximum power is dissipated by the transistor. When the input signal is larger and power delivered to the load is larger, less power is dissipated by the transistor. In other words, the transistor of a class A amplifier has to work hardest (dissipate the most power) when the load is disconnected from the amplifier, and the transistor dissipates the least power when the load is drawing maximum power from the circuit.

**EXAMPLE 12.5** For the circuit of Fig. 12.10 and results of Example 12.4, calculate the dc input power, power dissipated by the transistor, and efficiency of the circuit for the input signal of Example 12.4.

**Solution:** Eq. (12.14):

$$P_i(\text{dc}) = V_{CC}I_{C_Q} = (10 \text{ V})(140 \text{ mA}) = \mathbf{1.4 \text{ W}}$$

Eq. (12.15):

$$P_Q = P_i(\text{dc}) - P_o(\text{ac}) = 1.4 \text{ W} - 0.477 \text{ W} = \mathbf{0.92 \text{ W}}$$

The efficiency of the amplifier is then

$$\% \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{0.477 \text{ W}}{1.4 \text{ W}} \times 100\% = \mathbf{34.1\%}$$


---

**Maximum Theoretical Efficiency** For a class A transformer-coupled amplifier, the maximum theoretical efficiency goes up to 50%. Based on the signals obtained using the amplifier, the efficiency can be expressed as

$$\% \eta = 50 \left( \frac{V_{CE_{\max}} - V_{CE_{\min}}}{V_{CE_{\max}} + V_{CE_{\min}}} \right)^2 \% \quad (12.16)$$

The larger the value of  $V_{CE_{\max}}$  and the smaller the value of  $V_{CE_{\min}}$ , the closer the efficiency approaches the theoretical limit of 50%.

**EXAMPLE 12.6** Calculate the efficiency of a transformer-coupled class A amplifier for a supply of 12 V and outputs of:

- a.  $V(p) = 12 \text{ V}$ .
- b.  $V(p) = 6 \text{ V}$ .
- c.  $V(p) = 2 \text{ V}$ .

**Solution:**

- a. Since  $V_{CE_Q} = V_{CC} = 12 \text{ V}$ , the maximum and minimum of the voltage swing are, respectively,

$$\begin{aligned} V_{CE_{\max}} &= V_{CE_Q} + V(p) = 12 \text{ V} + 12 \text{ V} = 24 \text{ V} \\ V_{CE_{\min}} &= V_{CE_Q} - V(p) = 12 \text{ V} - 12 \text{ V} = 0 \text{ V} \end{aligned}$$

resulting in

$$\% \eta = 50 \left( \frac{24 \text{ V} - 0 \text{ V}}{24 \text{ V} + 0 \text{ V}} \right)^2 \% = 50\%$$

b.

$$\begin{aligned} V_{CE_{\max}} &= V_{CE_Q} + V(p) = 12 \text{ V} + 6 \text{ V} = 18 \text{ V} \\ V_{CE_{\min}} &= V_{CE_Q} - V(p) = 12 \text{ V} - 6 \text{ V} = 6 \text{ V} \end{aligned}$$

resulting in

$$\% \eta = 50 \left( \frac{18 \text{ V} - 6 \text{ V}}{18 \text{ V} + 6 \text{ V}} \right)^2 \% = 12.5\%$$

c.

$$\begin{aligned} V_{CE_{\max}} &= V_{CE_Q} + V(p) = 12 \text{ V} + 2 \text{ V} = 14 \text{ V} \\ V_{CE_{\min}} &= V_{CE_Q} - V(p) = 12 \text{ V} - 2 \text{ V} = 10 \text{ V} \end{aligned}$$

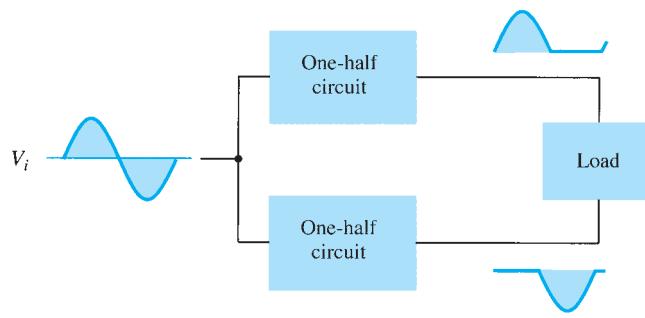
resulting in

$$\% \eta = 50 \left( \frac{14 \text{ V} - 10 \text{ V}}{14 \text{ V} + 10 \text{ V}} \right)^2 \% = 1.39\%$$

Notice how dramatically the amplifier efficiency drops from a maximum of 50% for  $V(p) = V_{CC}$  to slightly over 1% for  $V(p) = 2 \text{ V}$ .

## 12.4 CLASS B AMPLIFIER OPERATION

Class B operation is provided when the dc bias leaves the transistor biased just off, the transistor turning on when the ac signal is applied. This is essentially no bias, and the transistor conducts current for only one-half of the signal cycle. To obtain output for the full cycle of signal, it is necessary to use two transistors and have each conduct on opposite half-cycles, the combined operation providing a full cycle of output signal. Since one part of the circuit pushes the signal high during one half-cycle and the other part pulls the signal low during the other half-cycle, the circuit is referred to as a *push-pull circuit*. Figure 12.12 shows a diagram for push-pull operation. An ac input signal is applied to the push-pull circuit, with each half operating on alternate half-cycles, the load then



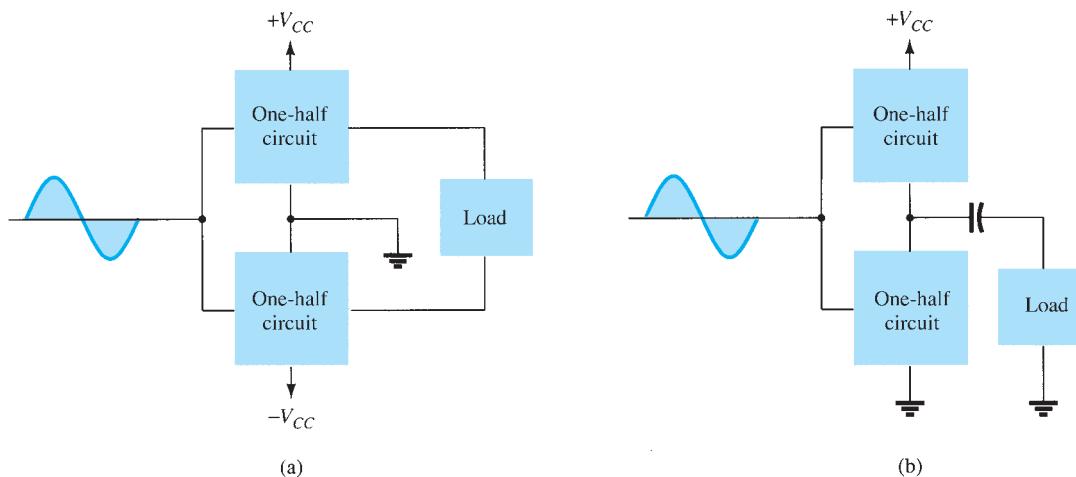
**FIG. 12.12**  
Block representation of push-pull operation.

receiving a signal for the full ac cycle. The power transistors used in the push-pull circuit are capable of delivering the desired power to the load, and the class B operation of these transistors provides greater efficiency than was possible using a single transistor in class A operation.

### Input (DC) Power

The power supplied to the load by an amplifier is drawn from the power supply (or power supplies; see Fig. 12.13) that provides the input or dc power. The amount of this input power can be calculated using

$$P_i(\text{dc}) = V_{CC}I_{\text{dc}} \quad (12.17)$$



**FIG. 12.13**  
Connection of push-pull amplifier to load: (a) using two voltage supplies; (b) using one voltage supply.

where  $I_{\text{dc}}$  is the average or dc current drawn from the power supplies. In class B operation, the current drawn from a single power supply has the form of a full-wave rectified signal, whereas that drawn from two power supplies has the form of a half-wave rectified signal from each supply. In either case, the value of the average current drawn can be expressed as

$$I_{\text{dc}} = \frac{2}{\pi} I(\text{p}) \quad (12.18)$$

where  $I(p)$  is the peak value of the output current waveform. Using Eq. (12.18) in the power input equation (12.17) results in

$$P_i(\text{dc}) = V_{CC} \left( \frac{2}{\pi} I(p) \right) \quad (12.19)$$

## Output (AC) Power

The power delivered to the load (usually referred to as a resistance  $R_L$ ) can be calculated using any one of a number of equations. If one is using an rms meter to measure the voltage across the load, the output power can be calculated as

$$P_o(\text{ac}) = \frac{V_L^2(\text{rms})}{R_L} \quad (12.20)$$

If one is using an oscilloscope, the measured peak or peak-to-peak output voltage can be used:

$$P_o(\text{ac}) = \frac{V_L^2(\text{p-p})}{8R_L} = \frac{V_L^2(\text{p})}{2R_L} \quad (12.21)$$

The larger the rms or peak output voltage, the larger is the power delivered to the load.

## Efficiency

The efficiency of the class B amplifier can be calculated using the basic equation

$$\% \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\%$$

Using Eqs. (12.19) and (12.21) in the efficiency equation above results in

$$\% \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{V_L^2(\text{p})/2R_L}{V_{CC}[(2/\pi)I(p)]} \times 100\% = \frac{\pi}{4} \frac{V_L(\text{p})}{V_{CC}} \times 100\% \quad (12.22)$$

[using  $I(p) = V_L(\text{p})/R_L$ ]. Equation (12.22) shows that the larger the peak voltage, the higher is the circuit efficiency, up to a maximum value when  $V_L(\text{p}) = V_{CC}$ , this maximum efficiency then being

$$\text{maximum efficiency} = \frac{\pi}{4} \times 100\% = 78.5\%$$

**Power Dissipated by Output Transistors** The power dissipated (as heat) by the output power transistors is the difference between the input power delivered by the supplies and the output power delivered to the load,

$$P_{2Q} = P_i(\text{dc}) - P_o(\text{ac}) \quad (12.23)$$

where  $P_{2Q}$  is the power dissipated by the two output power transistors. The dissipated power handled by each transistor is then

$$P_Q = \frac{P_{2Q}}{2} \quad (12.24)$$

**EXAMPLE 12.7** For a class B amplifier providing a 20-V peak signal to a 16-Ω load (speaker) and a power supply of  $V_{CC} = 30$  V, determine the input power, output power, and circuit efficiency.

**Solution:** A 20-V peak signal across a 16- $\Omega$  load provides a peak load current of

$$I_L(p) = \frac{V_L(p)}{R_L} = \frac{20 \text{ V}}{16 \Omega} = 1.25 \text{ A}$$

The dc value of the current drawn from the power supply is then

$$I_{dc} = \frac{2}{\pi} I_L(p) = \frac{2}{\pi} (1.25 \text{ A}) = 0.796 \text{ A}$$

and the input power delivered by the supply voltage is

$$P_i(dc) = V_{CC} I_{dc} = (30 \text{ V})(0.796 \text{ A}) = 23.9 \text{ W}$$

The output power delivered to the load is

$$P_o(ac) = \frac{V_L^2(p)}{2R_L} = \frac{(20 \text{ V})^2}{2(16 \Omega)} = 12.5 \text{ W}$$

for a resulting efficiency of

$$\% \eta = \frac{P_o(ac)}{P_i(dc)} \times 100\% = \frac{12.5 \text{ W}}{23.9 \text{ W}} \times 100\% = 52.3\%$$


---

### Maximum Power Considerations

For class B operation, the maximum output power is delivered to the load when  $V_L(p) = V_{CC}$ :

$$\text{maximum } P_o(ac) = \frac{V_{CC}^2}{2R_L} \quad (12.25)$$

The corresponding peak ac current  $I(p)$  is then

$$I(p) = \frac{V_{CC}}{R_L}$$

so that the maximum value of average current from the power supply is

$$\text{maximum } I_{dc} = \frac{2}{\pi} I(p) = \frac{2V_{CC}}{\pi R_L}$$

Using this current to calculate the maximum value of input power results in

$$\text{maximum } P_i(dc) = V_{CC} (\text{maximum } I_{dc}) = V_{CC} \left( \frac{2V_{CC}}{\pi R_L} \right) = \frac{2V_{CC}^2}{\pi R_L} \quad (12.26)$$

The maximum circuit efficiency for class B operation is then

$$\begin{aligned} \text{maximum } \% \eta &= \frac{P_o(ac)}{P_i(dc)} \times 100\% = \frac{V_{CC}^2/2R_L}{V_{CC}[(2/\pi)(V_{CC}/R_L)]} \times 100\% \\ &= \frac{\pi}{4} \times 100\% = 78.54\% \end{aligned} \quad (12.27)$$

When the input signal results in less than the maximum output signal swing, the circuit efficiency is less than 78.5%.

For class B operation, the maximum power dissipated by the output transistors does not occur at the maximum power input or output condition. The maximum power dissipated by the two output transistors occurs when the output voltage across the load is

$$V_L(p) = 0.636V_{CC} \quad \left( = \frac{2}{\pi} V_{CC} \right)$$

for a maximum transistor power dissipation of

$$\text{maximum } P_{2Q} = \frac{2V_{CC}^2}{\pi^2 R_L} \quad (12.28)$$

**EXAMPLE 12.8** For a class B amplifier using a supply of  $V_{CC} = 30$  V and driving a load of  $16 \Omega$ , determine the maximum input power, output power, and transistor dissipation.

**Solution:** The maximum output power is

$$\text{maximum } P_o(\text{ac}) = \frac{V_{CC}^2}{2R_L} = \frac{(30 \text{ V})^2}{2(16 \Omega)} = 28.125 \text{ W}$$

The maximum input power drawn from the voltage supply is

$$\text{maximum } P_i(\text{dc}) = \frac{2V_{CC}^2}{\pi RL} = \frac{2(30 \text{ V})^2}{\pi(16 \Omega)} = 35.81 \text{ W}$$

The circuit efficiency is then

$$\text{maximum \% } \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{28.125 \text{ W}}{35.81 \text{ W}} \times 100\% = 78.54\%$$

as expected. The maximum power dissipated by each transistor is

$$\text{maximum } P_Q = \frac{\text{maximum } P_{2Q}}{2} = 0.5 \left( \frac{2V_{CC}^2}{\pi^2 R_L} \right) = 0.5 \left[ \frac{2(30 \text{ V})^2}{\pi^2 16 \Omega} \right] = 5.7 \text{ W}$$

Under maximum conditions a pair of transistors each handling 5.7 W at most can deliver 28.125 W to a  $16\Omega$  load while drawing 35.81 W from the supply.

The maximum efficiency of a class B amplifier can also be expressed as follows:

$$\begin{aligned} P_o(\text{ac}) &= \frac{V_L^2(\text{p})}{2R_L} \\ P_i(\text{dc}) &= V_{CC}I_{\text{dc}} = V_{CC} \left[ \frac{2V_L(\text{p})}{\pi R_L} \right] \\ \text{so that } \% \eta &= \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{V_L^2(\text{p})/2R_L}{V_{CC}[(2/\pi)(V_L(\text{p})/R_L)]} \times 100\% \\ \% \eta &= 78.54 \frac{V_L(\text{p})}{V_{CC}} \% \end{aligned} \quad (12.29)$$

**EXAMPLE 12.9** Calculate the efficiency of a class B amplifier for a supply voltage of  $V_{CC} = 24$  V with peak output voltages of:

- a.  $V_L(\text{p}) = 22$  V.
- b.  $V_L(\text{p}) = 6$  V.

**Solution:** Using Eq. (12.29) gives

- a.  $\% \eta = 78.54 \frac{V_L(\text{p})}{V_{CC}} \% = 78.54 \left( \frac{22 \text{ V}}{24 \text{ V}} \right) = 72\%$
- b.  $\% \eta = 78.54 \left( \frac{6 \text{ V}}{24 \text{ V}} \right) \% = 19.6\%$

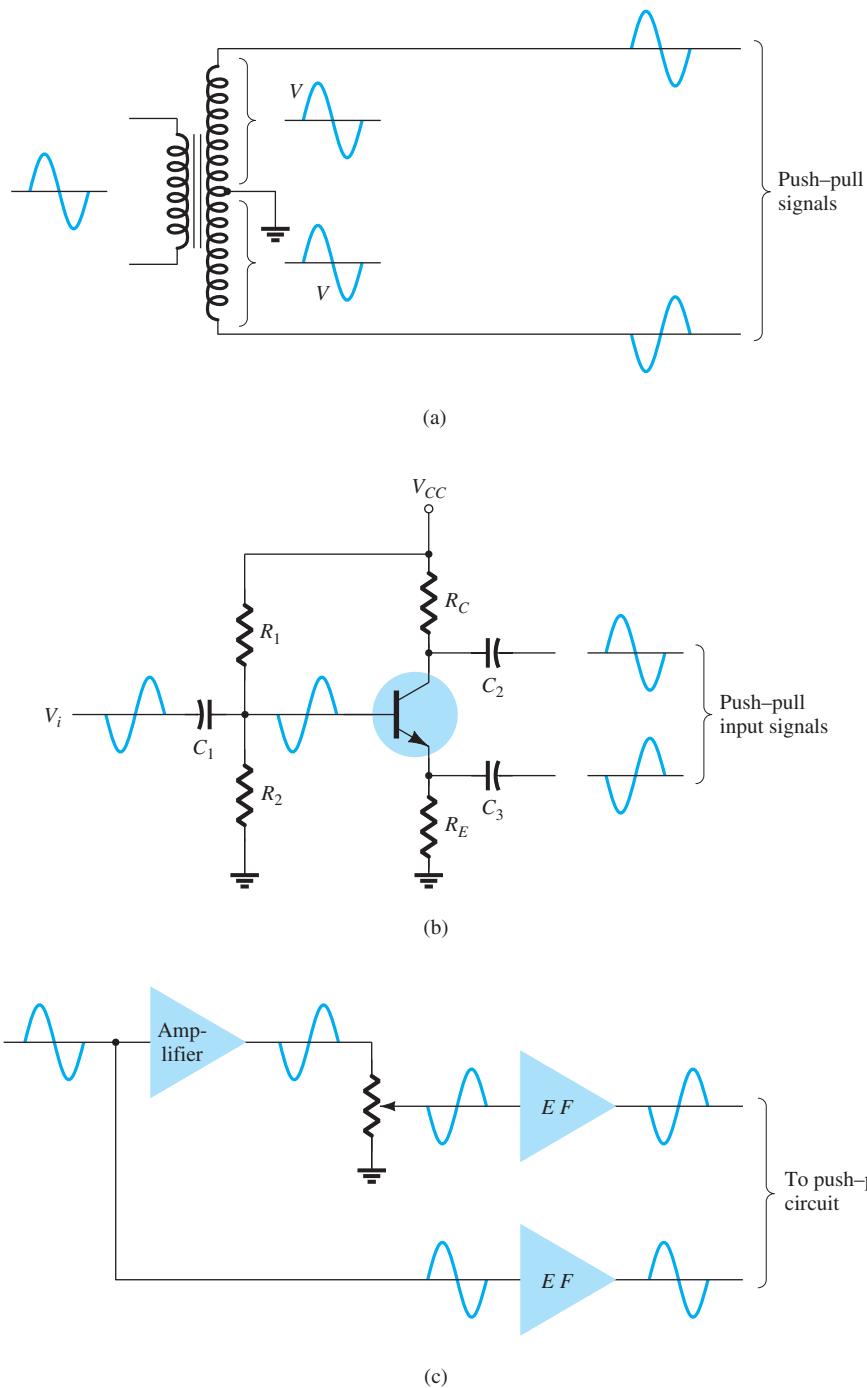
Notice that a voltage near the maximum [22 V in part (a)] results in an efficiency near the maximum, whereas a small voltage swing [6 V in part (b)] still provides an efficiency near 20%. Similar power supply and signal swings would have resulted in much poorer efficiency in a class A amplifier.

## 12.5 CLASS B AMPLIFIER CIRCUITS

A number of circuit arrangements for obtaining class B operation are possible. We will consider the advantages and disadvantages of a number of the more popular circuits in this section. The input signals to the amplifier could be a single signal, the circuit then

providing two different output stages, each operating for one-half the cycle. If the input is in the form of two opposite-polarity signals, two similar stages could be used, each operating on the alternate cycle because of the input signal. One means of obtaining polarity or phase inversion is using a transformer, and the transformer-coupled amplifier has been very popular for a long time. Opposite-polarity inputs can easily be obtained using an op-amp having two opposite outputs or using a few op-amp stages to obtain two opposite-polarity signals. An opposite-polarity operation can also be achieved using a single input and complementary transistors (*npn* and *pnp*, or *nMOS* and *pMOS*).

Figure 12.14 shows different ways to obtain phase-inverted signals from a single input signal. Figure 12.14a shows a center-tapped transformer to provide opposite-phase signals. If the transformer is exactly center-tapped, the two signals are exactly opposite



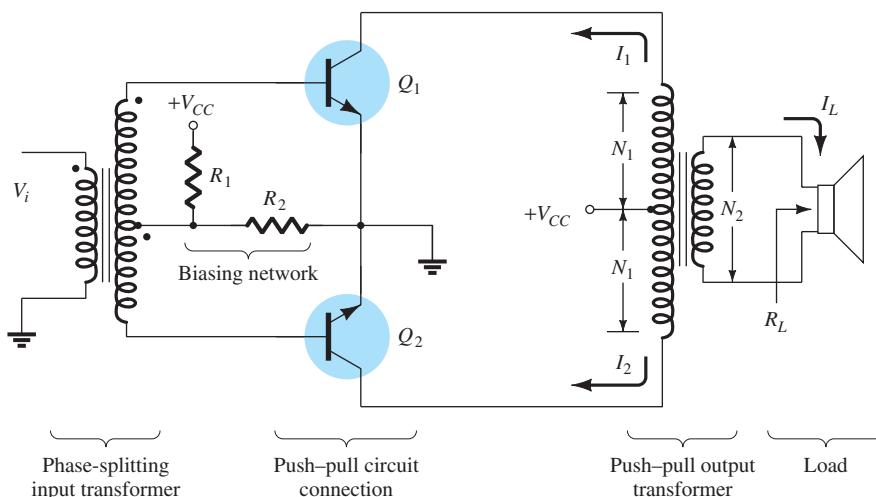
**FIG. 12.14**  
Phase-splitter circuits.

in phase and of the same magnitude. The circuit of Fig. 12.14b uses a BJT stage with in-phase output from the emitter and opposite-phase output from the collector. If the gain is made nearly 1 for each output, the same magnitude results. Probably most common would be using op-amp stages, one to provide an inverting gain of unity and the other a noninverting gain of unity, to provide two outputs of the same magnitude but of opposite phase.

### Transformer-Coupled Push-Pull Circuits

The circuit of Fig. 12.15 uses a center-tapped input transformer to produce opposite-polarity signals to the two transistor inputs and an output transformer to drive the load in a push-pull mode of operation described next.

During the first half-cycle of operation, transistor  $Q_1$  is driven into conduction, whereas transistor  $Q_2$  is driven off. The current  $I_1$  through the transformer results in the first half-cycle of signal to the load. During the second half-cycle of the input signal,  $Q_2$  conducts, whereas  $Q_1$  stays off, the current  $I_2$  through the transformer resulting in the second half-cycle to the load. The overall signal developed across the load then varies over the full cycle of signal operation.

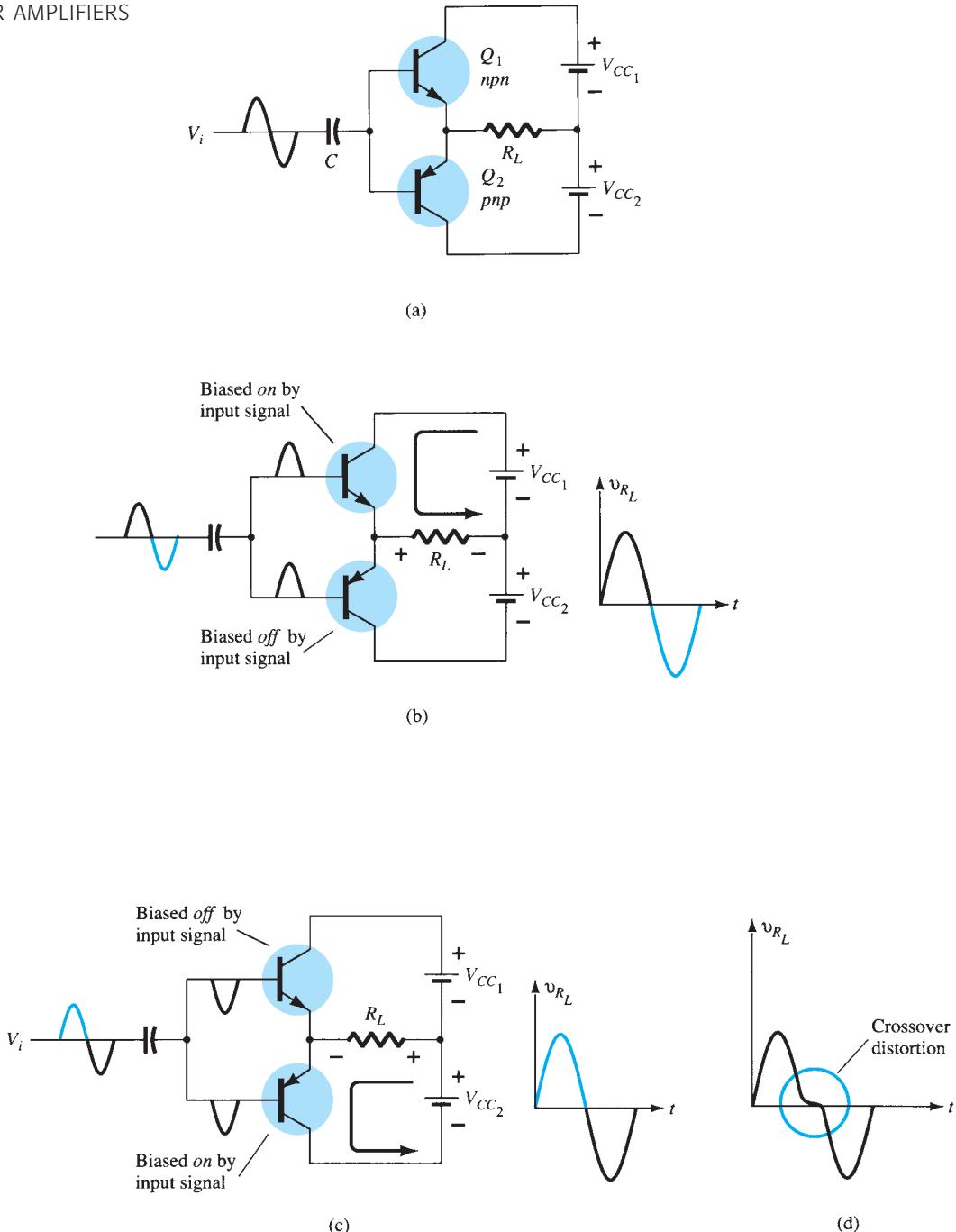


**FIG. 12.15**  
Push-pull circuit.

### Complementary-Symmetry Circuits

Using complementary transistors (*npn* and *pnp*) it is possible to obtain a full cycle output across a load using half-cycles of operation from each transistor, as shown in Fig. 12.16a. Whereas a single input signal is applied to the base of both transistors, the transistors, being of opposite type, will conduct on opposite half-cycles of the input. The *npn* transistor will be biased into conduction by the positive half-cycle of signal, with a resulting half-cycle of signal across the load as shown in Fig. 12.16b. During the negative half-cycle of signal, the *pnp* transistor is biased into conduction when the input goes negative, as shown in Fig. 12.16c.

During a complete cycle of the input, a complete cycle of output signal is developed across the load. One disadvantage of the circuit is the need for two separate voltage supplies. Another, less obvious disadvantage with the complementary circuit is shown in the resulting crossover distortion in the output signal (see Fig. 12.16d). *Crossover distortion* refers to the fact that during the signal crossover from positive to negative (or vice versa) there is some nonlinearity in the output signal. This results from the fact that the circuit does not provide exact switching of one transistor off and the other on at the zero-voltage condition. Both transistors may be partially off so that the output voltage does not follow the input around the zero-voltage condition. Biasing the transistors in class AB improves this operation by biasing both transistors to be on for more than half a cycle.

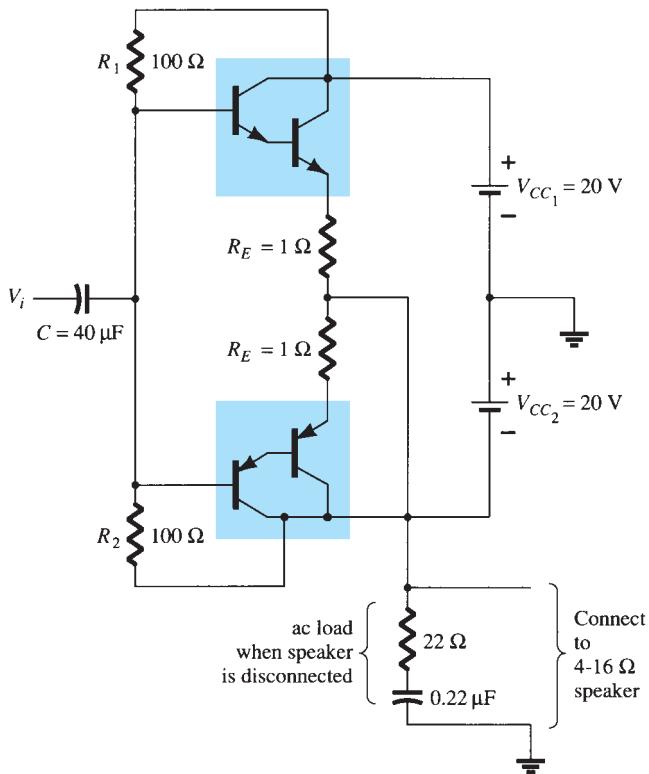


**FIG. 12.16**  
Complementary-symmetry push-pull circuit.

A more practical version of a push-pull circuit using complementary transistors is shown in Fig. 12.17. Note that the load is driven as the output of an emitter-follower so that the load resistance of the load is matched by the low output resistance of the driving source. The circuit uses complementary Darlington-connected transistors to provide higher output current and lower output resistance.

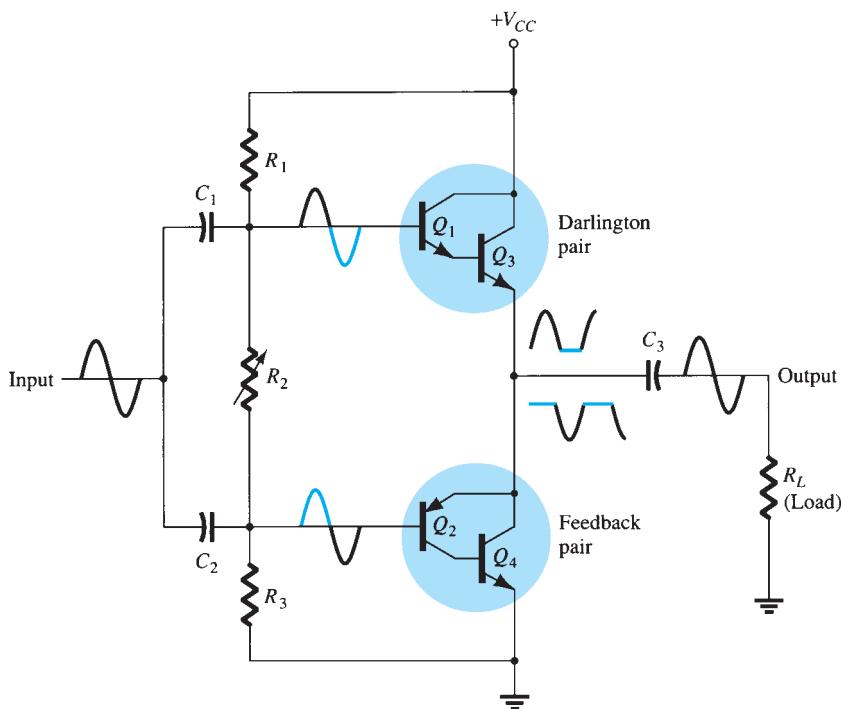
### Quasi-Complementary Push-Pull Amplifier

In practical power amplifier circuits, it is preferable to use *npn* transistors for both high-current-output devices. Since the push-pull connection requires complementary devices, a *pnp* high-power transistor must be used. A practical means of obtaining complementary operation while using the same matched *npn* transistors for the output is provided by a



**FIG. 12.17**  
Complementary-symmetry push–pull circuit using Darlington transistors.

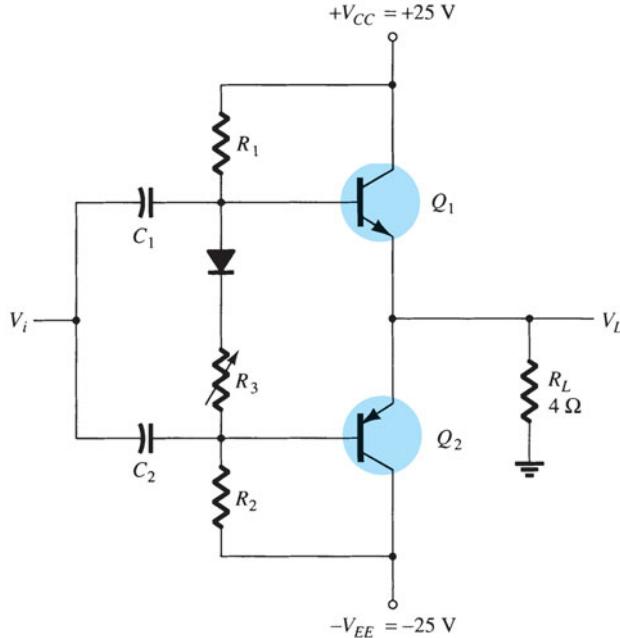
quasi-complementary circuit, as shown in Fig. 12.18. The push–pull operation is achieved by using complementary transistors ( $Q_1$  and  $Q_2$ ) before the matched *npn* output transistors ( $Q_3$  and  $Q_4$ ). Notice that transistors  $Q_1$  and  $Q_3$  form a Darlington connection that provides output from a low-impedance emitter-follower. The connection of transistors  $Q_2$  and  $Q_4$  forms a feedback pair, which similarly provides a low-impedance drive to the load. Resistor



**FIG. 12.18**  
Quasi-complementary push–pull transformerless power amplifier.

$R_2$  can be adjusted to minimize crossover distortion by adjusting the dc bias condition. The single input signal applied to the push-pull stage then results in a full cycle output to the load. The quasi-complementary push-pull amplifier is the most popular form of power amplifier.

**EXAMPLE 12.10** For the circuit of Fig. 12.19, calculate the input power, output power, and power handled by each output transistor and the circuit efficiency for an input of 12 V rms.



**FIG. 12.19**  
Class B power amplifier for Examples 12.10 to 12.12.

**Solution:** The peak input voltage is

$$V_i(p) = \sqrt{2} V_i(\text{rms}) = \sqrt{2} (12 \text{ V}) = 16.97 \text{ V} \approx 17 \text{ V}$$

Since the resulting voltage across the load is ideally the same as the input signal (the amplifier has, ideally, a voltage gain of unity),

$$V_L(p) = 17 \text{ V}$$

and the output power developed across the load is

$$P_o(\text{ac}) = \frac{V_L^2(p)}{2R_L} = \frac{(17 \text{ V})^2}{2(4 \Omega)} = 36.125 \text{ W}$$

The peak load current is

$$I_L(p) = \frac{V_L(p)}{R_L} = \frac{17 \text{ V}}{4 \Omega} = 4.25 \text{ A}$$

from which the dc current from the supplies is calculated to be

$$I_{\text{dc}} = \frac{2}{\pi} I_L(p) = \frac{2(4.25 \text{ A})}{\pi} = 2.71 \text{ A}$$

so that the power supplied to the circuit is

$$P_i(\text{dc}) = V_{CC} I_{\text{dc}} = (25 \text{ V})(2.71 \text{ A}) = 67.75 \text{ W}$$

The power dissipated by each output transistor is

$$P_Q = \frac{P_{2Q}}{2} = \frac{P_i - P_o}{2} = \frac{67.75 \text{ W} - 36.125 \text{ W}}{2} = 15.8 \text{ W}$$

The circuit efficiency (for the input of 12 V, rms) is then

$$\% \eta = \frac{P_o}{P_i} \times 100\% = \frac{36.125 \text{ W}}{67.75 \text{ W}} \times 100\% = 53.3\%$$

**EXAMPLE 12.11** For the circuit of Fig. 12.19, calculate the maximum input power, maximum output power, input voltage for maximum power operation, and power dissipated by the output transistors at this voltage.

**Solution:** The maximum input power is

$$\text{maximum } P_i(\text{dc}) = \frac{2V_{CC}^2}{\pi R_L} = \frac{2(25 \text{ V})^2}{\pi 4 \Omega} = 99.47 \text{ W}$$

The maximum output power is

$$\text{maximum } P_o(\text{ac}) = \frac{V_{CC}^2}{2R_L} = \frac{(25 \text{ V})^2}{2(4 \Omega)} = 78.125 \text{ W}$$

[Note that the maximum efficiency is achieved:

$$\% \eta = \frac{P_o}{P_i} \times 100\% = \frac{78.125 \text{ W}}{99.47 \text{ W}} 100\% = 78.54\%$$

To achieve maximum power operation the output voltage must be

$$V_L(p) = V_{CC} = 25 \text{ V}$$

and the power dissipated by the output transistors is then

$$P_{2Q} = P_i - P_o = 99.47 \text{ W} - 78.125 \text{ W} = 21.3 \text{ W}$$

**EXAMPLE 12.12** For the circuit of Fig. 12.19, determine the maximum power dissipated by the output transistors and the input voltage at which this occurs.

**Solution:** The maximum power dissipated by both output transistors is

$$\text{maximum } P_{2Q} = \frac{2V_{CC}^2}{\pi^2 R_L} = \frac{2(25 \text{ V})^2}{\pi^2 4 \Omega} = 31.66 \text{ W}$$

This maximum dissipation occurs at

$$V_L = 0.636V_L(p) = 0.636(25 \text{ V}) = 15.9 \text{ V}$$

(Notice that at  $V_L = 15.9 \text{ V}$  the circuit required the output transistors to dissipate 31.66 W, whereas at  $V_L = 25 \text{ V}$  they only had to dissipate 21.3 W.)

## 12.6 AMPLIFIER DISTORTION

A pure sinusoidal signal has a single frequency at which the voltage varies positive and negative by equal amounts. Any signal varying over less than the full  $360^\circ$  cycle is considered to have distortion. An ideal amplifier is capable of amplifying a pure sinusoidal signal to provide a larger version, the resulting waveform being a pure single-frequency sinusoidal signal. When distortion occurs, the output will not be an exact duplicate (except for magnitude) of the input signal.

Distortion can occur because the device characteristic is not linear, in which case nonlinear or amplitude distortion occurs. This can occur with all classes of amplifier operation. Distortion can also occur because the circuit elements and devices respond to the input signal differently at various frequencies, this being frequency distortion.

One technique for describing distorted but periodic waveforms uses Fourier analysis, a method that describes any periodic waveform in terms of its fundamental frequency component and frequency components at integer multiples—these components are called *harmonic components* or *harmonics*. For example, a signal that is originally 1000 Hz could result, after distortion, in a frequency component at 1000 Hz (1 kHz) and harmonic components at 2 kHz ( $2 \times 1 \text{ kHz}$ ), 3 kHz ( $3 \times 1 \text{ kHz}$ ), 4 kHz ( $4 \times 1 \text{ kHz}$ ), and so on. The original frequency of 1 kHz is called the *fundamental frequency*; those at integer multiples are the *harmonics*. The 2-kHz component is therefore called a *second harmonic*, that at 3 kHz is the *third harmonic*, and so on. The fundamental frequency is not considered a harmonic. Fourier analysis does not allow for fractional harmonic frequencies—only integer multiples of the fundamental.

## Harmonic Distortion

A signal is considered to have harmonic distortion when there are harmonic frequency components (not just the fundamental component). If the fundamental frequency has an amplitude  $A_1$  and the  $n$ th frequency component has an amplitude  $A_n$ , a harmonic distortion can be defined as

$$\% \text{ } n\text{th harmonic distortion} = \% D_n = \frac{|A_n|}{|A_1|} \times 100\% \quad (12.30)$$

The fundamental component is typically larger than any harmonic component.

**EXAMPLE 12.13** Calculate the harmonic distortion components for an output signal having fundamental amplitude of 2.5 V, second harmonic amplitude of 0.25 V, third harmonic amplitude of 0.1 V, and fourth harmonic amplitude of 0.05 V.

**Solution:** Using Eq. (12.30) yields

$$\% D_2 = \frac{|A_2|}{|A_1|} \times 100\% = \frac{0.25 \text{ V}}{2.5 \text{ V}} \times 100\% = 10\%$$

$$\% D_3 = \frac{|A_3|}{|A_1|} \times 100\% = \frac{0.1 \text{ V}}{2.5 \text{ V}} \times 100\% = 4\%$$

$$\% D_4 = \frac{|A_4|}{|A_1|} \times 100\% = \frac{0.05 \text{ V}}{2.5 \text{ V}} \times 100\% = 2\%$$

**Total Harmonic Distortion** When an output signal has a number of individual harmonic distortion components, the signal can be seen to have a total harmonic distortion based on the individual elements as combined by the relationship of the following equation:

$$\% \text{ THD} = \sqrt{D_2^2 + D_3^2 + D_4^2 + \dots} \times 100\% \quad (12.31)$$

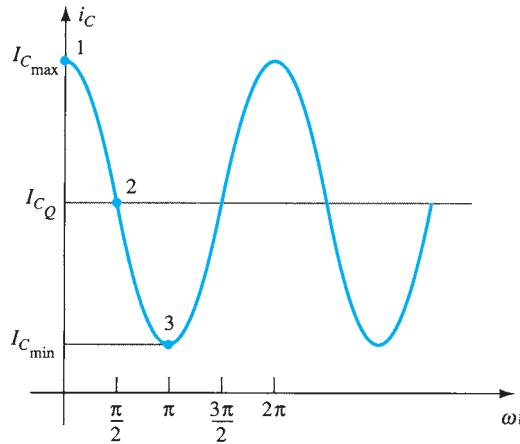
where THD is total harmonic distortion.

**EXAMPLE 12.14** Calculate the total harmonic distortion for the amplitude components given in Example 12.13.

**Solution:** Using the computed values of  $D_2 = 0.10$ ,  $D_3 = 0.04$ , and  $D_4 = 0.02$  in Eq. (12.31), we obtain

$$\begin{aligned} \% \text{ THD} &= \sqrt{D_2^2 + D_3^2 + D_4^2} \times 100\% \\ &= \sqrt{(0.10)^2 + (0.04)^2 + (0.02)^2} \times 100\% = 0.1095 \times 100\% \\ &= 10.95\% \end{aligned}$$

An instrument such as a spectrum analyzer would allow measurement of the harmonics present in the signal by providing a display of the fundamental component of a signal and a number of its harmonics on a display screen. Similarly, a wave analyzer instrument allows more precise measurement of the harmonic components of a distorted signal by filtering out each of these components and providing a reading of these components. In any case, the technique of considering any distorted signal as containing a fundamental component and harmonic components is practical and useful. For a signal occurring in class AB or class B, the distortion may be mainly even harmonics, of which the second harmonic component is the largest. Thus, although the distorted signal theoretically contains all harmonic components from the second harmonic up, the most important in terms of the amount of distortion in the classes presented above is the second harmonic.



**FIG. 12.20**  
Waveform for obtaining second harmonic distortion.

**Second Harmonic Distortion** Figure 12.20 shows a waveform to use for obtaining second harmonic distortion. A collector current waveform is shown with the quiescent, minimum, and maximum signal levels, and the time at which they occur is marked on the waveform. The signal shown indicates that some distortion is present. An equation that approximately describes the distorted signal waveform is

$$i_C \approx I_{C_Q} + I_0 + I_1 \cos \omega t + I_2 \cos 2\omega t \quad (12.32)$$

The current waveform contains the original quiescent current  $I_{C_Q}$ , which occurs with zero input signal; an additional dc current  $I_0$ , due to the nonzero average of the distorted signal; the fundamental component of the distorted ac signal  $I_1$ ; and a second harmonic component  $I_2$ , at twice the fundamental frequency. Although other harmonics are also present, only the second is considered here. Equating the resulting current from Eq. (12.32) at a few points in the cycle to that shown on the current waveform provides the following three relations:

At point 1 ( $\omega t = 0$ ),

$$\begin{aligned} i_C &= I_{C_{\max}} = I_{C_Q} + I_0 + I_1 \cos 0 + I_2 \cos 0 \\ I_{C_{\max}} &= I_{C_Q} + I_0 + I_1 + I_2 \end{aligned}$$

At point 2 ( $\omega t = \pi/2$ ),

$$i_C = I_{C_Q} = I_{C_Q} + I_0 + I_1 \cos \frac{\pi}{2} + I_2 \cos \frac{2\pi}{2}$$

$$I_{C_Q} = I_{C_Q} + I_0 - I_2$$

At point 3 ( $\omega t = \pi$ ),

$$\begin{aligned} i_C &= I_{C_{\min}} = I_{C_Q} + I_0 + I_1 \cos \pi + I_2 \cos 2\pi \\ I_{C_{\min}} &= I_{C_Q} + I_0 - I_1 + I_2 \end{aligned}$$

Solving the preceding three equations simultaneously gives the following results:

$$I_0 = I_2 = \frac{I_{C_{\max}} + I_{C_{\min}} - 2I_{C_Q}}{4}, \quad I_1 = \frac{I_{C_{\max}} - I_{C_{\min}}}{2}$$

Referring to Eq. (12.30), we can express the definition of second harmonic distortion as

$$D_2 = \left| \frac{I_2}{I_1} \right| \times 100\%$$

Inserting the values of  $I_1$  and  $I_2$  determined above gives

$$D_2 = \left| \frac{\frac{1}{2}(I_{C_{\max}} + I_{C_{\min}}) - I_{C_Q}}{I_{C_{\max}} - I_{C_{\min}}} \right| \times 100\% \quad (12.33)$$

In a similar manner, the second harmonic distortion can be expressed in terms of measured collector-emitter voltages:

$$D_2 = \left| \frac{\frac{1}{2}(V_{CE_{\max}} + V_{CE_{\min}}) - V_{CE_Q}}{V_{CE_{\max}} - V_{CE_{\min}}} \right| \times 100\% \quad (12.34)$$

**EXAMPLE 12.15** Calculate the second harmonic distortion if an output waveform displayed on an oscilloscope provides the following measurements:

- $V_{CE_{\min}} = 1 \text{ V}$ ,  $V_{CE_{\max}} = 22 \text{ V}$ ,  $V_{CE_Q} = 12 \text{ V}$ .
- $V_{CE_{\min}} = 4 \text{ V}$ ,  $V_{CE_{\max}} = 20 \text{ V}$ ,  $V_{CE_Q} = 12 \text{ V}$ .

**Solution:** Using Eq. (12.34), we get

$$\begin{aligned} \text{a. } D_2 &= \left| \frac{\frac{1}{2}(22 \text{ V} + 1 \text{ V}) - 12 \text{ V}}{22 \text{ V} - 1 \text{ V}} \right| \times 100\% = 2.38\% \\ \text{b. } D_2 &= \left| \frac{\frac{1}{2}(20 \text{ V} + 4 \text{ V}) - 12 \text{ V}}{20 \text{ V} - 4 \text{ V}} \right| \times 100\% = 0\% \quad (\text{no distortion}) \end{aligned}$$

### Power of a Signal Having Distortion

When distortion does occur, the output power calculated for the undistorted signal is no longer correct. When distortion is present, the output power delivered to the load resistor  $R_C$  due to the fundamental component of the distorted signal is

$$P_1 = \frac{I_1^2 R_C}{2} \quad (12.35)$$

The total power due to all the harmonic components of the distorted signal can then be calculated using

$$P = (I_1^2 + I_2^2 + I_3^2 + \dots) \frac{R_C}{2} \quad (12.36)$$

The total power can also be expressed in terms of the total harmonic distortion,

$$P = (1 + D_2^2 + D_3^2 + \dots) I_1^2 \frac{R_C}{2} = (1 + \text{THD}^2) P_1 \quad (12.37)$$

**EXAMPLE 12.16** For a harmonic distortion reading of  $D_2 = 0.1$ ,  $D_3 = 0.02$ , and  $D_4 = 0.01$ , with  $I_1 = 4 \text{ A}$  and  $R_C = 8 \Omega$ , calculate the total harmonic distortion, fundamental power component, and total power.

**Solution:** The total harmonic distortion is

$$\text{THD} = \sqrt{D_2^2 + D_3^2 + D_4^2} = \sqrt{(0.1)^2 + (0.02)^2 + (0.01)^2} \approx 0.1$$

The fundamental power, using Eq. (12.35), is

$$P_1 = \frac{I_1^2 R_C}{2} = \frac{(4 \text{ A})^2 (8 \Omega)}{2} = 64 \text{ W}$$

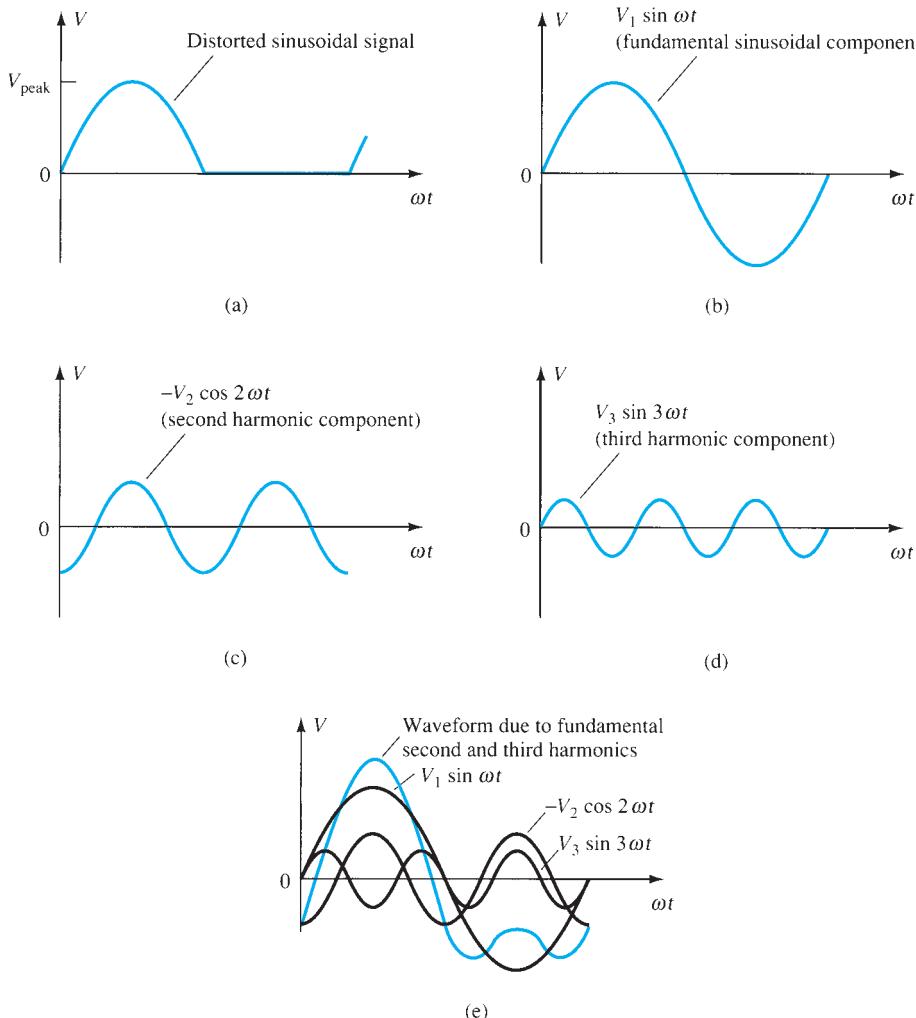
The total power calculated using Eq. (12.37) is then

$$P = (1 + \text{THD}^2) P_1 = [1 + (0.1)^2] 64 = (1.01) 64 = 64.64 \text{ W}$$

(Note that the total power is due mainly to the fundamental component even with 10% second harmonic distortion.)

### Graphical Description of Harmonic Components of a Distorted Signal

A distorted waveform such as that which occurs in class B operation can be represented using Fourier analysis as a fundamental with harmonic components. Figure 12.21a shows a positive half-cycle such as the type that would result in one side of a class B amplifier. Using Fourier analysis techniques, we can obtain the fundamental component of the distorted signal as shown in Fig. 12.21b. Similarly, the second and third harmonic components can be obtained and are shown in Fig. 12.21c and d, respectively. Using the Fourier technique, we can construct the distorted waveform by adding the fundamental and harmonic components, as shown in Fig. 12.21e. In general, any periodic distorted waveform can be represented by adding a fundamental component and all harmonic components, each of varying amplitude and at various phase angles.

**FIG. 12.21**

*Graphical representation of a distorted signal through the use of harmonic components.*

## 12.7 POWER TRANSISTOR HEAT SINKING

Although integrated circuits are used for small-signal and low-power applications, most high-power applications still require individual power transistors. Improvements in production techniques have provided higher power ratings in small-sized packaging cases, have increased the maximum transistor breakdown voltage, and have provided faster-switching power transistors.

The maximum power handled by a particular device and the temperature of the transistor junctions are related since the power dissipated by the device causes an increase in temperature at the junction of the device. Obviously, a 100-W transistor will provide more power capability than a 10-W transistor. On the other hand, proper heat-sinking techniques will allow operation of a device at about one-half its maximum power rating.

Of the two types of bipolar transistors—germanium and silicon—silicon transistors provide greater maximum temperature ratings. Typically, the maximum junction temperature of these types of power transistors is as follows:

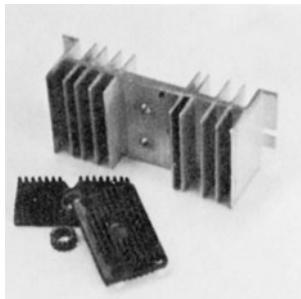
Silicon: 150–200°C

Germanium: 100–110°C

For many applications the average power dissipated may be approximated by

$$P_D = V_{CE}I_C \quad (12.38)$$

This power dissipation, however, is allowed only up to a maximum temperature. Above this temperature, the device power dissipation capacity must be reduced (or derated) so that at higher case temperatures the power-handling capacity is reduced, down to 0 W at the device maximum case temperature.

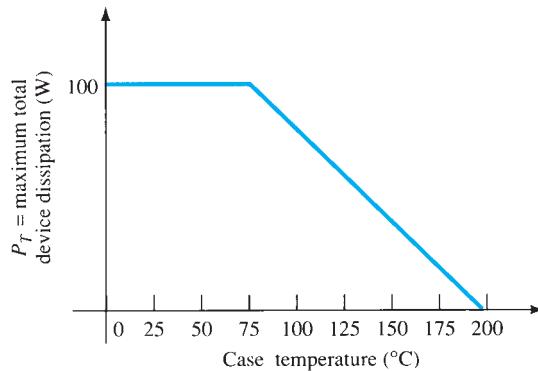


**FIG. 12.22**  
Typical power heat sinks.

The greater the power handled by the transistor, the higher is the case temperature. Actually, the limiting factor in power handling by a particular transistor is the temperature of the device's collector junction. Power transistors are mounted in large metal cases to provide a large area from which the heat generated by the device may radiate (be transferred). Even so, operating a transistor directly into air (mounting it on a plastic board, for example) severely limits the device power rating. If, instead (as is usual practice), the device is mounted on some form of heat sink, its power-handling capacity can approach the rated maximum value more closely. A few heat sinks are shown in Fig. 12.22. When the heat sink is used, the heat produced by the transistor dissipating power has a larger area from which to radiate (transfer) the heat into the air, thereby holding the case temperature to a much lower value than would result without the heat sink. Even with an infinite heat sink (which, of course, is not available), for which the case temperature is held at the ambient (air) temperature, the junction will be heated above the case temperature and a maximum power rating must be considered.

Since even a good heat sink cannot hold the transistor case temperature at ambient (which, by the way, could be more than 25°C if the transistor circuit is in a confined area where other devices are also radiating a good amount of heat), it is necessary to derate the amount of maximum power allowed for a particular transistor as a function of increased case temperature.

Figure 12.23 shows a typical power derating curve for a silicon transistor. The curve shows that the manufacturer will specify an upper temperature point (not necessarily 25°C), after which a linear derating takes place. For silicon, the maximum power that should be handled by the device does not reduce to 0 W until the case temperature is 200°C.



**FIG. 12.23**  
Typical power derating curve for silicon transistors.

It is not necessary to provide a derating curve since the same information could be given simply as a listed derating factor on the device specification sheet. Stated mathematically, we have

$$P_D(\text{temp}_1) = P_D(\text{temp}_0) - (\text{Temp}_1 - \text{Temp}_0)(\text{derating factor}) \quad (12.39)$$

where the value of  $\text{Temp}_0$  is the temperature at which derating should begin, the value of  $\text{Temp}_1$  is the particular temperature of interest (above the value  $\text{Temp}_0$ ),  $P_D(\text{temp}_0)$  and  $P_D(\text{temp}_1)$  are the maximum power dissipations at the temperatures specified, and the derating factor is the value given by the manufacturer in units of watts (or milliwatts) per degree of temperature.

**EXAMPLE 12.17** Determine what maximum dissipation will be allowed for an 80-W silicon transistor (rated at 25°C) if derating is required above 25°C by a derating factor of 0.5 W/°C at a case temperature of 125°C.

**Solution:**

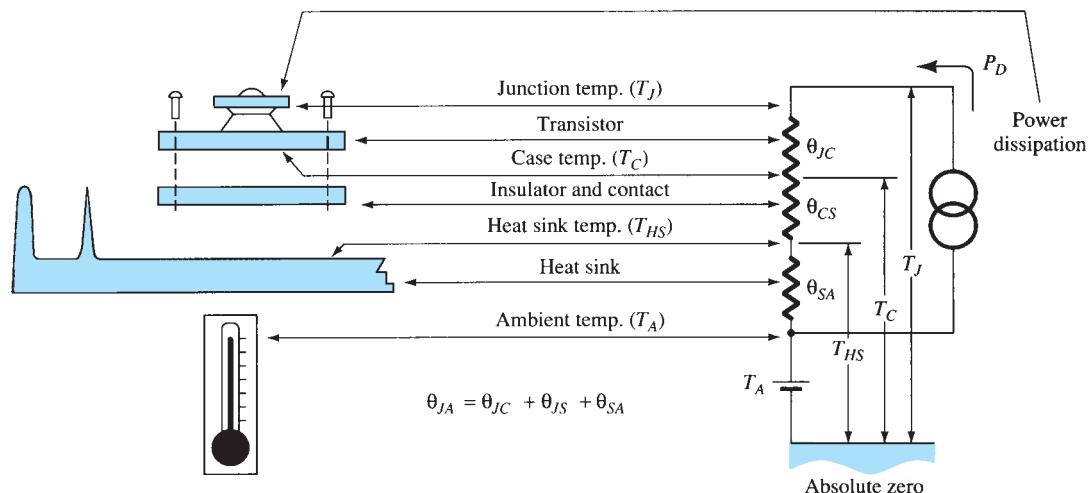
$$\begin{aligned} P_D(125^\circ\text{C}) &= P_D(25^\circ\text{C}) - (125^\circ\text{C} - 25^\circ\text{C})(0.5 \text{ W/}^\circ\text{C}) \\ &= 80 \text{ W} - 100^\circ\text{C}(0.5 \text{ W/}^\circ\text{C}) = 30 \text{ W} \end{aligned}$$

It is interesting to note what power rating results from using a power transistor without a heat sink. For example, a silicon transistor rated at 100 W at (or below) 100°C is rated only 4 W at (or below) 25°C, the free-air temperature. Thus, operated without a heat sink, the device can handle a maximum of only 4 W at the room temperature of 25°C. Using a heat sink large enough to hold the case temperature to 100°C at 100 W allows operating at the maximum power rating.

### Thermal Analogy of a Power Transistor

Selection of a suitable heat sink requires a considerable amount of detail that is not appropriate to our present basic considerations of the power transistor. However, more detail about the thermal characteristics of the transistor and its relation to the power dissipation of the transistor may help provide a clearer understanding of power as limited by temperature. The following discussion should prove useful.

A picture of how the junction temperature  $T_J$ , case temperature  $T_C$ , and ambient (air) temperature  $T_A$  are related by the device heat-handling capacity—a temperature coefficient usually called thermal resistance—is presented in the thermal-electrical analogy shown in Fig. 12.24.



**FIG. 12.24**  
*Thermal-to-electrical analogy.*

In providing a thermal-electrical analogy, the term *thermal resistance* is used to describe heat effects by an electrical term. The terms in Fig. 12.24 are defined as follows:

- $\theta_{JA}$  = total thermal resistance (junction to ambient)
- $\theta_{JC}$  = transistor thermal resistance (junction to case)
- $\theta_{CS}$  = insulator thermal resistance (case to heat sink)
- $\theta_{SA}$  = heat-sink thermal resistance (heat sink to ambient)

Using the electrical analogy for thermal resistances, we can write

$$\boxed{\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}} \quad (12.40)$$

The analogy can also be used in applying Kirchhoff's law to obtain

$$T_J = P_D \theta_{JA} + T_A \quad (12.41)$$

The last relation shows that the junction temperature “floats” on the ambient temperature, and that the higher the ambient temperature, the lower is the allowed value of device power dissipation.

The thermal factor  $\theta$  provides information about how much temperature drop (or rise) results for a given amount of power dissipation. For example, the value of  $\theta_{JC}$  is usually about 0.5°C/W. This means that for a power dissipation of 50 W, the difference in temperature

between case temperature (as measured by a thermocouple) and the inside junction temperature is only

$$T_J - T_C = \theta_{JC} P_D = (0.5^\circ\text{C}/\text{W})(50 \text{ W}) = 25^\circ\text{C}$$

Thus, if the heat sink can hold the case at, say, 50°C, the junction is then only at 75°C. This is a relatively small temperature difference, especially at lower power-dissipation levels.

The value of thermal resistance from junction to free air (using no heat sink) is, typically,

$$\theta_{JA} = 40^\circ\text{C}/\text{W} \quad (\text{into free air})$$

For this thermal resistance, only 1 W of power dissipation results in a junction temperature 40°C greater than the ambient.

A heat sink can now be seen to provide a low thermal resistance between case and air—much less than the 40°C/W value of the transistor case alone. Using a heat sink having

$$\theta_{SA} = 2^\circ\text{C}/\text{W}$$

and with an insulating thermal resistance (from case to heat sink) of

$$\theta_{CS} = 0.8^\circ\text{C}/\text{W}$$

and finally, for the transistor,

$$\theta_{CJ} = 0.5^\circ\text{C}/\text{W}$$

we obtain

$$\begin{aligned}\theta_{JA} &= \theta_{SA} + \theta_{CS} + \theta_{CJ} \\ &= 2.0^\circ\text{C}/\text{W} + 0.8^\circ\text{C}/\text{W} + 0.5^\circ\text{C}/\text{W} = 3.3^\circ\text{C}/\text{W}\end{aligned}$$

So, with a heat sink, the thermal resistance between air and the junction is only 3.3°C/W, compared to 40°C/W for the transistor operating directly into free air. Using the value of  $\theta_{JA}$  above for a transistor operated at, say, 2 W, we calculate

$$T_J - T_A = \theta_{JA} P_D = (3.3^\circ\text{C}/\text{W})(2 \text{ W}) = 6.6^\circ\text{C}$$

In other words, the use of a heat sink in this example provides only a 6.6°C increase in junction temperature as compared to an 80°C rise without a heat sink.

**EXAMPLE 12.18** A silicon power transistor is operated with a heat sink ( $\theta_{SA} = 1.5^\circ\text{C}/\text{W}$ ). The transistor, rated at 150 W (25°C), has  $\theta_{JC} = 0.5^\circ\text{C}/\text{W}$ , and the mounting insulation has  $\theta_{CS} = 0.6^\circ\text{C}/\text{W}$ . What maximum power can be dissipated if the ambient temperature is 40°C and  $T_{J_{\max}} = 200^\circ\text{C}$ ?

**Solution:**

$$P_D = \frac{T_J - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}} = \frac{200^\circ\text{C} - 40^\circ\text{C}}{0.5^\circ\text{C}/\text{W} + 0.6^\circ\text{C}/\text{W} + 1.5^\circ\text{C}/\text{W}} \approx 61.5 \text{ W}$$

## 12.8 CLASS C AND CLASS D AMPLIFIERS

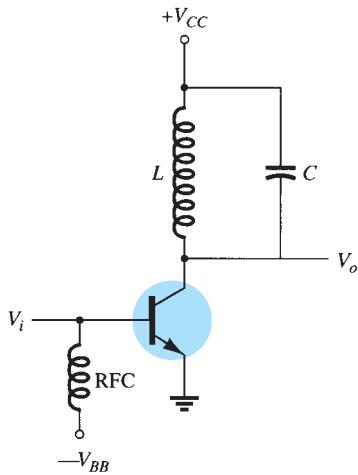
Although class A, class AB, and class B amplifiers are most used as power amplifiers, class D amplifiers are popular because of their very high efficiency. Class C amplifiers, although not used as audio amplifiers, do find use in tuned circuits as in communications.

### Class C Amplifier

A class C amplifier, such as that shown in Fig. 12.25, is biased to operate for less than 180° of the input signal cycle. The tuned circuit in the output, however, will provide a full cycle of output signal for the fundamental or resonant frequency of the tuned circuit ( $L$  and  $C$  tank circuit) of the output. This type of operation is therefore limited to use at one fixed frequency, as occurs in a communications circuit, for example. Operation of a class C circuit is not intended primarily for large-signal or power amplifiers.

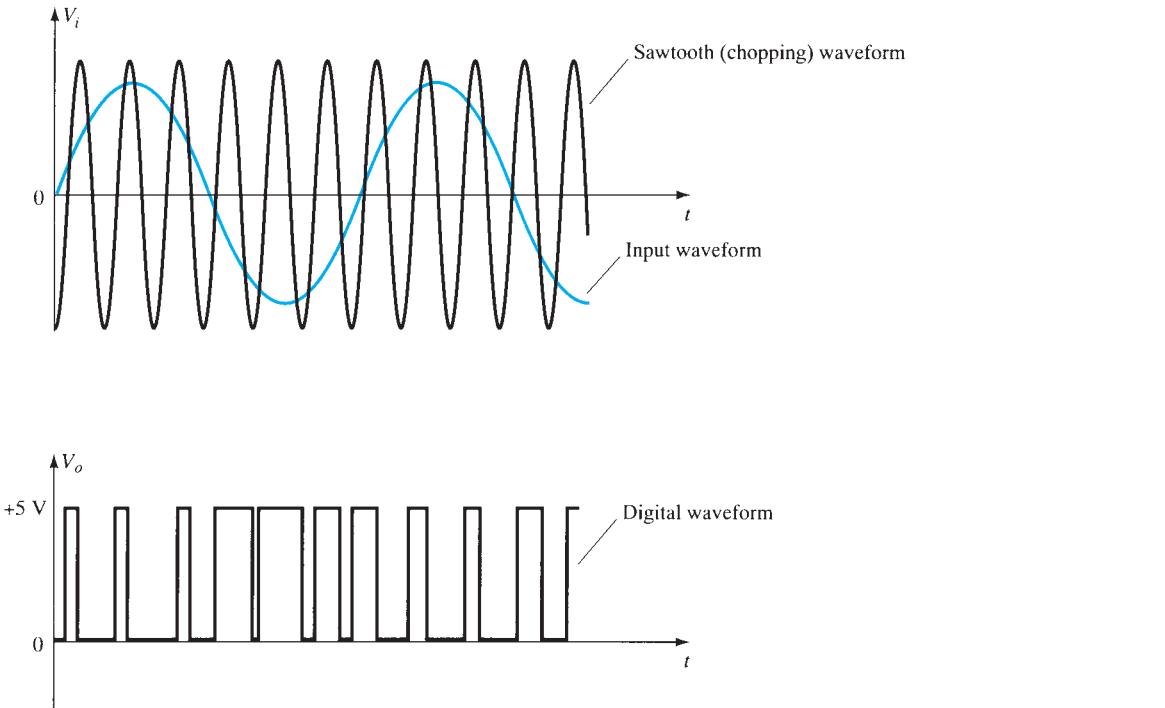
### Class D Amplifier

A class D amplifier is designed to operate with digital or pulse-type signals. An efficiency of over 90% is achieved using this type of circuit, making it quite desirable in power



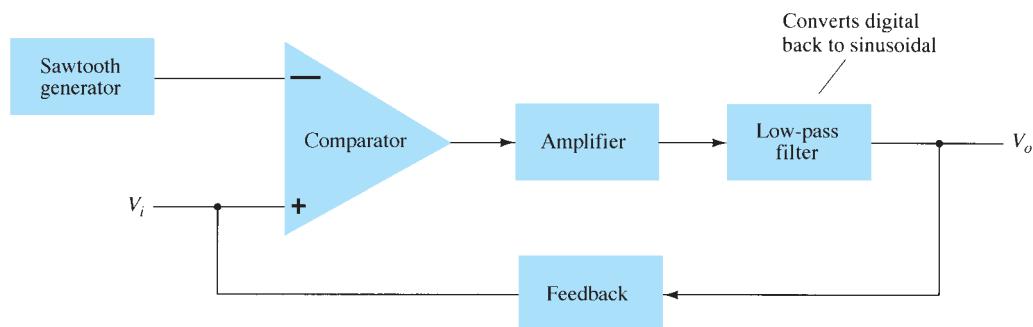
**FIG. 12.25**  
Class C amplifier circuit.

amplifiers. It is necessary, however, to convert any input signal into a pulse-type waveform before using it to drive a large power load and to convert the signal back into a sinusoidal-type signal to recover the original signal. Fig. 12.26 shows how a sinusoidal signal may be converted into a pulse-type signal using some form of sawtooth or chopping waveform to be applied with the input into a comparator-type op-amp circuit so that a representative pulse-type signal is produced. Although the letter D is used to describe the next type of bias operation after class C, the D could also be considered to stand for "Digital," since that is the nature of the signals provided to the class D amplifier.



**FIG. 12.26**  
Chopping of a sinusoidal waveform to produce a digital waveform.

Figure 12.27 shows a block diagram of the unit needed to amplify the class D signal and then convert back into the sinusoidal-type signal using a low-pass filter. Since the amplifier's transistor devices used to provide the output are basically either off or on, they provide current only when they are turned on, with little power loss due to their low "on" voltage. Since most of the power applied to the amplifier is transferred to the load, the efficiency of the circuit is typically very high. Power MOSFET devices have been quite popular as the driver devices for the class D amplifier.



**FIG. 12.27**  
Block diagram of class D amplifier.

## 12.9 SUMMARY

### Important Conclusions and Concepts

1. Amplifier classes:

*Class A*—the output stage conducts for a full  $360^\circ$  (a full waveform cycle).

*Class B*—the output stages each conduct for  $180^\circ$  (together providing a full cycle).

*Class AB*—the output stages each conduct between  $180^\circ$  and  $360^\circ$  (providing a full cycle at less efficiency).

*Class C*—the output stage conducts for less than  $180^\circ$  (used in tuned circuits).

*Class D*—has operation using digital or pulsed signals.

2. Amplifier efficiency:

*Class A*—maximum efficiency of 25% (without transformer) and 50% (with transformer).

*Class B*—maximum efficiency of 78.5%.

3. Power considerations:

a. Input power is provided by the dc power supply.

b. Output power is that delivered to the load.

c. Power dissipated by active devices is essentially the difference between the input and output powers.

4. Push-pull (complementary) operation is typically the opposite of that of devices with one on at a time—one “pushing” for half the cycle and the other “pulling” for half the cycle.

5. **Harmonic distortion** refers to the nonsinusoidal nature of a periodic waveform—the distortion being defined as that at the periodic frequency and multiples of that frequency.

6. **Heat sink** refers to the use of metal cases or frames and fans to remove the heat generated in a circuit element.

### Equations

$$P_i(\text{dc}) = V_{CC} I_{CQ}$$

$$P_o(\text{ac}) = V_{CE}(\text{rms}) I_C(\text{rms})$$

$$= I_C^2(\text{rms}) R_C$$

$$= \frac{V_C^2(\text{rms})}{R_C}$$

$$P_o(\text{ac}) = \frac{V_{CE}(\text{p}) I_C(\text{p})}{2}$$

$$= \frac{I_C^2(\text{p})}{2R_C}$$

$$= \frac{V_{CE}^2(\text{p})}{2R_C}$$

$$P_o(\text{ac}) = \frac{V_{CE}(\text{p-p}) I_C(\text{p-p})}{8}$$

$$= \frac{I_C^2(\text{p-p})}{8R_C} R_C$$

$$= \frac{V_{CE}^2(\text{p-p})}{8R_C}$$

$$\% \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\%$$

Transformer action:

$$\frac{V_2}{V_1} = \frac{N_2}{N_1}$$

$$\frac{I_2}{I_1} = \frac{N_1}{N_2}$$

$$I_{dc} = \frac{2}{\pi} I(p)$$

$$P_i(dc) = V_{CC} \left( \frac{2}{\pi} I(p) \right)$$

$$P_o(ac) = \frac{V_L^2(\text{rms})}{R_L}$$

$$\text{maximum } P_o(\text{ac}) = \frac{V_{CC}^2}{2R_L}$$

$$\text{maximum } P_i(dc) = V_{CC}(\text{maximum } I_{dc}) = V_{CC} \left( \frac{2V_{CC}}{\pi R_L} \right) = \frac{2V_{CC}^2}{\pi R_L}$$

$$\text{maximum } P_{2Q} = \frac{2V_{CC}^2}{\pi^2 R_L}$$

Harmonic distortion:

$$\% \text{ nth harmonic distortion} = \% D_n = \frac{|A_n|}{|A_1|} \times 100\%$$

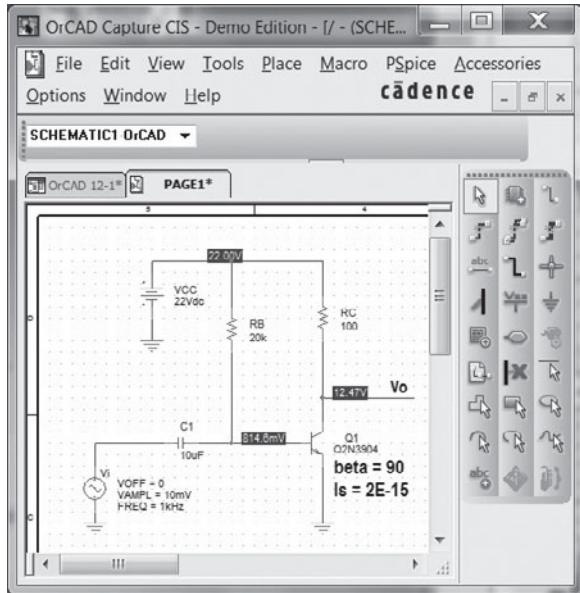
Heat sink:

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

## 12.10 COMPUTER ANALYSIS

### Program 12.1—Series-Fed Class A Amplifier

Using Design Center, we draw the circuit of a series-fed class A amplifier as shown in Fig. 12.28. Figure 12.29 shows some of the analysis output. Edit the transistor model for values of only **BF** = 90 and **IS** = 2E-15. This keeps the transistor model more ideal so that PSpice calculations better match those below.



**FIG. 12.28**  
Series-fed class A amplifier.

The dc bias of the collector voltage is shown to be

$$V_c(dc) = 12.47 \text{ V}$$

With transistor beta set to 90, the ac gain is calculated as follows:

$$I_E = I_c = 95 \text{ mA} \text{ (from analysis output of PSpice)}$$

$$r_e = 26 \text{ mV}/95 \text{ mA} = 0.27 \Omega$$

```

Series-fed Class-A Amplifier
*****
***** CIRCUIT DESCRIPTION *****
*****
***** BJT MODEL PARAMETERS *****
      Q2N3904
      NPN
      IS 2.00000E-15
      BF 90
*****
***** SMALL SIGNAL BIAS SOLUTION *****
*****
      NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE
      (N00210) .8146 (N00214) 0.0000 (N00232) 22.0000 (N00286) 12.4670
*****
      VOLTAGE SOURCE CURRENTS
      NAME CURRENT
      V_VCC -9.639E-02
      V_Vi 0.000E+00
*****
      TOTAL POWER DISSIPATION 2.12E+00 WATTS

```

**FIG. 12.29***Analysis output for the circuit of Fig. 12.28.*

For a gain of

$$A_v = -R_c/r_e = -100/0.27 = -370$$

The output voltage is then

$$V_o = A_v V_i = (-370) \cdot 10 \text{ mV} = -3.7 \text{ V(peak)}$$

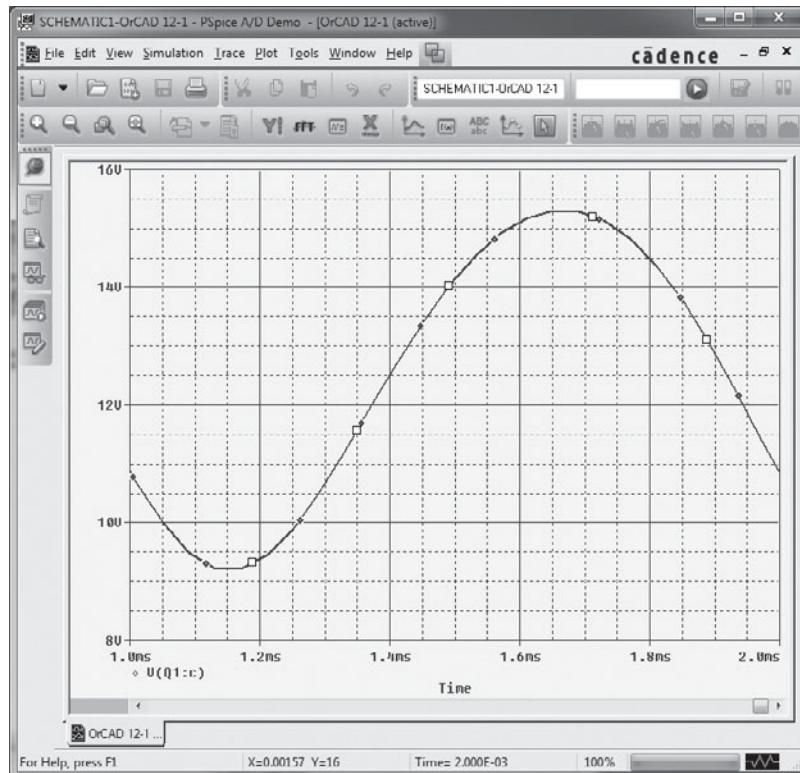
The output waveform obtained using **probe** is shown in Fig. 12.30. For a peak-to-peak output of

$$V_o(\text{p-p}) = 15.6 \text{ V} - 8.75 \text{ V} = 6.85 \text{ V}$$

the peak output is

$$V_o(\text{p}) = 6.85 \text{ V}/2 = 3.4 \text{ V}$$

which compares well with that calculated below.

**FIG. 12.30***Probe output for the circuit of Fig. 12.28.*

# Feedback and Oscillator Circuits

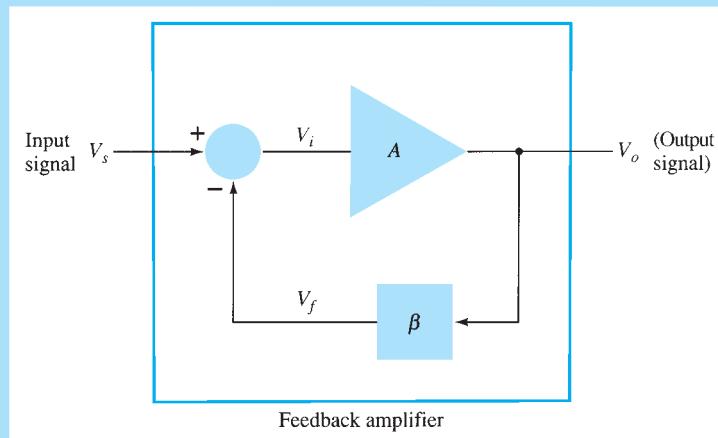
## CHAPTER OBJECTIVES

- The concept of negative feedback
- About practical feedback circuits
- Various types of oscillator circuits

### 14.1 FEEDBACK CONCEPTS

Feedback has been mentioned previously, in particular, in op-amp circuits as described in Chapters 10 and 11. Depending on the relative polarity of the signal being fed back into a circuit, one may have negative or positive feedback. Negative feedback results in decreased voltage gain, for which a number of circuit features are improved, as summarized below. Positive feedback drives a circuit into oscillation as in various types of oscillator circuits.

A typical feedback connection is shown in Fig. 14.1. The input signal  $V_s$  is applied to a mixer network, where it is combined with a feedback signal  $V_f$ . The difference of these signals  $V_i$  is then the input voltage to the amplifier. A portion of the amplifier output  $V_o$  is connected to the feedback network ( $\beta$ ), which provides a reduced portion of the output as feedback signal to the input mixer network.



**FIG. 14.1**  
Simple block diagram of feedback amplifier.

If the feedback signal is of opposite polarity to the input signal, as shown in Fig. 14.1, negative feedback results. Although negative feedback results in reduced overall voltage gain, a number of improvements are obtained, among them being:

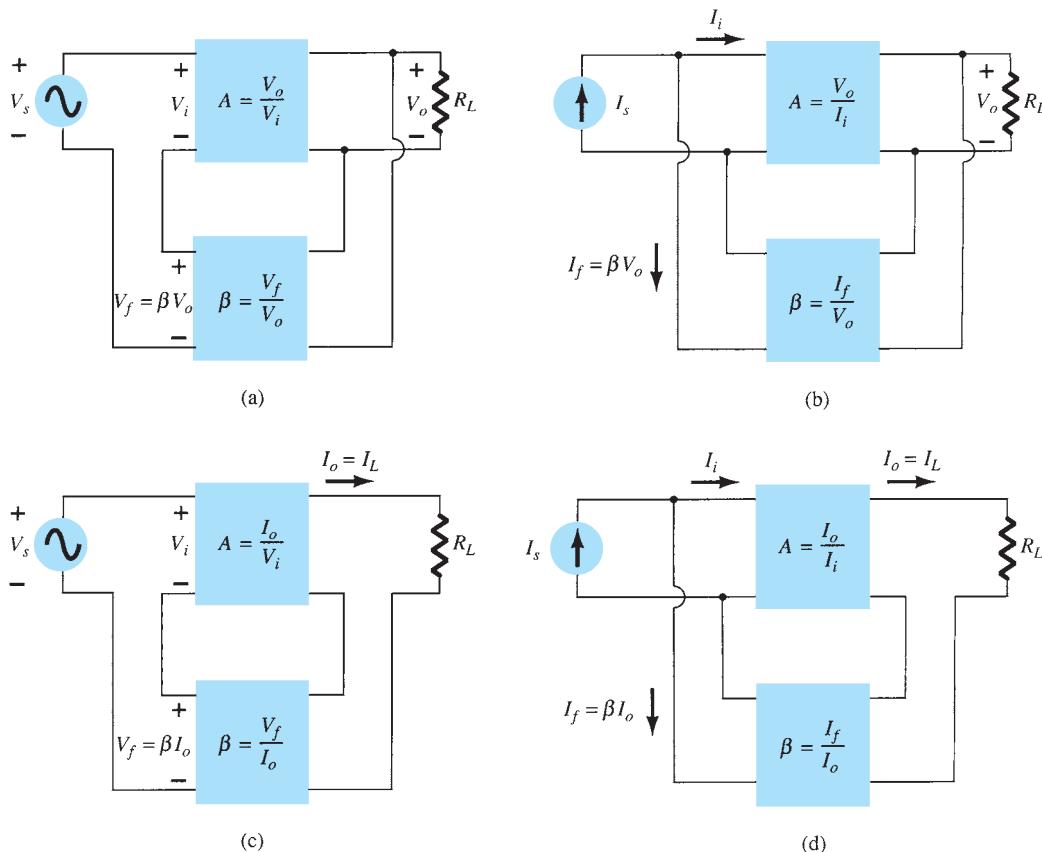
1. Higher input impedance.
2. Better stabilized voltage gain.
3. Improved frequency response.
4. Lower output impedance.
5. Reduced noise.
6. More linear operation.

## 14.2 FEEDBACK CONNECTION TYPES

There are four basic ways of connecting the feedback signal. Both *voltage* and *current* can be fed back to the input either in *series* or *parallel*. Specifically, there can be:

1. Voltage-series feedback (Fig. 14.2a).
2. Voltage-shunt feedback (Fig. 14.2b).
3. Current-series feedback (Fig. 14.2c).
4. Current-shunt feedback (Fig. 14.2d).

In the list above, *voltage* refers to connecting the output voltage as input to the feedback network; *current* refers to tapping off some output current through the feedback network. *Series* refers to connecting the feedback signal in series with the input signal voltage; *shunt* refers to connecting the feedback signal in shunt (parallel) with an input current source.



**FIG. 14.2**

Feedback amplifier types: (a) voltage-series feedback,  $A_f = V_o/V_s$ ; (b) voltage-shunt feedback,  $A_f = V_o/I_s$ ; (c) current-series feedback,  $A_f = I_o/V_s$ ; (d) current-shunt feedback,  $A_f = I_o/I_s$ .

Series feedback connections tend to *increase* the input resistance, whereas shunt feedback connections tend to *decrease* the input resistance. Voltage feedback tends to *decrease* the output impedance, whereas current feedback tends to *increase* the output impedance. Typically, higher input and lower output impedances are desired for most cascade amplifiers. Both of these are provided using the voltage-series feedback connection. We shall therefore concentrate first on this amplifier connection.

## Gain with Feedback

In this section we examine the gain of each of the feedback circuit connections of Fig. 14.2. The gain without feedback,  $A$ , is that of the amplifier stage. With feedback  $\beta$ , the overall gain of the circuit is reduced by a factor  $(1 + \beta A)$ , as detailed below. A summary of the gain, feedback factor, and gain with feedback of Fig. 14.2 is provided for reference in Table 14.1.

**TABLE 14.1**  
Summary of Gain, Feedback, and Gain with Feedback from Fig. 14.2

		Voltage-Series	Voltage-Shunt	Current-Series	Current-Shunt
Gain without feedback	$A$	$\frac{V_o}{V_i}$	$\frac{V_o}{I_i}$	$\frac{I_o}{V_i}$	$\frac{I_o}{I_i}$
Feedback	$\beta$	$\frac{V_f}{V_o}$	$\frac{I_f}{V_o}$	$\frac{V_f}{I_o}$	$\frac{I_f}{I_o}$
Gain with feedback	$A_f$	$\frac{V_o}{V_s}$	$\frac{V_o}{I_s}$	$\frac{I_o}{V_s}$	$\frac{I_o}{I_s}$

**Voltage-Series Feedback** Figure 14.2a shows the voltage-series feedback connection with a part of the output voltage fed back in series with the input signal, resulting in an overall gain reduction. If there is no feedback ( $V_f = 0$ ), the voltage gain of the amplifier stage is

$$A = \frac{V_o}{V_s} = \frac{V_o}{V_i} \quad (14.1)$$

If a feedback signal  $V_f$  is connected in series with the input, then

$$V_i = V_s - V_f$$

Since  $V_o = AV_i = A(V_s - V_f) = AV_s - AV_f = AV_s - A(\beta V_o)$

then  $(1 + \beta A)V_o = AV_s$

so that the overall voltage gain *with* feedback is

$$A_f = \frac{V_o}{V_s} = \frac{A}{1 + \beta A} \quad (14.2)$$

Equation (14.2) shows that the gain *with* feedback is the amplifier gain reduced by the factor  $(1 + \beta A)$ . This factor will be seen also to affect input and output impedance among other circuit features.

**Voltage-Shunt Feedback** The gain with feedback for the network of Fig. 14.2b is

$$A_f = \frac{V_o}{I_s} = \frac{A I_i}{I_i + I_f} = \frac{A I_i}{I_i + \beta V_o} = \frac{A I_i}{I_i + \beta A I_i}$$

$$A_f = \frac{A}{1 + \beta A} \quad (14.3)$$

## Input Impedance with Feedback

**Voltage-Series Feedback** A more detailed voltage-series feedback connection is shown in Fig. 14.3. The input impedance can be determined as follows:

$$I_i = \frac{V_s}{Z_i} = \frac{V_s - V_f}{Z_i} = \frac{V_s - \beta V_o}{Z_i} = \frac{V_s - \beta A V_i}{Z_i}$$

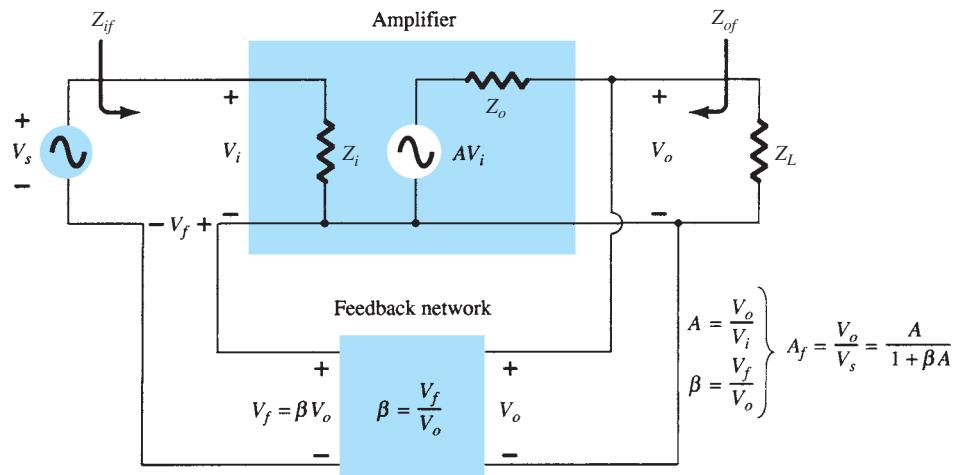
$$I_i Z_i = V_s - \beta A V_i$$

$$V_s = I_i Z_i + \beta A V_i = I_i Z_i + \beta A I_i Z_i$$

$$Z_{if} = \frac{V_s}{I_i} = Z_i + (\beta A) Z_i = Z_i(1 + \beta A)$$

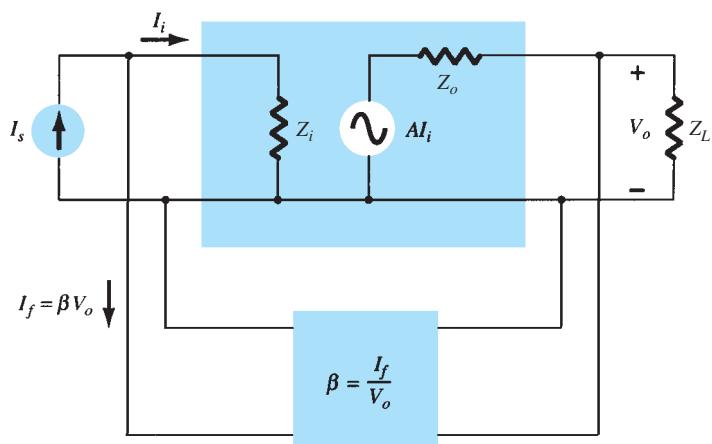
(14.4)

The input impedance with series feedback is seen to be the value of the input impedance without feedback multiplied by the factor  $(1 + \beta A)$ , and applies to both voltage-series (Fig. 14.2a) and current-series (Fig. 14.2c) configurations.



**FIG. 14.3**  
Voltage-series feedback connection.

**Voltage-Shunt Feedback** A more detailed voltage-shunt feedback connection is shown in Fig. 14.4. The input impedance can be determined to be



**FIG. 14.4**  
Voltage-shunt feedback connection.

$$\begin{aligned} Z_{if} &= \frac{V_i}{I_s} = \frac{V_i}{I_i + I_f} = \frac{V_i}{I_i + \beta V_o} \\ &= \frac{V_i/I_i}{I_i/I_i + \beta V_o/I_i} \end{aligned}$$

$Z_{if} = \frac{Z_i}{1 + \beta A}$

(14.5)

This reduced input impedance applies to the voltage-series connection of Fig. 14.2a and the voltage-shunt connection of Fig. 14.2b.

### Output Impedance with Feedback

The output impedance for the connections of Fig. 14.2 is dependent on whether voltage or current feedback is used. For voltage feedback, the output impedance is decreased, whereas current feedback increases the output impedance.

**Voltage-Series Feedback** The voltage-series feedback circuit of Fig. 14.3 provides sufficient circuit detail to determine the output impedance with feedback. The output impedance is determined by applying a voltage  $V$ , resulting in a current  $I$ , with  $V_s$  shorted out ( $V_s = 0$ ). The voltage  $V$  is then

$$V = IZ_o + AV_i$$

For  $V_s = 0$ ,

$$V_i = -V_f$$

so that

$$V = IZ_o - AV_f = IZ_o - A(\beta V)$$

Rewriting the equation as

$$V + \beta AV = IZ_o$$

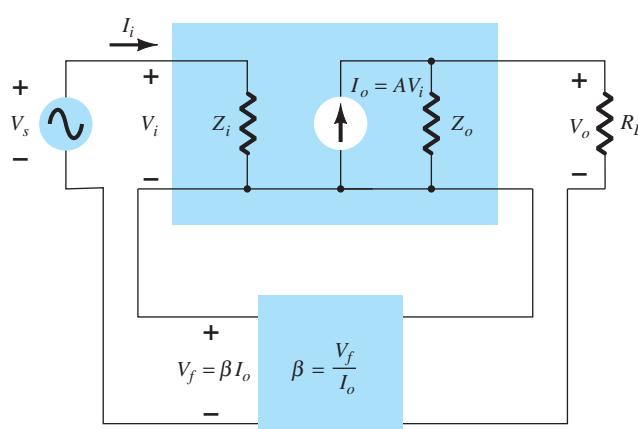
allows solving for the output impedance with feedback:

$Z_{of} = \frac{V}{I} = \frac{Z_o}{1 + \beta A}$

(14.6)

Equation (14.6) shows that with voltage-series feedback the output impedance is reduced from that without feedback by the factor  $(1 + \beta A)$ .

**Current-Series Feedback** The output impedance with current-series feedback can be determined by applying a signal  $V$  to the output with  $V_s$  shorted out, resulting in a current  $I$ , the ratio of  $V$  to  $I$  being the output impedance. Figure 14.5 shows a more detailed



**FIG. 14.5**

Current-series feedback connection.

connection with current-series feedback. For the output part of a current-series feedback connection shown in Fig. 14.5, the resulting output impedance is determined as follows. With  $V_s = 0$ ,

$$\begin{aligned} V_i &= V_f \\ I &= \frac{V}{Z_o} - AV_i = \frac{V}{Z_o} - AV_f = \frac{V}{Z_o} - A\beta I \\ Z_o(1 + \beta A)I &= V \\ Z_{of} &= \frac{V}{I} = Z_o(1 + \beta A) \end{aligned} \quad (14.7)$$

A summary of the effect of feedback on input and output impedance is provided in Table 14.2.

**TABLE 14.2**  
*Effect of Feedback Connection on Input and Output Impedance*

Voltage-Series	Current-Series	Voltage-Shunt	Current-Shunt
$Z_{if}$ (increased)	$Z_i(1 + \beta A)$ (increased)	$\frac{Z_i}{1 + \beta A}$ (decreased)	$\frac{Z_i}{1 + \beta A}$ (decreased)
$Z_{of}$ (decreased)	$\frac{Z_o}{1 + \beta A}$ (increased)	$\frac{Z_o}{1 + \beta A}$ (decreased)	$Z_o(1 + \beta A)$ (increased)

**EXAMPLE 14.1** Determine the voltage gain, input, and output impedance with feedback for voltage-series feedback having  $A = -100$ ,  $R_i = 10 \text{ k}\Omega$ , and  $R_o = 20 \text{ k}\Omega$  for feedback of (a)  $\beta = -0.1$  and (b)  $\beta = -0.5$ .

**Solution:** Using Eqs. (14.2), (14.4), and (14.6), we obtain

$$\text{a. } A_f = \frac{A}{1 + \beta A} = \frac{-100}{1 + (-0.1)(-100)} = \frac{-100}{11} = -9.09$$

$$Z_{if} = Z_i(1 + \beta A) = 10 \text{ k}\Omega (11) = 110 \text{ k}\Omega$$

$$Z_{of} = \frac{Z_o}{1 + \beta A} = \frac{20 \times 10^3}{11} = 1.82 \text{ k}\Omega$$

$$\text{b. } A_f = \frac{A}{1 + \beta A} = \frac{-100}{1 + (-0.5)(-100)} = \frac{-100}{51} = -1.96$$

$$Z_{if} = Z_i(1 + \beta A) = 10 \text{ k}\Omega (51) = 510 \text{ k}\Omega$$

$$Z_{of} = \frac{Z_o}{1 + \beta A} = \frac{20 \times 10^3}{51} = 392.16 \Omega$$

Example 14.1 demonstrates the trade-off of gain for desired input and output resistance. Reducing the gain by a factor of 11 (from 100 to 9.09) is complemented by a reduced output resistance and increased input resistance by the same factor of 11. Reducing the gain by a factor of 51 provides a gain of only 2 but with input resistance increased by the factor of 51 (to over 500 kΩ) and output resistance reduced from 20 kΩ to under 400 Ω. Feedback offers the designer the choice of trading away some of the available amplifier gain for other desired circuit features.

For a negative-feedback amplifier having  $\beta A \gg 1$ , the gain with feedback is  $A_f \approx 1/\beta$ . It follows from this that if the feedback network is purely resistive, the gain with feedback is not dependent on frequency even though the basic amplifier gain is frequency dependent. Practically, the frequency distortion arising because of varying amplifier gain with frequency is considerably reduced in a negative-voltage feedback amplifier circuit.

### Reduction in Noise and Nonlinear Distortion

Signal feedback tends to hold down the amount of noise signal (such as power-supply hum) and nonlinear distortion. The factor  $(1 + \beta A)$  reduces both input noise and resulting nonlinear distortion for considerable improvement. However, there is a reduction in overall gain (the price required for the improvement in circuit performance). If additional stages are used to bring the overall gain up to the level without feedback, the extra stage(s) might introduce as much noise back into the system as that reduced by the feedback amplifier. This problem can be somewhat alleviated by readjusting the gain of the feedback-amplifier circuit to obtain higher gain while also providing reduced noise signal.

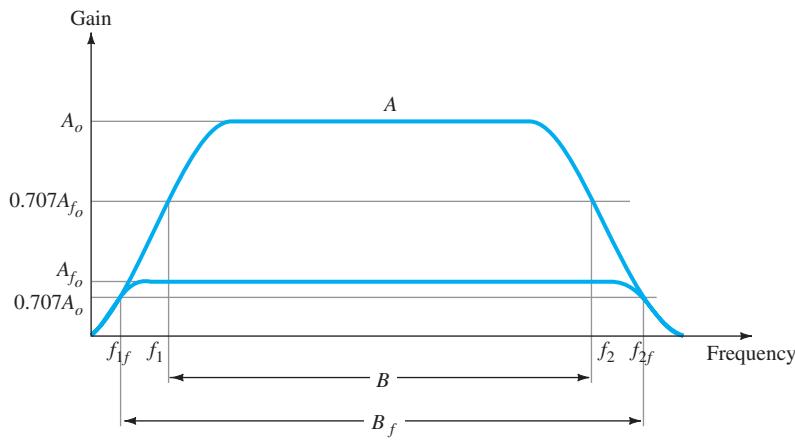
### Effect of Negative Feedback on Gain and Bandwidth

In Eq. (14.2), the overall gain with negative feedback is shown to be

$$A_f = \frac{A}{1 + \beta A} \approx \frac{A}{\beta A} = \frac{1}{\beta} \quad \text{for } \beta A \gg 1$$

As long as  $\beta A \gg 1$ , the overall gain is approximately  $1/\beta$ . For a practical amplifier (for single low- and high-frequency breakpoints) the open-loop gain drops off at high frequencies due to the active device and circuit capacitances. Gain may also drop off at low frequencies for capacitively coupled amplifier stages. Once the open-loop gain  $A$  drops low enough and the factor  $\beta A$  is no longer much larger than 1, the conclusion of Eq. (14.2) that  $A_f \approx 1/\beta$  no longer holds true.

Figure 14.6 shows that the amplifier with negative feedback has more bandwidth ( $B_f$ ) than the amplifier without feedback ( $B$ ). The feedback amplifier has a higher upper 3-dB frequency and smaller lower 3-dB frequency.



**FIG. 14.6**  
Effect of negative feedback on gain and bandwidth.

It is interesting to note that the use of feedback, although resulting in a lowering of voltage gain, has provided an increase in  $B$  and in the upper 3-dB frequency particularly. In fact, the product of gain and frequency remains the same, so that the gain-bandwidth product of the basic amplifier is the same value for the feedback amplifier. However, since the feedback amplifier has lower gain, the net operation was to *trade* gain for bandwidth (we use bandwidth for the upper 3-dB frequency since typically  $f_2 \gg f_1$ ).

## Gain Stability with Feedback

In addition to the  $\beta$  factor setting a precise gain value, we are also interested in how stable the feedback amplifier is compared to an amplifier without feedback. Differentiating Eq. (14.2) leads to

$$\left| \frac{dA_f}{A_f} \right| = \frac{1}{|1 + \beta A|} \left| \frac{dA}{A} \right| \quad (14.8)$$

$$\left| \frac{dA_f}{A_f} \right| \approx \left| \frac{1}{\beta A} \right| \left| \frac{dA}{A} \right| \quad \text{for } \beta A \gg 1 \quad (14.9)$$

This shows that magnitude of the relative change in gain  $\left| \frac{dA_f}{A_f} \right|$  is reduced by the factor  $|\beta A|$  compared to that without feedback  $\left( \left| \frac{dA}{A} \right| \right)$ .

**EXAMPLE 14.2** If an amplifier with gain of  $-1000$  and feedback of  $\beta = -0.1$  has a gain change of  $20\%$  due to temperature, calculate the change in gain of the feedback amplifier.

**Solution:** Using Eq. (14.9), we get

$$\left| \frac{dA_f}{A_f} \right| \approx \left| \frac{1}{\beta A} \right| \left| \frac{dA}{A} \right| = \left| \frac{1}{-0.1(-1000)} (20\%) \right| = 0.2\%$$

The improvement is 100 times. Thus, whereas the amplifier gain changes from  $|A| = 1000$  by  $20\%$ , the gain with feedback changes from  $|A_f| = 100$  by only  $0.2\%$ .

## 14.3 PRACTICAL FEEDBACK CIRCUITS

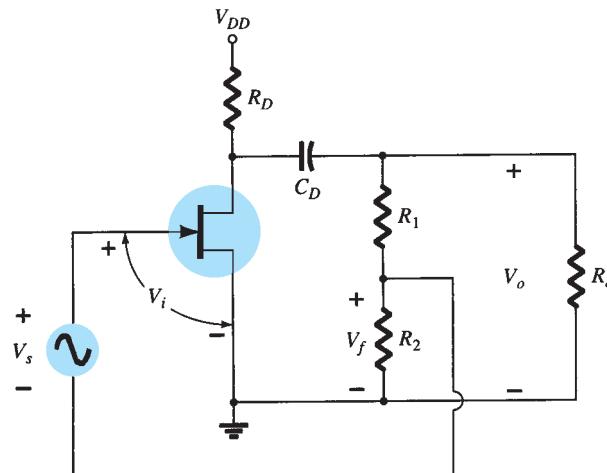
Examples of practical feedback circuits will provide a means of demonstrating the effect feedback has on the various connection types. This section provides only a basic introduction to this topic.

### Voltage-Series Feedback

Figure 14.7 shows an FET amplifier stage with voltage-series feedback. A part of the output signal ( $V_o$ ) is obtained using a feedback network of resistors  $R_1$  and  $R_2$ . The feedback voltage  $V_f$  is connected in series with the source signal  $V_s$ , their difference being the input signal  $V_i$ .

Without feedback the amplifier gain is

$$A = \frac{V_o}{V_i} = -g_m R_L \quad (14.10)$$



**FIG. 14.7**  
FET amplifier stage with voltage-series feedback.

where  $R_L$  is the parallel combination of resistors:

$$R_L = R_D R_o (R_1 + R_2) \quad (14.11)$$

The feedback network provides a feedback factor of

$$\beta = \frac{V_f}{V_o} = \frac{-R_2}{R_1 + R_2} \quad (14.12)$$

Using the values of  $A$  and  $\beta$  above in Eq. (14.2), we find the gain with negative feedback to be

$$A_f = \frac{A}{1 + \beta A} = \frac{-g_m R_L}{1 + [R_2 R_L / (R_1 + R_2)] g_m} \quad (14.13)$$

If  $\beta A \gg 1$ , we have

$$A_f \approx \frac{1}{\beta} = -\frac{R_1 + R_2}{R_2} \quad (14.14)$$

**EXAMPLE 14.3** Calculate the gain without and with feedback for the FET amplifier circuit of Fig. 14.7 and the following circuit values:  $R_1 = 80 \text{ k}\Omega$ ,  $R_2 = 20 \text{ k}\Omega$ ,  $R_o = 10 \text{ k}\Omega$ ,  $R_D = 10 \text{ k}\Omega$ , and  $g_m = 4000 \mu\text{S}$ .

**Solution:**

$$R_L \approx \frac{R_o R_D}{R_o + R_D} = \frac{10 \text{ k}\Omega (10 \text{ k}\Omega)}{10 \text{ k}\Omega + 10 \text{ k}\Omega} = 5 \text{ k}\Omega$$

Neglecting the 100-k $\Omega$  resistance of  $R_1$  and  $R_2$  in series gives

$$A = -g_m R_L = -(4000 \times 10^{-6} \mu\text{S})(5 \text{ k}\Omega) = -20$$

The feedback factor is

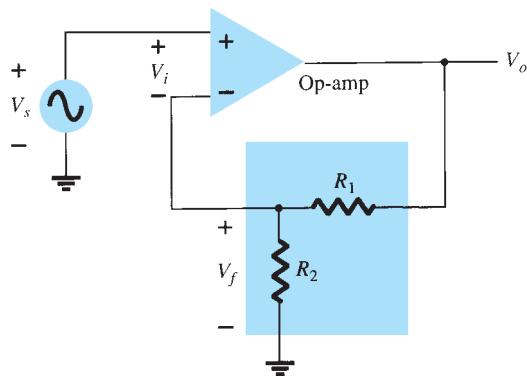
$$\beta = \frac{-R_2}{R_1 + R_2} = \frac{-20 \text{ k}\Omega}{80 \text{ k}\Omega + 20 \text{ k}\Omega} = -0.2$$

The gain with feedback is

$$A_f = \frac{A}{1 + \beta A} = \frac{-20}{1 + (-0.2)(-20)} = \frac{-20}{5} = -4$$

Figure 14.8 shows a voltage-series feedback connection using an op-amp. The gain of the op-amp,  $A$ , without feedback, is reduced by the feedback factor

$$\beta = \frac{R_2}{R_1 + R_2} \quad (14.15)$$



**FIG. 14.8**  
Voltage-series feedback in an op-amp connection.

**EXAMPLE 14.4** Calculate the amplifier gain of the circuit of Fig. 14.8 for op-amp gain  $A = 100,000$  and resistances  $R_1 = 1.8 \text{ k}\Omega$  and  $R_2 = 200 \Omega$ .

**Solution:**

$$\beta = \frac{R_2}{R_1 + R_2} = \frac{200 \Omega}{200 \Omega + 1.8 \text{ k}\Omega} = 0.1$$

$$A_f = \frac{A}{1 + \beta A} = \frac{100,000}{1 + (0.1)(100,000)} = \frac{100,000}{10,001} = 9.999$$

Note that since  $\beta A \gg 1$ ,

$$A_f \approx \frac{1}{\beta} = \frac{1}{0.1} = 10$$

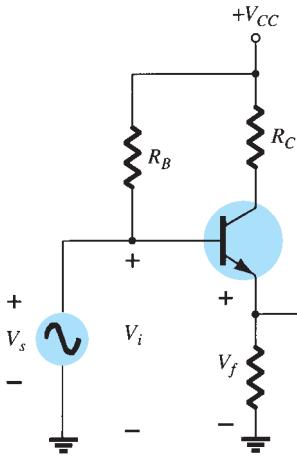


FIG. 14.9

Voltage-series feedback circuit (emitter-follower).

The emitter-follower circuit of Fig. 14.9 provides voltage-series feedback. The signal voltage  $V_s$  is the input voltage  $V_i$ . The output voltage  $V_o$  is also the feedback voltage in series with the input voltage. The amplifier, as shown in Fig. 14.9, provides the operation *with* feedback. The operation of the circuit without feedback provides  $V_f = 0$ , so that

$$A = \frac{V_o}{V_s} = \frac{h_{fe} I_b R_E}{V_s} = \frac{h_{fe} R_E (V_s/h_{ie})}{V_s} = \frac{h_{fe} R_E}{h_{ie}}$$

and

$$\beta = \frac{V_f}{V_o} = 1$$

The operation with feedback then provides that

$$A_f = \frac{V_o}{V_s} = \frac{A}{1 + \beta A} = \frac{h_{fe} R_E / h_{ie}}{1 + (1)(h_{fe} R_E / h_{ie})} = \frac{h_{fe} R_E}{h_{ie} + h_{fe} R_E}$$

For  $h_{fe} R_E \gg h_{ie}$ ,

$$A_f \approx 1$$

## Current-Series Feedback

Another feedback technique is to sample the output current  $I_o$  and return a proportional voltage in series with the input. Although it stabilizes the amplifier gain, the current-series feedback connection increases input resistance.

Figure 14.10 shows a single transistor amplifier stage. Since the emitter of this stage has an unbypassed emitter, it effectively has current-series feedback. The current through resistor  $R_E$  results in a feedback voltage that opposes the source signal applied, so that the output voltage  $V_o$  is reduced. To remove the current-series feedback, the emitter resistor must be either removed or bypassed by a capacitor (as is usually done).

**Without Feedback** Referring to the basic format of Fig. 14.2a and summarized in Table 14.1, we have

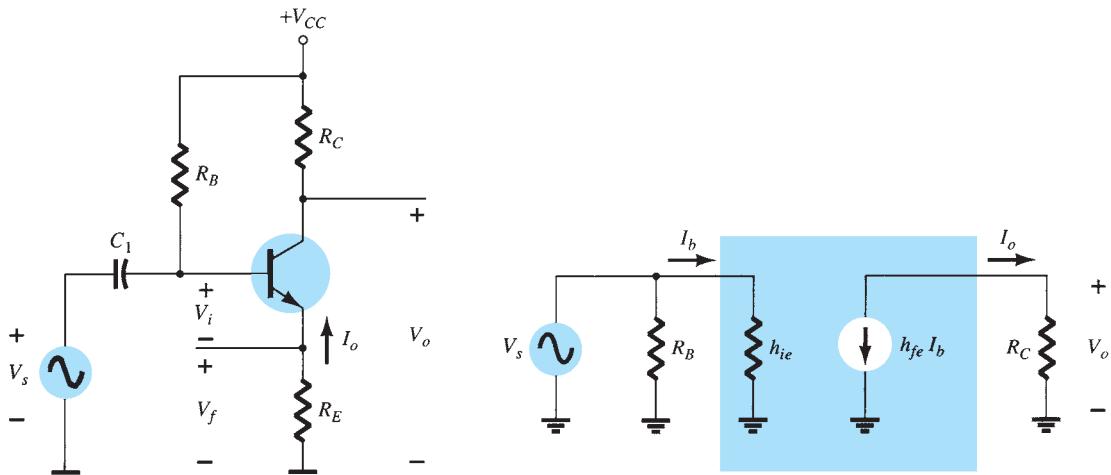
$$A = \frac{I_o}{V_i} = \frac{-I_b h_{fe}}{I_b h_{ie} + R_E} = \frac{-h_{fe}}{h_{ie} + R_E} \quad (14.16)$$

$$\beta = \frac{V_f}{I_o} = \frac{-I_o R_E}{I_o} = -R_E \quad (14.17)$$

The input and output impedances are, respectively,

$$Z_i = R_B \parallel (h_{ie} + R_E) \equiv h_{ie} + R_E \quad (14.18)$$

$$Z_o = R_C \quad (14.19)$$



(a)

(b)

FIG. 14.10

Transistor amplifier with unbypassed emitter resistor ( $R_E$ ) for current-series feedback: (a) amplifier circuit; (b) ac equivalent circuit without feedback.

### With Feedback

$$A_f = \frac{I_o}{V_s} = \frac{A}{1 + \beta A} = \frac{-h_{fe}/h_{ie}}{1 + (-R_E)\left(\frac{-h_{fe}}{h_{ie} + R_E}\right)} \cong \frac{-h_{fe}}{h_{ie} + h_{fe}R_E} \quad (14.20)$$

The input and output impedances are calculated as specified in Table 14.2:

$$Z_{if} = Z_i(1 + \beta A) \cong h_{ie}\left(1 + \frac{h_{fe}R_E}{h_{ie}}\right) = h_{ie} + h_{fe}R_E \quad (14.21)$$

$$Z_{of} = Z_o(1 + \beta A) = R_C\left(1 + \frac{h_{fe}R_E}{h_{ie}}\right) \quad (14.22)$$

The voltage gain  $A$  with feedback is

$$A_{vf} = \frac{V_o}{V_s} = \frac{I_o R_C}{V_s} = \left(\frac{I_o}{V_s}\right) R_C = A_f R_C \cong \frac{-h_{fe} R_C}{h_{ie} + h_{fe} R_E} \quad (14.23)$$

**EXAMPLE 14.5** Calculate the voltage gain of the circuit of Fig. 14.11.

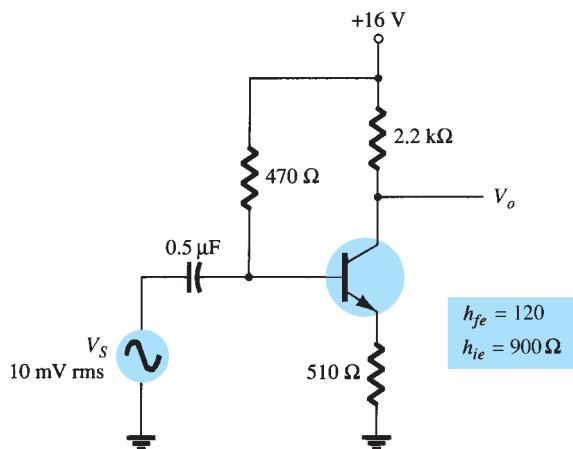


FIG. 14.11

BJT amplifier with current-series feedback for Example 14.5.

**Solution:** Without feedback,

$$A = \frac{I_o}{V_i} = \frac{-h_{fe}}{h_{ie} + R_E} = \frac{-120}{900 + 510} = -0.085$$

$$\beta = \frac{V_f}{I_o} = -R_E = -510$$

The factor  $(1 + \beta A)$  is then

$$1 + \beta A = 1 + (-0.085)(-510) = 44.35$$

The gain with feedback is then

$$A_f = \frac{I_o}{V_s} = \frac{A}{1 + \beta A} = \frac{-0.085}{44.35} = -1.92 \times 10^{-3}$$

and the voltage gain with feedback  $A_{vf}$  is

$$A_{vf} = \frac{V_o}{V_s} = A_f R_C = (-1.92 \times 10^{-3})(2.2 \times 10^3) = -4.2$$

Without feedback ( $R_E = 0$ ), the voltage gain is

$$A_v = \frac{-R_C}{r_e} = \frac{-2.2 \times 10^3}{7.5} = -293.3$$

### Voltage-Shunt Feedback

The constant-gain op-amp circuit of Fig. 14.12a provides voltage-shunt feedback. Referring to Fig. 14.2b and Table 14.1 and the op-amp ideal characteristics  $I_i = 0$ ,  $V_i = 0$ , and voltage gain of infinity, we have

$$A = \frac{V_o}{I_i} = \infty \quad (14.24)$$

$$\beta = \frac{I_f}{V_o} = \frac{-1}{R_o} \quad (14.25)$$

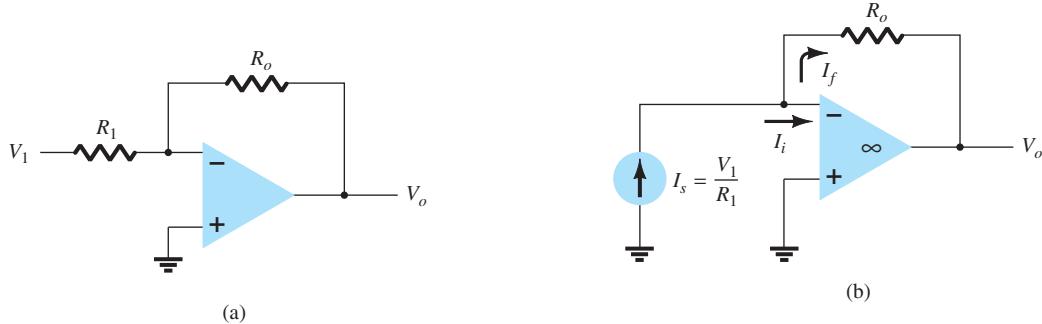


FIG. 14.12

Voltage-shunt negative feedback amplifier: (a) constant-gain circuit; (b) equivalent circuit.

The gain with feedback is then

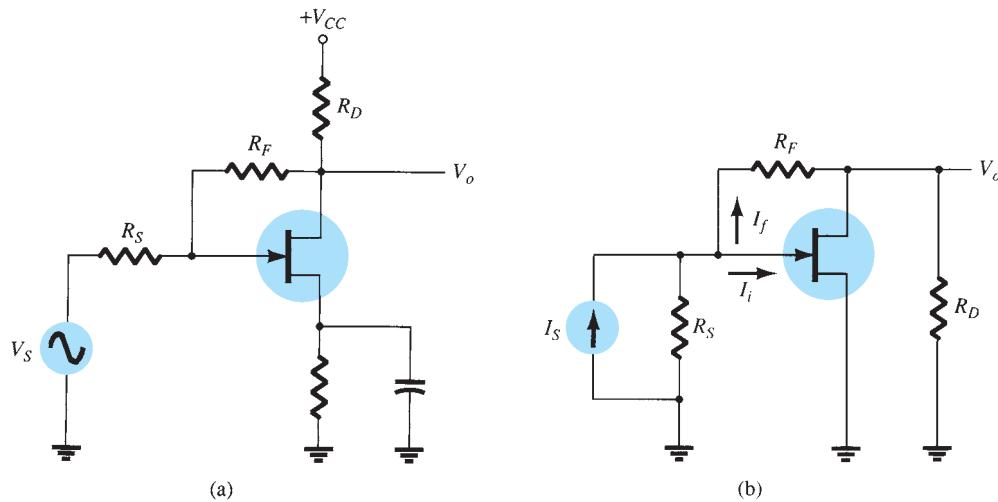
$$A_f = \frac{V_o}{I_s} = \frac{V_o}{I_i} = \frac{A}{1 + \beta A} = \frac{1}{\beta} = -R_o \quad (14.26)$$

This is a transfer resistance gain. The more usual gain is the voltage gain with feedback,

$$A_{vf} = \frac{V_o}{I_s} \frac{I_s}{V_1} = (-R_o) \frac{1}{R_1} = \frac{-R_o}{R_1} \quad (14.27)$$

The circuit of Fig. 14.13 is a voltage-shunt feedback amplifier using an FET with no feedback,  $V_f = 0$ .

$$A = \frac{V_o}{I_i} \cong -g_m R_D R_S \quad (14.28)$$


**FIG. 14.13**

Voltage-shunt feedback amplifier using an FET: (a) circuit; (b) equivalent circuit.

The feedback is

$$\beta = \frac{I_f}{V_o} = \frac{-1}{R_F} \quad (14.29)$$

With feedback, the gain of the circuit is

$$\begin{aligned} A_f &= \frac{V_o}{I_s} = \frac{A}{1 + \beta A} = \frac{-g_m R_D R_S}{1 + (-1/R_F)(-g_m R_D R_S)} \\ &= \frac{-g_m R_D R_S R_F}{R_F + g_m R_D R_S} \end{aligned} \quad (14.30)$$

The voltage gain of the circuit with feedback is then

$$\begin{aligned} A_{vf} &= \frac{V_o}{I_s} \frac{I_s}{V_s} = \frac{-g_m R_D R_S R_F}{R_F + g_m R_D R_S} \left( \frac{1}{R_S} \right) \\ &= \frac{-g_m R_D R_F}{R_F + g_m R_D R_S} = (-g_m R_D) \frac{R_F}{R_F + g_m R_D R_S} \end{aligned} \quad (14.31)$$

**EXAMPLE 14.6** Calculate the voltage gain with and without feedback for the circuit of Fig. 14.13a with values of  $g_m = 5 \text{ mS}$ ,  $R_D = 5.1 \text{ k}\Omega$ ,  $R_S = 1 \text{ k}\Omega$ , and  $R_F = 20 \text{ k}\Omega$ .

**Solution:** Without feedback, the voltage gain is

$$A_v = -g_m R_D = -(5 \times 10^{-3})(5.1 \times 10^3) = -25.5$$

With feedback the gain is reduced to

$$\begin{aligned} A_{vf} &= (-g_m R_D) \frac{R_F}{R_F + g_m R_D R_S} \\ &= (-25.5) \frac{20 \times 10^3}{(20 \times 10^3) + (5 \times 10^{-3})(5.1 \times 10^3)(1 \times 10^3)} \\ &= -25.5(0.44) = -11.2 \end{aligned}$$

## 14.4 FEEDBACK AMPLIFIER-PHASE AND FREQUENCY CONSIDERATIONS

So far we have considered the operation of a feedback amplifier in which the feedback signal was *opposite* to the input signal—negative feedback. In any practical circuit this condition occurs only for some mid-frequency range of operation. We know that an amplifier



**Harry Nyquist** was born in Sweden in 1889. He immigrated to the United States in 1907, and died in Texas in 1976. He received a Ph.D. in physics from Yale University in 1917. He worked at AT&T's Department of Development and Research and at Bell Telephone Laboratories from 1917 until his retirement in 1954. As an engineer at Bell Laboratories, Nyquist did important work on thermal noise, the stability of feedback amplifiers, telegraphy, facsimile, television, and other important communications problems. In 1932, he published a classic paper on stability of feedback amplifiers: The Nyquist stability criterion can now be found in all textbooks on feedback control theory.

(Courtesy of AT&T Archives and History Center)

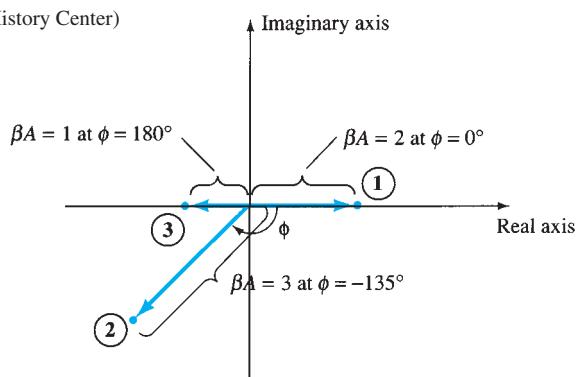


FIG. 14.14  
Complex plane showing typical gain-phase points.

An example of the Nyquist criterion is demonstrated by the curves in Fig. 14.16. The Nyquist plot in Fig. 14.16a is stable since it does not encircle the  $-1$  point, whereas that shown in Fig. 14.16b is unstable since the curve does encircle the  $-1$  point. Keep in mind that encircling the  $-1$  point means that at a phase shift of  $180^\circ$  the loop gain ( $\beta A$ ) is greater than 1; therefore, the feedback signal is in phase with the input and large enough to result in a larger input signal than that applied, with the result that oscillation occurs.

gain will change with frequency, dropping off at high frequencies from the mid-frequency value. In addition, the phase shift of an amplifier will also change with frequency.

If, as the frequency increases, the phase shift changes, then some of the feedback signal will *add* to the input signal. It is then possible for the amplifier to break into oscillations due to positive feedback. If the amplifier oscillates at some low or high frequency, it is no longer useful as an amplifier. Proper feedback-amplifier design requires that the circuit be stable at *all* frequencies, not merely those in the range of interest. Otherwise, a transient disturbance could cause a seemingly stable amplifier to suddenly start oscillating.

### Nyquist Criterion

In judging the stability of a feedback amplifier as a function of frequency, the  $\beta A$  product and the phase shift between input and output are the determining factors. One of the most popular techniques used to investigate stability is the Nyquist method. A Nyquist diagram is used to plot gain and phase shift as a function of frequency on a complex plane. The Nyquist plot, in effect, combines the two Bode plots of gain versus frequency and phase shift versus frequency on a single plot. A Nyquist plot is used to quickly show whether an amplifier is stable for all frequencies and how stable the amplifier is relative to some gain or phase-shift criteria.

As a start, consider the *complex plane* shown in Fig. 14.14. A few points of various gain ( $\beta A$ ) values are shown at a few different phase-shift angles. By using the positive real axis as reference ( $0^\circ$ ), we see a magnitude of  $\beta A = 2$  at a phase shift of  $0^\circ$  at point 1. Additionally, a magnitude of  $\beta A = 3$  at a phase shift of  $-135^\circ$  is shown at point 2 and a magnitude/phase of  $\beta A = 1$  at  $180^\circ$  is shown at point 3. Thus points on this plot can represent *both* gain magnitude of  $\beta A$  and phase shift. If the points representing gain and phase shift for an amplifier circuit are plotted at increasing frequency, then a Nyquist plot is obtained as shown by the plot in Fig. 14.15. At the origin, the gain is 0 at a frequency of 0 (for *RC*-type coupling). At increasing frequency, points  $f_1, f_2$ , and  $f_3$  and the phase shift increase, as does the magnitude of  $\beta A$ . At a representative frequency  $f_4$ , the value of  $A$  is the vector length from the origin to point  $f_4$  and the phase shift is the angle  $\phi$ . At a frequency  $f_5$ , the phase shift is  $180^\circ$ . At higher frequencies, the gain is shown to decrease back to 0.

The Nyquist criterion for stability can be stated as follows:

**The amplifier is unstable if the Nyquist curve encircles (encircles) the  $-1$  point, and it is stable otherwise.**

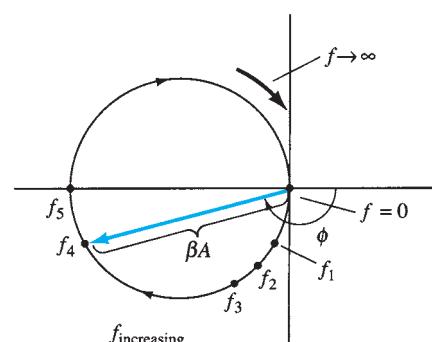
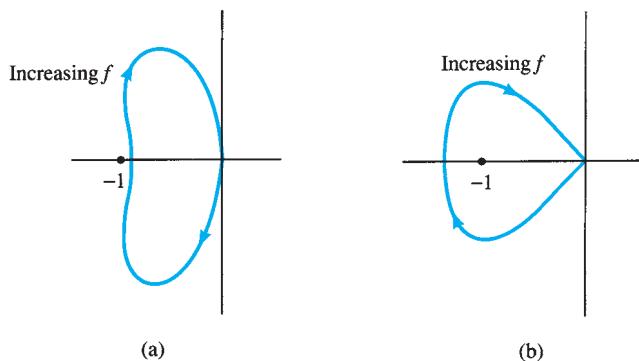


FIG. 14.15  
Nyquist plot.

**FIG. 14.16**

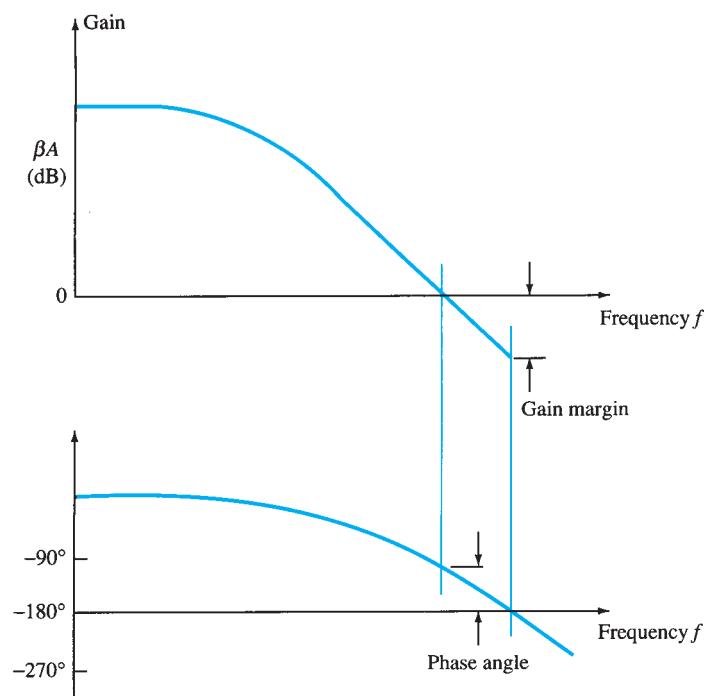
Nyquist plots showing stability conditions: (a) stable; (b) unstable.

## Gain and Phase Margins

From the Nyquist criterion, we know that a feedback amplifier is stable if the loop gain ( $\beta A$ ) is less than unity (0 dB) when its phase angle is  $180^\circ$ . We can additionally determine some margins of stability to indicate how close to instability the amplifier is. That is, if the gain ( $\beta A$ ) is less than unity but, say, 0.95 in value, this would not be as relatively stable as another amplifier having, say,  $\beta A = 0.7$  (both measured at  $180^\circ$ ). Of course, amplifiers with loop gains 0.95 and 0.7 are both stable, but one is closer to instability, if the loop gain increases, than the other. We can define the following terms:

*Gain margin (GM)* is defined as the negative of the value of  $|\beta A|$  in decibels at the frequency at which the phase angle is  $180^\circ$ . Thus, 0 dB, equal to a value of  $\beta A = 1$ , is on the border of stability and any negative decibel value is stable. The GM may be evaluated in decibels from the curve of Fig. 14.17.

*Phase margin (PM)* is defined as the angle of  $180^\circ$  minus the magnitude of the angle at which the value  $|\beta A|$  is unity (0 dB). The PM may also be evaluated directly from the curve of Fig. 14.17.

**FIG. 14.17**

Bode plots showing gain and phase margins.

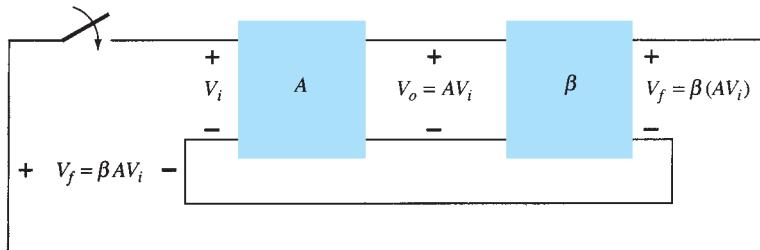
## 14.5 OSCILLATOR OPERATION

The use of positive feedback that results in a feedback amplifier having closed-loop gain  $|A_f|$  greater than 1 and satisfies the phase conditions will result in operation as an oscillator circuit. An oscillator circuit then provides a varying output signal. If the output signal varies sinusoidally, the circuit is referred to as a *sinusoidal oscillator*. If the output voltage rises quickly to one voltage level and later drops quickly to another voltage level, the circuit is generally referred to as a *pulse* or *square-wave oscillator*.

To understand how a feedback circuit performs as an oscillator, consider the feedback circuit of Fig. 14.18. When the switch at the amplifier input is open, no oscillation occurs. Consider that we have a *fictitious* voltage at the amplifier input  $V_i$ . This results in an output voltage  $V_o = AV_i$  after the amplifier stage and in a voltage  $V_f = \beta(AV_i)$  after the feedback stage. Thus, we have a feedback voltage  $V_f = \beta AV_i$ , where  $\beta A$  is referred to as the *loop gain*. If the circuits of the base amplifier and feedback network provide  $\beta A$  of a correct magnitude and phase,  $V_f$  can be made equal to  $V_i$ . Then, when the switch is closed and the fictitious voltage  $V_i$  is removed, the circuit will continue operating since the feedback voltage is sufficient to drive the amplifier and feedback circuits, resulting in a proper input voltage to sustain the loop operation. The output waveform will still exist after the switch is closed if the condition

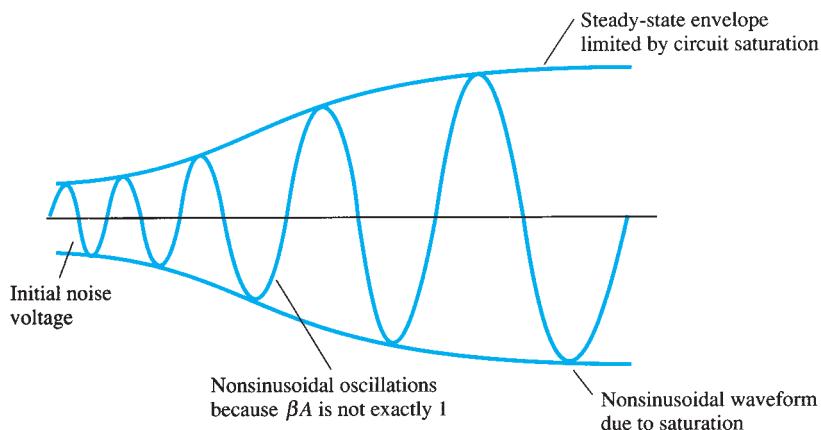
$$\beta A = 1 \quad (14.32)$$

is met. This is known as the *Barkhausen criterion* for oscillation.



**FIG. 14.18**  
Feedback circuit used as an oscillator.

In reality, no input signal is needed to start the oscillator going. Only the condition  $\beta A = 1$  must be satisfied for self-sustained oscillations to result. In practice,  $\beta A$  is made greater than 1 and the system is started oscillating by amplifying noise voltage, which is always present. Saturation factors in the practical circuit provide an “average” value of  $\beta A$  of 1. The resulting waveforms are never exactly sinusoidal. However, the closer the value  $\beta A$  is to exactly 1, the more nearly sinusoidal is the waveform. Figure 14.19 shows how the noise signal results in a buildup of a steady-state oscillation condition.



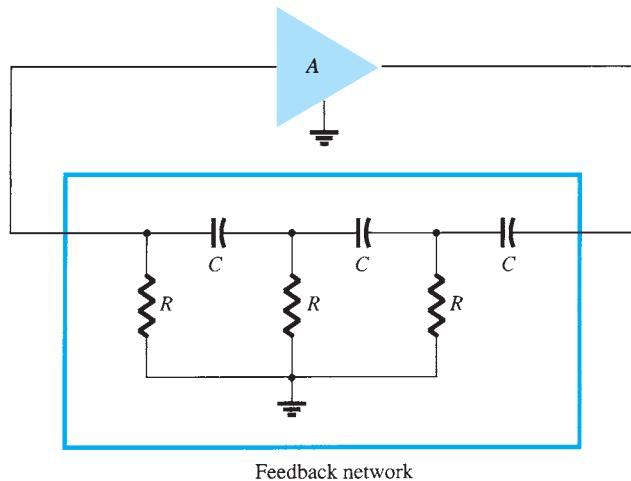
**FIG. 14.19**  
Buildup of steady-state oscillations.

Another way of seeing how the feedback circuit provides operation as an oscillator is obtained by noting the denominator in the basic feedback equation (14.2),  $A_f = A/(1 + \beta A)$ . When  $\beta A = -1$  or magnitude 1 at a phase angle of  $180^\circ$ , the denominator becomes 0 and the gain with feedback  $A_f$  becomes infinite. Thus, an infinitesimal signal (noise voltage) can provide a measurable output voltage, and the circuit acts as an oscillator even without an input signal.

The remainder of this chapter is devoted to various oscillator circuits that use a variety of components. Practical examples are included so that workable circuits in each of the various cases are discussed.

## 14.6 PHASE-SHIFT OSCILLATOR

An example of an oscillator circuit that follows the basic development of a feedback circuit is the *phase-shift oscillator*. An idealized version of this circuit is shown in Fig. 14.20. Recall that the requirements for oscillation are that the loop gain  $\beta A$  is greater than unity and that the phase shift around the feedback network is  $180^\circ$  (providing positive feedback). In the present idealization, we are considering the feedback network to be driven by a perfect source (zero source impedance) and the output of the feedback network to be connected into a perfect load (infinite load impedance). The idealized case will allow development of the theory behind the operation of the phase-shift oscillator. Practical circuit versions will then be considered.



**FIG. 14.20**  
Idealized phase-shift oscillator.

Concentrating our attention on the phase-shift network, we are interested in the attenuation of the network at the frequency at which the phase shift is exactly  $180^\circ$ . Using classical network analysis, we find that

$$f = \frac{1}{2\pi RC\sqrt{6}} \quad (14.33)$$

$$\beta = \frac{1}{29} \quad (14.34)$$

and the phase shift is  $180^\circ$ .

For the loop gain  $\beta A$  to be greater than unity, the gain of the amplifier stage must be greater than  $1/\beta$  or 29:

$$A > 29 \quad (14.35)$$

When considering the operation of the feedback network, one might naively select the values of  $R$  and  $C$  to provide (at a specific frequency)  $60^\circ$ -phase shift per section for three sections, resulting in a  $180^\circ$  phase shift, as desired. This, however, is not the case, since each section of the  $RC$  in the feedback network loads down the previous one. The net result that the *total* phase shift be  $180^\circ$  is all that is important. The frequency given by Eq. (14.33) is

that at which the *total* phase shift is  $180^\circ$ . If one measured the phase shift per  $RC$  section, each section would not provide the same phase shift (although the overall phase shift is  $180^\circ$ ). If it were desired to obtain exactly a  $60^\circ$  phase shift for each of three stages, then emitter-follower stages would be needed for each  $RC$  section to prevent each from being loaded from the following circuit.

### FET Phase-Shift Oscillator

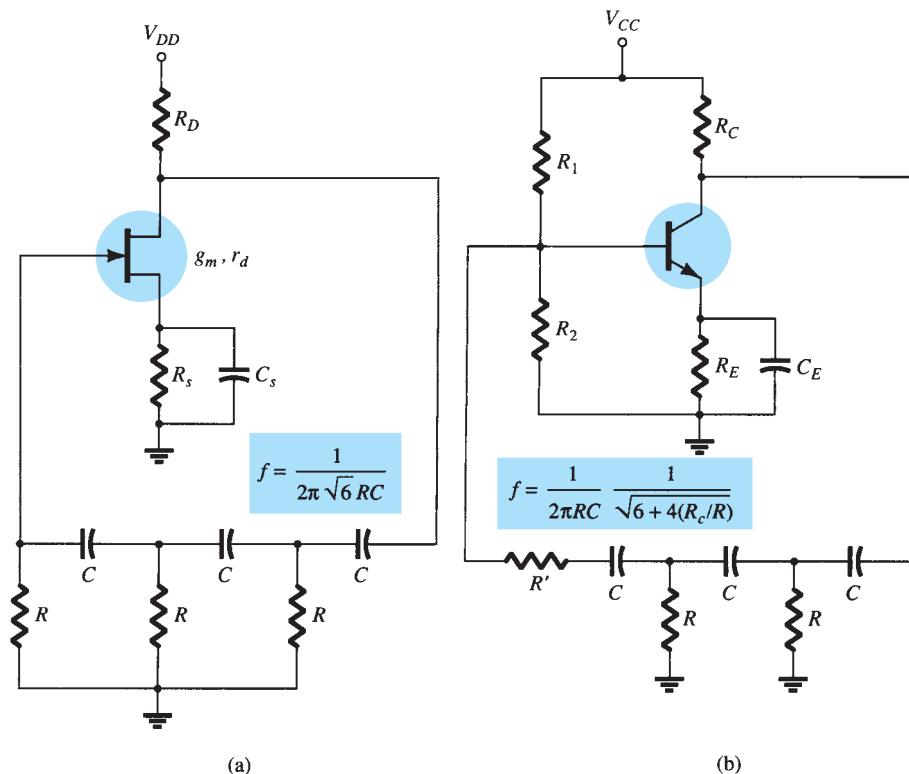
A practical version of a phase-shift oscillator circuit is shown in Fig. 14.21a. The circuit is drawn to show clearly the amplifier and feedback network. The amplifier stage is self-biased with a capacitor bypassed source resistor  $R_S$  and a drain bias resistor  $R_D$ . The FET device parameters of interest are  $g_m$  and  $r_d$ . From FET amplifier theory, the amplifier gain magnitude is calculated from

$$|A| = g_m R_L \quad (14.36)$$

where  $R_L$  in this case is the parallel resistance of  $R_D$  and  $r_d$ ,

$$R_L = \frac{R_D r_d}{R_D + r_d} \quad (14.37)$$

We shall assume as a very good approximation that the input impedance of the FET amplifier stage is infinite. This assumption is valid as long as the oscillator operating frequency is low enough so that FET capacitive impedances can be neglected. The output impedance of the amplifier stage given by  $R_L$  should also be small compared to the impedance seen looking into the feedback network so that no attenuation due to loading occurs. In practice, these considerations are not always negligible, and the amplifier stage gain is then selected somewhat larger than the needed factor of 29 to assure oscillator action.



**FIG. 14.21**  
Practical phase-shift oscillator circuits: (a) FET version; (b) BJT version.

**EXAMPLE 14.7** It is desired to design a phase-shift oscillator (as in Fig. 14.21a) using an FET having  $g_m = 5000 \mu\text{S}$ ,  $r_d = 40 \text{ k}\Omega$ , and a feedback circuit value of  $R = 10 \text{ k}\Omega$ . Select the value of  $C$  for oscillator operation at 1 kHz and  $R_D$  for  $A > 29$  to ensure oscillator action.

**Solution:** Equation (14.33) is used to solve for the capacitor value. Since  $f = 1/(2\pi RC\sqrt{6})$ , we can solve for  $C$ :

$$C = \frac{1}{2\pi R f \sqrt{6}} = \frac{1}{(6.28)(10 \times 10^3)(1 \times 10^3)(2.45)} = 6.5 \text{ nF}$$

Using Eq. (14.36), we solve for  $R_L$  to provide a gain of, say,  $A = 40$  (this allows for some loading between  $R_L$  and the feedback network input impedance):

$$R_L = \frac{|A|}{g_m} = \frac{40}{5000 \times 10^{-6}} = 8 \text{ k}\Omega$$

Using Eq. (14.37), we solve for  $R_D = 10 \text{ k}\Omega$ .

### Transistor Phase-Shift Oscillator

If a transistor is used as the active element of the amplifier stage, the output of the feedback network is loaded appreciably by the relatively low input resistance ( $h_{ie}$ ) of the transistor. Of course, an emitter-follower input stage followed by a common-emitter amplifier stage could be used. If a single transistor stage is desired, however, the use of voltage-shunt feedback (as shown in Fig. 14.21b) is more suitable. In this connection, the feedback signal is coupled through the feedback resistor  $R'$  in series with the amplifier stage input resistance ( $R_i$ ).

Analysis of the ac circuit provides the following equation for the resulting oscillator frequency:

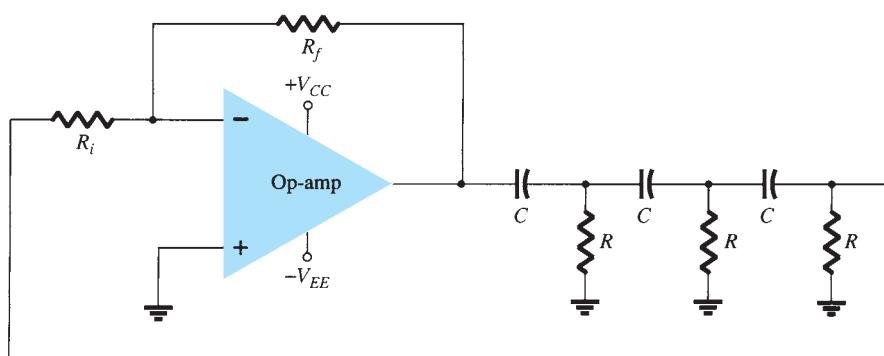
$$f = \frac{1}{2\pi RC} \frac{1}{\sqrt{6 + 4(R_C/R)}} \quad (14.38)$$

For the loop gain to be greater than unity, the requirement on the current gain of the transistor is found to be

$$h_{fe} > 23 + 29 \frac{R}{R_C} + 4 \frac{R_C}{R} \quad (14.39)$$

### IC Phase-Shift Oscillator

As IC circuits have become more popular, they have been adapted to operate in oscillator circuits. One need buy only an op-amp to obtain an amplifier circuit of stabilized gain setting and incorporate some means of signal feedback to produce an oscillator circuit. For example, a phase-shift oscillator is shown in Fig. 14.22. The output of the op-amp is fed to a three-stage  $RC$  network, which provides the needed  $180^\circ$  of phase shift (at an attenuation factor of 1/29). If the op-amp provides gain (set by resistors  $R_i$  and  $R_f$ ) of greater than 29,



**FIG. 14.22**  
Phase-shift oscillator using an op-amp.

a loop gain greater than unity results and the circuit acts as an oscillator [oscillator frequency is given by Eq. (14.33)].

### 14.7 WIEN BRIDGE OSCILLATOR

A practical oscillator circuit uses an op-amp and  $RC$  bridge circuit, with the oscillator frequency set by the  $R$  and  $C$  components. Figure 14.23 shows a basic version of a Wien bridge oscillator circuit. Note the basic bridge connection. Resistors  $R_1$  and  $R_2$  and capacitors  $C_1$  and  $C_2$  form the frequency-adjustment elements, and resistors  $R_3$  and  $R_4$  form part of the feedback path. The op-amp output is connected as the bridge input at points  $a$  and  $c$ . The bridge circuit output at points  $b$  and  $d$  is the input to the op-amp.

Neglecting loading effects of the op-amp input and output impedances, the analysis of the bridge circuit results in

$$\frac{R_3}{R_4} = \frac{R_1}{R_2} + \frac{C_2}{C_1} \quad (14.40)$$

and

$$f_o = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}} \quad (14.41)$$

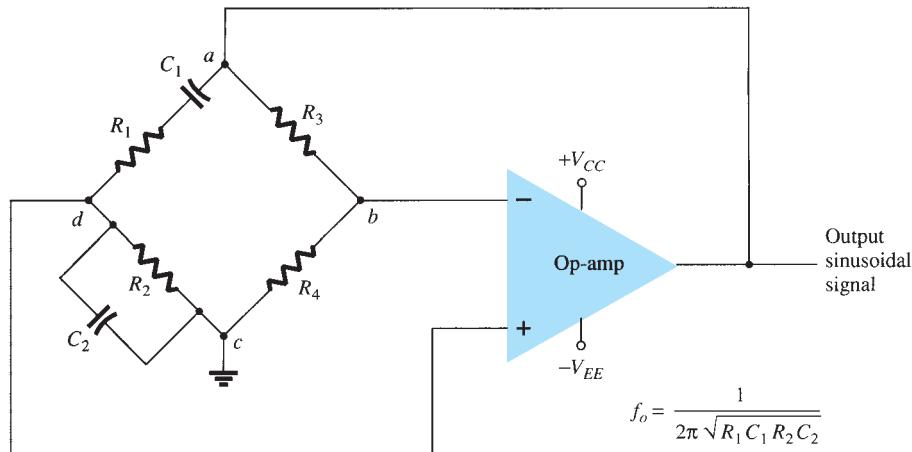
If, in particular, the values are  $R_1 = R_2 = R$  and  $C_1 = C_2 = C$ , the resulting oscillator frequency is

$$f_o = \frac{1}{2\pi RC} \quad (14.42)$$

and

$$\frac{R_3}{R_4} = 2 \quad (14.43)$$

Thus a ratio of  $R_3$  to  $R_4$  greater than 2 will provide sufficient loop gain for the circuit to oscillate at the frequency calculated using Eq. (14.42).



**FIG. 14.23**  
Wien bridge oscillator circuit using an op-amp amplifier.

**EXAMPLE 14.8** Calculate the resonant frequency of the Wien bridge oscillator of Fig. 14.24.

**Solution:** Using Eq. (14.42) yields

$$f_o = \frac{1}{2\pi RC} = \frac{1}{2\pi(51 \times 10^3)(0.001 \times 10^{-6})} = 3120.7 \text{ Hz}$$

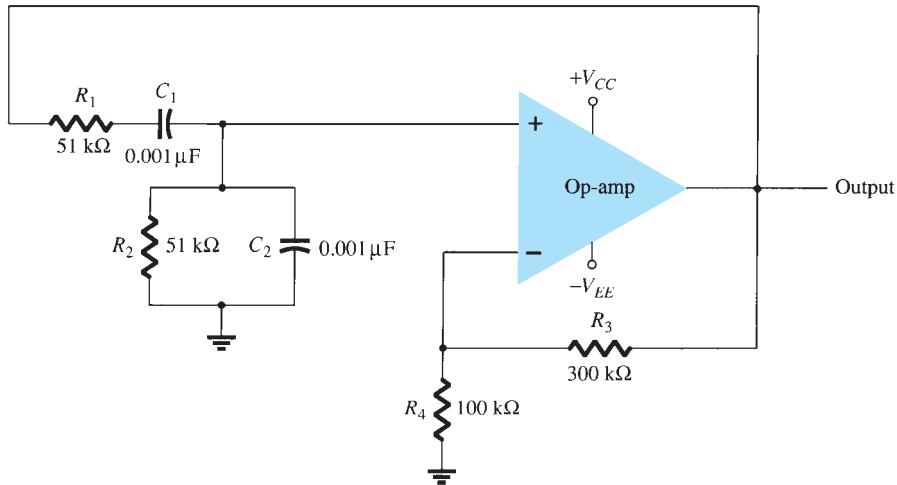


FIG. 14.24

Wien bridge oscillator circuit for Example 14.8.

**EXAMPLE 14.9** Design the  $RC$  elements of a Wien bridge oscillator as in Fig. 14.24 for operation at  $f_o = 10 \text{ kHz}$ .

**Solution:** Using equal values of  $R$  and  $C$ , we can select  $R = 100 \text{ k}\Omega$  and calculate the required value of  $C$  using Eq. (14.42):

$$C = \frac{1}{2\pi f_o R} = \frac{1}{6.28(10 \times 10^3)(100 \times 10^3)} = \frac{10^{-9}}{6.28} = 159 \text{ pF}$$

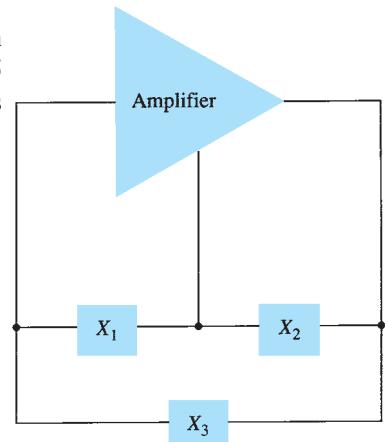
We can use  $R_3 = 300 \text{ k}\Omega$  and  $R_4 = 100 \text{ k}\Omega$  to provide a ratio  $R_3/R_4$  greater than 2 for oscillation to take place.

## 14.8 TUNED OSCILLATOR CIRCUIT

### Tuned-Input, Tuned-Output Oscillator Circuits

A variety of circuits can be built using that shown in Fig. 14.25 by providing tuning in both the input and output sections of the circuit. Analysis of the circuit of Fig. 14.25 reveals that the following types of oscillators are obtained when the reactance elements are as designated:

Oscillator Type	Reactance Element		
	$X_1$	$X_2$	$X_3$
Colpitts oscillator	$C$	$C$	$L$
Hartley oscillator	$L$	$L$	$C$
Tuned input, tuned output	$LC$	$LC$	—



### Colpitts Oscillator

**FET Colpitts Oscillator** A practical version of an FET Colpitts oscillator is shown in Fig. 14.26. The circuit is basically the same form as shown in Fig. 14.25 with the addition of the components needed for dc bias of the FET amplifier. The oscillator frequency can be found to be

$$f_o = \frac{1}{2\pi\sqrt{LC_{eq}}} \quad (14.44)$$

where

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} \quad (14.45)$$

FIG. 14.25

Basic configuration of resonant circuit oscillator.



**Edwin Henry Colpitts** (1872–1949) was a communications pioneer best known for his invention of the Colpitts oscillator. In 1915, his Western Electric team successfully demonstrated the first transatlantic radio telephone. In 1895 he entered Harvard University where he studied physics and mathematics. He received a B.A. in 1896 and a master's degree in 1897 from that institution. In 1899, Colpitts accepted a position with American Bell Telephone Company. He moved to Western Electric in 1907. His colleague Ralph Hartley invented an inductive coupling oscillator, which Colpitts improved in 1915. Colpitts served in the U.S. Army Signal Corps during World War I and spent some time in France as a staff officer involved with military communication. Colpitts died at home in 1949 in Orange, New Jersey.

(Courtesy of AT&T Archives and History Center)

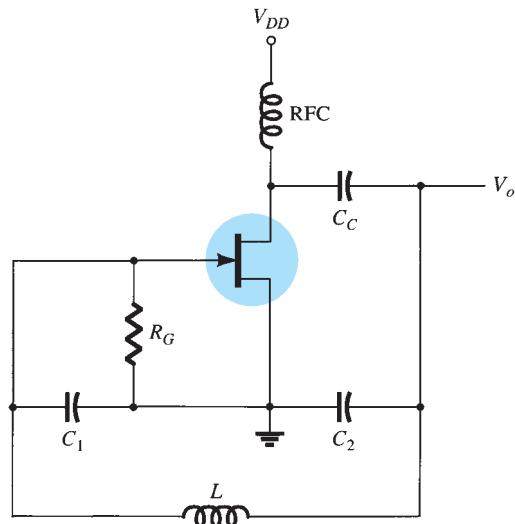


FIG. 14.26  
FET Colpitts oscillator.

**Transistor Colpitts Oscillator** A transistor Colpitts oscillator circuit can be made as shown in Fig. 14.27. The circuit frequency of oscillation is given by Eq. (14.44).

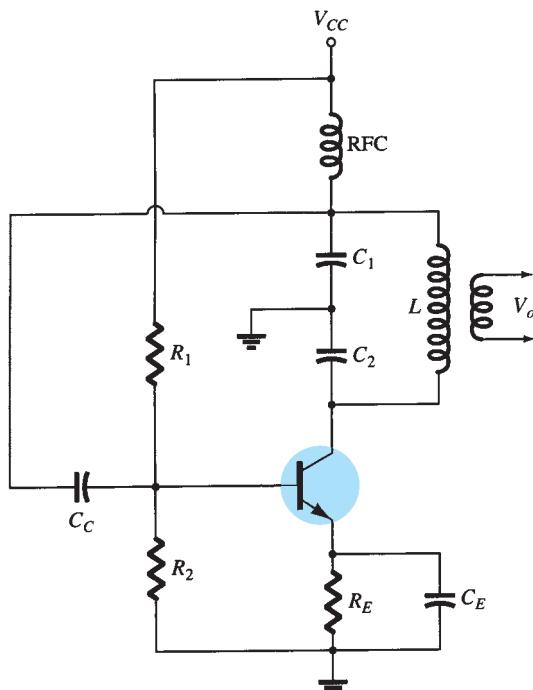


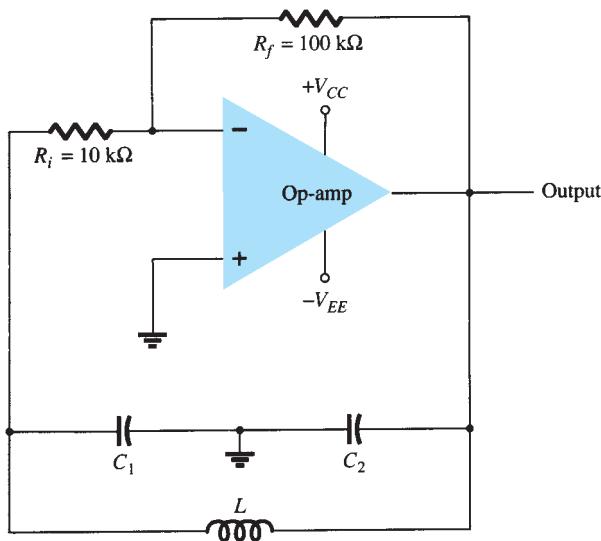
FIG. 14.27  
Transistor Colpitts oscillator.

**IC Colpitts Oscillator** An op-amp Colpitts oscillator circuit is shown in Fig. 14.28. Again, the op-amp provides the basic amplification needed, and the oscillator frequency is set by an  $LC$  feedback network of a Colpitts configuration. The oscillator frequency is given by Eq. (14.44).

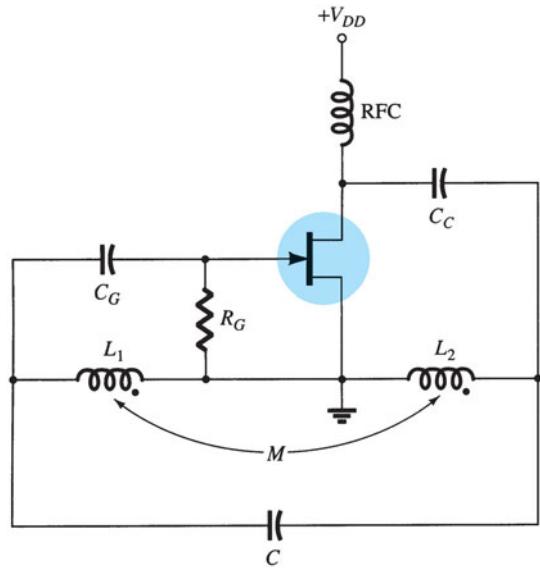
### Hartley Oscillator

If the elements in the basic resonant circuit of Fig. 14.25 are  $X_1$  and  $X_2$  (inductors) and  $X_3$  (capacitor), the circuit is a Hartley oscillator.

**FET Hartley Oscillator** An FET Hartley oscillator circuit is shown in Fig. 14.29. The circuit is drawn so that the feedback network conforms to the form shown in the basic resonant circuit (Fig. 14.25). Note, however, that inductors  $L_1$  and  $L_2$  have a mutual coupling  $M$ ,



**FIG. 14.28**  
Op-amp Colpitts oscillator.



**FIG. 14.29**  
FET Hartley oscillator.

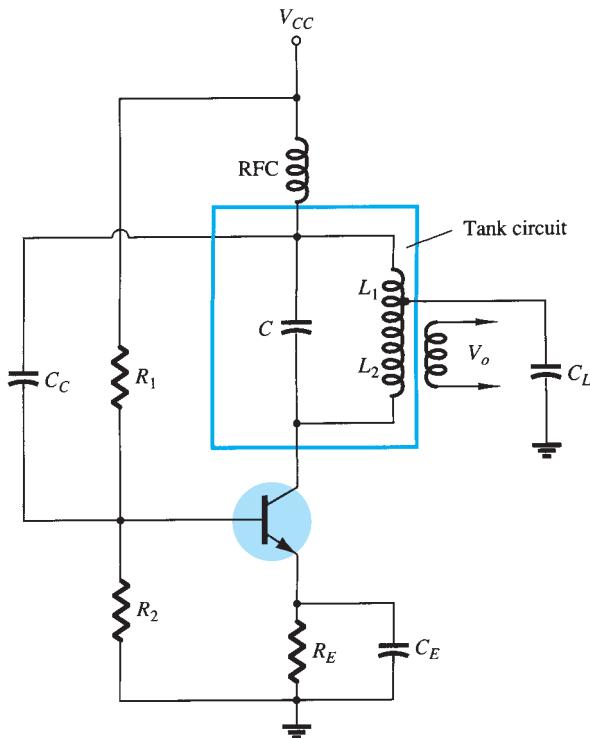
which must be taken into account in determining the equivalent inductance for the resonant tank circuit. The circuit frequency of oscillation is then given approximately by

$$f_o = \frac{1}{2\pi\sqrt{L_{eq}C}} \quad (14.46)$$

with

$$L_{eq} = L_1 + L_2 + 2M \quad (14.47)$$

**Transistor Hartley Oscillator** Figure 14.30 shows a transistor Hartley oscillator circuit. The circuit operates at a frequency given by Eq. (14.46).



**FIG. 14.30**

Transistor Hartley oscillator circuit.



**Ralph Hartley** was born in Nevada in 1888 and attended the University of Utah, receiving an A.B. degree in 1909. He became a Rhodes Scholar at Oxford University in 1910 and received a B.A. degree in 1912 and a B.Sc. degree in 1913.

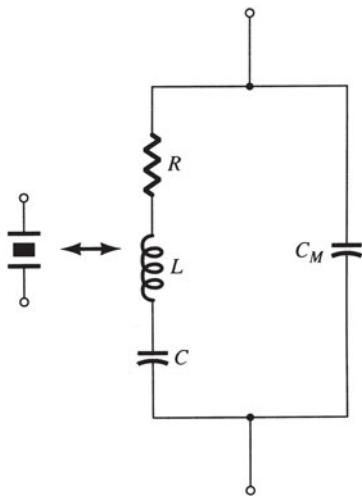
He returned to the United States and was employed at the Research Laboratory of the Western Electric Company. In 1915 he was in charge of radio receiver development for Bell Systems. He developed the Hartley oscillator and also a neutralizing circuit to eliminate triode singing resulting from internal coupling. During World War I he established the principles that led to sound-type directional finders. He retired from Bell Labs in 1950 and died on May 1, 1970.

(Courtesy of AT&T Archives and History Center)

## 14.9 CRYSTAL OSCILLATOR

A crystal oscillator is basically a tuned-circuit oscillator using a piezoelectric crystal as a resonant tank circuit. The crystal (usually quartz) has a greater stability in holding constant at whatever frequency the crystal is originally cut to operate. Crystal oscillators are used whenever great stability is required, such as in communication transmitters and receivers.

### Characteristics of a Quartz Crystal



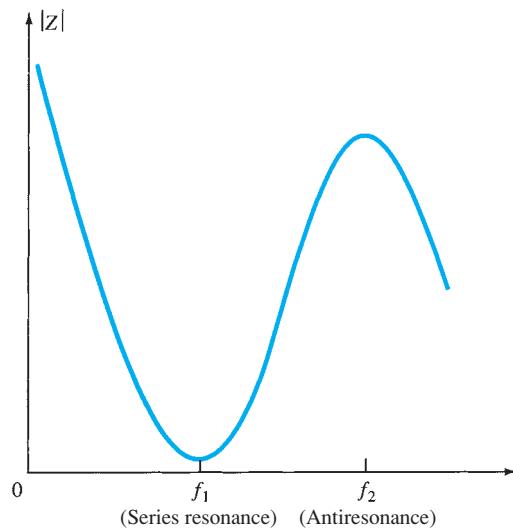
**FIG. 14.31**

Electrical equivalent circuit of a crystal.

A quartz crystal (one of a number of crystal types) exhibits the property that when mechanical stress is applied across one set of its faces, a difference of potential develops across the opposite faces. This property of a crystal is called the *piezoelectric effect*. Similarly, a voltage applied across one set of faces of the crystal causes mechanical distortion in the crystal shape.

When alternating voltage is applied to a crystal, mechanical vibrations are set up—these vibrations having a natural resonant frequency dependent on the crystal. Although the crystal has electromechanical resonance, we can represent the crystal action by an equivalent electrical resonant circuit as shown in Fig. 14.31. The inductor  $L$  and capacitor  $C$  represent electrical equivalents of crystal mass and compliance, respectively, whereas resistance  $R$  is an electrical equivalent of the crystal structure's internal friction. The shunt capacitance  $C_M$  represents the capacitance due to mechanical mounting of the crystal. Because the crystal losses, represented by  $R$ , are small, the equivalent crystal  $Q$  (quality factor) is high—typically 20,000. Values of  $Q$  up to almost  $10^6$  can be achieved by using crystals.

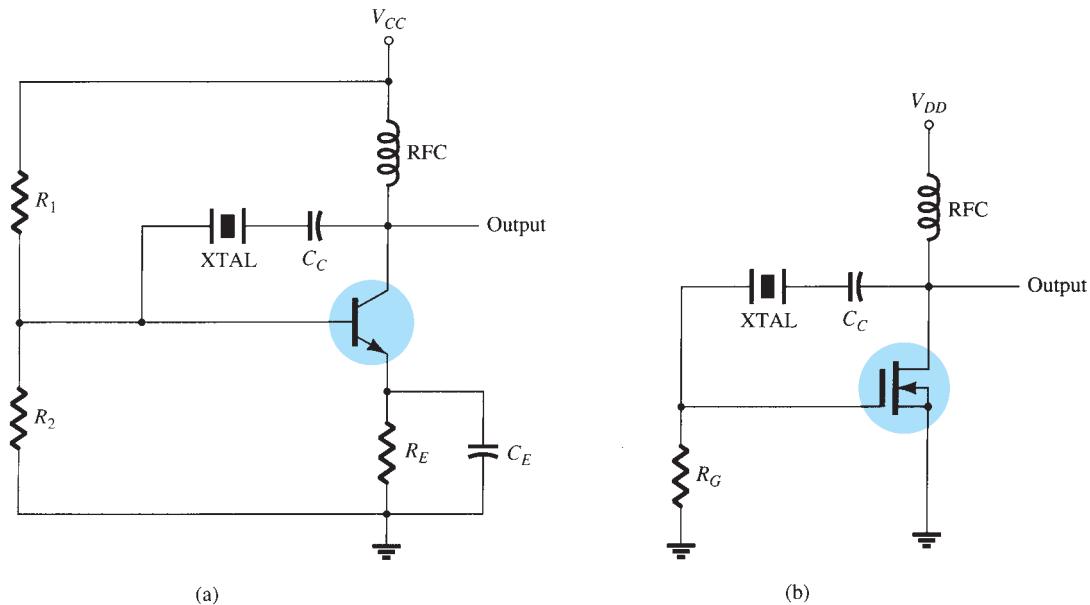
The crystal as represented by the equivalent electrical circuit of Fig. 14.31 can have two resonant frequencies. One resonant condition occurs when the reactances of the series  $RLC$  leg are equal (and opposite). For this condition, the *series-resonant* impedance is very low (equal to  $R$ ). The other resonant condition occurs at a higher frequency when the reactance of the series-resonant leg equals the reactance of capacitor  $C_M$ . This is a parallel resonance or antiresonance condition of the crystal. At this frequency, the crystal offers a very high impedance to the external circuit. The impedance versus frequency of the crystal is shown in Fig. 14.32. To use the crystal properly, it must be connected in a circuit so that its low impedance in the series-resonant operating mode or high impedance in the antiresonant operating mode is selected.



**FIG. 14.32**  
Crystal impedance versus frequency.

### Series-Resonant Circuits

To excite a crystal for operation in the series-resonant mode, it may be connected as a series element in a feedback path. At the series-resonant frequency of the crystal, its impedance is smallest and the amount of (positive) feedback is largest. A typical transistor circuit is



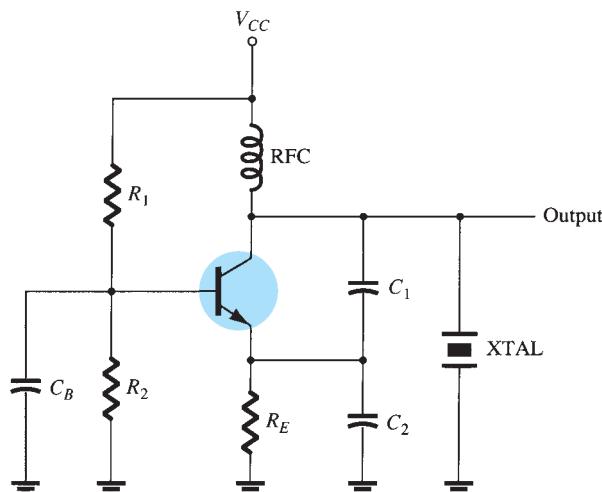
**FIG. 14.33**  
Crystal-controlled oscillator using a crystal (XTAL) in a series-feedback path: (a) BJT circuit; (b) FET circuit.

shown in Fig. 14.33. Resistors  $R_1$ ,  $R_2$ , and  $R_E$  provide a voltage-divider stabilized dc bias circuit. Capacitor  $C_E$  provides ac bypass of the emitter resistor, and the RFC coil provides for dc bias while decoupling any ac signal on the power lines from affecting the output signal. The voltage feedback from collector to base is a maximum when the crystal impedance is minimum (in series-resonant mode). The coupling capacitor  $C_C$  has negligible impedance at the circuit operating frequency but blocks any dc between collector and base.

The resulting circuit frequency of oscillation is set, then, by the series-resonant frequency of the crystal. Changes in supply voltage, transistor device parameters, and so on, have no effect on the circuit operating frequency, which is held stabilized by the crystal. The circuit frequency stability is set by the crystal frequency stability, which is good.

### Parallel-Resonant Circuits

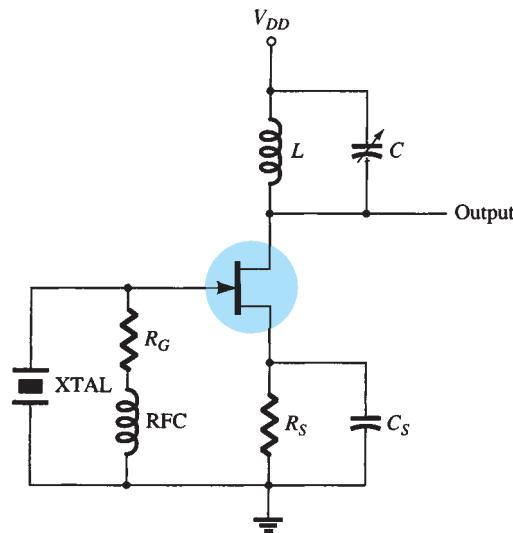
Since the parallel-resonant impedance of a crystal is a maximum value, it is connected in shunt. At the parallel-resonant operating frequency, a crystal appears as an inductive reactance of largest value. Figure 14.34 shows a crystal connected as the inductor element in a



**FIG. 14.34**  
Crystal-controlled oscillator operating in parallel-resonant mode.

modified Colpitts circuit. The basic dc bias circuit should be evident. Maximum voltage is developed across the crystal at its parallel-resonant frequency. The voltage is coupled to the emitter by a capacitor voltage divider—capacitors  $C_1$  and  $C_2$ .

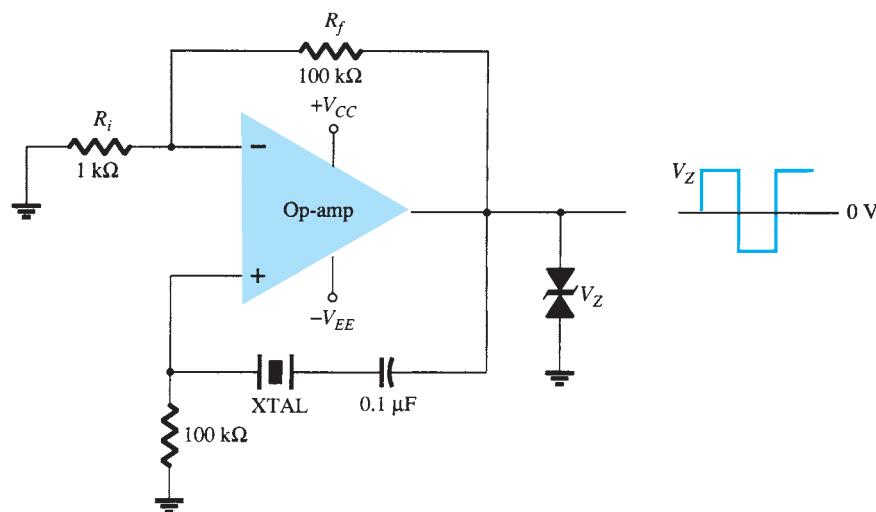
A *Miller crystal-controlled oscillator* circuit is shown in Fig. 14.35. A tuned  $LC$  circuit in the drain section is adjusted near the crystal parallel-resonant frequency. The maximum gate-source signal occurs at the crystal antiresonant frequency, controlling the circuit operating frequency.



**FIG. 14.35**  
Miller crystal-controlled oscillator.

### Crystal Oscillator

An op-amp can be used in a crystal oscillator as shown in Fig. 14.36. The crystal is connected in the series-resonant path and operates at the crystal series-resonant frequency. The present circuit has a high gain, so that an output square-wave signal results as shown in the figure. A pair of Zener diodes is shown at the output to provide output amplitude at exactly the Zener voltage ( $V_Z$ ).



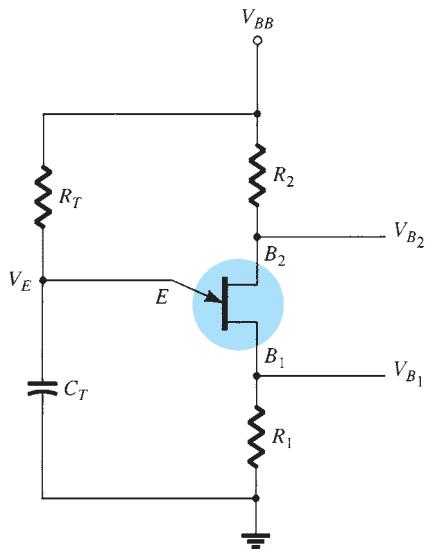
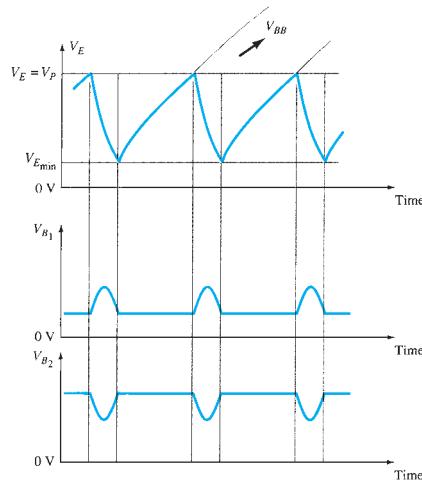
**FIG. 14.36**  
Crystal oscillator using an op-amp.

A particular device, the unijunction transistor, can be used in a single-stage oscillator circuit to provide a pulse signal suitable for digital-circuit applications. The unijunction transistor can be used in what is called a *relaxation oscillator* as shown by the basic circuit of Fig. 14.37. Resistor  $R_T$  and capacitor  $C_T$  are the timing components that set the circuit oscillating rate. The oscillating frequency may be calculated using Eq. (14.48), which includes the unijunction transistor *intrinsic stand-off ratio*  $\eta$  as a factor (in addition to  $R_T$  and  $C_T$ ) in the oscillator operating frequency:

$$f_o \cong \frac{1}{R_T C_T \ln[1/(1 - \eta)]} \quad (14.48)$$

Typically, a unijunction transistor has a stand-off ratio from 0.4 to 0.6. Using a value of  $\eta = 0.5$ , we get

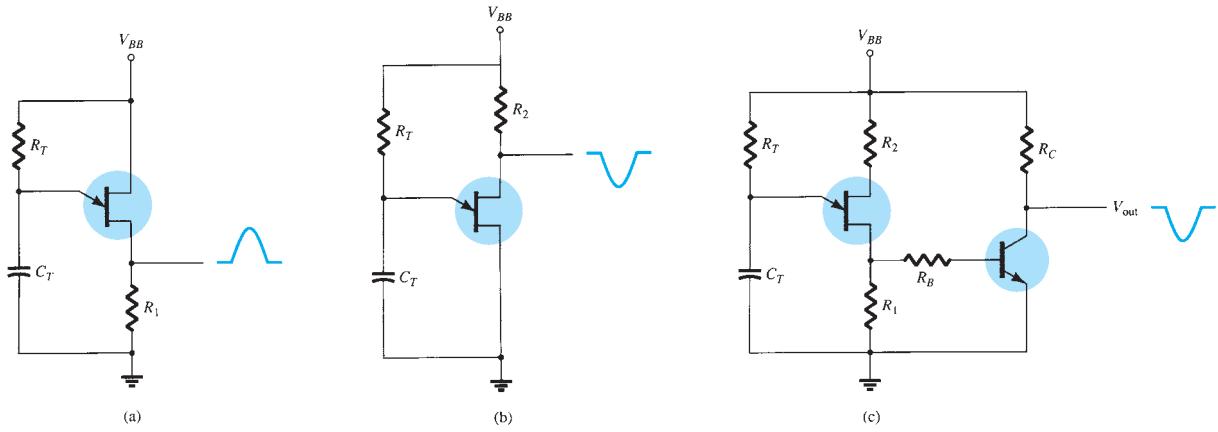
$$\begin{aligned} f_o &\cong \frac{1}{R_T C_T \ln[1/(1 - 0.5)]} = \frac{1.44}{R_T C_T \ln 2} = \frac{1.44}{R_T C_T} \\ &\cong \frac{1.5}{R_T C_T} \end{aligned} \quad (14.49)$$


**FIG. 14.37**
*Basic unijunction oscillator circuit.*

**FIG. 14.38**
*Unijunction oscillator waveforms.*

Capacitor  $C_T$  is charged through resistor  $R_T$  toward supply voltage  $V_{BB}$ . As long as the capacitor voltage  $V_E$  is below a stand-off voltage ( $V_P$ ) set by the voltage across  $B_1 - B_2$  and the transistor stand-off ratio  $\eta$ ,

$$V_P = \eta V_{B_1} V_{B_2} - V_D \quad (14.50)$$

the unijunction emitter lead appears as an open circuit. When the emitter voltage across capacitor  $C_T$  exceeds this value ( $V_P$ ), the unijunction circuit fires, discharging the capacitor, after which a new charge cycle begins. When the unijunction fires, a voltage rise is developed across  $R_1$  and a voltage drop is developed across  $R_2$  as shown in Fig. 14.38. The signal at the emitter is a sawtooth voltage waveform that at base 1 is a positive-going pulse and at base 2 is a negative-going pulse. A few circuit variations of the unijunction oscillator are provided in Fig. 14.39.



**FIG. 14.39**

Some unijunction oscillator circuit configurations.

## 14.11 SUMMARY

### Equations

Voltage-series feedback:

$$A_f = \frac{V_o}{V_s} = \frac{A}{1 + \beta A}, \quad Z_{if} = \frac{V_s}{I_i} = Z_i + (\beta A)Z_i = Z_i(1 + \beta A),$$

$$Z_{of} = \frac{V}{I} = \frac{Z_o}{(1 + \beta A)}$$

Voltage-shunt feedback:

$$A_f = \frac{A}{1 + \beta A}, \quad Z_{if} = \frac{Z_i}{(1 + \beta A)}$$

Current-series feedback:

$$Z_{if} = \frac{V}{I} = Z_i(1 + \beta A), \quad Z_{of} = \frac{V}{I} = Z_o(1 + \beta A)$$

Current shunt feedback:

$$Z_{if} = \frac{Z_i}{(1 + \beta A)}, \quad Z_{of} = \frac{V}{I} = Z_o(1 + \beta A)$$

Phase-shift oscillator:

$$f = \frac{1}{2\pi RC\sqrt{6}}, \quad \beta = \frac{1}{29}$$

Wien bridge oscillator:

$$f_o = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}}$$

Colpitts oscillator:

$$f_o = \frac{1}{2\pi\sqrt{LC_{eq}}} \quad \text{where} \quad C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$$

Hartley oscillator:

$$f_o = \frac{1}{2\pi\sqrt{L_{eq}C}} \quad \text{where} \quad L_{eq} = L_1 + L_2 + 2M$$

Unijunction oscillator:

$$f_o \cong \frac{1}{R_T C_T \ln[1/(1 - \eta)]}$$

**Example 14.11—IC Wien Bridge Oscillator** Using Multisim, we construct an IC Wien bridge oscillator as shown in Fig. 14.42a. The oscillator frequency is calculated using

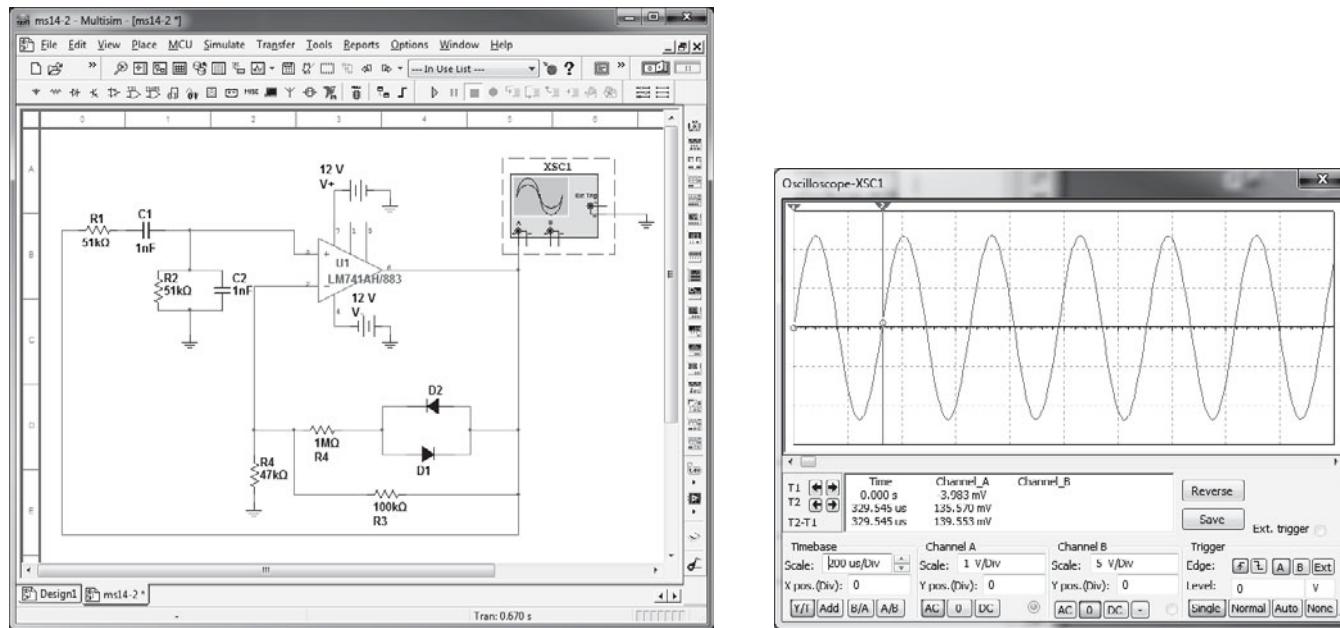
$$f_o = 1/(2\pi\sqrt{R_1C_1R_2C_2})$$

which, for  $R_1 = R_2 = R$  and  $C_1 = C_2 = C$ , is

$$\begin{aligned} f_o &= 1/(2\pi RC) = \frac{1}{2\pi(51\text{ k})(1\text{ nF})} \\ &= 312 \text{ Hz} \end{aligned}$$

The oscilloscope waveform in Fig. 14.42b shows the resonating waveform with cursors  $T2 - T1 = 329.545 \mu\text{s}$ , the scope frequency is

$$f = \frac{1}{T} = \frac{1}{329.545 \mu\text{s}} \cong 3,034.5 \text{ Hz}$$



(a) (b)

**FIG. 14.42**

(a) Wien bridge oscillator using Multisim; (b) scope waveform.

**Example 14.12—IC Colpitts Oscillator** Using Multisim, we construct a Colpitts oscillator as shown in Fig. 14.43a.

Using Eq. 14.45

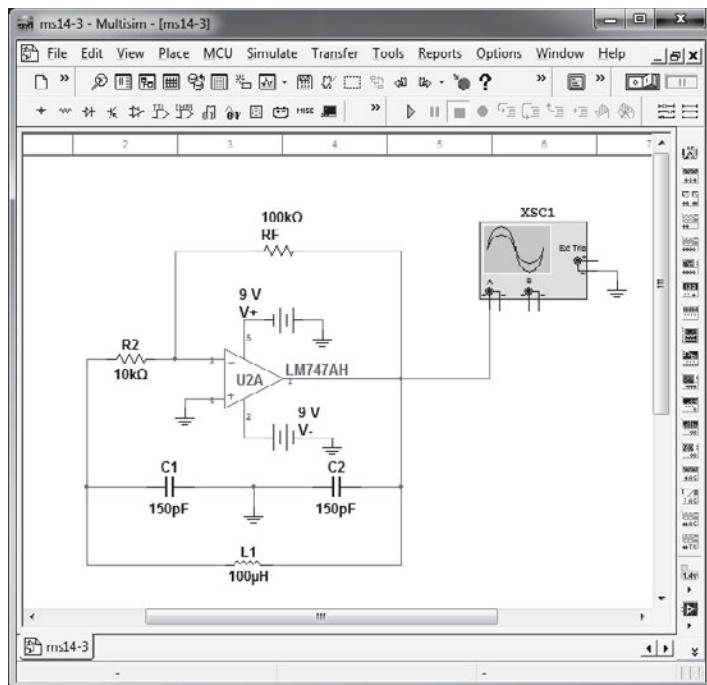
$$Ce_1 = \frac{C_1C_2}{C_1 + C_2} = \frac{(150 \text{ pF})(150 \text{ pF})}{(150 \text{ pF} + 150 \text{ pF})} = 75 \text{ pF}$$

The oscillator frequency for this circuit is then (Eq. 14.44)

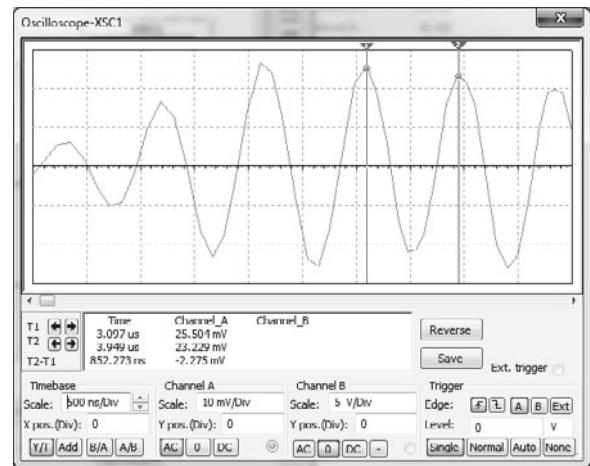
$$\begin{aligned} f_o &= \frac{1}{(2\pi\sqrt{LC_{eq}})} \\ &= \frac{1}{2\pi\sqrt{(100 \mu\text{H})(75 \text{ pF})}} \\ &= 1,837,762.985 \text{ Hz} \\ &\cong 1.8 \text{ MHz} \end{aligned}$$

Fig. 14.43b shows the oscilloscope waveform with

$$\begin{aligned} f &= \frac{1}{T} = \frac{1}{(852.273 \mu\text{s})} \\ &\cong 1.2 \text{ MHz} \end{aligned}$$



(a)



(b)

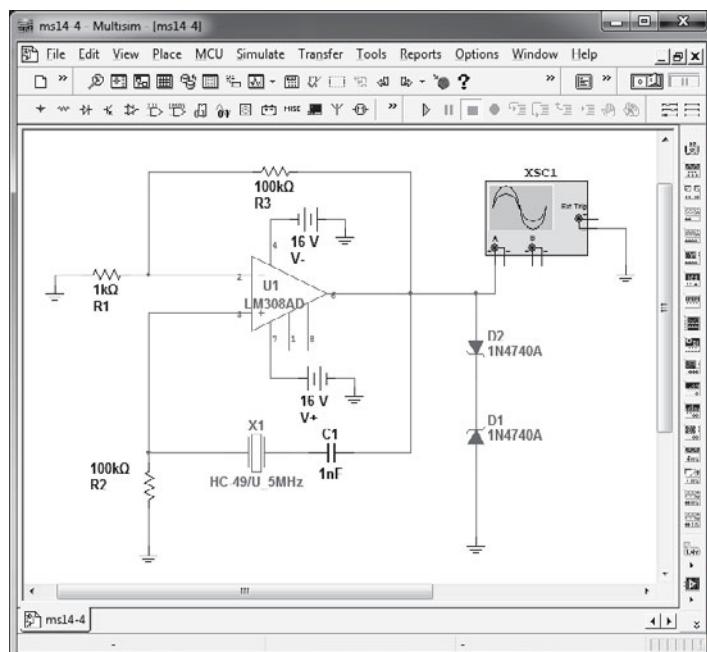
**FIG. 14.43**

(a) IC Colpitts oscillator using Multisim; (b) scope waveform.

**Example 14.13—Crystal Oscillator** Using Multisim, we draw a crystal oscillator circuit as shown in Fig. 14.44a. The oscillator frequency is kept from changing by the crystal. The waveform in Fig. 14.44b shows the period to be about 2.383 μS.

The frequency is then

$$f = 1/T = 1/2.383 \mu\text{s} = 0.42 \text{ MHz}$$



(a)



(b)

**FIG. 14.44**

(a) Crystal oscillator using Multisim; (b) oscilloscope output using Multisim.

## PROBLEMS

\*Note: Asterisks indicate more difficult problems.

### 14.2 Feedback Connection Types

- Calculate the gain of a negative-feedback amplifier having  $A = -2000$  and  $\beta = -1/10$ .
- If the gain of an amplifier changes from a value of  $-1000$  by 10%, calculate the gain change if the amplifier is used in a feedback circuit having  $\beta = -1/20$ .
- Calculate the gain, input, and output impedances of a voltage-series feedback amplifier having  $A = -300$ ,  $R_i = 1.5 \text{ k}\Omega$ ,  $R_o = 50 \text{ k}\Omega$ , and  $\beta = -1/15$ .

### 14.3 Practical Feedback Circuits

- Calculate the gain with and without feedback for an FET amplifier as in Fig. 14.7 for circuit values  $R_1 = 800 \text{ k}\Omega$ ,  $R_2 = 200 \Omega$ ,  $R_o = 40 \text{ k}\Omega$ ,  $R_D = 8 \text{ k}\Omega$ , and  $g_m = 5000 \mu\text{S}$ .
- For a circuit as in Fig. 14.11 and the following circuit values, calculate the circuit gain and the input and output impedances with and without feedback:  $R_B = 600 \text{ k}\Omega$ ,  $R_E = 1.2 \text{ k}\Omega$ ,  $R_C = 4.7 \text{ k}\Omega$ , and  $\beta = 75$ . Use  $V_{CC} = 16 \text{ V}$ .

### 14.6 Phase-Shift Oscillator

- An FET phase-shift oscillator having  $g_m = 6000 \mu\text{S}$ ,  $r_d = 36 \text{ k}\Omega$ , and feedback resistor  $R = 12 \text{ k}\Omega$  is to operate at  $2.5 \text{ kHz}$ . Select  $C$  for specified oscillator operation.
- Calculate the operating frequency of a BJT phase-shift oscillator as in Fig. 14.21b for  $R = 6 \text{ k}\Omega$ ,  $C = 1500 \text{ pF}$ , and  $R_C = 18 \text{ k}\Omega$ .

### 14.7 Wien Bridge Oscillator

- Calculate the frequency of a Wien bridge oscillator circuit (as in Fig. 14.23) when  $R = 10 \text{ k}\Omega$  and  $C = 2400 \text{ pF}$ .

### 14.8 Tuned Oscillator Circuit

- For an FET Colpitts oscillator as in Fig. 14.26 and the following circuit values determine the circuit oscillation frequency:  $C_1 = 750 \text{ pF}$ ,  $C_2 = 2500 \text{ pF}$ , and  $L = 40 \mu\text{H}$ .
- For the transistor Colpitts oscillator of Fig. 14.27 and the following circuit values, calculate the oscillation frequency:  $L = 100 \mu\text{H}$ ,  $L_{RFC} = 0.5 \text{ mH}$ ,  $C_1 = 0.005 \mu\text{F}$ ,  $C_2 = 0.01 \mu\text{F}$ , and  $C_C = 10 \mu\text{F}$ .
- Calculate the oscillator frequency for an FET Hartley oscillator as in Fig. 14.29 for the following circuit values:  $C = 250 \text{ pF}$ ,  $L_1 = 1.5 \text{ mH}$ ,  $L_2 = 1.5 \text{ mH}$ , and  $M = 0.5 \text{ mH}$ .
- Calculate the oscillation frequency for the transistor Hartley circuit of Fig. 14.30 and the following circuit values:  $L_{RFC} = 0.5 \text{ mH}$ ,  $L_1 = 750 \mu\text{H}$ ,  $L_2 = 750 \mu\text{H}$ ,  $M = 150 \mu\text{H}$ , and  $C = 150 \text{ pF}$ .

### 14.9 Crystal Oscillator

- Draw circuit diagrams of (a) a series-operated crystal oscillator and (b) a shunt-excited crystal oscillator.

### 14.10 Unijunction Oscillator

- Design a unijunction oscillator circuit for operation at (a)  $1 \text{ kHz}$  and (b)  $150 \text{ kHz}$ .

# Power Supplies (Voltage Regulators)

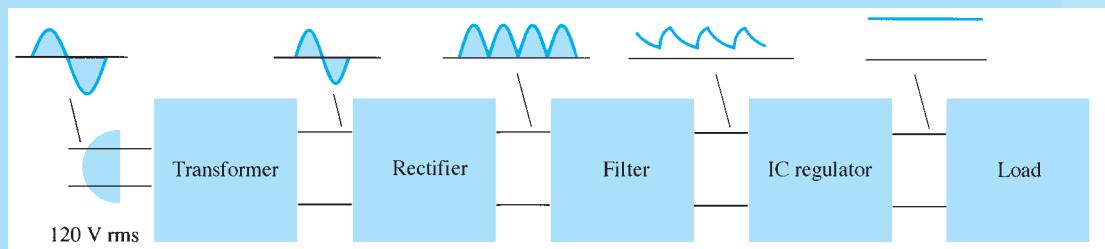
## CHAPTER OBJECTIVES

- How power supply circuits operate
- Operation of RC filters
- Discrete voltage regulator operation
- About practical IC voltage regulators

### 15.1 INTRODUCTION

Chapter 15 introduces the operation of power supply circuits built using filters, rectifiers, and then voltage regulators. (Refer to Chapter 2 for the initial description of diode rectifier circuits.) Starting with an ac voltage, we obtain a steady dc voltage by rectifying the ac voltage, then filtering to a dc level, and, finally, regulating to obtain a desired fixed dc voltage. The regulation is usually obtained from an IC voltage regulator unit, which takes a dc voltage and provides a somewhat lower dc voltage, which remains the same even if the input dc voltage varies or the output load connected to the dc voltage changes.

A block diagram containing the parts of a typical power supply and the voltage at various points in the unit is shown in Fig. 15.1. The ac voltage, typically 120 V rms, is connected to a transformer, which steps that ac voltage down to the level for the desired dc output. A diode rectifier then provides a full-wave rectified voltage, which is initially filtered by a basic capacitor filter to produce a dc voltage. This resulting dc voltage usually has some ripple or ac voltage variation. A regulator circuit can use this dc input to provide a dc voltage that not only has much less ripple voltage, but also remains at the same dc value even if the input dc voltage varies somewhat or the load connected to the output dc voltage changes. This voltage regulation is usually obtained using one of a number of popular voltage regulator IC units.



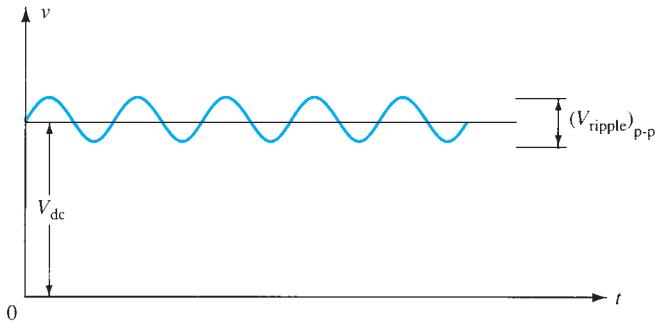
**FIG. 15.1**  
Block diagram showing parts of a power supply.

## 15.2 GENERAL FILTER CONSIDERATIONS

A rectifier circuit is necessary to convert a signal having zero average value into one that has a nonzero average. The output resulting from a rectifier is a pulsating dc voltage and not yet suitable as a battery replacement. Such a voltage could be used in, say, a battery charger, where the average dc voltage is large enough to provide a charging current for the battery. For dc supply voltages, such as those used in a radio, stereo system, computer, and so on, the pulsating dc voltage from a rectifier is not good enough. A filter circuit is necessary to provide a steadier dc voltage.

### Filter Voltage Regulation and Ripple Voltage

Before going into the details of a filter circuit, it would be appropriate to consider the usual methods of rating filter circuits so that we can compare a circuit's effectiveness as a filter. Figure 15.2 shows a typical filter output voltage, which will be used to define some of the signal factors. The filtered output of Fig. 15.2 has a dc value and some ac variation (ripple). Although a battery has essentially a constant or dc output voltage, the dc voltage derived from an ac source signal by rectifying and filtering will have some ac variation (ripple). The smaller the ac variation with respect to the dc level, the better is the filter circuit's operation.



**FIG. 15.2**  
Filter voltage waveform showing dc and ripple voltages.

Consider measuring the output voltage of a filter circuit using a dc voltmeter and an ac (rms) voltmeter. The dc voltmeter will read only the average or dc level of the output voltage. The ac (rms) meter will read only the rms value of the ac component of the output voltage (assuming the ac signal is coupled through a capacitor to block out the dc level).

**Definition:** Ripple is defined as

$$r = \frac{\text{ripple voltage (rms)}}{\text{dc voltage}} = \frac{V_r(\text{rms})}{V_{dc}} \times 100\% \quad (15.1)$$

**EXAMPLE 15.1** Using a dc and ac voltmeter to measure the output signal from a filter circuit, we obtain readings of 25 V dc and 1.5 V rms. Calculate the ripple of the filter output voltage.

**Solution:**

$$r = \frac{V_r(\text{rms})}{V_{dc}} \times 100\% = \frac{1.5 \text{ V}}{25 \text{ V}} \times 100\% = 6\%$$

**Voltage Regulation** Another factor of importance in a power supply is the amount the dc output voltage changes over a range of circuit operation. The voltage provided at the

output under no-load condition (no current drawn from the supply) is reduced when load current is drawn from the supply (under load). The amount the dc voltage changes between the no-load and load conditions is described by a factor called voltage regulation.

**Definition:** Voltage regulation is given by

$$\text{Voltage regulation} = \frac{\text{no-load voltage} - \text{full-load voltage}}{\text{full-load voltage}}$$

$$\% \text{V.R.} = \frac{V_{\text{NL}} - V_{\text{FL}}}{V_{\text{FL}}} \times 100\% \quad (15.2)$$

**EXAMPLE 15.2** A dc voltage supply provides 60 V when the output is unloaded. When connected to a load, the output drops to 56 V. Calculate the value of voltage regulation.

**Solution:**

$$\text{Eq. (15.2): } \% \text{V.R.} = \frac{V_{\text{NL}} - V_{\text{FL}}}{V_{\text{FL}}} \times 100\% = \frac{60 \text{ V} - 56 \text{ V}}{56 \text{ V}} \times 100\% = 7.1\%$$

If the value of full-load voltage is the same as the no-load voltage, the voltage regulation calculated is 0%, which is the best expected. This means that the supply is a perfect voltage source for which the output voltage is independent of the current drawn from the supply. The smaller the voltage regulation, the better is the operation of the voltage supply circuit.

**Ripple Factor of Rectified Signal** Although the rectified voltage is not a filtered voltage, it nevertheless contains a dc component and a ripple component. We will see that the full-wave rectified signal has a larger dc component and less ripple than the half-wave rectified voltage.

**Half-wave:** For a half-wave rectified signal, the output dc voltage is

$$V_{\text{dc}} = 0.318V_m \quad (15.3)$$

The rms value of the ac component of the output signal can be calculated (see Appendix C) to be

$$V_r(\text{rms}) = 0.385V_m \quad (15.4)$$

The percentage ripple of a half-wave rectified signal can then be calculated as

$$r = \frac{V_r(\text{rms})}{V_{\text{dc}}} \times 100\% = \frac{0.385V_m}{0.318V_m} \times 100\% = 121\% \quad (15.5)$$

**Full-wave:** For a full-wave rectified voltage the dc value is

$$V_{\text{dc}} = 0.636V_m \quad (15.6)$$

The rms value of the ac component of the output signal can be calculated (see Appendix C) to be

$$V_r(\text{rms}) = 0.308V_m \quad (15.7)$$

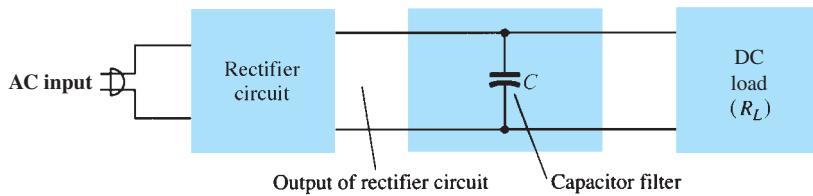
The percentage ripple of a full-wave rectified signal can then be calculated as

$$r = \frac{V_r(\text{rms})}{V_{\text{dc}}} \times 100\% = \frac{0.308V_m}{0.636V_m} \times 100\% = 48\% \quad (15.8)$$

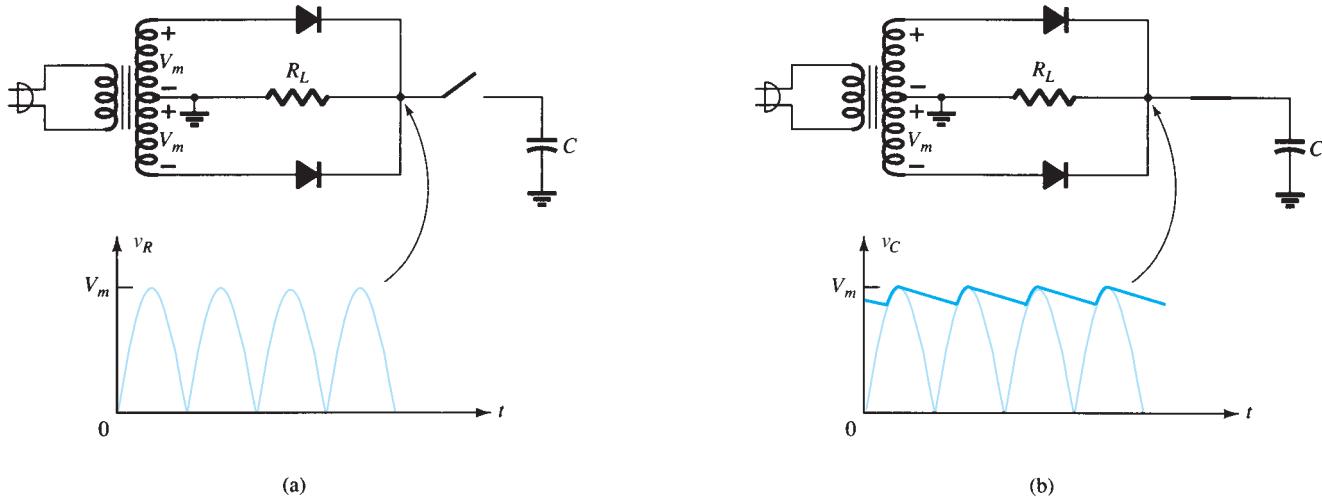
**In summary, a full-wave rectified signal has less ripple than a half-wave rectified signal and is thus better to apply to a filter.**

### 15.3 CAPACITOR FILTER

A very popular filter circuit is the capacitor-filter circuit shown in Fig. 15.3. A capacitor is connected at the rectifier output, and a dc voltage is obtained across the capacitor. Figure 15.4a shows the output voltage of a full-wave rectifier before the signal is filtered, whereas Fig. 15.4b shows the resulting waveform after the filter capacitor is connected at the rectifier output. Notice that the filtered waveform is essentially a dc voltage with some ripple (or ac variation).

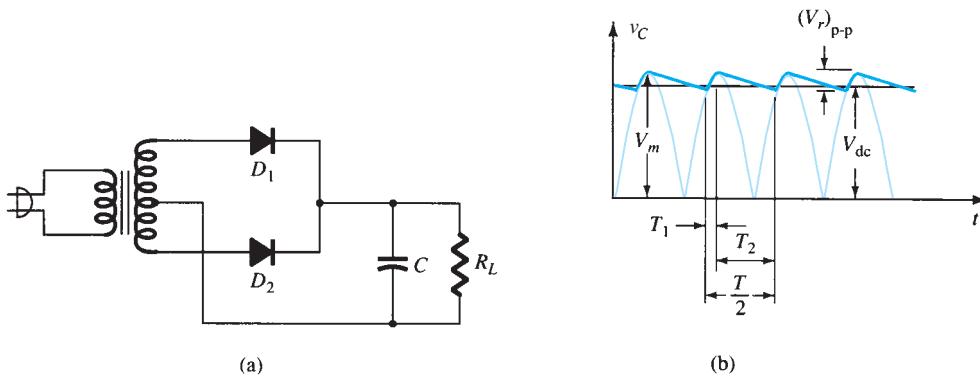


**FIG. 15.3**  
Basic capacitor filter.



**FIG. 15.4**  
Capacitor filter operation: (a) full-wave rectifier voltage; (b) filtered output voltage.

Figure 15.5a shows a full-wave bridge rectifier and the output waveform obtained from the circuit when connected to a load ( $R_L$ ). If no load were connected across the capacitor, the output waveform would ideally be a constant dc level equal in value to the peak voltage ( $V_m$ ) from the rectifier circuit. However, the purpose of obtaining a dc voltage is to provide

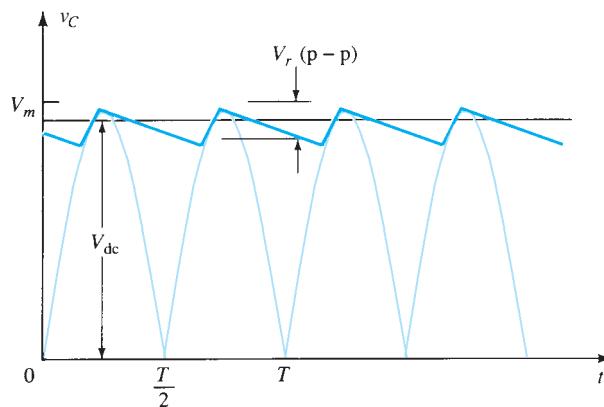


**FIG. 15.5**  
Capacitor filter: (a) capacitor filter circuit; (b) output voltage waveform.

this voltage for use by various electronic circuits, which then constitute a load on the voltage supply. Since there will always be a load on the filter output, we must consider this practical case in our discussion.

## Output Waveform

Figure 15.5b shows the waveform across a capacitor filter. Time  $T_1$  is the time during which diodes of the full-wave rectifier conduct, charging the capacitor up to the peak rectifier voltage  $V_m$ . Time  $T_2$  is the time interval during which the rectifier voltage drops below the peak voltage, and the capacitor discharges through the load. Since the charge-discharge cycle occurs for each half-cycle for a full-wave rectifier, the period of the rectified waveform is  $T/2$ . The filtered voltage, as shown in Fig. 15.6, shows the output waveform to have a dc level  $V_{dc}$  and a ripple voltage  $V_r$  (rms) as the capacitor charges and discharges. Some details of these waveforms and the circuit elements are considered next.



**FIG. 15.6**  
Approximate output voltage of capacitor filter circuit.

**Ripple Voltage  $V_r$  (RMS)** Appendix C provides the details for determining the value of the ripple voltage in terms of the other circuit parameters. The ripple voltage can be calculated from

$$V_r(\text{rms}) = \frac{I_{dc}}{4\sqrt{3}fC} = \frac{2.4I_{dc}}{C} = \frac{2.4V_{dc}}{R_L C} \quad (15.9)$$

where  $I_{dc}$  is in milliamperes,  $C$  is in microfarads, and  $R_L$  is in kilohms.

**EXAMPLE 15.3** Calculate the ripple voltage of a full-wave rectifier with a  $100-\mu\text{F}$  filter capacitor connected to a load drawing 50 mA.

**Solution:**

$$\text{Eq. (15.9): } V_r(\text{rms}) = \frac{2.4(50)}{100} = 1.2 \text{ V}$$

**DC Voltage  $V_{dc}$**  From Appendix C, we can express the dc value of the waveform across the filter capacitor as

$$V_{dc} = V_m - \frac{I_{dc}}{4fC} = V_m - \frac{4.17I_{dc}}{C} \quad (15.10)$$

where  $V_m$  is the peak rectifier voltage,  $I_{dc}$  is the load current in milliamperes, and  $C$  is the filter capacitor in microfarads.

**EXAMPLE 15.4** If the peak rectified voltage for the filter circuit of Example 15.3 is 30 V, calculate the filter dc voltage.

**Solution:**

$$\text{Eq. (15.10): } V_{\text{dc}} = V_m - \frac{4.17I_{\text{dc}}}{C} = 30 - \frac{4.17(50)}{100} = 27.9 \text{ V}$$

### Filter Capacitor Ripple

Using the definition of ripple [Eq. (15.1)], Eq. (15.9), and Eq. (15.10), with  $V_{\text{dc}} \approx V_m$ , we can obtain the expression for the output waveform ripple of a full-wave rectifier and filter-capacitor circuit:

$$r = \frac{V_r(\text{rms})}{V_{\text{dc}}} \times 100\% = \frac{2.4I_{\text{dc}}}{CV_{\text{dc}}} \times 100\% = \frac{2.4}{R_L C} \times 100\% \quad (15.11)$$

where  $I_{\text{dc}}$  is in milliamperes,  $C$  is in microfarads,  $V_{\text{dc}}$  is in volts, and  $R_L$  is in kilohms.

**EXAMPLE 15.5** Calculate the ripple of a capacitor filter for a peak rectified voltage of 30 V, capacitor  $C = 50 \mu\text{F}$ , and a load current of 50 mA.

**Solution:**

$$\text{Eq. (15.11): } r = \frac{2.4I_{\text{dc}}}{CV_{\text{dc}}} \times 100\% = \frac{2.4(50)}{100(27.9)} \times 100\% = 4.3\%$$

We could also calculate the ripple using the basic definition:

$$r = \frac{V_r(\text{rms})}{V_{\text{dc}}} \times 100\% = \frac{1.2 \text{ V}}{27.9 \text{ V}} \times 100\% = 4.3\%$$

### Diode Conduction Period and Peak Diode Current

From the previous discussion, it should be clear that larger values of capacitance provide less ripple and higher average voltage, thereby providing better filter action. From this one might conclude that to improve the performance of a capacitor filter it is only necessary to increase the size of the filter capacitor. The capacitor, however, also affects the peak current drawn through the rectifying diodes, and, as will be shown next, the larger the value of the capacitor, the larger is the peak current drawn through the rectifying diodes.

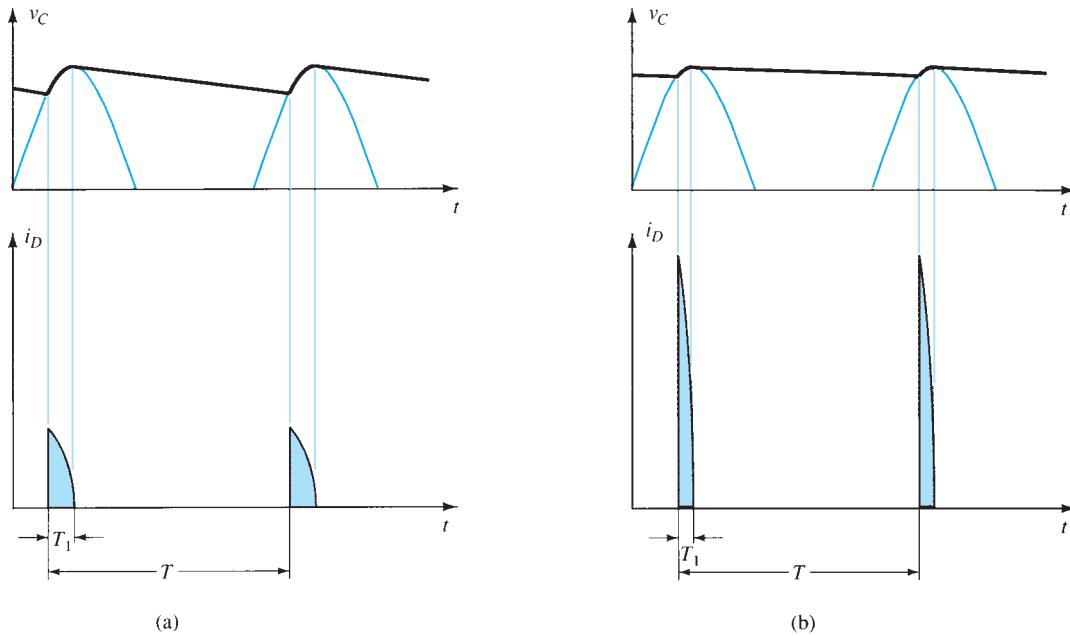
Recall that the diodes conduct during period  $T_1$  (see Fig. 15.5), during which time the diode must provide the necessary average current to charge the capacitor. The shorter this time interval, the larger is the amount of the charging current. Figure 15.7 shows this relation for a half-wave rectified signal (it would be the same basic operation for the full-wave case). Notice that for smaller values of capacitor, with  $T_1$  larger, the peak diode current is less than for larger values of filter capacitor.

Since the average current drawn from the supply must equal the average diode current during the charging period, the following relation can be used (assuming constant diode current during charge time):

$$I_{\text{dc}} = \frac{T_1}{T} I_{\text{peak}}$$

from which we obtain

$$I_{\text{peak}} = \frac{T}{T_1} I_{\text{dc}} \quad (15.12)$$



**FIG. 15.7**  
Output voltage and diode current waveforms: (a) small  $C$ ; (b) large  $C$ .

where  $T_1$  = diode conduction time

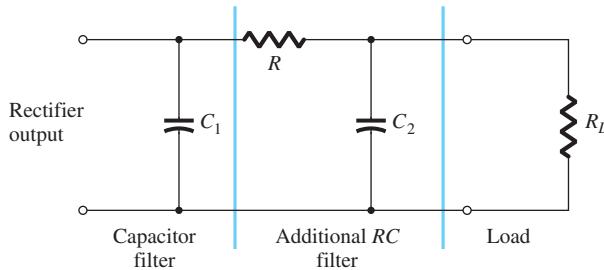
$$T = 1/f \quad (f = 2 \times 60 \text{ for the full-wave case})$$

$I_{dc}$  = average current drawn from the filter

$I_{peak}$  = peak current through the conducting diodes

## 15.4 RC FILTER

It is possible to further reduce the amount of ripple across a filter capacitor by using an additional  $RC$  filter section as shown in Fig. 15.8. The purpose of the added  $RC$  section is to pass most of the dc component while attenuating (reducing) as much of the ac component as possible. Figure 15.9 shows a full-wave rectifier with capacitor filter followed by an  $RC$  filter section. The operation of the filter circuit can be analyzed using superposition for the dc and ac components of the signal.

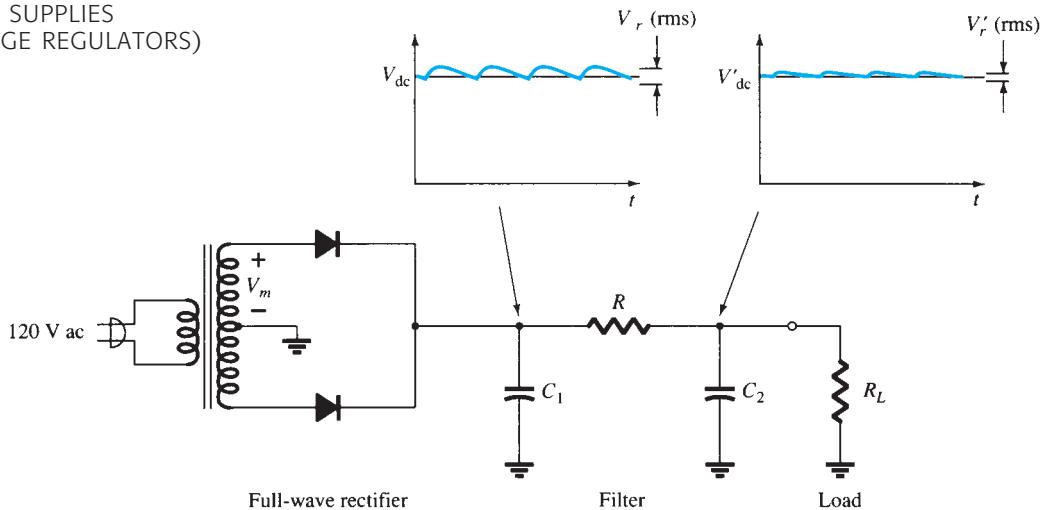


**FIG. 15.8**  
 $RC$  filter stage.

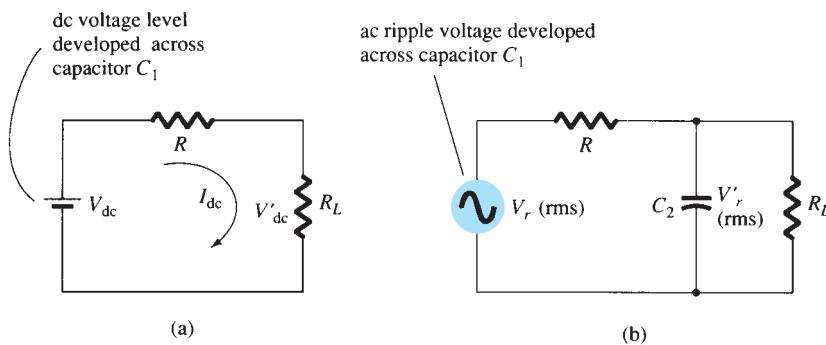
### DC Operation of $RC$ Filter Section

Figure 15.10a shows the dc equivalent circuit to use in analyzing the  $RC$  filter circuit of Fig. 15.9. Since both capacitors are open-circuit for dc operation, the resulting output dc voltage is

$$V'_{dc} = \frac{R_L}{R + R_L} V_{dc} \quad (15.13)$$



**FIG. 15.9**  
Full-wave rectifier and RC filter circuit.



**FIG. 15.10**  
(a) DC and (b) ac equivalent circuits of RC filter.

**EXAMPLE 15.6** Calculate the dc voltage across a  $1\text{-k}\Omega$  load for an  $RC$  filter section ( $R = 120 \Omega$ ,  $C = 10 \mu\text{F}$ ). The dc voltage across the initial filter capacitor is  $V_{dc} = 60 \text{ V}$ .

**Solution:**

$$\text{Eq. (15.13): } V'_{dc} = \frac{R_L}{R + R_L} V_{dc} = \frac{1000}{120 + 1000} (60 \text{ V}) = 53.6 \text{ V}$$

### AC Operation of RC Filter Section

Figure 15.10b shows the ac equivalent circuit of the  $RC$  filter section. Due to the voltage-divider action of the capacitor ac impedance and the load resistor, the ac component of voltage resulting across the load is

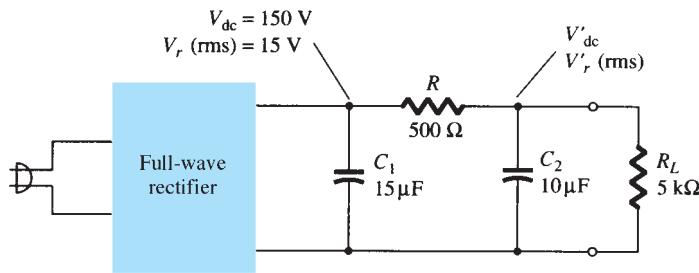
$$V'_r(\text{rms}) \approx \frac{X_C}{R} V_r(\text{rms}) \quad (15.14)$$

For a full-wave rectifier with ac ripple at 120 Hz, the impedance of a capacitor can be calculated using

$$X_C = \frac{1.3}{C} \quad (15.15)$$

where  $C$  is in microfarads and  $X_C$  is in kilohms.

**EXAMPLE 15.7** Calculate the dc and ac components of the output signal across load  $R_L$  in the circuit of Fig. 15.11. Calculate the ripple of the output waveform.



**FIG. 15.11**  
RC filter circuit for Example 15.7.

### Solution:

**DC Calculation** We obtain

$$\text{Eq. (15.13): } V'_\text{dc} = \frac{R_L}{R + R_L} V_\text{dc} = \frac{5 \text{ k}\Omega}{500 + 5 \text{ k}\Omega} (150 \text{ V}) = 136.4 \text{ V}$$

**AC Calculation** The  $RC$ -section capacitive impedance is

$$\text{Eq. (15.15): } X_C = \frac{1.3}{C} = \frac{1.3}{10} = 0.13 \text{ k}\Omega = 130 \Omega$$

The ac component of the output voltage, calculated using Eq. (15.14), is

$$V'_r(\text{rms}) = \frac{X_C}{R} V_r(\text{rms}) = \frac{130}{500} (15 \text{ V}) = 3.9 \text{ V}$$

The ripple of the output waveform is then

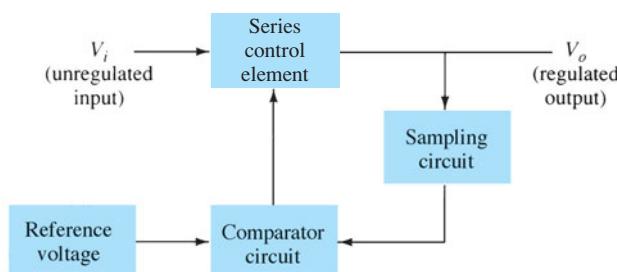
$$r = \frac{V'_r(\text{rms})}{V'_\text{dc}} \times 100\% = \frac{3.9 \text{ V}}{136.4 \text{ V}} \times 100\% = 2.86\%$$

## 15.5 DISCRETE TRANSISTOR VOLTAGE REGULATION

Two types of transistor voltage regulators are the series voltage regulator and the shunt voltage regulator. Each type of circuit can provide an output dc voltage that is regulated or maintained at a set value even if the input voltage varies or if the load connected to the output changes.

### Series Voltage Regulation

The basic connection of a series regulator circuit is shown in the block diagram of Fig. 15.12. The series element controls the amount of the input voltage that gets to the output.

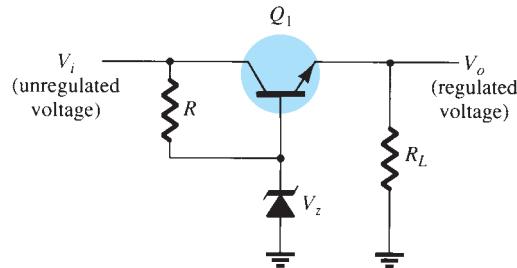


**FIG. 15.12**  
Series regulator block diagram.

The output voltage is sampled by a circuit that provides a feedback voltage to be compared to a reference voltage.

1. If the output voltage increases, the comparator circuit provides a control signal to cause the series control element to decrease the amount of the output voltage—thereby maintaining the output voltage.
2. If the output voltage decreases, the comparator circuit provides a control signal to cause the series control element to increase the amount of the output voltage.

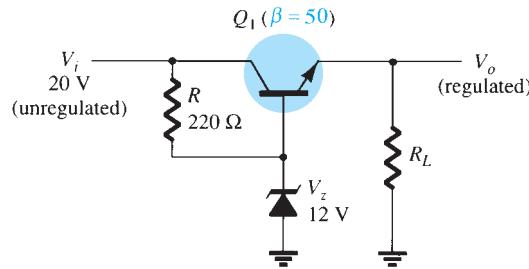
**Series Regulator Circuit** A simple series regulator circuit is shown in Fig. 15.13. Transistor  $Q_1$  is the series control element, and Zener diode  $D_Z$  provides the reference voltage. The regulating operation can be described as follows:



**FIG. 15.13**  
Series regulator circuit.

1. If the output voltage decreases, the increased base-emitter voltage causes transistor  $Q_1$  to conduct more, thereby raising the output voltage—maintaining the output constant.
2. If the output voltage increases, the decreased base-emitter voltage causes transistor  $Q_1$  to conduct less, thereby reducing the output voltage—maintaining the output constant.

**EXAMPLE 15.8** Calculate the output voltage and the Zener current in the regulator circuit of Fig. 15.14 for  $R_L = 1 \text{ k}\Omega$ .



**FIG. 15.14**  
Circuit for Example 15.8.

**Solution:**

$$V_o = V_z - V_{BE} = 12 \text{ V} - 0.7 \text{ V} = 11.3 \text{ V}$$

$$V_{CE} = V_i - V_o = 20 \text{ V} - 11.3 \text{ V} = 8.7 \text{ V}$$

$$I_R = \frac{20 \text{ V} - 12 \text{ V}}{220 \Omega} = \frac{8 \text{ V}}{220 \Omega} = 36.4 \text{ mA}$$

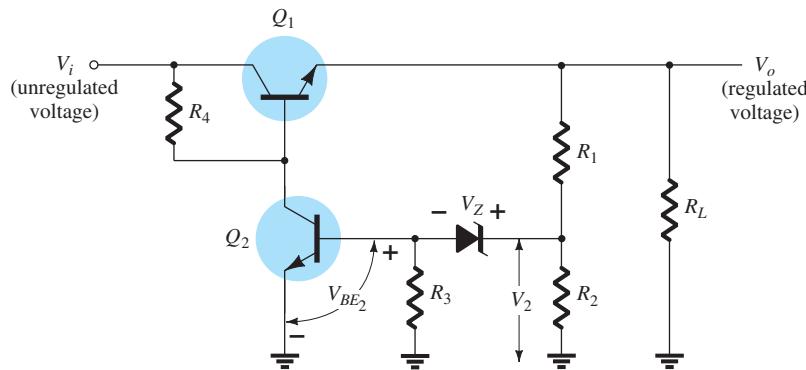
For  $R_L = 1 \text{ k}\Omega$ ,

$$I_L = \frac{V_o}{R_L} = \frac{11.3 \text{ V}}{1 \text{ k}\Omega} = 11.3 \text{ mA}$$

$$I_B = \frac{I_C}{\beta} = \frac{11.3 \text{ mA}}{50} = 226 \mu\text{A}$$

$$I_Z = I_R - I_B = 36.4 \text{ mA} - 226 \mu\text{A} \approx 36 \text{ mA}$$

**Improved Series Regulator** An improved series regulator circuit is shown in Fig. 15.15. Resistors  $R_1$  and  $R_2$  act as a sampling circuit, with Zener diode  $D_Z$  providing a reference voltage, and transistor  $Q_2$  then controls the base current to transistor  $Q_1$  to vary the current passed by transistor  $Q_1$  to maintain the output voltage constant.



**FIG. 15.15**  
*Improved series regulator circuit.*

If the output voltage tries to increase, the increased voltage,  $V_2$ , sampled by  $R_1$  and  $R_2$ , causes the base-emitter voltage of transistor  $Q_2$  to go up (since  $V_Z$  remains fixed). If  $Q_2$  conducts more current, less goes to the base of transistor  $Q_1$ , which then passes less current to the load, reducing the output voltage—thereby maintaining the output voltage constant. The opposite takes place if the output voltage tries to decrease, causing less current to be supplied to the load, to keep the voltage from decreasing.

The voltage  $V_2$  provided by sensing resistors  $R_1$  and  $R_2$  must equal the sum of the base-emitter voltage of  $Q_2$  and the Zener diode, that is,

$$V_{BE_2} + V_Z = V_2 = \frac{R_2}{R_1 + R_2} V_o \quad (15.16)$$

Solving Eq. (15.16) for the regulated output voltage  $V_o$  gives

$$V_o = \frac{R_1 + R_2}{R_2} (V_Z + V_{BE_2}) \quad (15.17)$$

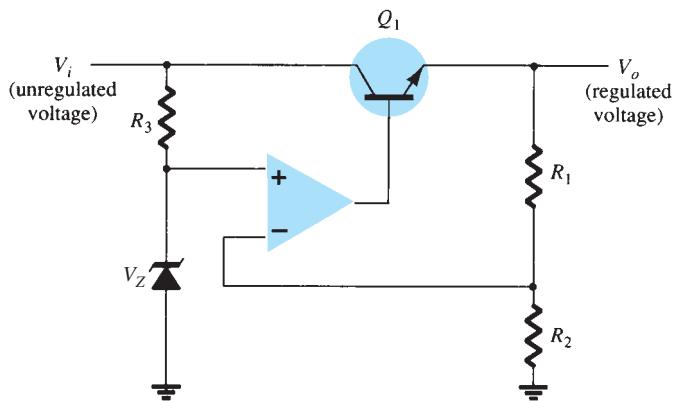
**EXAMPLE 15.9** What regulated output voltage is provided by the circuit of Fig. 15.15 for the circuit elements  $R_1 = 20 \text{ k}\Omega$ ,  $R_2 = 30 \text{ k}\Omega$ , and  $V_Z = 8.3 \text{ V}$ ?

**Solution:** From Eq. (15.17), the regulated output voltage is

$$V_o = \frac{20 \text{ k}\Omega + 30 \text{ k}\Omega}{30 \text{ k}\Omega} (8.3 \text{ V} + 0.7 \text{ V}) = 15 \text{ V}$$

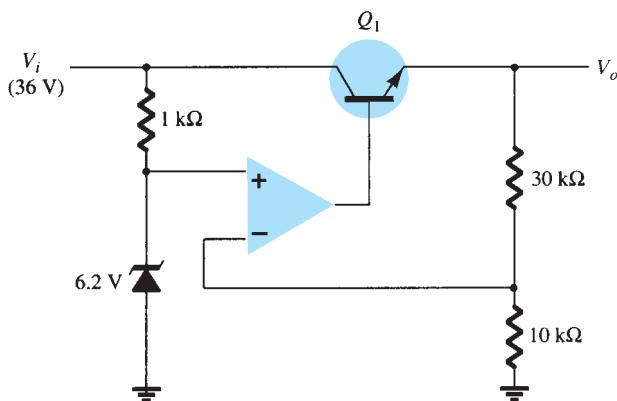
**Op-Amp Series Regulator** Another type of series regulator is shown in Fig. 15.16. The op-amp compares the Zener diode reference voltage with the feedback voltage from sensing resistors  $R_1$  and  $R_2$ . If the output voltage varies, the conduction of transistor  $Q_1$  is controlled to maintain the output voltage constant. The output voltage will be maintained at a value of

$$V_o = \left(1 + \frac{R_1}{R_2}\right) V_Z \quad (15.18)$$



**FIG. 15.16**  
Op-amp series regulator circuit.

**EXAMPLE 15.10** Calculate the regulated output voltage in the circuit of Fig. 15.17.



**FIG. 15.17**  
Circuit for Example 15.10.

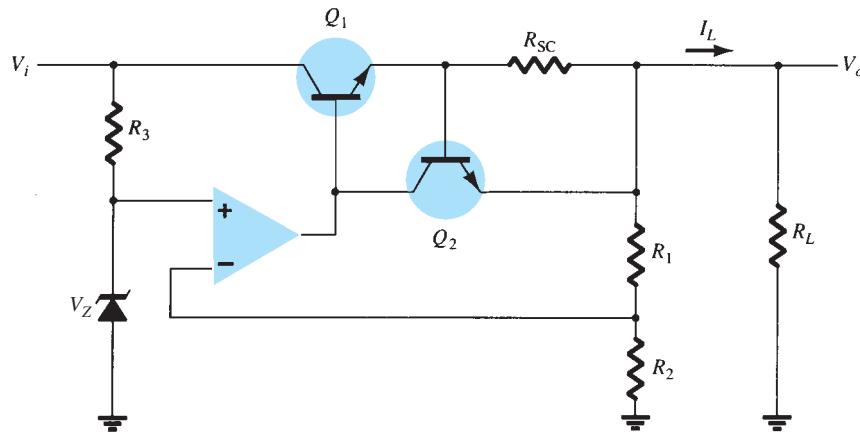
**Solution:**

$$\text{Eq. (15.18): } V_o = \left(1 + \frac{30 \text{ k}\Omega}{10 \text{ k}\Omega}\right) 6.2 \text{ V} = 24.8 \text{ V}$$

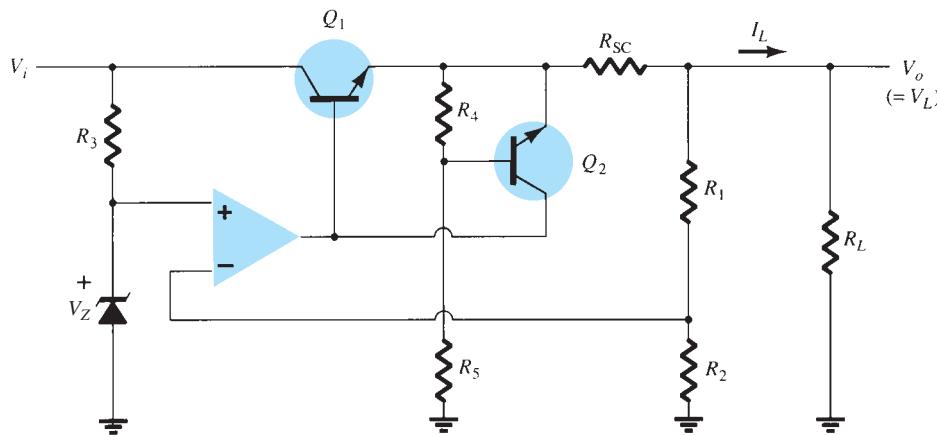
**Current-Limiting Circuit** One form of short-circuit or overload protection is current limiting, as shown in Fig. 15.18. As load current \$I\_L\$ increases, the voltage drop across the short-circuit sensing resistor \$R\_{SC}\$ increases. When the voltage drop across \$R\_{SC}\$ becomes large enough, it will drive \$Q\_2\$ on, diverting current from the base of transistor \$Q\_1\$, thereby reducing the load current through transistor \$Q\_1\$, preventing any additional current to load \$R\_L\$. The action of components \$R\_{SC}\$ and \$Q\_2\$ limits the maximum load current.

**Foldback Limiting** Current limiting reduces the load voltage when the current becomes larger than the limiting value. The circuit of Fig. 15.19 provides foldback limiting, which reduces both the output voltage and the output current, protecting the load from overcurrent as well as protecting the regulator.

Foldback limiting is provided by the additional voltage-divider network of \$R\_4\$ and \$R\_5\$ in the circuit of Fig. 15.19 (over that of Fig. 15.17). The divider circuit senses the voltage at the output (emitter) of \$Q\_1\$. When \$I\_L\$ increases to its maximum value, the voltage across \$R\_{SC}\$ becomes large enough to drive \$Q\_2\$ on, thereby providing current limiting. If the load resistance is made smaller, the voltage driving \$Q\_2\$ on becomes less, so that \$I\_L\$ drops when \$V\_L\$ also



**FIG. 15.18**  
Current-limiting voltage regulator.

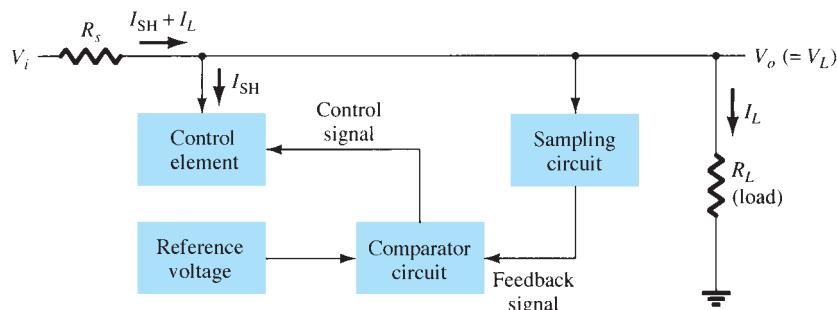


**FIG. 15.19**  
Foldback-limiting series regulator circuit.

drops in value—this action being foldback limiting. When the load resistance is returned to its rated value, the circuit resumes its voltage regulation action.

### Shunt Voltage Regulation

A shunt voltage regulator provides regulation by shunting current away from the load to regulate the output voltage. Figure 15.20 shows the block diagram of such a voltage regulator. The input unregulated voltage provides current to the load. Some of the current is pulled away by the control element to maintain the regulated output voltage across the load. If the load voltage tries to change due to a change in the load, the sampling circuit provides

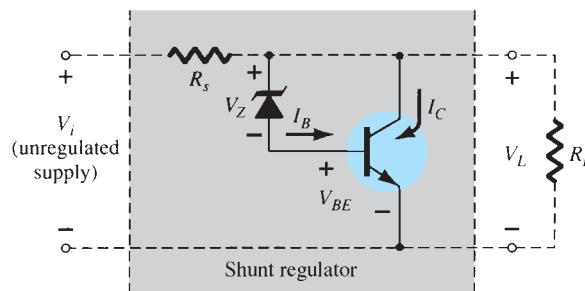


**FIG. 15.20**  
Block diagram of shunt voltage regulator.

a feedback signal to a comparator, which then provides a control signal to vary the amount of the current shunted away from the load. As the output voltage tries to get larger, for example, the sampling circuit provides a feedback signal to the comparator circuit, which then provides a control signal to draw increased shunt current, providing less load current, thereby keeping the regulated voltage from rising.

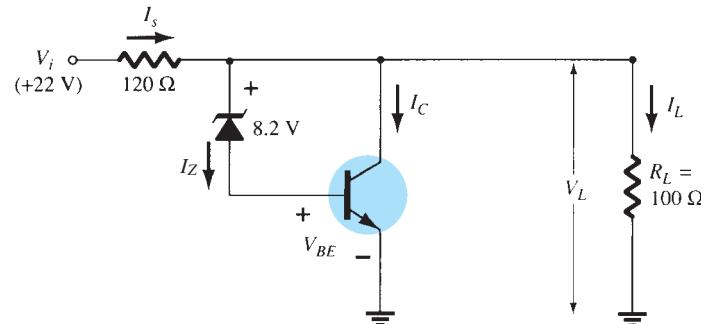
**Basic Transistor Shunt Regulator** A basic shunt regulator circuit is shown in Fig. 15.21. Resistor  $R_S$  drops the unregulated voltage by an amount that depends on the current supplied to the load  $R_L$ . The voltage across the load is set by the Zener diode and transistor base-emitter voltage. If the load resistance decreases, a reduced drive current to the base of  $Q_1$  results, shunting less collector current. The load current is thus larger, thereby maintaining the regulated voltage across the load. The output voltage to the load is

$$V_L = V_Z + V_{BE} \quad (15.19)$$



**FIG. 15.21**  
Transistor shunt voltage regulator.

**EXAMPLE 15.11** Determine the regulated voltage and circuit currents for the shunt regulator of Fig. 15.22.



**FIG. 15.22**  
Circuit for Example 15.11.

**Solution:** The load voltage is

$$\text{Eq. (15.19): } V_L = 8.2 \text{ V} + 0.7 \text{ V} = 8.9 \text{ V}$$

For the given load,

$$I_L = \frac{V_L}{R_L} = \frac{8.9 \text{ V}}{100 \Omega} = 89 \text{ mA}$$

With the unregulated input voltage at 22 V, the current through  $R_S$  is

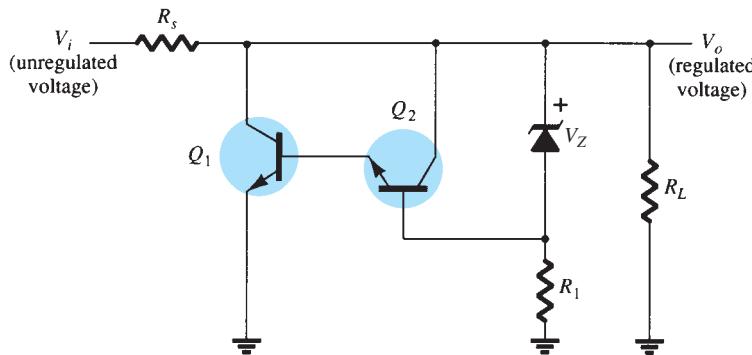
$$I_S = \frac{V_i - V_L}{R_S} = \frac{22 \text{ V} - 8.9 \text{ V}}{120 \Omega} = 109 \text{ mA}$$

so that the collector current is

$$I_C = I_S - I_L = 109 \text{ mA} - 89 \text{ mA} = 20 \text{ mA}$$

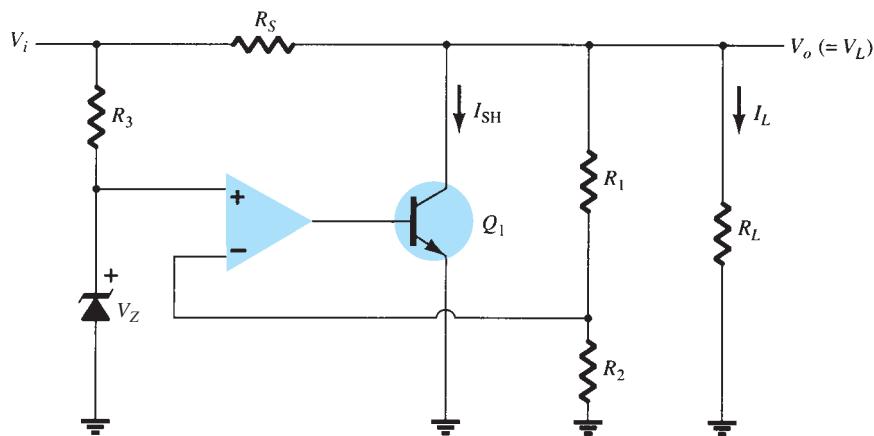
**Improved Shunt Regulator** The circuit of Fig. 15.23 shows an improved shunt voltage regulator circuit. The Zener diode provides a reference voltage so that the voltage across  $R_1$  senses the output voltage. As the output voltage tries to change, the current shunted by transistor  $Q_1$  is varied to maintain the output voltage constant. Transistor  $Q_2$  provides a larger base current to transistor  $Q_1$  than the circuit of Fig. 15.21, so that the regulator handles a larger load current. The output voltage is set by the Zener voltage and that across the two transistor base-emitters,

$$V_o = V_L = V_Z + V_{BE_2} + V_{BE_1} \quad (15.20)$$



**FIG. 15.23**  
Improved shunt voltage regulator circuit.

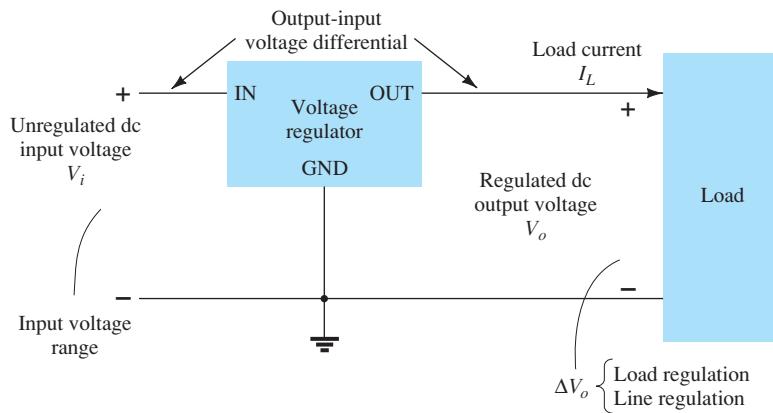
**Shunt Voltage Regulator Using Op-Amp** Figure 15.24 shows another version of a shunt voltage regulator using an op-amp as voltage comparator. The Zener voltage is compared to the feedback voltage obtained from voltage divider  $R_1$  and  $R_2$  to provide the control drive current to shunt element  $Q_1$ . The current through resistor  $R_S$  is thus controlled to drop a voltage across  $R_S$  so that the output voltage is maintained.



**FIG. 15.24**  
Shunt voltage regulator using an op-amp.

## Switching Regulation

A type of regulator circuit that is quite popular for its efficient transfer of power to the load is the switching regulator. Basically, a switching regulator passes voltage to the load in pulses, which are then filtered to provide a smooth dc voltage. Figure 15.25 shows the basic components of such a voltage regulator. The added circuit complexity is well worth the improved operating efficiency obtained.



**FIG. 15.25**  
Block representation of three-terminal voltage regulator.

## 15.6 IC VOLTAGE REGULATORS

Voltage regulators comprise a class of widely used ICs. Regulator IC units contain the circuitry for reference source, comparator amplifier, control device, and overload protection all in a single IC. Although the internal construction of the IC is somewhat different from that described for discrete voltage regulator circuits, the external operation is much the same. IC units provide regulation of either a fixed positive voltage, a fixed negative voltage, or an adjustably set voltage.

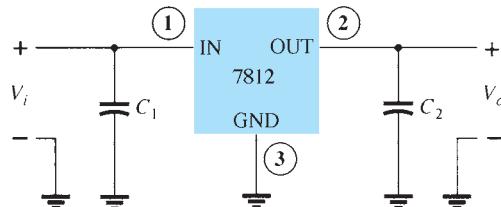
A power supply can be built using a transformer connected to the ac supply line to step the ac voltage to a desired amplitude, then rectifying that ac voltage, filtering with a capacitor and  $RC$  filter, if desired, and finally regulating the dc voltage using an IC regulator. The regulators can be selected for operation with load currents from hundreds of milliamperes to tens of amperes, corresponding to power ratings from milliwatts to tens of watts.

### Three-Terminal Voltage Regulators

Figure 15.25 shows the basic connection of a three-terminal voltage regulator IC to a load. The fixed voltage regulator has an unregulated dc input voltage  $V_i$  applied to one input terminal, a regulated output dc voltage  $V_o$  from a second terminal, and the third terminal connected to ground. For a selected regulator, IC device specifications list a voltage range over which the input voltage can vary to maintain a regulated output voltage over a range of load current. The specifications also list the amount of output voltage change resulting from a change in load current (load regulation) or in input voltage (line regulation).

### Fixed-Positive-Voltage Regulators

The series 78 regulators provide fixed regulated voltages from 5 V to 24 V. Figure 15.26 shows how one such IC, a 7812, is connected to provide voltage regulation with output from this unit of +12 V dc. An unregulated input voltage  $V_i$  is filtered by capacitor  $C_1$  and connected to the IC's IN terminal. The IC's OUT terminal provides a regulated +12 V, which is filtered by capacitor  $C_2$  (mostly for any high-frequency noise). The third IC terminal is connected to ground (GND). Whereas the input voltage may vary over some permissible



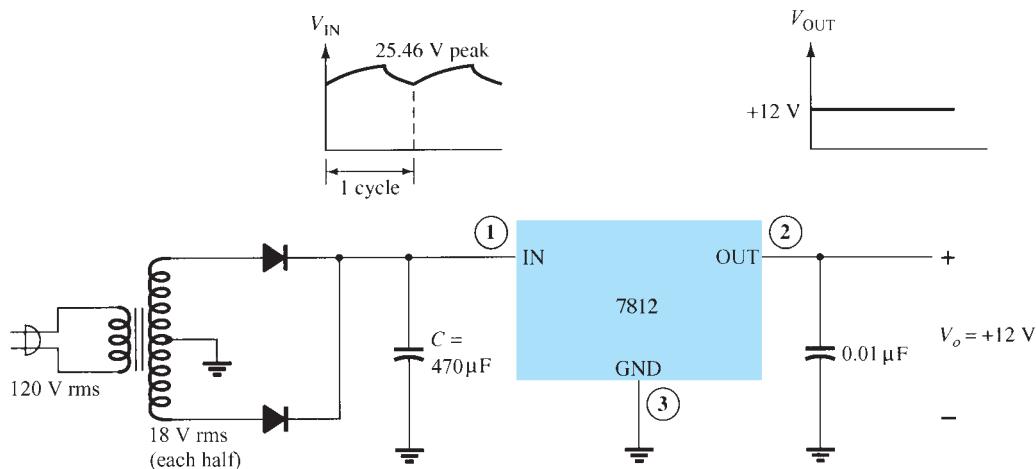
**FIG. 15.26**  
Connection of a 7812 voltage regulator.

voltage range and the output load may vary over some acceptable range, the output voltage remains constant within specified voltage variation limits. These limitations are spelled out in the manufacturer's specification sheets. A table of positive-voltage regulator ICs is provided in Table 15.1.

**TABLE 15.1**  
Positive-Voltage Regulators in the 7800 Series

IC Part	Output Voltage (V)	Minimum $V_i$ (V)
7805	+5	7.3
7806	+6	8.3
7808	+8	10.5
7810	+10	12.5
7812	+12	14.6
7815	+15	17.7
7818	+18	21.0
7824	+24	27.1

The connection of a 7812 in a complete voltage supply is shown in the connection of Fig. 15.27. The ac line voltage (120 V rms) is stepped down to 18 V rms across each half of the center-tapped transformer. A full-wave rectifier and capacitor filter then provides an unregulated dc voltage, shown as a dc voltage of about 22 V, with ac ripple of a few volts as input to the voltage regulator. The 7812 IC then provides an output that is a regulated +12 V dc.



**FIG. 15.27**  
A +12 V power supply.

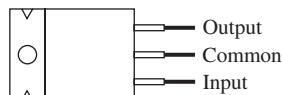
**Positive-Voltage-Regulator Specifications** The specifications sheet of voltage regulators is typified by that shown in Fig. 15.28 for the group of series 7800 positive-voltage regulators. Some consideration of a few of the more important parameters should be made.

**Output voltage:** The specification for the 7812 shows that the output voltage is typically +12 V but could be as low as 11.5 V or as high as 12.5 V.

**Output regulation:** The output voltage regulation is seen to be typically 4 mV, to a maximum of 100 mV (at output currents from 0.25 A to 0.75 A). This information specifies that the output voltage can typically vary only 4 mV from the rated 12 V dc.

**Short-circuit output current:** The amount of current is limited to typically 0.35 A if the output were to be short-circuited (presumably by accident or by another faulty component).

**Peak output current:** Although the rated maximum current is 1.5 A for this series of IC, the typical peak output current that might be drawn by a load is 2.2 A. This shows



Absolute maximum ratings:

Input voltage 40 V  
Continuous total dissipation 2 W  
Operating free-air temperature range -65 to 150°C

Nominal output voltage	Regulator
5 V	7805
6 V	7806
8 V	7808
10 V	7810
12 V	7812
15 V	7815
18 V	7818
24 V	7824

$\mu$ A 7812C electrical characteristics:

Parameter	Min.	Typ.	Max.	Units
Output voltage	11.5	12	12.5	V
Input regulation		3	120	mV
Ripple rejection	55	71		dB
Output regulation		4	100	mV
Output resistance		0.018		$\Omega$
Dropout voltage		2.0		V
Short-circuit output current		350		mA
Peak output current		2.2		A

**FIG. 15.28**  
*Specification sheet data for voltage regulator ICs.*

that although the manufacturer rates the IC as capable of providing 1.5 A, one could draw somewhat more current (possibly for a short period of time).

**Dropout voltage:** The dropout voltage, typically 2 V, is the minimum amount of voltage across the input–output terminals that must be maintained if the IC is to operate as a regulator. If the input voltage drops too low or the output rises so that at least 2 V is not maintained across the IC input–output, the IC will no longer provide voltage regulation. One therefore maintains an input voltage large enough to assure that the dropout voltage is provided.

### Fixed-Negative-Voltage Regulators

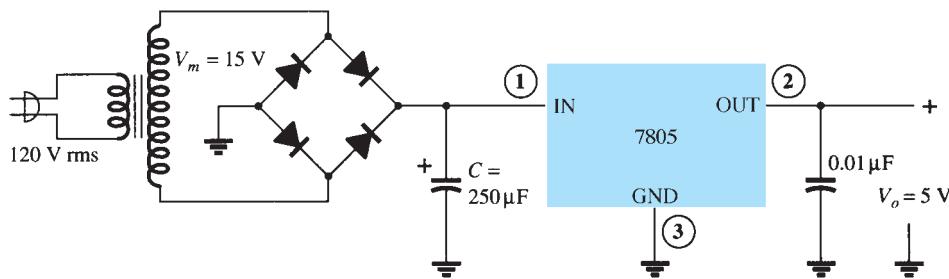
The series 7900 ICs provide negative-voltage regulators, similar to those providing positive voltages. A list of negative-voltage regulator ICs is provided in Table 15.2. As shown, IC regulators are available for a range of fixed negative voltages, the selected IC providing the rated output voltage as long as the input voltage is maintained greater than the minimum input value. For example, the 7912 provides an output of -12 V as long as the input to the regulator IC is more negative than -14.6 V.

**TABLE 15.2**  
*Negative-Voltage Regulators in 7900 Series*

IC Part	Output Voltage (V)	Minimum $V_i$ (V)
7905	-5	-7.3
7906	-6	-8.4
7908	-8	-10.5
7909	-9	-11.5
7912	-12	-14.6
7915	-15	-17.7
7918	-18	-20.8
7924	-24	-27.1

**EXAMPLE 15.12** Draw a voltage supply using a full-wave bridge rectifier, capacitor filter, and IC regulator to provide an output of +5 V.

**Solution:** The resulting circuit is shown in Fig. 15.29.



**FIG. 15.29**  
A +5-V power supply.

**EXAMPLE 15.13** For a transformer output of 15 V and a filter capacitor of  $250 \mu\text{F}$ , calculate the minimum input voltage when connected to a load drawing 400 mA.

**Solution:** The voltages across the filter capacitor are

$$V_r(\text{peak}) = \sqrt{3} V_r(\text{rms}) = \sqrt{3} \frac{2.4I_{\text{dc}}}{C} = \sqrt{3} \frac{2.4(400)}{250} = 6.65 \text{ V}$$

$$V_{\text{dc}} = V_m - V_r(\text{peak}) = 15 \text{ V} - 6.65 \text{ V} = 8.35 \text{ V}$$

Since the input swings around this dc level, the minimum input voltage can drop to as low as

$$V_i(\text{low}) = V_{\text{dc}} - V_r(\text{peak}) = 15 \text{ V} - 6.65 \text{ V} = 8.35 \text{ V}$$

Since this voltage is greater than the minimum required for the IC regulator (from Table 15.1,  $V_i = 7.3 \text{ V}$ ), the IC can provide a regulated voltage to the given load.

**EXAMPLE 15.14** Determine the maximum value of load current at which regulation is maintained for the circuit of Fig. 15.29.

**Solution:** To maintain  $V_i(\text{min}) \geq 7.3 \text{ V}$ ,

$$V_r(\text{peak}) \leq V_m - V_i(\text{min}) = 15 \text{ V} - 7.3 \text{ V} = 7.7 \text{ V}$$

so that

$$V_r(\text{rms}) = \frac{V_r(\text{peak})}{\sqrt{3}} = \frac{7.7 \text{ V}}{1.73} = 4.4 \text{ V}$$

The value of load current is then

$$I_{\text{dc}} = \frac{V_r(\text{rms})C}{2.4} = \frac{(4.4 \text{ V})(250)}{2.4} = 458 \text{ mA}$$

Any current above this value is too large for the circuit to maintain the regulator output at +5 V.

### Adjustable-Voltage Regulators

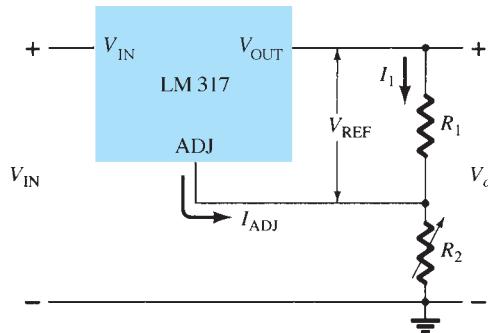
Voltage regulators are also available in circuit configurations that allow the user to set the output voltage to a desired regulated value. The LM317, for example, can be operated with the output voltage regulated at any setting over the range of voltage from 1.2 V to 37 V. Figure 15.30 shows how the regulated output voltage of an LM317 can be set.

Resistors  $R_1$  and  $R_2$  set the output to any desired voltage over the adjustment range (1.2 V to 37 V). The output voltage desired can be calculated using

$$V_o = V_{\text{ref}} \left( 1 + \frac{R_2}{R_1} \right) + I_{\text{adj}} R_2 \quad (15.21)$$

with typical IC values of

$$V_{\text{ref}} = 1.25 \text{ V} \quad \text{and} \quad I_{\text{adj}} = 100 \mu\text{A}$$



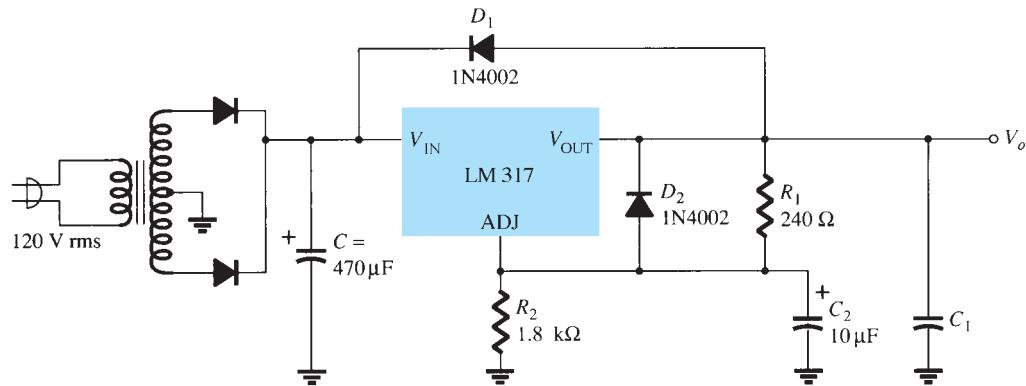
**FIG. 15.30**  
Connection of LM317 adjustable-voltage regulator.

**EXAMPLE 15.15** Determine the regulated voltage in the circuit of Fig. 15.30 with  $R_1 = 240 \Omega$  and  $R_2 = 2.4 \text{ k}\Omega$ .

**Solution:**

$$\begin{aligned} \text{Eq. (15.21): } V_o &= 1.25 \text{ V} \left( 1 + \frac{2.4 \text{ k}\Omega}{240 \Omega} \right) + (100 \mu\text{A})(2.4 \text{ k}\Omega) \\ &= 13.75 \text{ V} + 0.24 \text{ V} = \mathbf{13.99 \text{ V}} \end{aligned}$$

**EXAMPLE 15.16** Determine the regulated output voltage of the circuit in Fig. 15.31.



**FIG. 15.31**  
Positive adjustable-voltage regulator for Example 15.16.

**Solution:** The output voltage calculated using Eq. (15.21) is

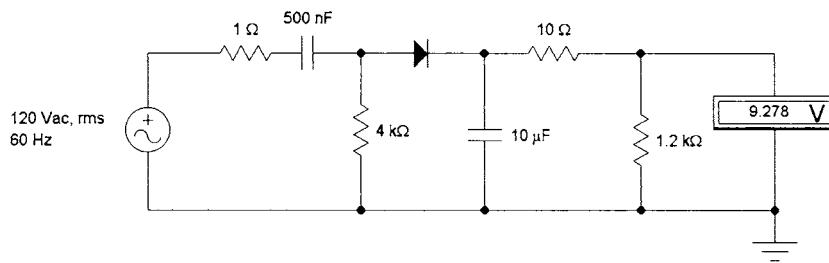
$$V_o = 1.25 \text{ V} \left( 1 + \frac{1.8 \text{ k}\Omega}{240 \Omega} \right) + (100 \mu\text{A})(1.8 \text{ k}\Omega) \approx \mathbf{10.8 \text{ V}}$$

A check of the filter capacitor voltage shows that an input-output difference of 2 V can be maintained up to at least 200 mA load current.

## Power Supplies

Power supplies are a part of every electronic device, so a wide variety of circuits are used to accommodate such factors as power rating, size of circuit, cost, desired regulation, and so on. This section will outline a number of practical supplies and chargers.

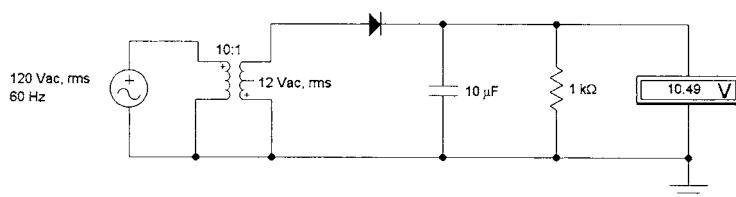
**Simple DC Supply** A simple way to drop the ac voltage, without a bulky and expensive transformer, is to use a capacitor in series with the line voltage. This type of supply, shown in Fig. 15.32, uses few parts and is thus very simple. A half-wave rectifier (or bridge rectifier) with a filter circuit is used to get a voltage with a dc component. This circuit has a number of drawbacks: There is no isolation from the ac line, a minimal current must always be drawn, and the load current cannot be excessive. Thus, the simple dc supply can be used to provide a poorly regulated dc voltage when light current draw is desired in an inexpensive device.



**FIG. 15.32**  
*Simple dc supply.*

**DC Supply with Transformer Input** The next type of power supply uses a transformer to step down the ac line voltage. The transformer can be either a wall mount (external) or a chassis mount (internal). A rectifier is used after the transformer, followed by a capacitor filter and possibly a regulator. The regulator becomes a problem as the power requirements increase. Heat sink size, cooling, and power requirements become a major obstacle to these types of supplies.

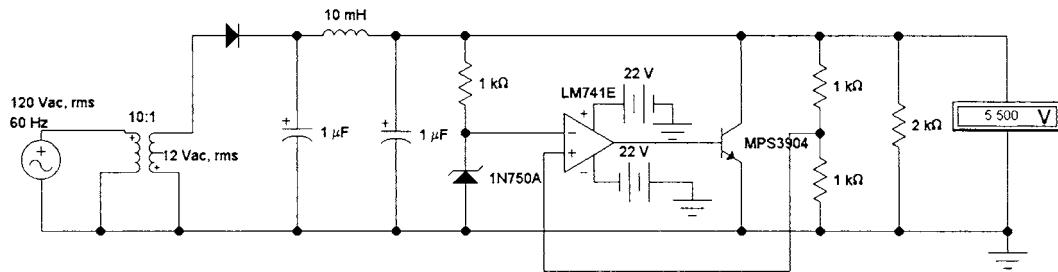
Figure 15.33 shows a simple half-wave rectified supply with an isolating step-down transformer. This relatively simple circuit provides no regulation.



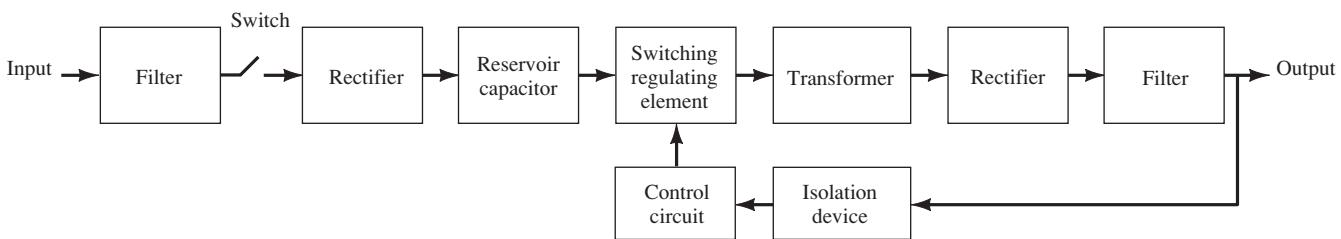
**FIG. 15.33**  
*DC supply with transformer input.*

Figure 15.34 shows probably the best standard power supply—with transformer isolation and voltage step-down; a bridge rectifier; a dual filter with choke; and a regulator circuit made of a Zener reference, a parallel regulation transistor, and an op-amp with feedback to aid the regulation. This circuit obviously provides excellent voltage regulation.

**Chopper Supply** Today's power supplies convert ac to dc using a chopper circuit such as that shown in Fig. 15.35. The ac input is connected to the circuit through various line conditioners and filters. This removes any electrical noise. The input is then rectified and lightly filtered. The high dc voltage is chopped at a rate of approximately 100 kHz. The rate and the duration of the chopping are controlled by a special-function integrated circuit. An isolation transformer couples the chopped dc to a filtering and rectifying circuit. The output of the power supply is fed back to the control integrated circuit. By monitoring the output, the IC can regulate the output voltage. Although this type of power supply is more complicated, it



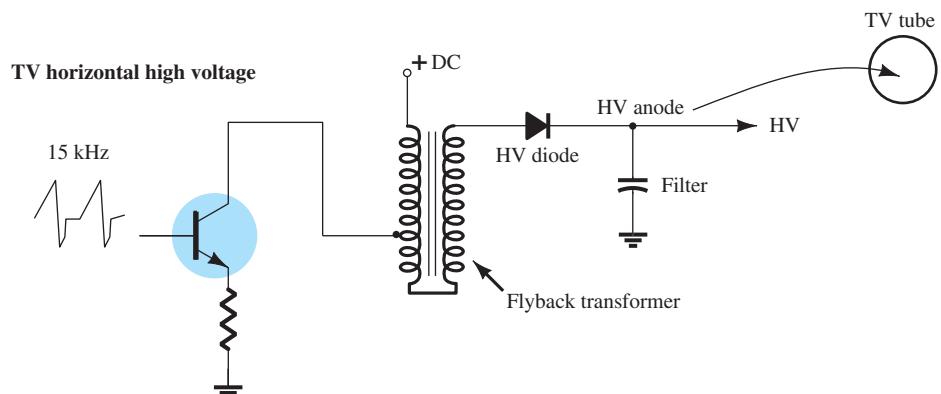
**FIG. 15.34**  
Series-regulated supply with transformer input and IC regulation.



**FIG. 15.35**  
Block diagram of chopper power supply.

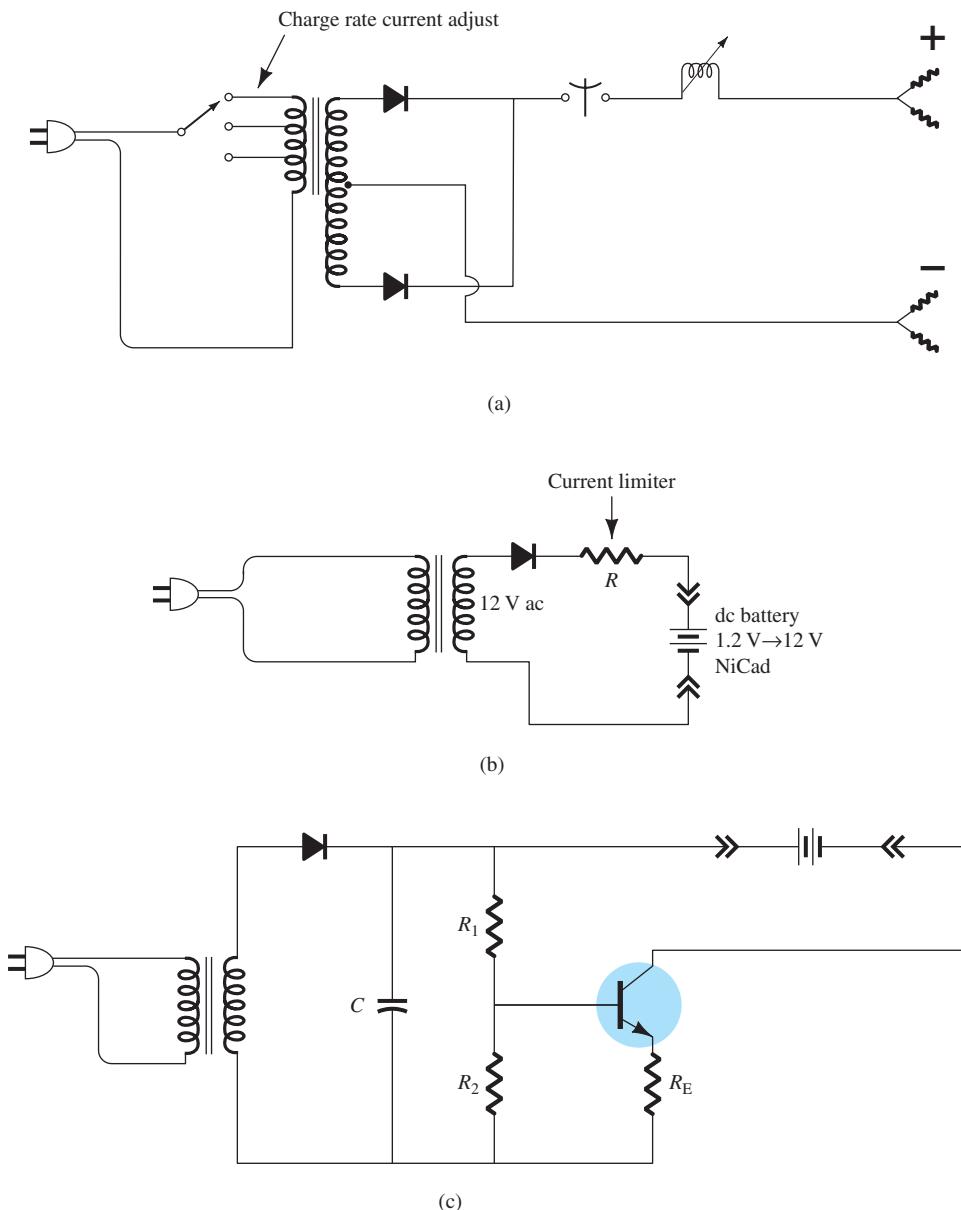
has many advantages over traditional supplies. For example, it operates over a very large range of input ac voltages, it operates independently of the input frequency, it can be made very small, and it operates over a large range of current demands and low heat dissipation.

**Special TV Horizontal High-Voltage Supply** Television sets require a very high dc voltage to operate the picture tube (cathode ray tube, CRT). In early TV sets this voltage was supplied by a high-voltage transformer with very high voltage rated capacitors. The circuit was very bulky, heavy, and dangerous. TV sets utilize two basic frequencies to scan the screen: 60 Hz (vertical oscillator) and 15 kHz (horizontal oscillator). Using the horizontal oscillator, one can build a high-voltage dc supply. The circuit is known as a *flyback power supply* (see Fig. 15.36). The low dc voltage is pulsed into a small flyback transformer. The flyback transformer is a step-up autotransformer. The output is rectified and filtered with a small-value capacitor. The flyback transformer can be small, and the filter capacitor can be a small, low-value unit, because the frequency is very high. This type of circuit is lightweight and very reliable.



**FIG. 15.36**  
TV horizontal high-voltage supply.

**Battery Charger Circuits** Battery charger circuits employ variations of the power supply circuits mentioned above. Figure 15.37a shows the basics of a simple charging circuit using a transformer setting with a selector switch to determine the charge rate current provided. For NiCad batteries the voltage that supplies the battery must be greater than the

**FIG. 15.37**

*Battery charger circuits: (a) Single charging circuit; (b) typical NiCad charging circuit; (c) lead-acid charging circuit.*

battery being charged. The current must also be controlled and limited. Figure 15.37b shows a typical NiCad charging circuit. For a lead-acid battery, the voltage must be controlled so as not to exceed the battery's rated voltage. The charge current is determined by the power supply's capability, the power rating of the battery, and the amount of charge required. Figure 15.37c shows a simple lead-acid charging circuit.

Batteries can be charged using traditional dc supplies or from more elaborate chopper supplies. The major problem with charging batteries is determining when the battery is completely charged. Many exotic circuits exist to check the battery status.

## 15.8 SUMMARY

### Equations

Ripple:

$$r = \frac{\text{ripple voltage (rms)}}{\text{dc voltage}} = \frac{V_r(\text{rms})}{V_{dc}} \times 100\%$$

Voltage regulation:

$$\%V.R. = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\%$$

Half-wave rectifier:

$$V_{dc} = 0.318V_m, \quad V_r(\text{rms}) = 0.385V_m$$

$$r = \frac{0.385V_m}{0.318V_m} \times 100\% = 121\%$$

Full-wave rectifier:

$$V_{dc} = 0.636V_m, \quad V_r(\text{rms}) = 0.308V_m$$

$$r = \frac{0.308V_m}{0.636V_m} \times 100\% = 48\%$$

Simple capacitor filter:

$$V_r(\text{rms}) = \frac{I_{dc}}{4\sqrt{3}fC} = \frac{2.4I_{dc}}{C} = \frac{2.4V_{dc}}{R_L C}, \quad V_{dc} = V_m - \frac{I_{dc}}{4fC} = \frac{4.17I_{dc}}{C}$$

$$r = \frac{V_r(\text{rms})}{V_{dc}} \times 100\% = \frac{2.4I_{dc}}{CV_{dc}} \times 100\% = \frac{2.4}{R_L C} \times 100\%$$

RC filter:

$$V'_{dc} = \frac{R_L}{R + R_L} V_{dc}, \quad X_C = \frac{1.3}{C}, \quad V'_r(\text{rms}) = \frac{X_C}{R} V_r(\text{rms})$$

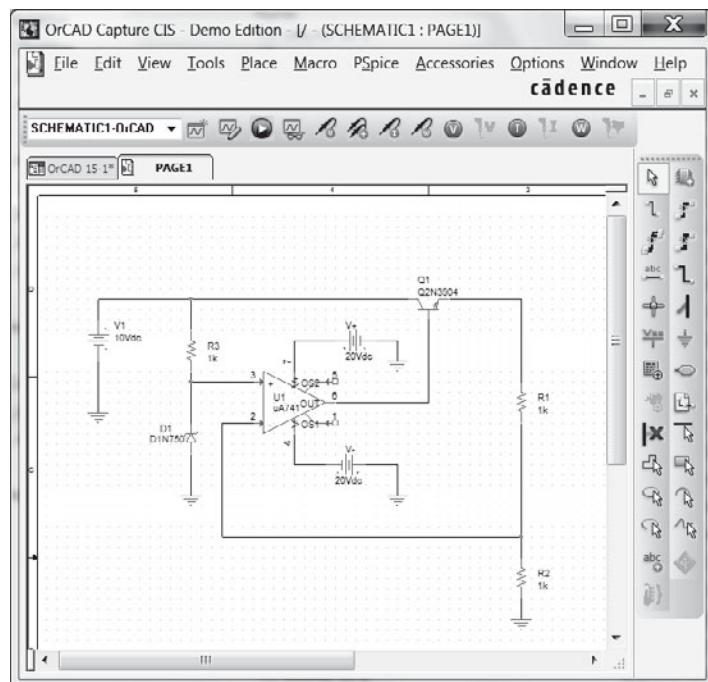
Op-amp series regulator:

$$V_o = \left(1 + \frac{R_1}{R_2}\right) V_Z$$

## 15.9 COMPUTER ANALYSIS

### Program 15.1—Op-Amp Series Regulator

The op-amp series regulator circuit of Fig. 15.16 can be analyzed using PSpice, with the resulting schematic drawn as shown in Fig. 15.38. The **Analysis Setup** was used to provide

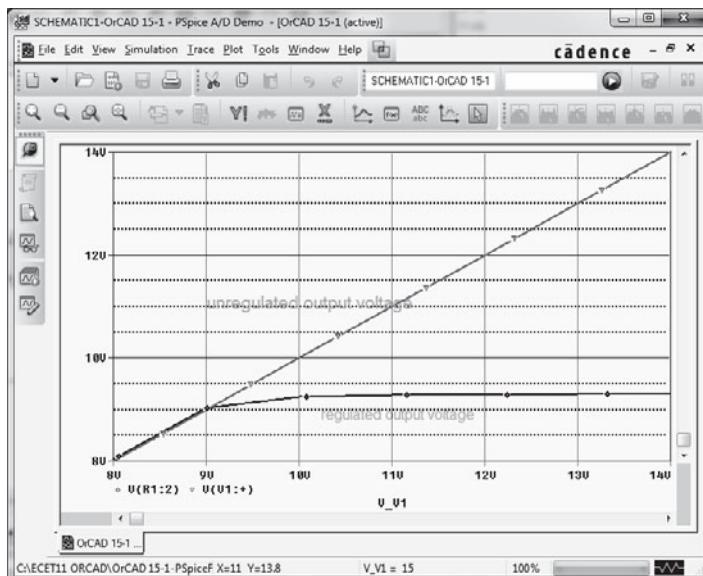


**FIG. 15.38**  
Op-amp series regulator using PSpice.

a dc voltage sweep from 8 V to 15 V in 0.5-V increments. Diode  $D_1$  provides a Zener voltage of 4.7 V ( $V_Z = 4.7$ ), and transistor  $Q_1$  is set to beta = 100. Using Eq. (15.18), we obtain

$$V_o = \left(1 + \frac{R_1}{R_2}\right)V_Z = \left(1 + \frac{1\text{ k}\Omega}{1\text{ k}\Omega}\right)4.7\text{ V} = 9.4\text{ V}$$

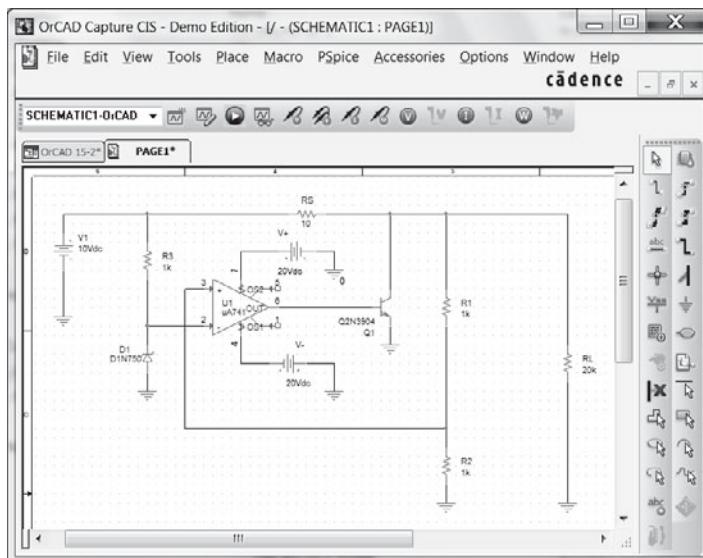
Notice in Fig. 15.38 that the regulated output voltage is 9.25 V when the input is 10 V. Figure 15.39 shows the PROBE output for the dc voltage sweep. Notice also that after the input goes above about 9 V, the output is held regulated at about 9.3 V.



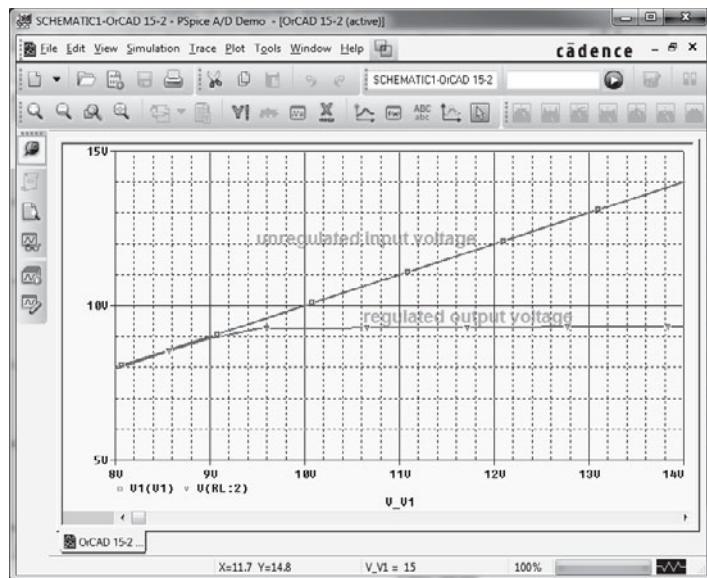
**FIG. 15.39**  
Probe output showing the voltage regulation of Fig. 15.38.

## Program 15.2—Shunt Voltage Regulator Using Op-Amp

The shunt voltage regulator circuit of Fig. 15.40 was drawn using PSpice. With the Zener voltage set at 4.7 V and transistor beta set at 100, the output is 9.255 V when the input is 10 V. A dc sweep from 8 V to 15 V is shown in the PROBE output in Fig. 15.41. The circuit provides good voltage regulation for inputs from about 9.5 V to over 14 V, the output being held at the regulated value of about 9.3 V.



**FIG. 15.40**  
Shunt voltage regulator using an op-amp.



**FIG. 15.41**  
Probe output for the dc voltage sweep of Fig. 15.40.

## PROBLEMS

\*Note: Asterisks indicate more difficult problems.

### 15.2 General Filter Considerations

1. What is the ripple factor of a sinusoidal signal having peak ripple of 2 V on an average of 50 V?
2. A filter circuit provides an output of 28 V unloaded and 25 V under full-load operation. Calculate the percentage voltage regulation.
3. A half-wave rectifier develops 20 V dc. What is the value of the ripple voltage?
4. What is the rms ripple voltage of a full-wave rectifier with output voltage 8 V dc?

### 15.3 Capacitor Filter

5. A simple capacitor filter fed by a full-wave rectifier develops 14.5 V dc at 8.5% ripple factor. What is the output ripple voltage (rms)?
6. A full-wave rectified signal of 18 V peak is fed into a capacitor filter. What is the voltage regulation of the filter if the output is 17 V dc at full load?
7. A full-wave rectified voltage of 18 V peak is connected to a  $400\text{-}\mu\text{F}$  filter capacitor. What are the ripple and dc voltages across the capacitor at a load of 100 mA?
8. A full-wave rectifier operating from the 60-Hz ac supply produces a 20-V peak rectified voltage. If a  $200\text{-}\mu\text{F}$  capacitor is used, calculate the ripple at a load of 120 mA.
9. A full-wave rectifier (operating from a 60-Hz supply) drives a capacitor-filter circuit ( $C = 100 \mu\text{F}$ ), which develops 12 V dc when connected to a  $2.5\text{-k}\Omega$  load. Calculate the output voltage ripple.
10. Calculate the size of the filter capacitor needed to obtain a filtered voltage having 15% ripple at a load of 150 mA. The full-wave rectified voltage is 24 V dc, and the supply is 60 Hz.
- \*11. A  $500\text{-}\mu\text{F}$  capacitor provides a load current of 200 mA at 8% ripple. Calculate the peak rectified voltage obtained from the 60-Hz supply and the dc voltage across the filter capacitor.
12. Calculate the size of the filter capacitor needed to obtain a filtered voltage with 7% ripple at a load of 200 mA. The full-wave rectified voltage is 30 V dc and the supply is 60 Hz.
13. Calculate the percentage ripple for the voltage developed across a  $120\text{-}\mu\text{F}$  filter capacitor when providing a load current of 80 mA. The full-wave rectifier operating from the 60-Hz supply develops a peak rectified voltage of 25 V.

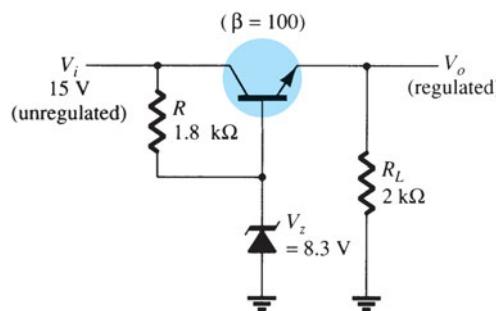
### 15.4 RC Filter

14. An  $RC$  filter stage is added after a capacitor filter to reduce the percentage of ripple to 2%. Calculate the ripple voltage at the output of the  $RC$  filter stage providing 80 V dc.

- \*15. An  $RC$  filter stage ( $R = 33 \Omega$ ,  $C = 120 \mu\text{F}$ ) is used to filter a signal of 24 V dc with 2 V rms operating from a full-wave rectifier. Calculate the percentage ripple at the output of the  $RC$  section for a 100-mA load. Also calculate the ripple of the filtered signal applied to the  $RC$  stage.
- \*16. A simple capacitor filter has an input of 40 V dc. If this voltage is fed through an  $RC$  filter section ( $R = 50 \Omega$ ,  $C = 40 \mu\text{F}$ ), what is the load current for a load resistance of  $500 \Omega$ ?
17. Calculate the rms ripple voltage at the output of an  $RC$  filter section that feeds a  $1\text{-k}\Omega$  load when the filter input is 50 V dc with 2.5-V rms ripple from a full-wave rectifier and capacitor filter. The  $RC$  filter section components are  $R = 100 \Omega$  and  $C = 100 \mu\text{F}$ .
18. If the no-load output voltage for Problem 17 is 50 V, calculate the percentage voltage regulation with a  $1\text{-k}\Omega$  load.

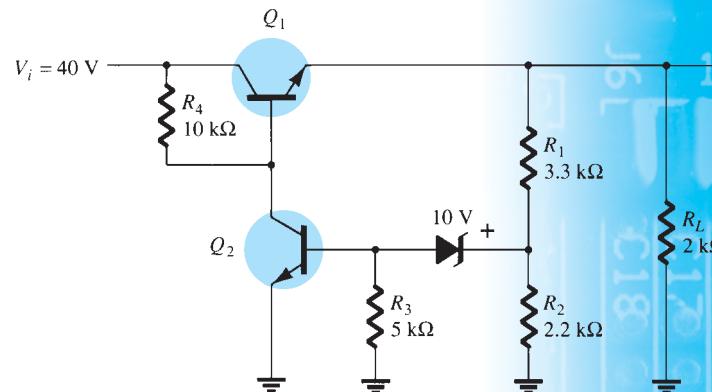
### 15.5 Discrete Transistor Voltage Regulation

- \*19. Calculate the output voltage and Zener diode current in the regulator circuit of Fig. 15.42.
20. What regulated output voltage results in the circuit of Fig. 15.43?



**FIG. 15.42**

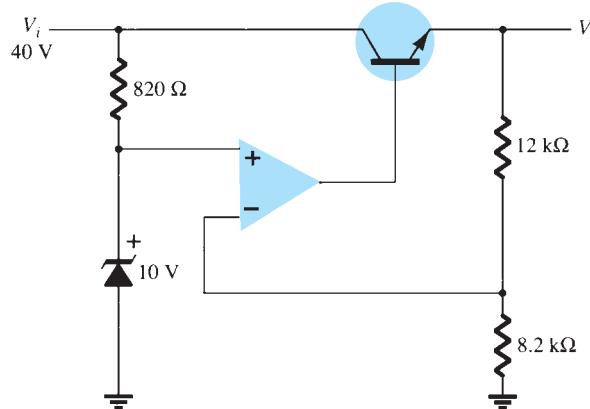
Problem 19.



**FIG. 15.43**

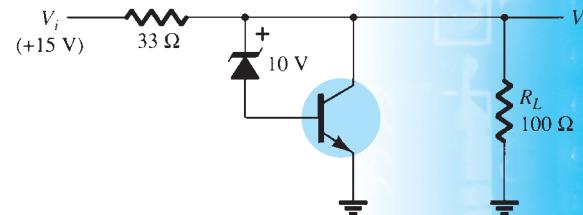
Problem 20.

21. Calculate the regulated output voltage in the circuit of Fig. 15.44.
22. Determine the regulated voltage and circuit currents for the shunt regulator of Fig. 15.45.



**FIG. 15.44**

Problem 21.

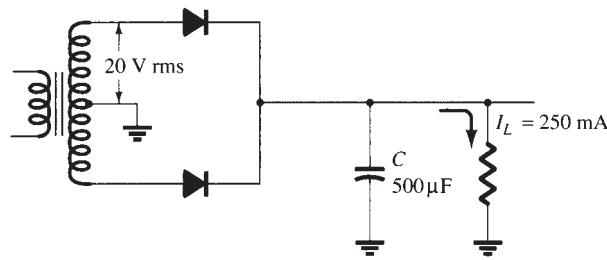


**FIG. 15.45**

Problem 22.

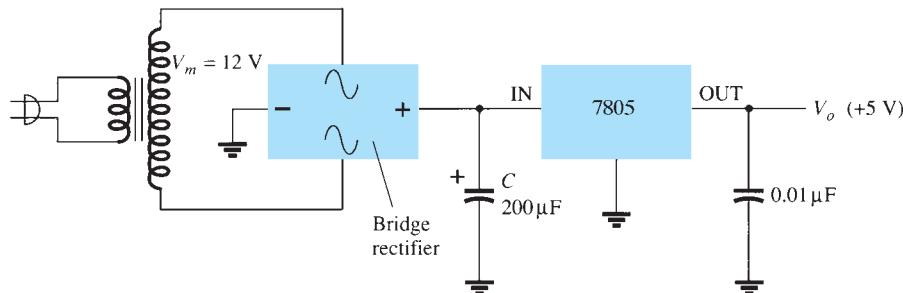
### 15.6 IC Voltage Regulators

23. Draw the circuit of a voltage supply comprised of a full-wave bridge rectifier, capacitor filter, and IC regulator to provide an output of +12 V.
- \*24. Calculate the minimum input voltage of the full-wave rectifier and filter capacitor network in Fig. 15.46 when connected to a load drawing 250 mA.
- \*25. Determine the maximum value of load current at which regulation is maintained for the circuit of Fig. 15.47.



**FIG. 15.46**

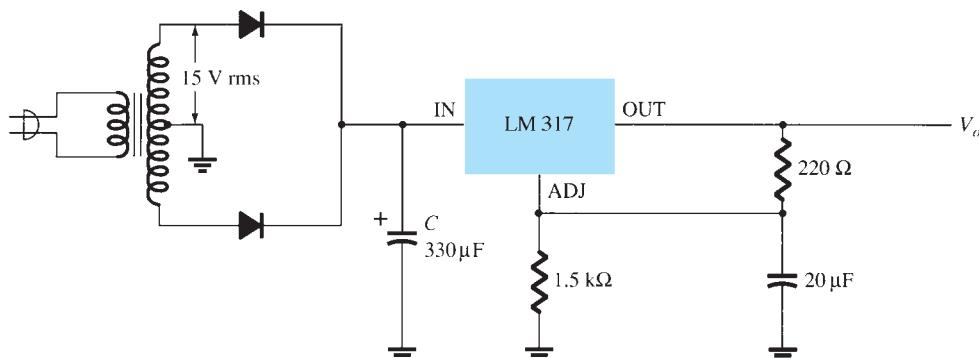
Problem 24.



**FIG. 15.47**

Problem 25.

26. Determine the regulated voltage in the circuit of Fig. 15.30 with  $R_1 = 240 \Omega$  and  $R_2 = 1.8 \text{ k}\Omega$ .
27. Determine the regulated output voltage from the circuit of Fig. 15.48.



**FIG. 15.48**

Problem 27.

### 15.9 Computer Analysis

- \*28. Modify the circuit of Fig. 15.38 to include a load resistor  $R_L$ . Keeping the input voltage fixed at 10 V, do a sweep of the load resistor from  $100 \Omega$  to  $20 \text{ k}\Omega$ , showing the output voltage using Probe.
- \*29. For the circuit of Fig. 15.40, do a sweep showing the output voltage for  $R_L$  varied from  $5 \text{ k}\Omega$  to  $20 \text{ k}\Omega$ .
- \*30. Run a PSpice analysis of the circuit of Fig. 15.19 for  $V_Z = 4.7 \text{ V}$  and beta ( $Q_1$ ) = beta ( $Q_2$ ) = 100, and vary  $V_i$  from 5 V to 20 V.