EECS 151/251A: Discussion 1

Intro, Boolean Algebra, Verilog Basics

8/30/2019

Intro

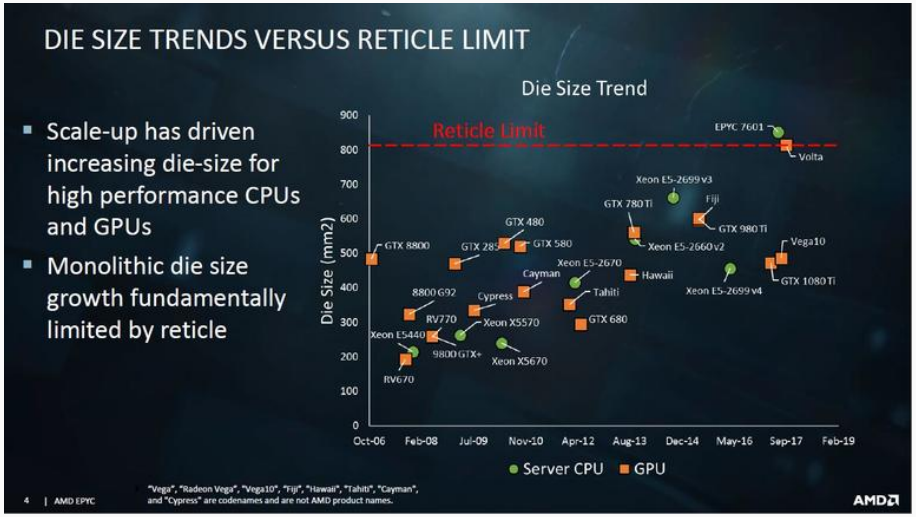
- A bit about me
- Each discussion will review the week's lectures and provide a few examples and questions to solve
- All labs, discussions, and lectures will be posted on the website `http://inst.eecs.berkeley.edu/~eecs151/fa19/`
- All instructor and TA office hours are on the website
- Sign up for Piazza `https://piazza.com/class/jzjemj1hg0z2nj`
- No textbook required. Digital Integrated Circuits (Rabaey) is helpful.

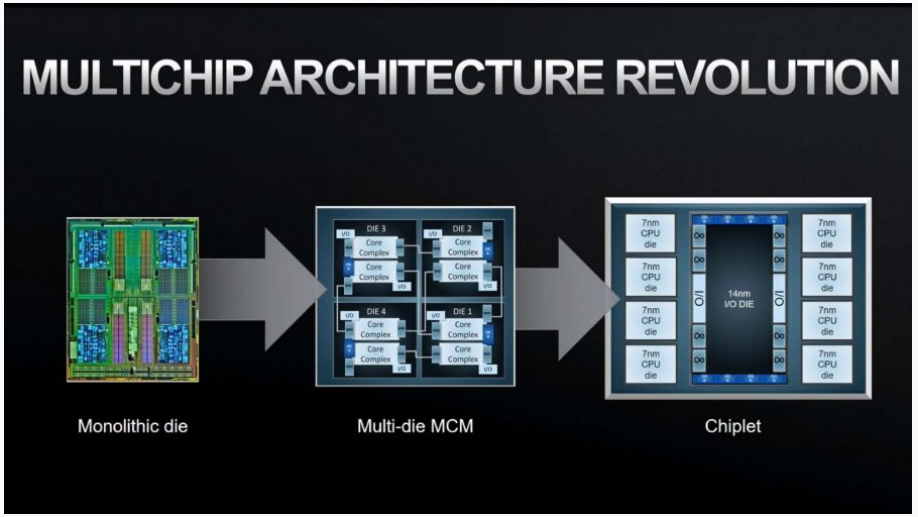
Pre-Reqs

- CS61C
  - C
  - digital logic
  - RISC-V ISA
  - 3/5-stage CPU pipeline
  - hazard handling
- EE16A/B
  - RC circuits
  - energy and power

Scaling

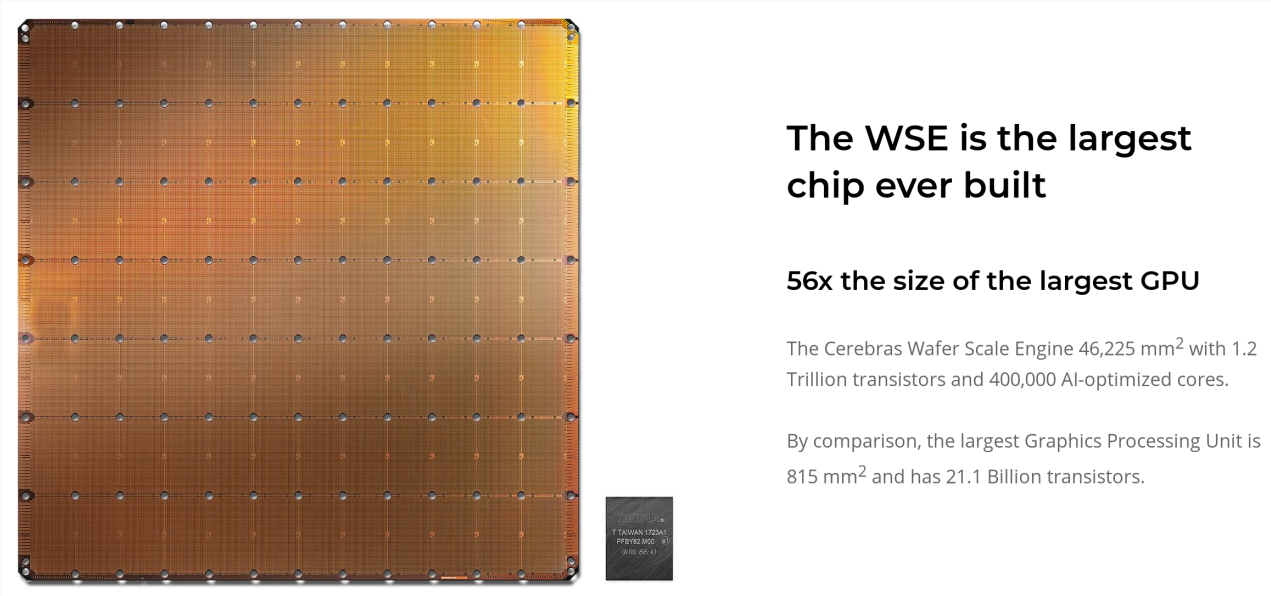
- *Moore's Law*: Number of transistors per chip doubles every two years $\rightarrow$ cost per transistor is halved.
  - Cost isn't going down anymore when scaling to a new node
  - But increasing die size and chiplet packaging can keep the trend alive





Wafer-Scale Integration

- Startup Cerebras presented a wafer-scale ML accelerator at HotChips this year
- Defects always exist on such a large scale, need redundancy
- Consumes **15 kW**! Custom cooling solution and power delivery required



Scaling

- *Dennard Scaling*: As MOSFETs scale down, voltages and currents scale proportionally and power density stays constant
  - Delay $\approx C \cdot V / I_{avg}$ (scales down linearly with transistor shrink)
  - $P \approx C \cdot V^2 /$ Delay (scales down quadratically)

Device or Circuit Parameter	Scaling Factor
Device dimension t_{ox}, L, W	$1/\kappa$
Doping concentration N_a	κ
Voltage V	$1/\kappa$
Current I	$1/\kappa$
Capacitance $\epsilon A/t$	$1/\kappa$
Delay time/circuit VC/I	$1/\kappa$
Power dissipation/circuit VI	$1/\kappa^2$
Power density VI/A	1

Logic Operators

- Logic operators work over boolean symbols
- Common boolean operators include AND, OR, and NOT
- We will usually write AND as ‘multiplication’, OR as ‘addition’, and NOT with an overline
- e.g. A AND B OR (NOT C) $= AB + \overline{C}$
- Logic operators in boolean expressions map to digital logic gates (a key abstraction)

Boolean Algebra

- Review some basic boolean algebra laws
- OR Identity: $A + 1 = 1$, $A + 0 = A$, $A + \overline{A} = 1$
- AND Identity: $A1 = A$, $A0 = 0$, $A\overline{A} = 0$
- Absorption: $A + AB = A$, $A(A + B) = A$
- DeMorgan's Laws: $\overline{A + B} = \overline{A}\,\overline{B}$, $\overline{AB} = \overline{A} + \overline{B}$

Verilog

- Check out the Verilog Primer Slides before Lab 2