Homework 4

P1 (a) add x_1, x_2, x_3

0000000 00011 00010 000 00001 0110011

(b) addi x_1, x_2, 100

000001100100 00010 000 00001 0010011

(c) lb x1, 4(x2)

000000000100 00010 000 00001 0000011

(d) beq x6, x8, 1024

0 000000 01000 00110 000 00001 1100011

P2 a) x1=100, x2=100, x3=200

b) x0 = 0, x1 = 100

c) 0xdead = -8531; 0xbeef = -16657; 0x1024 = 4132

x1 = 0xdead, x2 = 0xbeef, x4 = 0xdead.

d) x1 = -1, x2 = 1, x3 = 100

e) x_1=0 → x2=8, PC=20 → x3=24, PC = 8 → x1 = 100 → x1=300 → nop

x1=300, x2 = 8, x3 = 24.

P3 a) nop: addi x0, x0, 0

b) mv rd, rs: addi rd, rs, 0

c) li rd, imm: lui rd, imm[31:12]

addi rd, rd, imm[]

slli rd, rd, 5'd12

addi rd, rd, imm[11:0]

d) beqz rs, imm: beq rs, x0, imm

e) j imm: jal x0, imm

f) bgt rs1, rs2, imm: blt rs2, rs1, imm

P4 a)

WBSel JAL ↑ JALR ↑

pc+4 10: Jal(1101111) Jalr(1100111)
alu 01: add(0110011) addi(0010011) auipc(0010111)
mem 00: lw(0000011)

OP-FP OP-IMM AUIPC LOAD

```
sig[1:0]
assign sig[1] = (opcode == JAL) || (opcode == JALR)
assign sig[0] = (opcode == OP-FP) || (opcode == OP-IMM) || (opcode == AUIPC)
```

b) MemRW, 0: read, 1: write

0: add(0110011) addi(0010011) lw(0000011)
1: sw(0100011)

```
assign sig = (opcode == STORE)
```

c) PCSel

PC+4 0: add(0110011); addi(0010011); lw(0000011); sw(0100011)
alu 1: beq(1100011); jal(1101111); jalr(1100111)

```
assign sig = (opcode == BRANCH) || (opcode == JALR) || (opcode == JAL)
```

d) BSel

rs2 0: add(0110011)
imm 1: addi(0010011); lw(0000011); sw(0100011); beq(1100011); ...

```
assign sig = (opcode != OP-FP)
```