

EECS151 : Introduction to Digital Design and ICs

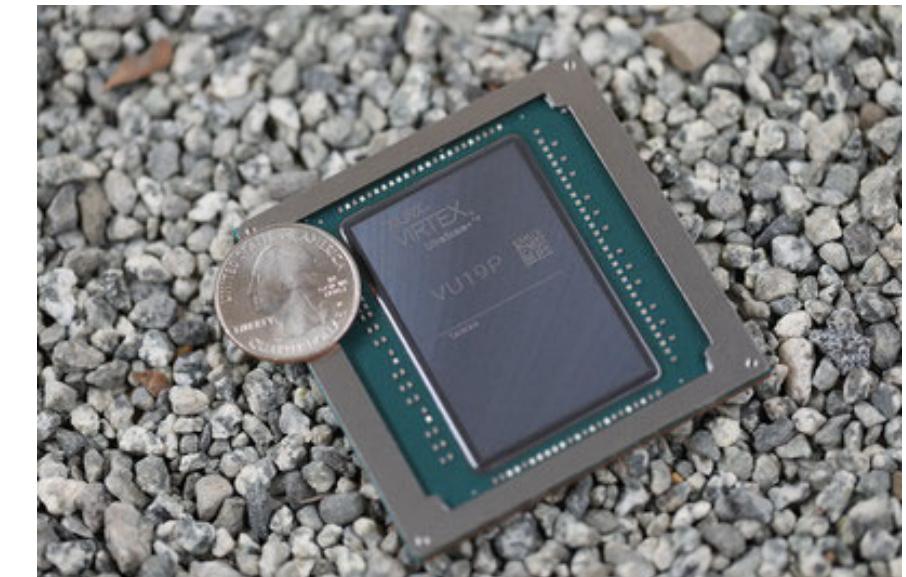
Lecture 11 – CMOS



Bora Nikolić and Sophia Shao

Xilinx Announces the World's Largest FPGA
Featuring 9 Million System Logic Cells

Aug. 21, 2019, Xilinx announced 16 nm Virtex® UltraScale+™ family to now include the world's largest FPGA — the Virtex UltraScale+ VU19P. The VU19P sets a new standard in FPGAs, featuring 9 million system logic cells, up to 1.5 Tb/s of DDR4 memory bandwidth and up to 4.5 Tb/s of transceiver bandwidth, and over 2,000 user I/Os.

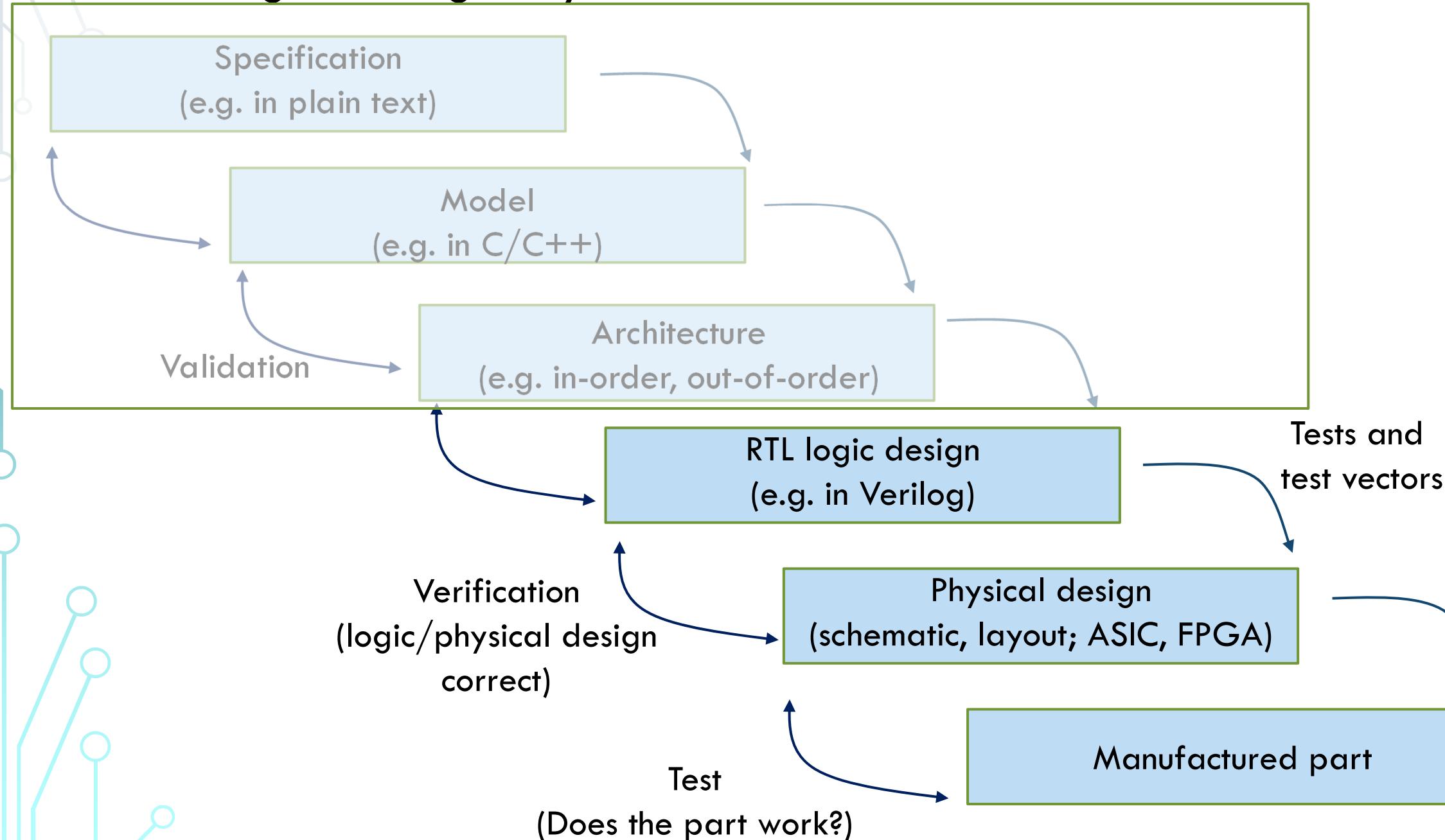


Review

- FPGAs are widely used for hardware prototyping and accelerating key applications.
- Core FPGA building blocks:
 - Configurable Logic Blocks (CLBs)
 - Slices
 - Look-Up Tables
 - Flip-Flops
 - Carry chain
 - Configurable Interconnect
 - Switch boxes
- Modern FPGA Designs:
 - BRAMs, DSPs, and AI Engines

Design Process

- Design through layers of abstractions





CMOS Process

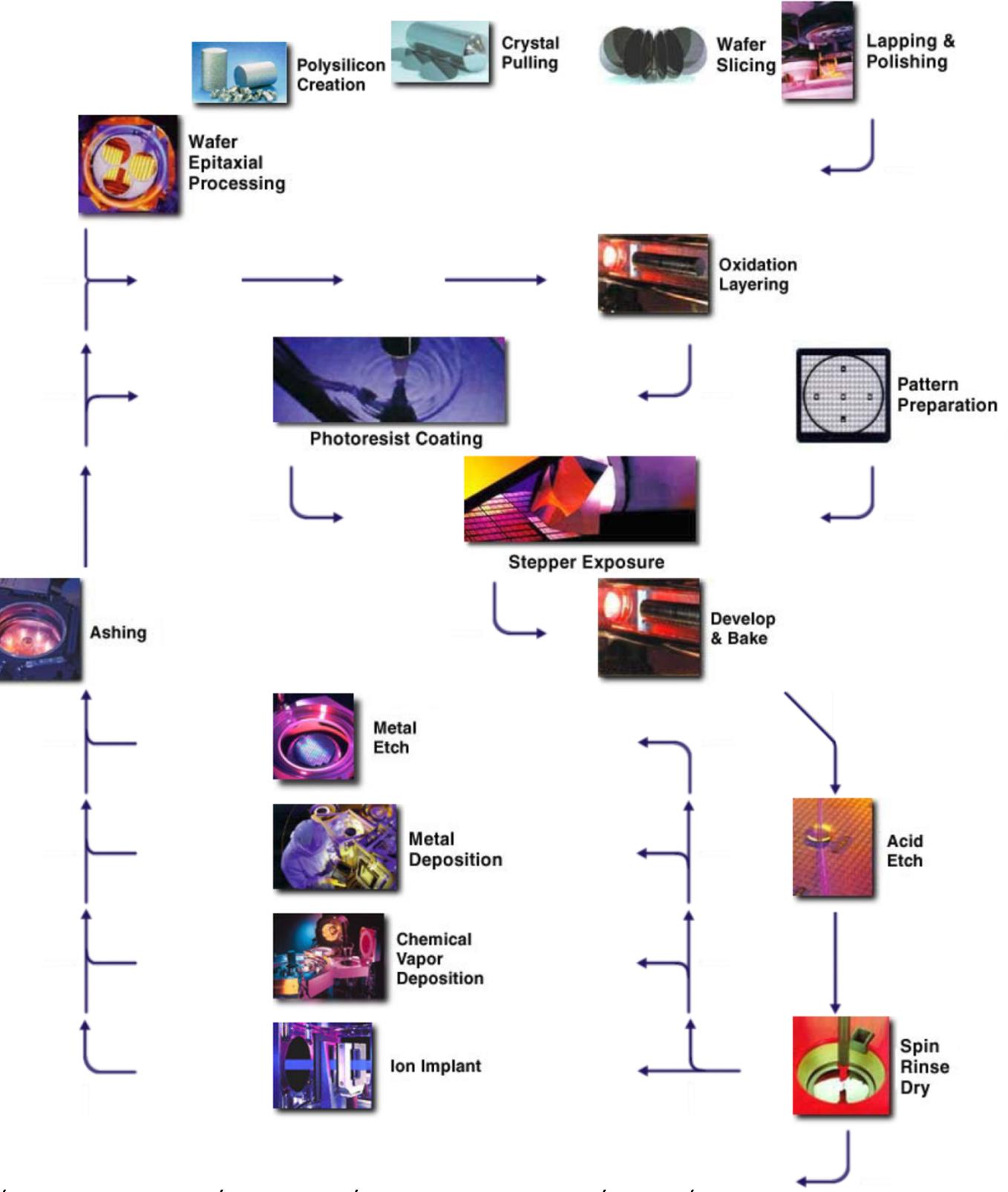
Semiconductor Manufacturing

- Repetitive steps (40-70 masks):

- Passivation
- Photoresist coating
- Patterning (stepper)
- Develop
- Etch
- Process step
 - Etching
 - Deposition
 - Implant
- Remove resist
- Repeat

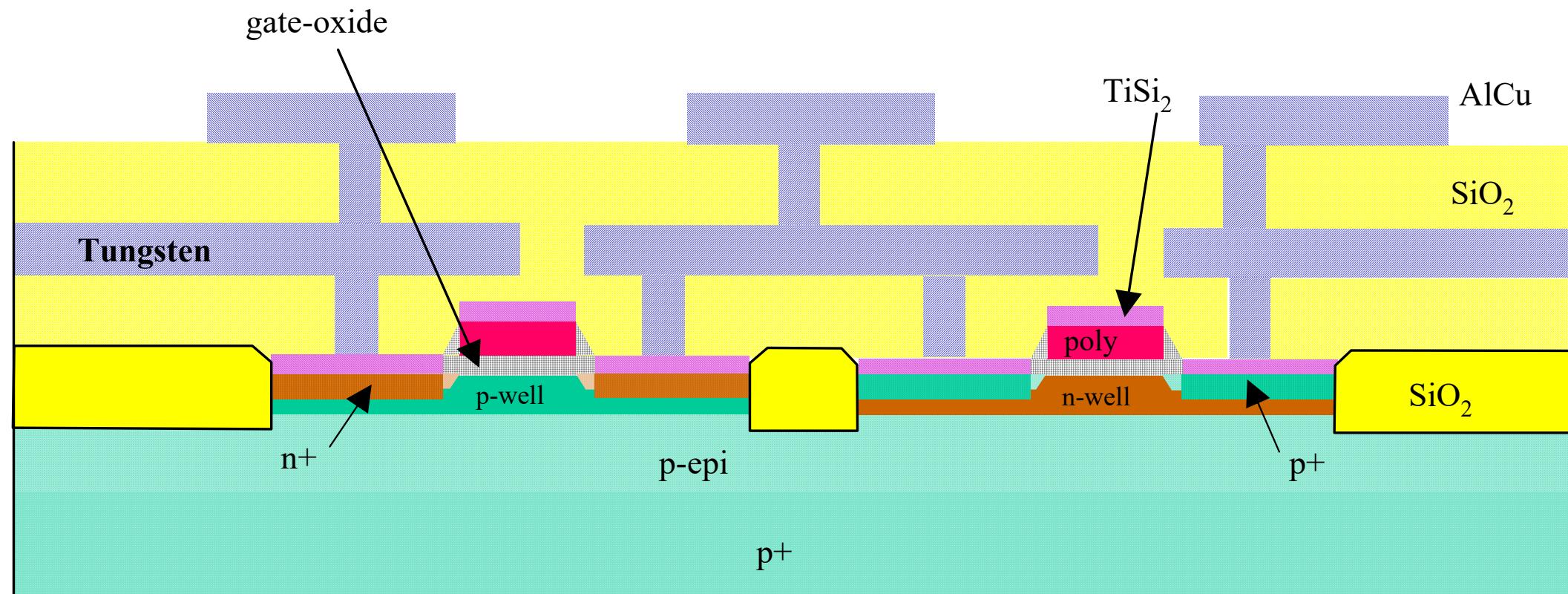
- Zoom into a chip:

<https://youtu.be/Fxv3JoS1uY8>



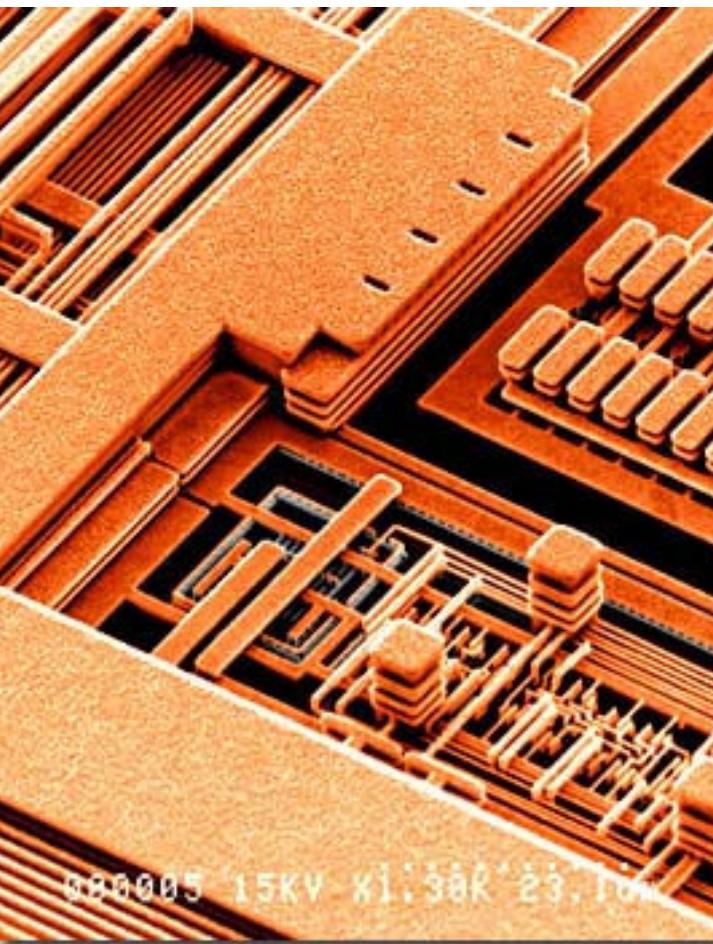
CMOS Process

- Post ~250nm CMOS
- Shallow-trench isolation, dual/triple-well process

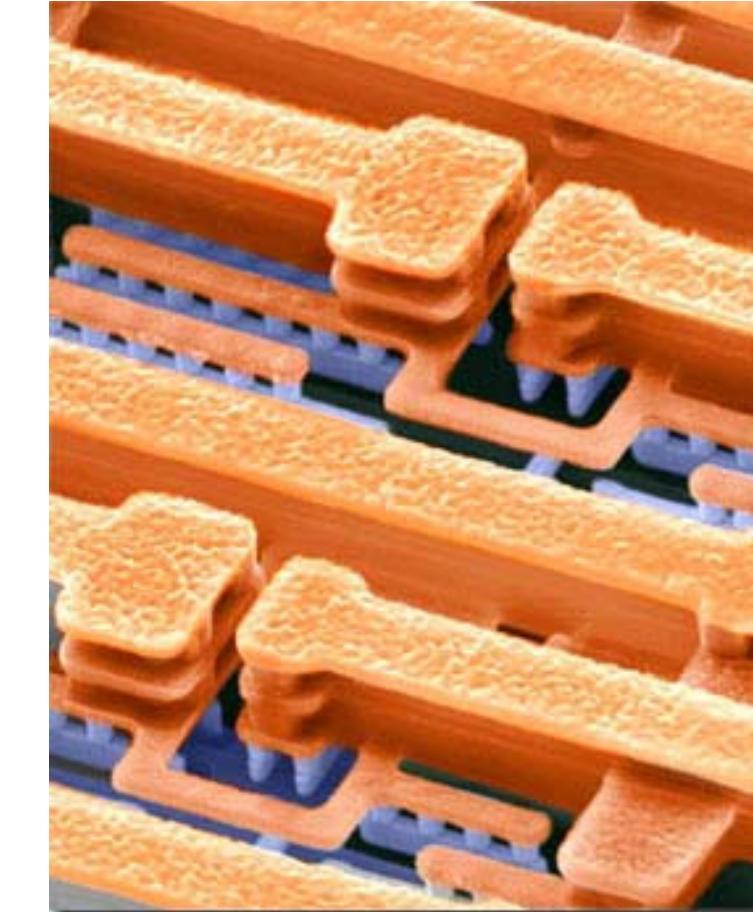


Metal Stack

- Interconnect is predominantly copper



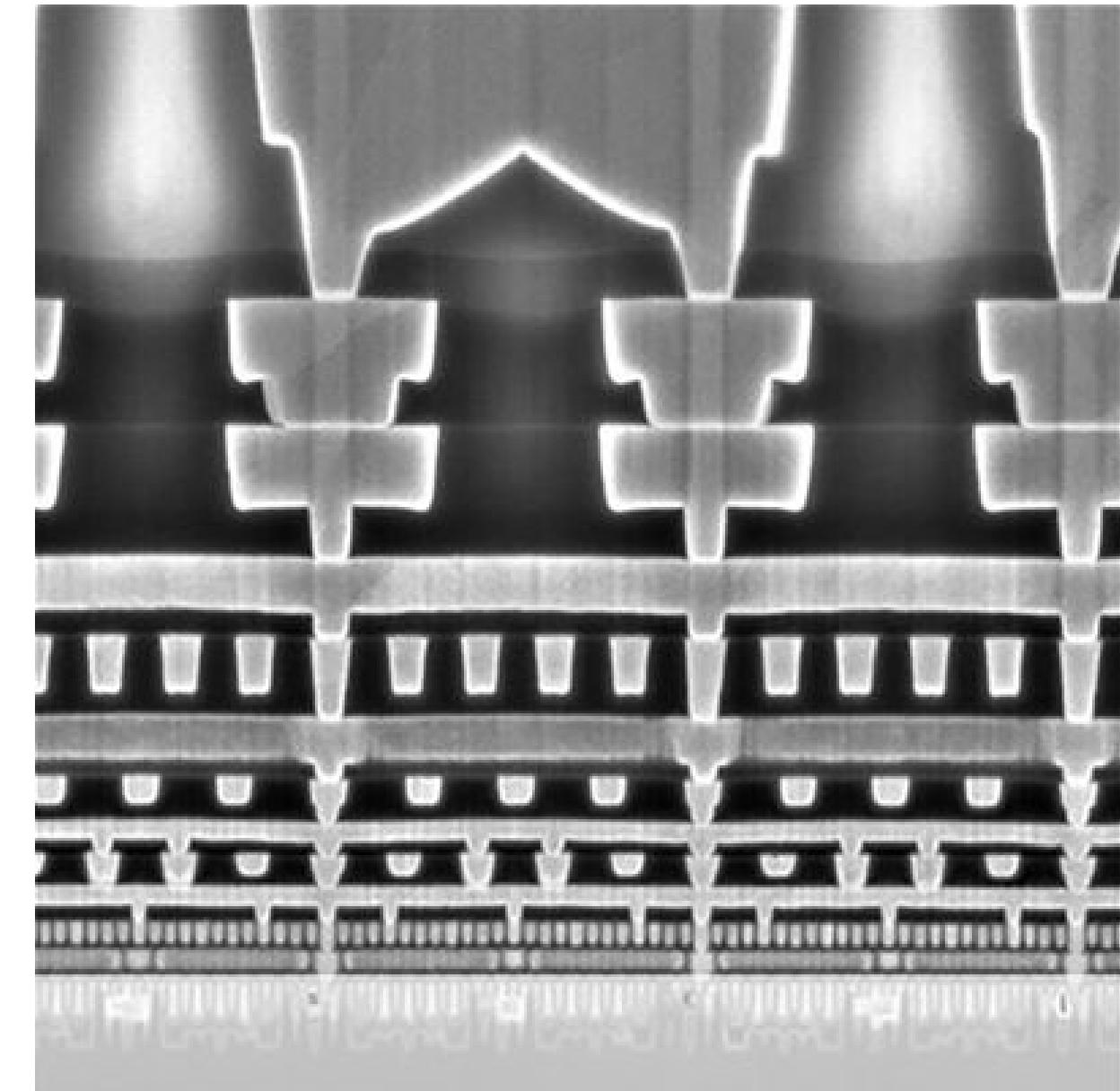
SEM view of Copper Interconnect
(IBM Microelectronics)



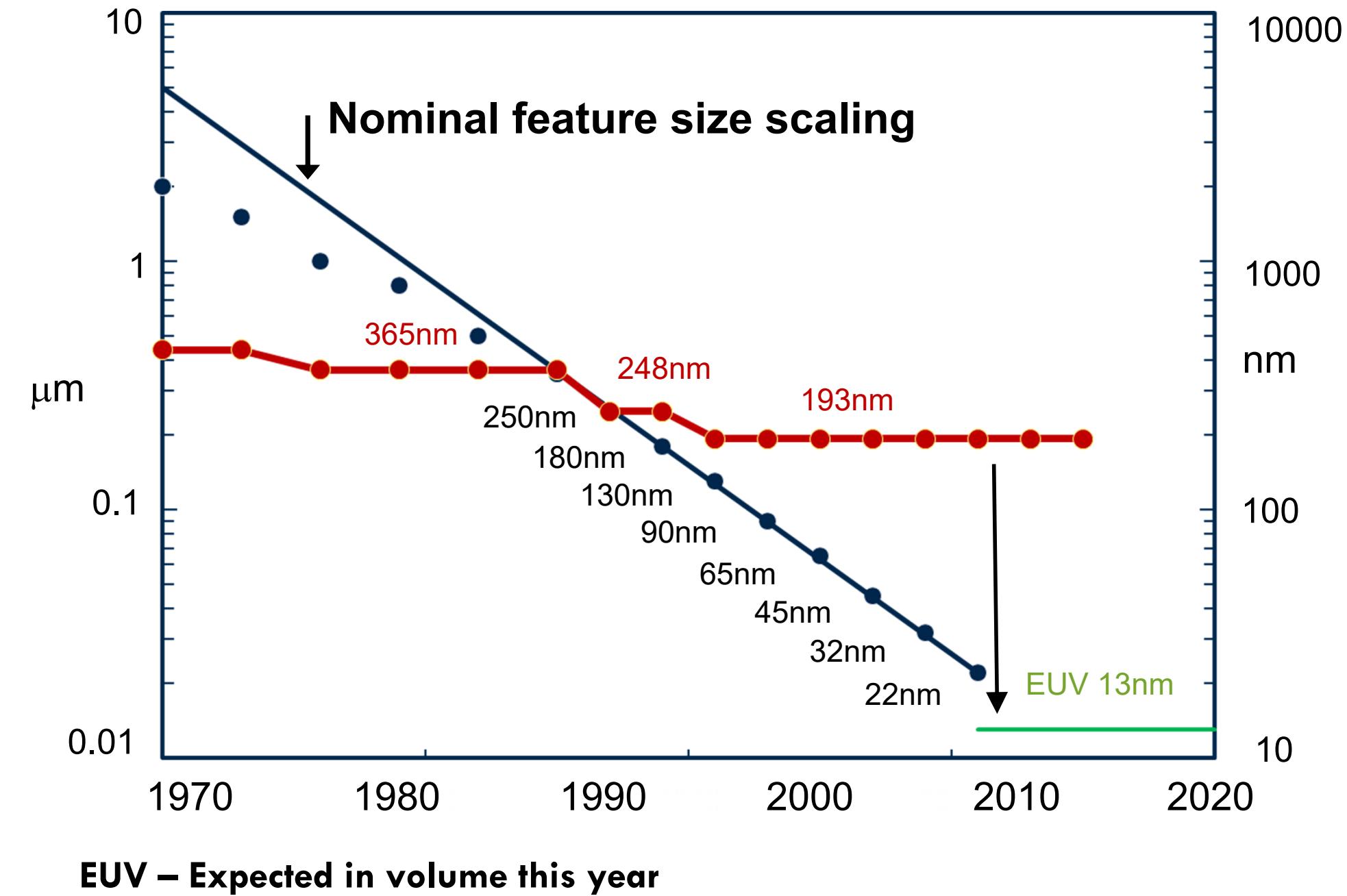
SEM view of Copper Interconnect
(IBM Microelectronics)

Metal Stack in Modern Processes

- Metal stack
 - Bottom layers have pitch that matches transistors
 - Intermediate are 2-4x
 - Top layers are wide and thick: Power distribution, clock

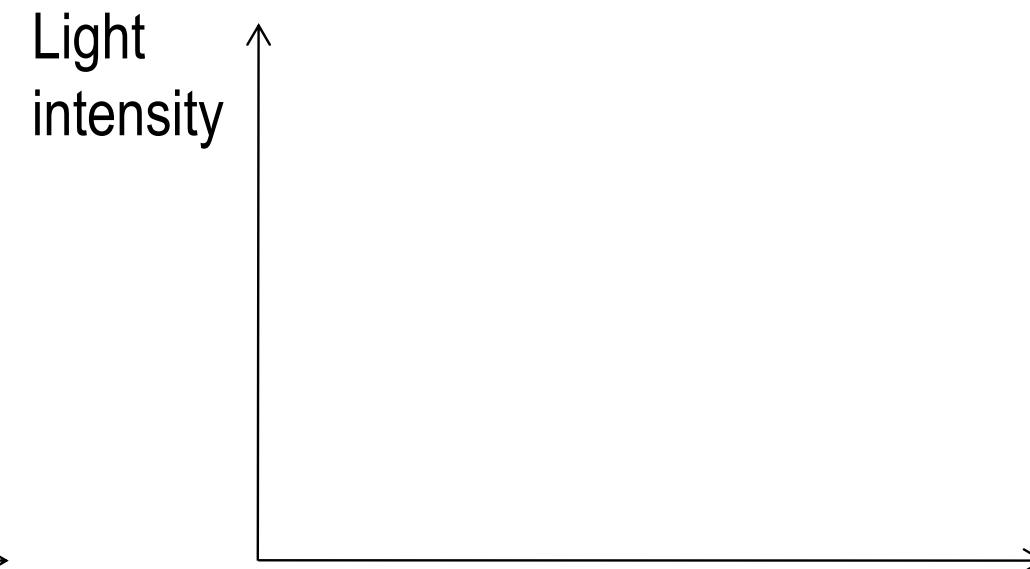
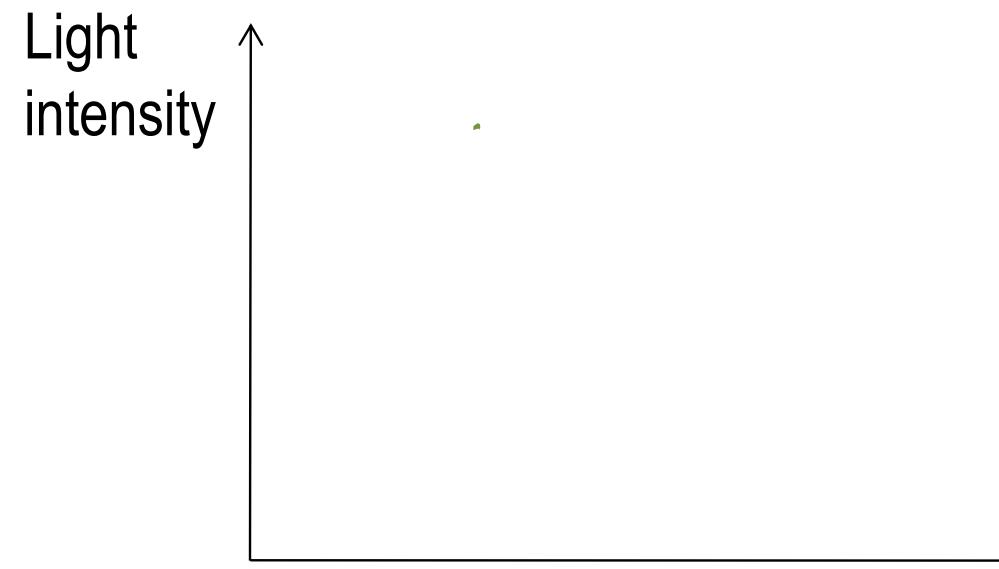
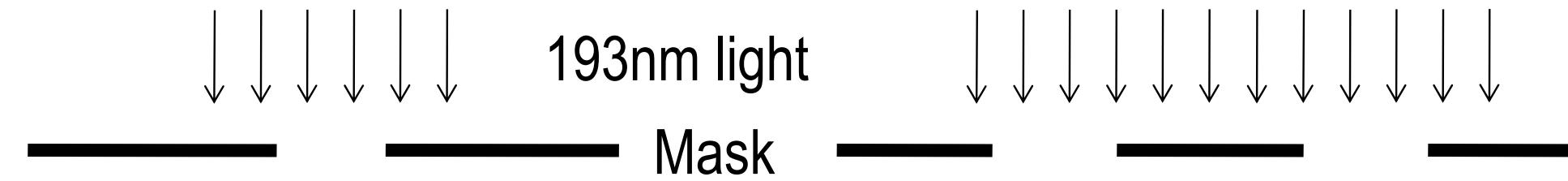


Lithography Scaling



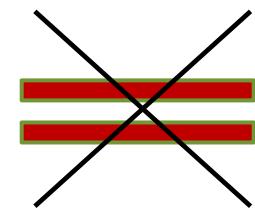
Sub-Wavelength Lithography

- Light projected through a gap

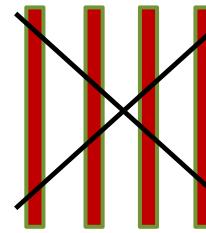
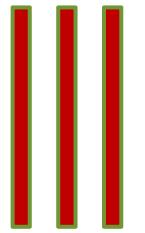


Lithography Implications

- Forbidden directions



- Forbidden pitches



- Optical proximity correction (OPC)



?



We Just Want a Square Contact...

- OPC vs. ILT

Optical Proximity Correction

**45 nm
node**

**without
OPC**



Inverse Lithography Technology

**14 nm
node**

**normal
ILT**



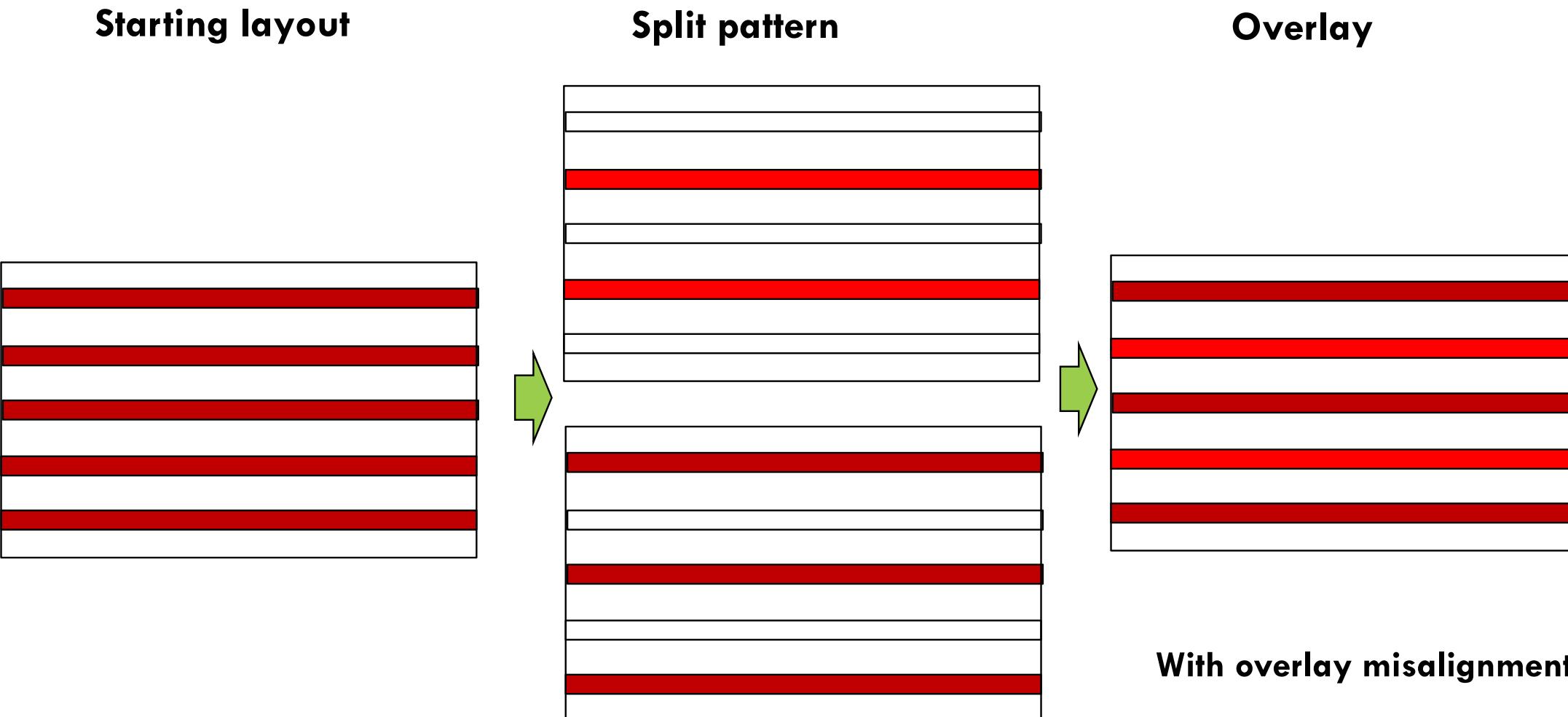
**7 nm
node**

**ideal
ILT**



Multiple Patterning

- Double patterning (pitch-split double exposure)



- “Layout coloring”
- 7nm process is quadruple patterned (w/o EUV)

Administrivia

- Midterm 1 scores released
 - Great job!
- Midterm 2 is in 3.5 weeks
 - Focus on material after midterm 1
 - RISC-V control, pipelining
 - CMOS logic
 - Logic delays, timing
 - Arithmetic

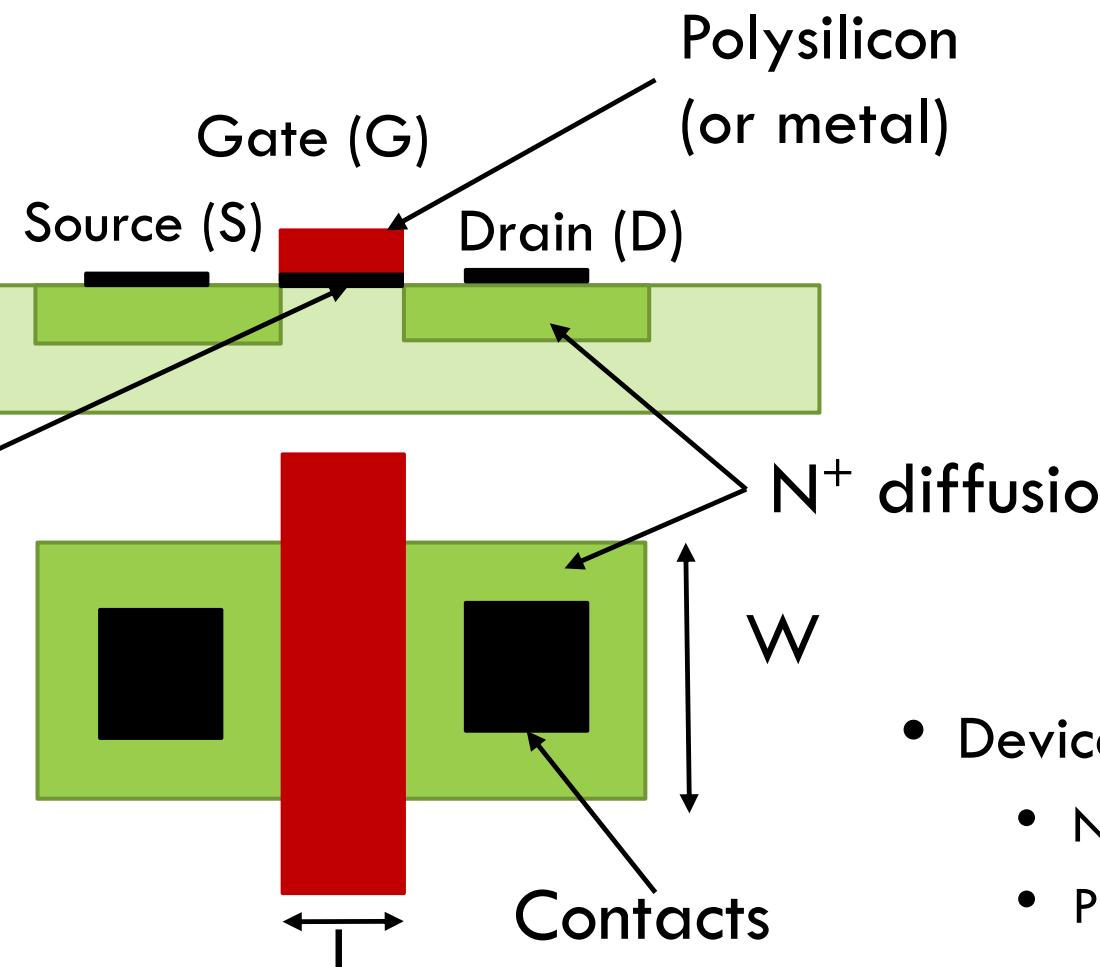
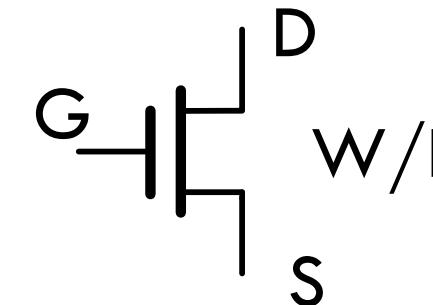


MOS Transistors

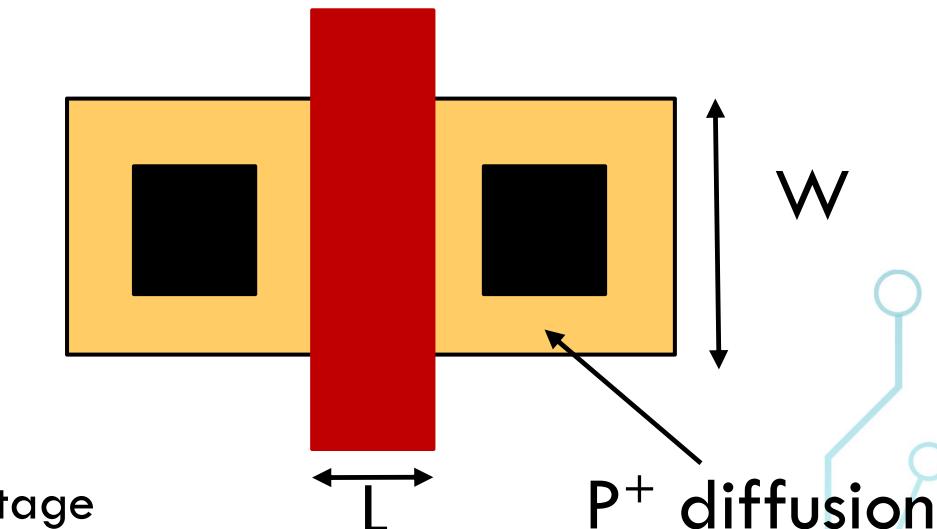
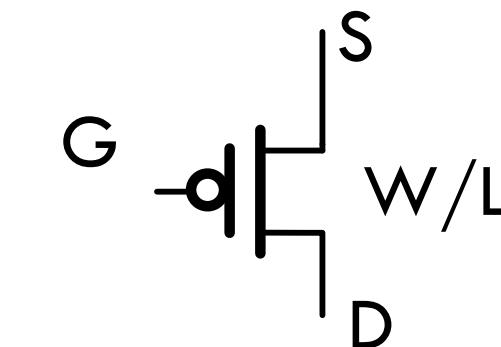
MOS Transistors

- Symbol

N-type
NMOS



P-type
PMOS

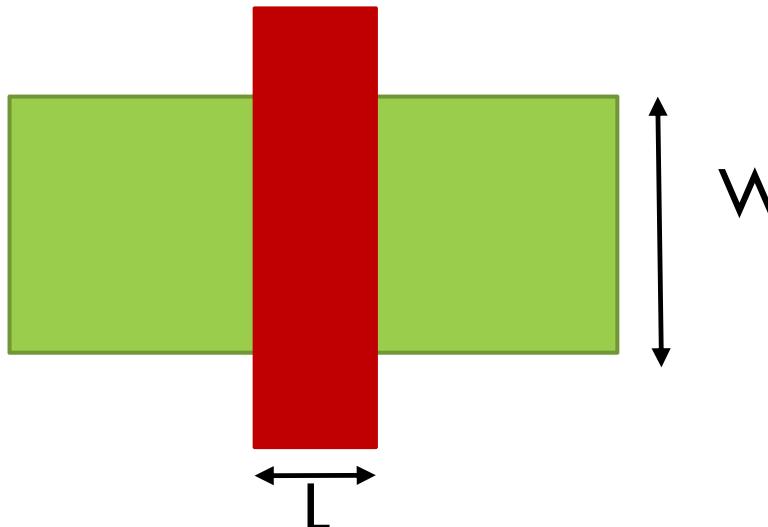
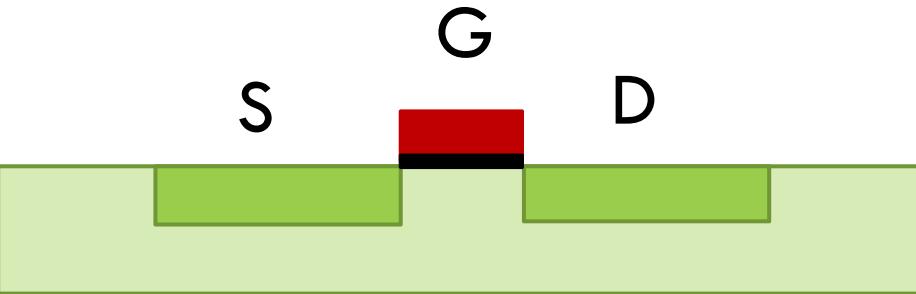
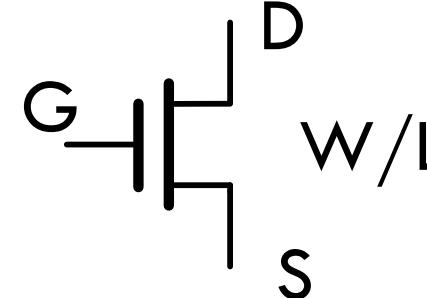


- Devices are symmetrical
 - NMOS: Drain is at higher voltage
 - PMOS: Source is at higher voltage

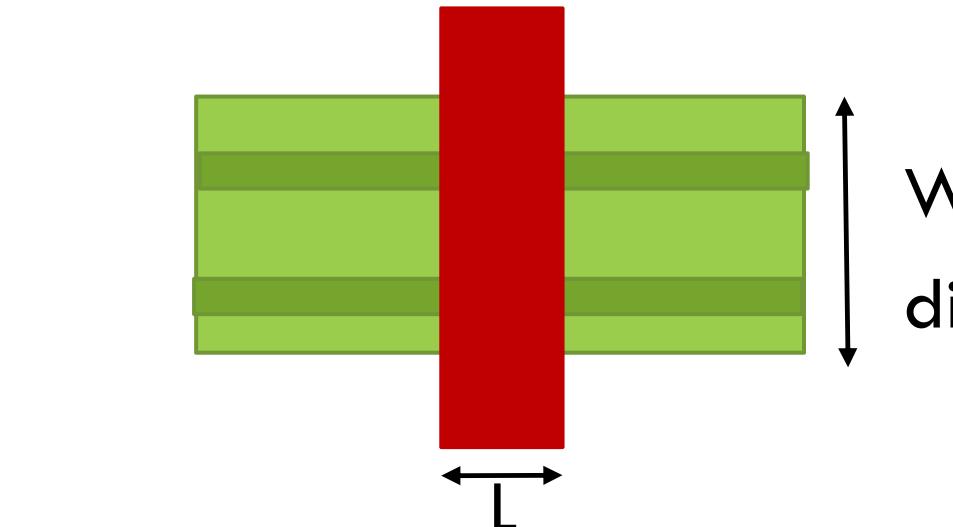
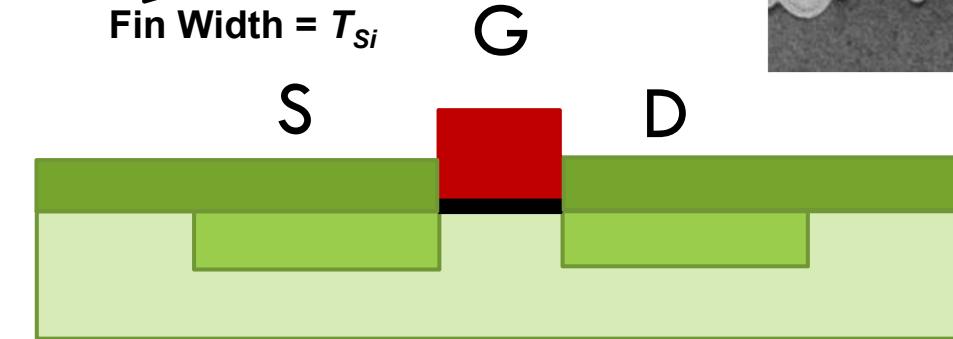
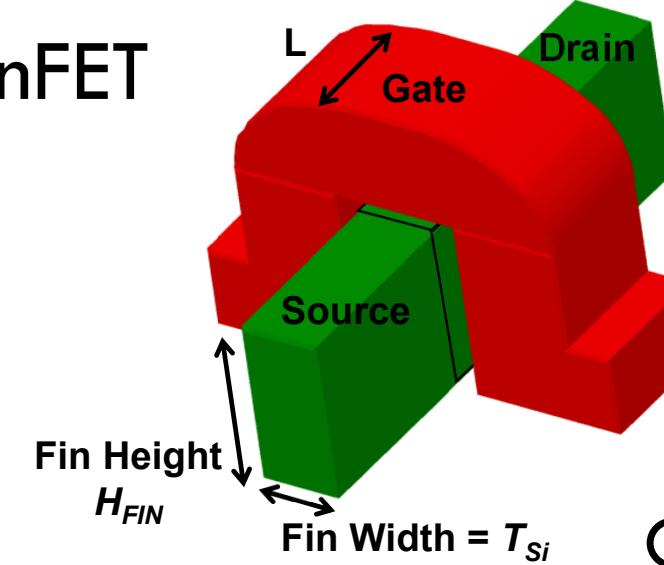
Different Kinds of MOS Transistors

- Planar bulk CMOS

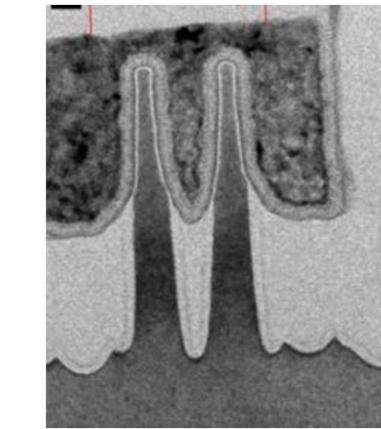
N-type
NMOS



- FinFET

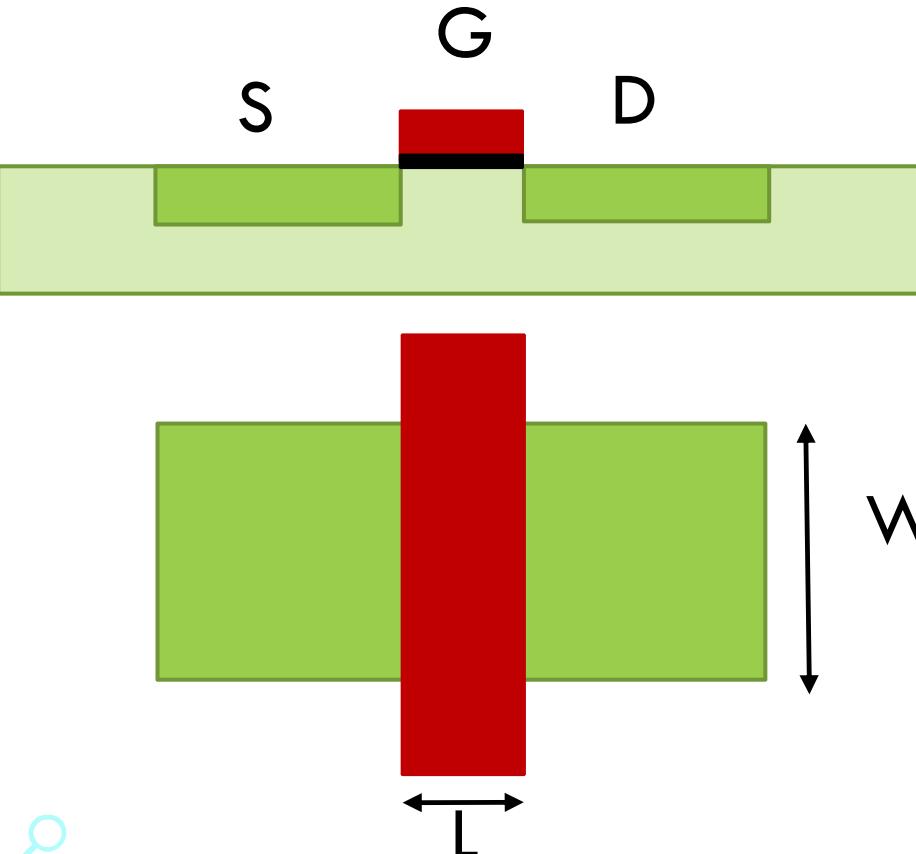


Intel 10nm
IEDM 2017

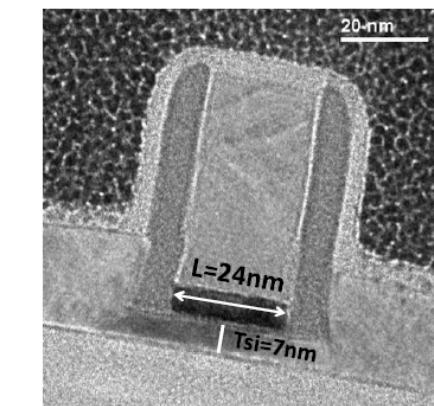
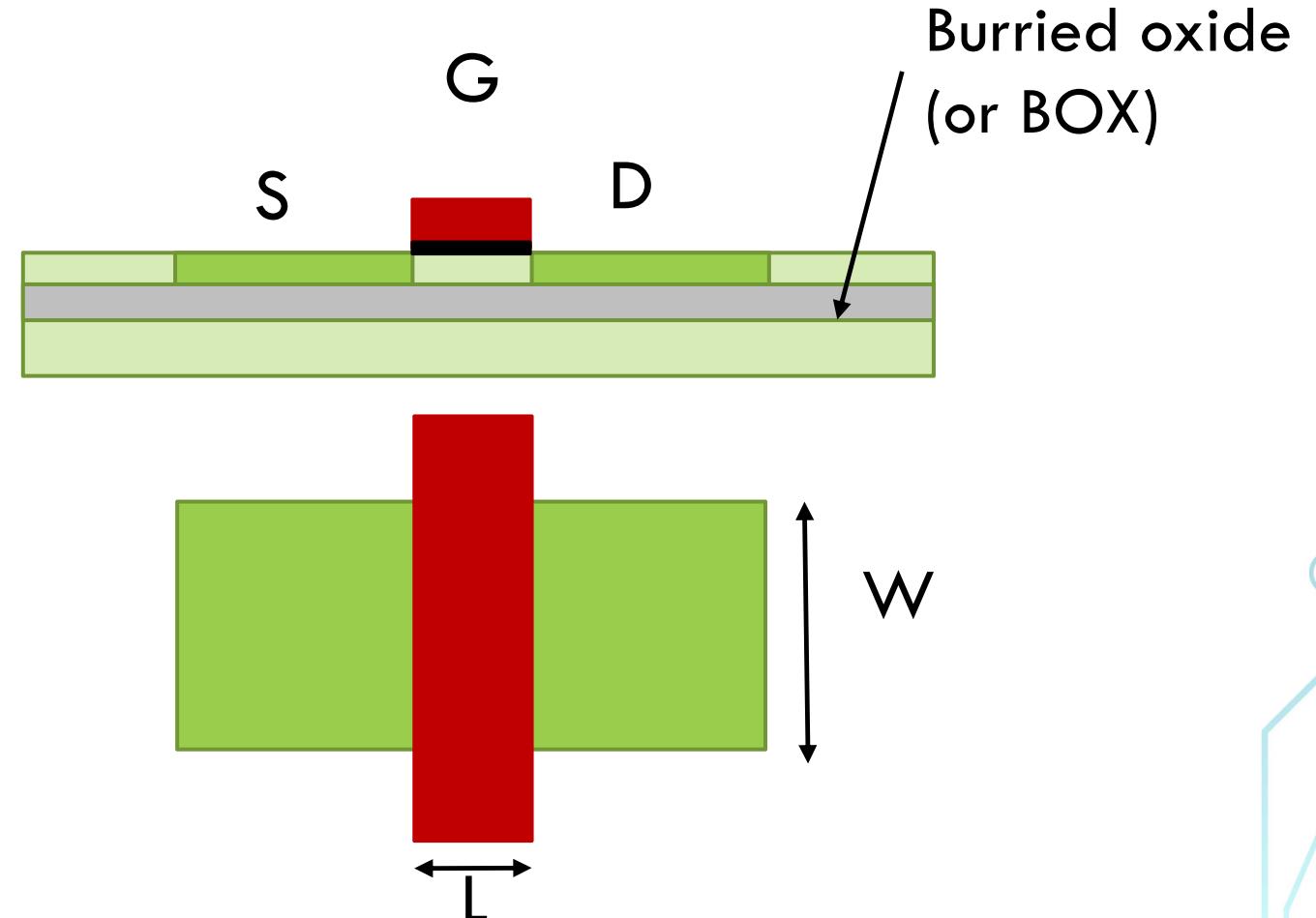


Different Kinds of MOS Transistors

- Planar bulk CMOS
N-type
NMOS
-



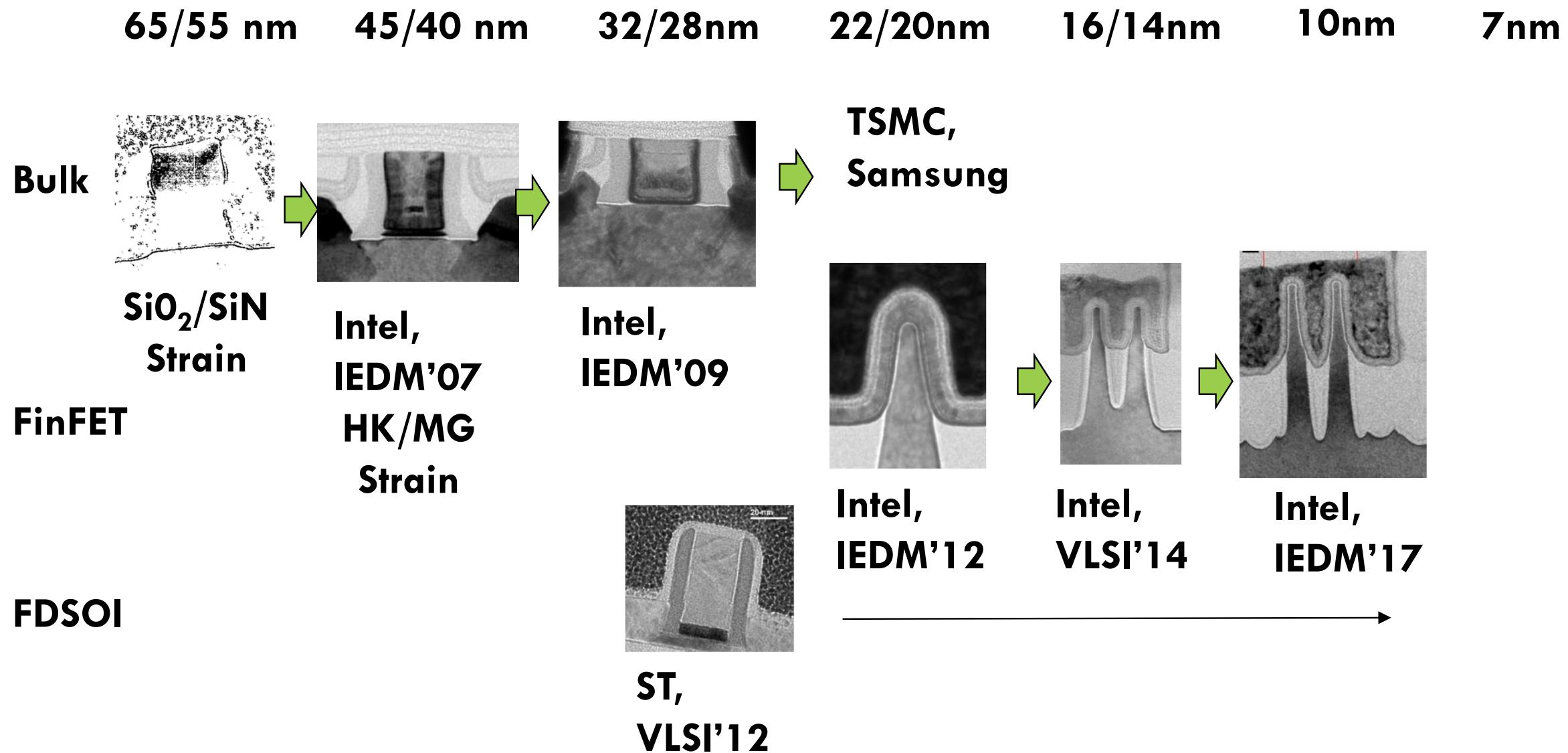
- Fully-depleted SOI



ST 28nm
VLSI 2012

Transistors are Changing

- From bulk to finFET and FDSOI

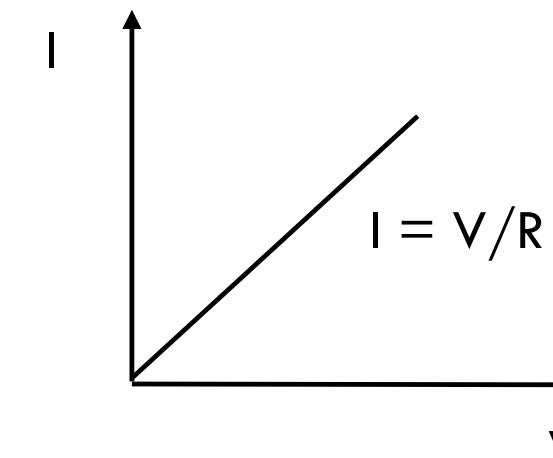
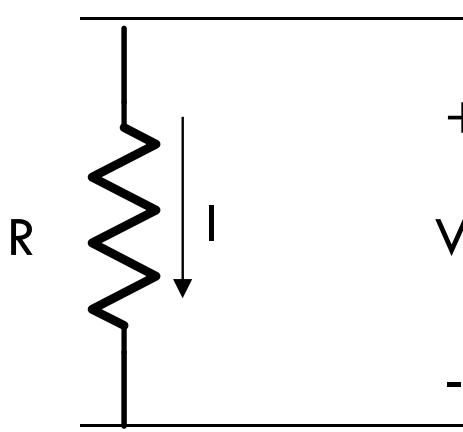


Transistor Dimensions are Quantized

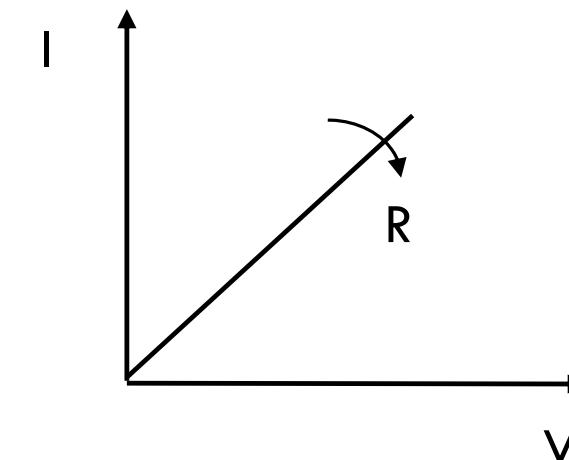
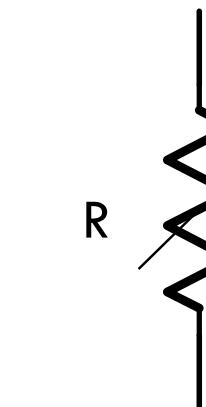
- FinFET widths are discrete ($W = kW_{\text{unit}}$)
- Lengths are quantized because of lithography
 - Also are quantized lower metal layers, contacts...

Ohm's Law

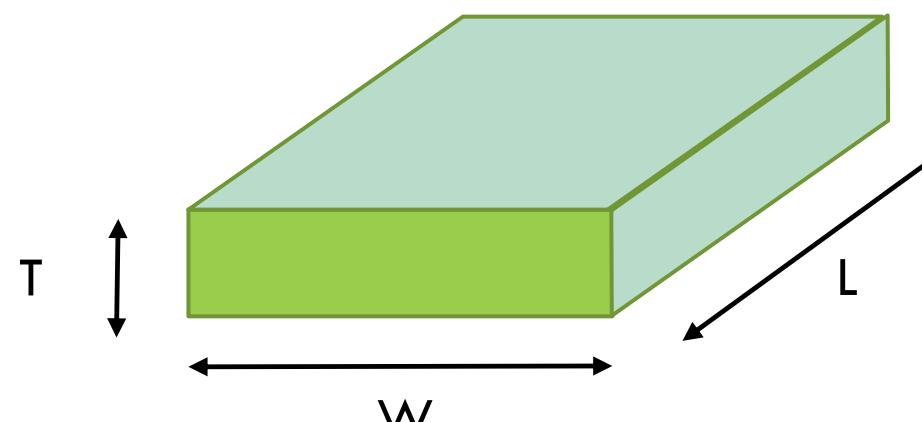
- Resistors



- Variable resistors



- Physical resistors

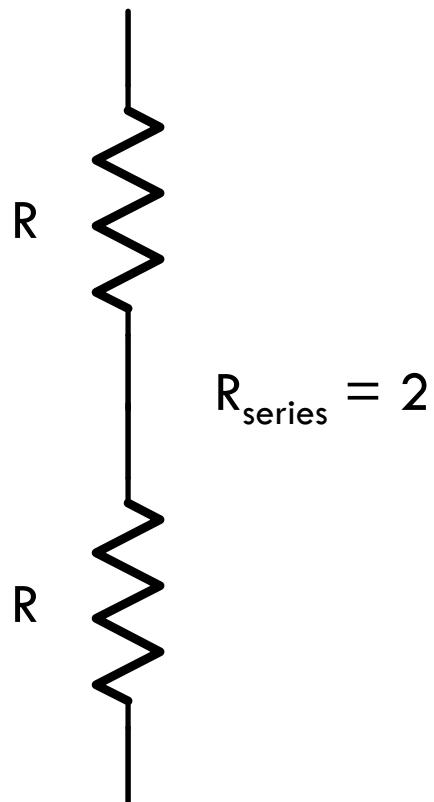


$$R = \rho \frac{L}{TW}$$

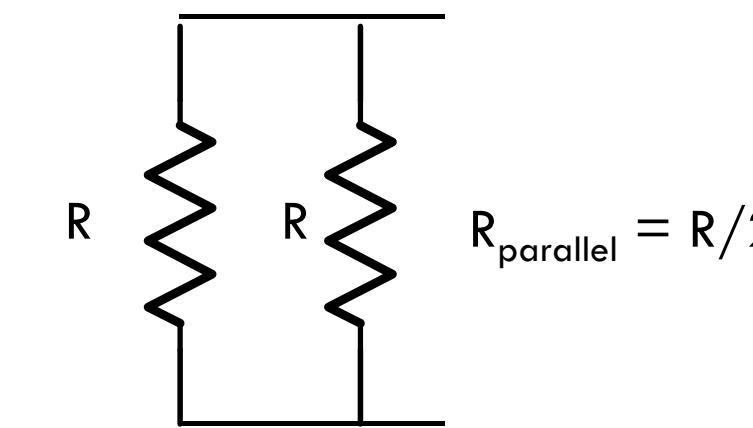
- In a planar process, designer controls W and L

Series and Parallel

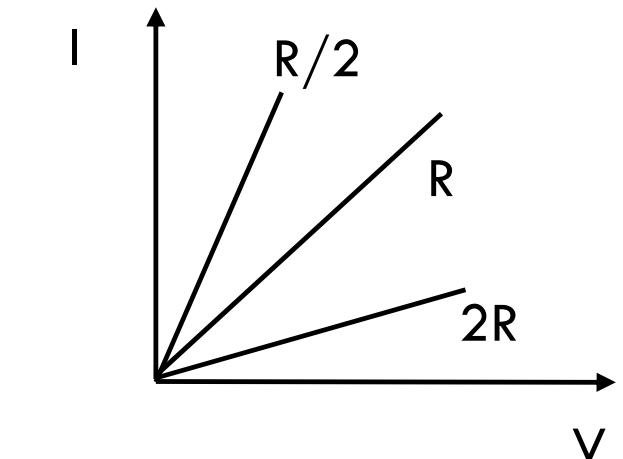
- With two identical resistors, R



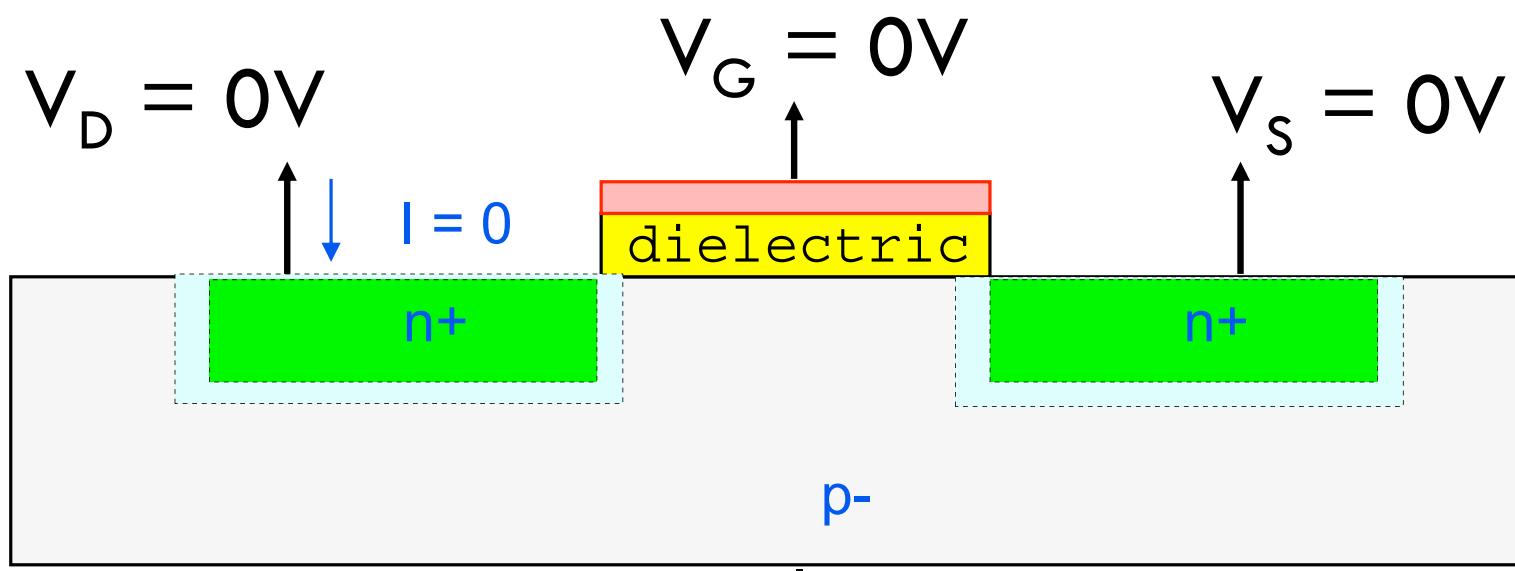
Equivalent to doubling length



Equivalent to doubling width

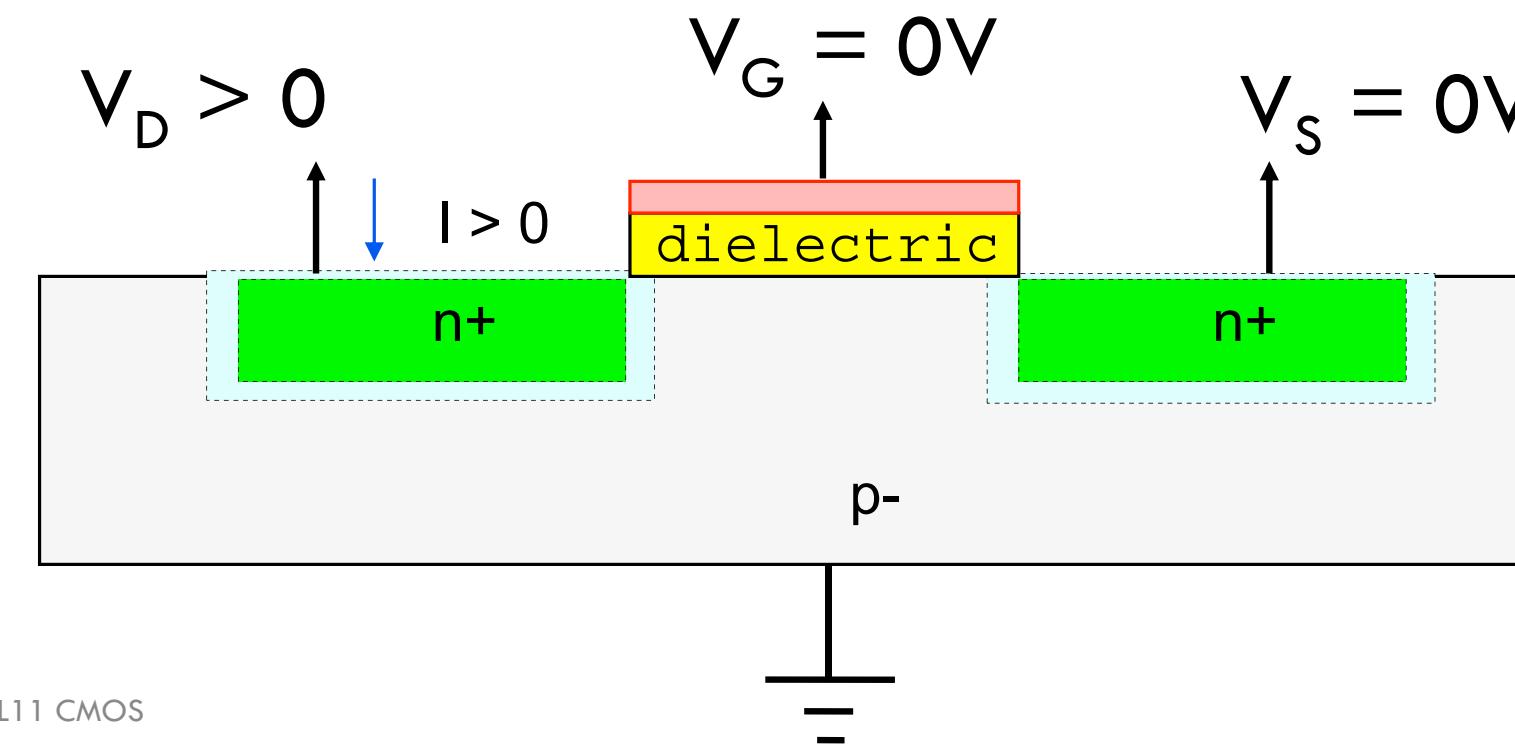


An n-Channel MOS Transistor



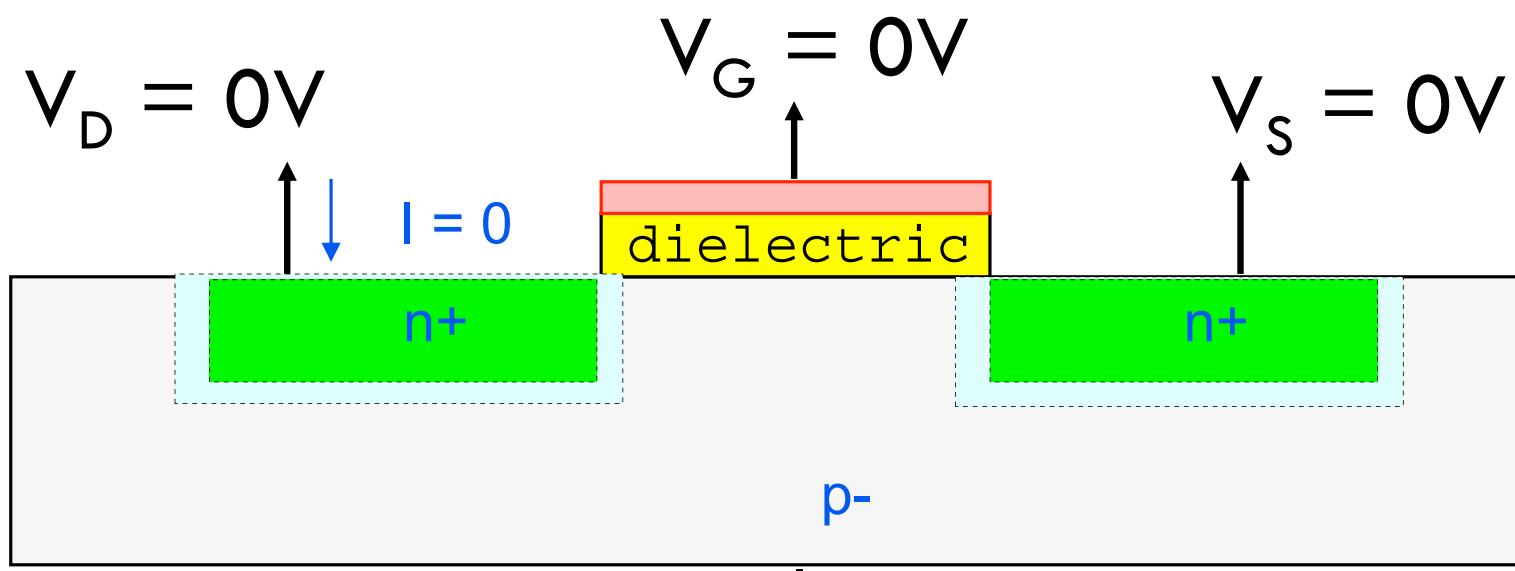
Polysilicon gate,
dielectric, and substrate form a
capacitor.

When $V_{GS} < V_{Th}$ transistor is off

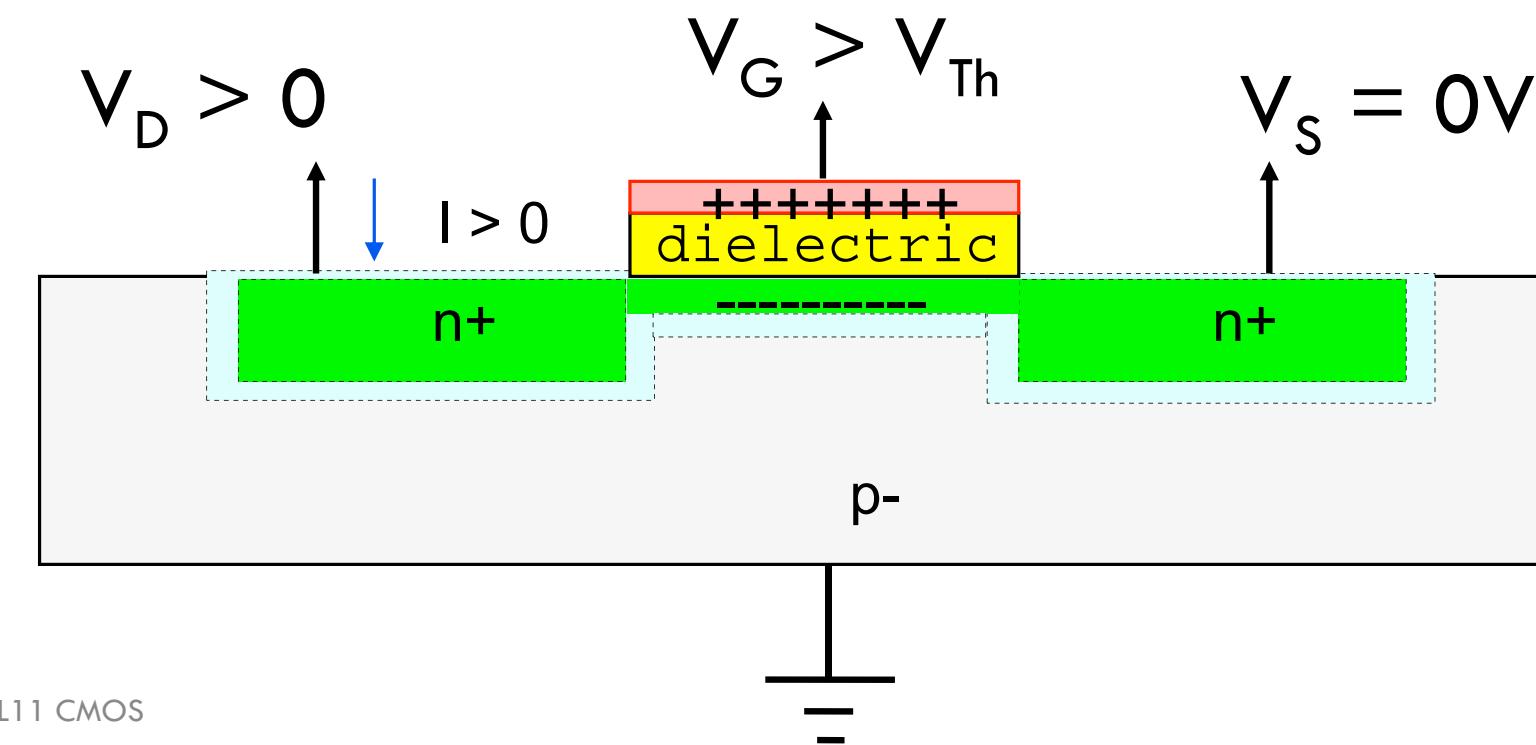


$V_{DS} > 0$, transistor leaks
 $I_{DS} \sim nA$

An n-Channel MOS Transistor



When $V_{GS} < V_{Th}$ transistor is off

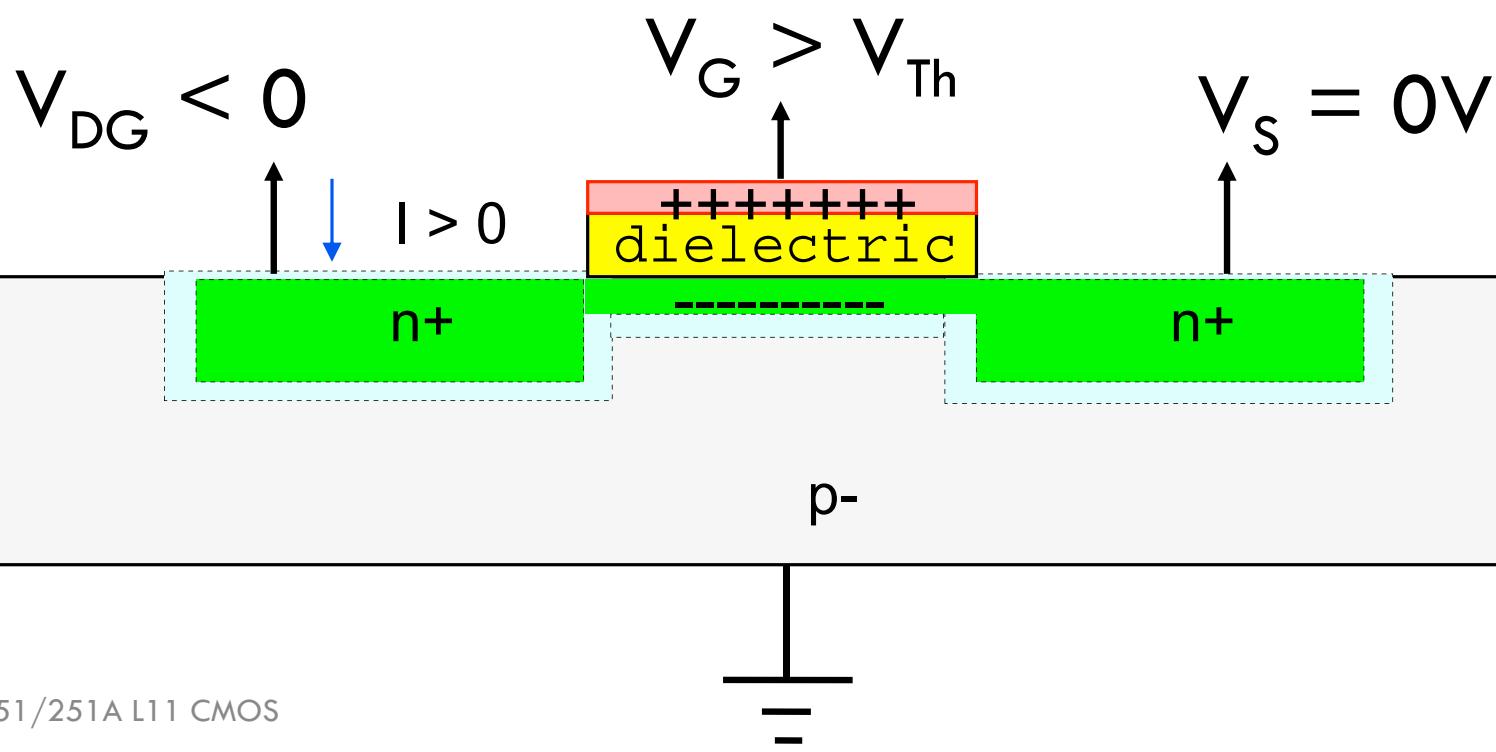
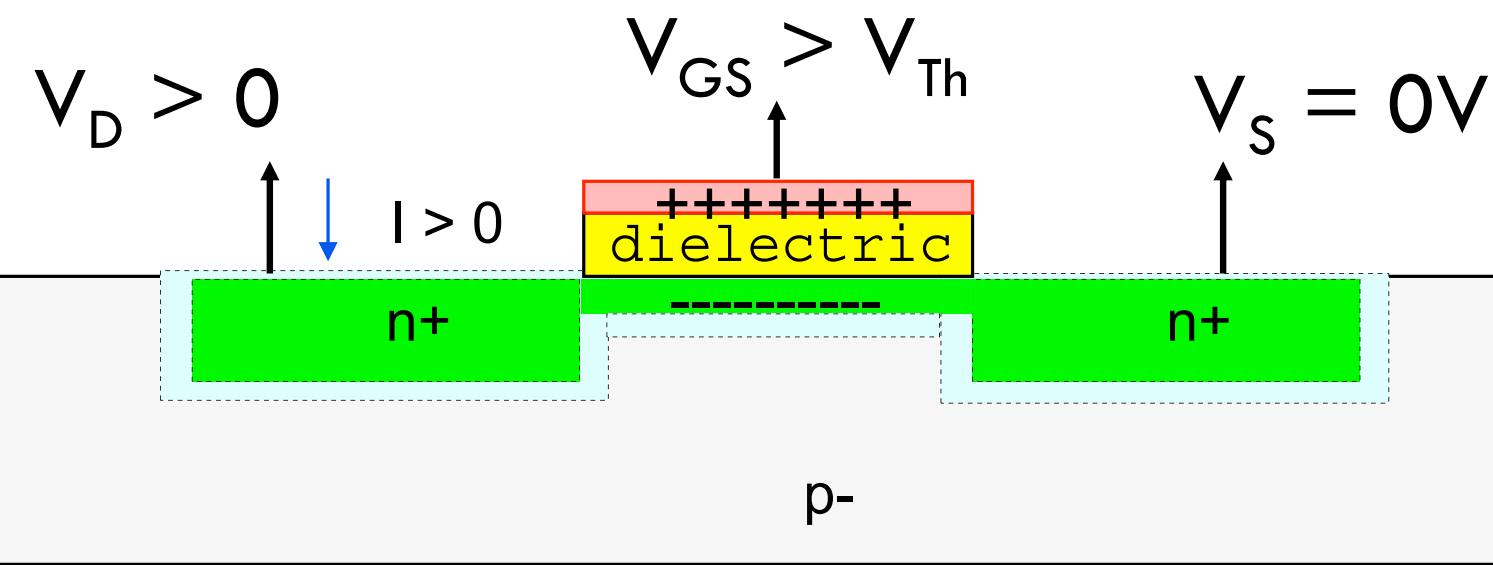


$V_G > V_{Th}$, small region near the surface turns from p-type to n-type.

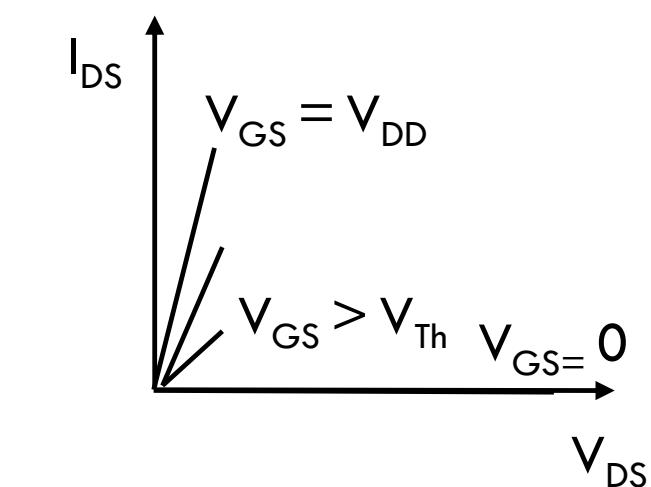
nFet is on.

Current is proportional to V_{DS}

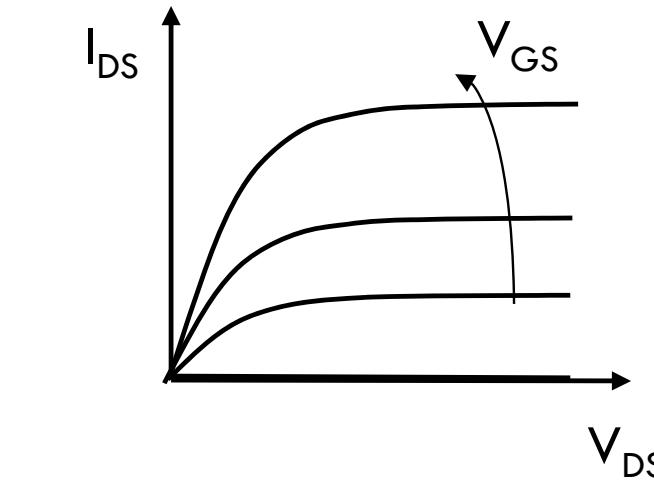
An n-Channel MOS Transistor



V_{DS} and V_{GS} change I_{DS}

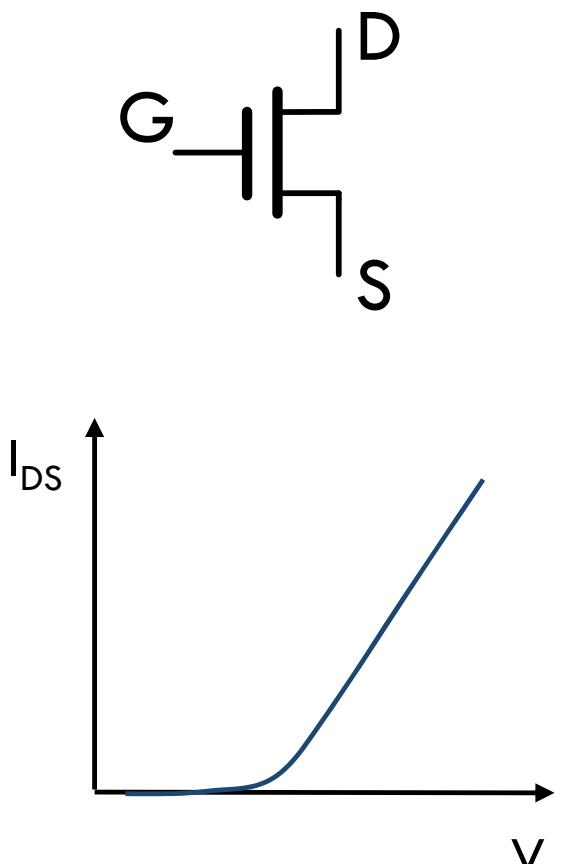


$V_{GD} < V_{Th}$ transistor saturates
($V_{DS} > V_{GS} - V_{Th}$)



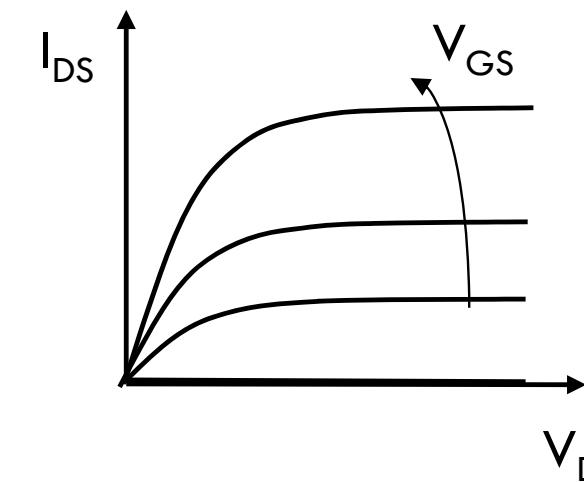
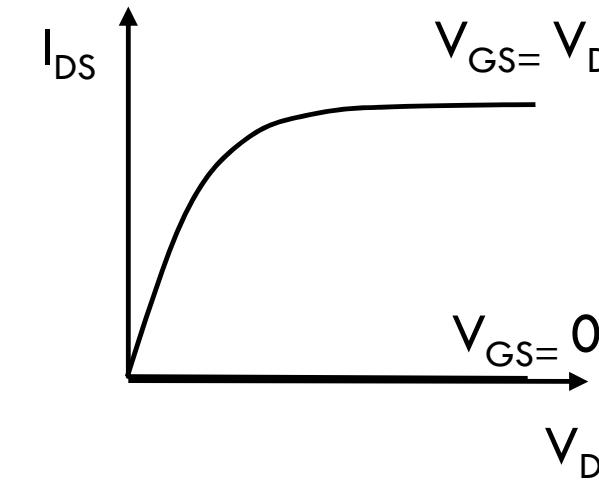
MOS Transistors

- NMOS Transistor I-V characteristics

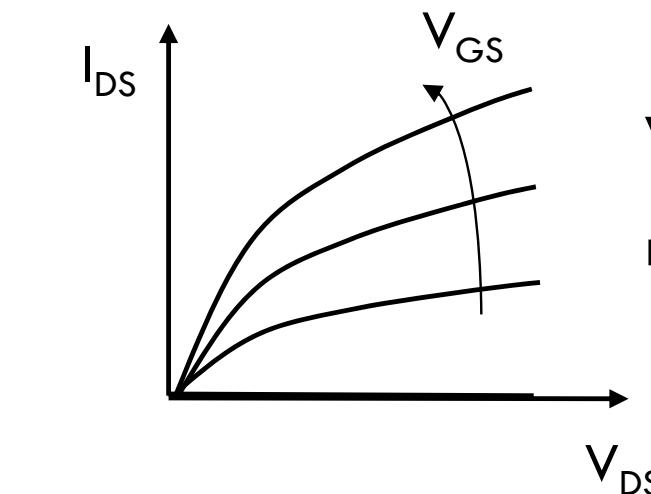
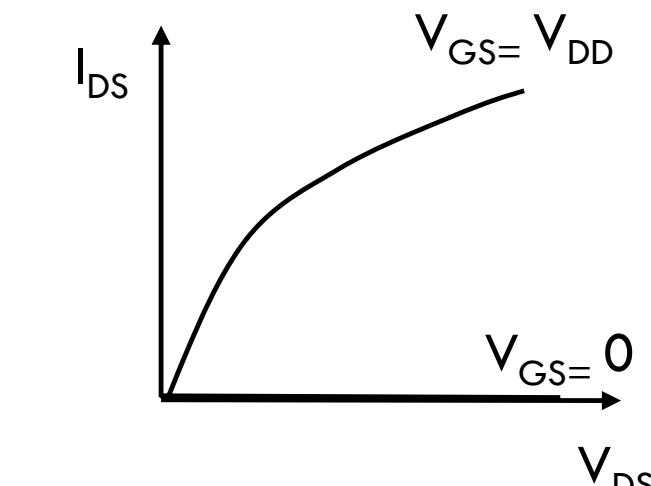


Nearly linear
 $I_{DS} \sim K(V_{GS} - V_{Th})$

Old transistor



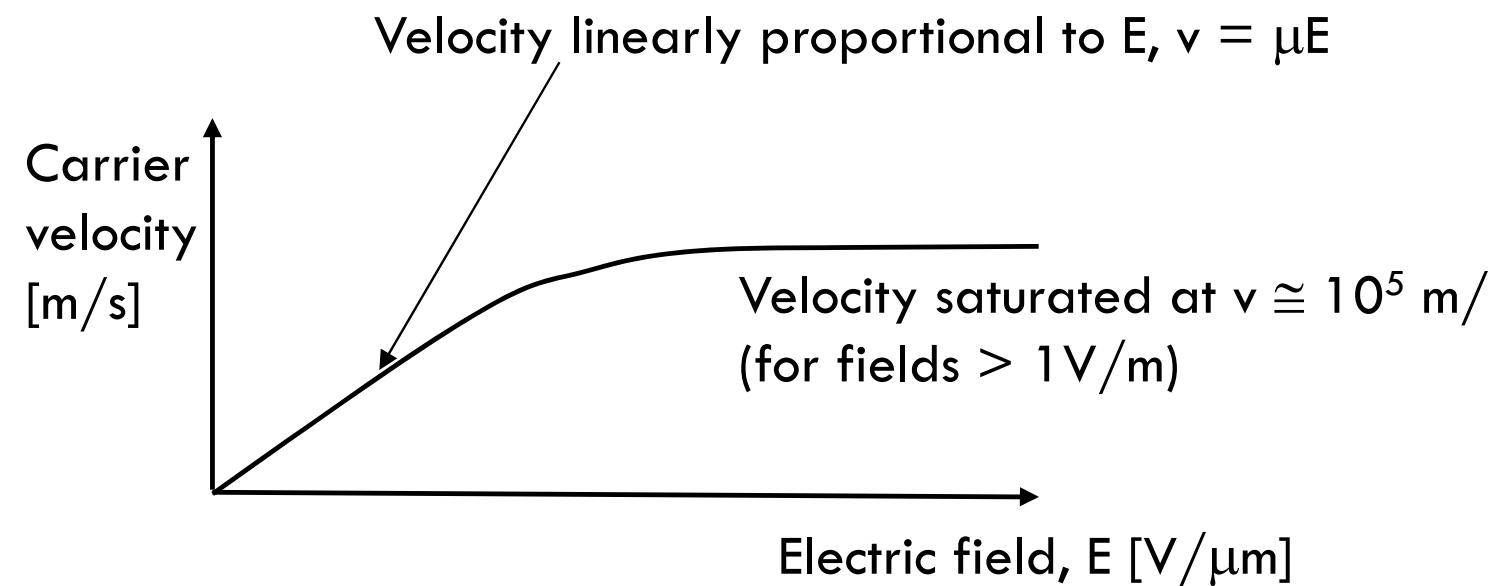
~7nm transistor



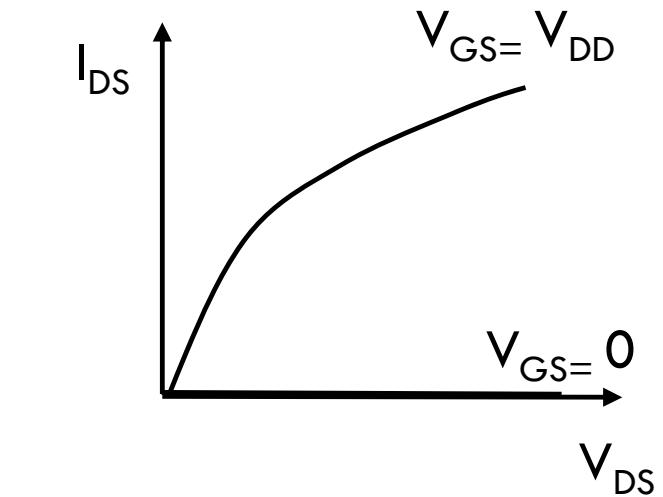
Variable
resistor!

Velocity Saturation

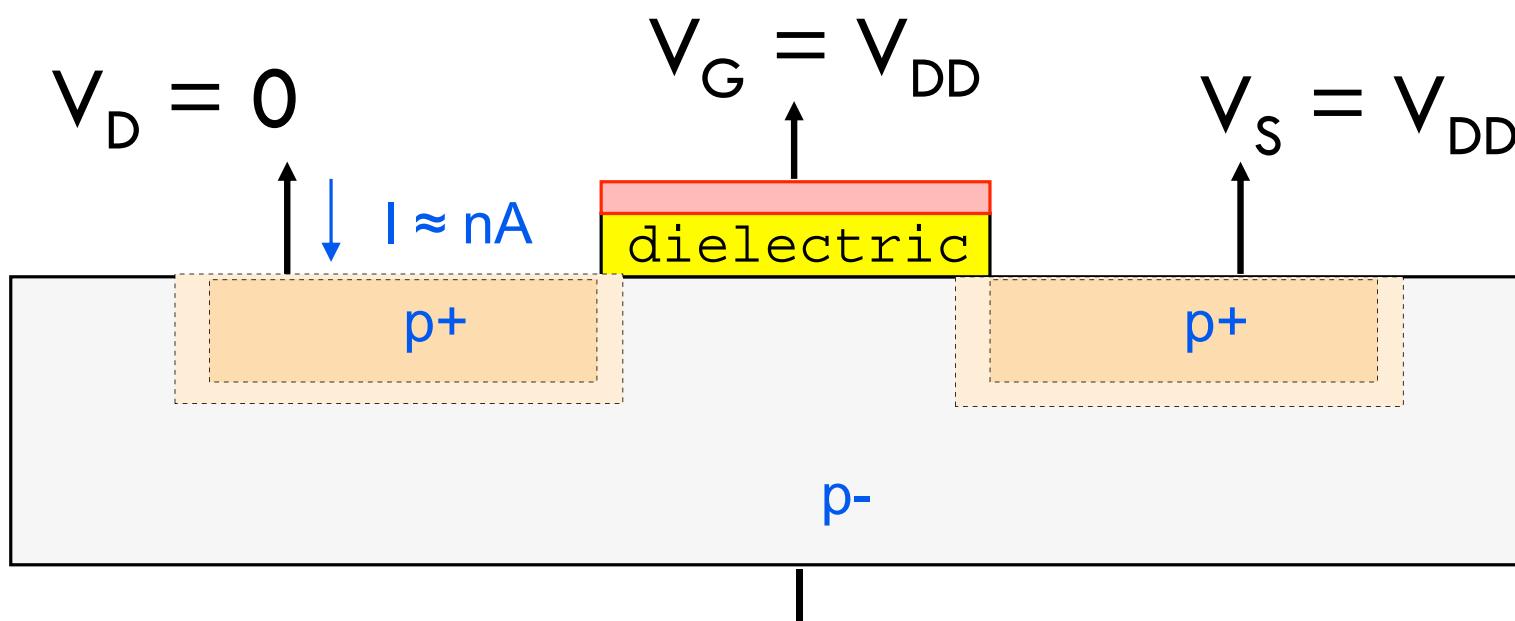
- Carrier velocity in the channel saturates



- All submicron transistors are velocity saturated
- Other effects (drain-induced barrier lowering) cause I_{DS} to increase in saturation

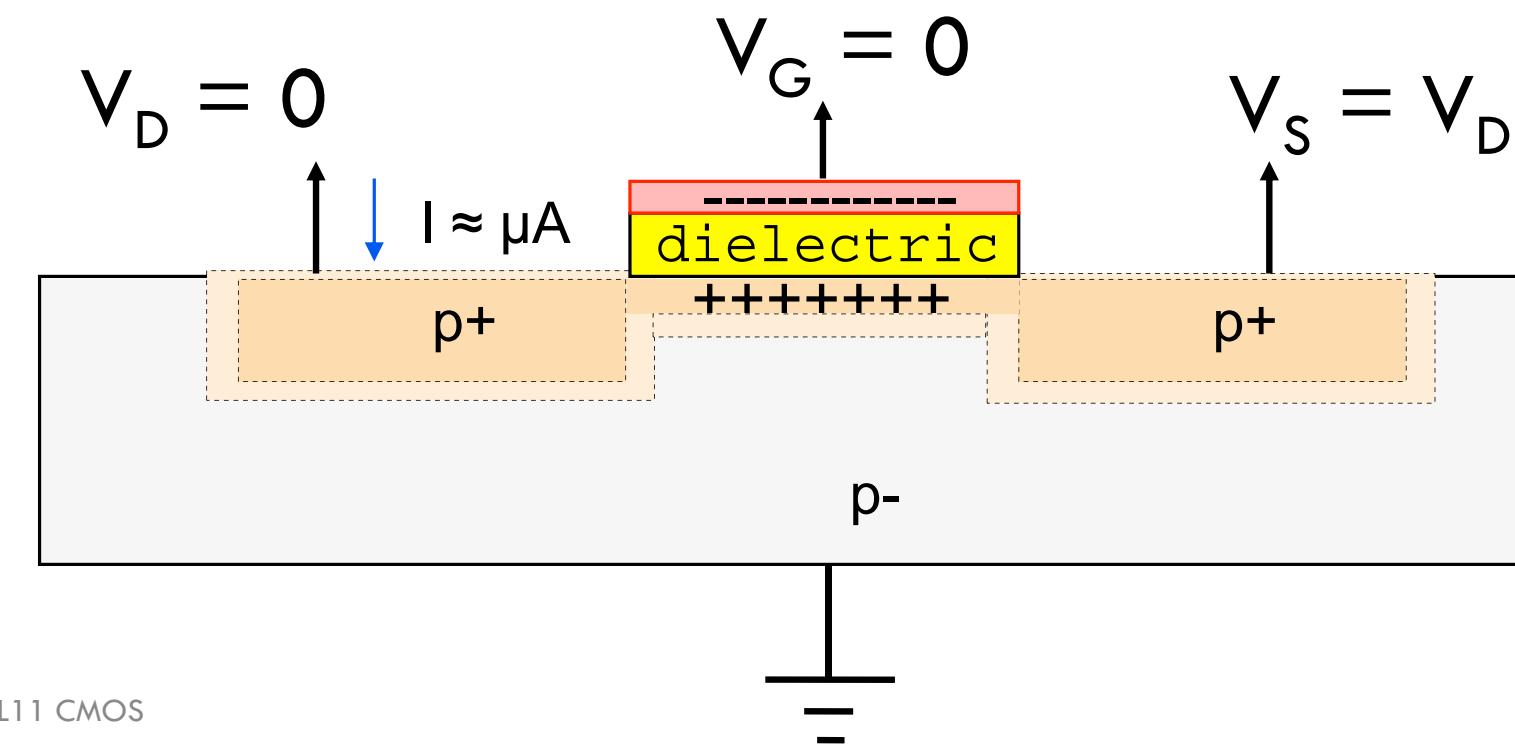


A p-Channel MOS Transistor



Polysilicon gate,
dielectric, and substrate
form a capacitor.

nFet is off
(I is “leakage”)



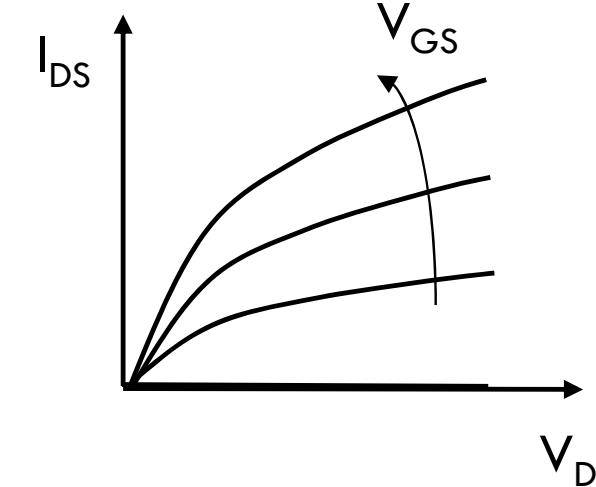
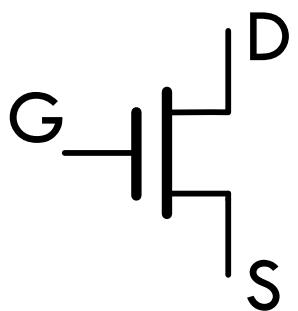
$V_{GS} = -V_{DD}$, small region
near the surface turns
from n-type to p-type.

nFet is on.

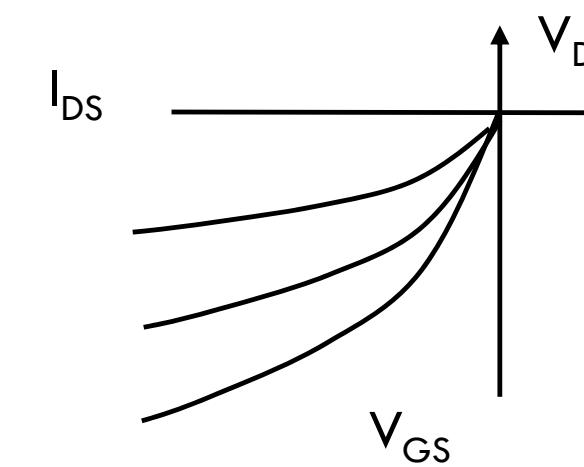
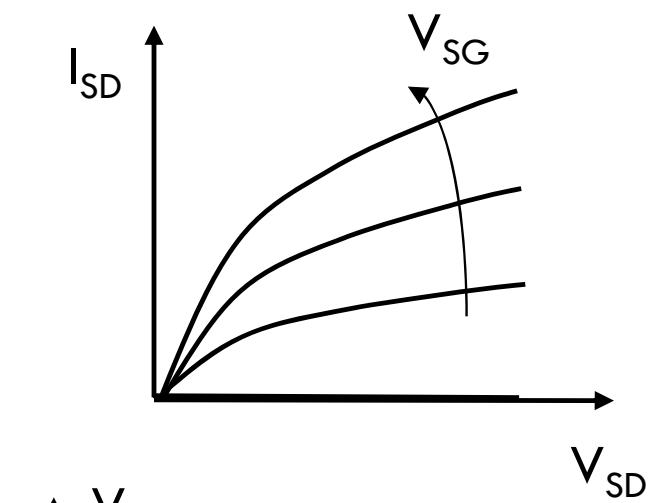
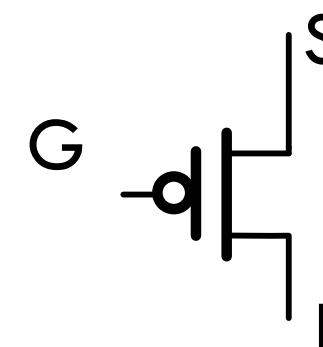
MOS Transistors

- PMOS Transistor I-V characteristics

NMOS



PMOS



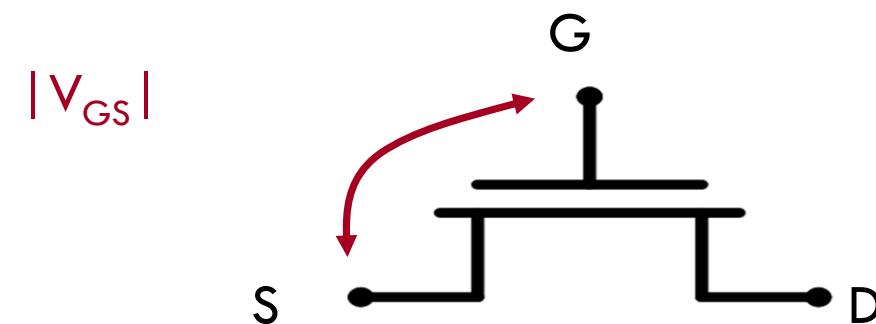


MOS Transistor as a Switch

MOS Transistor as a Resistive Switch

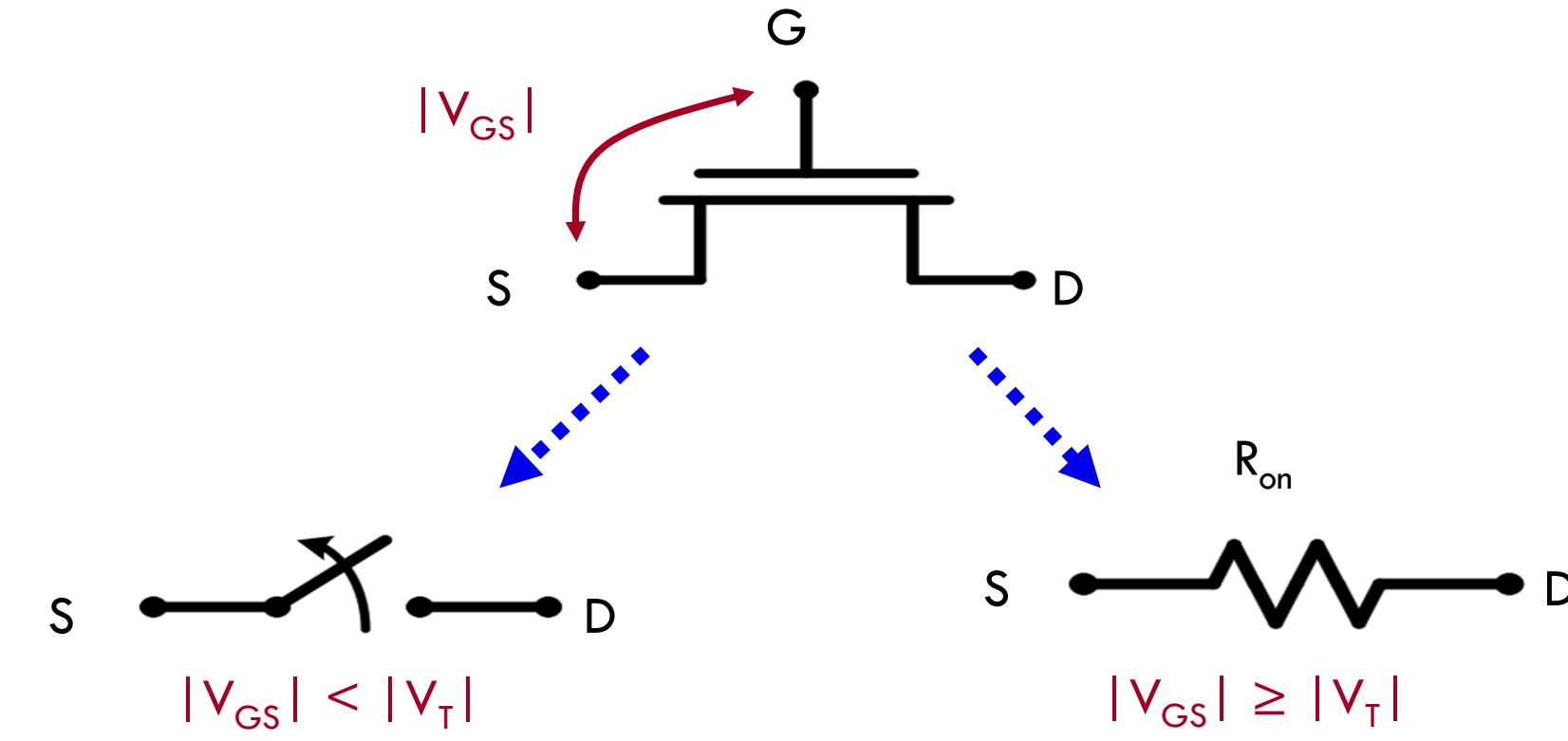
MOS Transistor

A Switch!

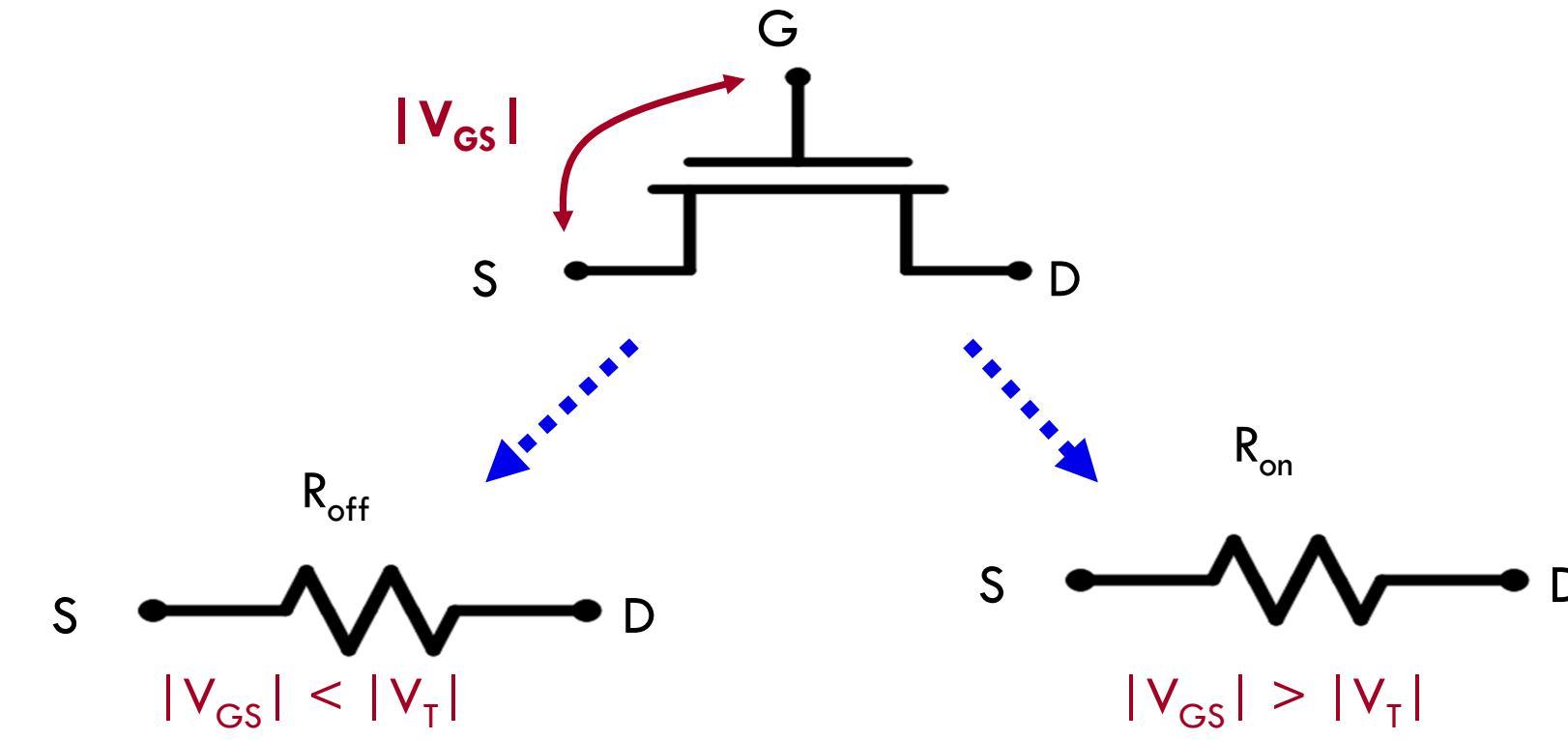


- V_{GS} controls the switch
 - (it also charges the channel capacitor)

ON/OFF Switch Model of MOS Transistor



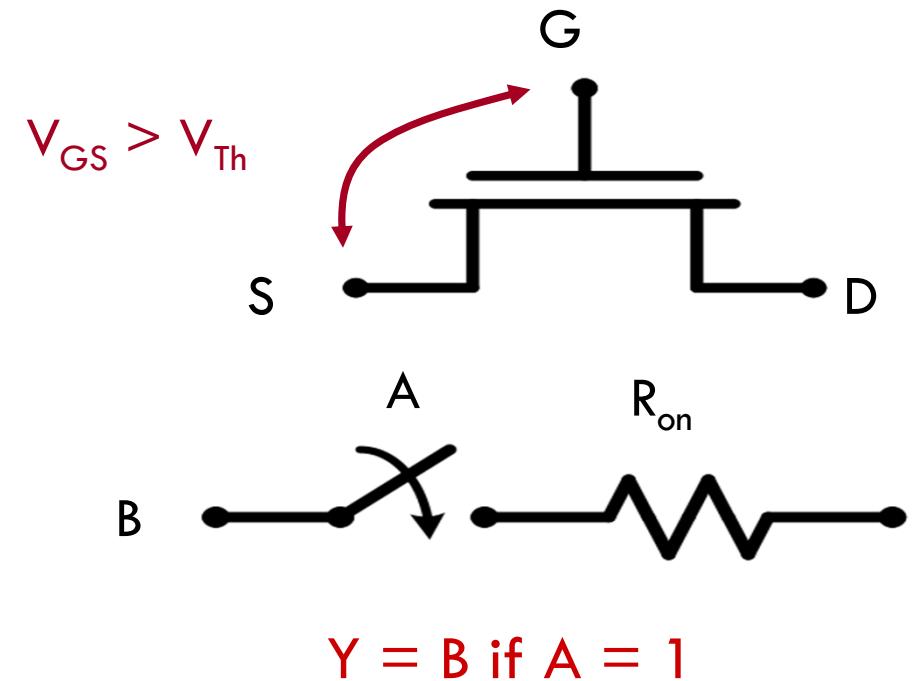
A More Realistic Model



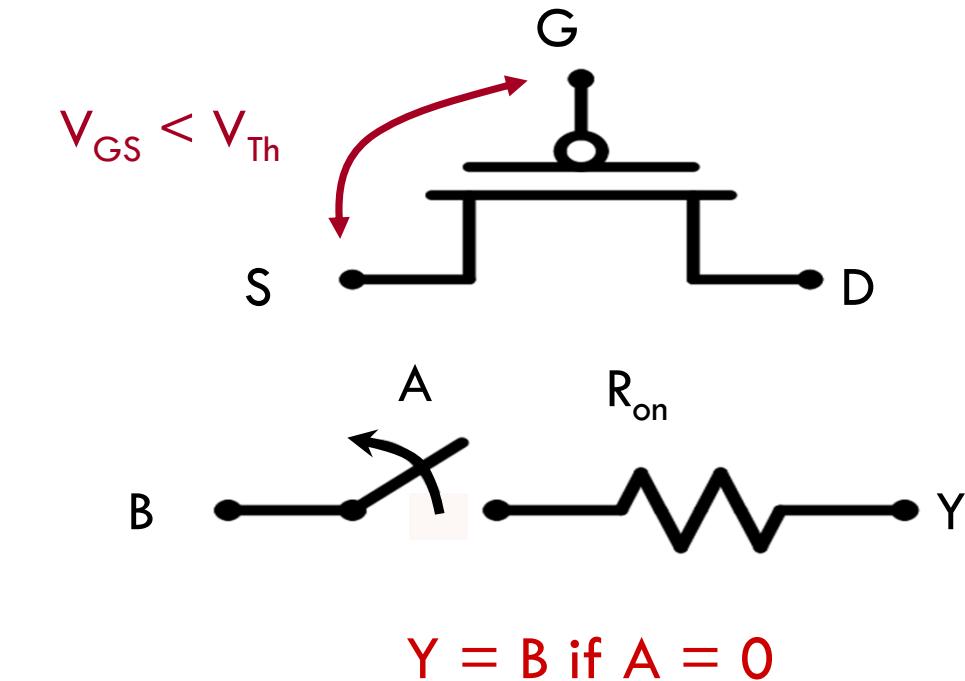
• It is a dimmer!

A Logic Perspective

NMOS Transistor

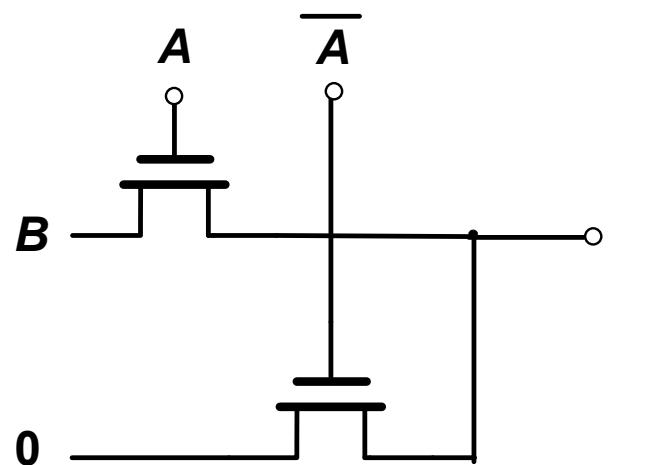


PMOS Transistor



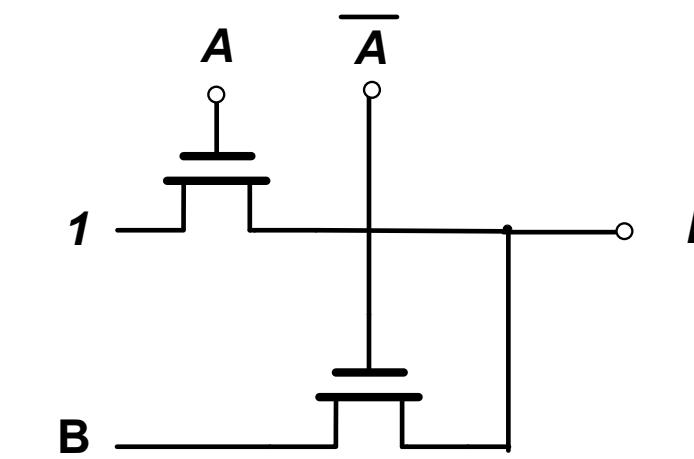
AND and OR

- AND



$$F = AB$$
$$(F = AB + \bar{A} \cdot 0)$$

- OR

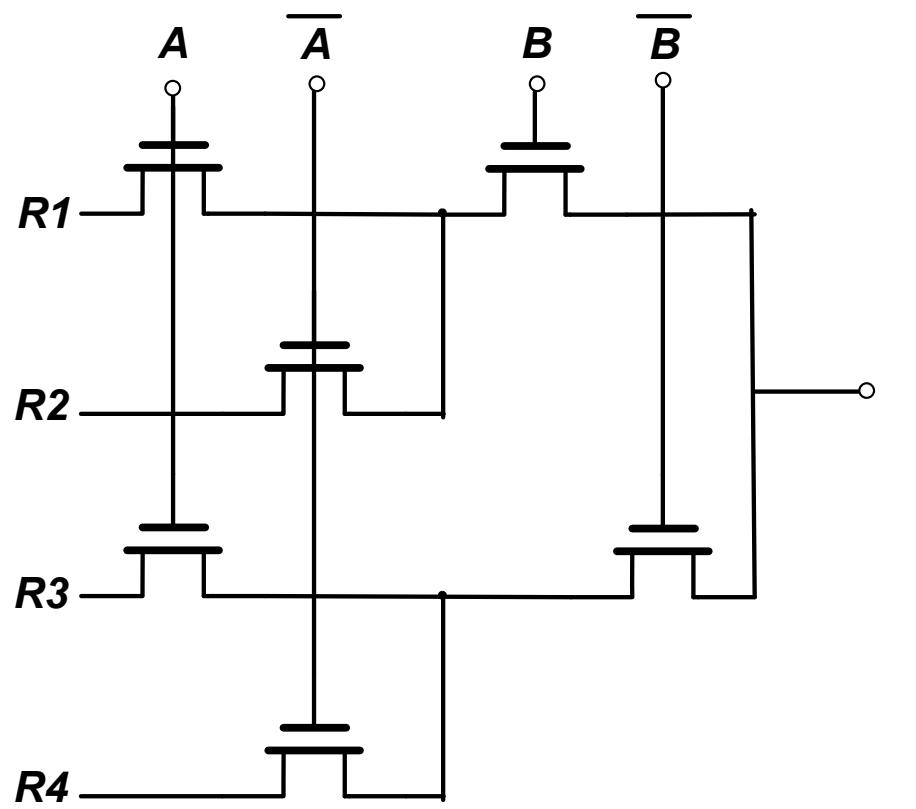


$$F = A + B$$
$$(F = A \cdot 1 + \bar{A}B)$$

- Keep in mind – single NMOS/PMOS transistors are imperfect switches!
 - Turns off when $|V_{GS}| = |V_{Th}|$

Peer Instruction

- Switch logic
- Which combination of inputs implements $F = AB$?



	$R1$	$R2$	$R3$	$R4$
a)	1	X	X	X
b)	0	X	X	X
c)	1	0	0	0
d)	1	1	1	0
e)	1	1	1	1

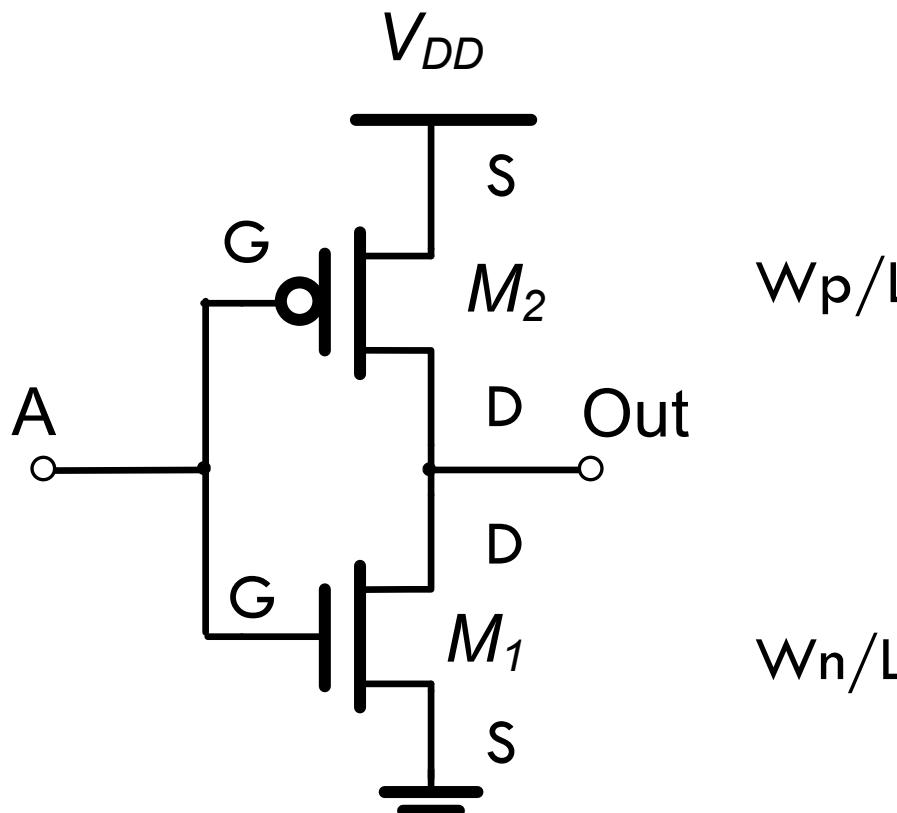


CMOS Inverter

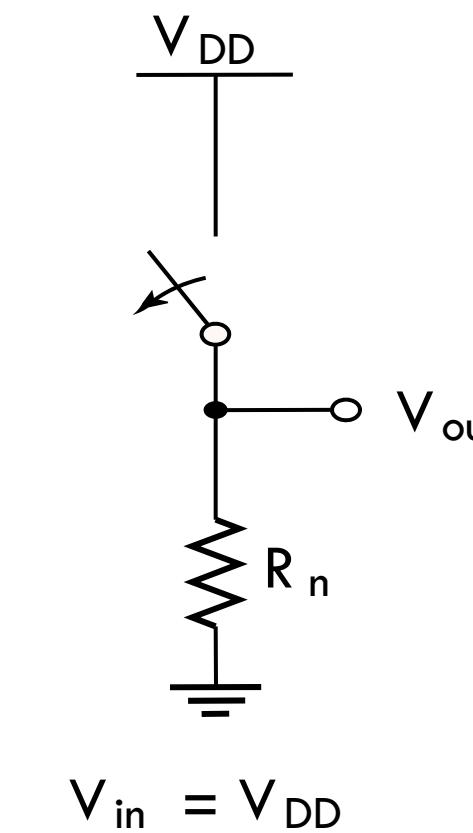
CMOS Inverter

- Simple DC behavior

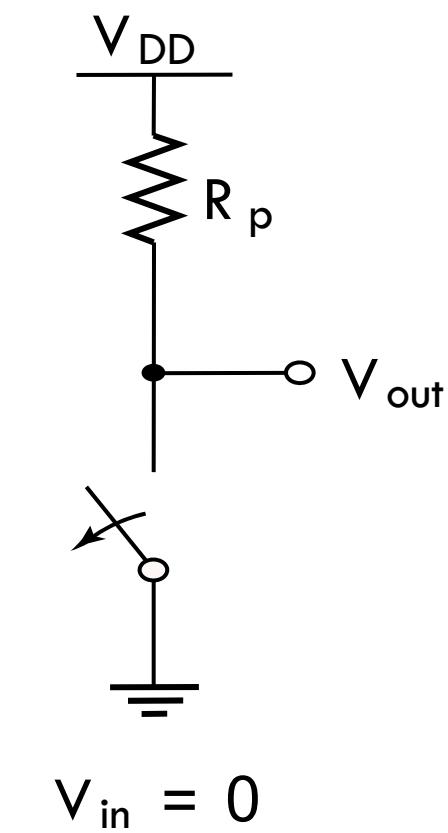
- Schematic



- Switch model



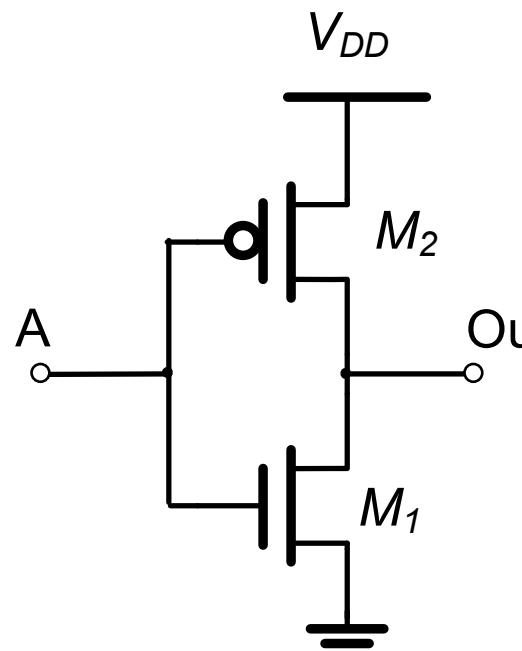
$$V_{in} = V_{DD}$$



$$V_{in} = 0$$

$$\begin{aligned}V_{OL} &= 0 \\V_{OH} &= V_{DD}\end{aligned}$$

Voltage Transfer Characteristic (VTC)



$$V_A = V_{GS,n} = V_{DD} - V_{SG,p}$$

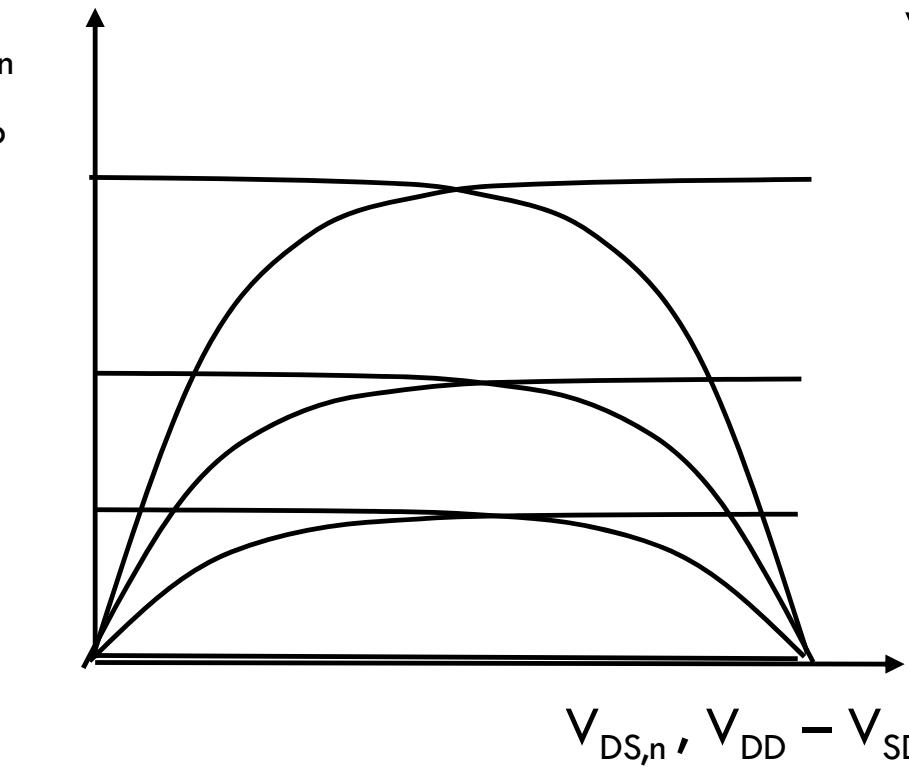
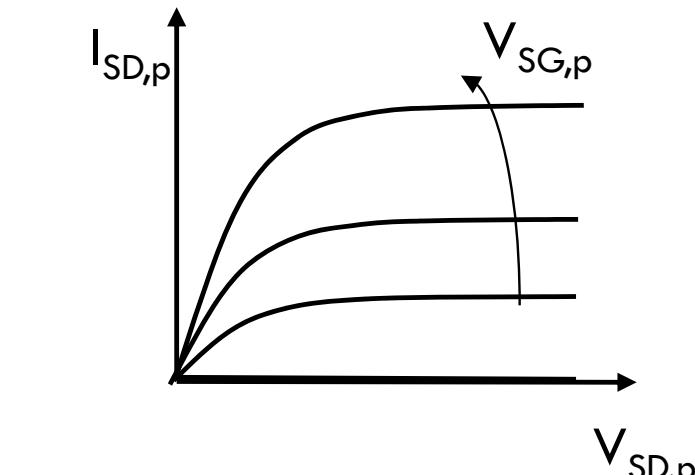
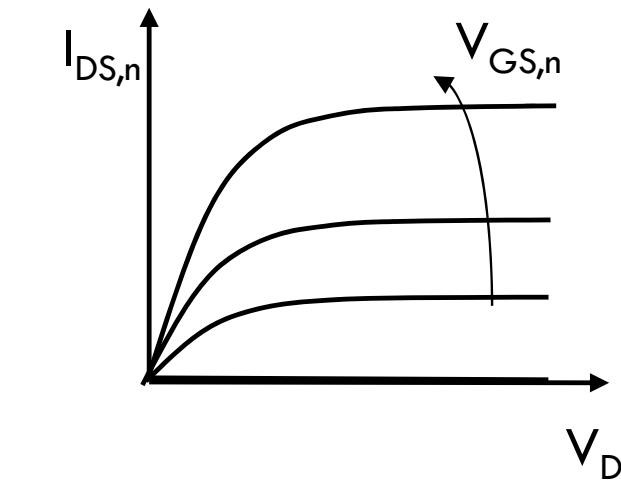
$$I_{DS,n} = I_{SD,p}$$

$$V_{Out} = V_{DS,n} = V_{DD} - V_{SD,p}$$

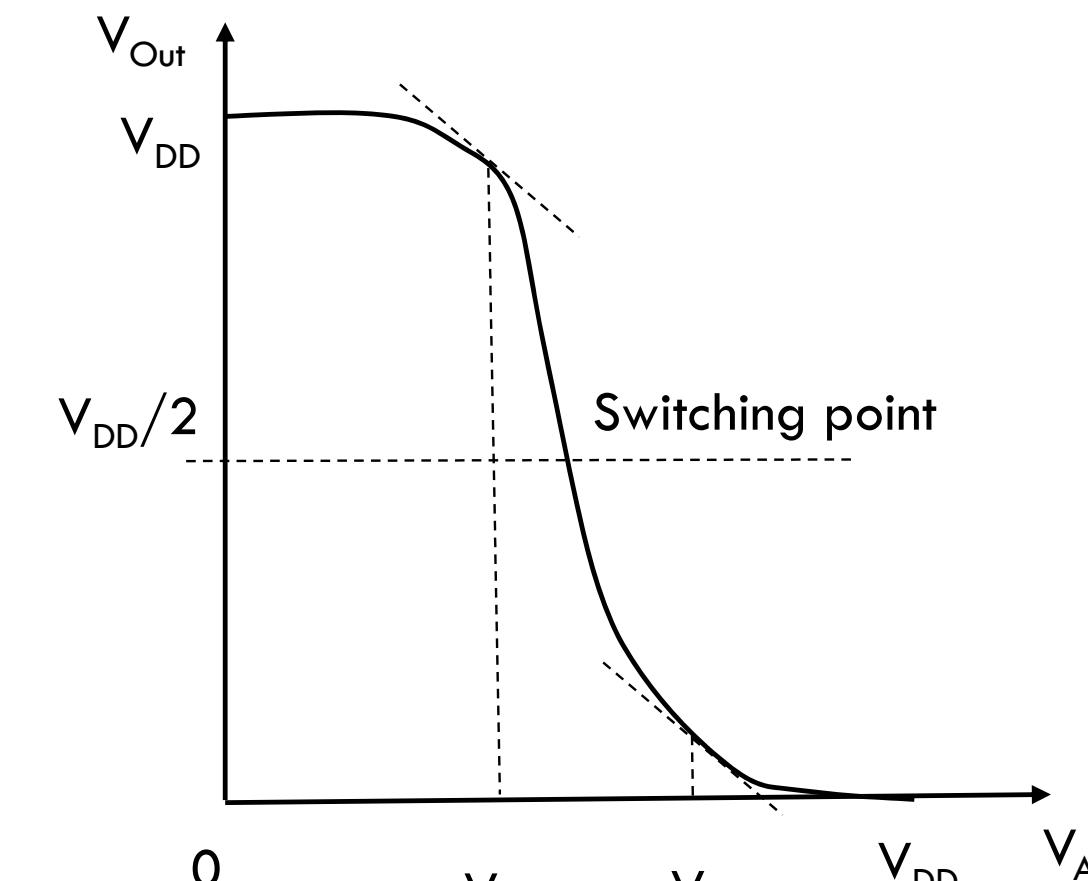
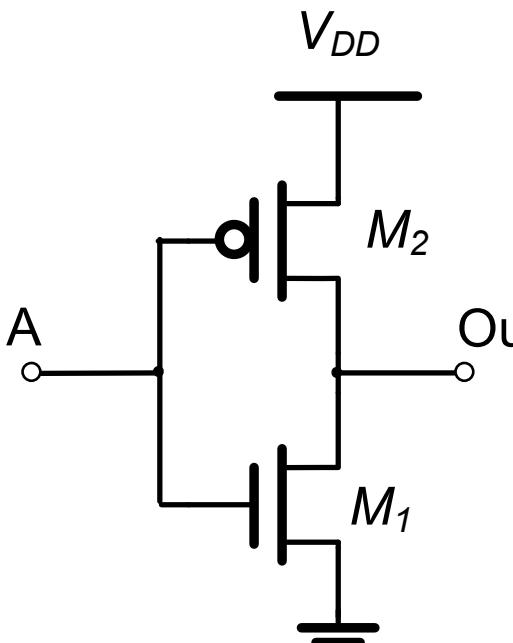
$$V_A = V_{DD} + V_{GS,p}$$

$$I_{Dn} = -I_{Dp}$$

$$V_{out} = V_{DD} + V_{DS,p}$$



Voltage Transfer Characteristic (VTC)



- Can we change switching point (V_A for which $V_{out} = V_{DD}/2$)?

Digital Circuits

- One logic representation

$$\text{Out} = \bar{A}$$

Truth table

A	Out
0	1
1	0

- Multiple libraries

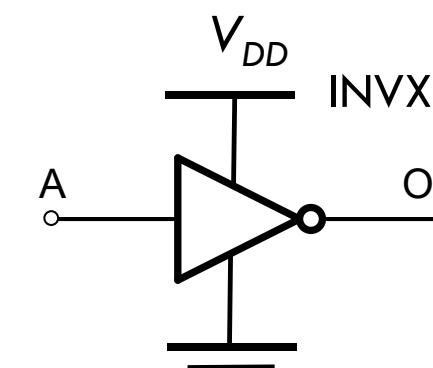
- Layouts

- Number of metal ‘tracks’
- More tracks, faster, but larger
- Less tracks – more compact, but slower

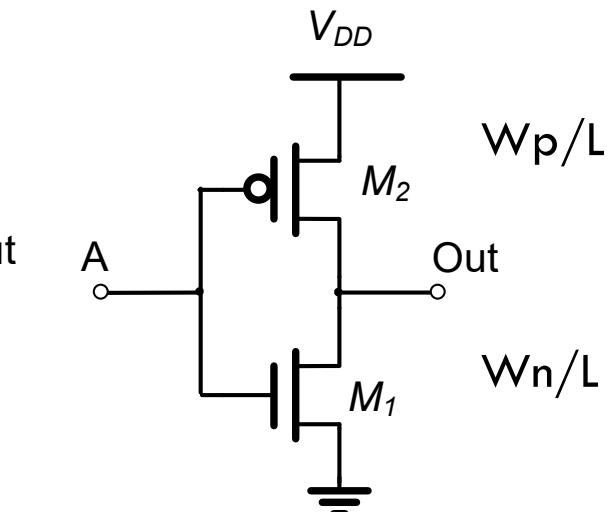
- Transistor thresholds (V_{Th}) (for each track height):
 - Regular (RVT)
 - Low (LVT)
 - Faster, higher power
 - Slower, lower power
 - High (HVT)
- Transistor lengths

- Multiple gate sizes within a library

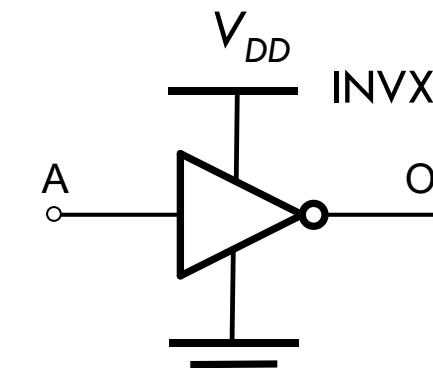
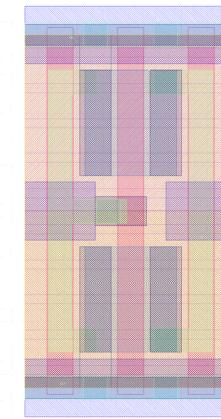
- Symbol



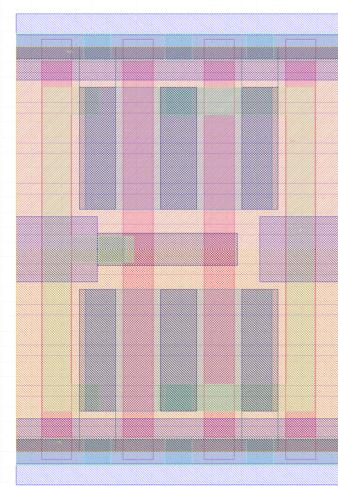
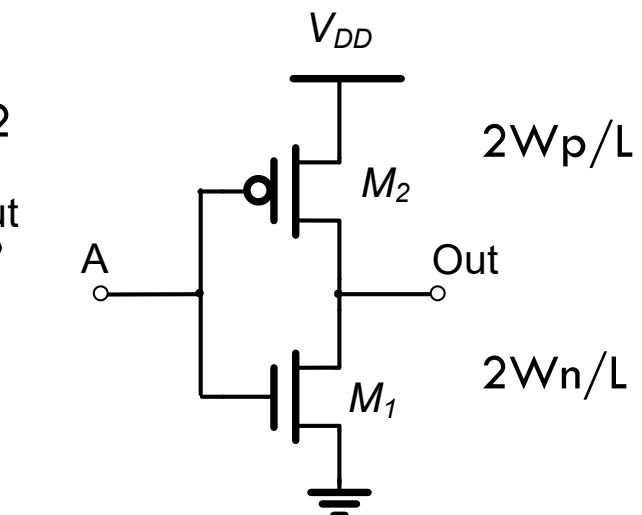
- Schematic



- Layout



INVX3,
INVX4,...



Summary

- Modern lithography is reflected in design rules
- FinFET widths are quantized
- MOS transistors can be modeled as resistive switches
 - They also have a capacitance
- CMOS VTC is nearly ideal