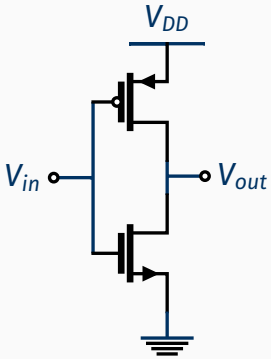
EECS 151/251A: Discussion 2

Noise Margins, RTL Design, Simulation

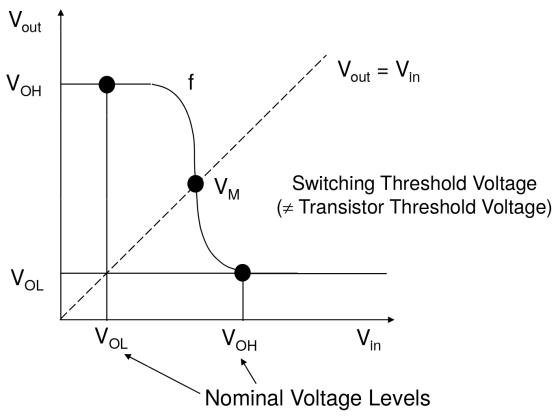
9/5/2019

The CMOS Inverter



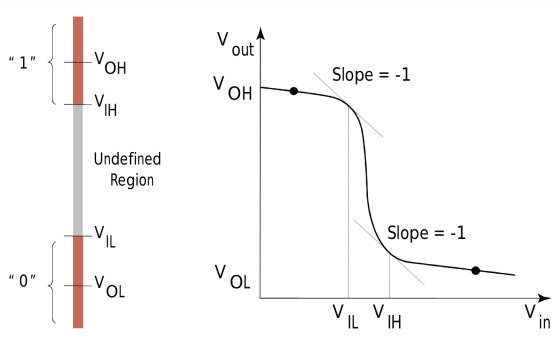
- NMOS turns ‘on’ when $V_{in} > V_{th,n}$
- PMOS turns ‘on’ when $V_{DD} - V_{in} > V_{th,p}$
- We assume each device has an on (R_{on}) and off (R_{off}) resistance

Voltage Transfer Characteristic



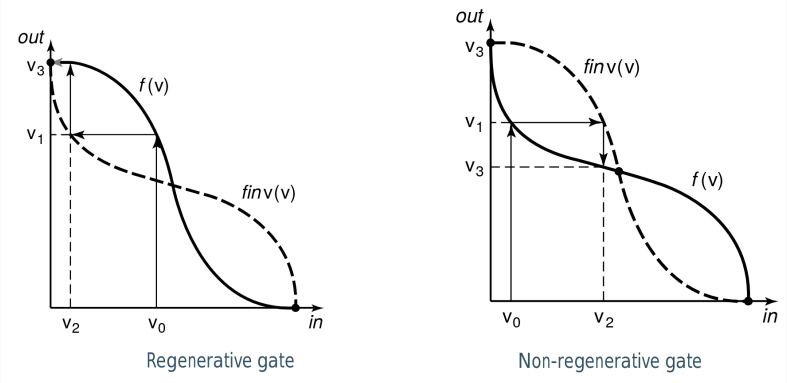
- $V_{OL} = 0$ and $V_{OH} = V_{DD}$ are the nominal low and high voltage levels
- V_M - the switching threshold is a function of the relative ‘strength‘ of the NMOS and PMOS
- Draw a VTC for $V_{DD} = 1, V_{th,n} = 0.2, V_{th,p} = 0.3, R_{on,n} = 10k\Omega, R_{on,p} = 20k\Omega$

Noise Margins



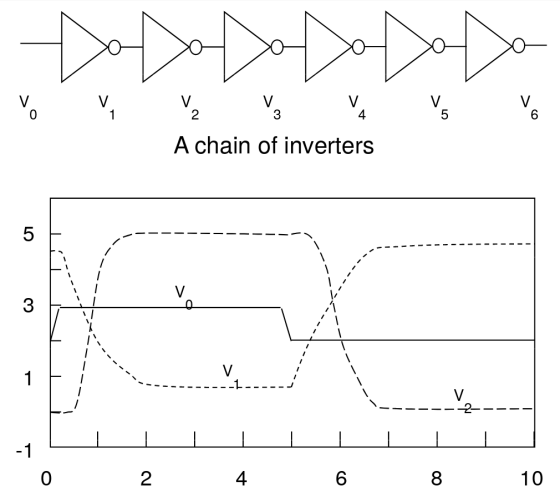
- V_{IL} and V_{IH} - bound the high-gain region of the VTC (unstable, high noise influence)
- In the undefined region the inverter acts like an amplifier and amplifies noise on the input and supply

Regeneration



- Regenerative inverter has a VTC with low-gain regions around supplies and a high-gain region in between

Inverter Chain



- A chain of CMOS inverters is regenerative, due to their VTCs
- As long as the input to the chain is not in the undefined region, the output will swing from rail to rail

Verilog

- We’re going over the Verilog Primer Slides and some slides from last semester’s Verilog discussion.

Simulation

We can test RTL via simulation before putting it on the FPGA or fabricating an ASIC.

Let’s test a simple adder circuit (demo time), then a freerunning counter, and some other stuff.