Q1) The power consumption stays the same at zow and the micro-processor becomes 40% faster to 5.661Hz in the next technology node based on the perfect Dennard scaling. Q2) VIL=0.75V; VIH=1.25V; VOL=0V; VOH=2V Noise margin high=0.75V Noise margin low = 0.75V. Q3) 1. NAND gate. 2. a) Let two inputs be the same. b) Use one blackbox with input A and B, then use the output of the blackbox as the both inputs for another blackbox. c) Let A be the two inputs for one blackbox, B be the two inputs for another blackbox, and let the two outputs from these two blackbox be the input of the third blackbox, 3,2-4. Propagation delay is 5 mich seconds. Q4) 1. CO=1, C1=0, C2=1, C3=0. 1. Yes, any arbitrary 2 input logics only has 4 possible inputs, the above architecture has all the possible combination as inputs to an DR gate with a control C'in C4.

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not ((notA and B) and (c xor D) and not (E or F))
Q5)
          = ~(1(~AB) (CAD)/ (E+F))
          = ~ C~ D+ CD+ ~ B+ F+E+A
          = noxCand not D or cand D or not B or For E or A
Q6) 1. ((Ā)(B) + C) (A+B)(B+AC)
     = ((A)(B)+c) (A+B) ((B)(AC))
     = ((A)(B)+c)(A+B)((B)(A+C))
     = (((A)(B)+c)(A)+((A)(B)+c)(B))((A)(B)+(C)(B))
     = (AAB+AC+ABB+BC) (AB+BC)
     = (AC+BC)(AB+BC)
    = AB(AC+BC) + BE (AC+BC)
     = (ABACT ABBC)+ (ACBG + BGBC)
      = ABC
   2, (A)(B)+ AB+ AB
     = (A)(B) + (B(A+A))
     = (A)(B)+B
     = (A+B)(B+B)
     = A+B
  3, A (A+B)+ (B+AA)(A+B)
     = AA + AB + (A+B) (A+B)
     = AB + (A(A+B) + B(A+B))
    - AB+ (A+ (AB+BB))
    = AB+ (A+ AB)
    = A+ AB+AB
    = A + B(A+A)
    = A+B
```