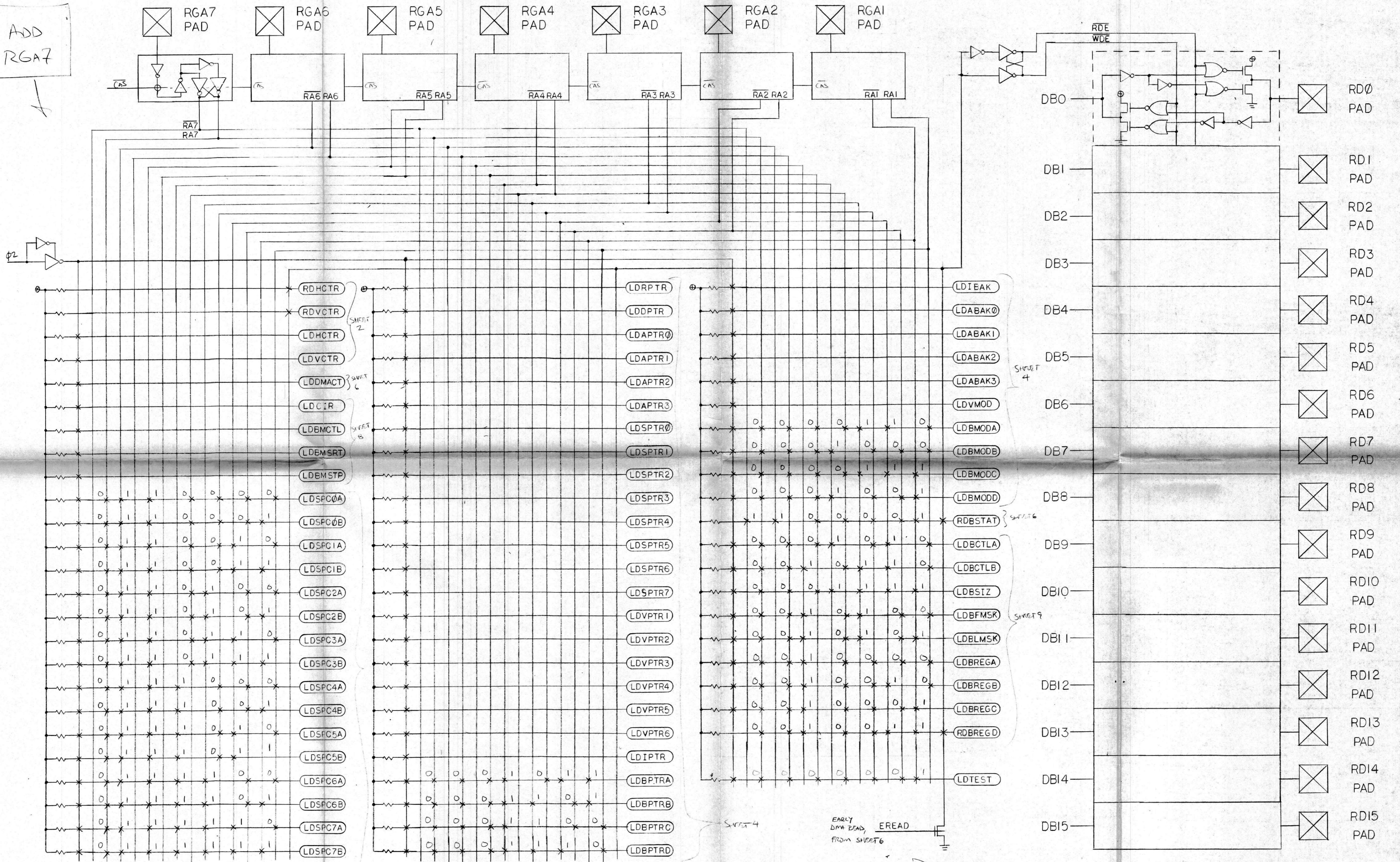
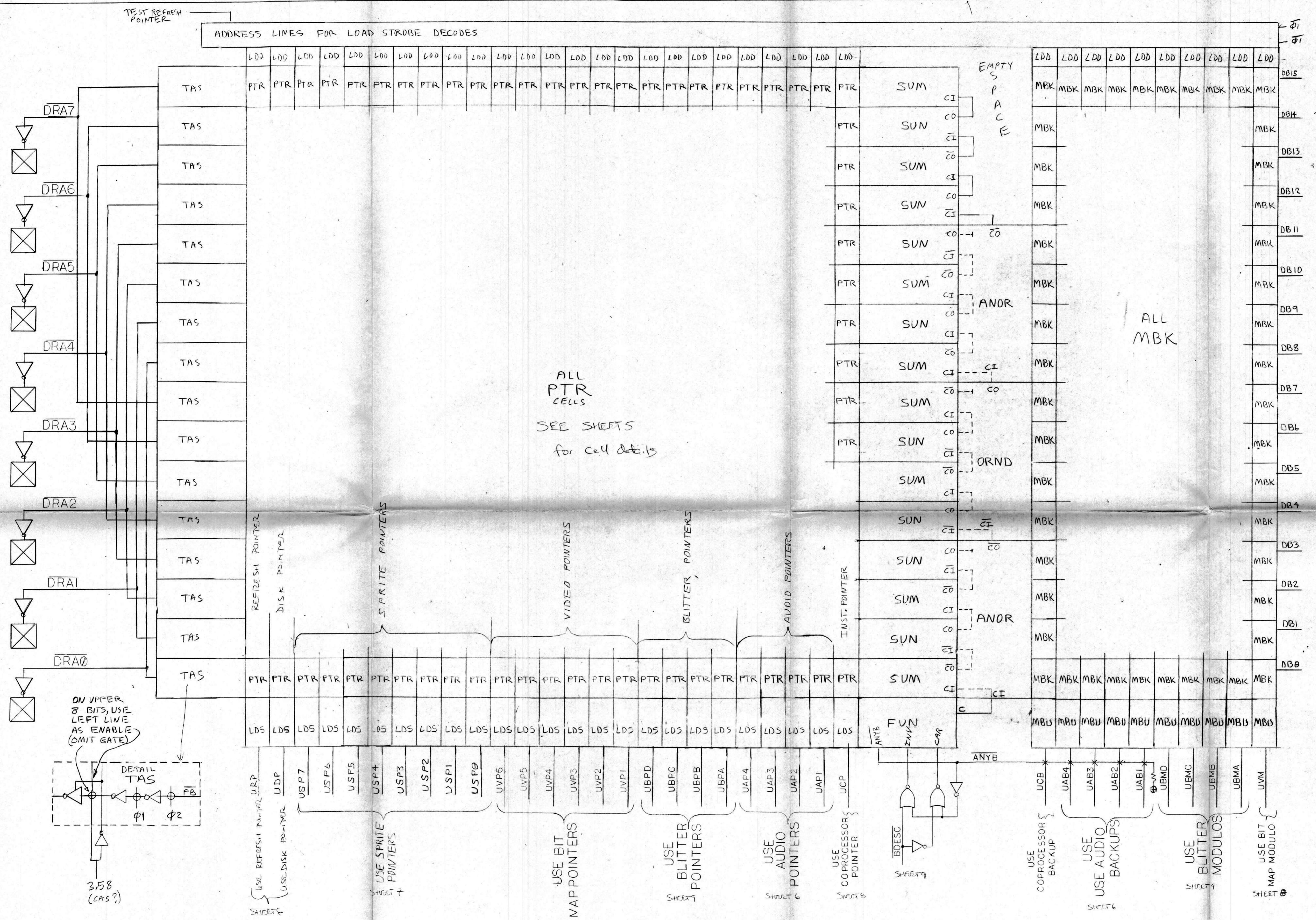
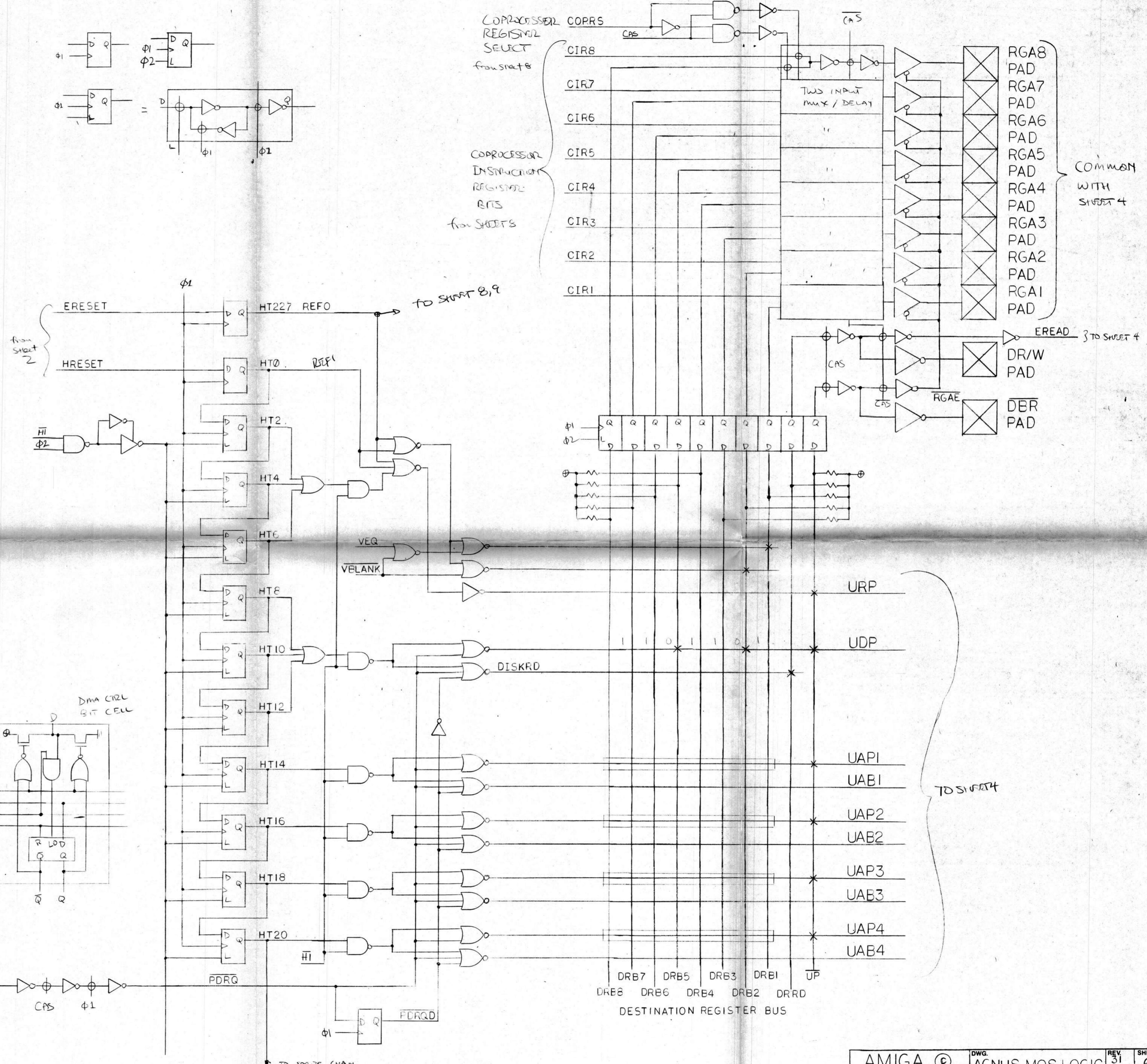
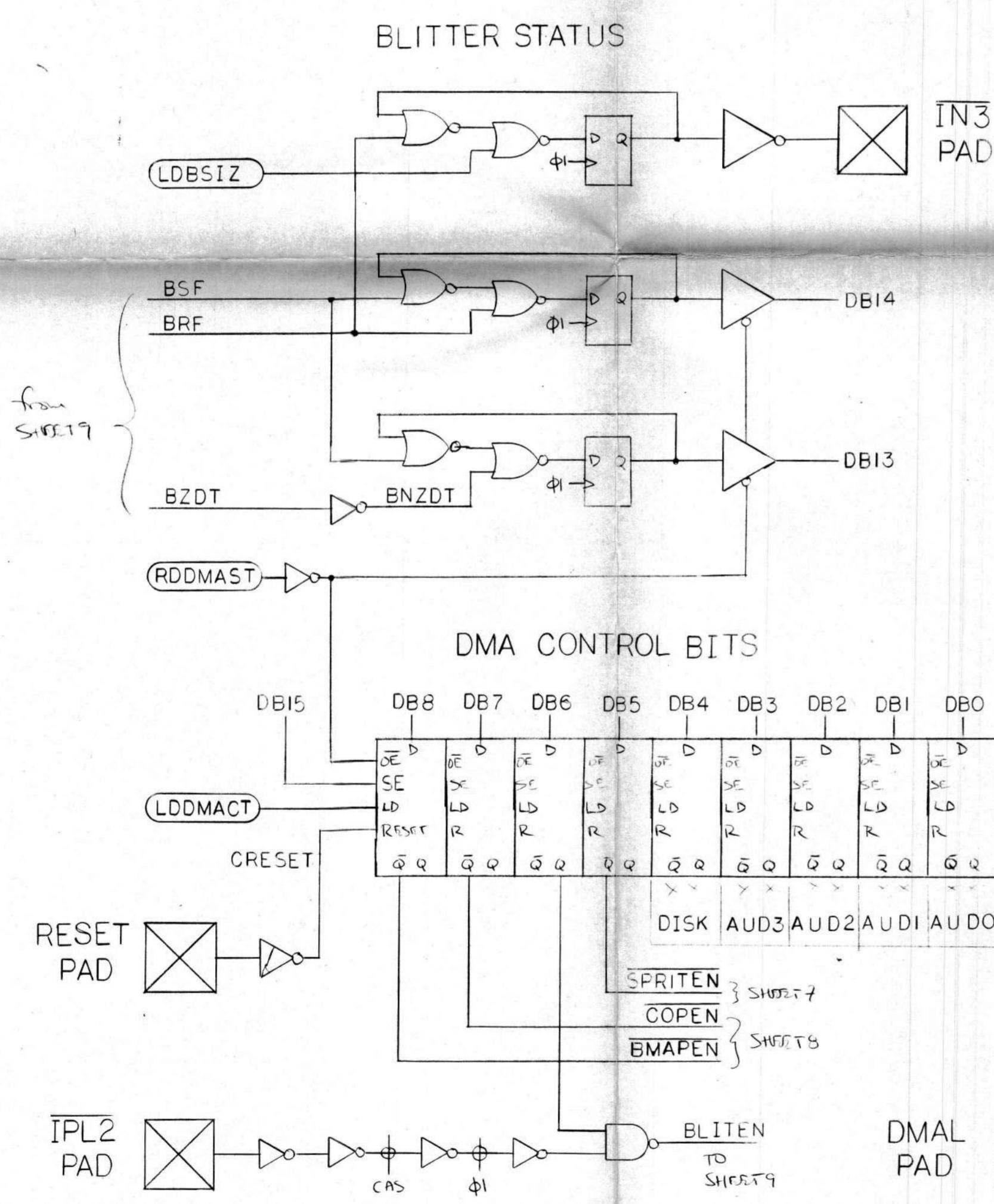
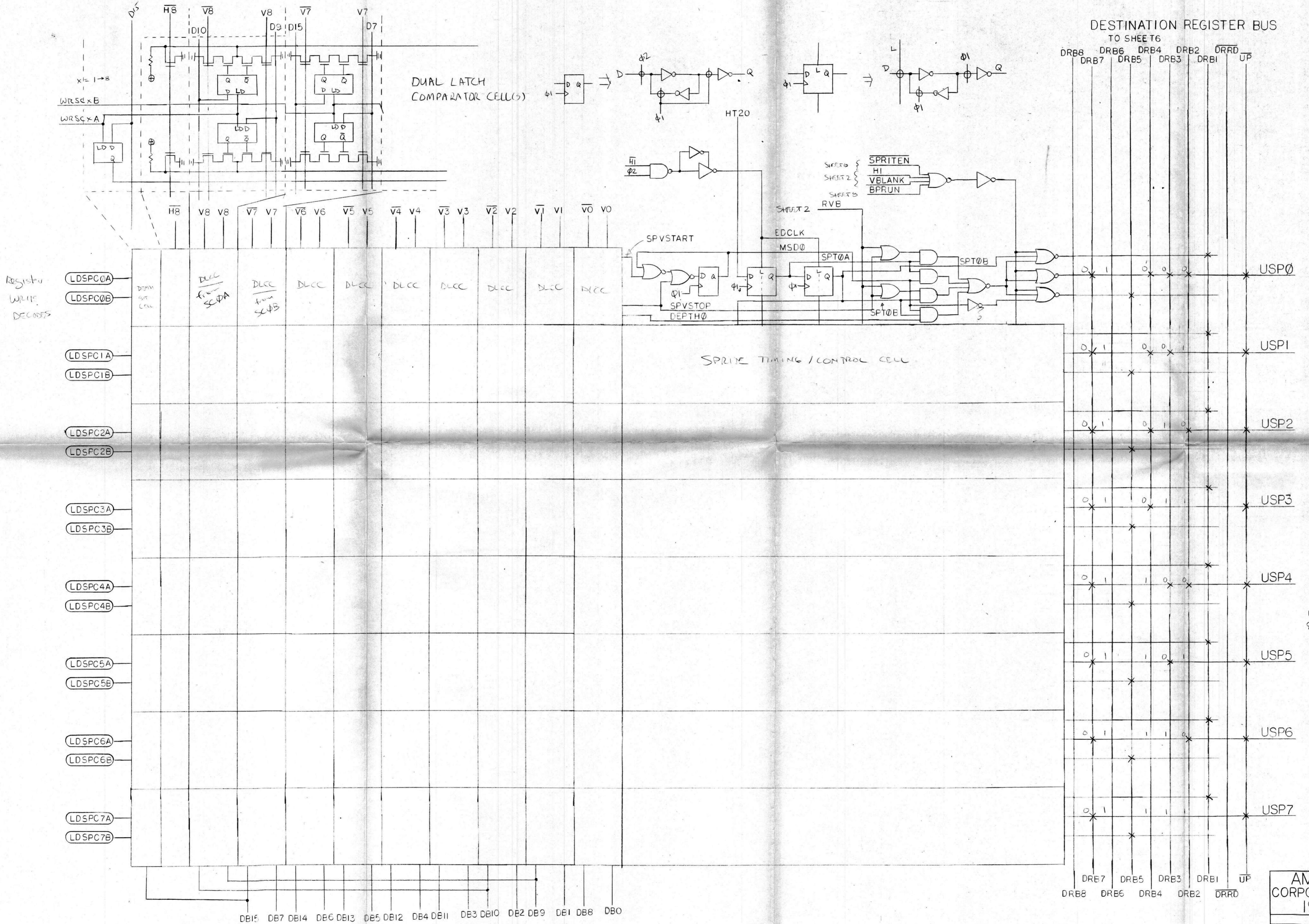


Review
EXACT
TIMING
WITH
DAPHNE,
DAVE DEAR



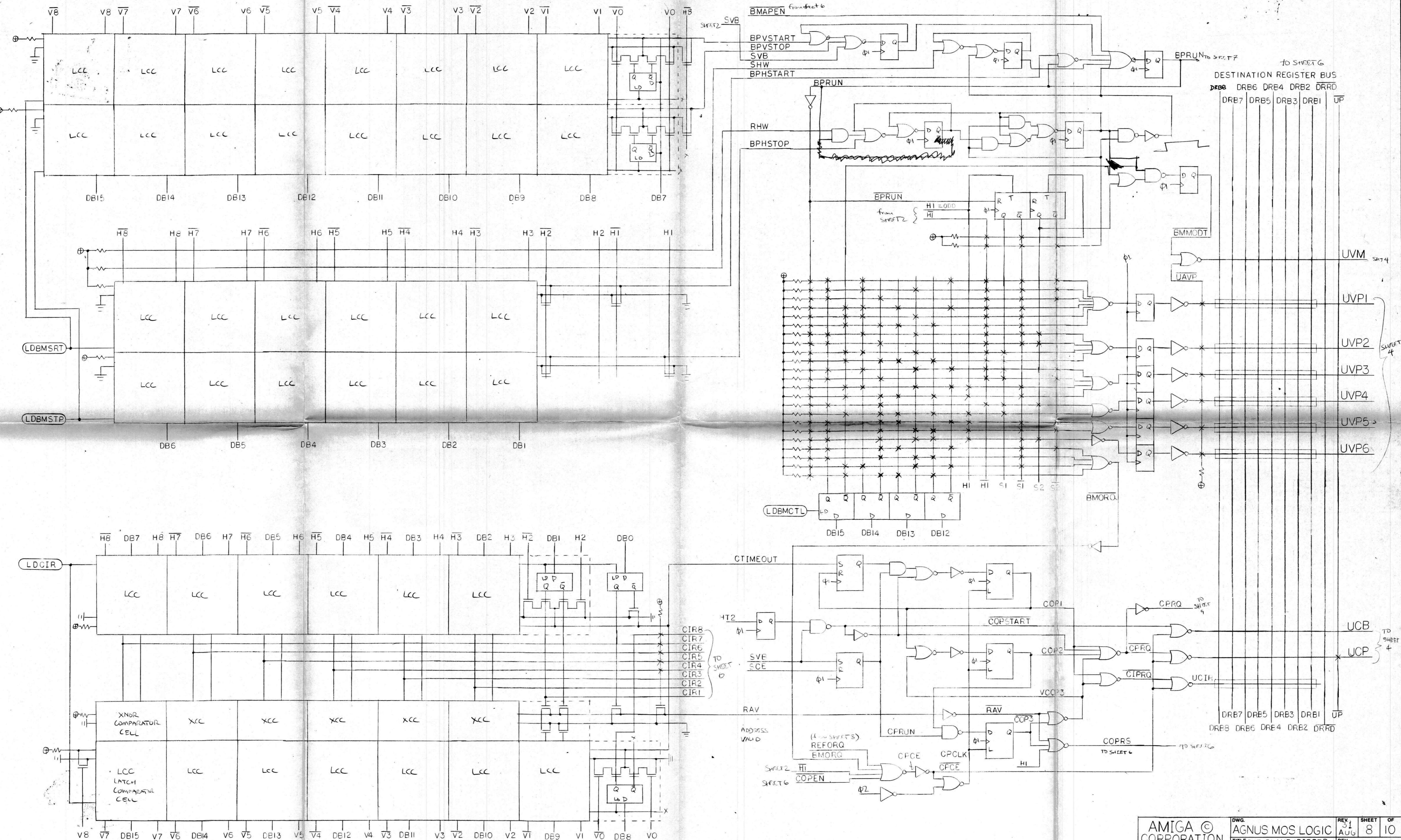




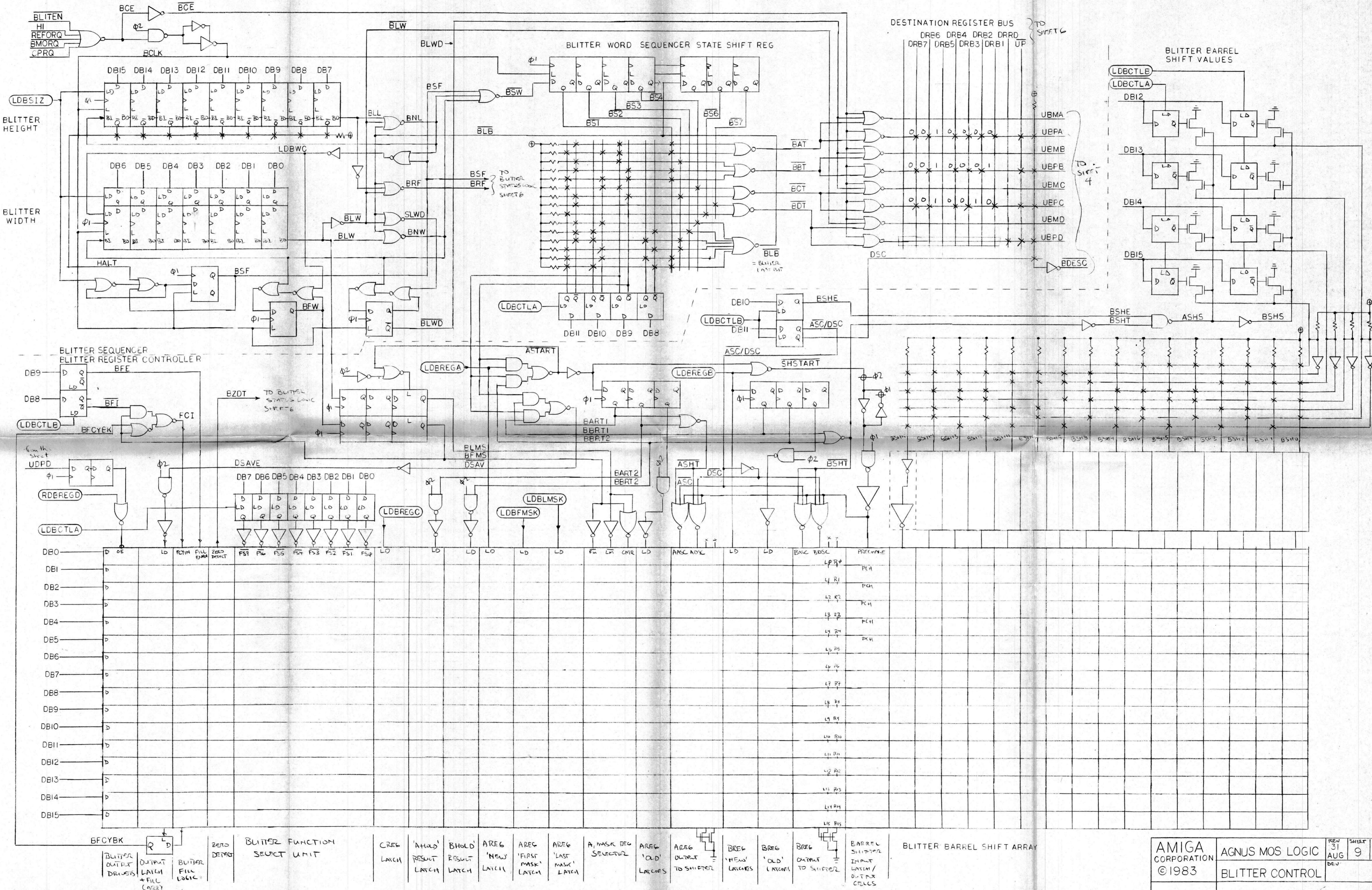


REGISTER ADDRESS 8:13	LABEL	FUNCTION
\$71654321	SDOA	SPRITE DATA (DU)
0100000	SDOB	"
0100010	SD1A	"
0100011	SD1B	"
0100100	SD2A	"
0100110	SD2B	"
0100111	SD3A	"
0101000	SD3B	"
0101001	SD4A	"
0101010	SD4B	"
0101011	SD5A	"
0101100	SD6A	"
0101101	SD6B	"
0101110	SD7A	"
0101111	SD7B	"
0110000	SC0A	HSTART0 (C4)
0110001	SC0B	VSTART0 (C5) VSTOP0 (C6)
0110010	SC1A	HSTART1
0110011	SC1B	VSTART1 VSTOP1
0110100	SC2A	HSTART2
0110101	SC2B	VSTART2 VSTOP2
0110110	SC3A	HSTART3
0110111	SC3B	VSTART3 VSTOP3
0111000	SC4A	HSTART4
0111001	SC4B	VSTART4 VSTOP4
0111010	SC5A	HSTART5
0111011	SC5B	VSTART5 VSTOP5
0111100	SC6A	HSTART6
0111101	SC6B	VSTART6 VSTOP6
0111110	SC7A	HSTART7
0111111	SC7B	VSTART7 VSTOP7

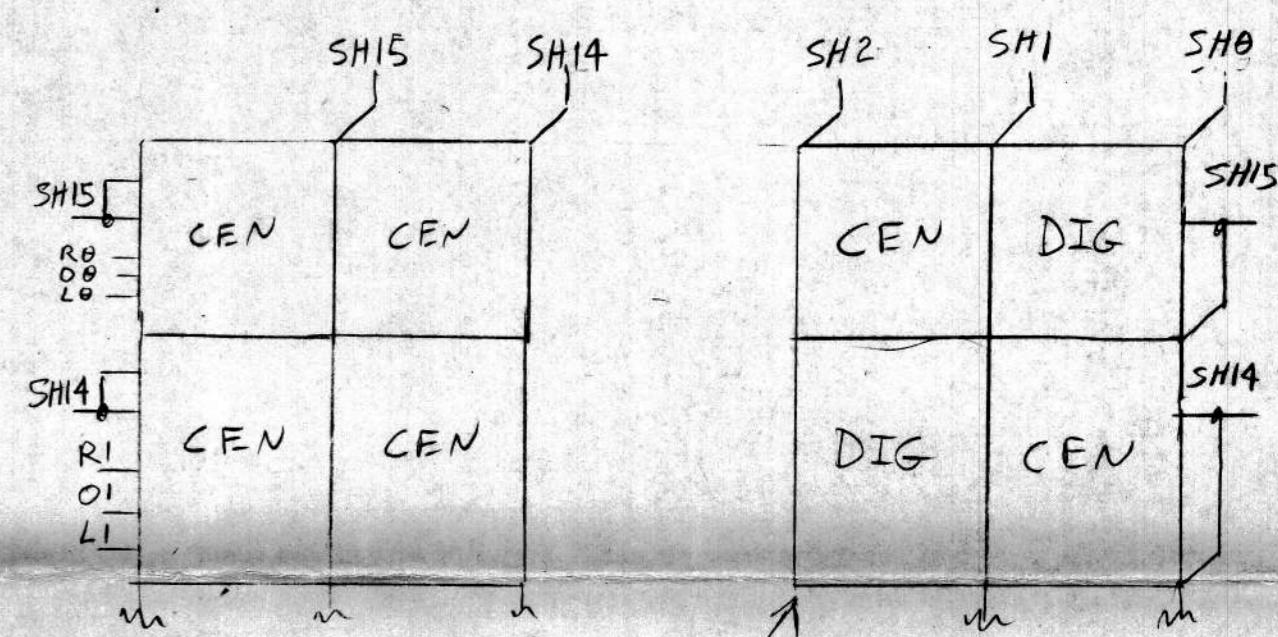
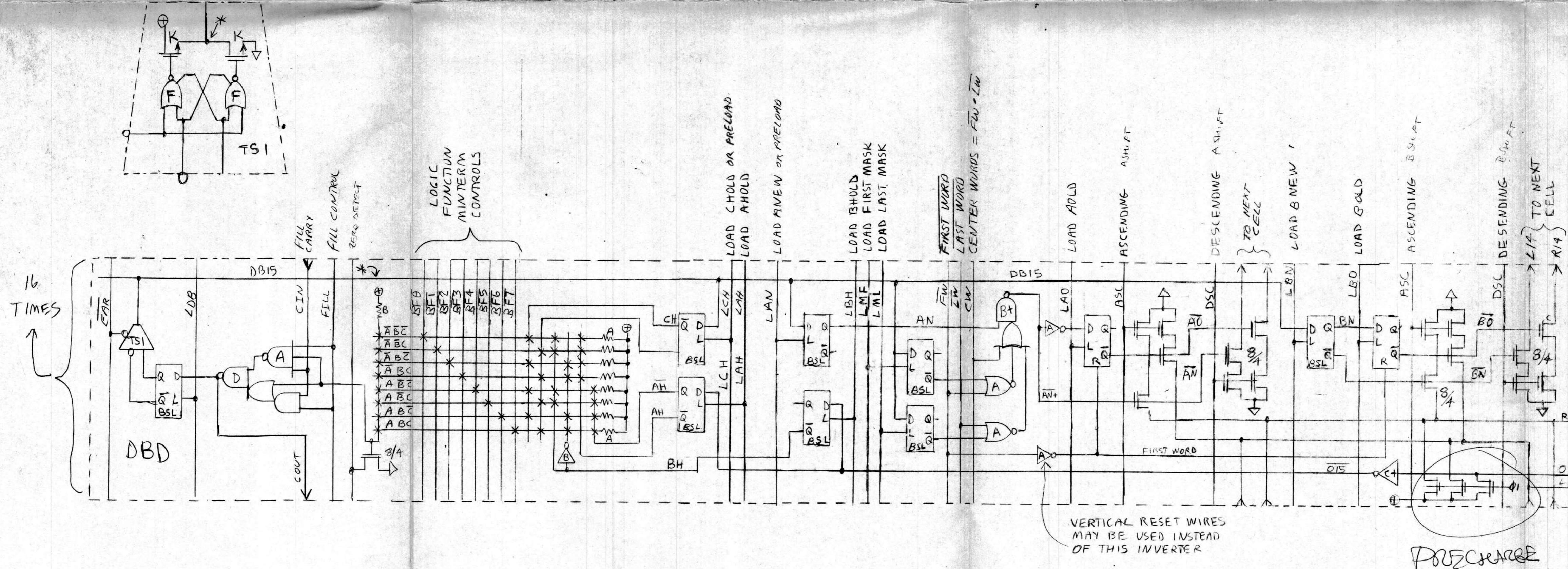
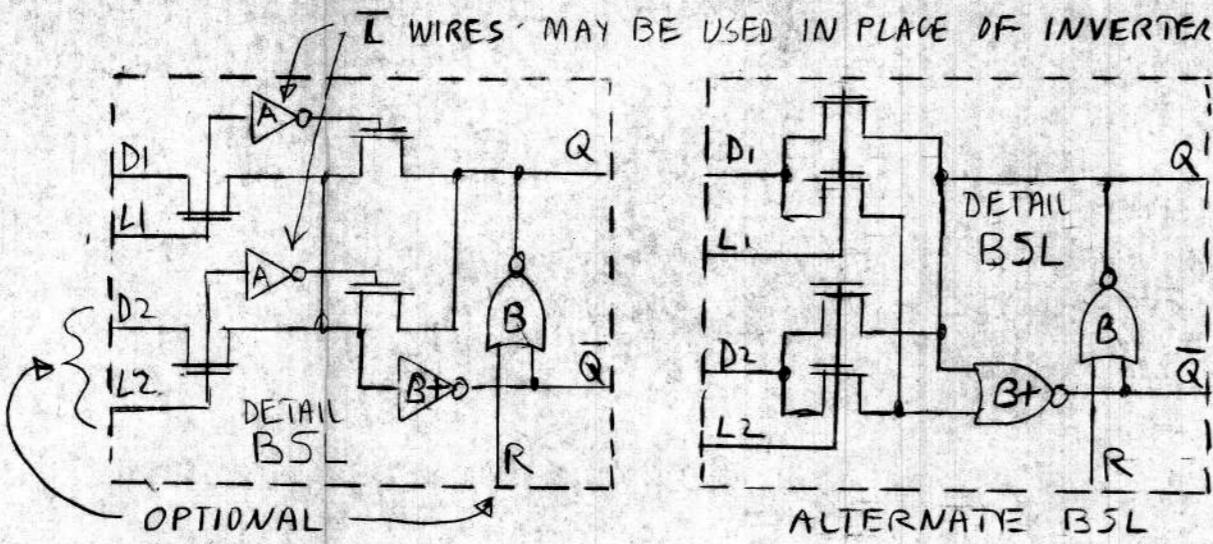
I = DATA
φ = CONTROL



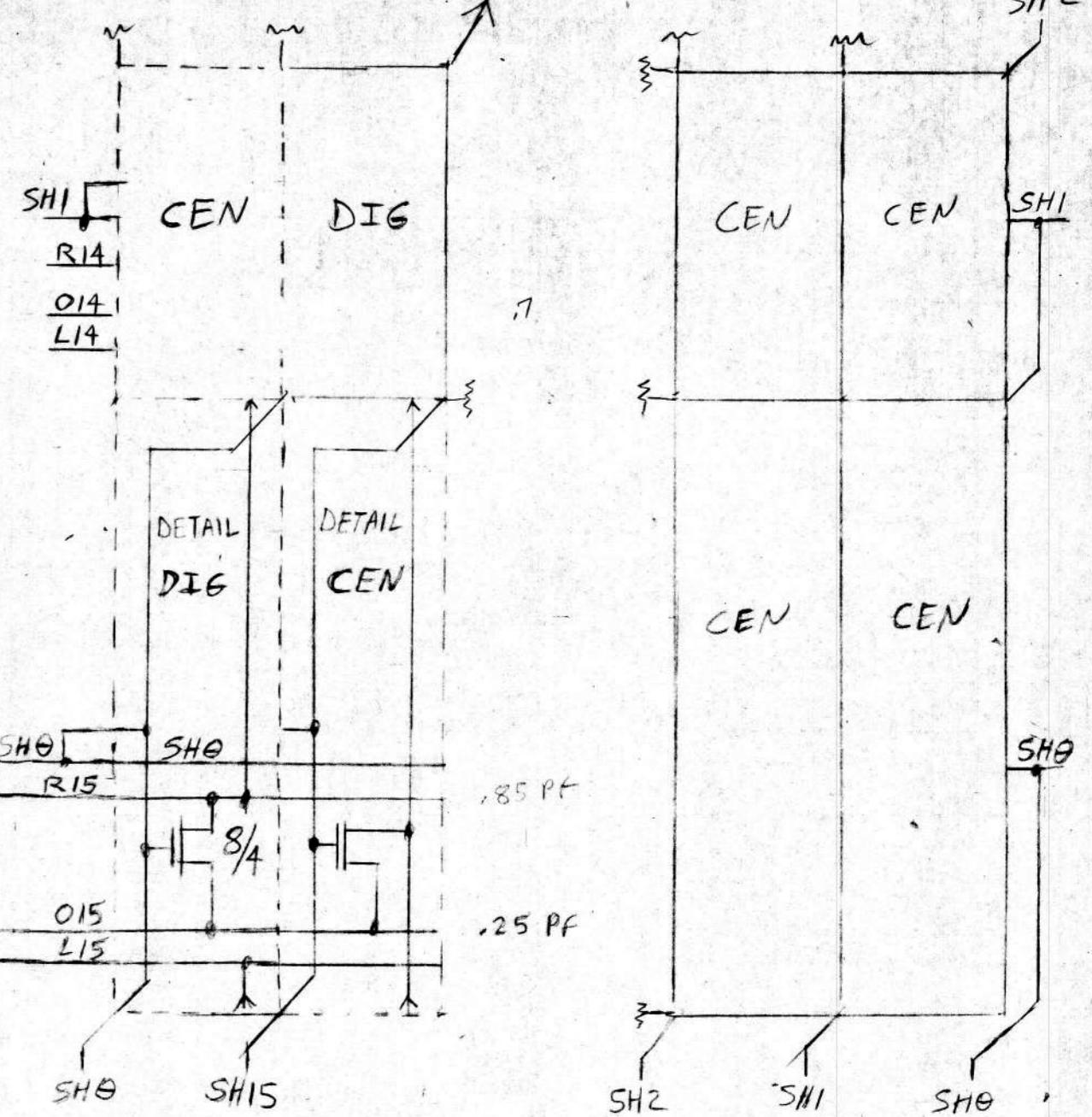
AMIGA © CORPORATION	DWG. NO.	REV. 31	SHEET 8	OF 10
1983	AGNUS MOS LOGIC			
JULY 83	TITLE: BIT PLANE / DIPPER DMA CONTROL LOGIC			
DECUIR				



APPROX RATIO → 6		+ = 12		++ = 18		
INVERTERS 2 NAND, OR 4 NOR GATES		3 NAND, OR 2 NAND AND SERIES GATE				
SYM	N	D	N	D	N	D
A	4/4	3/32	64	3/32	8/4	3/32
B	4/4	3/24	8/4	3/24	12/4	3/24
C	6/4	3/16	12/4	3/16	18/4	3/16
D	8/4	4/12	16/4	4/12	24/4	4/12
E	12/4	4/8	24/4	4/8	36/4	4/8
F	16/4	4/6	32/4	4/6		
G	24/4	4/4				
H	36/4	6/4				
I	48/4	8/4				
J	72/4	12/4				
K	96/4	16/4				



DIG CELL
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DIAGONAL
ONLY.
(16 TIMES)



AMIGA	DWG.	REV.	SHEET	OF
AGNUS LOGIC (BLIT UNIT)			10	10
6/21/83	J. Monner			