Minimum Acceptance Level

The minimum acceptance level of any lot shall be an AQL of 0.65 as defined by MIL-STD 105 single sampling techniques.

Age of Devices

Unit shall be rejected if EIA Date Code indicates an age of three (3) or more years.

Markings

Devices shall be marked with Commodore part number and copyright notice as follows:
© CBM 1989.

FAT GARY Chip Specification

Description

FAT GARY (which will subsequently be referred to as simply 'GARY') is a custom gate array IC used in the A4000. It is packaged in an 84-pin chip, whose pinout is shown below. GARY provides many different 'glue' functions for the system. These functions are:

- Address decoding and timing for ROM
- Address decoding and timing for Chip RAM
- Address decoding and timing for chip registers
- Address decoding and timing for 8520s (CIAs)
- Address decoding and timing for Real Time Clock (RTC)
- Address decoding for the Floating Point Unit (FPU)
- Address decoding for the SCSI/DMA controller IC
- Address decoding for the local bus card slot of the A3000
- Monitoring of the bus for timeout conditions
- Generation of ECLK clock signal
- Generation of 32-bit and 16-bit data strobe signals
- Decoding for generation of AUTOVECTOR (*AVEC) signal to 68030
- Selection of the AGNUS clock source
- System RESET logic
- System INTERRUPT control

Configuration

The device shall be configured as a standard 84-pin Plastic Leaded Chip Carrier with external dimensions as shown in Figure 6-23. Refer to Figure 6-24 for connection diagram.

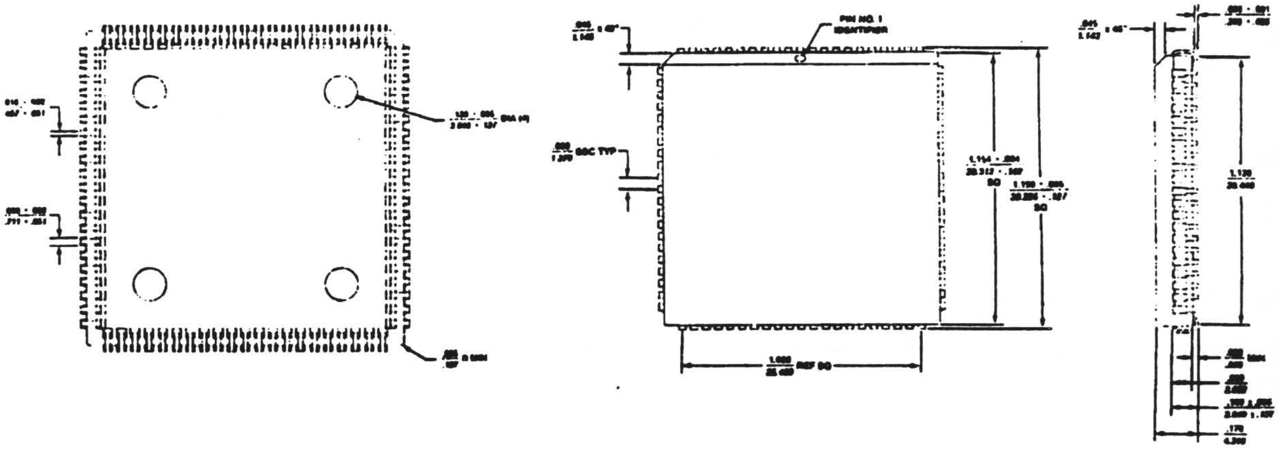


Figure 6-23. External Dimensions

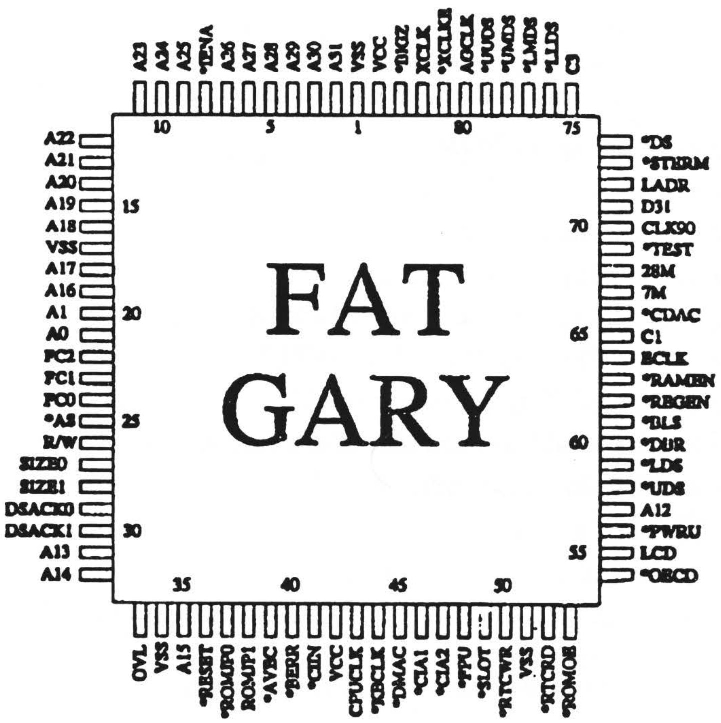


Figure 6-24. Connection Diagram

Sources

Refer to *Approved Vendor List* on page 6-58.

Pin Descriptions

Name	Dir	Description
CPUCLK	Input	
CLK90	Input	CPUCLK shifted 90 degrees.
28M	Input	
7M	Input	
*CDAC	Input	
C1	Input	
C3	Input	
XCLK	Input	
AGCLK	Output	
OVL	Input	Overlay. When high, ROM is mapped in at $00000000 in place of Chip RAM.
ROMJP0,1	Input	ROM jumpers. Used to select ROM access speed.
*AS	Input	68030 address strobe.
*DS	Input	68030 data strobe.
RW	Input	68030 read/write signal.
SIZ0-1	Input	68030 sizing information.
FC0-2	Input	68030 function code bits.
A0,1,12-23	Input	68030 address bits.
A24-31	Bi	68030 address bits.
*BIGZ	Input	When low, address bits A24-31 become outputs, and drive these lines low.
D31	Bi	68030 data bit. Used to communicate with internal registers.
*FPU	Output	Floating Point Unit chip select.
*ROMOE	Output	Output enable signal for the ROM.
*SLOT	Output	Select signal for local bus card slot.
*DMAC	Output	Chip select signal for the DMA controller.
*STERM	Output(OC)	68030 Synchronous Termination signal.
*RTCRD	Output	Real Time Clock read signal.
*RTCWR	Output	Real Time Clock write signal.
LADR	Output	Latch address (external latches for 8520s and RTC).
ECLK	Output	Clock whose frequency is 1/10th that of 7M.
*CIA1,0	Output	Chip select signals for the 2 CIAs (8520s).
*DBR	Input	When high, chip bus is available.
*BLS	Output	Blitter slow down. To AGNUS, requesting access to chip bus.
*RAMEN	Output	Select signal for Chip RAM.
*REGEN	Output	Select signal for chip registers.
LCD	Output	Latch chip data. Controls external latches for chip bus data being read by the 68030.
*OECD	Output	Output enable signal for data being read/written on chip bus.
*xxDS	Output	*UUDS, *UMDS, *LMDS, *LLDS. Data strobe signals for a 32-bit port.
*xDS	Output	*UDS, *LDS. Data strobe signals for a 16-bit port.

Name (cont'd)	Dir (cont'd)	Description (cont'd)
*BERR	Output(OC)	Bus error signal.
*CIIN	Output(OC)	Cache inhibit.
*DSACK0,1	Output(OC)	68030 Data Transfer and Size Acknowledge bits.
*AVEC	Output(OC)	AUTOVECTOR signal.
*IENA	Output	Interrupt enable. This bit is controlled by an internal register.
*RESET	Bi	Reset.
*PWRUP	Input	Power Up. When low, an internal bit is set.
*KBCLK	Input	Keyboard clock.
*TEST	Input	Test. Diagnostic use only.

ROM

The onboard ROMs are selected in the address range from $00F80000 to $00FFFFFF. The ROMs are also selected in the range from $000000000 to $0007FFFF when the overlay input signal (OVL) is true (this allows the RESET instructions to be contained in the ROMs). The ROM shows up in data and program space for both the user and supervisor. ROM caching is enabled.

ROM Timing

The ROM timing circuitry provides for four different speed settings, settable by two jumpers on the motherboard. The *STERM signal is used to terminate the CPU bus cycle during a ROM access.

Table 6-6. ROM Speed Jumper Settings

JP1	JP0	CPU cycles
0	0	5
0	1	6
1	0	7
1	1	8

The minimum output enable (Toe) and access (Tacc) times for the ROMs is determined by the following:

Toe = ((# CPU cycles) - 2) * Tcyc - Tgary

Tacc = ((# CPU cycles) - 1) * Tcyc

where

Tcyc = period of a single 68030 clock

Tgary = delay through GARY (30 ns max)

The timing waveform and state diagram for a ROM access is shown in Figure 6-25.

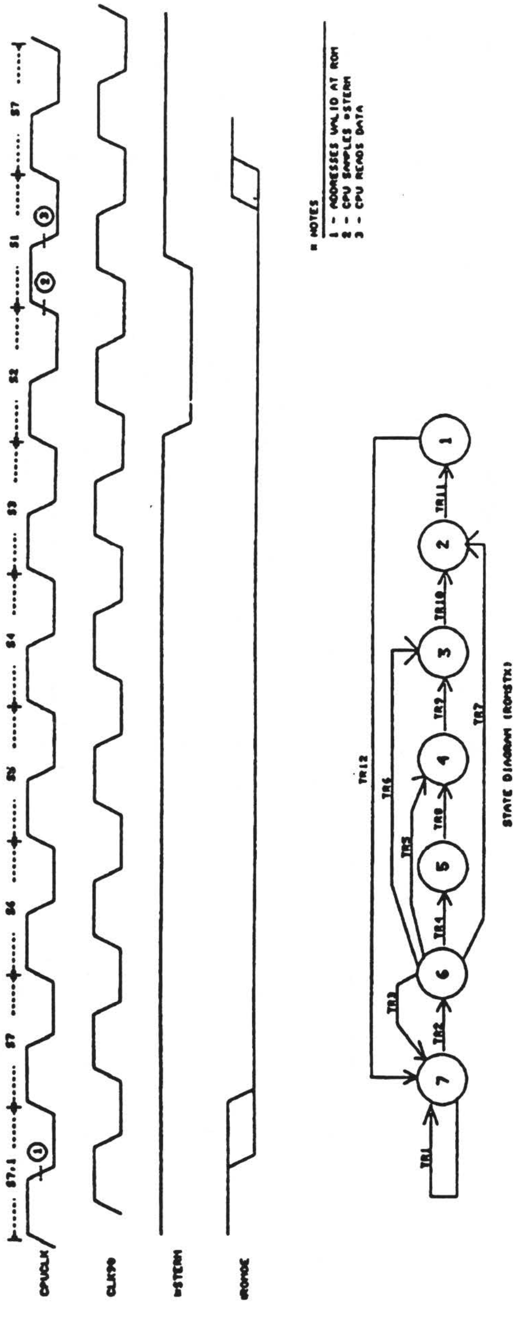


Figure 6-25. ROM Timing

Chip RAM

Chip RAM is selected in the address range from $00000000 to $001FFFFF. When the OVL input is true (high), Chip RAM is not selected for addresses in the range from $00000000 to $0007FFFF (ROM appears here while OVL is true). Chip RAM shows up in data and program space for both the user and supervisor. Chip RAM caching is disabled. The CPU cycle is terminated using both DSACKs, indicating that the Chip RAM data is 32 bits wide.

Chip RAM Timing

Timing for the signals used is shown in Figure 6-26.

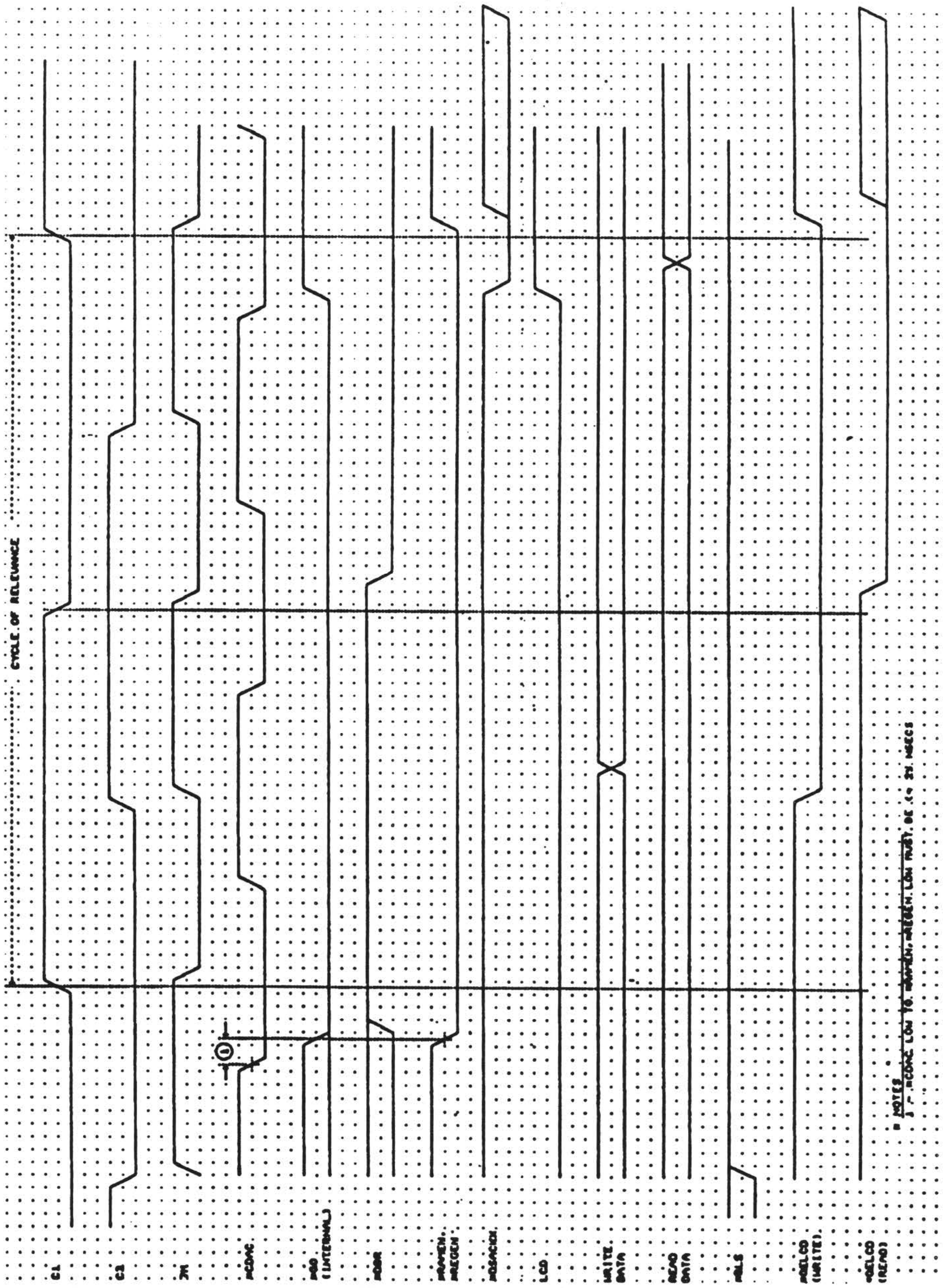


Figure 6-26. CPU Read/Write of Chip Registers and RAM

Chip Registers

The chip registers are selected in the range from $00DFC000 to $00DFFFFF. They also show up from $00C00000 to $00CFFFFF, so that code looking for $C00000 memory will work properly (consequently, C00000 memory is NOT supported). Chip registers show up in user and supervisor data space. Chip register caching is disabled. The CPU cycle is terminated using DSACK1, indicating that the chip registers are 16 bits wide.

8520s

There are two 8520 CIA ICs on the motherboard, referred to here as CIA0 and CIA1. CIA0 is selected in the address range from $00BFE000 to $00BFEFFF. CIA1 is selected from 00BFD000 to 00BFDFFF. The CIAs show up in user and supervisor data space. Caching is disabled. The CPU cycle is terminated by DSACK1, indicating that the CIA is 16 bits wide. In fact, the CIAs are only 8 bits wide, but respond as 16 bits for compatibility. In order to read the 8 bits in on the 68030's D0-D7, CIA0 must be read at an odd word address, and CIA1 must be read at an even word address.

8520 Timing

Figure 6-27 shows the timing for the signals when accessing the 8520s.

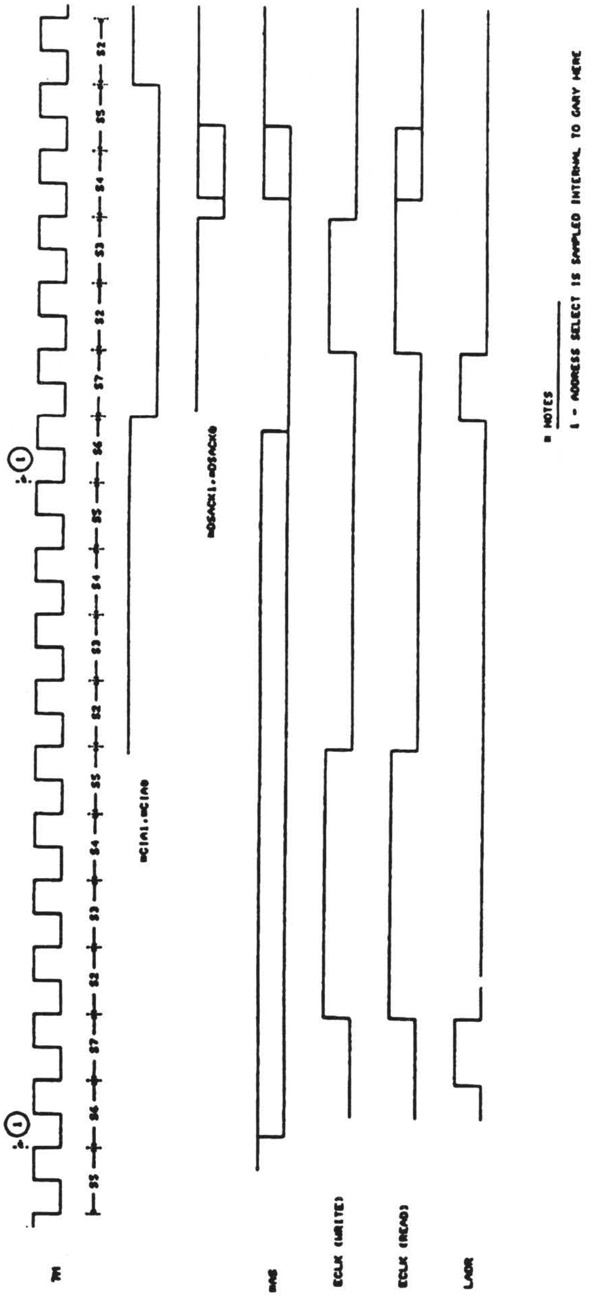

7M
S5 S6 S7 S2 S3 S4 S5 S2 S3 S4 S5 S6 S7 S2 S3 S4 S5 S2
1
1
*CIA1.*CIA0
*DSACK1.*DSACK0
RAS
ECLK (WRITE)
ECLK (READ)
LADR
* NOTES
1 - ADDRESS SELECT IS SAMPLED INTERNAL TO GARY HERE

Figure 6-27. 8520 Timing and ECLK Generation

Real Time Clock (RTC)

The RTC is selected in the range from $00DC0000 to $00DCFFFF. It appears in user and supervisor data space. Caching is disabled. The CPU cycle is terminated by DSACK1, indicating that the RTC is 16 bits wide. It is actually only 4 bits, but responds as 16 bits for compatibility. In order to read the 4 bits in on the 68030's D0-D3, the RTC must be read at an odd word address.

RTC Timing

Figure 6-28 shows the timing of the signals for reading and writing to the RTC.

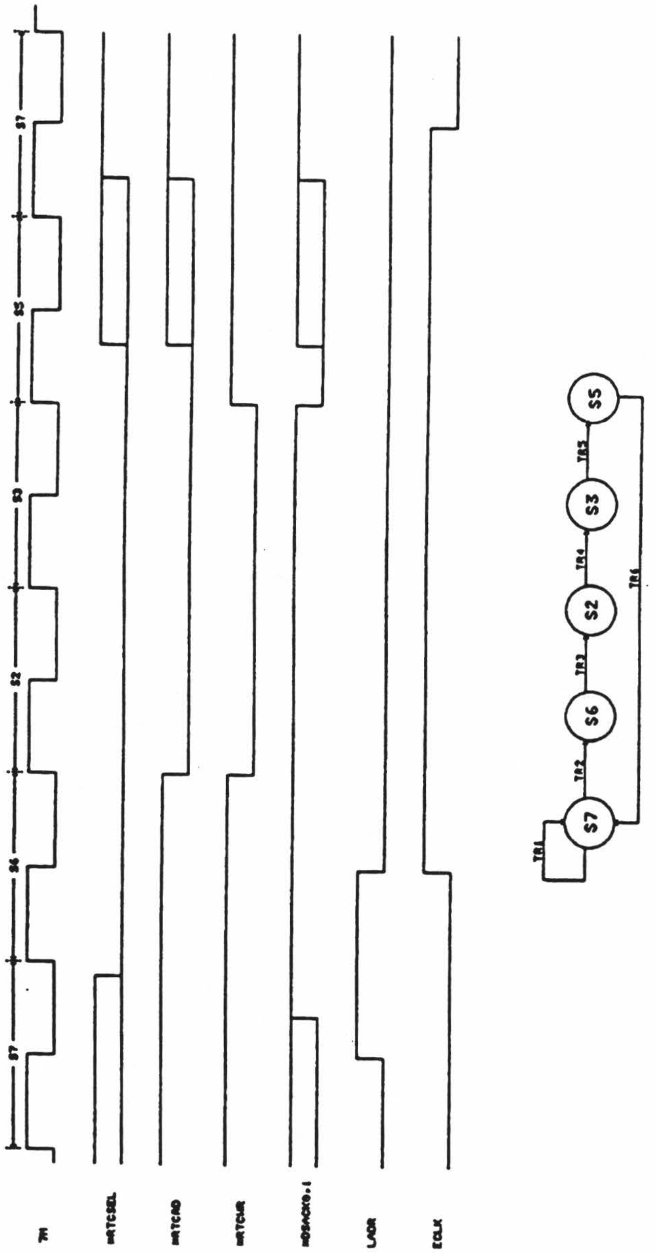


Figure 6-28. Real Time Clock Timing

Floating Point Unit (FPU)

!FPUCS = *AS & FC2 & FC1 & FC0 & !A19 & !A18 & A17 & !A16 & !A15 & !A14 & A13

The FPU performs its own bus cycle termination.

SCSI/DMA Controller

The SCSI/DMA controller is selected from $00DD0000 to $00DD3FFF. It appears in user and supervisor data space. Caching is disabled. In order to get this signal out to the chip as quickly as possible, it is NOT qualified with address strobe (*AS). The SCSI/DMA controller performs its own bus cycle termination.

!DMAC = !FC1 & FC0 & !A31 & !A30 & !A29 & !A28 & !A27 & !A26 & !A25 & !A24, & A23 & A22 & !A21 & A20 & A19 & A18 & !A17 & A16

Local Bus Card Slot

This signal is generated in the address range from $08000000 to $0FFFFFFF. The signal is NOT qualified with *AS. The selection shows up in all address spaces except for CPU space. No bus cycle termination is performed.

!SLOT = FC2 & FC1 & FC0 & !A31 & !A30 & !A29 & !A28 & A27

Bus Timeout

After the assertion of *AS, a counter in GARY starts running, and is reset by the de-assertion of *AS. If the counter counts down before *AS is de-asserted, GARY terminates the cycle automatically. There are two different timer values available, each of which terminates the cycle differently.

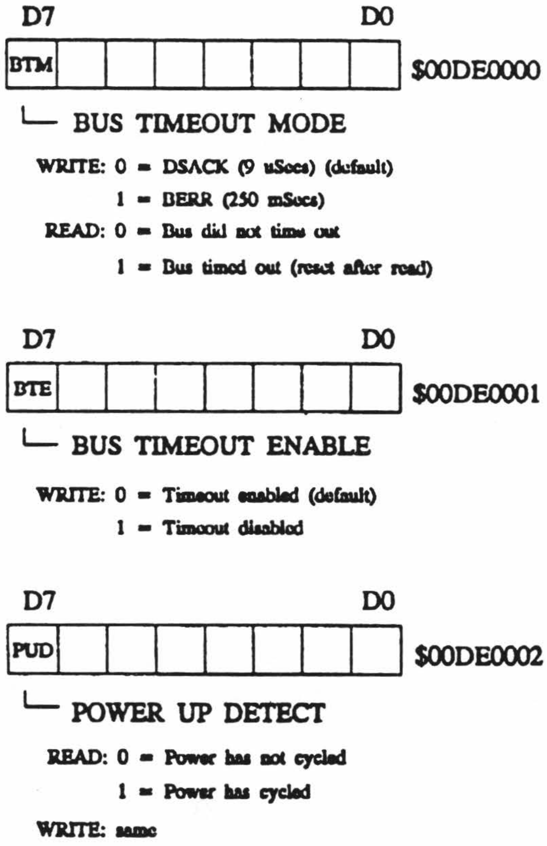
There is an 8-bit register in GARY at $00DE0000 of the user and supervisor data space. When written to, bit 7 selects the timeout mode to be used. Writing a 0 to this bit enables DSACK timeout, and a 1 enables BERR timeout (after a RESET, DSACK timeout is enabled). DSACK timeout counts for 32 C1 pulses (approximately 9 μsecs), and then asserts both DSACKs to terminate the cycle. BERR timeout takes much longer, counting for approximately 250 msecs before asserting the *BERR signal. Whenever a bus timeout occurs in either mode, bit 0 of the register at $00DE0000 is set, and is not reset until the register is read.

The purpose of the timeout is to keep the system from getting hung up if an address is asserted that selects nothing. Using BERR mode allows the system to be informed if this occurs.

The DSACK bus timeout mode was made much sorter, and terminates the bus much more 'discreetly' using DSACKs. This mode was made the default because of compatibility issues. The 1.3 ROMs purposely snoop through a large range of address spaces during boot up, which most of the time aren't there. Taking 250 msecs for each one causes it to take forever to boot up. Terminating each bus cycle with *BERR also makes the software get confused. The idea is to get everything running, and then change over to BERR mode.

Since the blitter has the capability of keeping the CPU off of the chip bus for a long time, bus timeout detection is disabled whenever Chip RAM or chip registers are being selected.

Automatic bus timeout can be disabled altogether by writing a 1 to bit 0 of the 8-bit register at $00DE0001. After a RESET, this bit is automatically set to 0 (timeout enabled).



WRITE: 0 = DSACK (9 uSecs) (default)
1 = BERR (250 mSecs)
READ: 0 = Bus did not time out
1 = Bus timed out (reset after read)

WRITE: 0 = Timeout enabled (default)
1 = Timout disabled

READ: 0 = Power has not cycled
1 = Power has cycled
WRITE: same

Figure 6-29. Bus Timeout

ECLK Clock

The ECLK signal is generated in GARY. It is a free running clock whose frequency is 1/10th of the 7M clock. Normally ECLK is low for six 7M clocks, and high for four 7M clocks. However, when the CIAs are accessed, the ECLK high time may be shorter than four 7M clocks. During writes to the CIAs, ECLK is high for only two 7M clocks. During reads ECLK stays high for a minimum of two 7M clocks, and a maximum of four 7M clocks. The frequency of ECLK does not change. If the ECLK high time is shortened during CIA access, the difference is made up by increasing the subsequent ECLK low time. Consequently, it is always ten 7M clocks from one rising edge of ECLK to the next.

The ECLK signal is derived from the onboard 28 megahertz oscillator. It is not derived from the XCLK signal when *XCLKE is true. Therefore, ECLK will not change frequency, even when an external system clock source is used (such as when genlocking the video).

Data Strobes

GARY generates six different data strobe signals. Four relate to 32-bit ports (*UUDS, *UMDS, *LMDS, *LLDS), and the other two to 16-bit ports (*DS, *LDS). GARY decodes SIZ1, SIZ0, A1, A0 and RW signals to determine which of the strobes should be active. Whenever RW indicates the CPU is doing a read, all of the strobes are active. Individual strobes are generated during write cycles.

!LDS = !SIZ0 # SIZ1 # A0 # RW

!UDS = !A0 # RW

!UUDS = (!A0 & !A1) # RW

!UMDS = (!A1 & !SIZ0) # (A0 & !A1) # (!A1 & SIZ1) # RW

!LMDS = (!A1 & !SIZ0 & !SIZ1) # (!A1 & SIZ0 & SIZ1) # (A0 & !A1 & !SIZ0) # (!A0 & A1) # RW

!LLDS = (A0 & SIZ0 & SIZ1) # (!SIZ0 & SIZ1) # (A0 & A1) # (A1 & SIZ1) # RW

AUTOVECTOR

When GARY senses that the CPU is doing an exception acknowledge cycle, it generates the AUTOVECTOR signal to tell the CPU to get the exception vectors from RAM.

!AVEC = !AS & FC2 & FC1 & FC0 & A19 & A18 & A17 & A16

AGNUS Clock Source

For genlocking purposes, an external clock can be fed to AGNUS instead of the internal 28 megahertz clock. The clock (XCLK) and the internal 28 meg clock (28M) are both inputs to GARY. The input signal called *XCLKE controls which signal is fed to AGNUS (via the output called AGCLK). When *XCLKE is low, XCLK is output to AGNUS.

!AGCLK = (XCLKE & !28M) # (!XCLKE & !XCLK)

System Reset Logic

GARY controls reset from two different sources. The first is during powerup. The input line called *PWRUP should be kept low via external circuitry until VCC has become stable. The rising edge of *POWERUP causes bit 0 of an 8-bit register at 00DE0002 to be set. The *RESET output is held low for approximately 250 msecs after *PWRUP goes high. This bit can be checked by software to determine what type of reset occurred. The bit can only be reset by writing a 0 back to it (you could just as easily set this bit in order to make the next reset look like a powerup).

The second source of a rest comes from the keyboard. If the input called *KBCLK is held low for at least 60 msecs, the *RESET output will then go low, and will remain low for approximately 250 msecs after *KBCLK goes high again.

System Interrupt Control

Individual system interrupts are controlled by writing to the INTENA register in PAULA. Since this register resides on the chip bus, the CPU is subject to synchronization delays when attempting to access it. Therefore, an alternate method for shutting off ALL of the interrupts in the system is provided in GARY (GARY actually provides only the bit that can be written to — the actual control is done externally in a PAL). The INTENA register in PAULA is located at the offset of $09A. The chip registers occupy only 4K of address space. Consequently, they are 'shadowed' in four 4K chunks from $DFC000 to $DFF000. The 16-bit register in GARY to control interrupts is also located at the offset of $09A, but is selected in the range from $DF8000 to $DFB000 (this register is shadowed at each of the 4K chunks as well). Wiring a 0 to bit 15 of this register will disable ALL of the interrupts going to the CPU. They are re-enabled by writing a 1 to the bit again (the bit is set after a RESET).

Physical Requirements

Marking

Devices shall be marked with Commodore part number plus a copyright notice as follows:
© 1989 CBM.

Packaging

The interconnected circuitry shall be contained in a standard 84-pin Plastic Leaded Chip Carrier with external dimensions as shown in Figure 6-23.

Process Qualification Tests

Integrated circuits supplied to the requirements of this specification shall meet the requirements of Engineering Policy No. 1.02.008. Supporting documentation shall be supplied by vendor upon request.

Environmental Test Conditions

Devices shall comply with the following environmental resistance tests per Commodore Engineering Policy 1.02.007.

1. Temperature/humidity (85° C and 85% RH non-condensing) for 168 hours
2. Operating life (1000 hours at 70° C ambient temperature)
3. Solderability per MIL-STD-883, Method 2003
4. Pressure cooker (15 psig, 120° C, and 100% RH for 24 hours)
5. Solvent resistance per MIL-STD-883, Method 2015, using water and trichloroethane
6. Solder temperature resistance (250° C for five seconds)

Note Devices shall meet this specification's operating performance requirements after the above tests are completed.

Minimum Acceptance Level

The minimum acceptance level of any lot shall be an AQL of 0.65 as defined by MIL-STD 105 single sampling techniques.

Age of Devices

Unit shall be rejected if EIA Date Code indicates an age of three (3) or more years.