Miniproject 1

Luke Nonas-Hunter

September 2023

All the files for this miniproject and be found on GitHub: `https://github.com/nonas-hunter/ENGR3426-MADVLSI/tree/main/miniproject_01`

1 Schematic Capture and Simulation

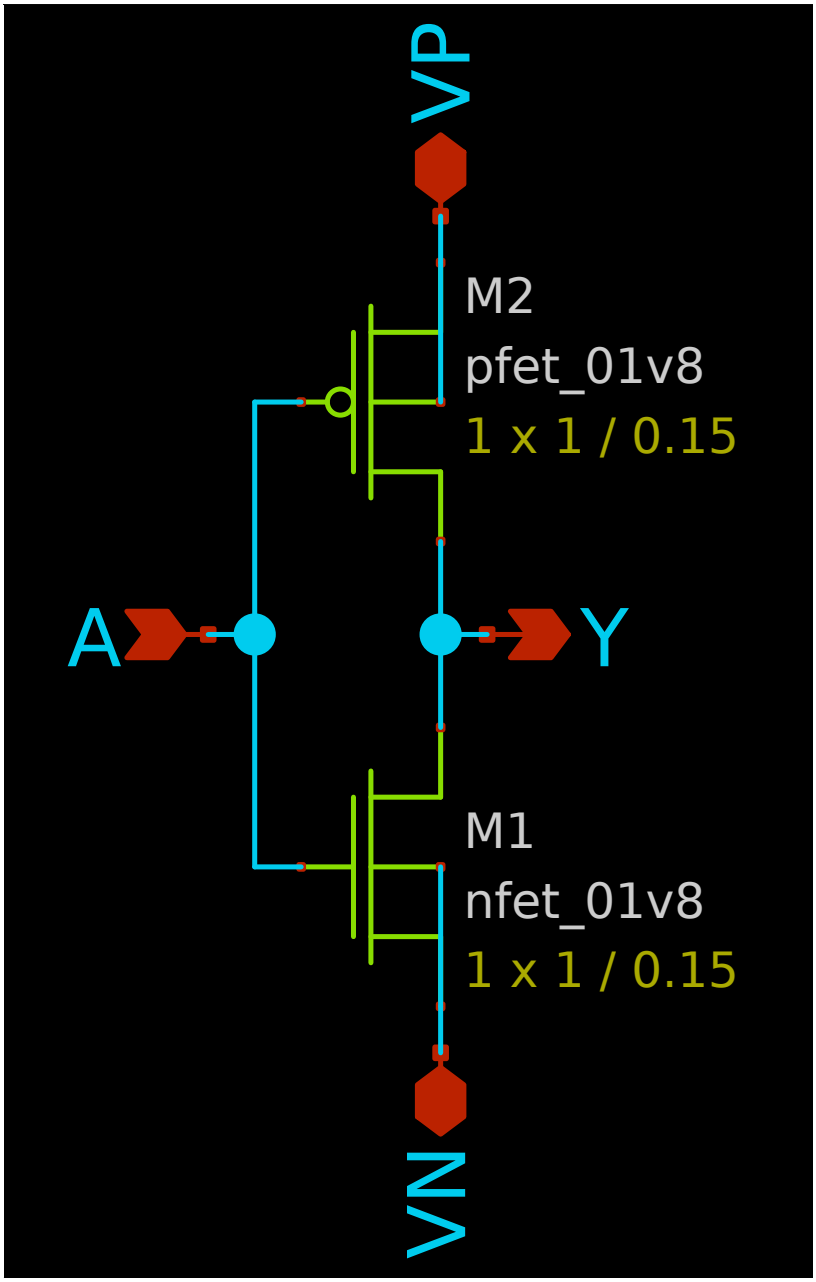

Figure 1: Xschem schematic of an INVERTER.

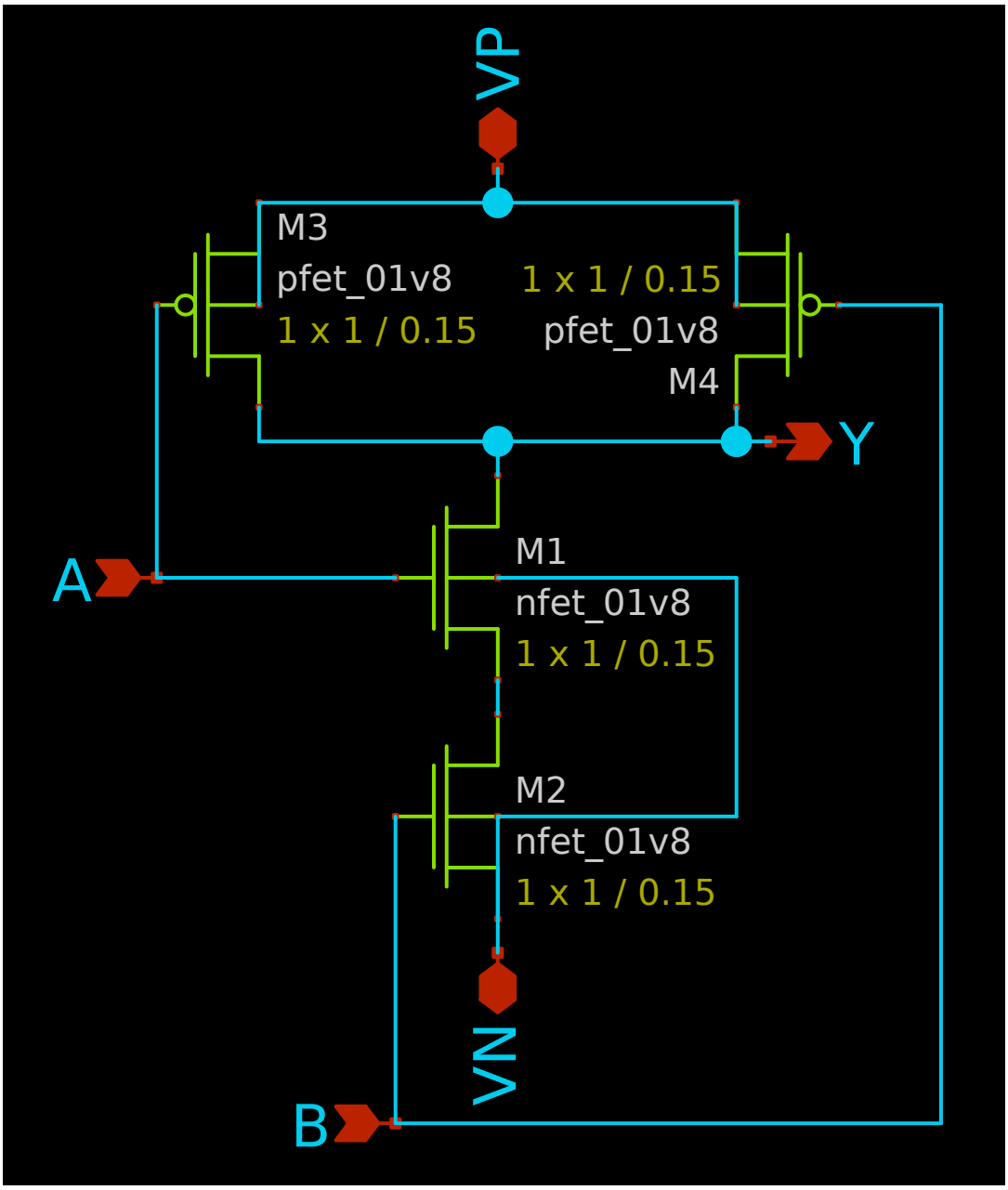

Figure 2: Xschem schematic of a two-input NAND gate.

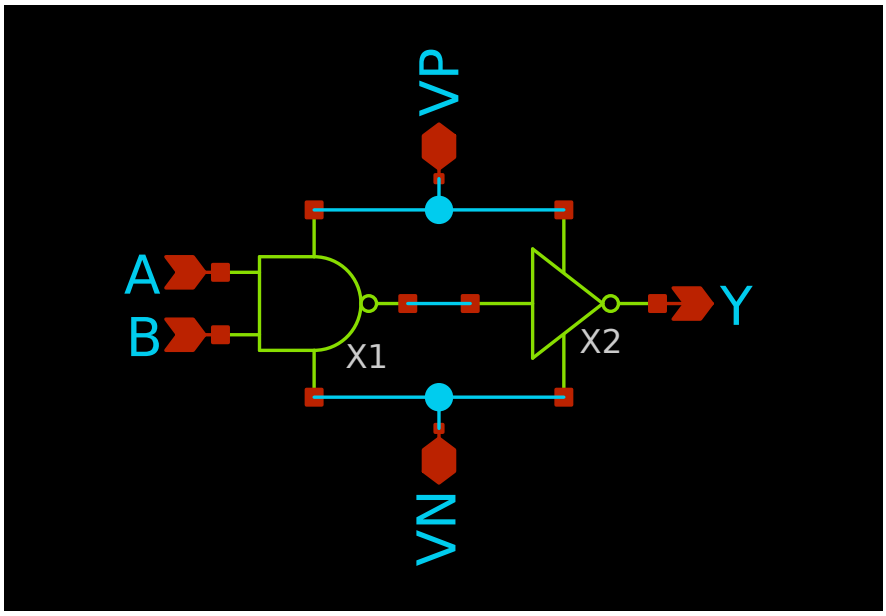

Figure 3: Xschem schematic of a two-input and gate made from the INVERTER cell (Figure 1) and the NAND gate cell (Figure 2).

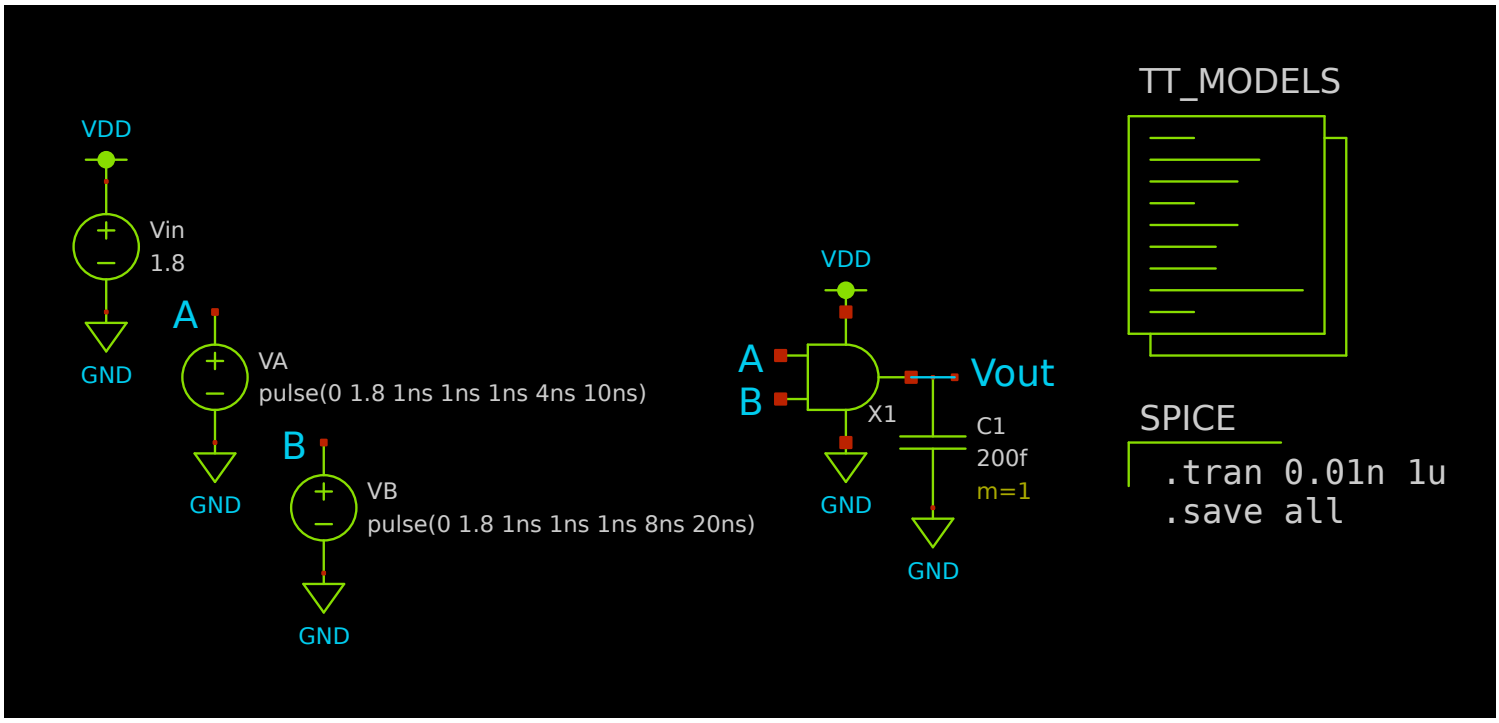

Figure 4: Xschem schematic of the simulation test harness for the AND gate (Figure 3).

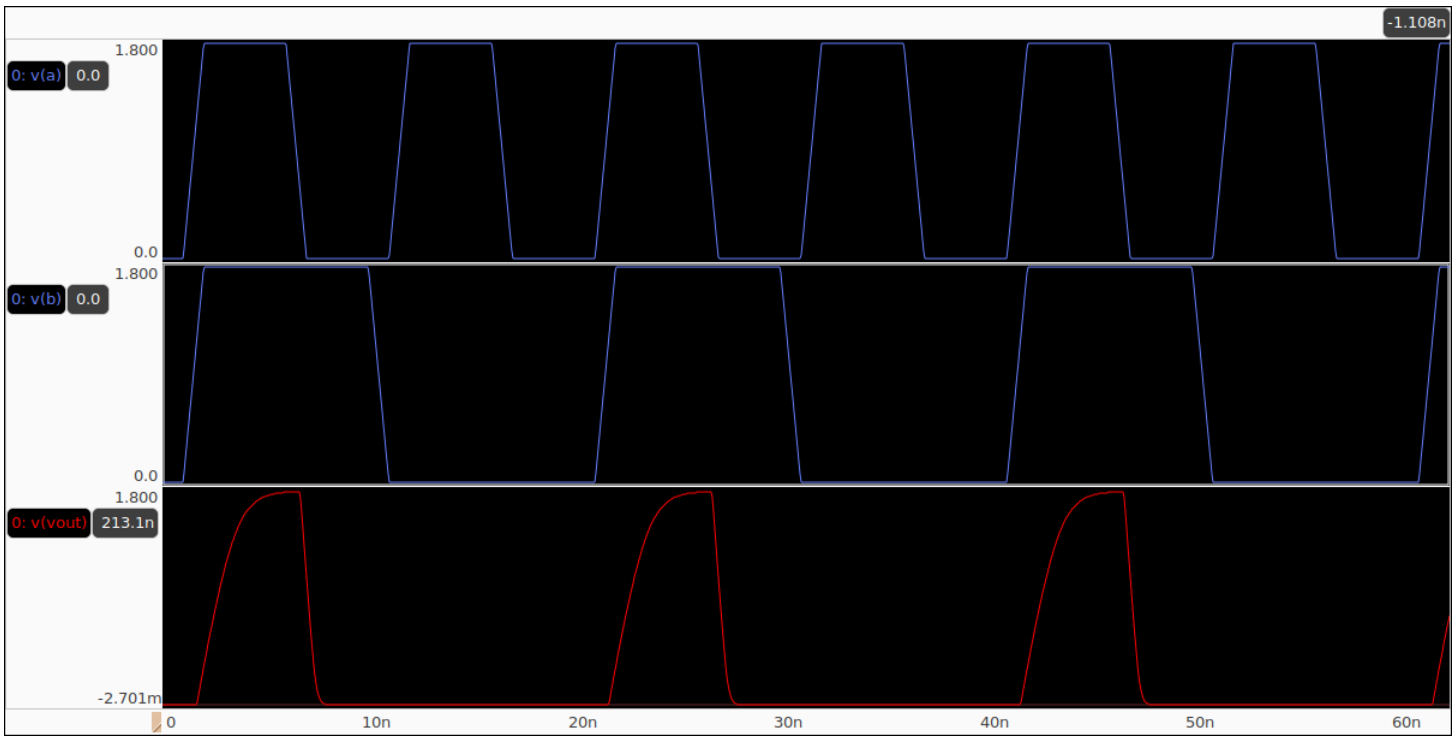

Figure 5: Ngspice simulation results from the Xschem simulation test harness schematic shown in Figure 4.

2 Layout Design

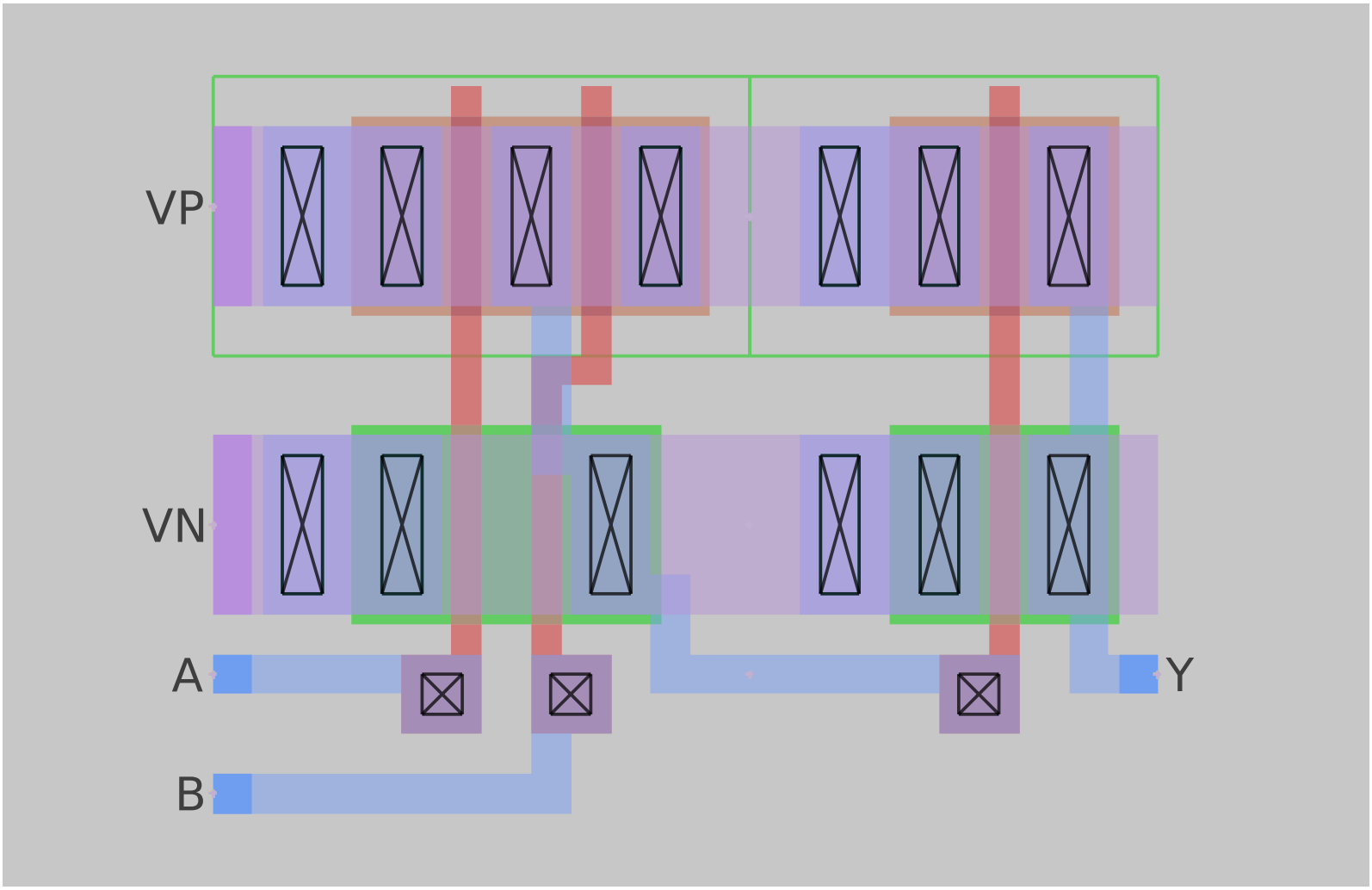

Figure 6: Top-level cell layout of a two-input AND gate. The schematic that this layout is based on can be seen in Figure 3.

3 Layout Versus Schematic

The following text is the output (comp.out) from using Netgen to compare the netlist generated from the Xschem schematic of the two-input AND gate cell (Figure 3) and the netlist generated from the MagicVLSI layout of the two-input AND gate cell (Figure 6).

```
1
2 Circuit 1 cell sky130_fd_pr__pfet_01v8 and Circuit 2 cell sky130_fd_pr__pfet_01v8 are
  ↪ black boxes.
3 Equate elements:  no current cell.
4 Device classes sky130_fd_pr__pfet_01v8 and sky130_fd_pr__pfet_01v8 are equivalent.
5
6 Circuit 1 cell sky130_fd_pr__nfet_01v8 and Circuit 2 cell sky130_fd_pr__nfet_01v8 are
  ↪ black boxes.
```

```
Equate elements:  no current cell.
Device classes sky130_fd_pr__nfet_01v8 and sky130_fd_pr__nfet_01v8 are equivalent.

Subcircuit summary:
Circuit 1: inverter                        |Circuit 2: inverter
-------------------------------------------|-------------------------------------------
sky130_fd_pr__pfet_01v8 (1)                |sky130_fd_pr__pfet_01v8 (1)
sky130_fd_pr__nfet_01v8 (1)                |sky130_fd_pr__nfet_01v8 (1)
Number of devices: 2                       |Number of devices: 2
Number of nets: 4                          |Number of nets: 4
-----------------------------------------------------------------------------------------
Netlists match uniquely.

Subcircuit pins:
Circuit 1: inverter                        |Circuit 2: inverter
-------------------------------------------|-------------------------------------------
Y                                          |Y
A                                          |A
VN                                         |VN
VP                                         |VP
-----------------------------------------------------------------------------------------
Cell pin lists are equivalent.
Device classes inverter and inverter are equivalent.

Subcircuit summary:
Circuit 1: nand2                           |Circuit 2: nand2
-------------------------------------------|-------------------------------------------
sky130_fd_pr__nfet_01v8 (2)                |sky130_fd_pr__nfet_01v8 (2)
sky130_fd_pr__pfet_01v8 (2)                |sky130_fd_pr__pfet_01v8 (2)
Number of devices: 4                       |Number of devices: 4
Number of nets: 6                          |Number of nets: 6
-----------------------------------------------------------------------------------------
Netlists match uniquely.

Subcircuit pins:
Circuit 1: nand2                           |Circuit 2: nand2
-------------------------------------------|-------------------------------------------
VP                                         |VP
A                                          |B **Mismatch**
B                                          |A **Mismatch**
Y                                          |Y
VN                                         |VN
-----------------------------------------------------------------------------------------
Cell pin lists for nand2 and nand2 altered to match.
Device classes nand2 and nand2 are equivalent.

Subcircuit summary:
Circuit 1: and2_magic.spice                |Circuit 2: and2_xschem.spice
-------------------------------------------|-------------------------------------------
inverter (1)                               |inverter (1)
nand2 (1)                                  |nand2 (1)
Number of devices: 2                       |Number of devices: 2
Number of nets: 6                          |Number of nets: 6
-----------------------------------------------------------------------------------------
```

```
Netlists match uniquely.
Cells have no pins;  pin matching not needed.
Device classes and2_magic.spice and and2_xschem.spice are equivalent.

Final result: Circuits match uniquely.
.
```