

Miniproject 1

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All the files for this miniproject and be found on GitHub: https://github.com/nonas-hunter/ENGR3426-MADVLSI/tree/main/miniproject_01

1 Schematic Capture and Simulation

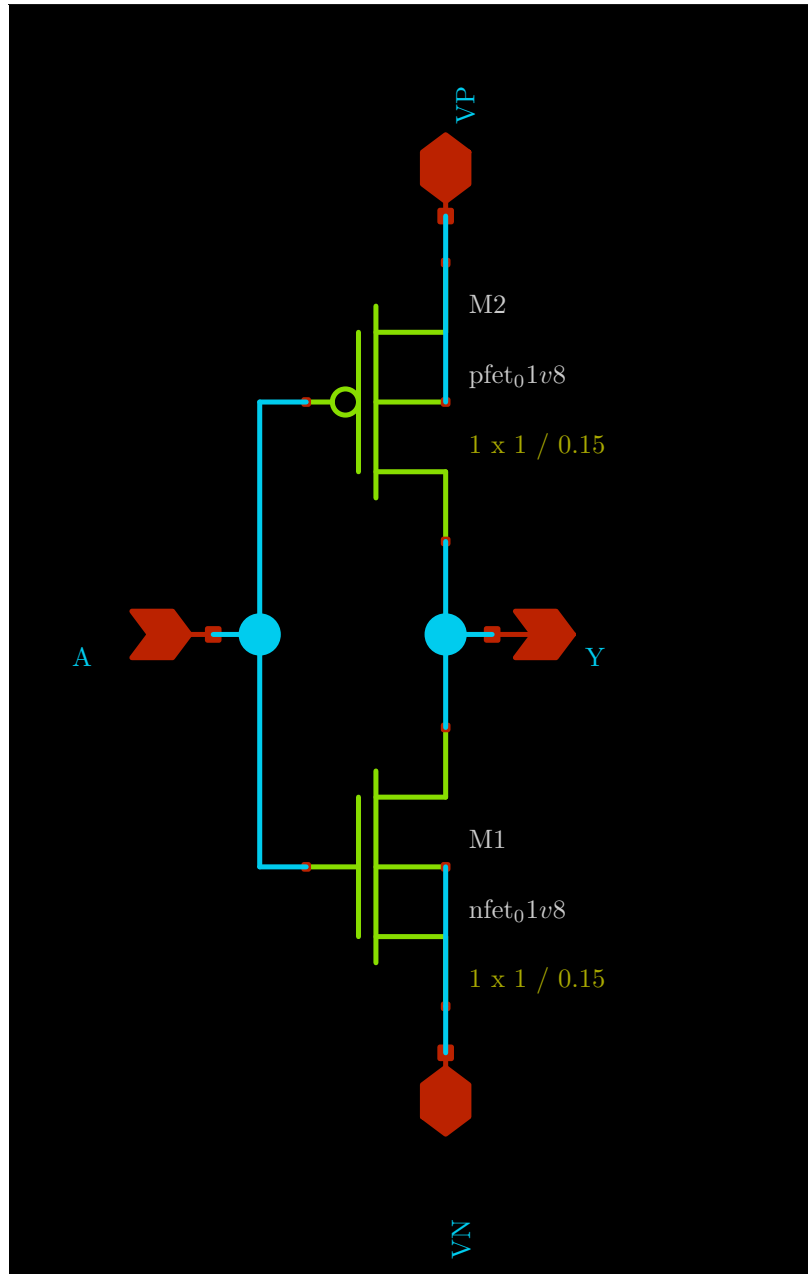


Figure 1: Xschem schematic of an INVERTER.

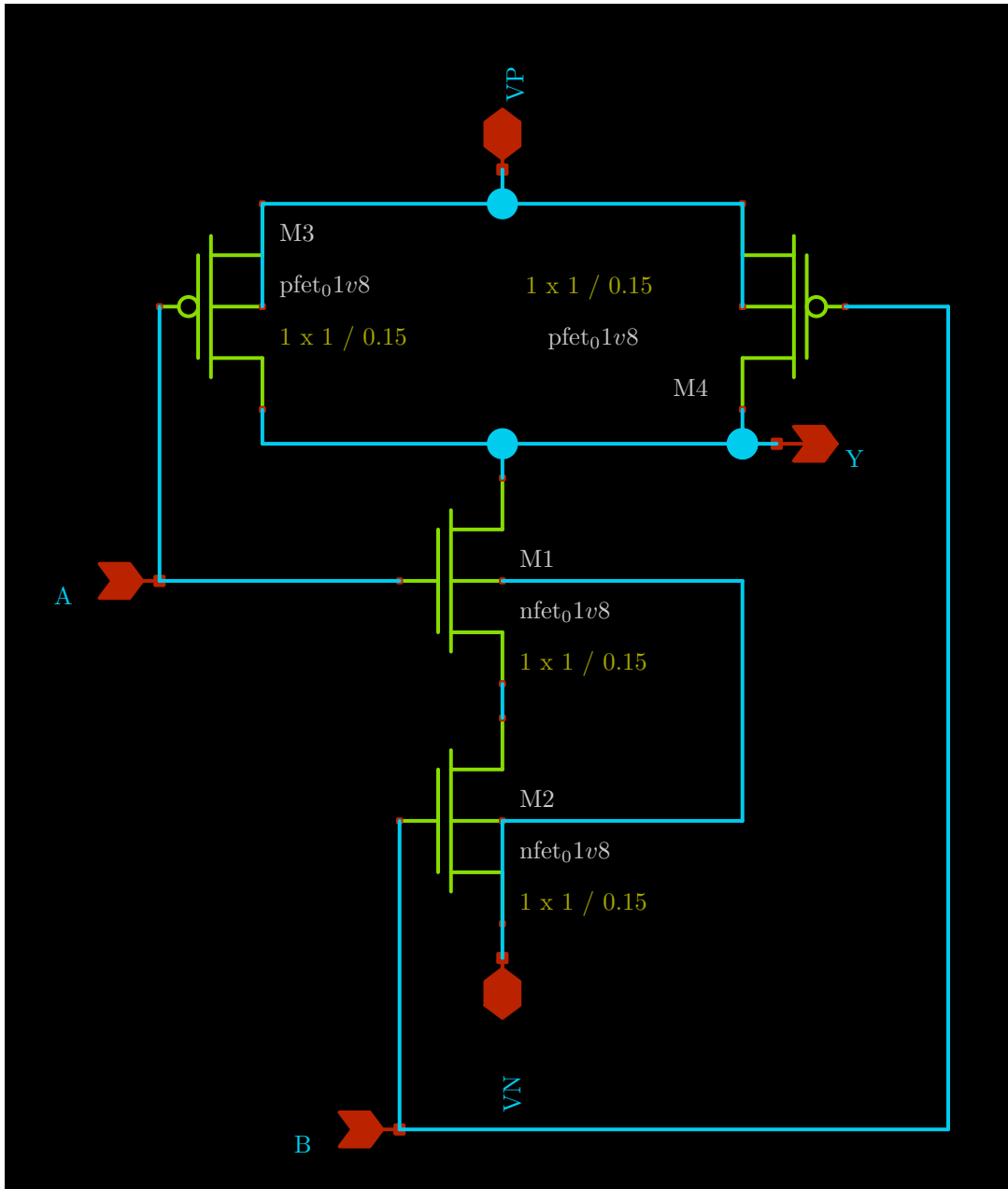


Figure 2: Xschem schematic of a two-input NAND gate.

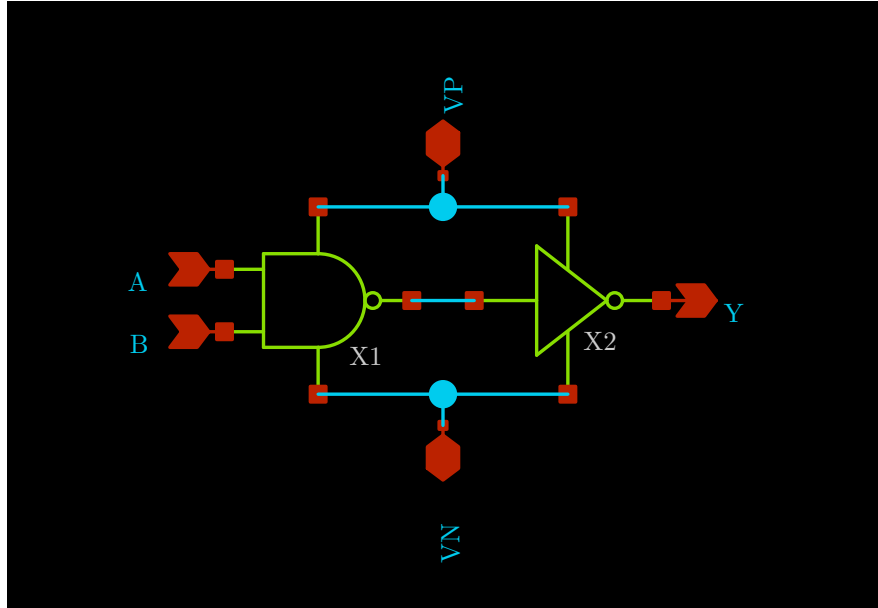


Figure 3: Xschem schematic of a two-input AND gate made from the INVERTER cell (Figure 1) and the NAND gate cell (Figure 2).

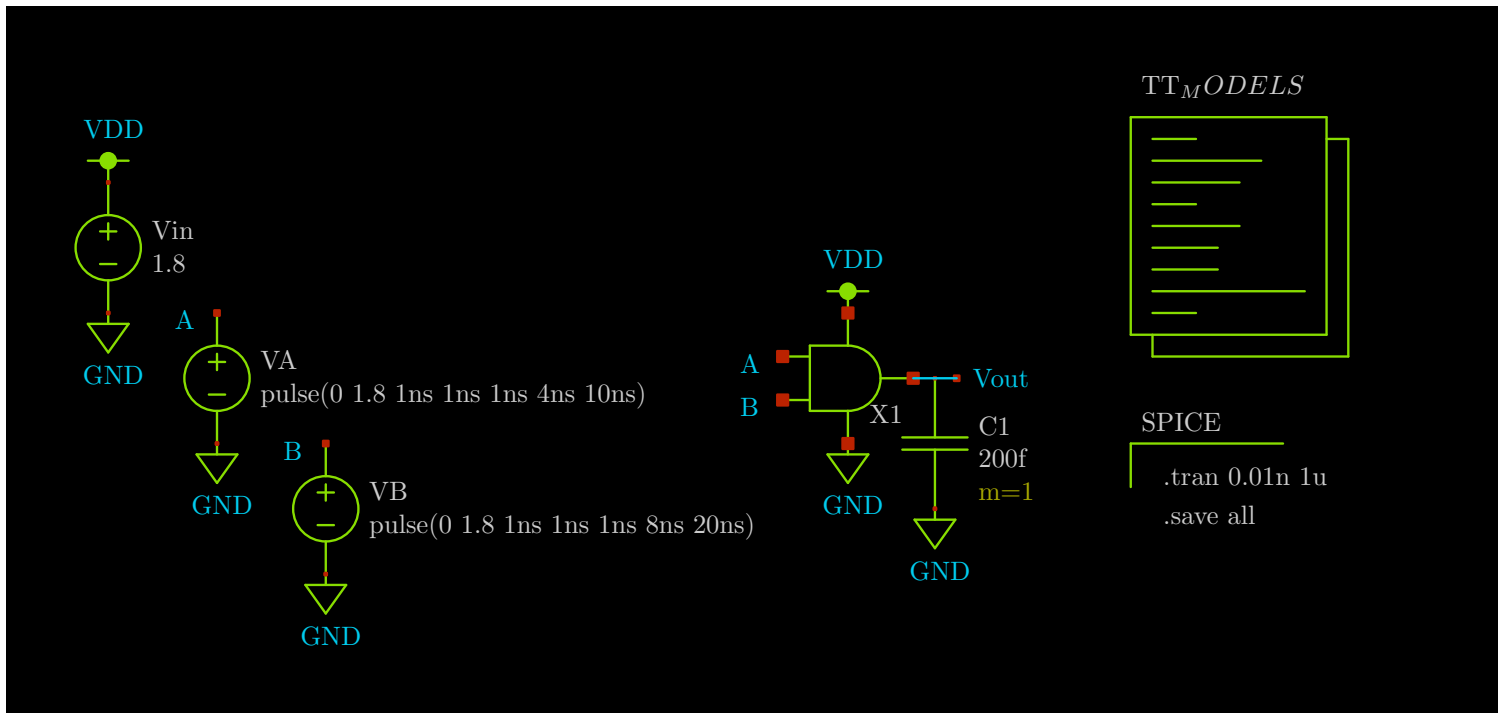


Figure 4: Xschem schematic of the simulation test harness for the AND gate (Figure 3).

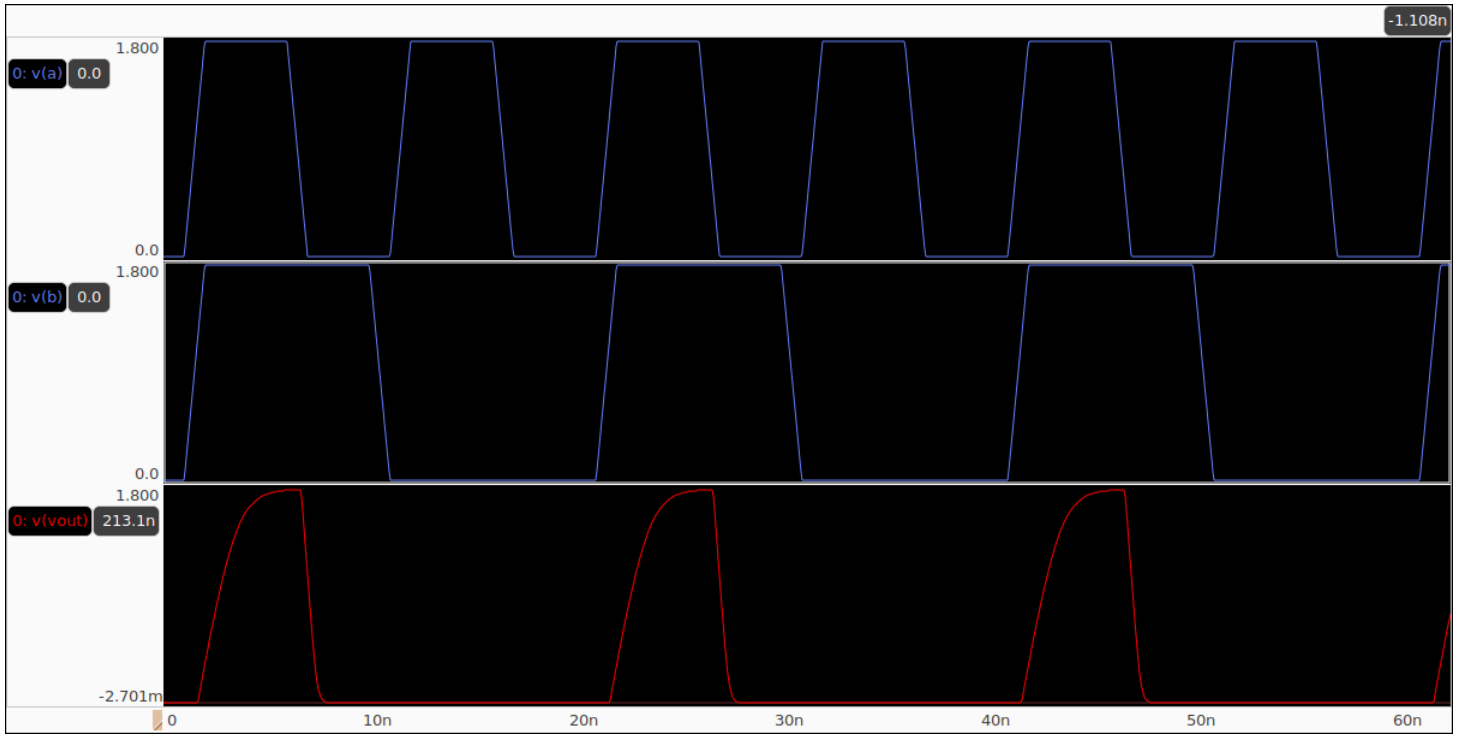


Figure 5: Ngspice simulation results from the Xschem simulation test harness schematic shown in Figure 4.

2 Layout Design

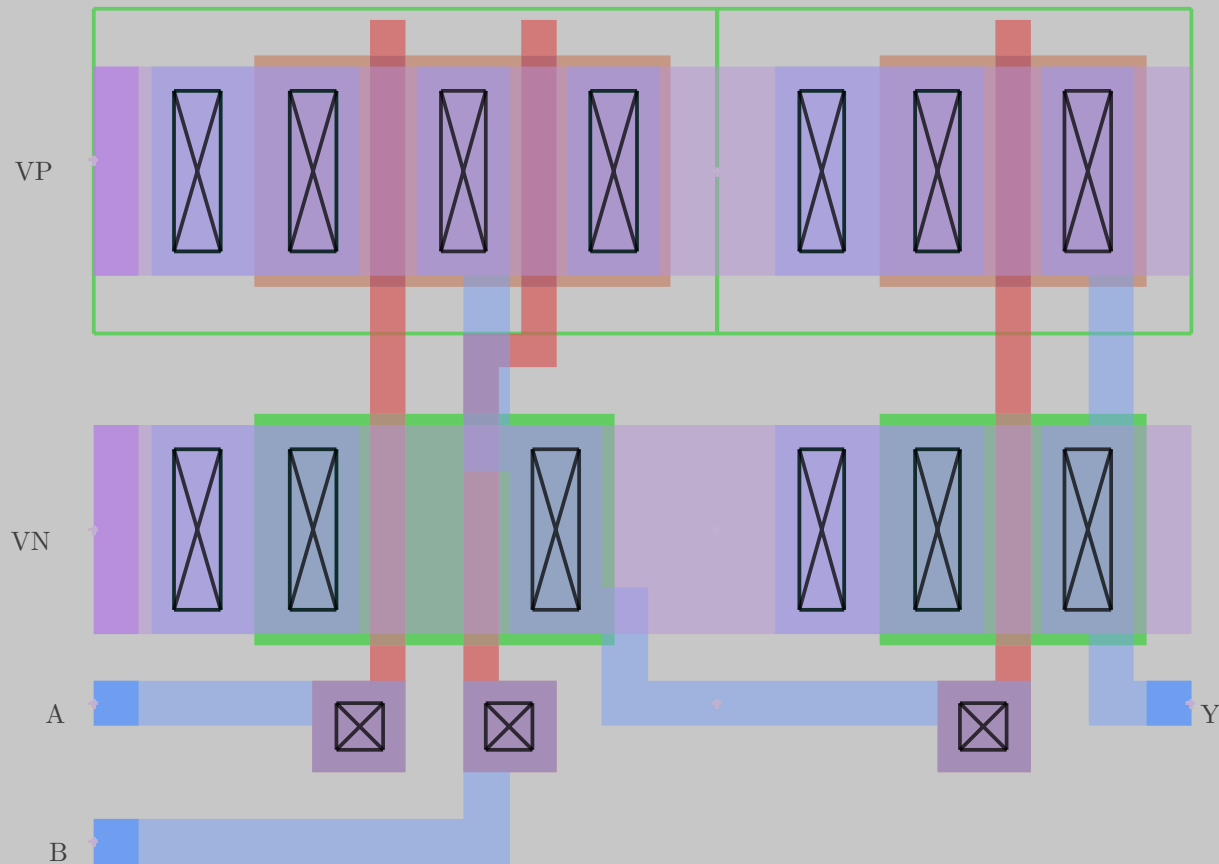


Figure 6: Top-level cell layout of a two-input AND gate. The schematic that this layout is based on can be seen in Figure 3.

3 Layout Versus Schematic

The following text is the output (comp.out) from using Netgen to compare the netlist generated from the Xschem schematic of the two-input AND gate cell (Figure 3) and the netlist generated from the MagicVLSI layout of the two-input AND gate cell (Figure 6).

```

1
2 Circuit 1 cell sky130_fd_pr__pfet_01v8 and Circuit 2 cell sky130_fd_pr__pfet_01v8 are
  ↳ black boxes.
3 Equate elements: no current cell.
4 Device classes sky130_fd_pr__pfet_01v8 and sky130_fd_pr__pfet_01v8 are equivalent.
5
6 Circuit 1 cell sky130_fd_pr__nfet_01v8 and Circuit 2 cell sky130_fd_pr__nfet_01v8 are
  ↳ black boxes.
```

```

7  Equate elements:  no current cell.
8  Device classes sky130_fd_pr__nfet_01v8 and sky130_fd_pr__nfet_01v8 are equivalent.
9
10 Subcircuit summary:
11 Circuit 1: inverter                                |Circuit 2: inverter
12 -----|-----
13 sky130_fd_pr__pfet_01v8 (1)                        |sky130_fd_pr__pfet_01v8 (1)
14 sky130_fd_pr__nfet_01v8 (1)                        |sky130_fd_pr__nfet_01v8 (1)
15 Number of devices: 2                                |Number of devices: 2
16 Number of nets: 4                                  |Number of nets: 4
17 -----|-----
18 Netlists match uniquely.
19
20 Subcircuit pins:
21 Circuit 1: inverter                                |Circuit 2: inverter
22 -----|-----
23 Y                                                    |Y
24 A                                                    |A
25 VN                                                    |VN
26 VP                                                    |VP
27 -----|-----
28 Cell pin lists are equivalent.
29 Device classes inverter and inverter are equivalent.
30
31 Subcircuit summary:
32 Circuit 1: nand2                                    |Circuit 2: nand2
33 -----|-----
34 sky130_fd_pr__nfet_01v8 (2)                        |sky130_fd_pr__nfet_01v8 (2)
35 sky130_fd_pr__pfet_01v8 (2)                        |sky130_fd_pr__pfet_01v8 (2)
36 Number of devices: 4                                |Number of devices: 4
37 Number of nets: 6                                  |Number of nets: 6
38 -----|-----
39 Netlists match uniquely.
40
41 Subcircuit pins:
42 Circuit 1: nand2                                    |Circuit 2: nand2
43 -----|-----
44 VP                                                    |VP
45 A                                                    |B **Mismatch**
46 B                                                    |A **Mismatch**
47 Y                                                    |Y
48 VN                                                    |VN
49 -----|-----
50 Cell pin lists for nand2 and nand2 altered to match.
51 Device classes nand2 and nand2 are equivalent.
52
53 Subcircuit summary:
54 Circuit 1: and2_magic.spice                          |Circuit 2: and2_xschem.spice
55 -----|-----
56 inverter (1)                                         |inverter (1)
57 nand2 (1)                                             |nand2 (1)
58 Number of devices: 2                                |Number of devices: 2
59 Number of nets: 6                                  |Number of nets: 6
60 -----|-----

```

```
61 Netlists match uniquely.  
62 Cells have no pins; pin matching not needed.  
63 Device classes and2_magic.spice and and2_xschem.spice are equivalent.  
64  
65 Final result: Circuits match uniquely.  
66 .
```