WM8994

Multi-Channel Audio Hub CODEC for Smartphones

DESCRIPTION

The WM8994 is a highly integrated ultra-low power hi-fi CODEC designed for smartphones and other portable devices rich in multimedia features.

An integrated stereo class D/AB speaker driver and class W headphone driver minimize power consumption during audio playback.

The device requires only two voltage supplies, with all other internal supply rails generated from integrated LDOs.

Stereo full duplex asynchronous sample rate conversion and multi-channel digital mixing combined with powerful analogue mixing allow the device to support a huge range of different architectures and use cases.

A fully programmable parametric EQ provides speaker compensation and a dynamic range controller can be used in the ADC or DAC paths for maintaining a constant signal level, maximizing loudness and protecting speakers against overloading and clipping.

A smart digital microphone interface provides power regulation, a low jitter clock output and decimation filters for up to four digital microphones. A MIC activity detect with interrupt is available.

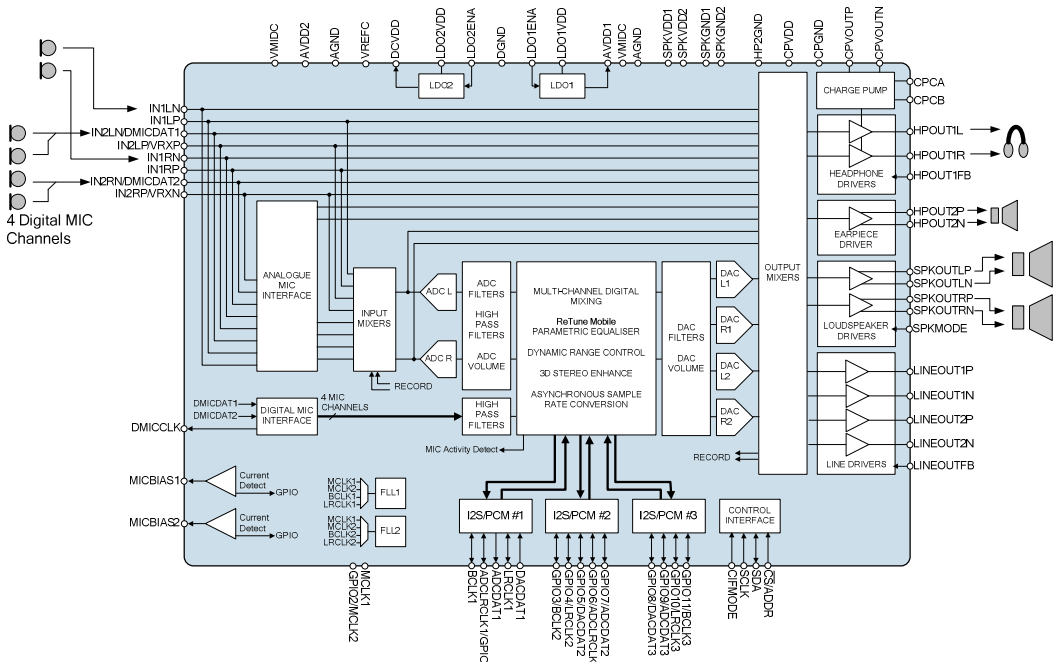
Active ground loop noise rejection and DC offset correction help prevent pop noise and suppress ground noise on the headphone outputs.

FEATURES

- Hi-Fi 24-bit 4-channel DAC and 2-channel ADC
- 100dB SNR during DAC playback ('A' weighted)
- Smart MIC interface
  - Power, clocking and data input for up to four digital MICs
  - High performance analogue MIC interface
  - MIC activity monitor & interrupt allows processor to sleep
- 1W stereo / 2W mono class D/AB speaker driver
- Capless Class W headphone drivers
  - Integrated charge pump
  - 6mW total power for DAC playback to headphones
- 4 Line outputs (single-ended or differential)
- BTL Earpiece driver
- Digital audio interfaces for multi-processor architecture
  - Asynchronous stereo duplex sample rate conversion
  - Powerful mixing and digital loopback functions
- ReTune™ Mobile 5-band, 6-channel parametric EQ
- Programmable dynamic range controller
- Dual FLL provides all necessary clocks
  - Self-clocking modes allow processor to sleep
  - All standard sample rates from 8kHz to 96kHz
- Active noise reduction circuits
  - DC offset correction removes pops and clicks
  - Ground loop noise cancellation
- Integrated LDO regulators
- 72-ball W-CSP package (4.511 x 4.023 x 0.7mm)

APPLICATIONS

- Smartphones and music phones
- Portable navigation



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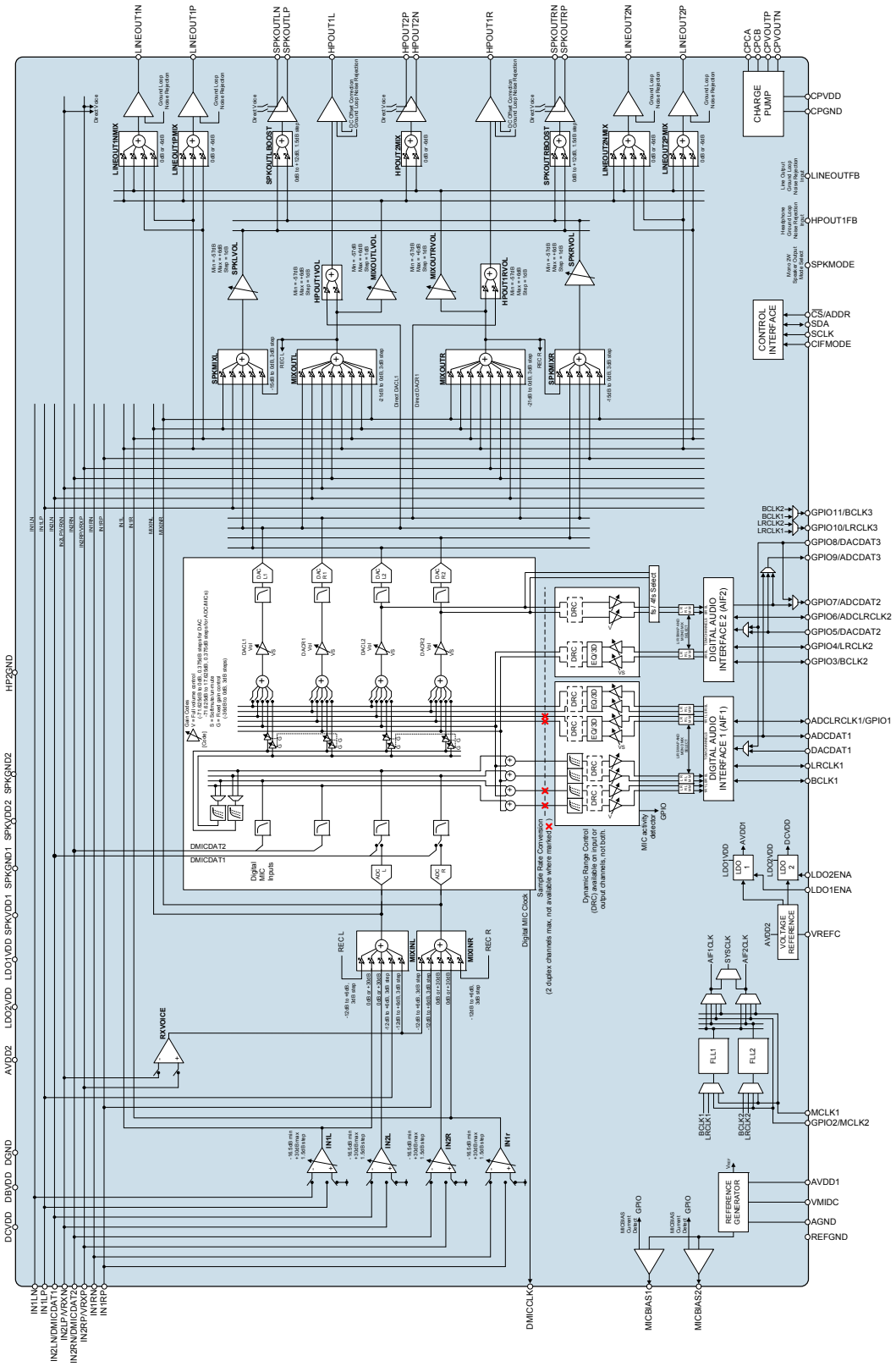
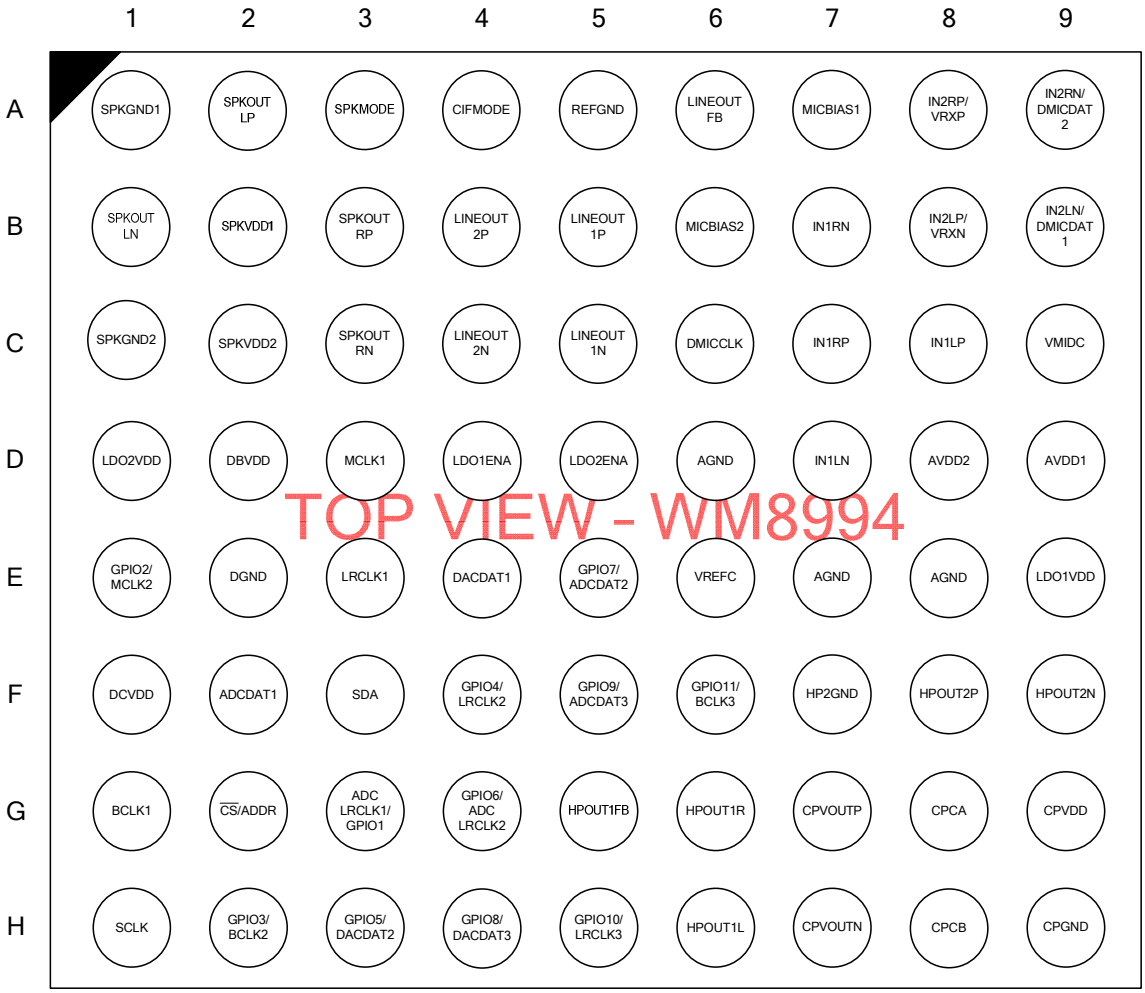
BLOCK DIAGRAM



PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8994ECS/RV	-40°C to +85°C	72-ball W-CSP (Pb-free, Tape and reel)	MSL1	260°C

Note:
Reel quantity = 3500

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
A1	SPKGND1	Supply	Ground for speaker driver (Return path for SPKVDD1)
A2	SPKOUTLP	Supply	Left speaker positive output
A3	SPKMODE	Digital Input	2W Mono/1W Stereo speaker mode select
A4	CIFMODE	Digital Input	Selects 2-wire or 3/4-wire control interface mode
A5	REFGND	Supply	Analogue ground
A6	LINEOUTFB	Analogue Input	Line output ground loop noise rejection feedback
A7	MICBIAS1	Analogue Output	Microphone bias 1
A8	IN2RP/VRXP	Analogue Input	Left channel line input / Left channel positive differential MIC input / Mono differential positive input (RXVOICE +)
A9	IN2RN/ DMICDAT2	Analogue Input / Digital Input	Right channel line input / Right channel negative differential MIC input /
B1	SPKOUTLN	Analogue Output	Left speaker negative output
B2	SPKVDD1	Analogue Output	Supply for speaker driver 1 (Left channel)
B3	SPKOUTRP	Analogue Output	Right speaker positive output
B4	LINEOUT2P	Analogue Output	Positive mono line output / Positive left line output
B5	LINEOUT1P	Analogue Output	Positive mono line output / Positive left line output
B6	MICBIAS2	Analogue Output	Microphone bias 2
B7	IN1RN	Analogue Input	Right channel single-ended MIC input / Right channel negative differential MIC input
B8	IN2LP/VRXN	Analogue Input	Left channel line input / Left channel positive differential MIC input / Mono differential negative input (RXVOICE -)
B9	IN2LN/ DMICDAT1	Analogue Input / Digital Input	Left channel line input / Left channel negative differential MIC input / Digital MIC data input 1
C1	SPKGND2	Supply	Ground for speaker driver (Return path for SPKVDD2)
C2	SPKVDD2	Supply	Supply for speaker driver 2 (Right channel)
C3	SPKOUTRN	Analogue Output	Right speaker negative output
C4	LINEOUT2N	Analogue Output	Negative mono line output / Positive left or right line output
C5	LINEOUT1N	Analogue Output	Negative mono line output / Positive left or right line output
C6	DMICCLK	Digital Output	Digital MIC clock output
C7	IN1RP	Analogue Input	Right channel line input / Right channel positive differential MIC input
C8	IN1LP	Analogue Input	Left channel line input / Left channel positive differential MIC input
C9	VMIDC	Analogue Output	Midrail voltage decoupling capacitor
D1	LDO2VDD	Supply	Supply for LDO2
D2	DBVDD	Supply	Digital buffer (I/O) supply
D3	MCLK1	Digital Input	Master clock 1
D4	LDO1ENA	Digital Input	Enable pin for LDO1
D5	LDO2ENA	Digital Input	Enable pin for LDO2
D6	AGND	Supply	Analogue ground (Return path for AVDD1)
D7	IN1LN	Analogue Input	Left channel single-ended MIC input / Left channel negative differential MIC input
D8	AVDD2	Supply	Bandgap reference, analogue class D and FLL supply
D9	AVDD1	Supply / Analogue Output	Analogue core supply / LDO1 Output
E1	GPIO2/ MCLK2	Digital Input	General Purpose pin GPI 2 / Master clock 2
E2	DGND	Supply	Digital ground (Return path for DCVDD and DBVDD)
E3	LRCLK1	Digital Input / Output	Audio interface 1 left / right clock

PIN NO	NAME	TYPE	DESCRIPTION
E4	DACDAT1	Digital Input	Audio interface 1 DAC digital audio data
E5	GPIO7/ ADCDAT2	Digital Input / Output	General Purpose pin GPIO 7 / Audio interface 2 ADC digital audio data
E6	VREFC	Analogue Output	Bandgap reference decoupling capacitor
E7	AGND	Supply	Analogue ground (Return path for AVDD1)
E8	AGND	Supply	Analogue ground (Return path for AVDD1)
E9	LDO1VDD	Supply	Supply for LDO1
F1	DCVDD	Supply / Analogue Output	Digital core supply / LDO2 output
F2	ADCDAT1	Digital Output	Audio interface 1 ADC digital audio data
F3	SDA	Digital Input / Output	Control interface data input / 2-wire acknowledge output
F4	GPIO4/ LRCLK2	Digital Input / Output	General Purpose pin GPIO 4 / Audio interface 2 left / right clock
F5	GPIO9/ ADCDAT3	Digital Input / Output	General Purpose pin GPIO 9 / Audio interface 3 ADC digital audio data
F6	GPIO11/ BCLK3	Digital Input / Output	General Purpose pin GPIO 11 / Audio interface 3 bit clock
F7	HP2GND	Supply	Analogue ground
F8	HPOUT2P	Analogue Output	Earpiece speaker non-inverted output
F9	HPOUT2N	Analogue Output	Earpiece speaker inverted output
G1	BCLK1	Digital Input / Output	Audio interface 1 bit clock
G2	$\overline{CS}$/ADDR	Digital Input	3-/4-wire (SPI) chip select or 2-wire (I2C) address select
G3	ADCLRCLK1/ GPIO1	Digital Input / Output	Audio interface 1 ADC left / right clock / General Purpose pin GPIO 1/ Control interface data output
G4	GPIO6/ ADCLRCLK2	Digital Input / Output	General Purpose pin GPIO 6 / Audio interface 2 ADC left / right clock
G5	HPOUT1FB	Analogue Input	HPOUT1L and HPOUT1R ground loop noise rejection feedback
G6	HPOUT1R	Analogue Output	Right headphone output
G7	CPVOUTP	Analogue Output	Charge pump positive supply decoupling pin (HPOUT1L, HPOUT1R)
G8	CPCA	Analogue Output	Charge pump fly-back capacitor pin
G9	CPVDD	Supply	Charge pump supply
H1	SCLK	Digital Input	Control interface clock input
H2	GPIO3/ BCLK2	Digital Input / Output	General Purpose pin GPIO 3 / Audio interface 2 bit clock
H3	GPIO5/ DACDAT2	Digital Input / Output	General Purpose pin GPIO 5 / Audio interface 2 DAC digital audio data
H4	GPIO8/ DACDAT3	Digital Input / Output	General Purpose pin GPIO 8 / Audio interface 3 DAC digital audio data
H5	GPIO10/ LRCLK3	Digital Input / Output	General Purpose pin GPIO 10 / Audio interface 3 left / right clock
H6	HPOUT1L	Analogue Output	Left headphone output
H7	CPVOUTN	Analogue Output	Charge pump negative supply decoupling pin (HPOUT1L, HPOUT1R)
H8	CPCB	Analogue Output	Charge pump fly-back capacitor pin
H9	CPGND	Supply	Charge pump ground (Return path for CPVDD)

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages (AVDD1, DBVDD)	-0.3V	+4.5V
Supply voltages (AVDD2, DCVDD, LDO2VDD)	-0.3V	+2.5V
Supply voltages (CPVDD)	-0.3V	+2.2V
Supply voltages (SPKVDD1, SPKVDD2, LDO1VDD)	-0.3V	+7.0V
Voltage range digital inputs	DGND -0.3V	DBVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD1 +0.3V
Operating temperature range, T_A	-40ºC	+85ºC
Junction temperature, T_{JMAX}	-40ºC	+150ºC
Storage temperature after soldering	-65ºC	+150ºC

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD	0.95	1.0	2.0	V
Digital supply range (I/O)	DBVDD	1.62	1.8	3.6	V
Analogue supply 1 range	AVDD1	2.24	3.0	3.3	V
Analogue supply 2 range	AVDD2	1.71	1.8	2.0	V
Charge Pump supply range	CPVDD	1.71	1.8	2.0	V
Speaker supply range	SPKVDD1, SPKVDD2	2.7	5.0	5.5	V
LDO1 supply range	LDO1VDD	2.7	5.0	5.5	V
LDO2 supply range	LDO2VDD	1.71	1.8	2.0	V
Ground	DGND, AGND, CPGND, SPKGND1, SPKGND2, REFGND, HP2GND		0		V

Notes

1. Analogue, digital and speaker grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are completely independent from each other (i.e. not internally connected).
3. AVDD1 must be less than or equal to SPKVDD1 and SPKVDD2.

THERMAL PERFORMANCE

Thermal analysis should be performed in the intended application to prevent the WM8994 from exceeding maximum junction temperature. Several contributing factors affect thermal performance most notably the physical properties of the mechanical enclosure, location of the device on the PCB in relation to surrounding components and the number of PCB layers. Connecting the GND balls through thermal vias and into a large ground plane will aid heat extraction.

Three main heat transfer paths exist to surrounding air as illustrated below in Figure 1:

- Package top to air (radiation).
- Package bottom to PCB (radiation).
- Package balls to PCB (conduction).

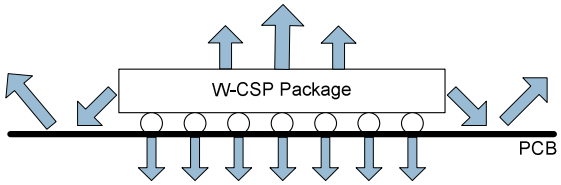


Figure 1 Heat Transfer Paths

The temperature rise T_R is given by $T_R = P_D * \Theta_{JA}$

- P_D is the power dissipated in the device.
- Θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature and is therefore a measure of heat transfer from the die to surrounding air. Θ_{JA} is determined with reference to JEDEC standard JESD51-9.

The junction temperature T_J is given by $T_J = T_A + T_R$, where T_A is the ambient temperature.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Operating temperature range	T_A	-40		85	°C
Operating junction temperature	T_J	-40		125	°C
Thermal Resistance	Θ_{JA}		TBC		°C/W

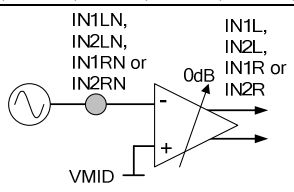
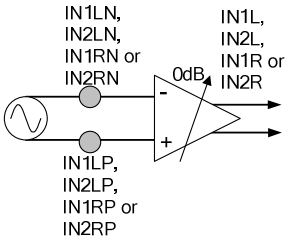
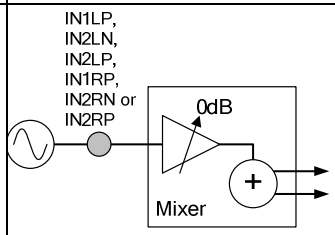
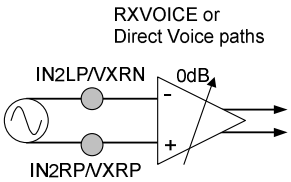
Note:

Junction temperature is a function of ambient temperature and of the device operating conditions. The ambient temperature limits and junction temperature limits must both be observed.

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD2=DBVDD=LDO2VDD=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, LDO1ENA=LDO2ENA=1.8V, DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

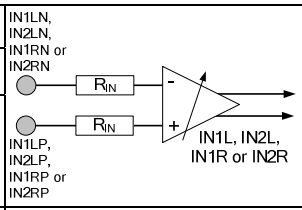
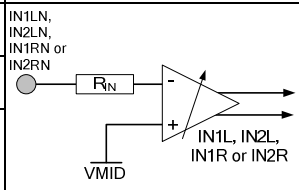
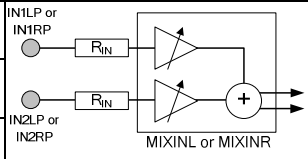
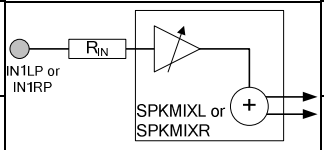
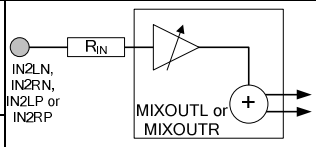
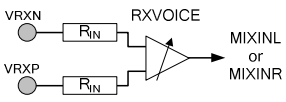
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Analogue Input Pin Maximum Signal Levels (IN1LN, IN1LP, IN2LN, IN2LP, IN1RN, IN1RP, IN2RN, IN2RP)							
A1	Maximum Full-Scale PGA Input Signal Level Note 1,2 and 3	Single-ended PGA input			1.0 0		Vrms dBV
		Differential PGA input			1.0 0		Vrms dBV
A2	Maximum Full-Scale Line Input Signal Level Note 1, 2 and 3	Single-ended Line input to mixers			1.0 0		Vrms dBV
		Differential mono line input on VRXP/VRXN to RXVOICE or Direct Voice paths to speaker outputs or earpiece output			1.0 0		Vrms dBV

Notes:

1. This changes in proportion to AVDD1 (AVDD1/3.0) when AVDD1 is applied with LDO1 enabled.
2. When mixing line inputs, input PGA outputs and DAC outputs the total signal must not exceed 1Vrms (0dBV).
3. A 1.0Vrms differential signal equates to 0.5Vrms/-6dBV per input.

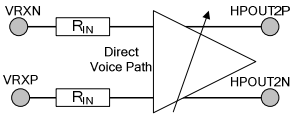
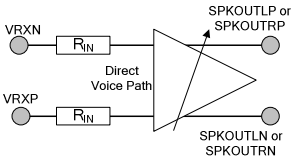
Test Conditions

AVDD2=DBVDD=LDO2VDD=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, LDO1ENA=LDO2ENA=1.8V,
DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Analogue Input Pin Impedances (IN1LN, IN1LP, IN2LN, IN2LP, IN1RN, IN1RP, IN2RN, IN2RP)							
B1	PGA Input Resistance Differential Mode Note 4	PGA Gain = -16.5dB			52.5		kΩ
		PGA Gain = 0dB			25.1		kΩ
		PGA Gain = +30dB			1.3		kΩ
B2	PGA Input Resistance Single-Ended Mode Note 4	PGA Gain = -16.5dB			58.0		kΩ
		PGA Gain = 0dB			36.2		kΩ
		PGA Gain = +30dB			2.5		kΩ
B3	Line Input Resistance Note 4	IN1LP or IN1RP to INMIXL or INMIXR (-12dB)			56.0		kΩ
		IN1LP or IN1RP to INMIXL or INMIXR (0dB)			17.4		kΩ
		IN1LP or IN1RP to INMIXL or INMIXR (+6dB)			9.8		kΩ
		IN1LP to SPKMIXL or IN1RP to SPKMIXR (SPKATTN = -12dB)			88.5		kΩ
		IN1LP to SPKMIXL or IN1RP to SPKMIXR (SPKATTN = 0dB)			26.7		kΩ
		IN2LN, IN2RN, IN2LP or IN2RP to MIXOUTL or MIXOUTR (-21dB)			150.9		kΩ
		IN2LN, IN2RN, IN2LP or IN2RP to MIXOUTL or MIXOUTR (0dB)			18.2		kΩ
		VRXP-VRXN via RXVOICE to MIXINL or MIXINR (Gain = -12dB)			47.7		kΩ
		VRXP-VRXN via RXVOICE to MIXINL or MIXINR (Gain = 0dB)			12.0		kΩ
		VRXP-VRXN via RXVOICE to MIXINL or MIXINR (Gain = +6dB)			6.0		kΩ

Test Conditions

AVDD2=DBVDD=LDO2VDD=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, LDO1ENA=LDO2ENA=1.8V,
DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
		Direct Voice to Earpiece Driver (Gain = -6dB)			33.3		kΩ
		Direct Voice to Earpiece Driver (Gain = 0dB)			16.7		kΩ
		Direct Voice to Speaker Driver (Gain = 0dB)			170.0		kΩ
		Direct Voice to Speaker Driver (Gain = +6dB)			85.2		kΩ
		Direct Voice to Speaker Driver (Gain = +9dB)			60.3		kΩ
		Direct Voice to Speaker Driver (Gain = +12dB)			42.7		kΩ
B4	Input Capacitance	All analogue input pins			TBD		pF

Note 4: Input resistance will be seen in parallel with the resistance of other enabled input paths from the same pins

Test Conditions

AVDD2=DBVDD=LDO2VDD=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, LDO1ENA=LDO2ENA=1.8V, DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Programmable Gain Amplifiers (PGAs) IN1L, IN2L, IN1R and IN2R						
C1	Minimum Programmable Gain			-16.5		dB
C2	Maximum Programmable Gain			30		dB
C3	Programmable Gain Step Size	Guaranteed monotonic		1.5		dB
C4	Mute Attenuation	Inputs disconnected		90		dB
C5	Common Mode Rejection Ratio (217Hz input)	Single PGA in differential mode, gain = +30dB		70		dB
		Single PGA in differential mode, gain = 0dB		60		dB
		Single PGA in differential mode, gain = -16.5dB		55		dB
Input Mixers MIXINL and MIXINR						
C6	Minimum Programmable Gain	PGA Outputs to MIXINL and MIXINR		0		dB
C7	Maximum Programmable Gain	PGA Outputs to MIXINL and MIXINR		+30		dB
C8	Programmable Gain Step Size	PGA Outputs to MIXINL and MIXINR		30		dB
C9	Minimum Programmable Gain	Line Inputs and Record path to MIXINL and MIXINR		-12		dB
C10	Maximum Programmable Gain	Line Inputs and Record path to MIXINL and MIXINR		+6		dB
C11	Programmable Gain Step Size	Line Inputs and Record path to MIXINL and MIXINR		3		dB
C12	Minimum Programmable Gain	RXVOICE to MIXINL and MIXINR		-12		dB
C13	Maximum Programmable Gain	RXVOICE to MIXINL and MIXINR		+6		dB
C14	Programmable Gain Step Size	RXVOICE to MIXINL and MIXINR		3		dB
C15	Mute attenuation			TBD		dB
C16	Common Mode Rejection Ratio (217Hz input)	RXVOICE to MIXINL or MIXINR, gain = +6dB		60		dB
		RXVOICE to MIXINL or MIXINR, gain = 0dB		65		dB
		RXVOICE to MIXINL or MIXINR, gain = -12dB		65		dB
Output Mixers MIXOUTL and MIXOUTR						
C17	Minimum Programmable Gain			-21		dB
C18	Maximum Programmable Gain			0		dB
C19	Programmable Gain Step Size			3		dB
C20	Mute attenuation			TBD		dB
Speaker Mixers SPKMIXL and SPKMIXR						
C21	Minimum Programmable Gain			-15		dB
C22	Maximum Programmable Gain			0		dB
C23	Programmable Gain Step Size			3		dB
C24	Mute attenuation			TBD		dB
Output Programmable Gain Amplifiers (PGAs) HPOUT1LVOL, HPOUT1RVOL, MIXOUTLVOL, MIXOUTRVOL, SPKLVOL and SPKRVOL						
C25	Minimum Programmable Gain			-57		dB
C26	Maximum Programmable Gain			+6		dB
C27	Programmable Gain Step Size	Guaranteed monotonic		1		dB
C28	Mute attenuation			TBD		dB
Line Output Driver Programmable Gain LINEOUT1NMIX, LINEOUT1PMIX, LINEOUT2NMIX and LINEOUT2PMIX						
C29	Minimum Programmable Gain			-6		dB
C30	Maximum Programmable Gain			0		dB
C31	Programmable Gain Step Size			6		dB
C32	Mute attenuation			TBD		dB

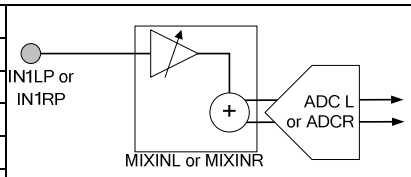
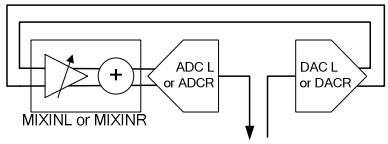
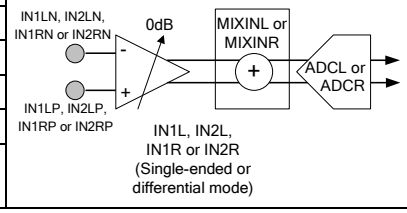
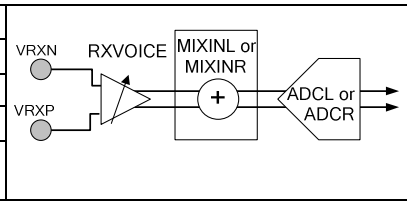
Test Conditions

AVDD2=DBVDD=LDO2VDD=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, LDO1ENA=LDO2ENA=1.8V,
DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Earpiece Driver Programmable Gain HPOUT2MIX						
C33	Minimum Programmable Gain			-6		dB
C34	Maximum Programmable Gain			0		dB
C35	Programmable Gain Step Size			6		dB
C36	Mute attenuation			TBD		dB
C37	Common Mode Rejection Ratio (217Hz input)	Direct Voice path to HPOUT2, gain = 0dB		50		dB
Speaker Output Driver Programmable Gain SPKOUTLBOOST and SPKOUTRBOOST						
C38	Minimum Programmable Gain			0		dB
C39	Maximum Programmable Gain			+12		dB
C40	Programmable Gain Step Size			1.5		dB
C41	Mute attenuation	Class D mode		TBD		dB
C42		Class AB mode		TBD		dB
C43	Common Mode Rejection Ratio (217Hz input)	Direct Voice path to SPKOUTL or SPKOUTR, gain = 0dB		50		dB
		Direct Voice path to SPKOUTL or SPKOUTR, gain = +12dB		50		dB

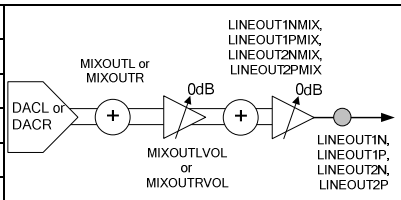
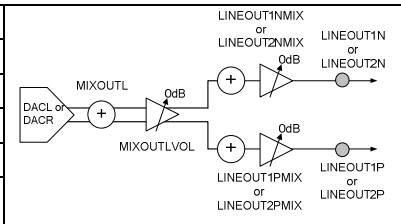
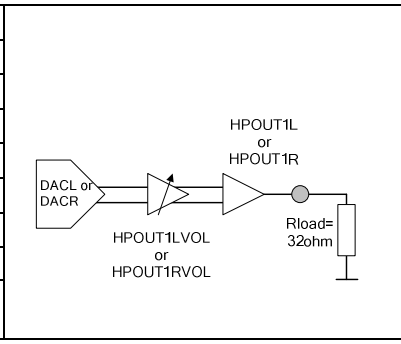
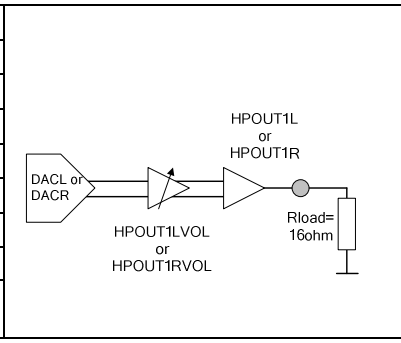
Test Conditions

AVDD2=DBVDD=LDO2VDD=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, LDO1ENA=LDO2ENA=1.8V,
DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ADC Input Path Performance							
D1	**Line Inputs to ADC via MIXINL and MIXINR**						
	SNR (A-weighted)				94		dB
	THD (-1dBFS input)				-87		dB
	THD+N (-1dBFS input)				-85		dB
	Crosstalk (L/R)				-100		dB
	PSRR (AVDD1 217Hz)	100mVpk-pk			TBD		dB
	PSRR (all other supplies 217Hz)	100mVpk-pk			TBD		dB
D2	**Record Path (DACs to ADCs via MIXINL and MIXINR)**						
	SNR (A-weighted)				92		dB
	THD (-1dBFS input)				-80		dB
	THD+N (-1dBFS input)				-78		dB
	Crosstalk (L/R)				-95		dB
	PSRR (AVDD1 217Hz)	100mVpk-pk			TBD		dB
	PSRR (all other supplies 217Hz)	100mVpk-pk			TBD		dB
D3	**Input PGAs to ADC via MIXINL or MIXINR**						
	SNR (A-weighted)				94		dB
	THD (-1dBFS input)				-87		dB
	THD+N (-1dBFS input)				-85		dB
	Crosstalk (L/R)				-100		dB
	PSRR (AVDD1 217Hz)	100mVpk-pk			TBD		dB
	PSRR (all other supplies 217Hz)	100mVpk-pk			TBD		dB
D4	**VRXP-VRXN to one ADC via RXVOICE**						
	SNR (A-weighted)				94		dB
	THD (-1dBFS input)				-87		dB
	THD+N (-1dBFS input)				-85		dB
	PSRR (AVDD1 217Hz)	100mVpk-pk			TBD		dB
	PSRR (all other supplies 217Hz)	100mVpk-pk			TBD		dB

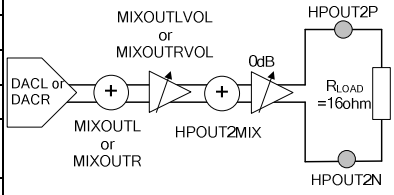
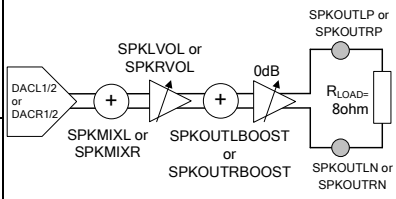
Test Conditions

AVDD2=DBVDD=LDO2VDD=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, LDO1ENA=LDO2ENA=1.8V, DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
DAC Output Path Performance							
E1	**DAC to Single-Ended Line Output (10kΩ / 50pF)**						
	SNR (A-weighted)				97		dB
	THD	0dBFS input			-74		dB
	THD+N	0dBFS input			-72		dB
	Crosstalk (L/R)				-75		dB
	PSRR (AVDD1 217Hz)	100mVpk-pk			TBD		dB
	PSRR (all other supplies 217Hz)	100mVpk-pk			TBD		dB
E2	**DAC to Differential Line Output (10kΩ / 50pF)**						
	SNR (A-weighted)				97		dB
	THD	0dBFS input			-77		dB
	THD+N	0dBFS input			-75		dB
	Crosstalk (L/R)				-90		dB
	PSRR (AVDD1 217Hz)	100mVpk-pk			TBD		dB
	PSRR (all other supplies 217Hz)	100mVpk-pk			TBD		dB
E3	Minimum Line Output Resistance	LINEOUT1N, LINEOUT1P, LINEOUT2N, LINEOUT2P		2			kΩ
E4	Line Output Capacitance	LINEOUT1N, LINEOUT1P, LINEOUT2N, LINEOUT2P	Direct connection			100	pF
			Connection via 1kΩ series resistor			2000	pF
E5	**DAC to Headphone on HPOUT1L or HPOUT1R (R_L=32Ω)**						
	SNR (A-weighted)	OSR = 128fs			100		dB
		OSR = 64fs			97		dB
	THD (P_O=20mW)				-79		dB
	THD+N (P_O=20mW)				-77		dB
	THD (P_O=5mW)				-84		dB
	THD+N (P_O=5mW)				-82		dB
	Crosstalk (L/R)				-95		dB
	PSRR (AVDD1 217Hz)	100mVpk-pk			TBD		dB
	PSRR (all other supplies 217Hz)	100mVpk-pk			TBD		dB
E6	**DAC to Headphone on HPOUT1L or HPOUT1R (R_L=16Ω)**						
	SNR (A-weighted)	OSR = 128fs			100		dB
		OSR = 64fs			97		dB
	THD (P_O=20mW)				-82		dB
	THD+N (P_O=20mW)				-80		dB
	THD (P_O=5mW)				-83		dB
	THD+N (P_O=5mW)				-81		dB
	Crosstalk (L/R)				-95		dB
	PSRR (AVDD1 217Hz)	100mVpk-pk			TBD		dB
	PSRR (all other supplies 217Hz)	100mVpk-pk			TBD		dB

Test Conditions

AVDD2=DBVDD=LDO2VDD=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, LDO1ENA=LDO2ENA=1.8V, DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
E7	Minimum Headphone Resistance	HPOUT1L or HPOUT1R	Normal operation	15			Ω
			Device survival with load applied indefinitely	1			Ω
E8	Headphone Capacitance	HPOUT1L or HPOUT1R				2	nF
E9	**DAC to Earpiece Driver (R_L=16Ω BTL)**						
	SNR (A-weighted)				97		dB
	THD (P_O=50mW)				-74		dB
	THD+N (P_O=50mW)				-72		dB
	PSRR (AVDD1 217Hz)	100mVpk-pk			TBD		dB
	PSRR (all other supplies 217Hz)	100mVpk-pk			TBD		dB
	DC Offset at Load				5		mV
E10	Earpiece Resistance			15			Ω
E11	Earpiece Capacitance		Direct connection			200	pF
E12	**DAC to Speaker Outputs (R_L=8Ω + 10µH BTL, Stereo Mode)**						
	SNR (A-weighted)	Class D mode SPK Boost=+12dB			94		dB
	THD (P_O=0.5W)				-65		dB
	THD+N (P_O=0.5W)				-63		dB
	THD (P_O=1.0W)				-70		dB
	THD+N (P_O=1.0W)				-68		dB
	PSRR (AVDD1 217Hz)				TBD		dB
	PSRR (SPKVDD 217Hz)				TBD		dB
	PSRR (all other supplies 217Hz)				TBD		dB
	Crosstalk (L/R)				-80		dB
	SNR (A-weighted)	Class AB mode SPK Boost=+12dB			96		dB
	THD (P_O=0.5W)				-67		dB
	THD+N (P_O=0.5W)				-65		dB
	THD (P_O=1.0W)				-64		dB
	THD+N (P_O=1.0W)				-62		dB
	PSRR (AVDD1 217Hz)				TBD		dB
	PSRR (SPKVDD 217Hz)				TBD		dB
	PSRR (all other supplies 217Hz)				TBD		dB
	Crosstalk (L/R)				-80		dB
	DC Offset at Load				5		mV

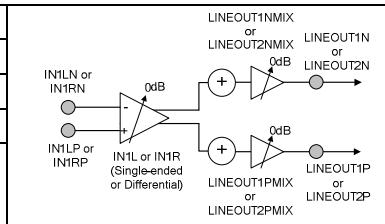
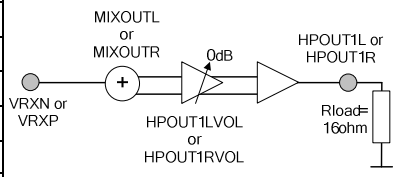
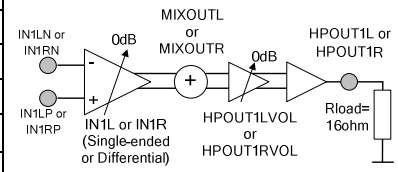
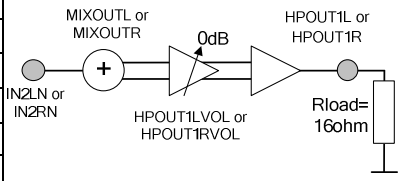
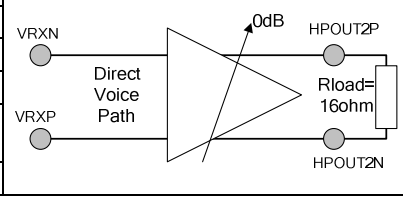
Test Conditions

AVDD2=DBVDD=LDO2VDD=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, LDO1ENA=LDO2ENA=1.8V,
DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
E13	**Speaker Output Power (R_L=8Ω + 10µH BTL, Stereo Mode)**						
	Output Power	SPKVDD=5.0V THD+N ≤ 1%	Class AB		1		W
			Class D		1		
		SPKVDD=4.2V THD+N ≤ 1%	Class AB		0.95		W
			Class D		0.95		
		SPKVDD=3.7V THD+N ≤ 1%	Class AB		0.75		W
			Class D		0.75		
E14	**Speaker Output Power (R_L=4Ω + 10µH BTL, Mono Mode)**						
	Output Power	SPKVDD=5.0V THD+N ≤ 1%	Class AB		2		W
			Class D		2		
		SPKVDD=4.2V THD+N ≤ 1%	Class AB		TBD		W
			Class D		TBD		
		SPKVDD=3.7V THD+N ≤ 1%	Class AB		TBD		W
			Class D		TBD		
E15	Speaker Resistance		Stereo Mode	8			Ω
			Mono Mode	4			Ω
E16	SPKVDD Leakage Current	SPKVDD=5.0V			1		µA

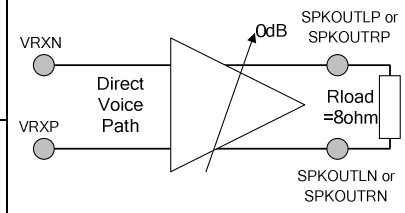
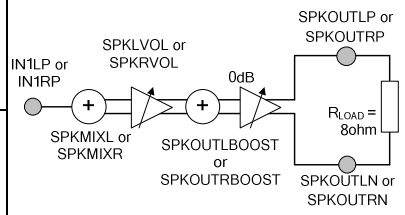
Test Conditions

AVDD2=DBVDD=LDO2VDD=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, LDO1ENA=LDO2ENA=1.8V, DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Bypass Path Performance							
F1	**Input PGA to Differential Line Out (10kΩ / 50pF)**						
	SNR (A-weighted)				102		dB
	THD (0dB output)				-96		dB
	THD+N (0dB output)				-94		dB
	PSRR (AVDD1 217Hz)	100mVpk-pk			TBD		dB
	PSRR (all other supplies 217Hz)	100mVpk-pk			TBD		dB
F2	**VRXP or VRXN to Headphone via MIXOUTL or MIXOUTR (R_L=16Ω)**						
	SNR (A-weighted)				100		dB
	THD (P_O=20mW)				-82		dB
	THD+N (P_O=20mW)				-80		dB
	THD (P_O=5mW)				-83		dB
	THD+N (P_O=5mW)				-81		dB
	PSRR (AVDD1 217Hz)	100mVpk-pk			TBD		dB
	PSRR (all other supplies 217Hz)	100mVpk-pk			TBD		dB
F3	**Input PGA to Headphone via MIXOUTL or MIXOUTR (R_L=16Ω)**						
	SNR (A-weighted)				98		dB
	THD (P_O=20mW)				-82		dB
	THD+N (P_O=20mW)				-80		dB
	THD (P_O=5mW)				-83		dB
	THD+N (P_O=5mW)				-81		dB
	PSRR (AVDD1 217Hz)	100mVpk-pk			TBD		dB
	PSRR (all other supplies 217Hz)	100mVpk-pk			TBD		dB
	Crosstalk (L/R)				-95		dB
F4	**Line Input to Headphone via MIXOUTL and MIXOUTR (R_L=16Ω)**						
	SNR (A-weighted)				100		dB
	THD (P_O=20mW)				-82		dB
	THD+N (P_O=20mW)				-80		dB
	THD (P_O=5mW)				-83		dB
	THD+N (P_O=5mW)				-81		dB
	PSRR (AVDD1 217Hz)	100mVpk-pk			TBD		dB
	PSRR (all other supplies 217Hz)	100mVpk-pk			TBD		dB
	Crosstalk (L/R)				-95		dB
F5	**VRXP-VRXN Direct Voice Path to Earpiece Driver (R_L=16Ω BTL)**						
	SNR (A-weighted)				103		dB
	THD (P_O=50mW)				-74		dB
	THD+N (P_O=50mW)				-72		dB
	PSRR (AVDD1 217Hz)	100mVpk-pk			TBD		dB
	PSRR (all other supplies 217Hz)	100mVpk-pk			TBD		dB
	DC Offset at Load				5		mV

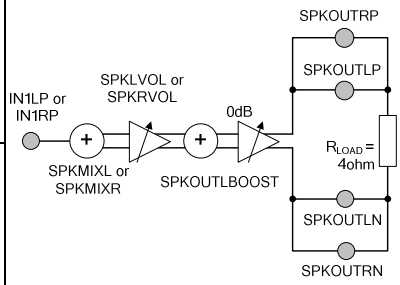
Test Conditions

AVDD2=DBVDD=LDO2VDD=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, LDO1ENA=LDO2ENA=1.8V,
DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
F6	**VRXP-VRXN Direct Voice Path to Speaker Outputs (R_L=8Ω BTL)**						
	SNR (A-weighted)	Class D Mode SPK Boost=+12dB			97		dB
	THD (P_O=0.5W)				-62		dB
	THD+N (P_O=0.5W)				-60		dB
	THD (P_O=1.0W)				-67		dB
	THD+N (P_O=1.0W)				-65		dB
	PSRR (AVDD1 217Hz)				TBD		dB
	PSRR (SPKVDD 217Hz)				TBD		dB
	PSRR (all other supplies 217Hz)				TBD		dB
	SNR (A-weighted)	Class AB Mode SPK Boost=+12dB			102		dB
	THD (P_O=0.5W)				-62		dB
	THD+N (P_O=0.5W)				-60		dB
	THD (P_O=1.0W)				-64		dB
	THD+N (P_O=1.0W)				-62		dB
	PSRR (AVDD1 217Hz)				TBD		dB
	PSRR (SPKVDD 217Hz)				TBD		dB
	PSRR (all other supplies 217Hz)				TBD		dB
	DC Offset at Load				5		mV
F7	**Line Input to Speaker Outputs via SPKMIXL or SPKMIXR (R_L=8Ω BTL)**						
	SNR (A-weighted)	Class D Mode SPK Boost =+12dB			93		dB
	THD (P_O=0.5W)				-62		dB
	THD+N (P_O=0.5W)				-60		dB
	THD (P_O=1.0W)				-67		dB
	THD+N (P_O=1.0W)				-65		dB
	PSRR (AVDD1 217Hz)				TBD		dB
	PSRR (SPKVDD 217Hz)				TBD		dB
	PSRR (all other supplies 217Hz)				TBD		dB
	SNR (A-weighted)	Class AB Mode SPK Boost=+12dB			TBD		dB
	THD (P_O=0.5W)				-62		dB
	THD+N (P_O=0.5W)				-60		dB
	THD (P_O=1.0W)				-64		dB
	THD+N (P_O=1.0W)				-62		dB
	PSRR (AVDD1 217Hz)				TBD		dB
	PSRR (SPKVDD 217Hz)				TBD		dB
	PSRR (all other supplies 217Hz)				TBD		dB
	DC Offset at Load				5		mV

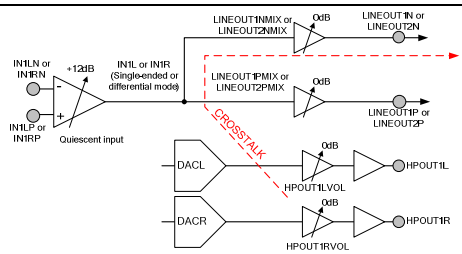
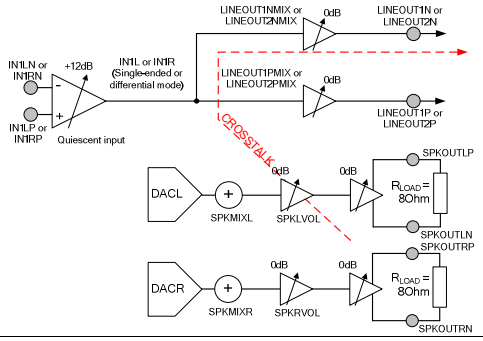
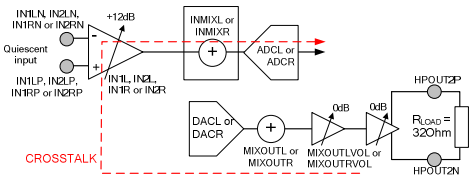
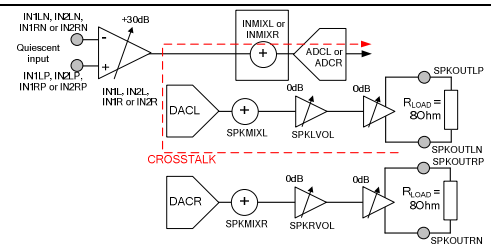
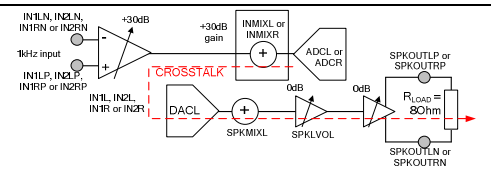
Test Conditions

AVDD2=DBVDD=LDO2VDD=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, LDO1ENA=LDO2ENA=1.8V, DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
F8	**Line Input to Speaker Outputs via SPKMIXL or SPKMIXR (R_L=4Ω BTL, 2W Mono Mode)**						
	SNR (A-weighted)	Class D Mode SPK Boost =+12dB			TBD		dB
	THD (P_O=1.0W)				TBD		dB
	THD+N (P_O=1.0W)				TBD		dB
	THD (P_O=2.0W)				TBD		dB
	THD+N (P_O=2.0W)				TBD		dB
	PSRR (AVDD1 217Hz)				TBD		dB
	PSRR (SPKVDD 217Hz)				TBD		dB
	PSRR (all other supplies 217Hz)				TBD		dB
	SNR (A-weighted)	Class AB Mode SPK Boost=+12dB			TBD		dB
	THD (P_O=1.0W)				TBD		dB
	THD+N (P_O=1.0W)				TBD		dB
	THD (P_O=2.0W)				TBD		dB
	THD+N (P_O=2.0W)				TBD		dB
	PSRR (AVDD1 217Hz)				TBD		dB
	PSRR (SPKVDD 217Hz)				TBD		dB
	PSRR (all other supplies 217Hz)				TBD		dB
	DC Offset at Load				5		mV

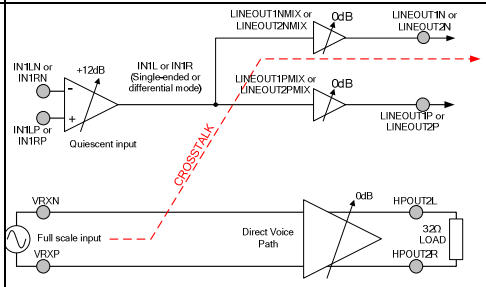
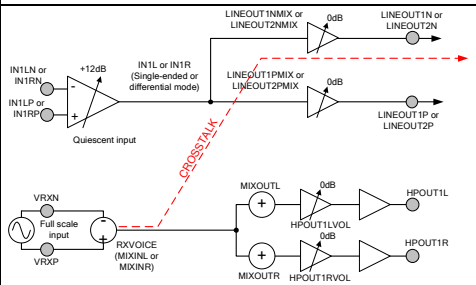
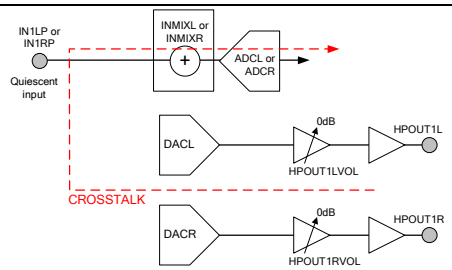
Test Conditions

AVDD2=DBVDD=LDO2VDD=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, LDO1ENA=LDO2ENA=1.8V, DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Multi-Path Channel Separation						
G1	Headset Voice Call: DAC/Headset to Tx Voice Separation 1kHz 0dBFS DAC playback direct to HPOUT1L and HPOUT1R; Quiescent input on IN1LN/P or IN1RN/P (Gain=+12dB), differential line output; Measure crosstalk at differential line output			85		dB
G2	Speakerphone Voice Call: DAC/Speaker to Tx Voice Separation 1kHz 0dBFS DAC playback to speakers, 1W/chan output; Quiescent input on IN1LN/P or IN1RN/P (Gain=+12dB), differential line output; Measure crosstalk at differential line output			100		dB
G3	Earpiece PCM Voice Call: RXVOICE to Tx Voice Separation fs=8kHz for ADC and DAC, DAC_SB_FILT=1; -5dBFS, DAC output to HPOUT2P-HPOUT2N; Quiescent input on input PGA (Gain=+12dB) to ADC via MIXINL or MIXINR; Measure crosstalk at ADC output			110		dB
G4	Speakerphone PCM Voice Call: DAC/Speaker to ADC Separation fs=8kHz for ADC and DAC, DAC_SB_FILT=1; 0dBFS DAC output to speaker (1W output); ADC record from input PGA (Gain=+30dB); Measure crosstalk on ADC output			90		dB
G5	Speakerphone PCM Voice Call: ADC to DAC/Speaker Separation fs=8kHz for ADC and DAC, DAC_SB_FILT=1; Quiescent DAC output to speaker; ADC record from input PGA (Gain=+30dB + 30dB boost); Measure crosstalk on speaker output			95		dB

Test Conditions

AVDD2=DBVDD=LDO2VDD=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, LDO1ENA=LDO2ENA=1.8V, DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
G6	Earpiece Speaker Voice Call: Tx Voice and RXVOICE Separation 1kHz Full scale differential input on VRXP-VRXN, output to HPOUT2P-HPOUT2N; Quiescent input on IN1LN/P or IN1RN/P (Gain=+12dB), differential line output; Measure crosstalk at differential line output			100		dB
G7	Headset Voice Call: Tx Voice and RXVOICE Separation 1kHz full scale differential input on VRXP-VRXN via RXVOICE to MIXOUTL and MIXOUTR, output to HPOUT1L and HPOUT1R; Quiescent input on IN1LN/P or IN1RN/P (Gain=+12dB), differential line output; Measure crosstalk at differential line output			90		dB
G8	Stereo Line Record and Playback: DAC/Headset to ADC Separation -5dBFS input to DACs, playback to HPOUT1L and HPOUT1R; ADC record from line input; Measure crosstalk on ADC output			95		dB

Test Conditions

AVDD2=DBVDD=LDO2VDD=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, LDO1ENA=LDO2ENA=1.8V,
DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Reference Levels						
H1	VMID Midrail Reference Voltage		-3%	AVDD1/2	+3%	V
Microphone Bias (MICBIAS1 and MICBIAS2)						
H2	Bias Voltage	2.4mA load current MICB1_LVL=0	-5%	0.9×AVDD1	+5%	V
		2.4mA load current MICB1_LVL=1	-5%	0.65×AVDD1	+5%	V
H3	Bias Current Source				2.4	mA
H4	Output Noise Spectral Density	1kHz to 20kHz		100		nV/√Hz
H5	PSRR (any supply)			TBD		dB
H6	MIC Current Detect Thresholds	JD_THR = 00		150		µA
		JD_THR = 01		300		µA
		JD_THR = 10		600		µA
		JD_THR = 11		1200		µA
	MIC Short Circuit Detect Thresholds	JD_SCTHR = 00		300		µA
		JD_SCTHR = 01		600		µA
		JD_SCTHR = 10		1200		µA
		JD_SCTHR = 11		2400		µA
	Current detect and short circuit detect thresholds are subject to a +/30% across temperature, supply and part-to-part variation. This should be factored into any application design.					
Charge Pump						
H7	Start-up Time				500	µs
H8	Supply Voltage		1.71		2.0	V
H9	CPVOUTP	Normal mode		CPVDD		V
		Low power mode		CPVDD/2		V
H10	CPVOUTN	Normal mode		-CPVDD		V
		Low power mode		-CPVDD/2		V
H11	Output Impedance			TBD		kΩ
H12	Switching Frequency			TBD		MHz
H13	Flyback Capacitor (between CPFB1 and CPFB2)	at 2V	1	2.2		µF
H14	CPVOUTP Capacitor	at 2V	2	2.2		µF
H15	CPVOUTN Capacitor	at 2V	2	2.2		µF
Digital Input / Output						
H16	Input HIGH Level		0.8×DBVDD			V
H17	Input LOW Level				0.2×DBVDD	V
Note that digital input pins should not be left unconnected / floating.						
H18	Output HIGH Level	I_{OL}=1mA	0.8×DBVDD			V
H19	Output LOW Level	I_{OH}=-1mA			0.2×DBVDD	V
H20	Input capacitance			10		pF
H21	Input leakage		-0.9		0.9	uA

Test Conditions

AVDD2=DBVDD=LDO2VDD=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, LDO1ENA=LDO2ENA=1.8V, DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FLL						
H22	Input Frequency	FLL_CLK_REF_DIV = 00	0.032		13.5	MHz
		FLL_CLK_REF_DIV = 01	0.032		27	MHz
H23	Lock time	F_{REF}=32kHz, F_{OUT}=12.288MHz		2.5		ms
		F_{REF}=12MHz, F_{OUT}=12.288MHz		300		µs
H24	Free-running mode start-up time	VMID enabled		100		µs
H25	Free-running mode frequency accuracy	Reference supplied initially		+/-10		%
		No reference provided		+/-30		%
LDOs						
H26	LDO1 output voltage		2.4		3.1	
H27	LDO1 output voltage step size			0.1		
H28	LDO1 maximum output current			150		mA
H29	LDO2 output voltage		0.9		1.2	
H30	LDO2 output voltage step size			0.1		
H31	LDO2 maximum output current			10		mA
GPIO						
H32	Interrupt response time for accessory / button detect	Input de-bounced	1		512	ms
		Input not de-bounced		0		ms

TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is a measure of the difference in level between the maximum full scale output signal and the output with no input signal applied.
2. Total Harmonic Distortion (dB) – THD is the level of the rms value of the sum of harmonic distortion products relative to the amplitude of the measured output signal.
3. Total Harmonic Distortion plus Noise (dB) – THD+N is the level of the rms value of the sum of harmonic distortion products plus noise in the specified bandwidth relative to the amplitude of the measured output signal.
4. Crosstalk (L/R) (dB) – left-to-right and right-to-left channel crosstalk is the measured signal level in the idle channel at the test signal frequency relative to the signal level at the output of the active channel. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel.
5. Multi-Path Channel Separation (dB) – is the measured signal level in the idle path at the test signal frequency relative to the signal level at the output of the active path. The active path is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the specified idle path.
6. Mute Attenuation – This is a measure of the difference in level between the full scale output signal and the output with mute applied.
7. All performance measurements carried out with 20kHz low pass filter, and where noted an A-weighted filter. Failure to use such a filter will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.

TYPICAL PERFORMANCE

Data to follow

SIGNAL TIMING REQUIREMENTS

MASTER CLOCK

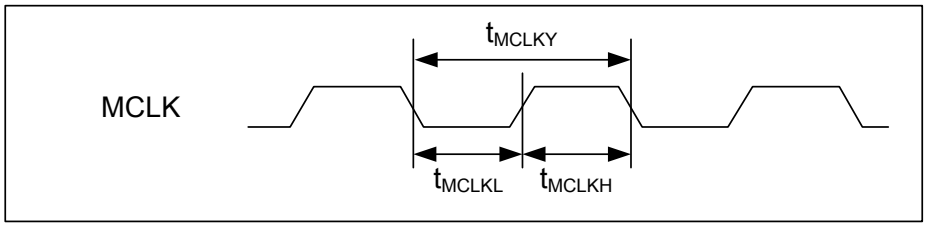


Figure 2 Master Clock Timing

Test Conditions

AVDD2=DBVDD=LDO2VDD=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, LDO1ENA=LDO2ENA=1.8V, DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Master Clock Timing						
MCLK cycle time	T_{MCLKY}	MCLK as input to FLL, FLLn_CLK_REF_DIV = 1	33.33			ns
		MCLK as input to FLL, FLLn_CLK_REF_DIV = 0	66.66			ns
		FLL not used, AIFnCLK_DIV = 1	40			ns
		FLL not used, AIFnCLK_DIV = 0	80			ns
MCLK duty cycle (= T_{MCLKH} : T_{MCLKL})			60:40		40:60	

AUDIO INTERFACE TIMING

MASTER MODE

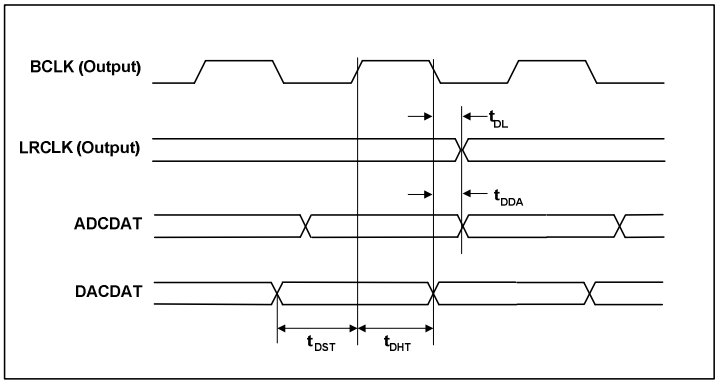


Figure 3 Audio Interface Timing - Master Mode

Test Conditions

AVDD2=DBVDD=LDO2VDD=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, LDO1ENA=LDO2ENA=1.8V, DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing - Master Mode					
LRCLK propagation delay from BCLK falling edge	t_{DL}			20	ns
ADCDAT propagation delay from BCLK falling edge	t_{DDA}			20	ns
DACDAT setup time to BCLK rising edge	t_{DST}	20			ns
DACDAT hold time from BCLK rising edge	t_{DHT}	10			ns

SLAVE MODE

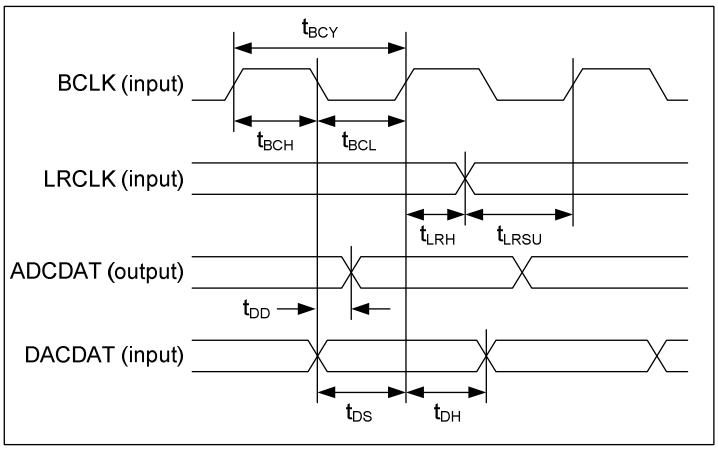


Figure 4 Audio Interface Timing – Slave Mode

Test Conditions

AVDD2=DBVDD=LDO2VDD=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, LDO1ENA=LDO2ENA=1.8V, DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing - Slave Mode					
BCLK cycle time	t_{BCY}	50			ns
BCLK pulse width high	t_{BCH}	20			ns
BCLK pulse width low	t_{BCL}	20			ns
LRCLK set-up time to BCLK rising edge	t_{LRSU}	20			ns
LRCLK hold time from BCLK rising edge	t_{LRH}	10			ns
DACDAT hold time from BCLK rising edge	t_{DH}	10			ns
ADCDAT propagation delay from BCLK falling edge	t_{DD}			20	ns
DACDAT set-up time to BCLK rising edge	t_{DS}	20			ns

TDM MODE

In TDM mode, it is important that two ADC devices do not attempt to drive the ADCDAT pin simultaneously. The timing of the WM8994 ADCDAT tri-stating at the start and end of the data transmission is described in Figure 5 below. Note that this only applies to AIF2; tri-stating is not supported on AIF1 or AIF3.

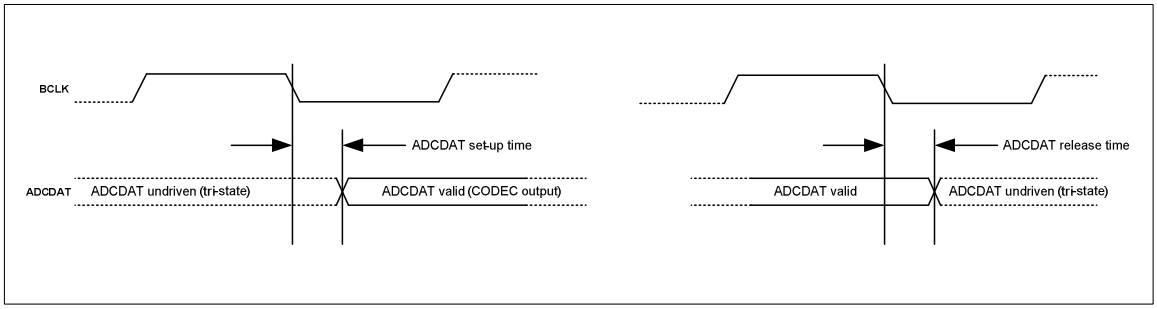


Figure 5 Audio Interface Timing - TDM Mode

Test Conditions

AVDD2=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, LDO1ENA=1.8V, LDO2ENA=0V,
DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Timing Information					
ADCDAT setup time from BCLK falling edge	DCVDD = 2.0V DBVDD = 3.6V		5		ns
	DCVDD = 0.95V DBVDD = 1.71V		15		ns
ADCDAT release time from BCLK falling edge	DCVDD = 2.0V DBVDD = 3.6V		5		ns
	DCVDD = 0.95V DBVDD = 1.71V		15		ns

CONTROL INTERFACE TIMING

2-WIRE (I2C) CONTROL MODE

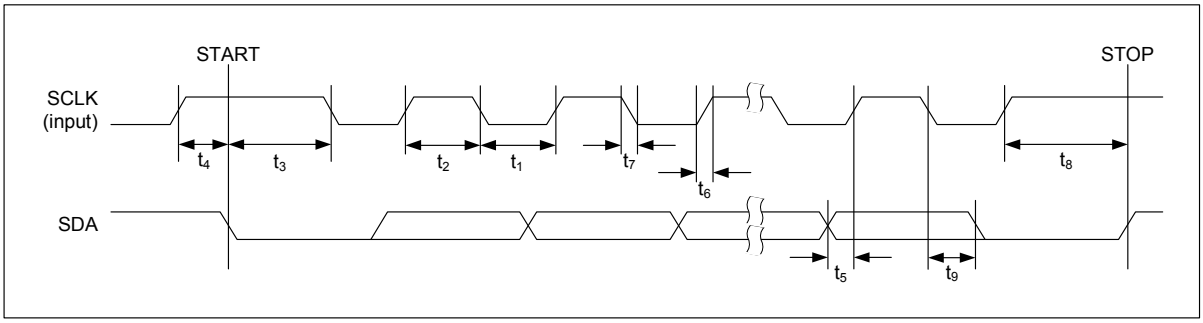


Figure 6 Control Interface Timing - 2-wire (I2C) Control Mode

Test Conditions

AVDD2=DBVDD=LDO2VDD=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, LDO1ENA=LDO2ENA=1.8V, DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SCLK Frequency				400	kHz
SCLK Low Pulse-Width	t_1	1300			ns
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDA, SCLK Rise Time	t_6			300	ns
SDA, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

3-WIRE (SPI) CONTROL MODE

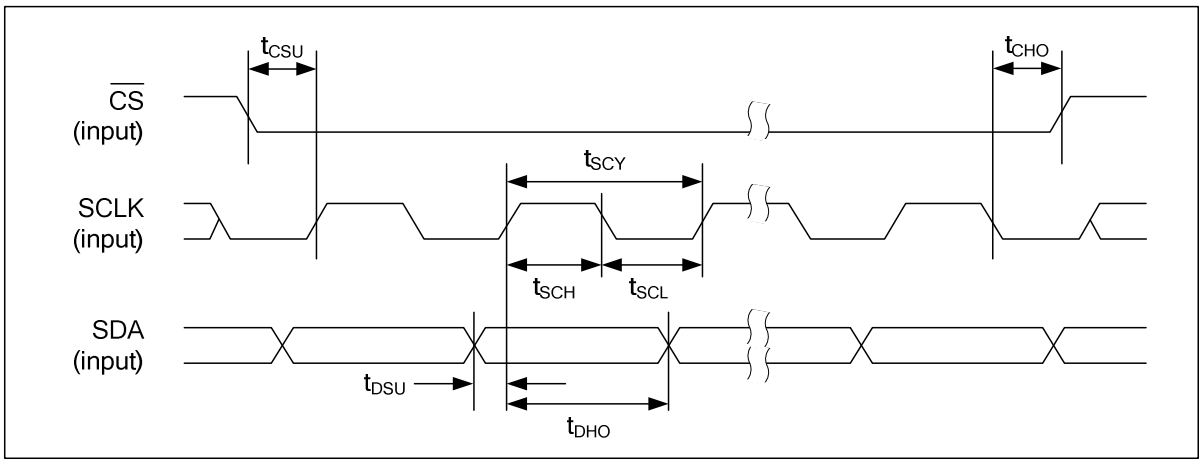


Figure 7 Control Interface Timing - 3-wire (SPI) Control Mode (Write Cycle)

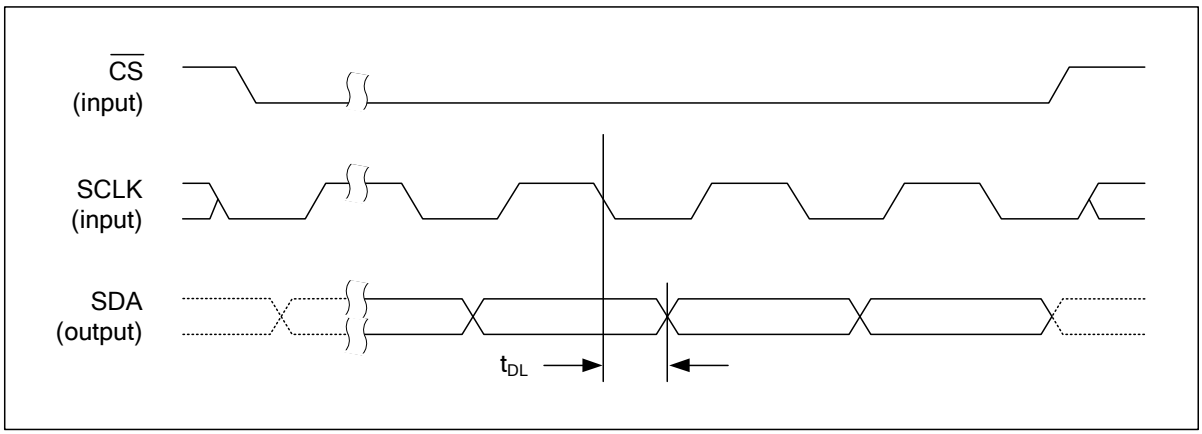


Figure 8 Control Interface Timing - 3-wire (SPI) Control Mode (Read Cycle)

Test Conditions

AVDD2=DBVDD=LDO2VDD=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, LDO1ENA=LDO2ENA=1.8V, DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CS falling edge to SCLK rising edge	t_{CSU}	40			ns
SCLK falling edge to CS rising edge	t_{CHO}	10			ns
SCLK pulse cycle time	t_{SCY}	200			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDA to SCLK set-up time	t_{DSU}	40			ns
SDA to SCLK hold time	t_{DHO}	10			ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns
SCLK falling edge to SDA output transition	t_{DL}			40	ns

4-WIRE (SPI) CONTROL MODE

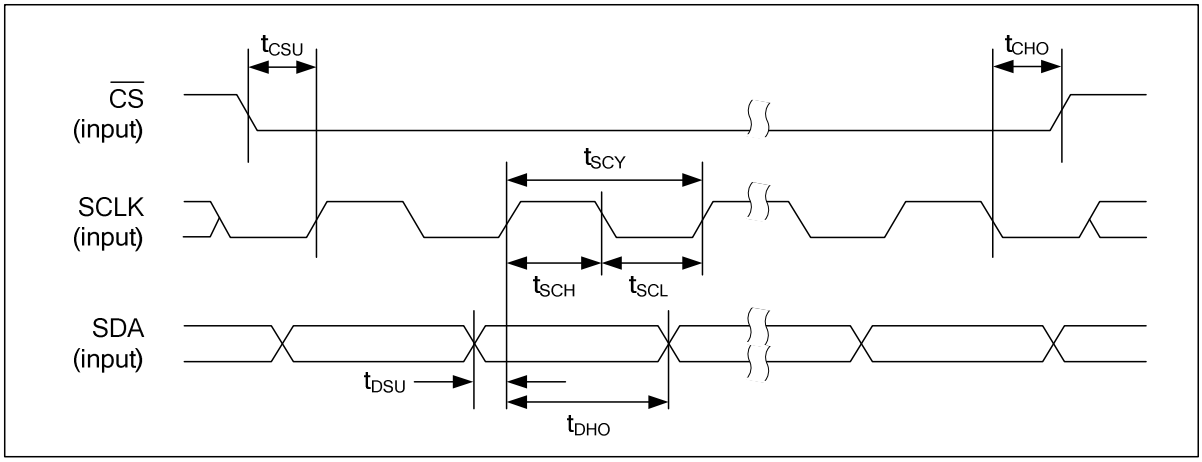


Figure 9 Control Interface Timing - 4-wire (SPI) Control Mode (Write Cycle)

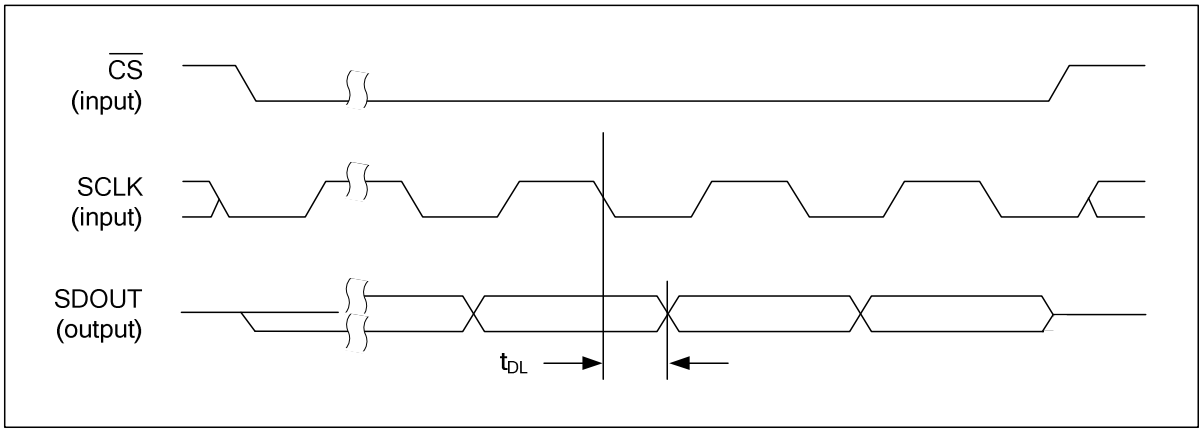


Figure 10 Control Interface Timing - 4-wire (SPI) Control Mode (Read Cycle)

Test Conditions

AVDD2=DBVDD=LDO2VDD=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, LDO1ENA=LDO2ENA=1.8V, DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CS falling edge to SCLK rising edge	t_{CSU}	40			ns
SCLK falling edge to CS rising edge	t_{CHO}	10			ns
SCLK pulse cycle time	t_{SCY}	200			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDA to SCLK set-up time	t_{DSU}	40			ns
SDA to SCLK hold time	t_{DHO}	10			ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns
SCLK falling edge to SDOUT transition	t_{DL}			40	ns

DEVICE DESCRIPTION

INTRODUCTION

The WM8994 is a low power, high quality audio codec designed to interface with a wide range of processors and analogue components. A high level of mixed-signal integration in a very small footprint makes it ideal for portable applications such as mobile phones.

The analogue circuits of the WM8994 are almost entirely backwards-compatible with the WM8993 with the exception of two additional DAC channels, a dual FLL and two integrated LDO regulators.

Three sets of audio interface pins are available in order to provide independent and fully asynchronous connections to multiple processors, typically an application processor, baseband processor and wireless transceiver. Any two of these interfaces can operate totally independently and asynchronously while the third interface can be synchronised to either of the other two and can also provide ultra low power loopback modes to support, for example, wireless headset voice calls.

Four digital microphone input channels are available to support advanced multi-microphone applications such as noise reduction. An integrated microphone activity monitor is available to enable the processor to sleep during periods of microphone inactivity, saving power.

Four DAC channels are available to support use cases requiring up to four simultaneous digital audio streams to the output drivers.

Eight highly flexible analogue inputs allow interfacing to up to four microphone inputs (single-ended or differential), plus multiple stereo or mono line inputs. Connections to an external voice CODEC, FM radio, line input, handset MIC and headset MIC are all fully supported. Signal routing to the output mixers and within the CODEC has been designed for maximum flexibility to support a wide variety of usage modes. A 'Direct Voice' path from a voice CODEC directly to the Speaker or Earpiece output drivers is included.

Nine analogue output drivers are integrated, including a stereo pair of high power, high quality Class D/AB switchable speaker drivers; these can support 1W each in stereo mode, or can be coupled to support a 2W mono speaker output. A mono earpiece driver is provided, providing output from the output mixers or from the low-power differential 'Direct Voice' path.

One pair of ground-reference headphone outputs is provided; these are powered from an integrated Charge Pump, enabling high quality, power efficient headphone playback without any requirement for DC blocking capacitors. A DC Servo circuit is available for DC offset correction, thereby suppressing pops and reducing power consumption. Four line outputs are provided, with multiple configuration options including 4 x single-ended output or 2 x differential outputs. The line outputs are suitable for output to a voice CODEC, an external speaker driver or line output connector. Ground loop feedback is available on the headphone outputs and the line outputs, providing rejection of noise on the ground connections. All outputs have integrated pop and click suppression features.

Internal differential signal routing and amplifier configurations have been optimised to provide the highest performance and lowest possible power consumption for a wide range of usage scenarios, including voice calls and music playback. The speaker drivers offer low leakage and high PSRR; this enables direct connection to a Lithium battery. The speaker drivers provide eight levels of AC and DC gain to allow output signal levels to be maximised for many commonly-used SPKVDD/AVDD1 combinations.

The ADCs and DACs are of hi-fi quality, using a 24-bit low-order oversampling architecture to deliver optimum performance. A flexible clocking arrangement supports mixed sample rates, whilst an integrated ultra-low power dual FLL provides additional flexibility. A high pass filter is available in all ADC and digital MIC paths for removing DC offsets and suppressing low frequency noise such as mechanical vibration and wind noise. A digital mixing path from the ADC or digital MICs to the DAC provides a sidetone of enhanced quality during voice calls. DAC soft mute and un-mute is available for pop-free music playback.

The integrated Dynamic Range Controllers (DRC) and ReTune™ Mobile 5-band parametric equaliser (EQ) provide further processing capability of the digital audio paths. The DRC provides compression and signal level control to improve the handling of unpredictable signal levels. 'Anti-clip' and 'quick release' algorithms improve intelligibility in the presence of transients and impulsive noises. The EQ provides the capability to tailor the audio path according to the frequency characteristics of an earpiece or loudspeaker, and/or according to user preferences.

The WM8994 has highly flexible digital audio interfaces, supporting a number of protocols, including I^2S, DSP, MSB-first left/right justified, and can operate in master or slave modes. PCM operation is supported in the DSP mode. A-law and μ-law companding are also supported. Time division multiplexing (TDM) is available to allow multiple devices to stream data simultaneously on the same bus, saving space and power. The four digital MIC and ADC channels and four DAC channels are available via four TDM channels on Digital Audio Interface 1 (AIF1).

A powerful digital mixing core allows data from each TDM channel of each audio interface and from the ADCs and digital MICs to be mixed and re-routed back to a different audio interface and to the 4 DAC output channels. The digital mixing core can operate synchronously with either Audio Interface 1 or Audio Interface 2, with asynchronous stereo full duplex sample rate conversion performed on the other audio interface as required.

The system clock (SYSCLK) provides clocking for the ADCs, DACs, DSP core, digital audio interface and other circuits. SYSCLK can be derived directly from one of the MCLK1 or MCLK2 pins or via one of two integrated FLLs, providing flexibility to support a wide range of clocking schemes. Typical portable system MCLK frequencies, and sample rates from 8kHz to 96kHz are all supported. Automatic configuration of the clocking circuits is available, derived from the sample rate and from the MCLK / SYSCLK ratio.

The WM8994 uses a standard 2, 3 or 4-wire control interface, providing full software control of all features, together with device register readback. An integrated Control Write Sequencer enables automatic scheduling of control sequences; commonly-used signal configurations may be selected using ready-programmed sequences, including time-optimised control of the WM8994 pop suppression features. It is an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs. Unused circuitry can be disabled under software control, in order to save power; low leakage currents enable extended standby/off time in portable battery-powered applications.

Versatile GPIO functionality is provided, with support for button/accessory detect inputs, or for clock, system status, or programmable logic level output for control of additional external circuitry. Interrupt logic, status readback and de-bouncing options are supported within this functionality.

ANALOGUE INPUT SIGNAL PATH

The WM8994 has eight highly flexible analogue input channels, configurable in a large number of combinations:

1. Up to four fully differential or single-ended microphone inputs

2. Up to eight mono line inputs or 4 stereo line inputs

3. A dedicated mono differential input from external voice CODEC

These inputs may be mixed together or independently routed to different combinations of output drivers. An internal record path is provided at the input mixers to allow DAC output to be mixed with the input signal path (e.g. for voice call recording).

The WM8994 input signal paths and control registers are illustrated in Figure 11.

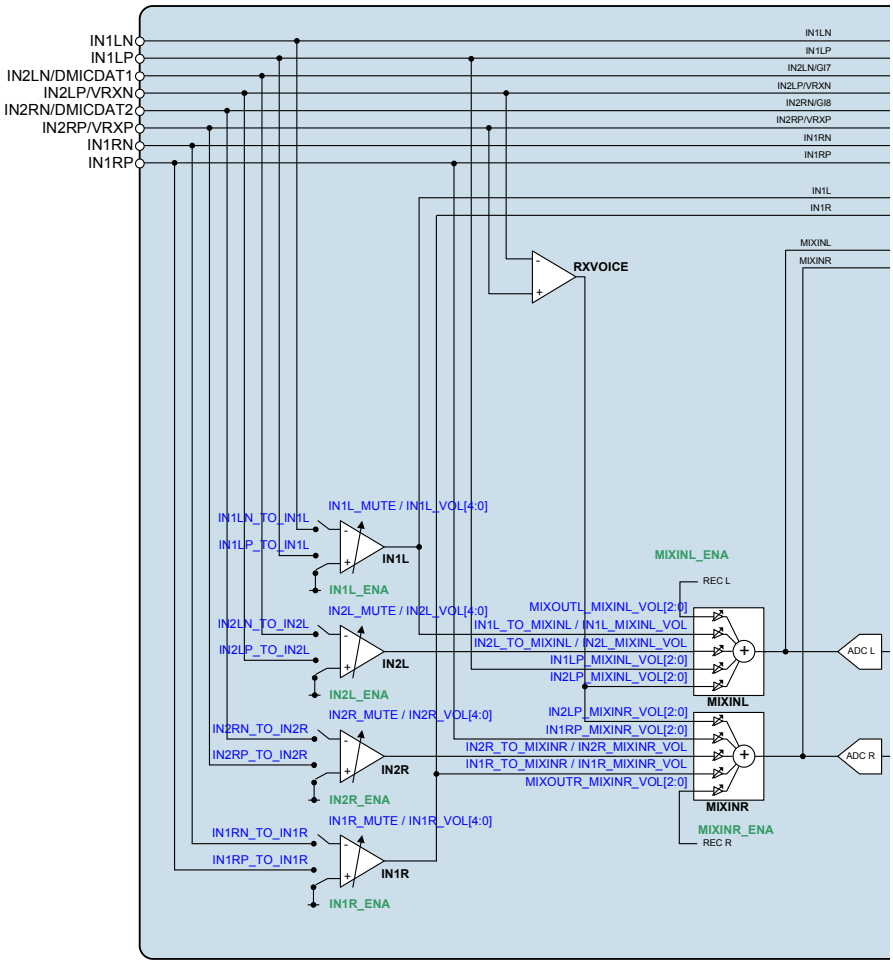


Figure 11 Control Registers for Input Signal Path

MICROPHONE INPUTS

Up to four microphones can be connected to the WM8994, either in single-ended or differential mode. A dedicated PGA is provided for each microphone input. Two low noise microphone bias circuits are provided, reducing the need for external components.

For single-ended microphone inputs, the microphone signal is connected to the inverting input of the PGAs (IN1LN, IN2LN, IN1RN or IN2RN). The non-inverting inputs of the PGAs are internally connected to VMID in this configuration. The non-inverting input pins IN1LP, IN2LP, IN1RP and IN2RP are free to be used as line connections to the input or output mixers in this configuration.

For differential microphone inputs, the non-inverted microphone signal is connected to the non-inverting input of the PGAs (IN1LP, IN2LP, IN1RP or IN2RP), whilst the inverted (or 'noisy ground') signal is connected to the inverting input pins (IN1LN, IN2LN, IN1RN and IN2RN).

The gain of the input PGAs is controlled via register settings, as defined in Table 4. Note that the input impedance of both inverting and non-inverting inputs changes with the input PGA gain setting, as described under "Electrical Characteristics".

The microphone input configurations are illustrated in Figure 12 and Figure 13. Note that any PGA input pin that is used in either microphone configuration is not available for use as a line input path at the same time.

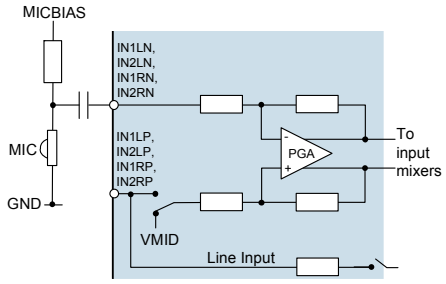


Figure 12 Single-Ended Microphone Input

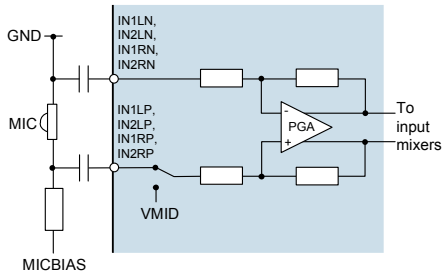


Figure 13 Differential Microphone Input

MICROPHONE BIAS CONTROL

There are two MICBIAS generators which provide low noise reference voltages suitable for biasing electret condenser (ECM) type microphones via an external resistor. Refer to the Applications Information section for recommended external components. The MICBIAS voltages can be enabled using the MICB1_ENA and MICB2_ENA control bits; the voltage of each can be selected using the MICB1_LVL and MICB2_LVL register bits as detailed in Table 1.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (0001h) Power Management (1)	5	MICB2_ENA	0b	Microphone Bias 2 Enable 0 = OFF (high impedance output) 1 = ON
	4	MICB1_ENA	0b	Microphone Bias 1 Enable 0 = OFF (high impedance output) 1 = ON
R58 (003Ah) MICBIAS	1	MICB2_LVL	0b	Microphone Bias 2 Voltage Control 0 = 0.9 * AVDD1 1 = 0.65 * AVDD1
	0	MICB1_LVL	0b	Microphone Bias 1 Voltage Control 0 = 0.9 * AVDD1 1 = 0.65 * AVDD1

Table 1 Microphone Bias Control

Note that the maximum source current capability for MICBIAS1 and MICBIAS2 is 2.4mA each. The external biasing resistance must be large enough to limit each MICBIAS current to 2.4mA across the full microphone impedance range.

MICROPHONE CURRENT DETECT

A MICBIAS current detect function allows detection of accessories such as headset microphones. When the MICBIAS load current exceeds one of two programmable thresholds, (e.g. short circuit current or normal operating current), an interrupt or GPIO output can be generated. The current detection circuit is enabled by the MICD_ENA bit; the current thresholds are selected by the MICD_THR and MICD_SCTHR register fields as described in Table 70. See “General Purpose Input/Output” for a full description of these fields.

LINE AND VOICE CODEC INPUTS

All eight analogue input pins may be used as line inputs. Each line input has different signal path options, providing flexibility, high performance and low power consumption for many different usage modes.

IN1LN and IN1RN can operate as single-ended line inputs to the input PGAs IN1L and IN1R respectively. These inputs provide a high gain path if required for low input signal levels.

IN2LN and IN2RN can operate as single-ended line inputs to the input PGAs IN2L and IN2R respectively, providing further high gain signal paths. These pins can also be connected to either of the output mixers MIXOUTL and MIXOUTR.

IN1LP and IN1RP can operate as single-ended line inputs to the input mixers MIXINL and MIXINR, or to the speaker mixers SPKMIXL and SPKMIXR. These signal paths enable power consumption to be reduced, by allowing the input PGAs and other circuits to be disabled if not required.

IN2LP/VRXN and IN2RP/VRXP can operate in three different ways:

- Mono differential ’RXVOICE’ input (e.g. from an external voice CODEC) to the input mixers MIXINL and MIXINR.
- Single-ended line inputs to either of the output mixers MIXOUTL and MIXOUTR.
- Ultra-low power mono differential ‘Direct Voice’ input (e.g. from an external voice CODEC) to the ear speaker driver on HPOUT2, or to either of the speaker drivers on SPKOUTL and SPKOUTR.

Signal path configuration to the input PGAs and input mixers is detailed later in this section. Signal path configuration to the output mixers and speaker mixers is described in “Output Signal Paths”.

The line input and voice CODEC input configurations are illustrated in Figure **14** through to Figure **17**.

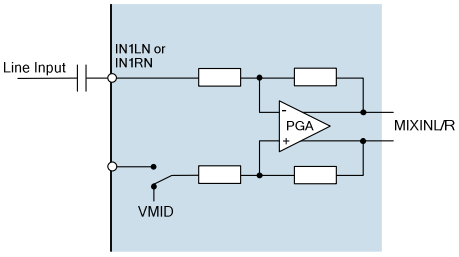


Figure 14 IN1LN or IN1RN as Line Inputs

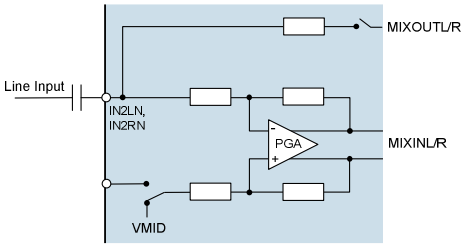


Figure 15 IN2LN or IN2RN as Line Inputs

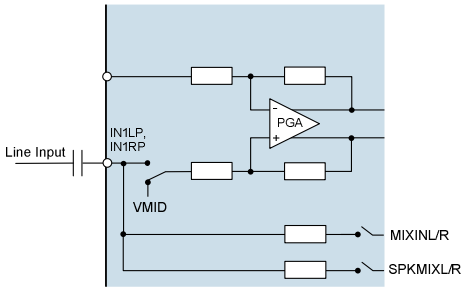


Figure 16 IN1LP or IN1RP as Line Inputs

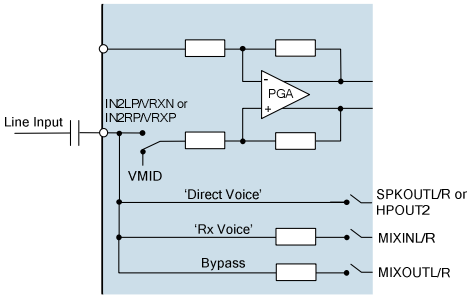


Figure 17 IN2LP or IN2RP as Line Inputs

INPUT PGA ENABLE

The Input PGAs are enabled using register bits IN1L_ENA, IN2L_ENA, IN1R_ENA and IN2R_ENA, as described in Table 2. The Input PGAs must be enabled for microphone input on the respective input pins, or for line input on the inverting input pins IN1LN, IN1RN, IN2LN, IN2RN.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (0002h) Power Management (2)	7	IN2L_ENA	0b	IN2L Input PGA Enable 0 = Disabled 1 = Enabled
	6	IN1L_ENA	0b	IN1L Input PGA Enable 0 = Disabled 1 = Enabled
	5	IN2R_ENA	0b	IN2R Input PGA Enable 0 = Disabled 1 = Enabled
	4	IN1R_ENA	0b	IN1R Input PGA Enable 0 = Disabled 1 = Enabled

Table 2 Input PGA Enable

For normal operation of the input PGAs, the reference voltage VMID and the bias current must also be enabled. See "Reference Voltages and Master Bias" for details of the associated controls VMID_SEL and BIAS_ENA.

INPUT PGA CONFIGURATION

Each of the Input PGAs can operate in a single-ended or differential mode. In differential mode, both inputs to the PGA are connected to the input source. In single-ended mode, the non-inverting input to the PGA must be connected to VMID. Configuration of the PGA inputs to the WM8994 input pins is controlled using the register bits shown in Table 3.

Single-ended microphone operation is configured by connecting the input source to the inverting input of the applicable PGA. The non-inverting input of the PGA must be connected to VMID.

Differential microphone operation is configured by connecting the input source to both inputs of the applicable PGA.

Line inputs to the input pins IN1LN, IN2LN, IN1RN and IN2RN must be connected to the applicable PGA. The non-inverting input of the PGA must be connected to VMID.

Line inputs to the input pins IN1LP, IN2LP, IN1RP or IN2RP do not connect to the input PGAs. The non-inverting inputs of the associated PGAs must be connected to VMID. The inverting inputs of the associated PGAs may be used as separate mic/line inputs if required.

The maximum available attenuation on any of these input paths is achieved by using register bits shown in Table 3 to disconnect the input pins from the applicable PGA.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R40 (0028h) Input Mixer2	7	IN2LP_TO_IN2L	0b	IN2L PGA Non-Inverting Input Select 0 = Connected to VMID 1 = Connected to IN2LP
	6	IN2LN_TO_IN2L	0b	IN2L PGA Inverting Input Select 0 = Not connected 1 = Connected to IN2LN
	5	IN1LP_TO_IN1L	0b	IN1L PGA Non-Inverting Input Select 0 = Connected to VMID 1 = Connected to IN1LP
	4	IN1LN_TO_IN1L	0b	IN1L PGA Inverting Input Select 0 = Not connected 1 = Connected to IN1LN
	3	IN2RP_TO_IN2R	0b	IN2R PGA Non-Inverting Input Select 0 = Connected to VMID 1 = Connected to IN2RP
	2	IN2RN_TO_IN2R	0b	IN2R PGA Inverting Input Select 0 = Not connected 1 = Connected to IN2RN
	1	IN1RP_TO_IN1R	0b	IN1R PGA Non-Inverting Input Select 0 = Connected to VMID 1 = Connected to IN1RP
	0	IN1RN_TO_IN1R	0b	IN1R PGA Inverting Input Select 0 = Not connected 1 = Connected to IN1RN

Table 3 Input PGA Configuration

INPUT PGA VOLUME CONTROL

Each of the four Input PGAs has an independently controlled gain range of -16.5dB to +30dB in 1.5dB steps. The gains on the inverting and non-inverting inputs to the PGAs are always equal. Each Input PGA can be independently muted using the PGA mute bits as described in Table 4, with maximum mute attenuation achieved by simultaneously disconnecting the corresponding inputs described in Table 3.

To prevent "zipper noise", a zero-cross function is provided on the input PGAs. When this feature is enabled, volume updates will not take place until a zero-crossing is detected. In the case of a long period without zero-crossings, a timeout function is provided. When the zero-cross function is enabled, the volume will update after the timeout period if no earlier zero-cross has occurred. The timeout clock is enabled using TOCLK_ENA, the timeout period is set by TOCLK_RATE. See “Clocking and Sample Rates” for more information on these fields.

The IN1_VU and IN2_VU bits control the loading of the input PGA volume data. When IN1_VU and IN2_VU are set to 0, the PGA volume data will be loaded into the respective control register, but will not actually change the gain setting. The IN1L and IN1R volume settings are both updated when a 1 is written to IN1_VU; the IN2L and IN2R volume settings are both updated when a 1 is written to IN2_VU. This makes it possible to update the gain of the left and right signal paths simultaneously.

The Input PGA Volume Control register fields are described in Table 4 and Table 5.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (0018h) Left Line Input 1&2 Volume	8	IN1_VU	N/A	Input PGA Volume Update Writing a 1 to this bit will cause IN1L and IN1R input PGA volumes to be updated simultaneously
	7	IN1L_MUTE	1b	IN1L PGA Mute 0 = Disable Mute 1 = Enable Mute
	6	IN1L_ZC	0b	IN1L PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only
	4:0	IN1L_VOL [4:0]	01011b (0dB)	IN1L Volume -16.5dB to +30dB in 1.5dB steps (See Table 5 for volume range)
R25 (0019h) Left Line Input 3&4 Volume	8	IN2_VU	N/A	Input PGA Volume Update Writing a 1 to this bit will cause IN2L and IN2R input PGA volumes to be updated simultaneously
	7	IN2L_MUTE	1b	IN2L PGA Mute 0 = Disable Mute 1 = Enable Mute
	6	IN2L_ZC	0b	IN2L PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only
	4:0	IN2L_VOL [4:0]	01011b (0dB)	IN2L Volume -16.5dB to +30dB in 1.5dB steps (See Table 5 for volume range)
R26 (001Ah) Right Line Input 1&2 Volume	8	IN1_VU	N/A	Input PGA Volume Update Writing a 1 to this bit will cause IN1L and IN1R input PGA volumes to be updated simultaneously
	7	IN1R_MUTE	1b	IN1R PGA Mute 0 = Disable Mute 1 = Enable Mute
	6	IN1R _ZC	0b	IN1R PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only
	4:0	IN1R _VOL [4:0]	01011b (0dB)	IN1R Volume -16.5dB to +30dB in 1.5dB steps (See Table 5 for volume range)
R27 (001Bh) Right Line Input 3&4 Volume	8	IN2_VU	N/A	Input PGA Volume Update Writing a 1 to this bit will cause IN2L and IN2R input PGA volumes to be updated simultaneously
	7	IN2R_MUTE	1b	IN2R PGA Mute 0 = Disable Mute 1 = Enable Mute
	6	IN2R _ZC	0b	IN2R PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only
	4:0	IN2R _VOL [4:0]	01011b (0dB)	IN2R Volume -16.5dB to +30dB in 1.5dB steps (See Table 5 for volume range)

Table 4 Input PGA Volume Control

IN1L_VOL[4:0], IN2L_VOL[4:0], IN1R_VOL[4:0], IN2R_VOL[4:0]	VOLUME (dB)
00000	-16.5
00001	-15.0
00010	-13.5
00011	-12.0
00100	-10.5
00101	-9.0
00110	-7.5
00111	-6.0
01000	-4.5
01001	-3.0
01010	-1.5
01011	0
01100	+1.5
01101	+3.0
01110	+4.5
01111	+6.0
10000	+7.5
10001	+9.0
10010	+10.5
10011	+12.0
10100	+13.5
10101	+15.0
10110	+16.5
10111	+18.0
11000	+19.5
11001	+21.0
11010	+22.5
11011	+24.0
11100	+25.5
11101	+27.0
11110	+28.5
11111	+30.0

Table 5 Input PGA Volume Range

INPUT MIXER ENABLE

The WM8994 has two analogue input mixers which allow the Input PGAs and Line Inputs to be combined in a number of ways and output to the ADCs, Output Mixers, or directly to the output drivers via bypass paths.

The input mixers MIXINL and MIXINR are enabled by the MIXINL_ENA and MIXINR_ENA register bits, as described in Table 6. These control bits also enable the RXVOICE input path, described in the following section.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (0002h) Power Management (2)	9	MIXINL_ENA	0b	Left Input Mixer Enable (Enables MIXINL and RXVOICE input to MIXINL) 0 = Disabled 1 = Enabled
	8	MIXINR_ENA	0b	Right Input Mixer Enable (Enables MIXINR and RXVOICE input to MIXINR) 0 = Disabled 1 = Enabled

Table 6 Input Mixer Enable

INPUT MIXER CONFIGURATION AND VOLUME CONTROL

The left and right channel input mixers MIXINL and MIXINR can be configured to take input from up to five sources:

1. IN1L or IN1R Input PGA
2. IN2L or IN2R Input PGA
3. IN1LP or IN1RP pin (PGA bypass)
4. RXVOICE mono differential input from IN2LP/VRXN and IN2RP/VRXP
5. MIXOUTL or MIXOUTR Output Mixer (Record path)

The Input Mixer configuration and volume controls are described in Table 7 for the Left input mixer (MIXINL) and Table 8 for the Right input mixer (MIXINR). The signal levels from the Input PGAs may be set to Mute, 0dB or 30dB boost. Gain controls for the PGA bypass, RXVOICE and Record paths provide adjustment from -12dB to +6dB in 3dB steps.

To prevent pop noise, it is recommended that gain and mute controls for the input mixers are not modified while the signal paths are active. If volume control is required on these signal paths, it is recommended that this is implemented using the input PGA volume controls or the ADC volume controls. The ADC volume controls are described in the “Analogue to Digital Converter (ADC)” section.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R41 (0029h) Input Mixer3	8	IN2L_TO_MIXINL	0b	IN2L PGA Output to MIXINL Mute 0 = Mute 1 = Un-Mute
	7	IN2L_MIXINL_VOL	0b	IN2L PGA Output to MIXINL Gain 0 = 0dB 1 = +30dB
	5	IN1L_TO_MIXINL	0b	IN1L PGA Output to MIXINL Mute 0 = Mute 1 = Un-Mute
	4	IN1L_MIXINL_VOL	0b	IN1L PGA Output to MIXINL Gain 0 = 0dB 1 = +30dB
	2:0	MIXOUTL_MIXINL_VOL [2:0]	000b (Mute)	Record Path MIXOUTL to MIXINL Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
R43 (002Bh) Input Mixer5	8:6	IN1LP_MIXINL_VOL [2:0]	000b (Mute)	IN1LP Pin (PGA Bypass) to MIXINL Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
	2:0	VRX_MIXINL_VOL [2:0]	000b (Mute)	RXVOICE (VRXN/VRXP) Differential Input to MIXINL Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB

Table 7 Left Input Mixer (MIXINL) Volume Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R42 (002A) Input Mixer4	8	IN2R_TO_MIXINR	0b	IN2R PGA Output to MIXINR Mute 0 = Mute 1 = Un-Mute
	7	IN2R_MIXINR_VOL	0b	IN2R PGA Output to MIXINR Gain 0 = 0dB 1 = +30dB
	5	IN1R_TO_MIXINR	0b	IN1R PGA Output to MIXINR Mute 0 = Mute 1 = Un-Mute
	4	IN1R_MIXINR_VOL	0b	IN1R PGA Output to MIXINR Gain 0 = 0dB 1 = +30dB
	2:0	MIXOUTR_MIXINR_VOL [2:0]	000b (Mute)	Record Path MIXOUTR to MIXINR Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
R44 (002Ch) Input Mixer6	8:6	IN1RP_MIXINR_VOL [2:0]	000b (Mute)	IN1RP Pin (PGA Bypass) to MIXINR Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
	2:0	VRX_MIXINR_VOL [2:0]	000b (Mute)	RXVOICE (VRXN/VRXP) Differential Input to MIXINR Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB

Table 8 Right Input Mixer (MIXINR) Volume Control

DIGITAL MICROPHONE INTERFACE

The WM8994 supports a four-channel digital microphone interface. Two channels of audio data are multiplexed on the DMICDAT1 pin and a further two channels are multiplexed on the DMICDAT2 pin. All four channels are clocked using the DMICCLK output pin.

The DMICDAT1 function is shared with the IN2LN pin; the analogue signal paths from IN2LN cannot be used when this pin is used for DMICDAT1 digital microphone input.

The DMICDAT2 function is shared with the IN2RN pin; the analogue signal paths from IN2RN cannot be used when this pin is used for DMICDAT2 digital microphone input.

When digital microphone input is enabled, the WM8994 outputs a clock signal on the DMICCLK pin, which supports digital microphone operation at the AIF1 sampling rate. See "Clocking and Sample Rates" for details of the supported clocking configurations. Note that MICBIAS1 must be enabled (MIC1B_ENA=1), and configured for 0.9*AVDD1 (MICB1_LVL=0), for the digital microphone interface to operate. It is intended that MICBIAS1 is used as a low noise supply for the digital microphones.

The DMICDAT1 digital microphone channels are enabled using DMIC1L_ENA and DMIC1R_ENA. When these signal paths are enabled, the respective ADC path is disconnected and the digital microphone data is routed to the digital mixing input bus, as illustrated in "Digital Mixing".

The DMICDAT2 digital microphone channels are enabled using DMIC2L_ENA and DMIC2R_ENA. When these signal paths are enabled, the digital microphone data is routed to the digital mixing input bus, as illustrated in "Digital Mixing".

On each of DMICDAT1 and DMICDAT2, the two microphones are interleaved as illustrated in Figure 18. The interface requires that MIC1 (Left channel) transmits a data bit each time that DMICCLK is high, and MIC2 (Right channel) transmits when DMICCLK is low. The WM8994 samples the digital microphone data in the middle of each DMICCLK clock phase. Each microphone must tri-state its data output when the other microphone is transmitting.

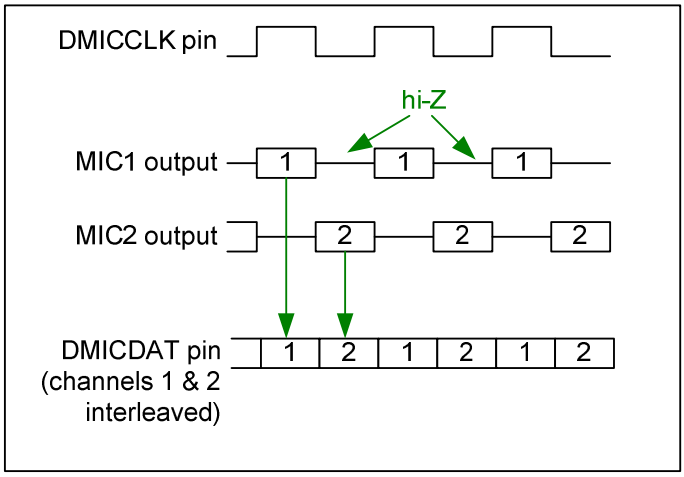


Figure 18 Digital Microphone Interface Timing

The four digital microphone channels can be routed to one of the four timeslots on AIF1. The DMICDAT1 microphones, when enabled, are routed to the Left/Right channels of AIF1 Timeslot 0. The DMICDAT2 microphones, when enabled, are routed to the Left/Right channels of AIF1 Timeslot 1.

The digital microphone channels can be routed, in a limited number of configurations, to the digital mixing output bus, via the digital sidetone signal paths. See "Digital Mixing" for further details.

The digital microphone interface control fields are described in Table 9.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 (0004h) Power Management (4)	5	DMIC2L_ENA	0	Digital microphone DMICDAT2 Left channel enable 0 = Disabled 1 = Enabled
	4	DMIC2R_ENA	0	Digital microphone DMICDAT2 Right channel enable 0 = Disabled 1 = Enabled
	3	DMIC1L_ENA	0	Digital microphone DMICDAT1 Left channel enable 0 = Disabled 1 = Enabled
	2	DMIC1R_ENA	0	Digital microphone DMICDAT1 Right channel enable 0 = Disabled 1 = Enabled

Table 9 Digital Microphone Interface Control

DIGITAL PULL-UP AND PULL-DOWN

The WM8994 provides integrated pull-up and pull-down resistors on the DMICDAT1 and DMICDAT2 pins. This provides a flexible capability for interfacing with other devices. Each of the pull-up and pull-down resistors can be configured independently using the register bits described in Table 10.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1824 (0720h) Digital Pulls	11	DMICDAT2_PU	0	DMICDAT2 Pull-Up enable 0 = Disabled 1 = Enabled
	10	DMICDAT2_PD	0	DMICDAT2 Pull-Down enable 0 = Disabled 1 = Enabled
	9	DMICDAT1_PU	0	DMICDAT1 Pull-Up enable 0 = Disabled 1 = Enabled
	8	DMICDAT1_PD	0	DMICDAT1 Pull-Down enable 0 = Disabled 1 = Enabled

Table 10 Digital Pull-Up and Pull-Down Control

ANALOGUE TO DIGITAL CONVERTER (ADC)

The WM8994 uses stereo 24-bit, 128x oversampled sigma-delta ADCs. The use of multi-bit feedback and high oversampling rates reduces the effects of jitter and high frequency noise. An oversample rate of 64x can also be supported - see “Clocking and Sample Rates” for details. The ADC full scale input level is proportional to AVDD1 - see “Electrical Characteristics”. Any input signal greater than full scale may overload the ADC and cause distortion.

The ADCs are enabled by the ADCL_ENA and ADCR_ENA register bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 (0004h) Power Management (4)	1	ADCL_ENA	0	Left ADC Enable 0 = ADC disabled 1 = ADC enabled
	0	ADCR_ENA	0	Right ADC Enable 0 = ADC disabled 1 = ADC enabled

Table 11 ADC Enable Control

ADC DIGITAL VOLUME AND FILTER CONTROL

The digital volume control between the ADCs and the Audio Interface (AIF1) is controlled by the AIF1ADC1L_VOL and AIF1ADC1R_VOL registers. Digital high pass filters are also provided in the ADC output signal paths. The applicable control registers are defined in the “Digital Volume and Filter Control” section.

DIGITAL CORE ARCHITECTURE

The WM8994 Digital Core provides an extensive set of mixing and signal processing features. The Digital Core Architecture is illustrated in Figure 19, which also identifies the datasheet sections applicable to each portion of the Digital Core.

Audio Interface 1 (AIF1) supports audio input and output on two stereo timeslots simultaneously, making a total of four inputs and four outputs. The mixing of the four AIF1 output paths is described in “Audio Interface 1 (AIF1) Output Mixing”.

A digital mixing path from the ADCs or Digital Microphones to the DAC output paths provides a high quality sidetone for voice calls or other applications. The sidetone configuration is described in “Digital Sidetone Mixing”; the associated filter and volume control is described in “Digital Sidetone Volume and Filter Control”.

Each of the four hi-fi DACs has a dedicated mixer for controlling the signal paths to that DAC. The configuration of these signal paths is described in “DAC Output Digital Mixing”.

Each DAC is provided with digital volume control, soft mute / un-mute and a low pass filter. The associated controls are defined in the “Digital to Analogue Converter (DAC)” section.

Digital processing can be applied to the four input channels of AIF1 and the two input channels of AIF2. The available features include 5-band equalization (EQ), 3D stereo expansion and dynamic range control (DRC).

The EQ provides the capability to tailor the audio path according to the frequency characteristics of an earpiece or loudspeaker, and/or according to user preferences. The EQ controls are described in “ReTune™ Mobile Parametric Equalizer (EQ)”. The DRC provides adaptive signal level control to improve the handling of unpredictable signal levels and to improve intelligibility in the presence of transients and impulsive noises. The DRC controls are described in “Dynamic Range Control (DRC)”. 3D stereo expansion provides a stereo enhancement effect; the depth of the effect is programmable, as described in “3D Stereo Expansion”.

The input channels of AIF1 and AIF2 are also equipped with digital volume control, soft mute / un-mute and de-emphasis filter control; see “Digital Volume and Filter Control” for details of these features.

The output channels of AIF1 and AIF2 can be configured using the digital volume control and a programmable high-pass filter (HPF). The Dynamic Range Control (DRC) circuit can also be applied here, with the restriction that a DRC cannot be enabled in the input and output path of one AIF channel at the same time. The AIF output volume and filter controls are described in “Digital Volume and Filter Control”.

The WM8994 provides two full audio interfaces, AIF1 and AIF2. Each interface supports a number of protocols, including I^2S, DSP, MSB-first left/right justified, and can operate in master or slave modes. PCM operation is supported in the DSP mode. A-law and μ-law companding are also supported. Time division multiplexing (TDM) is available to allow multiple devices to stream data simultaneously on the same bus, saving space and power.

Four-channel input and output is supported using TDM on AIF1. Two-channel input and output is supported on AIF2. A third interface, AIF3, is partially supported, using multiplexers to re-configure alternate connections to AIF1 or AIF2.

Signal mixing between audio interfaces is possible. The WM8994 performs stereo full-duplex sample rate conversion between the audio interfaces as required. (Note that sample rate conversion is not supported on some signal paths, as noted in Figure 19.)

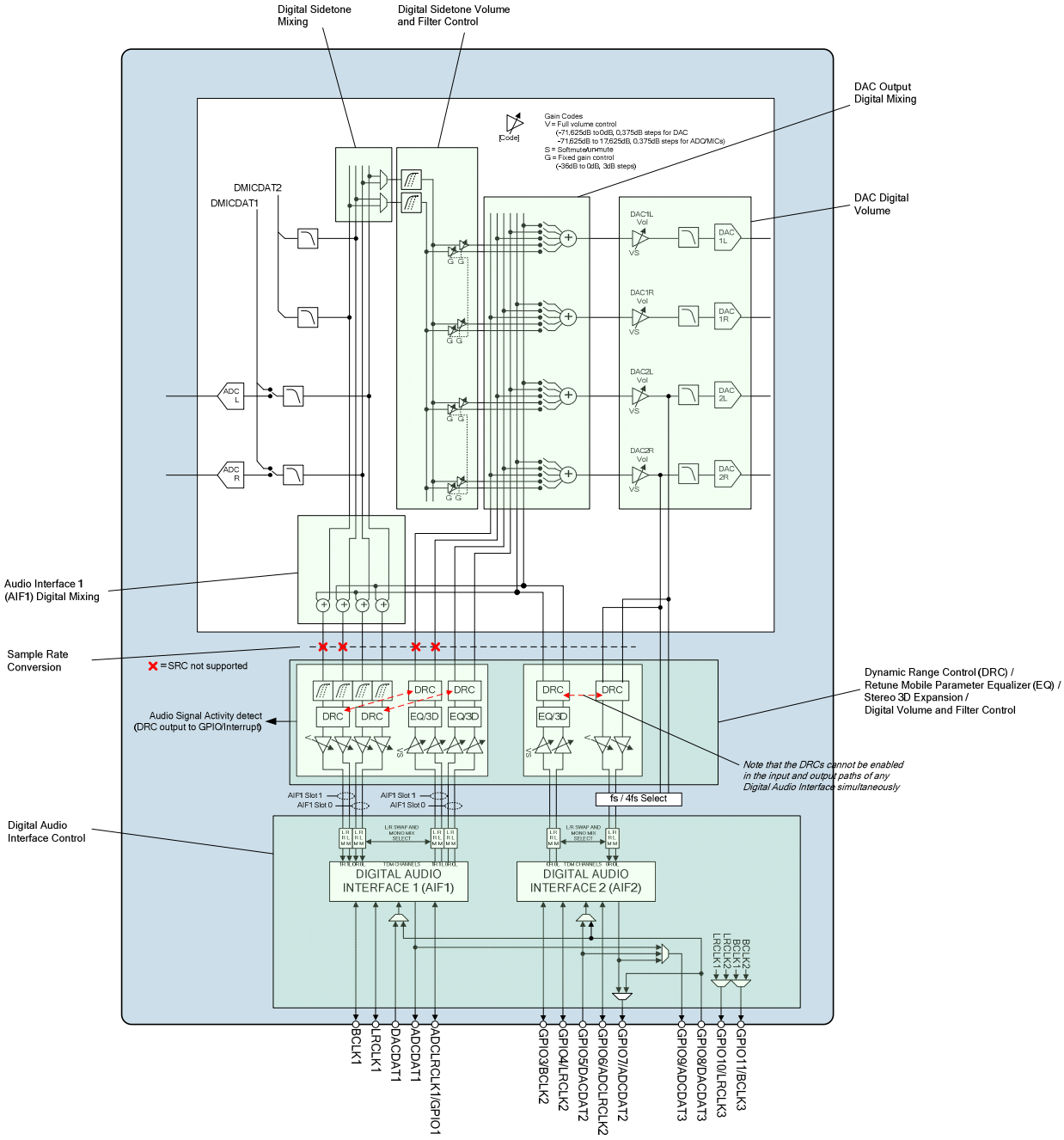


Figure 19 Digital Core Architecture

DIGITAL MIXING

This section describes the digital mixing functions of the WM8994.

Digital audio mixing is provided on four AIF1 output paths, two digital sidetone paths, and four Digital to Analogue converters (DACs).

Note that the two AIF2 output paths are connected to the DAC2L and DAC2R signal paths.

AUDIO INTERFACE 1 (AIF1) OUTPUT MIXING

There are four AIF1 digital mixers, one for each AIF1 audio channel (ie. Left/Right channels on Timeslots 0/1). The inputs to each AIF1 mixer comprise signals from the ADC / Digital Microphone inputs and from AIF2.

Note that the Left/Right channels of AIF1 can be inverted or interchanged if required; see “Digital Audio Interface Control”.

The AIF1 Left Timeslot 0 output channel is derived from the ADCL / DMIC1 (Left) and AIF2 (Left) inputs. The ADCL / DMIC1 (Left) path is enabled by ADC1L_TO_AIF1ADC1L, whilst the AIF2 (Left) path is enabled by AIF2DACL_TO_AIF1ADC1L.

The AIF1 Right Timeslot 0 output channel is derived from the ADCR / DMIC1 (Right) and AIF2 (Right) inputs. The ADCR / DMIC1 (Right) path is enabled by ADC1R_TO_AIF1ADC1R, whilst the AIF2 (Right) path is enabled by AIF2DACR_TO_AIF1ADC1R.

The AIF1 Left Timeslot 1 output channel is derived from the DMIC2 (Left) and AIF2 (Left) inputs. The DMIC2 (Left) path is enabled by ADC2L_TO_AIF1ADC2L, whilst the AIF2 (Left) path is enabled by AIF2DACL_TO_AIF1ADC2L.

The AIF1 Right Timeslot 1 output channel is derived from the DMIC2 (Right) and AIF2 (Right) inputs. The DMIC2 (Right) path is enabled by ADC2R_TO_AIF1ADC2R, whilst the AIF2 (Right) path is enabled by AIF2DACR_TO_AIF1ADC2R.

The AIF1 output mixer controls are defined in Table 12.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1542 (0606h) AIF1 ADC1 Left Mixer Routing	1	ADC1L_TO_AIF 1ADC1L	0	Enable ADCL / DMIC1 (Left) to AIF1 (Timeslot 0, Left) output 0 = Disabled 1 = Enabled
	0	AIF2DACL_TO_ AIF1ADC1L	0	Enable AIF2 (Left) to AIF1 (Timeslot 0, Left) output 0 = Disabled 1 = Enabled
R1543 (0607h) AIF1 ADC1 Right Mixer Routing	1	ADC1R_TO_AIF 1ADC1R	0	Enable ADCR / DMIC1 (Right) to AIF1 (Timeslot 0, Right) output 0 = Disabled 1 = Enabled
	0	AIF2DACR_TO_ AIF1ADC1R	0	Enable AIF2 (Right) to AIF1 (Timeslot 0, Right) output 0 = Disabled 1 = Enabled
R1544 (0608h) AIF1 ADC2 Left Mixer Routing	1	ADC2L_TO_AIF 1ADC2L	0	Enable DMIC2 (Left) to AIF1 (Timeslot 1, Left) output 0 = Disabled 1 = Enabled
	0	AIF2DACL_TO_ AIF1ADC2L	0	Enable AIF2 (Left) to AIF1 (Timeslot 1, Left) output 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1545 (0609h) AIF1 ADC2 Right Mixer Routing	1	ADC2R_TO_AIF 1ADC2R	0	Enable DMIC2 (Right) to AIF1 (Timeslot 1, Right) output 0 = Disabled 1 = Enabled
	0	AIF2DACR_TO_ AIF1ADC2R	0	Enable AIF2 (Right) to AIF1 (Timeslot 1, Right) output 0 = Disabled 1 = Enabled

Table 12 AIF1 Output Mixing

DIGITAL SIDETONE MIXING

There are two digital sidetone signal paths, ST1 and ST2. The sidetone sources are selectable for each path. The sidetone mixer outputs are inputs to the DAC signal mixers.

The source for sidetone path ST1 is ADCL / DMIC1 (Left) or ADCR / DMIC1 (Right), depending on the ST1_SEL bit.

The source for sidetone path ST2 is DMIC2 (Left) or DMIC2 (Right), depending on the ST2_SEL bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1569 (0621h) Sidetone	1	ST2_SEL	0	Select source for sidetone ST2 path 0 = DMIC2 (Left) 1 = DMIC2 (Right)
	0	ST1_SEL	0	Select source for sidetone ST1 path 0 = ADCL / DMIC1 (Left) 1 = ADCR / DMIC1 (Right)

Table 13 Digital Sidetone Mixing

DIGITAL SIDETONE VOLUME AND FILTER CONTROL

A digital volume control is provided for the digital sidetone paths. The associated register controls are described in Table 14.

A digital high-pass filter can be enabled in the sidetone paths to remove DC offsets. This filter is enabled using the ST_HPF register bit; the cut-off frequency is configured using ST_HPF_CUT. When the filter is enabled, it is enabled in both digital sidetone paths.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1536 (0600h) DAC1 Mixer Volumes	8:5	ADC2_DAC1_V OL [3:0]	0000	Sidetone ST2 to DAC1L and DAC1R Volume 0000 = -36dB 0001 = -33dB …. (3dB steps) 1011 = -3dB 1100 = 0dB (see Table 15 for gain range)
	3:0	ADC1_DAC1_V OL [3:0]	0000	Sidetone ST1 to DAC1L and DAC1R Volume 0000 = -36dB 0001 = -33dB …. (3dB steps) 1011 = -3dB 1100 = 0dB (see Table 15 for gain range)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1539 (0603h) DAC2 Mixer Volumes	8:5	ADC2_DAC2_VOL [3:0]	0000	Sidetone ST2 to DAC2L and DAC2R Volume 0000 = -36dB 0001 = -33dB …. (3dB steps) 1011 = -3dB 1100 = 0dB (see Table 15 for gain range)
	3:0	ADC1_DAC2_VOL [3:0]	0000	Sidetone ST1 to DAC2L and DAC2R Volume 0000 = -36dB 0001 = -33dB …. (3dB steps) 1011 = -3dB 1100 = 0dB (see Table 15 for gain range)
R1569 (0621h) Sidetone	9:7	ST_HPF_CUT [2:0]	000	Sidetone HPF cut-off frequency (relative to 44.1kHz sample rate) 000 = 2.7kHz 001 = 1.35kHz 010 = 675Hz 011 = 370Hz 100 = 180Hz 101 = 90Hz 110 = 45Hz 111 = Reserved Note - the cut-off frequencies scale with the Digital Mixing (SYSCLK) clocking rate. The quoted figures apply to 44.1kHz sample rate.
	6	ST_HPF	0	Digital Sidetone HPF Select 0 = Disabled 1 = Enabled

Table 14 Digital Sidetone Volume Control

ADC1_DAC1_VOL, ADC1_DAC2_VOL, ADC2_DAC1_VOL or ADC2_DAC2_VOL	SIDETONE GAIN (dB)
0000	-36
0001	-33
0010	-30
0011	-27
0100	-24
0101	-21
0110	-18
0111	-15
1000	-12
1001	-9
1010	-6
1011	-3
1100	0
1101	0
1110	0
1111	0

Table 15 Digital Sidetone Volume Range

DAC OUTPUT DIGITAL MIXING

There are four DAC digital mixers, one for each DAC. The inputs to each DAC mixer comprise signals from AIF1, AIF2 and the digital sidetone signals.

Note that the Left/Right channels of the AIF1 and AIF2 inputs can be inverted or interchanged if required; see “Digital Audio Interface Control”.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1537 (0601h) DAC1 Left Mixer Routing	5	ADC2_TO_DAC 1L	0	Enable Sidetone ST2 to DAC1L 0 = Disabled 1 = Enabled
	4	ADC1_TO_DAC 1L	0	Enable Sidetone ST1 to DAC1L 0 = Disabled 1 = Enabled
	2	AIF2DACL_TO_ DAC1L	0	Enable AIF2 (Left) to DAC1L 0 = Disabled 1 = Enabled
	1	AIF1DAC2L_TO _DAC1L	0	Enable AIF1 (Timeslot 1, Left) to DAC1L 0 = Disabled 1 = Enabled
	0	AIF1DAC1L_TO _DAC1L	0	Enable AIF1 (Timeslot 0, Left) to DAC1L 0 = Disabled 1 = Enabled
R1538 (0602h) DAC1 Right Mixer Routing	5	ADC2_TO_DAC 1R	0	Enable Sidetone ST2 to DAC1R 0 = Disabled 1 = Enabled
	4	ADC1_TO_DAC 1R	0	Enable Sidetone ST1 to DAC1R 0 = Disabled 1 = Enabled
	2	AIF2DACR_TO_ DAC1R	0	Enable AIF2 (Right) to DAC1R 0 = Disabled 1 = Enabled
	1	AIF1DAC2R_TO _DAC1R	0	Enable AIF1 (Timeslot 1, Right) to DAC1R 0 = Disabled 1 = Enabled
	0	AIF1DAC1R_TO _DAC1R	0	Enable AIF1 (Timeslot 0, Right) to DAC1R 0 = Disabled 1 = Enabled
R1540 (0604h) DAC2 Left Mixer Routing	5	ADC2_TO_DAC 2L	0	Enable Sidetone ST2 to DAC2L 0 = Disabled 1 = Enabled
	4	ADC1_TO_DAC 2L	0	Enable Sidetone ST1 to DAC2L 0 = Disabled 1 = Enabled
	2	AIF2DACL_TO_ DAC2L	0	Enable AIF2 (Left) to DAC2L 0 = Disabled 1 = Enabled
	1	AIF1DAC2L_TO _DAC2L	0	Enable AIF1 (Timeslot 1, Left) to DAC2L 0 = Disabled 1 = Enabled
	0	AIF1DAC1L_TO	0	Enable AIF1 (Timeslot 0, Left) to

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
		_DAC2L		DAC2L 0 = Disabled 1 = Enabled
R1541 (0605h) DAC2 Right Mixer Routing	5	ADC2_TO_DAC 2R	0	Enable Sidetone ST2 to DAC2R 0 = Disabled 1 = Enabled
	4	ADC1_TO_DAC 2R	0	Enable Sidetone ST1 to DAC2R 0 = Disabled 1 = Enabled
	2	AIF2DACR_TO_ DAC2R	0	Enable AIF2 (Right) to DAC2R 0 = Disabled 1 = Enabled
	1	AIF1DAC2R_TO _DAC2R	0	Enable AIF1 (Timeslot 1, Right) to DAC2R 0 = Disabled 1 = Enabled
	0	AIF1DAC1R_TO _DAC2R	0	Enable AIF1 (Timeslot 0, Right) to DAC2R 0 = Disabled 1 = Enabled

Table 16 DAC Output Digital Mixing

AUDIO INTERFACE 2 (AIF2) DIGITAL MIXING

There are two output channels on AIF2. The audio source for these two channels is the same as the selected source for DAC2L and DAC2R, as described in “DAC Output Digital Mixing”.

Note that the Left/Right channels of AIF2 can be inverted or interchanged if required; see “Digital Audio Interface Control”.

SAMPLE RATE CONVERSION

The WM8994 supports two main digital audio interfaces, AIF1 and AIF2. These interfaces are configured independently and may operate entirely asynchronously to each other. The WM8994 performs stereo full-duplex sample rate conversion between the audio interfaces, allowing digital audio to be routed between the interfaces, and allowing asynchronous audio data to be mixed together.

The Sample Rate Converters (SRCs) are configured and enabled automatically within the WM8994, and no user settings are required. Synchronisation between the audio interfaces is not instantaneous when the clocking or sample rate configurations are updated; the lock status of the SRCs is signalled via the GPIO or Interrupt circuits, as described in “General Purpose Input/Output” and “Interrupts”.

Separate clocks can be used for AIF1 and AIF2, allowing asynchronous operation on these interfaces. The digital mixing core is clocked by SYSCLK, which is linked to either AIF1CLK or AIF2CLK, as described in “Clocking and Sample Rates”. The digital mixing core is, therefore, always synchronised to AIF1, or to AIF2, or to both interfaces at once.

SAMPLE RATE CONVERTER 1 (SRC1)

SRC1 performs sample rate conversion of digital audio data input to the WM8994. Sample Rate Conversion is required when digital audio data is received on an audio interface that is not synchronised to the digital mixing core.

SRC1 is automatically configured on AIF1 or AIF2, depending on the selected Clocking and Sample Rate configuration. Note that SRC1 cannot convert input data on AIF1 and AIF2 simultaneously. Sample Rate conversion on AIF1 is only supported on TDM Timeslot 0.

The SRC1 Lock status indicates when audio data can be received on the interface channel that is not synchronised to the digital mixing core. No audio will be present on this signal path until SRC1 Lock is achieved.

SAMPLE RATE CONVERTER 1 (SRC2)

SRC2 performs sample rate conversion of digital audio data output from the WM8994. Sample Rate Conversion is required when digital audio data is transmitted on an audio interface that is not synchronised to the digital mixing core.

SRC2 is automatically configured on AIF1 or AIF2, depending on the selected Clocking and Sample Rate configuration. Note that SRC2 cannot convert output data on AIF1 and AIF2 simultaneously. Sample Rate conversion on AIF1 is only supported on TDM Timeslot 0.

The SRC2 Lock status indicates when audio data can be transmitted on the interface channel that is not synchronised to the digital mixing core. No audio will be present on this signal path until SRC2 Lock is achieved.

SAMPLE RATE CONVERTER RESTRICTIONS

The following restrictions apply to the configuration of the WM8994 Sample Rate Converters.

No SRC on AIF1 Timeslot 1. Sample Rate Conversion on audio interface AIF1 is not supported on the TDM Timeslot 1. Therefore, it is not possible to route digital audio between AIF1 Timeslot 1 and AIF2, or to mix together audio from these interface paths. Note that this only applies when the SRC is applied to AIF1.

Maximum of three sample rates in the system. The audio sample rate of AIF1 input and AIF1 output may be different to each other. The audio sample rate of AIF2 input and AIF2 output may be different to each other. However, it is not possible to have four different sample rates operating simultaneously, as this would require sample rate conversion in too many paths. A maximum of three different sample rates can be supported in the system.

No SRC capability when using 88.2kHz or 96kHz AIF input (DAC playback). If either interface is configured for 88.2kHz or 96kHz sample rate, then the digital mixing core must also be configured for this sample rate. Sample Rate Conversion cannot be supported in this mode, therefore AIF output is not supported at any sample rate under these conditions.

Restricted Sample Rate options when AIF1 and AIF2 are synchronised. When the same clock source is used for AIF1CLK and AIF2CLK, then the AIF to which the SYSCLK is synchronised cannot be mixed sample rates. If AIF1CLK_SRC = AIF2CLK_SRC and SYSCLK_SRC = 0, then AIF1 cannot support mixed sample rates. If AIF1CLK_SRC = AIF2CLK_SRC and SYSCLK_SRC = 1, then AIF2 cannot support mixed sample rates.

Restricted Sample Rate options when AIF1 and AIF2 are not synchronised. When a different clock source is used for AIF1CLK and AIF2CLK, and mixed sample rates are selected on both interfaces, then the DAC sample rate of one interface must be the same as the ADC sample rate of the other.

SAMPLE RATE CONVERTER CONFIGURATION ERROR INDICATION

The WM8894 verifies the register settings relating to Clocking, Sample Rates and Sample Rate Conversion. If an invalid configuration is attempted, then the SR_ERROR register will indicate the error by showing a non-zero value. This read-only field may be checked to confirm that the WM8994 can support the selected Clocking and Sample Rate settings.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R530 (0212h) Rate Status	3:0	SR_ERROR [3:0]	0000	Sample Rate Configuration status Indicates an error with the register settings related to sample rate configuration 0000 = No errors 0001 = Invalid sample rate 0010 = Invalid AIF divide 0011 = ADC and DAC divides both set in an interface 0100 = Invalid combination of AIF divides and sample-rate 0101 = Invalid set of enables for 96kHz mode 0110 = Invalid SYSCLK rate (derived from AIF1CLK_RATE or AIF2CLK_RATE) 0111 = Mixed ADC and DAC rates in SYSCLK AIF when AIFs are asynchronous 1000 = Invalid combination of sample rates when both AIFs are from the same clock source 1001 = Invalid combination of mixed ADC/DAC AIFs when both from the same clock source 1010 = AIF1DAC2 (Timeslot 1) ports enabled when SRCs connected to AIF1

Table 17 Sample Rate Converter Configuration Status

DYNAMIC RANGE CONTROL (DRC)

The Dynamic Range Control (DRC) is a circuit which can be enabled in the digital playback or digital record paths of the WM8994 audio interfaces. The function of the DRC is to adjust the signal gain in conditions where the input amplitude is unknown or varies over a wide range, e.g. when recording from microphones built into a handheld system. The DRC can apply Compression and Automatic Level Control to the signal path. It incorporates 'anti-clip' and 'quick release' features for handling transients in order to improve intelligibility in the presence of loud impulsive noises.

The DRC can apply Compression and Automatic Level Control to the signal path. It incorporates 'anti-clip' and 'quick release' features for handling transients in order to improve intelligibility in the presence of loud impulsive noises.

The DRC also incorporates a Noise Gate function, which provides additional attenuation of very low-level input signals. This means that the signal path is quiet when no signal is present, giving an improvement in background noise level under these conditions.

The WM8994 provides three stereo Dynamic Range Controllers (DRCs); these are associated with AIF1 timeslot 0, AIF1 timeslot 1 and AIF2 respectively. Each DRC can be enabled either in the DAC playback (AIF input) path or in the ADC record (AIF output) path, as described in the "Digital Core Architecture" section.

The DRCs are enabled in the DAC or ADCs audio signal paths using the register bits described in Table 18. Note that enabling any DRC in the DAC and ADC paths simultaneously is an invalid selection.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1088 (0440h) AIF1 DRC1 (1)	2	AIF1DAC1_DRC_ENA	0	Enable DRC in AIF1DAC1 playback path (AIF1, Timeslot 0) 0 = Disabled 1 = Enabled
	1	AIF1ADC1L_DRC_ENA	0	Enable DRC in AIF1ADC1 (Left) record path (AIF1, Timeslot 0) 0 = Disabled 1 = Enabled
	0	AIF1ADC1R_DRC_ENA	0	Enable DRC in AIF1ADC1 (Right) record path (AIF1, Timeslot 0) 0 = Disabled 1 = Enabled
R1104 (0450h) AIF1 DRC2 (1)	2	AIF1DAC2_DRC_ENA	0	Enable DRC in AIF1DAC2 playback path (AIF1, Timeslot 1) 0 = Disabled 1 = Enabled
	1	AIF1ADC2L_DRC_ENA	0	Enable DRC in AIF1ADC2 (Left) record path (AIF1, Timeslot 1) 0 = Disabled 1 = Enabled
	0	AIF1ADC2R_DRC_ENA	0	Enable DRC in AIF1ADC2 (Right) record path (AIF1, Timeslot 1) 0 = Disabled 1 = Enabled
R1344 (0550h) AIF2 DRC (1)	2	AIF2DAC_DRC_ENA	0	Enable DRC in AIF2DAC playback path 0 = Disabled 1 = Enabled
	1	AIF2ADCL_DRC_ENA	0	Enable DRC in AIF2ADC (Left) record path 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	0	AIF2ADCR_DRC_ENA	0	Enable DRC in AIF2ADC (Right) record path 0 = Disabled 1 = Enabled

Table 18 DRC Enable

The following description of the DRC is applicable to all three DRCs. The associated register control fields are described in Table 20, Table 21 and Table 22 for the respective DRCs.

Note that, there the following description refers to register names, the generic prefix *[DRC]* is quoted:

- For the DRC associated with AIF1 timeslot 0, *[DRC]* = AIF1DRC1.
- For the DRC associated with AIF1 timeslot 1, *[DRC]* = AIF1DRC2.
- For the DRC associated with AIF2, *[DRC]* = AIF2DRC.

DRC COMPRESSION / EXPANSION / LIMITING

The DRC supports two different compression regions, separated by a "Knee" at a specific input amplitude. In the region above the knee, the compression slope *[DRC]*_HI_COMP applies; in the region below the knee, the compression slope *[DRC]*_LO_COMP applies.

The DRC also supports a noise gate region, where low-level input signals are heavily attenuated. This function can be enabled or disabled according to the application requirements. The DRC response in this region is defined by the expansion slope *[DRC]*_NG_EXP.

For additional attenuation of signals in the noise gate region, an additional "knee" can be defined (shown as "Knee2" in Figure 20). When this knee is enabled, this introduces an infinitely steep drop-off in the DRC response pattern between the *[DRC]*_LO_COMP and *[DRC]*_NG_EXP regions.

The overall DRC compression characteristic in "steady state" (i.e. where the input amplitude is near-constant) is illustrated in Figure 20.

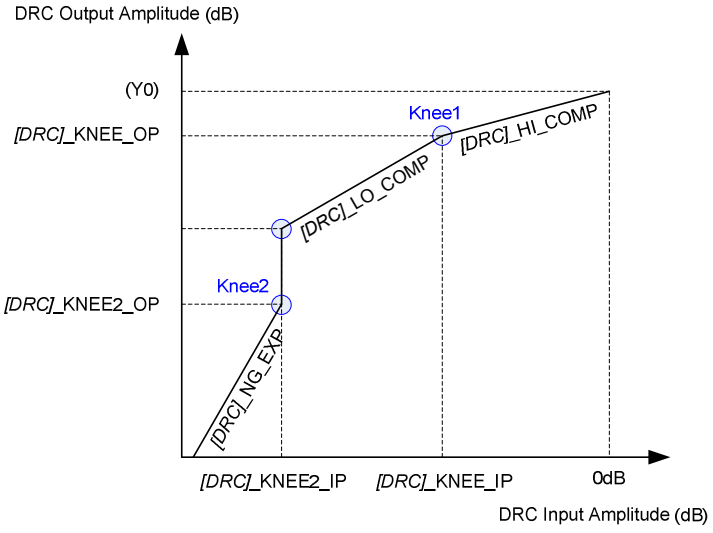


Figure 20 DRC Response Characteristic

The slope of the DRC response is determined by register fields *[DRC]*_HI_COMP and *[DRC]*_LO_COMP. A slope of 1 indicates constant gain in this region. A slope less than 1 represents compression (i.e. a change in input amplitude produces only a smaller change in output amplitude). A slope of 0 indicates that the target output amplitude is the same across a range of input amplitudes; this is infinite compression.

When the noise gate is enabled, the DRC response in this region is determined by the *[DRC]*_NG_EXP register. A slope of 1 indicates constant gain in this region. A slope greater than 1 represents expansion (ie. a change in input amplitude produces a larger change in output amplitude).

When the DRC_KNEE2_OP knee is enabled ("Knee2" in Figure 20), this introduces the vertical line in the response pattern illustrated, resulting in infinitely steep attenuation at this point in the response.

The DRC parameters are listed in Table 19.

REF	PARAMETER	DESCRIPTION
1	*[DRC]*_KNEE_IP	Input level at Knee1 (dB)
2	*[DRC]*_KNEE_OP	Output level at Knee2 (dB)
3	*[DRC]*_HI_COMP	Compression ratio above Knee1
4	*[DRC]*_LO_COMP	Compression ratio below Knee1
5	*[DRC]*_KNEE2_IP	Input level at Knee2 (dB)
6	*[DRC]*_NG_EXP	Expansion ratio below Knee2
7	*[DRC]*_KNEE2_OP	Output level at Knee2 (dB)

Table 19 DRC Response Parameters

The noise gate is enabled when the *[DRC]*_NG_ENA register is set. When the noise gate is not enabled, parameters 5, 6, 7 above are ignored, and the *[DRC]*_LO_COMP slope applies to all input signal levels below Knee1.

The DRC_KNEE2_OP knee is enabled when the *[DRC]*_KNEE2_OP_ENA register is set. When this bit is not set, then parameter 7 above is ignored, and the Knee2 position always coincides with the low end of the *[DRC]*_LO_COMP region.

The "Knee1" point in Figure 20 is determined by register fields *[DRC]*_KNEE_IP and *[DRC]*_KNEE_OP.

Parameter Y0, the output level for a 0dB input, is not specified directly, but can be calculated from the other parameters, using the equation:

$$Y0 = [DRC]\_KNEE\_OP - ([DRC]\_KNEE\_IP * [DRC]\_HI\_COMP)$$

GAIN LIMITS

The minimum and maximum gain applied by the DRC is set by register fields *[DRC]*_MINGAIN, *[DRC]*_MAXGAIN and *[DRC]*_NG_MINGAIN. These limits can be used to alter the DRC response from that illustrated in Figure 20. If the range between maximum and minimum gain is reduced, then the extent of the dynamic range control is reduced.

The minimum gain in the Compression regions of the DRC response is set by *[DRC]*_MINGAIN. The mimimum gain in the Noise Gate region is set by *[DRC]*_NG_MINGAIN. The minimum gain limit prevents excessive attenuation of the signal path.

The maximum gain limit set by *[DRC]*_MAXGAIN prevents quiet signals (or silence) from being excessively amplified.

DYNAMIC CHARACTERISTICS

The dynamic behaviour determines how quickly the DRC responds to changing signal levels. Note that the DRC responds to the average (RMS) signal amplitude over a period of time.

The *[DRC]*_ATK determines how quickly the DRC gain decreases when the signal amplitude is high. The *[DRC]*_DCY determines how quickly the DRC gain increases when the signal amplitude is low.

These register fields are described in Table 20, Table 21 and Table 22. Note that the register defaults are suitable for general purpose microphone use.

ANTI-CLIP CONTROL

The DRC includes an Anti-Clip feature to avoid signal clipping when the input amplitude rises very quickly. This feature uses a feed-forward technique for early detection of a rising signal level. Signal clipping is avoided by dynamically increasing the gain attack rate when required. The Anti-Clip feature is enabled using the *[DRC]*_ANTICLIP bit.

Note that the feed-forward processing increases the latency in the input signal path.

Note that the Anti-Clip feature operates entirely in the digital domain. It cannot be used to prevent signal clipping in the analogue domain nor in the source signal. Analogue clipping can only be prevented by reducing the analogue signal gain or by adjusting the source signal.

QUICK RELEASE CONTROL

The DRC includes a Quick-Release feature to handle short transient peaks that are not related to the intended source signal. For example, in handheld microphone recording, transient signal peaks sometimes occur due to user handling, key presses or accidental tapping against the microphone. The Quick Release feature ensures that these transients do not cause the intended signal to be masked by the longer time constants of *[DRC]*_DCY.

The Quick-Release feature is enabled by setting the *[DRC]*_QR bit. When this bit is enabled, the DRC measures the crest factor (peak to RMS ratio) of the input signal. A high crest factor is indicative of a transient peak that may not be related to the intended source signal. If the crest factor exceeds the level set by *[DRC]*_QR_THR, then the normal decay rate (*[DRC]*_DCY) is ignored and a faster decay rate (*[DRC]*_QR_DCY) is used instead.

SIGNAL ACTIVITY DETECT

The DRC incorporates a configurable signal detect function, allowing the signal level at the DRC input to be monitored and to be used to trigger other events. This can be used to detect the presence of a microphone signal on an ADC or digital mic channel, or can be used to detect an audio signal received over the digital audio interface.

The Peak signal level or the RMS signal level of the DRC input can be selected as the detection threshold. When the threshold condition is exceeded, an interrupt or GPIO output can be generated. See “General Purpose Input/Output” for a full description of the applicable control fields.

DRC REGISTER CONTROLS

The AIF1DRC1 control registers are described in Table 20. The AIF1DRC2 control registers are described in Table 21. The AIF2DRC control registers are described in Table 22.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1080 (0440h) AIF1 DRC1 (1)	8	AIF1DRC1_NG_ ENA	0	AIF1 DRC1 Noise Gate Enable 0 = Disabled 1 = Enabled
	5	AIF1DRC1_KNE E2_OP_ENA	0	AIF1 DRC1 KNEE2_OP Enable 0 = Disabled 1 = Enabled
	4	AIF1DRC1_QR	1	AIF1 DRC1 Quick-release Enable 0 = Disabled 1 = Enabled
	3	AIF1DRC1_ANT ICLIP	1	AIF1 DRC1 Anti-clip Enable 0 = Disabled 1 = Enabled
R1081 (0441h) AIF1 DRC1 (2)	12:9	AIF1DRC1_ATK [3:0]	0100	AIF1 DRC1 Gain attack rate (seconds/6dB) 0000 = Reserved 0001 = 181us 0010 = 363us 0011 = 726us 0100 = 1.45ms 0101 = 2.9ms 0110 = 5.8ms 0111 = 11.6ms 1000 = 23.2ms 1001 = 46.4ms 1010 = 92.8ms 1011 = 185.6ms 1100-1111 = Reserved
	8:5	AIF1DRC1_DCY [3:0]	0010	AIF1 DRC1 Gain decay rate (seconds/6dB) 0000 = 186ms 0001 = 372ms 0010 = 743ms 0011 = 1.49s 0100 = 2.97s 0101 = 5.94s 0110 = 11.89s 0111 = 23.78s 1000 = 47.56s 1001-1111 = Reserved
	4:2	AIF1DRC1_MIN GAIN [2:0]	001	AIF1 DRC1 Minimum gain to attenuate audio signals 000 = 0dB 001 = -12dB (default) 010 = -18dB 011 = -24dB 100 = -36dB 101 = Reserved 11X = Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1:0	AIF1DRC1_MAX GAIN [1:0]	01	AIF1 DRC1 Maximum gain to boost audio signals (dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 36dB
R1082 (0442h) AIF1 DRC1 (3)	15:12	AIF1DRC1_NG_ MINGAIN [3:0]	0000	AIF1 DRC1 Minimum gain to attenuate audio signals when the noise gate is active. 0000 = -36dB 0001 = -30dB 0010 = -24dB 0011 = -18dB 0100 = -12dB 0101 = -6dB 0110 = 0dB 0111 = 6dB 1000 = 12dB 1001 = 18dB 1010 = 24dB 1011 = 30dB 1100 = 36dB 1101 to 1111 = Reserved
	11:10	AIF1DRC1_NG_ EXP [1:0]	00	AIF1 DRC1 Noise Gate slope 00 = 1 (no expansion) 01 = 2 10 = 4 11 = 8
	9:8	AIF1DRC1_QR_ THR [1:0]	00	AIF1 DRC1 Quick-release threshold (crest factor in dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB
	7:6	AIF1DRC1_QR_ DCY [1:0]	00	AIF1 DRC1 Quick-release decay rate (seconds/6dB) 00 = 0.725ms 01 = 1.45ms 10 = 5.8ms 11 = reserved
	5:3	AIF1DRC1_HI_ COMP [2:0]	000	AIF1 DRC1 Compressor slope (upper region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 0 110 = Reserved 111 = Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	2:0	AIF1DRC1_LO_COMP [2:0]	000	AIF1 DRC1 Compressor slope (lower region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 0 101 = Reserved 11X = Reserved
R1083 (0443h) AIF1 DRC1 (4)	10:5	AIF1DRC1_KNEE_IP [5:0]	000000	AIF1 DRC1 Input signal level at the Compressor 'Knee'. 000000 = 0dB 000001 = -0.75dB 000010 = -1.5dB … (-0.75dB steps) 111100 = -45dB 111101 = Reserved 11111X = Reserved
	4:0	AIF1DRC1_KNEE_OP [4:0]	00000	AIF1 DRC1 Output signal at the Compressor 'Knee'. 00000 = 0dB 00001 = -0.75dB 00010 = -1.5dB … (-0.75dB steps) 11110 = -22.5dB 11111 = Reserved
R1084 (0444h) AIF1 DRC1 (5)	9:5	AIF1DRC1_KNEE2_IP [4:0]	00000	AIF1 DRC1 Input signal level at the Noise Gate threshold 'Knee2'. 00000 = -36dB 00001 = -37.5dB 00010 = -39dB … (-1.5dB steps) 11110 = -81dB 11111 = -82.5dB Only applicable when DRC_NG_ENA = 1.
	4:0	AIF1DRC1_KNEE2_OP [4:0]	00000	AIF1 DRC1 Output signal at the Noise Gate threshold 'Knee2'. 00000 = -30dB 00001 = -31.5dB 00010 = -33dB … (-1.5dB steps) 11110 = -75dB 11111 = -76.5dB Only applicable when DRC_KNEE2_OP_ENA = 1.

Table 20 AIF1 Timeslot 0 DRC Controls

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1104 (0450h) AIF1 DRC2 (1)	8	AIF1DRC2_NG_ENA	0	AIF1 DRC2 Noise Gate Enable 0 = Disabled 1 = Enabled
	5	AIF1DRC2_KNEE2_OP_ENA	0	AIF1 DRC2 KNEE2_OP Enable 0 = Disabled 1 = Enabled
	4	AIF1DRC2_QR	1	AIF1 DRC2 Quick-release Enable 0 = Disabled 1 = Enabled
	3	AIF1DRC2_ANTICLIP	1	AIF1 DRC2 Anti-clip Enable 0 = Disabled 1 = Enabled
R1105 (0451h) AIF1 DRC2 (2)	12:9	AIF1DRC2_ATK [3:0]	0100	AIF1 DRC2 Gain attack rate (seconds/6dB) 0000 = Reserved 0001 = 181us 0010 = 363us 0011 = 726us 0100 = 1.45ms 0101 = 2.9ms 0110 = 5.8ms 0111 = 11.6ms 1000 = 23.2ms 1001 = 46.4ms 1010 = 92.8ms 1011 = 185.6ms 1100-1111 = Reserved
	8:5	AIF1DRC2_DCY [3:0]	0010	AIF1 DRC2 Gain decay rate (seconds/6dB) 0000 = 186ms 0001 = 372ms 0010 = 743ms 0011 = 1.49s 0100 = 2.97s 0101 = 5.94s 0110 = 11.89s 0111 = 23.78s 1000 = 47.56s 1001-1111 = Reserved
	4:2	AIF1DRC2_MINGAIN [2:0]	001	AIF1 DRC2 Minimum gain to attenuate audio signals 000 = 0dB 001 = -12dB (default) 010 = -18dB 011 = -24dB 100 = -36dB 101 = Reserved 11X = Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1:0	AIF1DRC2_MAX GAIN [1:0]	01	AIF1 DRC2 Maximum gain to boost audio signals (dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 36dB
R1106 (0452h) AIF1 DRC2 (3)	15:12	AIF1DRC2_NG_ MINGAIN [3:0]	0000	AIF1 DRC2 Minimum gain to attenuate audio signals when the noise gate is active. 0000 = -36dB 0001 = -30dB 0010 = -24dB 0011 = -18dB 0100 = -12dB 0101 = -6dB 0110 = 0dB 0111 = 6dB 1000 = 12dB 1001 = 18dB 1010 = 24dB 1011 = 30dB 1100 = 36dB 1101 to 1111 = Reserved
	11:10	AIF1DRC2_NG_ EXP [1:0]	00	AIF1 DRC2 Noise Gate slope 00 = 1 (no expansion) 01 = 2 10 = 4 11 = 8
	9:8	AIF1DRC2_QR_ THR [1:0]	00	AIF1 DRC2 Quick-release threshold (crest factor in dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB
	7:6	AIF1DRC2_QR_ DCY [1:0]	00	AIF1 DRC2 Quick-release decay rate (seconds/6dB) 00 = 0.725ms 01 = 1.45ms 10 = 5.8ms 11 = reserved
	5:3	AIF1DRC2_HI_ COMP [2:0]	000	AIF1 DRC2 Compressor slope (upper region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 0 110 = Reserved 111 = Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	2:0	AIF1DRC2_LO_COMP [2:0]	000	AIF1 DRC2 Compressor slope (lower region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 0 101 = Reserved 11X = Reserved
R1107 (0453h) AIF1 DRC2 (4)	10:5	AIF1DRC2_KNEE_IP [5:0]	000000	AIF1 DRC2 Input signal level at the Compressor 'Knee'. 000000 = 0dB 000001 = -0.75dB 000010 = -1.5dB … (-0.75dB steps) 111100 = -45dB 111101 = Reserved 11111X = Reserved
	4:0	AIF1DRC2_KNEE_OP [4:0]	00000	AIF1 DRC2 Output signal at the Compressor 'Knee'. 00000 = 0dB 00001 = -0.75dB 00010 = -1.5dB … (-0.75dB steps) 11110 = -22.5dB 11111 = Reserved
R1108 (0454h) AIF1 DRC2 (5)	9:5	AIF1DRC2_KNEE2_IP [4:0]	00000	AIF1 DRC2 Input signal level at the Noise Gate threshold 'Knee2'. 00000 = -36dB 00001 = -37.5dB 00010 = -39dB … (-1.5dB steps) 11110 = -81dB 11111 = -82.5dB Only applicable when DRC_NG_ENA = 1.
	4:0	AIF1DRC2_KNEE2_OP [4:0]	00000	AIF1 DRC2 Output signal at the Noise Gate threshold 'Knee2'. 00000 = -30dB 00001 = -31.5dB 00010 = -33dB … (-1.5dB steps) 11110 = -75dB 11111 = -76.5dB Only applicable when DRC_KNEE2_OP_ENA = 1.

Table 21 AIF1 Timeslot 1 DRC Controls

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1344 (0540h) AIF2 DRC (1)	8	AIF2DRC_NG_ENA	0	AIF2 DRC Noise Gate Enable 0 = Disabled 1 = Enabled
	5	AIF2DRC_KNEE2_OP_ENA	0	AIF2 DRC KNEE2_OP Enable 0 = Disabled 1 = Enabled
	4	AIF2DRC_QR	1	AIF2 DRC Quick-release Enable 0 = Disabled 1 = Enabled
	3	AIF2DRC_ANTICLIP	1	AIF2 DRC Anti-clip Enable 0 = Disabled 1 = Enabled
R1345 (0541h) AIF2 DRC (2)	12:9	AIF2DRC_ATK [3:0]	0100	AIF2 DRC Gain attack rate (seconds/6dB) 0000 = Reserved 0001 = 181us 0010 = 363us 0011 = 726us 0100 = 1.45ms 0101 = 2.9ms 0110 = 5.8ms 0111 = 11.6ms 1000 = 23.2ms 1001 = 46.4ms 1010 = 92.8ms 1011 = 185.6ms 1100-1111 = Reserved
	8:5	AIF2DRC_DCY [3:0]	0010	AIF2 DRC Gain decay rate (seconds/6dB) 0000 = 186ms 0001 = 372ms 0010 = 743ms 0011 = 1.49s 0100 = 2.97s 0101 = 5.94s 0110 = 11.89s 0111 = 23.78s 1000 = 47.56s 1001-1111 = Reserved
	4:2	AIF2DRC_MINGAIN [2:0]	001	AIF2 DRC Minimum gain to attenuate audio signals 000 = 0dB 001 = -12dB (default) 010 = -18dB 011 = -24dB 100 = -36dB 101 = Reserved 11X = Reserved
	1:0	AIF2DRC_MAXGAIN [1:0]	01	AIF2 DRC Maximum gain to boost audio signals (dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 36dB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1346 (0542h) AIF2 DRC (3)	15:12	AIF2DRC_NG_ MINGAIN [3:0]	0000	AIF2 DRC Minimum gain to attenuate audio signals when the noise gate is active. 0000 = -36dB 0001 = -30dB 0010 = -24dB 0011 = -18dB 0100 = -12dB 0101 = -6dB 0110 = 0dB 0111 = 6dB 1000 = 12dB 1001 = 18dB 1010 = 24dB 1011 = 30dB 1100 = 36dB 1101 to 1111 = Reserved
	11:10	AIF2DRC_NG_E XP [1:0]	00	AIF2 DRC Noise Gate slope 00 = 1 (no expansion) 01 = 2 10 = 4 11 = 8
	9:8	AIF2DRC_QR_T HR [1:0]	00	AIF2 DRC Quick-release threshold (crest factor in dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB
	7:6	AIF2DRC_QR_D CY [1:0]	00	AIF2 DRC Quick-release decay rate (seconds/6dB) 00 = 0.725ms 01 = 1.45ms 10 = 5.8ms 11 = reserved
	5:3	AIF2DRC_HI_C OMP [2:0]	000	AIF2 DRC Compressor slope (upper region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 0 110 = Reserved 111 = Reserved
	2:0	AIF2DRC_LO_C OMP [2:0]	000	AIF2 DRC Compressor slope (lower region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 0 101 = Reserved 11X = Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1347 (0543h) AIF2 DRC (4)	10:5	AIF2DRC_KNEE_IP [5:0]	000000	AIF2 DRC Input signal level at the Compressor 'Knee'. 000000 = 0dB 000001 = -0.75dB 000010 = -1.5dB … (-0.75dB steps) 111100 = -45dB 111101 = Reserved 11111X = Reserved
	4:0	AIF2DRC_KNEE_OP [4:0]	00000	AIF2 DRC Output signal at the Compressor 'Knee'. 00000 = 0dB 00001 = -0.75dB 00010 = -1.5dB … (-0.75dB steps) 11110 = -22.5dB 11111 = Reserved
R1348 (0544h) AIF2 DRC (5)	9:5	AIF2DRC_KNEE2_IP [4:0]	00000	AIF2 DRC Input signal level at the Noise Gate threshold 'Knee2'. 00000 = -36dB 00001 = -37.5dB 00010 = -39dB … (-1.5dB steps) 11110 = -81dB 11111 = -82.5dB Only applicable when DRC_NG_ENA = 1.
	4:0	AIF2DRC_KNEE2_OP [4:0]	00000	AIF2 DRC Output signal at the Noise Gate threshold 'Knee2'. 00000 = -30dB 00001 = -31.5dB 00010 = -33dB … (-1.5dB steps) 11110 = -75dB 11111 = -76.5dB Only applicable when DRC_KNEE2_OP_ENA = 1.

Table 22 AIF2 DRC Controls

RETUNE™ MOBILE PARAMETRIC EQUALIZER (EQ)

The ReTune™ Mobile Parametric EQ is a circuit which can be enabled in the digital playback path of the WM8994 audio interfaces. The function of the EQ is to adjust the frequency characteristic of the output in order to compensate for unwanted frequency characteristics in the loudspeaker (or other output transducer). It can also be used to tailor the response according to user preferences, for example to accentuate or attenuate specific frequency bands to emulate different sound profiles or environments e.g. concert hall, rock etc.

The WM8994 provides three stereo EQ circuits; these are associated with AIF1 timeslot 0, AIF1 timeslot 1 and AIF2 respectively. The EQ is enabled in these three signal paths using the register bits described in Table 23.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1152 (0480h) AIF1 DAC1 EQ Gains (1)	0	AIF1DAC1_EQ_ENA	0	Enable EQ in AIF1DAC1 playback path (AIF1, Timeslot 0) 0 = Disabled 1 = Enabled
R1184 (04A0h) AIF1 DAC2 EQ Gains (1)	0	AIF1DAC2_EQ_ENA	0	Enable EQ in AIF1DAC2 playback path (AIF1, Timeslot 1) 0 = Disabled 1 = Enabled
R1408 (0580h) AIF2 EQ Gains (1)	0	AIF2DAC_EQ_ENA	0	Enable EQ in AIF2DAC playback path 0 = Disabled 1 = Enabled

Table 23 ReTune™ Mobile Parametric EQ Enable

The following description of the EQ is applicable to all three EQ circuits. The associated register control fields are described in Table 25, Table 26 and Table 27 for the respective EQs.

The EQ can be configured to operate in two modes - "Default" mode or "ReTune™ Mobile" mode.

DEFAULT MODE (5-BAND PARAMETRIC EQ)

In default mode, the cut-off / centre frequencies are fixed as per Table 24. The filter bandwidths are also fixed in default mode. The gain of the individual bands (-12dB to +12dB) can be controlled as described in Table 25.

The cut-off / centre frequencies noted in Table 24 are applicable to a sample rate of 48kHz. When using other sample rates, these frequencies will be scaled in proportion to the selected sample rate for the associated Audio Interface (AIF1 or AIF2).

If AIF1 and AIF2 are operating at different sample rates, then the cut-off / centre frequencies will be different for the two interfaces. Note that the frequencies can be set to other values by using the features described in "ReTune™ Mobile Mode".

EQ BAND	CUT-OFF/CENTRE FREQUENCY
1	100 Hz
2	300 Hz
3	875 Hz
4	2400 Hz
5	6900 Hz

Table 24 EQ Band Cut-off / Centre Frequencies

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1152 (0480h) AIF1 DAC1 EQ Gains (1)	15:11	AIF1DAC1_EQ_B1_GAIN [4:0]	00000 (-12dB)	AIF1DAC1 (AIF1, Timeslot 0) EQ Band 1 Gain (see Table 28 for gain range)
	10:6	AIF1DAC1_EQ_B2_GAIN [4:0]	00000 (-12dB)	AIF1DAC1 (AIF1, Timeslot 0) EQ Band 2 Gain (see Table 28 for gain range)
	5:1	AIF1DAC1_EQ_B3_GAIN [4:0]	00000 (-12dB)	AIF1DAC1 (AIF1, Timeslot 0) EQ Band 3 Gain (see Table 28 for gain range)
R1153 (0481h) AIF1 DAC1 EQ Gains (2)	15:11	AIF1DAC1_EQ_B4_GAIN [4:0]	00000 (-12dB)	AIF1DAC1 (AIF1, Timeslot 0) EQ Band 4 Gain (see Table 28 for gain range)
	10:6	AIF1DAC1_EQ_B5_GAIN [4:0]	00000 (-12dB)	AIF1DAC1 (AIF1, Timeslot 0) EQ Band 5 Gain (see Table 28 for gain range)

Table 25 AIF1 Timeslot 0 EQ Band Gain Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1184 (04A0h) AIF1 DAC2 EQ Gains (1)	15:11	AIF1DAC2_EQ_B1_GAIN [4:0]	00000 (-12dB)	AIF1DAC2 (AIF1, Timeslot 1) EQ Band 1 Gain (see Table 28 for gain range)
	10:6	AIF1DAC2_EQ_B2_GAIN [4:0]	00000 (-12dB)	AIF1DAC2 (AIF1, Timeslot 1) EQ Band 2 Gain (see Table 28 for gain range)
	5:1	AIF1DAC2_EQ_B3_GAIN [4:0]	00000 (-12dB)	AIF1DAC2 (AIF1, Timeslot 1) EQ Band 3 Gain (see Table 28 for gain range)
R1185 (04A1h) AIF1 DAC2 EQ Gains (2)	15:11	AIF1DAC2_EQ_B4_GAIN [4:0]	00000 (-12dB)	AIF1DAC2 (AIF1, Timeslot 1) EQ Band 4 Gain (see Table 28 for gain range)
	10:6	AIF1DAC2_EQ_B5_GAIN [4:0]	00000 (-12dB)	AIF1DAC2 (AIF1, Timeslot 1) EQ Band 5 Gain (see Table 28 for gain range)

Table 26 AIF1 Timeslot 1 EQ Band Gain Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1408 (0580h) AIF2 EQ Gains (1)	15:11	AIF2DAC_EQ_B1_GAIN [4:0]	00000 (-12dB)	AIF2 EQ Band 1 Gain (see Table 28 for gain range)
	10:6	AIF2DAC_EQ_B2_GAIN [4:0]	00000 (-12dB)	AIF2EQ Band 2 Gain (see Table 28 for gain range)
	5:1	AIF2DAC_EQ_B3_GAIN [4:0]	00000 (-12dB)	AIF2EQ Band 3 Gain (see Table 28 for gain range)
R1409 (0581h) AIF2 EQ Gains (2)	15:11	AIF2DAC_EQ_B4_GAIN [4:0]	00000 (-12dB)	AIF2EQ Band 4 Gain (see Table 28 for gain range)
	10:6	AIF2DAC_EQ_B5_GAIN [4:0]	00000 (-12dB)	AIF2EQ Band 5 Gain (see Table 28 for gain range)

Table 27 AIF2 EQ Band Gain Control

EQ GAIN SETTING	Gain (dB)
00000	-12
00001	-11
00010	-10
00011	-9
00100	-8
00101	-7
00110	-6
00111	-5
01000	-4
01001	-3
01010	-2
01011	-1
01100	0
01101	+1
01110	+2
01111	+3
10000	+4
10001	+5
10010	+6
10011	+7
10100	+8
10101	+9
10110	+10
10111	+11
11000	+12
11001 to 11111	Reserved

Table 28 EQ Gain Control Range

RETUNE™ MOBILE MODE

ReTune™ Mobile mode provides a comprehensive facility for the user to define the cut-off/centre frequencies and filter bandwidth for each EQ band, in addition to the gain controls already described. This enables the EQ to be accurately customised for a specific transducer characteristic or desired sound profile.

The EQ enable and EQ gain controls are the same as defined for the default mode. The additional coefficients used in ReTune™ Mobile mode are held in registers R1154 to R1171 for AIF1DAC1, registers R1186 to R1203 for AIF1DAC2 and registers R1410 to R1427 for AIF2. These coefficients are derived using tools provided in Wolfson's WISCE™ evaluation board control software.

Please contact your local Wolfson representative for more details.

Note that the WM8994 audio interfaces may operate at different sample rates concurrently. The EQ settings for each interface must be programmed relative to the applicable sample rate of the corresponding audio interface. If the audio interface sample rate is changed, then different EQ register settings will be required to achieve a given EQ response.

EQ FILTER CHARACTERISTICS

The filter characteristics for each frequency band are shown in Figure 21 to Figure 25. These figures show the frequency response for all available gain settings, using default cut-off/centre frequencies and bandwidth.

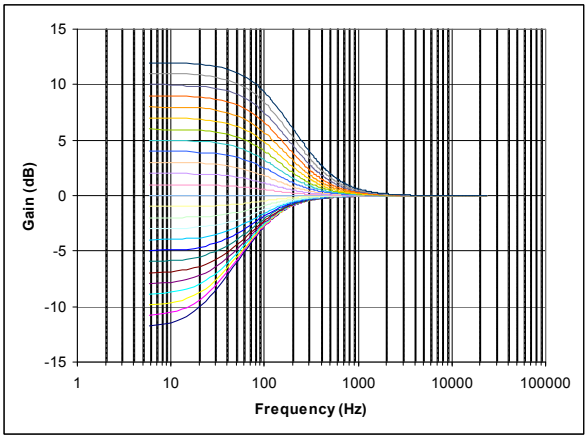


Figure 21 EQ Band 1 – Low Freq Shelf Filter Response

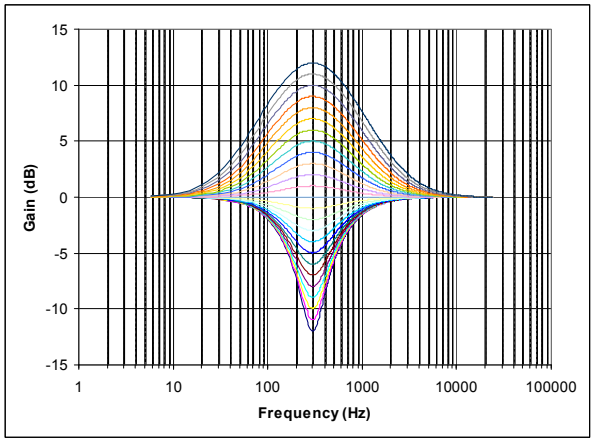


Figure 22 EQ Band 2 – Peak Filter Response

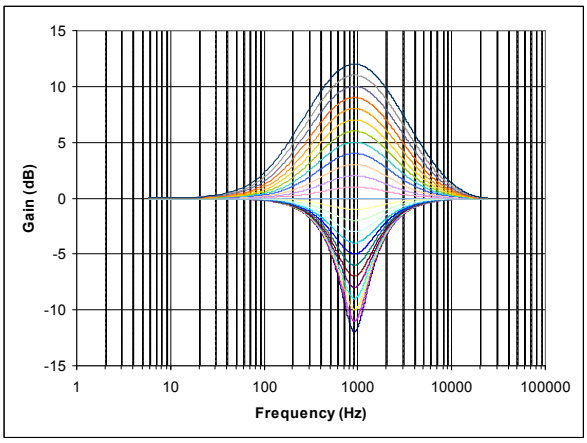


Figure 23 EQ Band 3 – Peak Filter Response

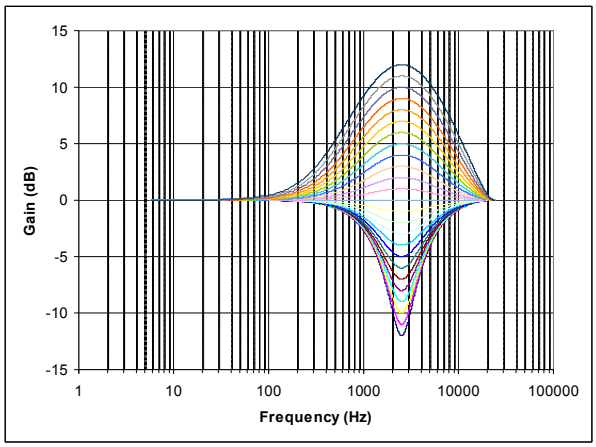


Figure 24 EQ Band 4 – Peak Filter Response

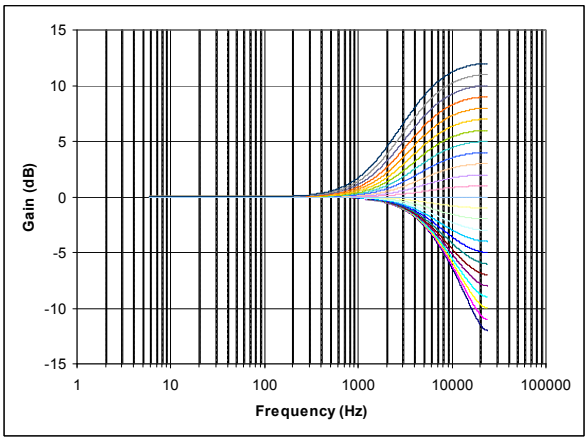


Figure 25 EQ Band 5 – High Freq Shelf Filter Response

3D STEREO EXPANSION

The 3D Stereo Expansion is an audio enhancement feature which can be enabled in the digital playback path of the WM8994 audio interfaces. This feature uses configurable cross-talk mechanisms to adjust the depth or width of the stereo audio.

The WM8994 provides three 3D Stereo Expansion circuits; these are associated with AIF1 timeslot 0, AIF1 timeslot 1 and AIF2 respectively. The 3D Stereo Expansion is enabled and controlled in these signal paths using the register bits described in Table 29.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1057 (0421h) AIF1 DAC1 Filters (2)	13:9	AIF1DAC1_3D_GAIN	00000	AIF1DAC1 playback path (AIF1, Timeslot 0) 3D Stereo depth 00000 = Off 00001 = Minimum (-16dB) …(0.915dB steps) 11111 = Maximum (+11.5dB)
	8	AIF1DAC1_3D_ENA	0	Enable 3D Stereo in AIF1DAC1 playback path (AIF1, Timeslot 0) 0 = Disabled 1 = Enabled
R1059 (0423h) AIF1 DAC2 Filters (2)	13:9	AIF1DAC2_3D_GAIN	00000	AIF1DAC2 playback path (AIF1, Timeslot 1) 3D Stereo depth 00000 = Off 00001 = Minimum (-16dB) …(0.915dB steps) 11111 = Maximum (+11.5dB)
	8	AIF1DAC2_3D_ENA	0	Enable 3D Stereo in AIF1DAC2 playback path (AIF1, Timeslot 1) 0 = Disabled 1 = Enabled
R1313 (0521h) AIF2 DAC Filters (2)	13:9	AIF2DAC_3D_GAIN	00000	AIF2DAC playback path 3D Stereo depth 00000 = Off 00001 = Minimum (-16dB) …(0.915dB steps) 11111 = Maximum (+11.5dB)
	8	AIF2DAC_3D_ENA	0	Enable 3D Stereo in AIF2DAC playback path 0 = Disabled 1 = Enabled

Table 29 3D Stereo Expansion Control

DIGITAL VOLUME AND FILTER CONTROL

This section describes the digital volume and filter controls of the WM8994 AIF paths.

Digital volume control and High Pass Filter (HPF) control is provided on four AIF1 output (digital record) paths and two AIF2 output (digital record) paths.

Digital volume control, soft-mute control, mono mix and de-emphasis filter control is provided on four AIF1 input (digital playback) paths and two AIF2 input (digital playback) paths.

AIF1 - OUTPUT PATH VOLUME CONTROL

The AIF1 interface supports four output channels when TDM mode is enabled, or two output channels in normal mode (ie. TDM not enabled). A digital volume control is provided on each of these output signal paths, allowing attenuation in the range -71.625dB to +17.625dB in 0.375dB steps. The level of attenuation for an eight-bit code X is given by:

$0.375 \times (X-192)$ dB for $1 \leq X \leq 239$; MUTE for $X = 0$ +17.625dB for $239 \leq X \leq 255$

The AIF1ADC1_VU and AIF1ADC2_VU bits control the loading of digital volume control data. When the volume update bit is set to 0, the associated volume control data will be loaded into the respective control register, but will not actually change the digital gain setting.

The AIF1ADC1L and AIF1ADC1R gain settings are updated when a 1 is written to AIF1ADC1_VU. The AIF1ADC2L and AIF1ADC2R gain settings are updated when a 1 is written to AIF1ADC2_VU. This makes it possible to update the gain of left and right channels simultaneously.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1026 (0402h) AIF1 DAC1 Left Volume	8	AIF1ADC1_ VU	N/A	AIF1ADC1 output path (AIF1, Timeslot 0) Volume Update Writing a 1 to this bit will cause the AIF1ADC1L and AIF1ADC1R volume to be updated simultaneously
	7:0	AIF1ADC1L _VOL [7:0]	C0h (0dB)	AIF1ADC1 (Left) output path (AIF1, Timeslot 0) Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) EFh = +17.625dB (See Table 31 for volume range)
R1027 (0403h) AIF1 DAC1 Right Volume	8	AIF1ADC1_ VU	N/A	AIF1ADC1 output path (AIF1, Timeslot 0) Volume Update Writing a 1 to this bit will cause the AIF1ADC1L and AIF1ADC1R volume to be updated simultaneously
	7:0	AIF1ADC1R _VOL [7:0]	C0h (0dB)	AIF1ADC1 (Right) output path (AIF1, Timeslot 0) Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) EFh = +17.625dB (See Table 31 for volume range)
R1028 (0404h) AIF1 ADC2 Left Volume	8	AIF1ADC2_ VU	N/A	AIF1ADC2 output path (AIF1, Timeslot 1) Volume Update Writing a 1 to this bit will cause the AIF1ADC2L and AIF1ADC2R volume to be updated simultaneously

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:0	AIF1ADC2L _VOL [7:0]	C0h (0dB)	AIF1ADC2 (Left) output path (AIF1, Timeslot 1) Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) EFh = +17.625dB (See Table 31 for volume range)
R1029 (0405h) AIF1 ADC2 Right Volume	8	AIF1ADC2_ VU	N/A	AIF1ADC2 output path (AIF1, Timeslot 1) Volume Update Writing a 1 to this bit will cause the AIF1ADC2L and AIF1ADC2R volume to be updated simultaneously
	7:0	AIF1ADC2R _VOL [7:0]	C0h (0dB)	AIF1ADC2 (Right) output path (AIF1, Timeslot 1) Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) EFh = +17.625dB (See Table 31 for volume range)

Table 30 AIF1 Output Path Volume Control

AIF1/AIF2 Output Volume	Volume (dB)	AIF1/AIF2 Output Volume	Volume (dB)	AIF1/AIF2 Output Volume	Volume (dB)	AIF1/AIF2 Output Volume	Volume (dB)
0h	MUTE	40h	-48.000	80h	-24.000	C0h	0.000
1h	-71.625	41h	-47.625	81h	-23.625	C1h	0.375
2h	-71.250	42h	-47.250	82h	-23.250	C2h	0.750
3h	-70.875	43h	-46.875	83h	-22.875	C3h	1.125
4h	-70.500	44h	-46.500	84h	-22.500	C4h	1.500
5h	-70.125	45h	-46.125	85h	-22.125	C5h	1.875
6h	-69.750	46h	-45.750	86h	-21.750	C6h	2.250
7h	-69.375	47h	-45.375	87h	-21.375	C7h	2.625
8h	-69.000	48h	-45.000	88h	-21.000	C8h	3.000
9h	-68.625	49h	-44.625	89h	-20.625	C9h	3.375
Ah	-68.250	4Ah	-44.250	8Ah	-20.250	CAh	3.750
Bh	-67.875	4Bh	-43.875	8Bh	-19.875	CBh	4.125
Ch	-67.500	4Ch	-43.500	8Ch	-19.500	CCh	4.500
Dh	-67.125	4Dh	-43.125	8Dh	-19.125	CDh	4.875
Eh	-66.750	4Eh	-42.750	8Eh	-18.750	CEh	5.250
Fh	-66.375	4Fh	-42.375	8Fh	-18.375	CFh	5.625
10h	-66.000	50h	-42.000	90h	-18.000	D0h	6.000
11h	-65.625	51h	-41.625	91h	-17.625	D1h	6.375
12h	-65.250	52h	-41.250	92h	-17.250	D2h	6.750
13h	-64.875	53h	-40.875	93h	-16.875	D3h	7.125
14h	-64.500	54h	-40.500	94h	-16.500	D4h	7.500
15h	-64.125	55h	-40.125	95h	-16.125	D5h	7.875
16h	-63.750	56h	-39.750	96h	-15.750	D6h	8.250
17h	-63.375	57h	-39.375	97h	-15.375	D7h	8.625
18h	-63.000	58h	-39.000	98h	-15.000	D8h	9.000
19h	-62.625	59h	-38.625	99h	-14.625	D9h	9.375
1Ah	-62.250	5Ah	-38.250	9Ah	-14.250	DAh	9.750
1Bh	-61.875	5Bh	-37.875	9Bh	-13.875	DBh	10.125
1Ch	-61.500	5Ch	-37.500	9Ch	-13.500	DCh	10.500
1Dh	-61.125	5Dh	-37.125	9Dh	-13.125	DDh	10.875
1Eh	-60.750	5Eh	-36.750	9Eh	-12.750	DEh	11.250
1Fh	-60.375	5Fh	-36.375	9Fh	-12.375	DFh	11.625
20h	-60.000	60h	-36.000	A0h	-12.000	E0h	12.000
21h	-59.625	61h	-35.625	A1h	-11.625	E1h	12.375
22h	-59.250	62h	-35.250	A2h	-11.250	E2h	12.750
23h	-58.875	63h	-34.875	A3h	-10.875	E3h	13.125
24h	-58.500	64h	-34.500	A4h	-10.500	E4h	13.500
25h	-58.125	65h	-34.125	A5h	-10.125	E5h	13.875
26h	-57.750	66h	-33.750	A6h	-9.750	E6h	14.250
27h	-57.375	67h	-33.375	A7h	-9.375	E7h	14.625
28h	-57.000	68h	-33.000	A8h	-9.000	E8h	15.000
29h	-56.625	69h	-32.625	A9h	-8.625	E9h	15.375
2Ah	-56.250	6Ah	-32.250	AAh	-8.250	EAh	15.750
2Bh	-55.875	6Bh	-31.875	ABh	-7.875	EBh	16.125
2Ch	-55.500	6Ch	-31.500	ACh	-7.500	ECh	16.500
2Dh	-55.125	6Dh	-31.125	ADh	-7.125	EDh	16.875
2Eh	-54.750	6Eh	-30.750	AEh	-6.750	EEh	17.250
2Fh	-54.375	6Fh	-30.375	AFh	-6.375	EFh	17.625
30h	-54.000	70h	-30.000	B0h	-6.000	F0h	17.625
31h	-53.625	71h	-29.625	B1h	-5.625	F1h	17.625
32h	-53.250	72h	-29.250	B2h	-5.250	F2h	17.625
33h	-52.875	73h	-28.875	B3h	-4.875	F3h	17.625
34h	-52.500	74h	-28.500	B4h	-4.500	F4h	17.625
35h	-52.125	75h	-28.125	B5h	-4.125	F5h	17.625
36h	-51.750	76h	-27.750	B6h	-3.750	F6h	17.625
37h	-51.375	77h	-27.375	B7h	-3.375	F7h	17.625
38h	-51.000	78h	-27.000	B8h	-3.000	F8h	17.625
39h	-50.625	79h	-26.625	B9h	-2.625	F9h	17.625
3Ah	-50.250	7Ah	-26.250	BAh	-2.250	FAh	17.625
3Bh	-49.875	7Bh	-25.875	BBh	-1.875	FBh	17.625
3Ch	-49.500	7Ch	-25.500	BCh	-1.500	FCh	17.625
3Dh	-49.125	7Dh	-25.125	BDh	-1.125	FDh	17.625
3Eh	-48.750	7Eh	-24.750	BEh	-0.750	FEh	17.625
3Fh	-48.375	7Fh	-24.375	BFh	-0.375	FFh	17.625

Table 31 AIF1 Output Path Digital Volume Range

AIF1 - OUTPUT PATH HIGH PASS FILTER

A digital high-pass filter can be enabled in the AIF1 output paths to remove DC offsets. This filter is enabled independently in the four AIF1 output channels using the register bits described in Table 32.

The HPF cut-off frequency for the AIF1 Timeslot 0 channels is set using AIF1ADC1_HPF_CUT. The HPF cut-off frequency for the AIF1 Timeslot 1 channels is set using AIF1ADC2_HPF_CUT.

In hi-fi mode, the high pass filter is optimised for removing DC offsets without degrading the bass response and has a cut-off frequency of 3.7Hz when the sample rate (fs) = 44.1kHz.

In voice modes, the high pass filter is optimised for voice communication; it is recommended to set the cut-off frequency below 300Hz.

Note that the cut-off frequencies scale with the AIF1 sample rate. See Table 33 for the HPF cut-off frequencies at all supported sample rates.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1040 (0410h) AIF1 ADC1 Filters	14:13	AIF1ADC1_ HPF_CUT [1:0]	00	AIF1ADC1 output path (AIF1, Timeslot 0) Digital HPF cut-off frequency (fc) 00 = Hi-fi mode (fc = 4Hz at fs = 48kHz) 01 = Voice mode 1 (fc = 127Hz at fs = 8kHz) 10 = Voice mode 2 (fc = 130Hz at fs = 8kHz) 11 = Voice mode 3 (fc = 267Hz at fs = 8kHz)
	12	AIF1ADC1L_ HPF	0	AIF1ADC1 (Left) output path (AIF1, Timeslot 0) Digital HPF Enable 0 = Disabled 1 = Enabled
	11	AIF1ADC1R _HPF	0	AIF1ADC1 (Right) output path (AIF1, Timeslot 0) Digital HPF Enable 0 = Disabled 1 = Enabled
R1041 (0411h) AIF1 ADC2 Filters	14:13	AIF1ADC2_ HPF_CUT [1:0]	00	AIF1ADC2 output path (AIF1, Timeslot 1) Digital HPF cut-off frequency (fc) 00 = Hi-fi mode (fc = 4Hz at fs = 48kHz) 01 = Voice mode 1 (fc = 127Hz at fs = 8kHz) 10 = Voice mode 2 (fc = 130Hz at fs = 8kHz) 11 = Voice mode 3 (fc = 267Hz at fs = 8kHz)
	12	AIF1ADC2L_ HPF	0	AIF1ADC2 (Left) output path (AIF1, Timeslot 1) Digital HPF Enable 0 = Disabled 1 = Enabled
	11	AIF1ADC2R _HPF	0	AIF1ADC2 (Right) output path (AIF1, Timeslot 1) Digital HPF Enable 0 = Disabled 1 = Enabled

Table 32 AIF1 Output Path High Pass Filter

Sample Frequency (kHz)	Cut-Off Frequency (Hz) for given value of AIF*n*ADC*n*_HPF_CUT			
	00	01	10	11
8.000	0.7	64	130	267
11.025	0.9	88	178	367
16.000	1.3	127	258	532
22.050	1.9	175	354	733
24.000	2.0	190	386	798
32.000	2.7	253	514	1063
44.100	3.7	348	707	1464
48.000	4.0	379	770	1594
88.200	7.4	696	1414	2928
96.000	8.0	758	1540	3188

Table 33 AIF1 Output Path High Pass Filter Cut-Off Frequencies

AIF1 - INPUT PATH VOLUME CONTROL

The AIF1 interface supports four input channels when TDM mode is enabled, or two input channels in normal mode (ie. TDM not enabled). A digital volume control is provided on each of these input signal paths, allowing attenuation in the range -71.625dB to 0dB in 0.375dB steps. The level of attenuation for an eight-bit code X is given by:

$0.375 \times (X-192)$ dB for $1 \leq X \leq 192$; MUTE for $X = 0$ 0dB for $192 \leq X \leq 255$

The AIF1DAC1_VU and AIF1DAC2_VU bits control the loading of digital volume control data. When the volume update bit is set to 0, the associated volume control data will be loaded into the respective control register, but will not actually change the digital gain setting.

The AIF1DAC1L and AIF1DAC1R gain settings are updated when a 1 is written to AIF1DAC1_VU. The AIF1DAC2L and AIF1DAC2R gain settings are updated when a 1 is written to AIF1DAC2_VU. This makes it possible to update the gain of left and right channels simultaneously.

Note that a digital gain function is also available at the audio interface input, to boost the DAC volume when a small signal is received on DACDAT1. See “Digital Volume and Filter Control” for further details.

Digital volume control is also possible at the DAC stage of the signal path, after the audio signal has passed through the DAC digital mixers. See “Digital to Analogue Converter (DAC)” for further details.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1026 (0402h) AIF1 DAC1 Left Volume	8	AIF1DAC1_ VU	N/A	AIF1DAC1 input path (AIF1, Timeslot 0) Volume Update Writing a 1 to this bit will cause the AIF1DAC1L and AIF1DAC1R volume to be updated simultaneously
	7:0	AIF1DAC1L _VOL [7:0]	C0h (0dB)	AIF1DAC1 (Left) input path (AIF1, Timeslot 0) Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB (See Table 35 for volume range)
R1027 (0403h) AIF1 DAC1 Right Volume	8	AIF1DAC1_ VU	N/A	AIF1DAC1 input path (AIF1, Timeslot 0) Volume Update Writing a 1 to this bit will cause the AIF1DAC1L and AIF1DAC1R volume to be updated simultaneously
	7:0	AIF1DAC1R _VOL [7:0]	C0h (0dB)	AIF1DAC1 (Right) input path (AIF1, Timeslot 0) Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB (See Table 35 for volume range)
R1030 (0406h) AIF1 DAC2 Left Volume	8	AIF1DAC2_ VU	N/A	AIF1DAC2 input path (AIF1, Timeslot 1) Volume Update Writing a 1 to this bit will cause the AIF1DAC2L and AIF1DAC2R volume to be updated simultaneously

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:0	AIF1DAC2L _VOL [7:0]	C0h (0dB)	AIF1DAC2 (Left) input path (AIF1, Timeslot 1) Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB (See Table 35 for volume range)
R1031 (0407h) AIF1 DAC2 Right Volume	8	AIF1DAC2_ VU	N/A	AIF1DAC2 input path (AIF1, Timeslot 1) Volume Update Writing a 1 to this bit will cause the AIF1DAC2L and AIF1DAC2R volume to be updated simultaneously
	7:0	AIF1DAC2R _VOL [7:0]	C0h (0dB)	AIF1DAC2 (Right) input path (AIF1, Timeslot 1) Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB (See Table 35 for volume range)

Table 34 AIF1 Input Path Volume Control

AIF1/AIF2 Input Volume, DAC Volume	Volume (dB)	AIF1/AIF2 Input Volume, DAC Volume	Volume (dB)	AIF1/AIF2 Input Volume, DAC Volume	Volume (dB)	AIF1/AIF2 Input Volume, DAC Volume	Volume (dB)
0h	MUTE	40h	-48.000	80h	-24.000	C0h	0.000
1h	-71.625	41h	-47.625	81h	-23.625	C1h	0.000
2h	-71.250	42h	-47.250	82h	-23.250	C2h	0.000
3h	-70.875	43h	-46.875	83h	-22.875	C3h	0.000
4h	-70.500	44h	-46.500	84h	-22.500	C4h	0.000
5h	-70.125	45h	-46.125	85h	-22.125	C5h	0.000
6h	-69.750	46h	-45.750	86h	-21.750	C6h	0.000
7h	-69.375	47h	-45.375	87h	-21.375	C7h	0.000
8h	-69.000	48h	-45.000	88h	-21.000	C8h	0.000
9h	-68.625	49h	-44.625	89h	-20.625	C9h	0.000
Ah	-68.250	4Ah	-44.250	8Ah	-20.250	CAh	0.000
Bh	-67.875	4Bh	-43.875	8Bh	-19.875	CBh	0.000
Ch	-67.500	4Ch	-43.500	8Ch	-19.500	CCh	0.000
Dh	-67.125	4Dh	-43.125	8Dh	-19.125	CDh	0.000
Eh	-66.750	4Eh	-42.750	8Eh	-18.750	CEh	0.000
Fh	-66.375	4Fh	-42.375	8Fh	-18.375	CFh	0.000
10h	-66.000	50h	-42.000	90h	-18.000	D0h	0.000
11h	-65.625	51h	-41.625	91h	-17.625	D1h	0.000
12h	-65.250	52h	-41.250	92h	-17.250	D2h	0.000
13h	-64.875	53h	-40.875	93h	-16.875	D3h	0.000
14h	-64.500	54h	-40.500	94h	-16.500	D4h	0.000
15h	-64.125	55h	-40.125	95h	-16.125	D5h	0.000
16h	-63.750	56h	-39.750	96h	-15.750	D6h	0.000
17h	-63.375	57h	-39.375	97h	-15.375	D7h	0.000
18h	-63.000	58h	-39.000	98h	-15.000	D8h	0.000
19h	-62.625	59h	-38.625	99h	-14.625	D9h	0.000
1Ah	-62.250	5Ah	-38.250	9Ah	-14.250	DAh	0.000
1Bh	-61.875	5Bh	-37.875	9Bh	-13.875	DBh	0.000
1Ch	-61.500	5Ch	-37.500	9Ch	-13.500	DCh	0.000
1Dh	-61.125	5Dh	-37.125	9Dh	-13.125	DDh	0.000
1Eh	-60.750	5Eh	-36.750	9Eh	-12.750	DEh	0.000
1Fh	-60.375	5Fh	-36.375	9Fh	-12.375	DFh	0.000
20h	-60.000	60h	-36.000	A0h	-12.000	E0h	0.000
21h	-59.625	61h	-35.625	A1h	-11.625	E1h	0.000
22h	-59.250	62h	-35.250	A2h	-11.250	E2h	0.000
23h	-58.875	63h	-34.875	A3h	-10.875	E3h	0.000
24h	-58.500	64h	-34.500	A4h	-10.500	E4h	0.000
25h	-58.125	65h	-34.125	A5h	-10.125	E5h	0.000
26h	-57.750	66h	-33.750	A6h	-9.750	E6h	0.000
27h	-57.375	67h	-33.375	A7h	-9.375	E7h	0.000
28h	-57.000	68h	-33.000	A8h	-9.000	E8h	0.000
29h	-56.625	69h	-32.625	A9h	-8.625	E9h	0.000
2Ah	-56.250	6Ah	-32.250	AAh	-8.250	EAh	0.000
2Bh	-55.875	6Bh	-31.875	ABh	-7.875	EBh	0.000
2Ch	-55.500	6Ch	-31.500	ACh	-7.500	ECh	0.000
2Dh	-55.125	6Dh	-31.125	ADh	-7.125	EDh	0.000
2Eh	-54.750	6Eh	-30.750	AEh	-6.750	EEh	0.000
2Fh	-54.375	6Fh	-30.375	AFh	-6.375	EFh	0.000
30h	-54.000	70h	-30.000	B0h	-6.000	F0h	0.000
31h	-53.625	71h	-29.625	B1h	-5.625	F1h	0.000
32h	-53.250	72h	-29.250	B2h	-5.250	F2h	0.000
33h	-52.875	73h	-28.875	B3h	-4.875	F3h	0.000
34h	-52.500	74h	-28.500	B4h	-4.500	F4h	0.000
35h	-52.125	75h	-28.125	B5h	-4.125	F5h	0.000
36h	-51.750	76h	-27.750	B6h	-3.750	F6h	0.000
37h	-51.375	77h	-27.375	B7h	-3.375	F7h	0.000
38h	-51.000	78h	-27.000	B8h	-3.000	F8h	0.000
39h	-50.625	79h	-26.625	B9h	-2.625	F9h	0.000
3Ah	-50.250	7Ah	-26.250	BAh	-2.250	FAh	0.000
3Bh	-49.875	7Bh	-25.875	BBh	-1.875	FBh	0.000
3Ch	-49.500	7Ch	-25.500	BCh	-1.500	FCh	0.000
3Dh	-49.125	7Dh	-25.125	BDh	-1.125	FDh	0.000
3Eh	-48.750	7Eh	-24.750	BEh	-0.750	FEh	0.000
3Fh	-48.375	7Fh	-24.375	BFh	-0.375	FFh	0.000

Table 35 AIF1 Input Path Digital Volume Range

AIF1 - INPUT PATH SOFT MUTE CONTROL

The WM8994 provides a soft mute function for each of the AIF1 interface input paths. When the soft-mute function is selected, the WM8994 gradually attenuates the associated signal paths until the path is entirely muted.

When the soft-mute function is de-selected, the gain will either return instantly to the digital gain setting, or will gradually ramp back to the digital gain setting, depending on the applicable _UNMUTE_RAMP register field.

The mute and un-mute ramp rate is selectable between two different rates.

The AIF1 input paths are soft-muted by default. To play back an audio signal, the soft-mute must first be de-selected by setting the applicable Mute bit to 0.

The soft un-mute would typically be used during playback of audio data so that when the Mute is subsequently disabled, a smooth transition is scheduled to the previous volume level and pop noise is avoided. This is desirable when resuming playback after pausing during a track.

The soft un-mute would typically not be required when un-muting at the start of a music file, in order that the first part of the music track is not attenuated. The instant un-mute behaviour is desirable in this case, when starting playback of a new track. See “DAC Soft Mute and Soft Un-Mute” (Figure 26) for an illustration of the soft mute function.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1056 (0420h) AIF1 DAC1 Filters (1)	9	AIF1DAC1_ MUTE	1	AIF1DAC1 input path (AIF1, Timeslot 0) Soft Mute Control 0 = Un-mute 1 = Mute
	5	AIF1DAC1_ MUTERATE	0	AIF1DAC1 input path (AIF1, Timeslot 0) Soft Mute Ramp Rate 0 = Fast ramp (fs/2, maximum ramp time is 10.7ms at fs=48k) 1 = Slow ramp (fs/32, maximum ramp time is 171ms at fs=48k) (Note: ramp rate scales with sample rate.)
	4	AIF1DAC1_ UNMUTE_ RAMP	0	AIF1DAC1 input path (AIF1, Timeslot 0) Unmute Ramp select 0 = Disabling soft-mute (AIF1DAC1_MUTE=0) will cause the volume to change immediately to AIF1DAC1L_VOL and AIF1DAC1R_VOL settings 1 = Disabling soft-mute (AIF1DAC1_MUTE=0) will cause the DAC volume to ramp up gradually to the AIF1DAC1L_VOL and AIF1DAC1R_VOL settings
R1058 (0422h) AIF1 DAC2 Filters (1)	9	AIF1DAC2_ MUTE	1	AIF1DAC2 input path (AIF1, Timeslot 1) Soft Mute Control 0 = Un-mute 1 = Mute
	5	AIF1DAC2_ MUTERATE	0	AIF1DAC2 input path (AIF1, Timeslot 1) Soft Mute Ramp Rate 0 = Fast ramp (fs/2, maximum ramp time is 10.7ms at fs=48k) 1 = Slow ramp (fs/32, maximum ramp time is 171ms at fs=48k) (Note: ramp rate scales with sample rate.)
	4	AIF1DAC2_ UNMUTE_ RAMP	0	AIF1DAC2 input path (AIF1, Timeslot 1) Unmute Ramp select 0 = Disabling soft-mute (AIF1DAC2_MUTE=0) will cause the volume to change immediately to AIF1DAC2L_VOL and AIF1DAC2R_VOL settings 1 = Disabling soft-mute (AIF1DAC2_MUTE=0) will cause the DAC volume to ramp up gradually to the AIF1DAC2L_VOL and AIF1DAC2R_VOL settings

Table 36 AIF1 Input Path Soft Mute Control

AIF1 - INPUT PATH MONO MIX AND DE-EMPHASIS FILTER

A digital mono mix can be selected on one or both pairs of AIF1 input channels. The mono mix is generated as the sum of the Left and Right AIF channel data. To prevent clipping, a 6dB attenuation is applied to the mono mix.

Digital de-emphasis can be applied to the AIF1 input (playback) paths; this is appropriate when the data source is a CD where pre-emphasis is used in the recording. De-emphasis filtering is available for sample rates of 48kHz, 44.1kHz and 32kHz. See "Digital Filter Characteristics" section for details of de-emphasis filter characteristics.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1056 (0420h) AIF1 DAC1 Filters (1)	7	AIF1DAC1_ MONO	0	AIF1DAC1 input path (AIF1, Timeslot 0) Mono Mix Control 0 = Disabled 1 = Enabled
	2:1	AIF1DAC1_ DEEMP [1:0]	00	AIF1DAC1 input path (AIF1, Timeslot 0) De-Emphasis Control 00 = No de-emphasis 01 = 32kHz sample rate 10 = 44.1kHz sample rate 11 = 48kHz sample rate
R1058 (0422h) AIF1 DAC2 Filters (1)	7	AIF1DAC2_ MONO	0	AIF1DAC2 input path (AIF1, Timeslot 1) Mono Mix Control 0 = Disabled 1 = Enabled
	2:1	AIF1DAC2_ DEEMP [1:0]	00	AIF1DAC2 input path (AIF1, Timeslot 1) De-Emphasis Control 00 = No de-emphasis 01 = 32kHz sample rate 10 = 44.1kHz sample rate 11 = 48kHz sample rate

Table 37 AIF1 Input Path Mono Mix and De-Emphasis Filter Control

AIF2 - OUTPUT PATH VOLUME CONTROL

The AIF2 interface supports two output channels. A digital volume control is provided on each output signal path, allowing attenuation in the range -71.625dB to +17.625dB in 0.375dB steps. The level of attenuation for an eight-bit code X is given by:

$0.375 \times (X-192)$ dB for $1 \leq X \leq 239$; MUTE for $X = 0$ +17.625dB for $239 \leq X \leq 255$

The AIF2ADC_VU bit controls the loading of digital volume control data. When AIF2ADC_VU bit is set to 0, the AIF2ADCL_VOL and AIF2ADCR_VOL control data will be loaded into the respective control register, but will not actually change the digital gain setting. Both left and right gain settings are updated when a 1 is written to AIF2ADC_VU. This makes it possible to update the gain of left and right channels simultaneously.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1280 (0500h) AIF2 ADC Left Volume	8	AIF2ADC_VU	N/A	AIF2ADC output path Volume Update Writing a 1 to this bit will cause the AIF2ADCL and AIF2ADCR volume to be updated simultaneously
	7:0	AIF2ADCL_VOL [7:0]	C0h (0dB)	AIF2ADC (Left) output path Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) EFh = +17.625dB (See Table 31 for volume range)
R1281 (0501h) AIF2 ADC Right Volume	8	AIF2ADC_VU	N/A	AIF2ADC output path Volume Update Writing a 1 to this bit will cause the AIF2ADCL and AIF2ADCR volume to be updated simultaneously
	7:0	AIF2ADCR_VOL [7:0]	C0h (0dB)	AIF2ADC (Right) output path Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) EFh = +17.625dB (See Table 31 for volume range)

Table 38 AIF2 Output Path Volume Control

AIF2 - OUTPUT PATH HIGH PASS FILTER

A digital high-pass filter can be enabled in the AIF2 output paths to remove DC offsets. This filter is enabled independently in the two AIF2 output channels using the register bits described in Table 39.

The HPF cut-off frequency for the AIF2 channels is set using AIF2ADC_HPF_CUT.

In hi-fi mode, the high pass filter is optimised for removing DC offsets without degrading the bass response and has a cut-off frequency of 3.7Hz when the sample rate (fs) = 44.1kHz.

In voice modes, the high pass filter is optimised for voice communication; it is recommended to set the cut-off frequency below 300Hz.

Note that the cut-off frequencies scale with the AIF2 sample rate. See Table 33 for the HPF cut-off frequencies at all supported sample rates.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1040 (0410h) AIF1 ADC1 Filters	14:13	AIF2ADC_HPF_CUT [1:0]	00	AIF2ADC output path Digital HPF Cut-Off Frequency (fc) 00 = Hi-fi mode (fc = 4Hz at fs = 48kHz) 01 = Voice mode 1 (fc = 127Hz at fs = 8kHz) 10 = Voice mode 2 (fc = 130Hz at fs = 8kHz) 11 = Voice mode 3 (fc = 267Hz at fs = 8kHz)
	12	AIF2ADCL_HPF	0	AIF2ADC (Left) output path Digital HPF Enable 0 = Disabled 1 = Enabled
	11	AIF2ADCR_HPF	0	AIF2ADC (Right) output path Digital HPF Enable 0 = Disabled 1 = Enabled

Table 39 AIF2 Output Path High Pass Filter

AIF2 - INPUT PATH VOLUME CONTROL

The AIF2 interface supports two input channels. A digital volume control is provided on each input signal path, allowing attenuation in the range -71.625dB to 0dB in 0.375dB steps. The level of attenuation for an eight-bit code X is given by:

$0.375 \times (X-192)$ dB for $1 \leq X \leq 192$; MUTE for $X = 0$ 0dB for $192 \leq X \leq 255$

The AIF2DAC_VU bit controls the loading of digital volume control data. When AIF2DAC_VU bit is set to 0, the AIF2DACL_VOL and AIF2DACR_VOL control data will be loaded into the respective control register, but will not actually change the digital gain setting. Both left and right gain settings are updated when a 1 is written to AIF2DAC_VU. This makes it possible to update the gain of left and right channels simultaneously.

Note that a digital gain function is also available at the audio interface input, to boost the DAC volume when a small signal is received on DACDAT2. See "Digital Volume and Filter Control" for further details.

Digital volume control is also possible at the DAC stage of the signal path, after the audio signal has passed through the DAC digital mixers. See "Digital to Analogue Converter (DAC)" for further details.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1282 (0502h) AIF2 DAC Left Volume	8	AIF2DAC_VU	N/A	AIF2DAC input path Volume Update Writing a 1 to this bit will cause the AIF2DACL and AIF2DACR volume to be updated simultaneously
	7:0	AIF2DACL_VOL [7:0]	C0h (0dB)	AIF2DAC (Left) input path Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB (See Table 35 for volume range)
R1283 (0503h) AIF2 DAC Right Volume	8	AIF2DAC_VU	N/A	AIF2DAC input path Volume Update Writing a 1 to this bit will cause the AIF2DACL and AIF2DACR volume to be updated simultaneously
	7:0	AIF2DACR_VOL [7:0]	C0h (0dB)	AIF2DAC (Right) input path Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB (See Table 35 for volume range)

Table 40 AIF2 Input Path Volume Control

AIF2 - INPUT PATH SOFT MUTE CONTROL

The WM8994 provides a soft mute function for each of the AIF1 interface input paths. When the soft-mute function is selected, the WM8994 gradually attenuates the associated signal paths until the path is entirely muted.

When the soft-mute function is de-selected, the gain will either return instantly to the digital gain setting, or will gradually ramp back to the digital gain setting, depending on the applicable _UNMUTE_RAMP register field.

The mute and un-mute ramp rate is selectable between two different rates.

The AIF1 input paths are soft-muted by default. To play back an audio signal, the soft-mute must first be de-selected by setting the applicable Mute bit to 0.

The soft un-mute would typically be used during playback of audio data so that when the Mute is subsequently disabled, a smooth transition is scheduled to the previous volume level and pop noise is avoided. This is desirable when resuming playback after pausing during a track.

The soft un-mute would typically not be required when un-muting at the start of a music file, in order that the first part of the music track is not attenuated. The instant un-mute behaviour is desirable in this case, when starting playback of a new track. See “DAC Soft Mute and Soft Un-Mute” (Figure 26) for an illustration of the soft mute function.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1312 (0520h) AIF2 DAC Filters (1)	9	AIF2DAC_MUTE	1	AIF2DAC input path Soft Mute Control 0 = Un-mute 1 = Mute
	5	AIF2DAC_MUTERATE	0	AIF2DAC input path Soft Mute Ramp Rate 0 = Fast ramp (fs/2, maximum ramp time is 10.7ms at fs=48k) 1 = Slow ramp (fs/32, maximum ramp time is 171ms at fs=48k) (Note: ramp rate scales with sample rate.)
	4	AIF2DAC_UNMUTE_RAMP	0	AIF2DAC input path Unmute Ramp select 0 = Disabling soft-mute (AIF2DAC_MUTE=0) will cause the volume to change immediately to AIF2DACL_VOL and AIF2DACR_VOL settings 1 = Disabling soft-mute (AIF2DAC_MUTE=0) will cause the DAC volume to ramp up gradually to the AIF2DACL_VOL and AIF2DACR_VOL settings

Table 41 AIF2 Input Path Soft Mute Control

AIF1 - INPUT PATH MONO MIX AND DE-EMPHASIS FILTER

A digital mono mix can be selected on one or both pairs of AIF1 input channels. The mono mix is generated as the sum of the Left and Right AIF channel data. To prevent clipping, a 6dB attenuation is applied to the mono mix.

Digital de-emphasis can be applied to the AIF1 input (playback) paths; this is appropriate when the data source is a CD where pre-emphasis is used in the recording. De-emphasis filtering is available for sample rates of 48kHz, 44.1kHz and 32kHz. See "Digital Filter Characteristics" section for details of de-emphasis filter characteristics.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1056 (0420h) AIF1 DAC1 Filters (1)	7	AIF2DAC_MONO	0	AIF2DAC input path Mono Mix Control 0 = Disabled 1 = Enabled
	2:1	AIF2DAC_DEEMP [1:0]	00	AIF2DAC input path De-Emphasis Control 00 = No de-emphasis 01 = 32kHz sample rate 10 = 44.1kHz sample rate 11 = 48kHz sample rate

Table 42 AIF2 Input Path Mono Mix and De-Emphasis Filter Control

DIGITAL TO ANALOGUE CONVERTER (DAC)

The WM8994 DACs receive digital input data from the DAC mixers - see “Digital Mixing”. The digital audio data is converted to oversampled bit streams in the on-chip, true 24-bit digital interpolation filters. The bitstream data enters four multi-bit, sigma-delta DACs, which convert them to high quality analogue audio signals. The multi-bit DAC architecture reduces high frequency noise and sensitivity to clock jitter. It also uses a Dynamic Element Matching technique for high linearity and low distortion.

A high performance mode of DAC operation can be selected by setting the DAC_OSR128 bit - see “Clocking and Sample Rates” for details.

The analogue outputs from the DACs can be mixed with analogue line/mic inputs using the line output mixers MIXOUTL / MIXOUTR and the speaker output mixers SPKMIXL / SPKMIXR.

The DACs are enabled using the register bits defined in Table 43.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (0005h) Power Management (5)	3	DAC2L_ENA	0	Left DAC2 Enable 0 = Disabled 1 = Enabled
	2	DAC2R_ENA	0	Right DAC2 Enable 0 = Disabled 1 = Enabled
	1	DAC1L_ENA	0	Left DAC1 Enable 0 = Disabled 1 = Enabled
	0	DAC1R_ENA	0	Right DAC1 Enable 0 = Disabled 1 = Enabled

Table 43 DAC Enable Control

DAC DIGITAL VOLUME

The output level of each DAC can be controlled digitally over a range from -71.625dB to 0dB in 0.375dB steps. The level of attenuation for an eight-bit code X is given by:

$0.375 \times (X-192)$ dB for $1 \leq X \leq 192$; MUTE for $X = 0$; 0dB for $192 \leq X \leq 255$

Each of the DACs can be muted using the soft mute control bits described in Table 44. The WM8994 always applies a soft mute, where the volume is decreased gradually. The un-mute behaviour is configurable, as described in the “DAC Soft Mute and Soft Un-Mute” section.

The DAC1_VU and DAC2_VU bits control the loading of digital volume control data. When DAC1_VU is set to 0, the DAC1L_VOL or DAC1R_VOL control data will be loaded into the respective control register, but will not actually change the digital gain setting. Both left and right gain settings are updated when a 1 is written to DAC1_VU. This makes it possible to update the gain of both channels simultaneously. A similar function for DAC2L and DAC2R is controlled by the DAC2_VU register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1552 (0610h) DAC1 Left Volume	9	DAC1L_MUTE	1	DAC1L Soft Mute Control 0 = DAC Un-mute 1 = DAC Mute
	8	DAC1_VU	N/A	DAC1L and DAC1R Volume Update Writing a 1 to this bit will cause the DAC1L and DAC1R volume to be updated simultaneously
	7:0	DAC1L_VOL [7:0]	C0h (0dB)	DAC1L Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB (See Table 35 for volume range)
R1553 (0611h) DAC1 Right Volume	9	DAC1R_MUTE	1	DAC1R Soft Mute Control 0 = DAC Un-mute 1 = DAC Mute
	8	DAC1_VU	N/A	DAC1L and DAC1R Volume Update Writing a 1 to this bit will cause the DAC1L and DAC1R volume to be updated simultaneously
	7:0	DAC1R_VOL [7:0]	C0h (0dB)	DAC1R Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB (See Table 35 for volume range)
R1554 (0612h) DAC2 Left Volume	9	DAC2L_MUTE	1	DAC2L Soft Mute Control 0 = DAC Un-mute 1 = DAC Mute
	8	DAC2_VU	N/A	DAC2L and DAC2R Volume Update Writing a 1 to this bit will cause the DAC2L and DAC2R volume to be updated simultaneously
	7:0	DAC2L_VOL [7:0]	C0h (0dB)	DAC2L Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB (See Table 35 for volume range)
R1555 (0613h) DAC2 Right Volume	9	DAC2R_MUTE	1	DAC2R Soft Mute Control 0 = DAC Un-mute 1 = DAC Mute
	8	DAC2_VU	N/A	DAC2R and DAC2R Volume Update Writing a 1 to this bit will cause the DAC2R and DAC2R volume to be updated simultaneously

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:0	DAC2R_VOL [7:0]	C0h (0dB)	DAC2R Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB (See Table 35 for volume range)

Table 44 DAC Digital Volume Control

DAC Volume, AIF1/AIF2 Input Volume	Volume (dB)	DAC Volume, AIF1/AIF2 Input Volume	Volume (dB)	DAC Volume, AIF1/AIF2 Input Volume	Volume (dB)	DAC Volume, AIF1/AIF2 Input Volume	Volume (dB)
0h	MUTE	40h	-48.000	80h	-24.000	C0h	0.000
1h	-71.625	41h	-47.625	81h	-23.625	C1h	0.000
2h	-71.250	42h	-47.250	82h	-23.250	C2h	0.000
3h	-70.875	43h	-46.875	83h	-22.875	C3h	0.000
4h	-70.500	44h	-46.500	84h	-22.500	C4h	0.000
5h	-70.125	45h	-46.125	85h	-22.125	C5h	0.000
6h	-69.750	46h	-45.750	86h	-21.750	C6h	0.000
7h	-69.375	47h	-45.375	87h	-21.375	C7h	0.000
8h	-69.000	48h	-45.000	88h	-21.000	C8h	0.000
9h	-68.625	49h	-44.625	89h	-20.625	C9h	0.000
Ah	-68.250	4Ah	-44.250	8Ah	-20.250	CAh	0.000
Bh	-67.875	4Bh	-43.875	8Bh	-19.875	CBh	0.000
Ch	-67.500	4Ch	-43.500	8Ch	-19.500	CCh	0.000
Dh	-67.125	4Dh	-43.125	8Dh	-19.125	CDh	0.000
Eh	-66.750	4Eh	-42.750	8Eh	-18.750	CEh	0.000
Fh	-66.375	4Fh	-42.375	8Fh	-18.375	CFh	0.000
10h	-66.000	50h	-42.000	90h	-18.000	D0h	0.000
11h	-65.625	51h	-41.625	91h	-17.625	D1h	0.000
12h	-65.250	52h	-41.250	92h	-17.250	D2h	0.000
13h	-64.875	53h	-40.875	93h	-16.875	D3h	0.000
14h	-64.500	54h	-40.500	94h	-16.500	D4h	0.000
15h	-64.125	55h	-40.125	95h	-16.125	D5h	0.000
16h	-63.750	56h	-39.750	96h	-15.750	D6h	0.000
17h	-63.375	57h	-39.375	97h	-15.375	D7h	0.000
18h	-63.000	58h	-39.000	98h	-15.000	D8h	0.000
19h	-62.625	59h	-38.625	99h	-14.625	D9h	0.000
1Ah	-62.250	5Ah	-38.250	9Ah	-14.250	DAh	0.000
1Bh	-61.875	5Bh	-37.875	9Bh	-13.875	DBh	0.000
1Ch	-61.500	5Ch	-37.500	9Ch	-13.500	DCh	0.000
1Dh	-61.125	5Dh	-37.125	9Dh	-13.125	DDh	0.000
1Eh	-60.750	5Eh	-36.750	9Eh	-12.750	DEh	0.000
1Fh	-60.375	5Fh	-36.375	9Fh	-12.375	DFh	0.000
20h	-60.000	60h	-36.000	A0h	-12.000	E0h	0.000
21h	-59.625	61h	-35.625	A1h	-11.625	E1h	0.000
22h	-59.250	62h	-35.250	A2h	-11.250	E2h	0.000
23h	-58.875	63h	-34.875	A3h	-10.875	E3h	0.000
24h	-58.500	64h	-34.500	A4h	-10.500	E4h	0.000
25h	-58.125	65h	-34.125	A5h	-10.125	E5h	0.000
26h	-57.750	66h	-33.750	A6h	-9.750	E6h	0.000
27h	-57.375	67h	-33.375	A7h	-9.375	E7h	0.000
28h	-57.000	68h	-33.000	A8h	-9.000	E8h	0.000
29h	-56.625	69h	-32.625	A9h	-8.625	E9h	0.000
2Ah	-56.250	6Ah	-32.250	AAh	-8.250	EAh	0.000
2Bh	-55.875	6Bh	-31.875	ABh	-7.875	EBh	0.000
2Ch	-55.500	6Ch	-31.500	ACh	-7.500	ECh	0.000
2Dh	-55.125	6Dh	-31.125	ADh	-7.125	EDh	0.000
2Eh	-54.750	6Eh	-30.750	AEh	-6.750	EEh	0.000
2Fh	-54.375	6Fh	-30.375	AFh	-6.375	EFh	0.000
30h	-54.000	70h	-30.000	B0h	-6.000	F0h	0.000
31h	-53.625	71h	-29.625	B1h	-5.625	F1h	0.000
32h	-53.250	72h	-29.250	B2h	-5.250	F2h	0.000
33h	-52.875	73h	-28.875	B3h	-4.875	F3h	0.000
34h	-52.500	74h	-28.500	B4h	-4.500	F4h	0.000
35h	-52.125	75h	-28.125	B5h	-4.125	F5h	0.000
36h	-51.750	76h	-27.750	B6h	-3.750	F6h	0.000
37h	-51.375	77h	-27.375	B7h	-3.375	F7h	0.000
38h	-51.000	78h	-27.000	B8h	-3.000	F8h	0.000
39h	-50.625	79h	-26.625	B9h	-2.625	F9h	0.000
3Ah	-50.250	7Ah	-26.250	BAh	-2.250	FAh	0.000
3Bh	-49.875	7Bh	-25.875	BBh	-1.875	FBh	0.000
3Ch	-49.500	7Ch	-25.500	BCh	-1.500	FCh	0.000
3Dh	-49.125	7Dh	-25.125	BDh	-1.125	FDh	0.000
3Eh	-48.750	7Eh	-24.750	BEh	-0.750	FEh	0.000
3Fh	-48.375	7Fh	-24.375	BFh	-0.375	FFh	0.000

Table 45 DAC Digital Volume Range

DAC SOFT MUTE AND SOFT UN-MUTE

The WM8994 has a soft mute function which ensures that a gradual attenuation is applied to the DAC outputs when the mute is asserted. The soft mute rate can be selected using the DAC_MUTERATE bit.

When a mute bit is disabled, the gain will either gradually ramp back up to the digital gain setting, or return instantly to the digital gain setting, depending on the DAC_SOFTMUTEMODE register bit. If the gradual un-mute ramp is selected (DAC_SOFTMUTEMODE = 1), then the un-mute rate is determined by the DAC_MUTERATE bit.

Note that each DAC is soft-muted by default. To play back an audio signal, the mute must first be disabled by setting the applicable mute control to 0 (see Table 44).

Soft Mute Mode would typically be enabled (DAC_SOFTMUTEMODE = 1) when using mute during playback of audio data so that when the mute is subsequently disabled, the volume increase will not create pop noise by jumping immediately to the previous volume level (e.g. resuming playback after pausing during a track).

Soft Mute Mode would typically be disabled (DAC_SOFTMUTEMODE = 0) when un-muting at the start of a music file, in order that the first part of the track is not attenuated (e.g. when starting playback of a new track, or resuming playback after pausing between tracks).

The DAC soft-mute function is illustrated in Figure 26 for DAC1L and DAC1R. The same function is applicable to DAC2L and DAC2R also.

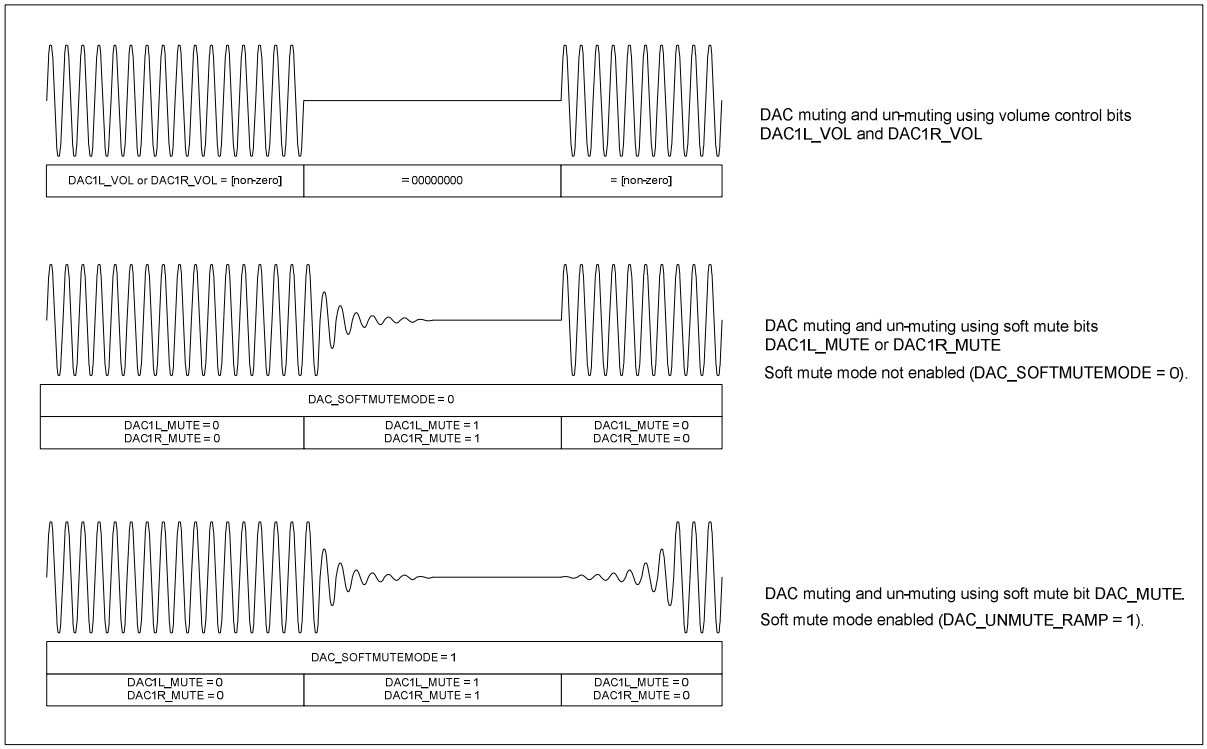


Figure 26 DAC Soft Mute Control

The DAC Soft Mute register controls are defined in Table 46.

The volume ramp rate during soft mute and un-mute is controlled by the DAC_MUTERATE bit. Ramp rates of fs/32 and fs/2 are selectable. The ramp rate determines the rate at which the volume will be increased or decreased. Note that the actual ramp time depends on the extent of the difference between the muted and un-muted volume settings.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1556 (0614h) DAC Softmute	1	DAC_SOFT MUTEMODE	0	DAC Unmute Ramp select 0 = Disabling soft-mute (DAC[1/2][L/R]_MUTE=0) will cause the DAC volume to change immediately to DAC[1/2][L/R]_VOL settings 1 = Disabling soft-mute (DAC[1/2][L/R]_MUTE=0) will cause the DAC volume to ramp up gradually to the DAC[1/2][L/R]_VOL settings
	0	DAC_MUTE RATE	0	DAC Soft Mute Ramp Rate 0 = Fast ramp (fs/2, maximum ramp time is 10.7ms at fs=48k) 1 = Slow ramp (fs/32, maximum ramp time is 171ms at fs=48k) (Note: ramp rate scales with sample rate.)

Table 46 DAC Soft-Mute Control

OUTPUT SIGNAL PATH

The WM8994 output routing and mixers provide a high degree of flexibility, allowing operation of many simultaneous signal paths through the device to a variety of analogue outputs. The outputs include a ground referenced headphone driver, two switchable class D/AB loudspeaker drivers, an ear speaker driver and four highly flexible line drivers. See “Analogue Outputs” for further details of these outputs.

The WM8994 output signal paths and control registers are illustrated in Figure 27.

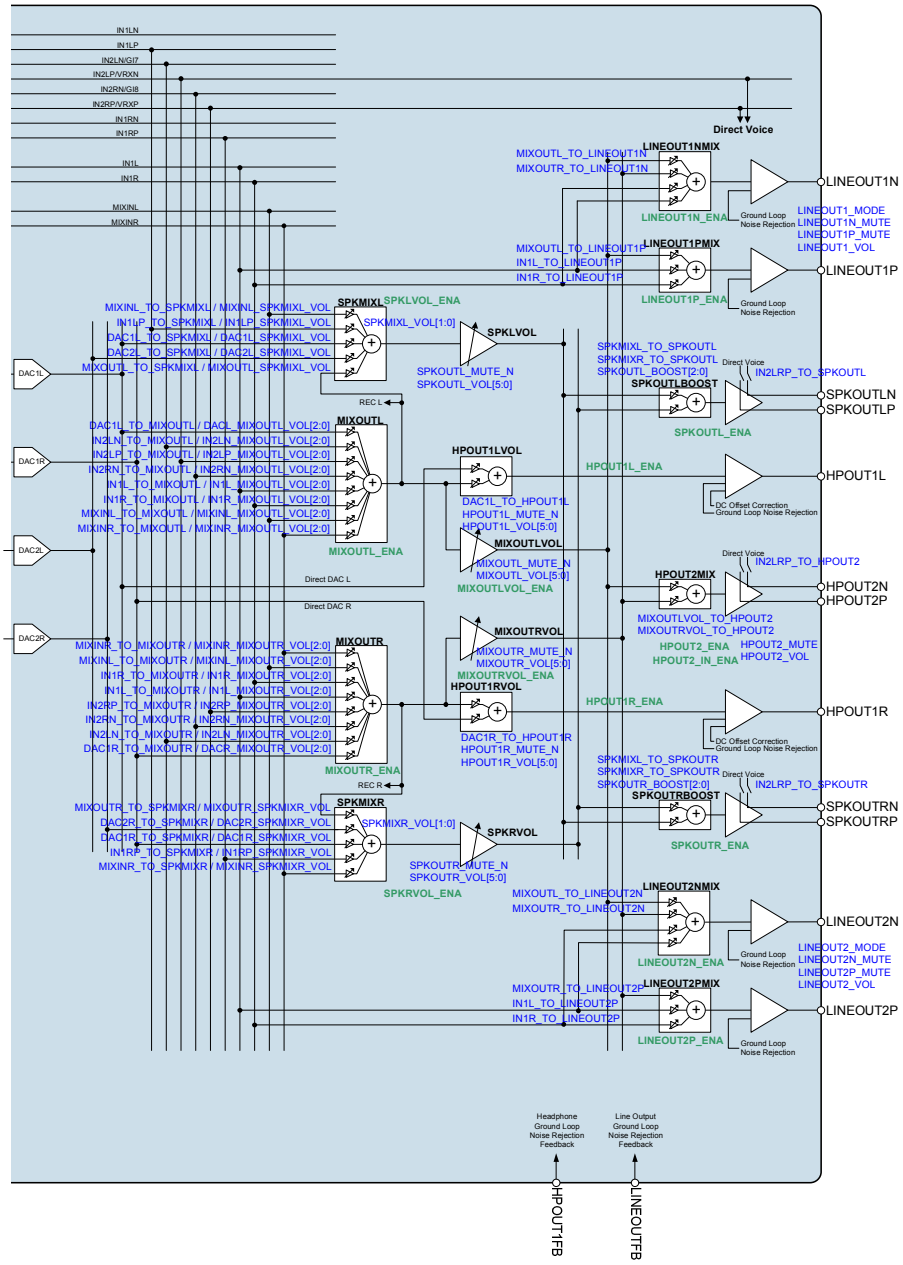


Figure 27 Control Registers for Output Signal Path

OUTPUT SIGNAL PATHS ENABLE

The output mixers and drivers can be independently enabled and disabled as described in Table 47.

Note that the headphone outputs HPOUT1L and HPOUT1R have dedicated output PGAs and volume controls. As a result, a low power consumption DAC playback path can be supported without needing to enable the output mixers MIXOUTL / MIXOUTR or the mixer output PGAs MIXOUTLVOL / MIXOUTRVOL.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (0001h) Power Management (1)	13	SPKOUTR_ENA	0	SPKMIXR Mixer, SPKRVOL PGA and SPKOUTR Output Enable 0 = Disabled 1 = Enabled
	12	SPKOUTL_ENA	0	SPKMIXL Mixer, SPKLVOL PGA and SPKOUTL Output Enable 0 = Disabled 1 = Enabled
	11	HPOUT2_ENA	0	HPOUT2 Output Stage Enable 0 = Disabled 1 = Enabled
	9	HPOUT1L_ENA	0	Enables HPOUT1L input stage 0 = Disabled 1 = Enabled Note: When HPOUT1_AUTO_PU is set, the HPOUT1L_ENA bit automatically enables all stages of the left headphone driver
	8	HPOUT1R_ENA	0	Enables HPOUT1R input stage 0 = Disabled 1 = Enabled Note: When HPOUT1_AUTO_PU is set, the HPOUT1R_ENA bit automatically enables all stages of the right headphone driver
R3 (0003h) Power Management (3)	13	LINEOUT1N_ENA	0	LINEOUT1N Line Out and LINEOUT1NMIX Enable 0 = Disabled 1 = Enabled
	12	LINEOUT1P_ENA	0	LINEOUT1P Line Out and LINEOUT1PMIX Enable 0 = Disabled 1 = Enabled
	11	LINEOUT2N_ENA	0	LINEOUT2N Line Out and LINEOUT2NMIX Enable 0 = Disabled 1 = Enabled
	10	LINEOUT2P_ENA	0	LINEOUT2P Line Out and LINEOUT2PMIX Enable 0 = Disabled 1 = Enabled
	9	SPKRVOL_ENA	0	SPKMIXR Mixer and SPKRVOL PGA Enable 0 = Disabled 1 = Enabled Note that SPKMIXR and SPKRVOL are also enabled when SPKOUTR_ENA is set.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	8	SPKLVOL_ENA	0	SPKMIXL Mixer and SPKLVOL PGA Enable 0 = Disabled 1 = Enabled Note that SPKMIXL and SPKLVOL are also enabled when SPKOUTL_ENA is set.
	7	MIXOUTLVOL_ENA	0	MIXOUTL Left Volume Control Enable 0 = Disabled 1 = Enabled
	6	MIXOUTRVOL_ENA	0	MIXOUTR Right Volume Control Enable 0 = Disabled 1 = Enabled
	5	MIXOUTL_ENA	0	MIXOUTL Left Output Mixer Enable 0 = Disabled 1 = Enabled
	4	MIXOUTR_ENA	0	MIXOUTR Right Output Mixer Enable 0 = Disabled 1 = Enabled
R56 (0038h) AntiPOP1	6	HPOUT2_IN_ENA	0	HPOUT2MIX Mixer and Input Stage Enable 0 = Disabled 1 = Enabled

Table 47 Output Signal Paths Enable

OUTPUT MIXER CONTROL

The Output Mixer path select and volume controls are described in Table 48 for the Left Channel (MIXOUTL) and Table 49 for the Right Channel (MIXOUTR). The gain of each of input path may be controlled independently in the range described in Table 50. Note that the DAC input levels may also be controlled by the DAC digital volume controls (see “Digital to Analogue Converter (DAC)”) and the Audio Interface digital volume controls (see “Digital Volume and Filter Control”).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R45 (002Dh) Output Mixer1	5	IN2RN_TO_MIXOUTL	0	IN2RN to MIXOUTL Mute 0 = Mute 1 = Un-mute
R49 (0031h) Output Mixer5	8:6	IN2RN_MIXOUTL_VOL [2:0]	000	IN2RN to MIXOUTL Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB (See Table 50 for Volume Range)
R45 (002Dh) Output Mixer1	4	IN2LN_TO_MIXOUTL	0	IN2LN to MIXOUTL Mute 0 = Mute 1 = Un-mute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R47 (002Fh) Output Mixer3	8:6	IN2LN_MIXOUTL_VOL [2:0]	000	IN2LN to MIXOUTL Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB (See Table 50 for Volume Range)
R45 (002Dh) Output Mixer1	2	IN1L_TO_MIXOUTL	0	IN1L PGA Output to MIXOUTL Mute 0 = Mute 1 = Un-mute
R47 (002Fh) Output Mixer3	2:0	IN1L_MIXOUTL_VOL [2:0]	000	IN1L PGA Output to MIXOUTL Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB (See Table 50 for Volume Range)
R45 (002Dh) Output Mixer1	3	IN1R_TO_MIXOUTL	0	IN1R PGA Output to MIXOUTL Mute 0 = Mute 1 = Un-mute
R47 (002Fh) Output Mixer3	5:3	IN1R_MIXOUTL_VOL [2:0]	000	IN1R PGA Output to MIXOUTL Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB (See Table 50 for Volume Range)
R45 (002Dh) Output Mixer1	1	IN2LP_TO_MIXOUTL	0	IN2LP to MIXOUTL Mute 0 = Mute 1 = Un-mute
R47 (002Fh) Output Mixer3	11:9	IN2LP_MIXOUTL_VOL [2:0]	00b	IN2LP to MIXOUTL Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB (See Table 50 for Volume Range)
R45 (002Dh) Output Mixer1	7	MIXINR_TO_MIXOUTL	0	MIXINR Output (Right ADC bypass) to MIXOUTL Mute 0 = Mute 1 = Un-mute
R49 (0031h) Output Mixer5	5:3	MIXINR_MIXOUTL_VOL [2:0]	000	MIXINR Output (Right ADC bypass) to MIXOUTL Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB (See Table 50 for Volume Range)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R45 (002Dh) Output Mixer1	6	MIXINL_TO_MIXOUTL	0	MIXINL Output (Left ADC bypass) to MIXOUTL Mute 0 = Mute 1 = Un-mute
R49 (0031h) Output Mixer5	2:0	MIXINL_MIXOUTL_VOL [2:0]	000	MIXINL Output (Left ADC bypass) to MIXOUTL Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB (See Table 50 for Volume Range)
R45 (002Dh) Output Mixer1	0	DAC1L_TO_MIXOUTL	0	Left DAC1 to MIXOUTL Mute 0 = Mute 1 = Un-mute
R49 (0031h) Output Mixer5	11:9	DACL_MIXOUTL_VOL [2:0]	000	Left DAC1 to MIXOUTL Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB (See Table 50 for Volume Range)

Table 48 Left Output Mixer (MIXOUTL) Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R46 (002Eh) Output Mixer2	5	IN2LN_TO_MIXOUTR	0	IN2LN to MIXOUTR Mute 0 = Mute 1 = Un-mute
R50 (0032h) Output Mixer6	8:6	IN2LN_MIXOUTR_VOL [2:0]	000	IN2LN to MIXOUTR Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB (See Table 50 for Volume Range)
R46 (002Eh) Output Mixer2	4	IN2RN_TO_MIXOUTR	0	IN2RN to MIXOUTR Mute 0 = Mute 1 = Un-mute
R48 (0030h) Output Mixer4	8:6	IN2RN_MIXOUTR_VOL [2:0]	000	IN2RN to MIXOUTR Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB (See Table 50 for Volume Range)
R46 (002Eh) Output Mixer2	3	IN1L_TO_MIXOUTR	0	IN1L PGA Output to MIXOUTR Mute 0 = Mute 1 = Un-mute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R48 (0030h) Output Mixer4	5:3	IN1L_MIXOUTR_VOL [2:0]	000	IN1L PGA Output to MIXOUTR Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB (See Table 50 for Volume Range)
R46 (002Eh) Output Mixer2	2	IN1R_TO_MIXOUTR	0	IN1R PGA Output to MIXOUTR Mute 0 = Mute 1 = Un-mute
R48 (0030h) Output Mixer4	2:0	IN1R_MIXOUTR_VOL [2:0]	000	IN1R PGA Output to MIXOUTR Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB (See Table 50 for Volume Range)
R46 (002Eh) Output Mixer2	1	IN2RP_TO_MIXOUTR	0	IN2RP to MIXOUTR Mute 0 = Mute 1 = Un-mute
R48 (0030h) Output Mixer4	11:9	IN2RP_MIXOUTR_VOL [2:0]	000	IN2RP to MIXOUTR Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB (See Table 50 for Volume Range)
R46 (002Eh) Output Mixer2	7	MIXINL_TO_MIXOUTR	0	MIXINL Output (Left ADC bypass) to MIXOUTR Mute 0 = Mute 1 = Un-mute
R50 (0032h) Output Mixer6	5:3	MIXINL_MIXOUTR_VOL[2:0]	000	MIXINL Output (Left ADC bypass) to MIXOUTR Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB (See Table 50 for Volume Range)
R46 (002Eh) Output Mixer2	6	MIXINR_TO_MIXOUTR	0	MIXINR Output (Right ADC bypass) to MIXOUTR Mute 0 = Mute 1 = Un-mute
R50 (0032h) Output Mixer6	2:0	MIXINR_MIXOUTR_VOL [2:0]	000	MIXINR Output (Right ADC bypass) to MIXOUTR Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB (See Table 50 for Volume Range)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R46 (002Eh) Output Mixer2	0	DAC1R_TO_MIXOUTR	0	Right DAC1 to MIXOUTR Mute 0 = Mute 1 = Un-mute
R50 (0032h) Output Mixer6	11:9	DACR_MIXOUTR_VOL [2:0]	000	Right DAC1 to MIXOUTR Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB (See Table 50 for Volume Range)

Table 49 Right Output Mixer (MIXOUTR) Control

VOLUME SETTING	VOLUME (dB)
000	0
001	-3
010	-6
011	-9
100	-12
101	-15
110	-18
111	-21

Table 50 MIXOUTL and MIXOUTR Volume Range

SPEAKER MIXER CONTROL

The Speaker Mixer path select and volume controls are described in Table 51 for the Left Channel (SPKMIXL) and Table 52 for the Right Channel (SPKMIXR).

Care should be taken when enabling more than one path to a speaker mixer in order to avoid clipping. The gain of each input path is adjustable using a selectable -3dB control in each path to facilitate this. Each Speaker Mixer output is also controlled by an additional independent volume control. Note that the DAC input levels may also be controlled by the DAC digital volume controls (see "Digital to Analogue Converter (DAC)") and the Audio Interface digital volume controls (see "Digital Volume and Filter Control").

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R54 (0034h) Speaker Mixer	9	DAC2L_TO_SPKMIXL	0	Left DAC2 to SPKMIXL Mute 0 = Mute 1 = Un-mute
	7	MIXINL_TO_SPKMIXL	0	MIXINL (Left ADC bypass) to SPKMIXL Mute 0 = Mute 1 = Un-mute
	5	IN1LP_TO_SPKMIXL	0	IN1LP to SPKMIXL Mute 0 = Mute 1 = Un-mute
	3	MIXOUTL_TO_SPKMIXL	0	Left Mixer Output to SPKMIXL Mute 0 = Mute 1 = Un-mute
	1	DAC1L_TO_SPKMIXL	0	Left DAC1 to SPKMIXL Mute 0 = Mute 1 = Un-mute
R34 (0022h) SPKMIXL Attenuation	6	DAC2L_SPKMIXL_VOL	0	Left DAC2 to SPKMIXL Fine Volume Control 0 = 0dB 1 = -3dB
	5	MIXINL_SPKMIXL_VOL	0	MIXINL (Left ADC bypass) to SPKMIXL Fine Volume Control 0 = 0dB 1 = -3dB
	4	IN1LP_SPKMIXL_VOL	0	IN1LP to SPKMIXL Fine Volume Control 0 = 0dB 1 = -3dB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3	MIXOUTL_SPKMIXL_VOL	0	Left Mixer Output to SPKMIXL Fine Volume Control 0 = 0dB 1 = -3dB
	2	DAC1L_SPKMIXL_VOL	0	Left DAC1 to SPKMIXL Fine Volume Control 0 = 0dB 1 = -3dB
	1:0	SPKMIXL_VOL [1:0]	11	Left Speaker Mixer Volume Control 00 = 0dB 01 = -6dB 10 = -12dB 11 = mute

Table 51 Left Speaker Mixer (SPKMIXL) Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R54 (0034h) Speaker Mixer	8	DAC2R_TO_SPKMIXR	0	Right DAC2 to SPKMIXR Mute 0 = Mute 1 = Un-mute
	6	MIXINR_TO_SPKMIXR	0	MIXINR (Right ADC bypass) to SPKMIXR Mute 0 = Mute 1 = Un-mute
	4	IN1RP_TO_SPKMIXR	0	IN1RP to SPKMIXR Mute 0 = Mute 1 = Un-mute
	2	MIXOUTR_TO_SPKMIXR	0	Right Mixer Output to SPKMIXR Mute 0 = Mute 1 = Un-mute
	0	DAC1R_TO_SPKMIXR	0	Right DAC1 to SPKMIXR Mute 0 = Mute 1 = Un-mute
R35 (0022h) SPKMIXR Attenuation	6	DAC2R_SPKMIXR_VOL	0	Right DAC2 to SPKMIXR Fine Volume Control 0 = 0dB 1 = -3dB
	5	MIXINR_SPKMIXR_VOL	0	MIXINR (Right ADC bypass) to SPKMIXR Fine Volume Control 0 = 0dB 1 = -3dB
	4	IN1RP_SPKMIXR_VOL	0	IN1RP to SPKMIXR Fine Volume Control 0 = 0dB 1 = -3dB
	3	MIXOUTR_SPKMIXR_VOL	0	Right Mixer Output to SPKMIXR Fine Volume Control 0 = 0dB 1 = -3dB
	2	DAC1R_SPKMIXR_VOL	0	Right DAC1 to SPKMIXR Fine Volume Control 0 = 0dB 1 = -3dB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1:0	SPKMIXR_VOL [1:0]	11	Right Speaker Mixer Volume Control 00 = 0dB 01 = -6dB 10 = -12dB 11 = mute

Table 52 Right Speaker Mixer (SPKMIXR) Control

OUTPUT SIGNAL PATH VOLUME CONTROL

There are six output PGAs - MIXOUTLVOL, MIXOUTRVOL, HPOUT1LVOL, HPOUT1RVOL, SPKLVOL and SPKRVOL. Each can be independently controlled, with MIXOUTLVOL and MIXOUTRVOL providing volume control to both the earpiece and line drivers, HPOUT1LVOL and HPOUT1RVOL to the headphone driver, and SPKLVOL and SPKRVOL to the speaker drivers.

The volume control of each of these output PGAs can be adjusted over a wide range of values. To minimise pop noise, it is recommended that only the MIXOUTLVOL, MIXOUTRVOL, HPOUT1LVOL, HPOUT1RVOL, SPKLVOL and SPKRVOL are modified while the output signal path is active. Other gain controls are provided in the signal paths to provide scaling of signals from different sources, and to prevent clipping when multiple signals are mixed. However, to prevent pop noise, it is recommended that those other gain controls should not be modified while the signal path is active.

To prevent "zipper noise", a zero-cross function is provided on the output PGAs. When this feature is enabled, volume updates will not take place until a zero-crossing is detected. In the case of a long period without zero-crossings, a timeout function is provided. When the zero-cross function is enabled, the volume will update after the timeout period if no earlier zero-cross has occurred. The timeout clock is enabled using TOCLK_ENA; the timeout period is set by TOCLK_RATE. See “Clocking and Sample Rates” for more information on these fields.

The mixer output PGA controls are shown in Table 53. The MIXOUT_VU bits control the loading of the output mixer PGA volume data. When MIXOUT_VU is set to 0, the volume control data will be loaded into the respective control register, but will not actually change the gain setting. The output mixer PGA volume settings are both updated when a 1 is written to either MIXOUT_VU bit. This makes it possible to update the gain of both output paths simultaneously.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (0020h) Left OPGA Volume	8	MIXOUT_VU	N/A	Mixer Output PGA Volume Update Writing a 1 to this bit will update MIXOUTLVOL and MIXOUTRVOL volumes simultaneously.
	7	MIXOUTL_ZC	0	MIXOUTLVOL (Left Mixer Output PGA) Zero Cross Enable 0 = Zero cross disabled 1 = Zero cross enabled
	6	MIXOUTL_MUTE_N	1	MIXOUTLVOL (Left Mixer Output PGA) Mute 0 = Mute 1 = Un-mute
	5:0	MIXOUTL_VOL [5:0]	39h (0dB)	MIXOUTLVOL (Left Mixer Output PGA) Volume -57dB to +6dB in 1dB steps 00_0000 = -57dB 00_0001 = -56dB … (1dB steps) 11_1111 = +6dB (See Table 56 for output PGA volume control range)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R33 (0021h) Right OPGA Volume	8	MIXOUT_VU	N/A	Mixer Output PGA Volume Update Writing a 1 to this bit will update MIXOUTLVOL and MIXOUTRVOL volumes simultaneously.
	7	MIXOUTR_ZC	0	MIXOUTRVOL (Right Mixer Output PGA) Zero Cross Enable 0 = Zero cross disabled 1 = Zero cross enabled
	6	MIXOUTR_MUTE_N	1	MIXOUTLVOL (Right Mixer Output PGA) Mute 0 = Mute 1 = Un-mute
	5:0	MIXOUTR_VOL [5:0]	39h (0dB)	MIXOUTRVOL (Right Mixer Output PGA) Volume -57dB to +6dB in 1dB steps 00_0000 = -57dB 00_0001 = -56dB … (1dB steps) 11_1111 = +6dB (See Table 56 for output PGA volume control range)

Table 53 Mixer Output PGA (MIXOUTLVOL, MIXOUTRVOL) Control

The headphone output PGA is configurable between two input sources. The default input to each headphone output PGA is the respective output mixer (MIXOUTL or MIXOUTR). A direct path from the DACL or DACR can be selected using the DACL_TO_HPOUT1L and DACR_TO_HPOUT1R register bits. When these bits are selected, a DAC to Headphone playback path is possible without using the output mixers; this offers reduced power consumption by allowing the output mixers to be disabled in this typical usage case.

The headphone output PGA controls are shown in Table 54. The HPOUT1_VU bits control the loading of the headphone PGA volume data. When HPOUT1_VU is set to 0, the volume control data will be loaded into the respective control register, but will not actually change the gain setting. The headphone PGA volume settings are both updated when a 1 is written to either HPOUT1_VU bit. This makes it possible to update the gain of both output paths simultaneously.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R28 (001Ch) Left Output Volume	8	HPOUT1_VU	N/A	Headphone Output PGA Volume Update Writing a 1 to this bit will update HPOUT1LVOL and HPOUT1RVOL volumes simultaneously.
	7	HPOUT1L_ZC	0	HPOUT1LVOL (Left Headphone Output PGA) Zero Cross Enable 0 = Zero cross disabled 1 = Zero cross enabled
	6	HPOUT1L_MUTE_N	1	HPOUT1LVOL (Left Headphone Output PGA) Mute 0 = Mute 1 = Un-mute
	5:0	HPOUT1L_VOL [5:0]	2Dh (-12dB)	HPOUT1LVOL (Left Headphone Output PGA) Volume -57dB to +6dB in 1dB steps 00_0000 = -57dB 00_0001 = -56dB … (1dB steps) 11_1111 = +6dB (See Table 56 for output PGA volume control range)
R45 (002Dh) Output Mixer1	8	DAC1L_TO_HPOUT1L	0	HPOUT1LVOL (Left Headphone Output PGA) Input Select 0 = MIXOUTL 1 = DAC1L
R29 (001Dh) Right Output Volume	8	HPOUT1_VU	N/A	Headphone Output PGA Volume Update Writing a 1 to this bit will update HPOUT1LVOL and HPOUT1RVOL volumes simultaneously.
	7	HPOUT1R_ZC	0	HPOUT1RVOL (Right Headphone Output PGA) Zero Cross Enable 0 = Zero cross disabled 1 = Zero cross enabled
	6	HPOUT1R_MUTE_N	1	HPOUT1RVOL (Right Headphone Output PGA) Mute 0 = Mute 1 = Un-mute
	5:0	HPOUT1R_VOL [5:0]	2Dh (-12dB)	HPOUT1RVOL (Right Headphone Output PGA) Volume -57dB to +6dB in 1dB steps 00_0000 = -57dB 00_0001 = -56dB … (1dB steps) 11_1111 = +6dB (See Table 56 for output PGA volume control range)
R46 (002Eh) Output Mixer2	8	DAC1R_TO_HPOUT1R	0	HPOUT1RVOL (Right Headphone Output PGA) Input Select 0 = MIXOUTR 1 = DAC1R

Table 54 Headphone Output PGA (HPOUT1LVOL, HPOUT1RVOL) Control

The speaker output PGA controls are shown in Table 55.The SPKOUT_VU bits control the loading of the speaker PGA volume data. When SPKOUT_VU is set to 0, the volume control data will be loaded into the respective control register, but will not actually change the gain setting. The speaker PGA volume settings are both updated when a 1 is written to either SPKOUT_VU bit. This makes it possible to update the gain of both output paths simultaneously.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R38 (0026h) Speaker Volume Left	8	SPKOUT_VU	N/A	Speaker Output PGA Volume Update Writing a 1 to this bit will update SPKLVOL and SPKRVOL volumes simultaneously.
	7	SPKOUTL_ZC	0	SPKLVOL (Left Speaker Output PGA) Zero Cross Enable 0 = Zero cross disabled 1 = Zero cross enabled
	6	SPKOUTL_MUTE_N	1	SPKLVOL (Left Speaker Output PGA) Mute 0 = Mute 1 = Un-mute
	5:0	SPKOUTL_VOL [5:0]	39h (0dB)	SPKLVOL (Left Speaker Output PGA) Volume -57dB to +6dB in 1dB steps 00_0000 = -57dB 00_0001 = -56dB … (1dB steps) 11_1111 = +6dB (See Table 56 for output PGA volume control range)
R39 (0027h) Speaker Volume Right	8	SPKOUT_VU	N/A	Speaker PGA Volume Update Writing a 1 to this bit will update SPKLVOL and SPKRVOL volumes simultaneously.
	7	SPKOUTR_ZC	0	SPKRVOL (Right Speaker Output PGA) Zero Cross Enable 0 = Zero cross disabled 1 = Zero cross enabled
	6	SPKOUTR_MUTE_N	1	SPKRVOL (Right Speaker Output PGA) Mute 0 = Mute 1 = Un-mute
	5:0	SPKOUTR_VOL [5:0]	39h (0dB)	SPKRVOL (Right Speaker Output PGA) Volume -57dB to +6dB in 1dB steps 00_0000 = -57dB 00_0001 = -56dB … (1dB steps) 11_1111 = +6dB (See Table 56 for output PGA volume control range)

Table 55 Speaker Output PGA (SPKLVOL, SPKRVOL) Control

PGA GAIN SETTING	VOLUME (dB)	PGA GAIN SETTING	VOLUME (dB)
00h	-57	20h	-25
01h	-56	21h	-24
02h	-55	22h	-23
03h	-54	23h	-22
04h	-53	24h	-21
05h	-52	25h	-20
06h	-51	26h	-19
07h	-50	27h	-18
08h	-49	28h	-17
09h	-48	29h	-16
0Ah	-47	2Ah	-15
0Bh	-46	2Bh	-14
0Ch	-45	2Ch	-13
0Dh	-44	2Dh	-12
0Eh	-43	2Eh	-11
0Fh	-42	2Fh	-10
10h	-41	30h	-9
11h	-40	31h	-8
12h	-39	32h	-7
13h	-38	33h	-6
14h	-37	34h	-5
15h	-36	35h	-4
16h	-35	36h	-3
17h	-34	37h	-2
18h	-33	38h	-1
19h	-32	39h	0
1Ah	-31	3Ah	+1
1Bh	-30	3Bh	+2
1Ch	-29	3Ch	+3
1Dh	-28	3Dh	+4
1Eh	-27	3Eh	+5
1Fh	-26	3Fh	+6

Table 56 Output PGA Volume Range

SPEAKER BOOST MIXER

Each class D/AB speaker driver has its own boost mixer which performs a dual role. It allows the output from the left speaker mixer (via SPKLVOL), right speaker mixer (via SPKRVOL), or the 'Direct Voice' path to be routed to either speaker driver. (The 'Direct Voice' path is the differential input, VRXN/VRXP, routed directly to the output drivers, providing a low power differential path from baseband voice to loudspeakers.) The speaker boost mixers are controlled using the registers defined in Table 57 below.

The second function of the speaker boost mixers is that they provide an additional AC gain (boost) function to shift signal levels between the AVDD1 and SPKVDD voltage domains for maximum output power. The AC gain (boost) function is described in the "Analogue Outputs" section.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R36 (0024h) SPKOUT Mixers	5	IN2LP_TO_SPKOUTL	0	Differential Input (IN2RP/IN2LP) to Left Speaker Mute 0 = Mute 1 = Un-mute
	4	SPKMIXL_TO_SPKOUTL	1	SPKMIXL Left Speaker Mixer to Left Speaker Mute 0 = Mute 1 = Un-mute
	3	SPKMIXR_TO_SPKOUTL	0	SPKMIXR Right Speaker Mixer to Left Speaker Mute 0 = Mute 1 = Un-mute
	2	IN2LP_TO_SPKOUTR	0	Differential Input (IN2RP/IN2LP) to Right Speaker Mute 0 = Mute 1 = Un-mute
	1	SPKMIXL_TO_SPKOUTR	0	SPKMIXL Left Speaker Mixer to Right Speaker Mute 0 = Mute 1 = Un-mute
	0	SPKMIXR_TO_SPKOUTR	1	SPKMIXR Right Speaker Mixer to Right Speaker Mute 0 = Mute 1 = Un-mute

Table 57 Speaker Boost Mixer (SPKOUTLBOOST, SPKOUTRBOOST) Control

EARPIECE DRIVER MIXER

The earpiece driver has a dedicated mixer, HPOUT2MIX, which is controlled using the registers defined in Table 58. The earpiece driver is configurable to select output from the left output mixer (via MIXOUTLVOL), the right output mixer (via MIXOUTRVOL), or the 'Direct Voice' path. (The 'Direct Voice' path is the differential input, VRXN/VRXP, routed directly to the output drivers, providing a low power differential path from baseband voice to earpiece.)

Care should be taken to avoid clipping when enabling more than one path to the earpiece driver. The HPOUT2VOL volume control can be used to avoid clipping when more than one full scale signal is input to the mixer.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R31 (001Fh) HPOUT2 Volume	5	HPOUT2_MUTE	1	HPOUT2 (Earpiece Driver) Mute 0 = Un-mute 1 = Mute
	4	HPOUT2_VOL	0	HPOUT2 (Earpiece Driver) Volume 0 = 0dB 1 = -6dB
R51 (0033h) HPOUT2 Mixer	5	IN2LRP_TO_HPOUT2	0	Differential Input (IN2RP/IN2LP) to Earpiece Driver 0 = Mute 1 = Un-mute
	4	MIXOUTLVOL_TO_HPOUT2	0	MIXOUTLVOL (Left Output Mixer PGA) to Earpiece Driver 0 = Mute 1 = Un-mute
	3	MIXOUTRVOL_TO_HPOUT2	0	MIXOUTRVOL (Right Output Mixer PGA) to Earpiece Driver 0 = Mute 1 = Un-mute

Table 58 Earpiece Driver Mixer (HPOUT2MIX) Control

LINE OUTPUT MIXERS

The WM8994 provides two pairs of line outputs, both with highly configurable output mixers. The outputs LINEOUT1N and LINEOUT1P can be configured as two single-ended outputs or as a differential output. In the same manner, LINEOUT2N and LINEOUT2P can be configured either as two single-ended outputs or as a differential output. The respective line output mixers can be configured in single-ended mode or differential mode; each mode supports multiple signal path configurations.

LINEOUT1 single-ended mode is selected by setting LINEOUT1_MODE = 1. In single-ended mode, any of three possible signal paths may be enabled:

- MIXOUTL (left output mixer) to LINEOUT1P
- MIXOUTR (right output mixer) to LINEOUT1N
- MIXOUTL (left output mixer) to LINEOUT1N

LINEOUT1 differential mode is selected by setting LINEOUT1_MODE = 0. In differential mode, any of three possible signal paths may be enabled:

- MIXOUTL (left output mixer) to LINEOUT1N and LINEOUT1P
- IN1L (input PGA) to LINEOUT1N and LINEOUT1P
- IN1R (input PGA) to LINEOUT1N and LINEOUT1P

The LINEOUT1 output mixers are controlled as described in Table 59. Care should be taken to avoid clipping when enabling more than one path to the line output mixers. The LINEOUT1_VOL control can be used to provide -6dB attenuation when more than one full scale signal is applied.

When using the LINEOUT1 mixers in single-ended mode, a buffered VMID must be enabled. This is achieved by setting LINEOUT_VMID_BUF_ENA, as described in the “Analogue Outputs” section.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R30 (001Eh) Line Outputs Volume	6	LINEOUT1N_MUTE	1	LINEOUT1N Line Output Mute 0 = Un-mute 1 = Mute
	5	LINEOUT1P_MUTE	1	LINEOUT1P Line Output Mute 0 = Un-mute 1 = Mute
	4	LINEOUT1_VOL	0	LINEOUT1 Line Output Volume 0 = 0dB 1 = -6dB Applies to both LINEOUT1N and LINEOUT1P
R52 (0034h) Line Mixer1	6	MIXOUTL_TO_LINEOUT1N	0	MIXOUTL to Single-Ended Line Output on LINEOUT1N 0 = Mute 1 = Un-mute (LINEOUT1_MODE = 1)
	5	MIXOUTR_TO_LINEOUT1N	0	MIXOUTR to Single-Ended Line Output on LINEOUT1N 0 = Mute 1 = Un-mute (LINEOUT1_MODE = 1)
	4	LINEOUT1_MODE	0	LINEOUT1 Mode Select 0 = Differential 1 = Single-Ended
	2	IN1R_TO_LINEOUT1P	0	IN1R Input PGA to Differential Line Output on LINEOUT1 0 = Mute 1 = Un-mute (LINEOUT1_MODE = 0)
	1	IN1L_TO_LINEOUT1P	0	IN1L Input PGA to Differential Line Output on LINEOUT1 0 = Mute 1 = Un-mute (LINEOUT1_MODE = 0)
	0	MIXOUTL_TO_LINEOUT1P	0	Differential Mode (LINEOUT1_MODE = 0): MIXOUTL to Differential Output on LINEOUT1 0 = Mute 1 = Un-mute Single Ended Mode (LINEOUT1_MODE = 1): MIXOUTL to Single-Ended Line Output on LINEOUT1P 0 = Mute 1 = Un-mute

Table 59 LINEOUT1N and LINEOUT1P Control

LINEOUT2 single-ended mode is selected by setting LINEOUT2_MODE = 1. In single-ended mode, any of three possible signal paths may be enabled:

- MIXOUTR (right output mixer) to LINEOUT2P
- MIXOUTL (left output mixer) to LINEOUT2N
- MIXOUTR (right output mixer) to LINEOUT2N

LINEOUT2 differential mode is selected by setting LINEOUT2_MODE = 0. In differential mode, any of three possible signal paths may be enabled:

- MIXOUTR (right output mixer) to LINEOUT2N and LINEOUT2P
- IN1L (input PGA) to LINEOUT2P and LINEOUT2P
- IN1R (input PGA) to LINEOUT2N and LINEOUT2P

The LINEOUT2 output mixers are controlled as described in Table 60. Care should be taken to avoid clipping when enabling more than one path to the line output mixers. The LINEOUT2_VOL control can be used to provide -6dB attenuation when more than one full scale signal is applied.

When using the LINEOUT2 mixers in single-ended mode, a buffered VMID must be enabled. This is achieved by setting LINEOUT_VMID_BUF_ENA, as described in the “Analogue Outputs” section.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R30 (001Eh) Line Outputs Volume	2	LINEOUT2N_MUTE	1	LINEOUT2N Line Output Mute 0 = Un-mute 1 = Mute
	1	LINEOUT2P_MUTE	1	LINEOUT2P Line Output Mute 0 = Un-mute 1 = Mute
	0	LINEOUT2_VOL	0	LINEOUT2 Line Output Volume 0 = 0dB 1 = -6dB Applies to both LINEOUT2N and LINEOUT2P
R53 (0035h) Line Mixer2	6	MIXOUTR_TO_LINEOUT2N	0	MIXOUTR to Single-Ended Line Output on LINEOUT2N 0 = Mute 1 = Un-mute (LINEOUT2_MODE = 1)
	5	MIXOUTL_TO_LINEOUT2N	0	MIXOUTL to Single-Ended Line Output on LINEOUT2N 0 = Mute 1 = Un-mute (LINEOUT2_MODE = 1)
	4	LINEOUT2_MODE	0	LINEOUT2 Mode Select 0 = Differential 1 = Single-Ended
	2	IN1L_TO_LINEOUT2P	0	IN1L Input PGA to Differential Line Output on LINEOUT2 0 = Mute 1 = Un-mute (LINEOUT2_MODE = 0)
	1	IN1R_TO_LINEOUT2P	0	IN1R Input PGA to Differential Line Output on LINEOUT2 0 = Mute 1 = Un-mute (LINEOUT2_MODE = 0)
	0	MIXOUTR_TO_LINEOUT2P	0	Differential Mode (LINEOUT2_MODE = 0): MIXOUTR to Differential Output on LINEOUT2 0 = Mute 1 = Un-mute Single-Ended Mode (LINEOUT2_MODE = 0): MIXOUTR to Single-Ended Line Output on LINEOUT2P 0 = Mute 1 = Un-mute

Table 60 LINEOUT2N and LINEOUT2P Control

ANALOGUE OUTPUTS

The speaker, headphone, earpiece and line outputs are highly configurable and may be used in many different ways.

SPEAKER OUTPUT CONFIGURATIONS

The speaker outputs SPKOUTL and SPKOUTR can be driven by either of the speaker mixers, SPKMIXL or SPKMIXR, or by the low power, differential Direct Voice path from IN2LP/VRXN and IN2RP/VRXP. Fine volume control is available on the speaker mixer paths using the SPKLVOL and SPKRVOL PGAs. A boost function is available on both the speaker mixer paths and the Direct Voice path. For information on the speaker mixing options, refer to the "Output Signal Path" section.

The speaker outputs SPKOUTL and SPKOUTR operate in a BTL configuration in Class AB or Class D amplifier modes. The default mode is class D but class AB mode can be selected by setting the SPARE_SPKMIX register bit, as defined in Table 62. The speaker outputs may be configured in two ways:

1. Stereo Mode – supports up to 1W into stereo 8Ω BTL loads
2. Mono Mode – supports up to 2W into a single 4Ω BTL load

The 2W Mono mode is selected by applying a logic high input to the SPKMODE pin (A3), as described in Table 61. For Stereo mode this pin should be connected to GND. Note that SPKMODE is referenced to DBVDD.

SPEAKER CONFIGURATION	SPKMODE PIN (A3)
Stereo Mode	GND
Mono Mode	DBVDD

Table 61 SPKMONO Pin Function

For 2W mono operation, the P channels, SPKOUTLP and SPKOUTRP should be connected together on the PCB, and similarly with the N channels, SPKOUTLN and SPKOUTRN, as illustrated in Figure 28. In this configuration both left and right speaker drivers should be enabled (SPKOUTL_ENA=1 and SPKOUTR_ENA=1), but path selection and volume controls are available on left channel only (SPKMIXL, SPKLVOL and SPKOUTLBOOST).

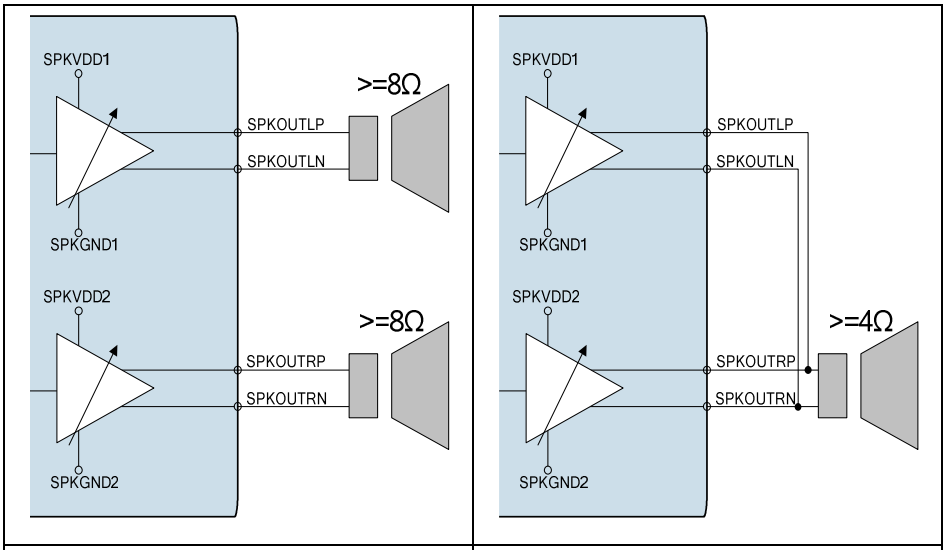


Figure 28 Stereo 1W / 8Ω and Mono 2W / 4Ω Speaker Output Configurations

Note that for applications with only a mono 8Ω speaker it is possible to improve THD performance at higher power levels by configuring the output in mono mode instead of running either the left of right channel in stereo mode.

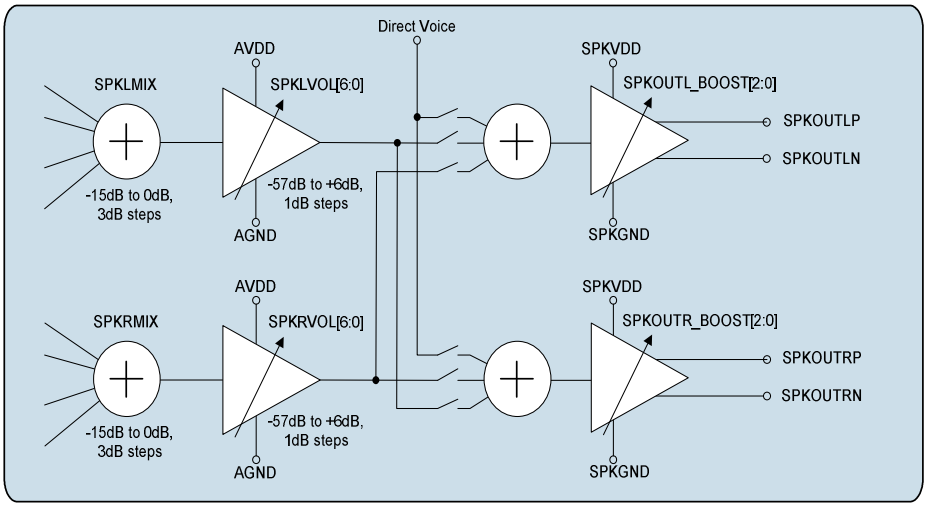
Eight levels of AC signal boost are provided in order to deliver maximum output power for many commonly-used SPKVDD/AVDD1 combinations. (Note that SPKVDD1 powers the Left Speaker driver, and SPKVDD2 powers the Right Speaker driver; it is assumed that SPKVDD1 = SPKVDD2 = SPKVDD.)

The signal boost options are available in both Class AB and Class D modes. The AC boost levels from 0dB to +12dB are selected using register bits SPKOUTL_BOOST and SPKOUTR_BOOST. To prevent pop noise, SPKOUTL_BOOST and SPKOUTR_BOOST should not be modified while the speaker outputs are enabled. Figure 29 illustrates the speaker outputs and the mixing and gain/boost options available.

Ultra-low leakage and high PSRR allow the speaker supply SPKVDD to be directly connected to a lithium battery. Note that an appropriate SPKVDD supply voltage must be provided to prevent waveform clipping when speaker boost is used.

DC gain is applied automatically in both class AB and class D modes with a shift from VMID to SPKVDD/2. This provides optimum signal swing for maximum output power. In class AB mode, an ultra-high PSRR mode is available, in which the DC reference for the speaker driver is fixed at VMID. This mode is selected by enabling the SPKAB_REF_SEL bit (see Table 62). In this mode, the output power is limited but the driver will still be capable of driving more than 500mW in 8Ω while maintaining excellent suppression of noise on SPKVDD (for example, TDMA noise in a GSM phone application).

The AC and DC gain functions are illustrated in Figure 29.



SPKOUTL_BOOST SPKOUTR_BOOST
000 = 1.00x (+0dB)
000 = 1.19x (+1.5dB)
000 = 1.41x (+3.0dB)
000 = 1.68x (+4.5dB)
000 = 2.00x (+6.0dB)
000 = 2.37x (+7.5dB)
000 = 2.81x (+9.0dB)
000 = 3.98x (+12.0dB)

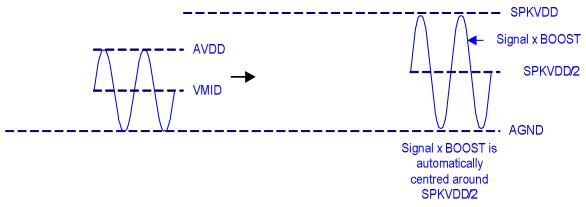


Figure 29 Speaker Output Configuration and AC Boost Operation

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R35 (0023h) SPKMIXR Attenuation	8	SPKOUT_CLASSAB	0b	Speaker Class AB Mode Enable 0 = Class D mode 1 = Class AB mode
R37 (0025h) SPKOUT Boost	5:3	SPKOUTL_BOOST [2:0]	000b (1.0x)	Left Speaker Gain Boost 000 = 1.00x boost (+0dB) 001 = 1.19x boost (+1.5dB) 010 = 1.41x boost (+3.0dB) 011 = 1.68x boost (+4.5dB) 100 = 2.00x boost (+6.0dB) 101 = 2.37x boost (+7.5dB) 110 = 2.81x boost (+9.0dB) 111 = 3.98x boost (+12.0dB)
	2:0	SPKOUTR_BOOST [2:0]	000b (1.0x)	Right Speaker Gain Boost 000 = 1.00x boost (+0dB) 001 = 1.19x boost (+1.5dB) 010 = 1.41x boost (+3.0dB) 011 = 1.68x boost (+4.5dB) 100 = 2.00x boost (+6.0dB) 101 = 2.37x boost (+7.5dB) 110 = 2.81x boost (+9.0dB) 111 = 3.98x boost (+12.0dB)
R34 (0022h) SPKMIXL Attenuation	8	SPARE_SPKMIX	0b	Selects Reference for Speaker in Class AB mode 0 = SPKVDD/2 1 = VMID

Table 62 Speaker Mode and Boost Control

HEADPHONE OUTPUT CONFIGURATIONS

The headphone outputs HPOUT1L and HPOUT1R are driven by the headphone output PGAs HPOUT1LVOL and HPOUT1RVOL. Each PGA has its own dedicated volume control, as described in the “Output Signal Path” section. The input to these PGAs can be either the output mixers MIXOUTL and MIXOUTR or the direct DAC1 outputs DAC1L and DAC1R.

The headphone output driver is capable of driving up to 30mW into a 16Ω load or 25mW into a 32Ω load such as a stereo headset or headphones. The outputs are ground-referenced, eliminating any requirement for AC coupling capacitors. This is achieved by having separate positive and negative supply rails powered by an on-chip charge pump. A DC Servo circuit removes any DC offset from the headphone outputs, suppressing ‘pop’ noise and minimising power consumption. The Charge Pump and DC Servo are described separately (see “Charge Pump” and “DC Servo” respectively).

It is recommended to connect a zobel network to the headphone output pins HPOUT1L and HPOUT1R for best audio performance in all applications. The components of the zobel network have the effect of dampening high frequency oscillations or instabilities that can arise outside the audio band under certain conditions. Possible sources of these instabilities include the inductive load of a headphone coil or an active load in the form of an external line amplifier. The capacitance of lengthy cables or PCB tracks can also lead to amplifier instability. The zobel network should comprise of a 20Ω resistor and 100nF capacitor in series with each other, as illustrated in Figure 30.

Note that the zobel network may be unnecessary in some applications; it depends upon the characteristics of the connected load. It is recommended to include these components for best audio quality and amplifier stability in all cases.

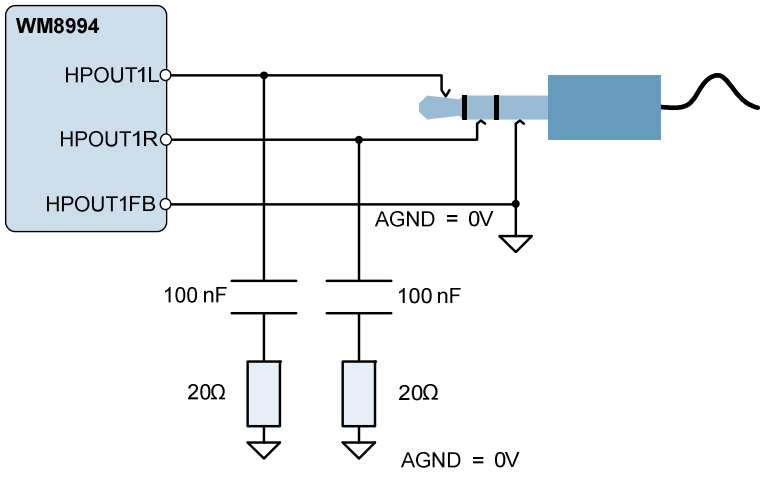


Figure 30 Zobel Network Components for HPOUT1L and HPOUT1R

The headphone output incorporates a common mode, or ground loop, feedback path which provides rejection of system-related ground noise. The return path is via HPOUT1FB. This pin must be connected to ground for normal operation of the headphone output. No register configuration is required.

EARPIECE DRIVER OUTPUT CONFIGURATIONS

The earpiece driver outputs HPOUT2P and HPOUT2N are driven by the HPOUT2MIX output mixer, which can take inputs from the mixer output PGAs MIXOUTLVOL and MIXOUTRVOL, or from the low power, differential Direct Voice path IN2LP/VRXN and IN2RP/VRXP. Fine volume control is available on the output mixer paths using MIXOUTLVOL and MIXOUTRVOL. A selectable -6dB attenuation is available on the HPOUT2MIX output, as described in Table 58 (refer to the "Output Signal Path" section).

The earpiece outputs are designed to operate in a BTL configuration, driving 50mW into a typical 16Ω ear speaker.

For suppression of pop noise there are two separate enables for the earpiece driver; HPOUT2_ENA enables the output stage and HPOUT2_IN_ENA enables the mixer and input stage. HPOUT2_IN_ENA should be enabled a minimum of 50µs before HPOUT2_ENA – see "Control Write Sequencer" section for an example power sequence.

LINE OUTPUT CONFIGURATIONS

The four line outputs LINEOUT1P, LINEOUT1N, LINEOUT2P and LINEOUT2N provide a highly flexible combination of differential and single-ended configurations, each driven by a dedicated output mixer. There is a selectable -6dB gain option in each mixer to avoid clipping when mixing more than one signal into a line output. Additional volume control is available at other locations within each of the supported signal paths. For more information about the line output mixing options, refer to the "Output Signal Path" section.

Typical applications for the line outputs (single-ended or differential) are:

- Handset or headset microphone output to external voice CODEC
- Stereo line output
- Output to external speaker driver(s) to support additional loudspeakers (e.g. stereo 2W with external driver plus on-chip mono 2W output)

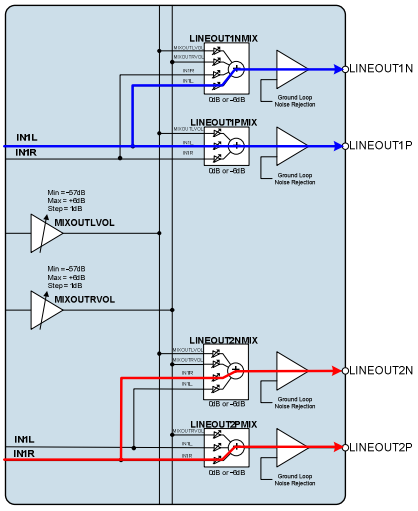
When single-ended mode is selected for either LINEOUT1 or LINEOUT2, a buffered VMID must be enabled as a reference for the outputs. This is enabled by setting the LINEOUT_VMID_BUF_ENA bit as defined in Table 63.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R56 (0038h) AntiPOP1	7	LINEOUT_VMID_BUF_ENA	0b	Enables VMID reference for line outputs in single-ended mode 0 = Disabled 1 = Enabled

Table 63 LINEOUT VMID Buffer for Single-Ended Operation

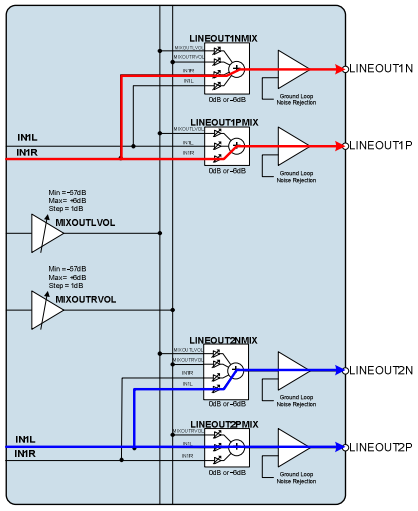
Some example line output configurations are listed and illustrated below.

- Differential line output from Mic/Line input on IN1L PGA
- Differential line output from Mic/Line input on IN1R PGA
- Stereo differential line output from output mixers MIXOUTL and MIXOUTR
- Stereo single-ended line output from output mixer to either LINEOUT1 or LINEOUT2
- Mono single-ended line output from output mixer



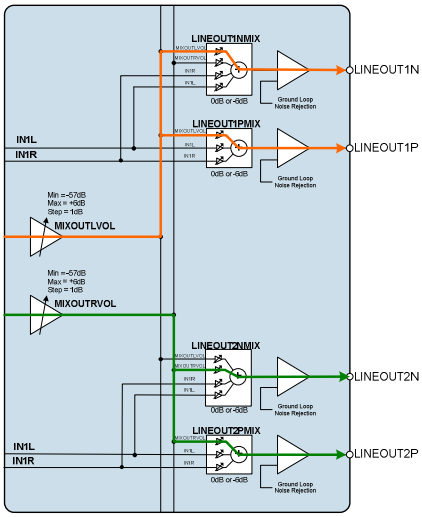
LINEOUT1N_MUTE=0, LINEOUT1P_MUTE=0
LINEOUT2N_MUTE=0, LINEOUT2P_MUTE=0
LINEOUT1_MODE=0
LINEOUT2_MODE=0
IN1L_TO_LINEOUT1P=1
IN1R_TO_LINEOUT2P=1

Figure 31 Differential Line Out from input PGA IN1L (to LINEOUT1) and IN1R (to LINEOUT2)



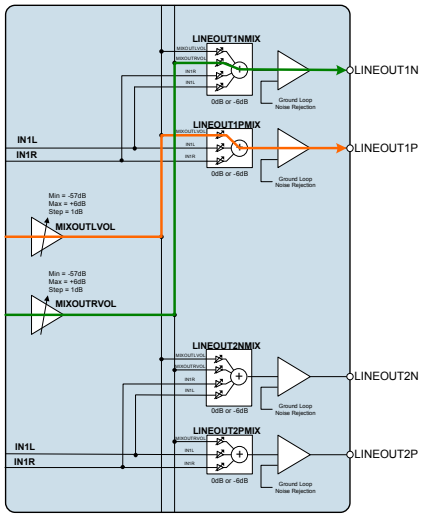
LINEOUT1N_MUTE=0, LINEOUT1P_MUTE=0
LINEOUT2N_MUTE=0, LINEOUT2P_MUTE=0
LINEOUT1_MODE=0
LINEOUT2_MODE=0
IN1R_TO_LINEOUT1P=1
IN1L_TO_LINEOUT2P=1

Figure 32 Differential Line Out from input PGA IN1R (to LINEOUT1) and IN1L (to LINEOUT2)



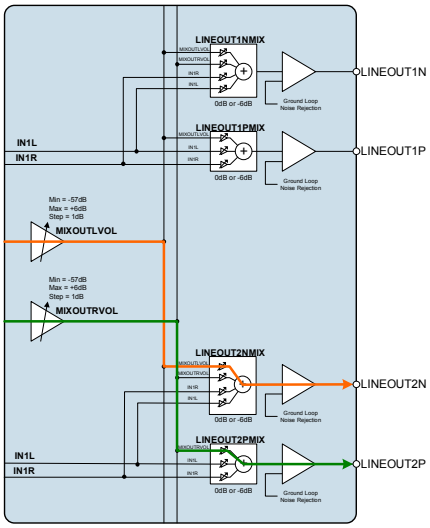
LINEOUT1N_MUTE=0, LINEOUT1P_MUTE=0
LINEOUT2N_MUTE=0, LINEOUT2P_MUTE=0
LINEOUT1_MODE=0
LINEOUT2_MODE=0
MIXOUTL_TO_LINEOUT1P=1
MIXOUTR_TO_LINEOUT2P=1

Figure 33 Stereo Differential Line Out from MIXOUTL and MIXOUTR



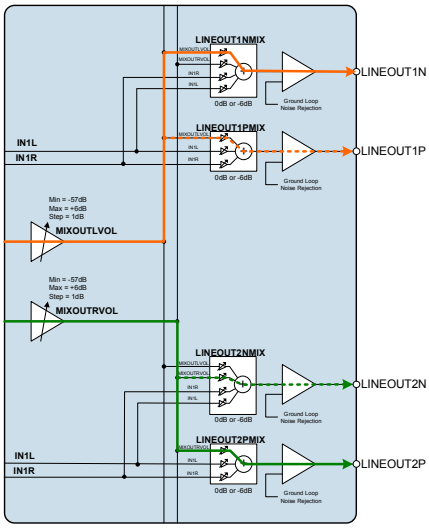
LINEOUT1N_MUTE=0, LINEOUT1P_MUTE=0
LINEOUT2N_MUTE=0, LINEOUT2P_MUTE=0
LINEOUT1_MODE=1
MIXOUTL_TO_LINEOUT1P=1
MIXOUTR_TO_LINEOUT1N=1
LINEOUT_VMID_BUF_ENA=1

Figure 34 Stereo Single-Ended Line Out from MIXOUTL and MIXOUTR to LINEOUT1



LINEOUT1N_MUTE=0, LINEOUT1P_MUTE=0
LINEOUT2N_MUTE=0, LINEOUT2P_MUTE=0
LINEOUT1_MODE=1
MIXOUTL_TO_LINEOUT2N=1
MIXOUTR_TO_LINEOUT2P=1
LINEOUT_VMID_BUF_ENA=1

Figure 35 Stereo Single-Ended Line Out from MIXOUTL and MIXOUTR to LINEOUT2



LINEOUT1N_MUTE=0, LINEOUT1P_MUTE=0
LINEOUT2N_MUTE=0, LINEOUT2P_MUTE=0
LINEOUT1_MODE=1
LINEOUT2_MODE=1
MIXOUTL_TO_LINEOUT1N=1 and/or
MIXOUTL_TO_LINEOUT1P=1
MIXOUTR_TO_LINEOUT2N=1 and/or
MIXOUTR_TO_LINEOUT2P=1
LINEOUT_VMID_BUF_ENA=1

Figure 36 Mono Line Out to LINEOUT1N, LINEOUT1P, LINEOUT2N, LINEOUT2P

The line outputs incorporate a common mode, or ground loop, feedback path which provides rejection of system-related ground noise. The return path, via LINEOUTFB, is enabled separately for LINEOUT1 and LINEOUT2 using the LINEOUT1_FB and LINEOUT2_FB bits as defined in Table 64.

Ground loop feedback is a benefit to single-ended line outputs only; it is not applicable to differential outputs, which already inherently offer common mode noise rejection.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R55 (0037h) Additional Control	7	LINEOUT1_FB	0	Enable ground loop noise feedback on LINEOUT1 0 = Disabled 1 = Enabled
	6	LINEOUT2_FB	0	Enable ground loop noise feedback on LINEOUT2 0 = Disabled 1 = Enabled

Table 64 Line Output Ground Loop Feedback Enable

LDO REGULATORS

The WM8994 provides two integrated Low Drop-Out Regulators (LDOs). These are provided in order to generate the appropriate power supplies for internal circuits, simplifying and reducing the requirements for external supplies and associated components. A reference circuit powered by AVDD2 ensures the accuracy of the LDO regulator voltage settings.

LDO1 is intended for generating AVDD1 - the primary analogue power domain of the WM8994. LDO1 is enabled when a logic '1' is applied to the LDO1ENA pin. The logic level is determined with respect to the DBVDD voltage domain.

When LDO1 is enabled, the output voltage is controlled by the LDO1_VSEL register field. When LDO1 is disabled, the output can be left floating or can be actively discharged, depending on the LDO1_DISCH control bit.

LDO2 is intended for generating the DCVDD power domain which supplies the digital core functions on the WM8994. LDO2 is enabled when a logic '1' is applied to the LDO2ENA pin. The logic level is determined with respect to the DBVDD voltage domain.

When LDO2 is enabled, the output voltage is controlled by the LDO2_VSEL register field. When LDO2 is disabled, the output can be left floating or can be actively discharged, depending on the LDO2_DISCH control bit.

Decoupling capacitors should be connected to the voltage reference pin, VREFC, and also to the LDO outputs, AVDD1 and DCVDD. See "Applications Information" for further details.

The LDO Regulator connections and controls are illustrated in Figure 37. The register controls are defined in Table 65.

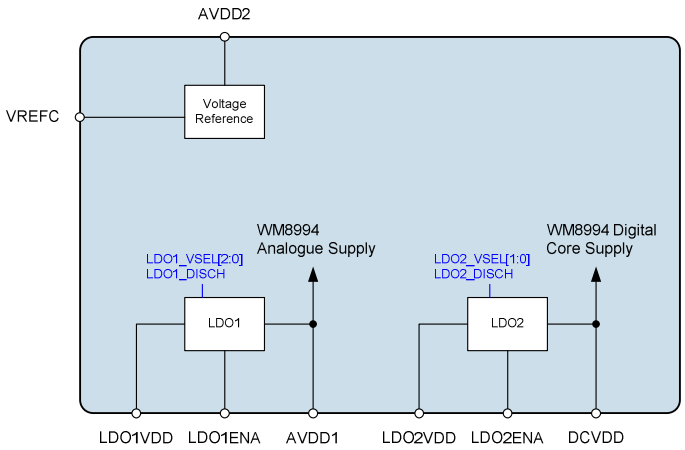


Figure 37 LDO Regulators

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R59 (003Bh) LDO 1	3:1	LDO1_VSEL [2:0]	110	LDO1 Output Voltage Select 2.4V to 3.1V in 100mV steps 000 = 2.4V 001 = 2.5V 010 = 2.6V 011 = 2.7V 100 = 2.8V 101 = 2.9V 110 = 3.0V 111 = 3.1V
	0	LDO1_DISCH	1	LDO1 Discharge Select 0 = LDO1 floating when disabled 1 = LDO1 discharged when disabled
R60 (003Ch) LDO 2	2:1	LDO2_VSEL [1:0]	01	LDO2 Output Voltage Select 0.9V to 1.2V in 100mV steps 00 = 0.9V 01 = 1.0V 10 = 1.1V 11 = 1.2V
	0	LDO2_DISCH	1	LDO2 Discharge Select 0 = LDO2 floating when disabled 1 = LDO2 discharged when disabled

Table 65 LDO Regulator Control

GENERAL PURPOSE INPUT/OUTPUT

The WM8994 provides a number of GPIO functions to enable interfacing and detection of external hardware and to provide logic outputs to other devices. The input functions can be polled directly or can be used to generate an Interrupt (IRQ) event. The GPIO and Interrupt circuits support the following functions:

- Button detect (GPIO input)
- Accessory detection (MICBIAS current detection)
- Clock output (SYSCLK divided by OPCLK_DIV)
- Frequency Locked Loop (FLL) Lock status detect
- Sample Rate Conversion (SRC) Lock status detect
- Dynamic Range Control (DRC) Signal activity detect
- Over-Temperature detection
- Digital Core FIFO error status detection
- Control Write Sequencer status detection
- Logic '1' and logic '0' output
- Interrupt (IRQ) status output

GPIO CONTROL

For each GPIO, the selected function is determined by the GPn_FN field, where n identifies the GPIO pin (1 to 11). The pin direction, set by GPn_DIR, must be set according to function selected by GPn_SEL, with the exception of GPIO2 which is always an input.

The alternate audio interfaces AIF2 and AIF3 are both supported using GPIO pins; the applicable pin functions are selected by setting the corresponding GPn_FN register to 00h. See Table 69 for the definition of which AIF function is available on each GPIO pin.

Note that the GPIO2 pin supports functions MCLK2 and Button Detect / Logic Level Input only.

When a pin is configured as a GPIO input (GPn_DIR = 1), the logic level at the pin can be read from the respective GPn_LVL bit. The polarity of the GPIO input can be inverted using the GPn_POL bit; when GPn_POL = 1, then the GPn_LVL will read the opposite logic level to the external input.

A de-bounce circuit can be enabled on any GPIO input, to avoid false event triggers. This is enabled on each pin by setting the respective GPn_DB bit. Note that TOCLK must be enabled when this input de-bouncing is required.

When a pin is configured as a Logic Level output (GPn_DIR = 0, GPn_FN = 01h), its level can be set to logic 0 or logic 1 using the GPn_LVL field. In this case, the respective GPn_POL bit has no effect.

A GPIO output can be either CMOS driven or Open Drain. This is selected on each pin using the respective GPn_OP_CFG bit.

Internal pull-up and pull-down resistors may be enabled using the GPn_PU and GPn_PD fields; this allows greater flexibility to interface with different signals from other devices.

Each of the GPIO pins is an input to the Interrupt control circuit and can be used to trigger an Interrupt event. An interrupt event is triggered on the rising and falling edge of the GPIO input. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See "Interrupts" for more details of the Interrupt event handling.

The register fields that control the GPIO pins are described in Table 68, Table 67 and .

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1792 (0700h) GPIO1	15	GP1_DIR	1	GPIO1 Pin Direction 0 = Output 1 = Input
	14	GP1_PU	0	GPIO1 Pull-Up Enable 0 = Disabled 1 = Enabled
	13	GP1_PD	1	GPIO1 Pull-Down Enable 0 = Disabled 1 = Enabled
	10	GP1_POL	0	GPIO1 Polarity Select 0 = Non-inverted (Active High) 1 = Inverted (Active Low)
	9	GP1_OP_CFG	0	GPIO1 Output Configuration 0 = CMOS 1 = Open Drain
	8	GP1_DB	1	GPIO1 Input De-bounce 0 = Disabled 1 = Enabled
	6	GP1_LVL	0	GPIO1 level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP1_POL is set, and GP1_DIR = 1 (GPIO input), the GP1_LVL register contains the opposite logic level to the external pin.
	4:0	GP1_FN [4:0]	0000	GPIO1 Pin Function (see Table 69 for details)

Table 66 GPIO1 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1793 (0701h) GPIO2	14	GP2_PU	0	GPIO2 Pull-Up Enable 0 = Disabled 1 = Enabled
	13	GP2_PD	1	GPIO2 Pull-Down Enable 0 = Disabled 1 = Enabled
	10	GP2_POL	0	GPIO2 Polarity Select 0 = Non-inverted (Active High) 1 = Inverted (Active Low)
	8	GP2_DB	1	GPIO2 Input De-bounce 0 = Disabled 1 = Enabled
	6	GP2_LVL	0	GPIO2 level. Read from this bit to read GPIO input level. When GP2_POL is set, and GP2_DIR = 1 (GPIO input), the GP2_LVL register contains the opposite logic level to the external pin.
	4:0	GP2_FN [4:0]	0001	GPIO2 Pin Function (see Table 69 for details)

Table 67 GPIO2 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1794 (0701h) GPIO3 to R1802 (070Ah) GPIO11	15	GPn_DIR	1	GPIOn Pin Direction 0 = Output 1 = Input
	14	GPn_PU	0	GPIOn Pull-Up Enable 0 = Disabled 1 = Enabled
	13	GPn_PD	1	GPIOn Pull-Down Enable 0 = Disabled 1 = Enabled
	10	GPn_POL	0	GPIOn Polarity Select 0 = Non-inverted (Active High) 1 = Inverted (Active Low)
	9	GPn_OP_CFG	0	GPIOn Output Configuration 0 = CMOS 1 = Open Drain
	8	GPn_DB	1	GPIOn Input De-bounce 0 = Disabled 1 = Enabled
	6	GPn_LVL	0	GPIOn level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GPn_POL is set, and GPn_DIR = 1 (GPIO input), the GPn_LVL register contains the opposite logic level to the external pin.
	4:0	GPn_FN [4:0]	0001	GPIOn Pin Function (see Table 69 for details)
Note: *n* is a number between 3 and 11 that identifies the individual GPIO.				

Table 68 GPIO3 to GPIO11 Control

GPIO FUNCTION SELECT

The available GPIO functions are described in Table 69. The function of each GPIO is set using the GPn_FN register, where n identifies the GPIO pin (1 to 11). Note that the respective GPn_DIR must also be set according to whether the function is an input or output.

Note that GPIO2 supports functions MCLK2 and Button Detect / Logic Level Input only.

GPn_FN	DESCRIPTION	COMMENTS
00h	GPIO1 - ADCLRCLK1 GPIO2 - MCLK2 GPIO3 - BCLK2 GPIO4 - LRCLK2 GPIO5 - DACDAT2 GPIO6 - ADCLRCLK2 GPIO7 - ADCDAT2 GPIO8 - DACDAT3 GPIO9 - ADCDAT3 GPIO10 - LRCLK3 GPIO11 - BCLK3	Alternate Audio Interface connections.
01h	Button detect input / Logic level output	GPn_DIR = 0: GPIO pin logic level is set by GPn_LVL. GPn_DIR = 1: Button detect or logic level input. Note that GPIO2 can only be configured as an input.
02h	SDOUT	SPI Control Interface data output

GPn_FN	DESCRIPTION	COMMENTS
03h	IRQ	Interrupt (IRQ) output 0 = IRQ not asserted 1 = IRQ asserted Polarity can be inverted by setting IRQ_POL = 1
04h	Temperature flag output	Indicates Temperature Sensor status 0 = Normal 1 = Over-temperature Polarity can be inverted by setting TEMP_SHUT_POL = 1
05h	MICBIAS1 Current Detect	Indicates MICBIAS1 Current Detection status 0 = Current Detect threshold not exceeded 1 = Current Detect threshold exceeded Polarity can be inverted by setting MIC1_DET_POL = 1
06h	MICBIAS1 Short Circuit Detect	Indicates MICBIAS1 Short Circuit Detection status 0 = Short Circuit threshold not exceeded 1 = Short Circuit threshold exceeded Polarity can be inverted by setting MIC1_SHRT_POL = 1
07h	MICBIAS2 Current Detect	Indicates MICBIAS2 Current Detection status 0 = Current Detect threshold not exceeded 1 = Current Detect threshold exceeded Polarity can be inverted by setting MIC2_DET_POL = 1
08h	MICBIAS2 Short Circuit Detect	Indicates MICBIAS2 Short Circuit Detection status 0 = Short Circuit threshold not exceeded 1 = Short Circuit threshold exceeded Polarity can be inverted by setting MIC2_SHRT_POL = 1
09h	FLL1 Lock	Indicates FLL1 Lock status 0 = Not locked 1 = Locked Polarity can be inverted by setting FLL1_LOCK_POL = 1
0Ah	FLL2 Lock	Indicates FLL2 Lock status 0 = Not locked 1 = Locked Polarity can be inverted by setting FLL2_LOCK_POL = 1
0Bh	SRC1 Lock	Indicates SRC1 Lock status 0 = Not locked 1 = Locked Polarity can be inverted by setting SRC1_LOCK_POL = 1
0Ch	SRC2 Lock	Indicates SRC2 Lock status 0 = Not locked 1 = Locked Polarity can be inverted by setting SRC2_LOCK_POL = 1
0Dh	DRC1 Signal Activity	Indicates DRC1 Activity Detect status 0 = Normal 1 = Activity Detected Polarity can be inverted by setting DRC1_ACTDET_POL = 1
0Eh	DRC2 Signal Activity	Indicates DRC2 Activity Detect status 0 = Normal 1 = Activity Detected Polarity can be inverted by setting DRC2_ACTDET_POL = 1
0Fh	DRC3 Signal Activity	Indicates DRC3 Activity Detect status 0 = Normal 1 = Activity Detected Polarity can be inverted by setting DRC3_ACTDET_POL = 1

GPn_FN	DESCRIPTION	COMMENTS
10h	Write Sequencer Status	Indicates Write Sequencer status 0 = Write Sequencer Idle 1 = Write Sequence Busy Polarity can be inverted by setting WSEQ_DONE_POL = 1
11h	FIFO Error	Indicates a Digital Core FIFO Error condition 0 = Normal 1 = FIFO Error
12h	Clock Output OPCLK	GPIO Clock derived from SYSCLK
13h to 1Fh	Reserved	

Table 69 GPIO Function Select

BUTTON DETECT (GPIO INPUT)

Button detect functionality can be selected on any GPIO pin by setting the respective GPIO registers as described in "GPIO Control". The same functionality can be used to support a Jack Detect input function.

It is recommended to enable the GPIO input de-bounce feature when using GPIOs as button input or Jack Detect input.

The GPn_LVL fields may be read to determine the logic levels on a GPIO input, after the selectable de-bounce and polarity inversion controls.

The de-bounced GPIO signals are also inputs to the Interrupt control circuit. An interrupt event is triggered on the rising and falling edge of the GPIO input. The associated interrupt bits are latched once set; it can be polled at any time or used to control the IRQ signal. See "Interrupts" for more details of the Interrupt event handling.

ACCESSORY DETECTION (MICBIAS CURRENT DETECT)

Current detection is provided on each of the microphone bias sources MICBIAS1 and MICBIAS2. These can be configured to detect when an external accessory (such as a microphone) has been connected. The output voltage of each of the microphone bias sources is selectable. Two current detection threshold levels can be set; these thresholds are applicable to both microphone bias sources.

The logic signals from the current detect circuits may be output directly on any GPIO pin by setting the respective GPIO registers as described in "GPIO Control". De-bounce and polarity inversion can be applied to these signals using the register bits described in Table 70.

The current detection circuits are inputs to the Interrupt control circuit, after the selectable de-bounce. An interrupt event is triggered on the rising and falling edges of the current detect signals. The associated interrupt bits are latched once set; they can be polled at any time or used to control the IRQ signal. See "Interrupts" for more details of the Interrupt event handling.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (0001h) Power Management (1)	5	MICB2_ENA	0	Microphone Bias 2 Enable 0 = OFF (high impedance output) 1 = ON
	4	MICB1_ENA	0	Microphone Bias 2 Enable 0 = OFF (high impedance output) 1 = ON
R58 (003Ah) MICBIAS	7:6	MICD_SCTHR [1:0]	00	MICBIAS Short Circuit Current threshold 00 = 300uA 01 = 600uA 10 = 1200uA 11 = 2400uA These values are for AVDD1=3.0V and scale proportionally with AVDD1.

	5:4	MICD_THR [1:0]	00	MICBIAS Current Detect threshold 00 = 150uA 01 = 300uA 10 = 600uA 11 = 1200uA These values are for AVDD1=3.0V and scale proportionally with AVDD1.
	2	MICD_ENA	0	MICBIAS Current Detect / Short Circuit Threshold enable 0 = disabled 1 = enabled
	1	MICB2_LVL	0	Microphone Bias 2 Voltage Control 0 = 0.9 * AVDD1 1 = 0.65 * AVDD1
	0	MICB1_LVL	0	Microphone Bias 1 Voltage Control 0 = 0.9 * AVDD1 1 = 0.65 * AVDD1
R1864 (0748h) IRQ Debounce	4	MIC2_SHRT _DB	1	MICBIAS2 Short Circuit de-bounce 0 = disabled 1 = enabled
	3	MIC2_DET_ DB	1	MICBIAS2 Current Detect de-bounce 0 = disabled 1 = enabled
	2	MIC1_SHRT _DB	1	MICBIAS1 Short Circuit de-bounce 0 = disabled 1 = enabled
	1	MIC1_DET_ DB	1	MICBIAS1 Current Detect de-bounce 0 = disabled 1 = enabled
R1865 (0749h) IRQ Polarity	4	MIC2_SHRT _POL	0	MICBIAS2 Short Circuit polarity 0 = active high (asserted when MICD_SCTHR is exceeded) 1 = active low
	3	MIC2_DET_ POL	0	MICBIAS2 Current Detect polarity 0 = active high (asserted when MICD_THR is exceeded) 1 = active low
	2	MIC1_SHRT _POL	0	MICBIAS1 Short Circuit polarity 0 = active high (asserted when MICD_SCTHR is exceeded) 1 = active low
	1	MIC1_DET_ POL	0	MICBIAS1 Current Detect polarity 0 = active high (asserted when MICD_THR is exceeded) 1 = active low

Table 70 MICBIAS Enable and GPIO/Interrupt Control

CLOCK OUTPUT

A clock output (OPCLK) derived from SYSCLK may be output on any GPIO pin by setting the respective GPIO registers as described in “GPIO Control”. This clock is enabled by register bit OPCLK_ENA, and its frequency is controlled by OPCLK_DIV.

See “Clocking and Sample Rates” for more details of the System Clock (SYSCLK).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (0002h) Power Management (2)	11	OPCLK_ENA	0b	GPIO Clock Output (OPCLK) Enable 0 = Disabled 1 = Enabled
R521 (0209h) Clocking 1	2:0	OPCLK_DIV	000	GPIO Output Clock (OPCLK) Divider 000 = SYSCLK 001 = SYSCLK / 2 010 = SYSCLK / 3 011 = SYSCLK / 4 100 = SYSCLK / 6 101 = SYSCLK / 8 110 = SYSCLK / 12 111 = SYSCLK / 16

Table 71 OPCLK Control

FREQUENCY LOCKED LOOP (FLL) LOCK STATUS DETECT

The WM8994 maintains a flag indicating the lock status of each of FLLs, which may be used to control other events if required. See “Clocking and Sample Rates” for more details of the FLL.

The FLL Lock signals may be output directly on any GPIO pin by setting the respective GPIO registers as described in “GPIO Control”. Polarity inversion can be applied to these signals using the register bits described in Table 72.

The FLL Lock signals are inputs to the Interrupt control circuit. An interrupt event is triggered on the rising and falling edges of the FLL Lock signals. The associated interrupt bits are latched once set; they can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1865 (0749h) IRQ Polarity	6	FLL2_LOCK_POL	0	FLL2 Lock polarity 0 = active high (asserted when FLL2 locked) 1 = active low
	5	FLL1_LOCK_POL	0	FLL1 Lock polarity 0 = active high (asserted when FLL1 locked) 1 = active low

Table 72 FLL Lock GPIO/Interrupt Control

SAMPLE RATE CONVERTER (SRC) LOCK STATUS DETECT

The WM8994 maintains a flag indicating the lock status of each of Sample Rate Converters, which may be used to control other events if required. See "Sample Rate Conversion" for more details of the Sample Rate Converters.

The SRC Lock signals may be output directly on any GPIO pin by setting the respective GPIO registers as described in "GPIO Control". Polarity inversion can be applied to these signals using the register bits described in Table 73.

The SRC Lock signals are inputs to the Interrupt control circuit, after the selectable de-bounce. An interrupt event is triggered on the rising and falling edges of the SRC Lock signals. The associated interrupt bits are latched once set; they can be polled at any time or used to control the IRQ signal. See "Interrupts" for more details of the Interrupt event handling.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1865 (0749h) IRQ Polarity	8	SRC2_LOCK_POL	0	SRC2 Lock polarity 0 = active high (asserted when SRC2 locked) 1 = active low
	7	SRC1_LOCK_POL	0	SRC1 Lock polarity 0 = active high (asserted when SRC1 locked) 1 = active low

Table 73 SRC Lock GPIO/Interrupt Control

DYNAMIC RANGE CONTROL (DRC) SIGNAL ACTIVITY DETECT

Signal activity detection is provided on each of the Dynamic Range Controllers (DRCs). These may be configured to indicate when a signal is present on the respective signal path. The activity status signals may be used to control other events if required. See "Digital Core Architecture" for more details of the DRCs and the available digital signal paths.

When a DRC is enabled, as described in "Dynamic Range Control (DRC)", then signal activity detection can be enabled by setting the respective *[DRC]*_SIG_DET register bit. The applicable threshold can be defined either as a Peak level (Crest Factor) or an RMS level, depending on the *[DRC]*_SIG_DET_MODE register bit. When Peak level is selected, the threshold is determined by *[DRC]*_SIG_DET_PK, which defines the applicable Crest Factor (Peak to RMS ratio) threshold. If RMS level is selected, then the threshold is set using *[DRC]*_SIG_DET_RMS. These register fields are set independently for each of the three Dynamic Range Controllers, as described in Table 74.

The DRC Activity Detect signals may be output directly on any GPIO pin by setting the respective GPIO registers as described in "GPIO Control". Polarity inversion can be applied to these signals using the register bits described in Table 74.

The DRC Activity Detect signals are inputs to the Interrupt control circuit. An interrupt event is triggered on the rising and falling edges of the DRC Activity Detect signals. The associated interrupt bits are latched once set; they can be polled at any time or used to control the IRQ signal. See "Interrupts" for more details of the Interrupt event handling.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1088 (0440h) AIF1 DRC1 (1)	15:11	AIF1DRC1_SIG_DET_RMS [4:0]	00000	AIF1 DRC1 Signal Detect RMS Threshold. This is the RMS signal level for signal detect to be indicated when AIF1DRC1_SIG_DET_MODE=0. 00000 = -30dB 00001 = -31.5dB …. (1.5dB steps) 11110 = -75dB 11111 = -76.5dB
	10:9	AIF1DRC1_SIG_DET_PK [1:0]	00	AIF1 DRC1 Signal Detect Peak Threshold. This is the Peak/RMS ratio, or Crest Factor, level for signal detect to be indicated when AIF1DRC1_SIG_DET_MODE=1. 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB
	7	AIF1DRC1_SIG_DET_MODE	0	AIF1 DRC1 Signal Detect Mode 0 = RMS threshold mode 1 = Peak threshold mode
	6	AIF1DRC1_SIG_DET	0	AIF1 DRC1 Signal Detect Enable 0 = Disabled 1 = Enabled
R1104 (0450h) AIF1 DRC2 (1)	15:11	AIF1DRC2_SIG_DET_RMS [4:0]	00000	AIF1 DRC2 Signal Detect RMS Threshold. This is the RMS signal level for signal detect to be indicated when AIF1DRC2_SIG_DET_MODE=0. 00000 = -30dB 00001 = -31.5dB …. (1.5dB steps) 11110 = -75dB 11111 = -76.5dB
	10:9	AIF1DRC2_SIG_DET_PK [1:0]	00	AIF1 DRC2 Signal Detect Peak Threshold. This is the Peak/RMS ratio, or Crest Factor, level for signal detect to be indicated when AIF1DRC2_SIG_DET_MODE=1. 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB
	7	AIF1DRC2_SIG_DET_MODE	0	AIF1 DRC2 Signal Detect Mode 0 = RMS threshold mode 1 = Peak threshold mode
	6	AIF1DRC2_SIG_DET	0	AIF1 DRC2 Signal Detect Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1344 (0550h) AIF2 DRC (1)	15:11	AIF2DRC_SIG_DET_RMS [4:0]	00000	AIF2 DRC Signal Detect RMS Threshold. This is the RMS signal level for signal detect to be indicated when AIF2DRC_SIG_DET_MODE=0. 00000 = -30dB 00001 = -31.5dB …. (1.5dB steps) 11110 = -75dB 11111 = -76.5dB
	10:9	AIF2DRC_SIG_DET_PK [1:0]	00	AIF2 DRC Signal Detect Peak Threshold. This is the Peak/RMS ratio, or Crest Factor, level for signal detect to be indicated when AIF2DRC_SIG_DET_MODE=1. 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB
	7	AIF2DRC_SIG_DET_MODE	0	AIF2 DRC Signal Detect Mode 0 = RMS threshold mode 1 = Peak threshold mode
	6	AIF2DRC_SIG_DET	0	AIF2 DRC Signal Detect Enable 0 = Disabled 1 = Enabled
R1865 (0749h) IRQ Polarity	11	DRC3_ACTDET_POL	0	DRC3 (AIF2) Activity Detect polarity 0 = active high (asserted when DRC3 activity is detected) 1 = active low
	10	DRC2_ACTDET_POL	0	DRC2 (AIF1) Activity Detect polarity 0 = active high (asserted when DRC2 activity is detected) 1 = active low
	9	DRC1_ACTDET_POL	0	DRC1 (AIF1) Activity Detect polarity 0 = active high (asserted when DRC1 activity is detected) 1 = active low

Table 74 DRC Signal Activity Detect GPIO/Interrupt Control

OVER-TEMPERATURE DETECTION

The WM8994 incorporates a temperature sensor which detects when the device temperature is within normal limits or if the device is approaching a hazardous temperature condition.

The Temperature status may be output directly on any GPIO pin by setting the respective GPIO registers as described in “GPIO Control”. De-bounce and polarity inversion can be applied to this signal using the register bits described in Table 75.

The Temperature status is an input to the Interrupt control circuit, after the selectable de-bounce. An interrupt event is triggered on the rising and falling edges of the temperature status flag. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

Note that the temperature sensor can be configured to automatically disable the audio outputs of the WM8994 (see “Thermal Shutdown”). In some applications, it may be preferable to manage the temperature sensor event through GPIO or Interrupt functions, allowing a host processor to implement a controlled system response to an over-temperature condition.

The temperature sensor must be enabled by setting the TSHUT_ENA register bit. When the TSHUT_OPDIS is also set, then a device over-temperature condition will cause the speaker outputs (SPKOUTL and SPKOUTR) of the WM8994 to be disabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (0002h) Power Management (2)	14	TSHUT_ENA	1	Thermal sensor enable 0 = disabled 1 = enabled
	13	TSHUT_OPDIS	1	Thermal shutdown control (Causes audio outputs to be disabled if an overtemperature occurs. The thermal sensor must also be enabled.) 0 = disabled 1 = enabled
R1864 (0748h) IRQ Debounce	0	TEMP_SHUT_DB	0	Thermal shutdown de-bounce 0 = disabled 1 = enabled
R1865 (0749h) IRQ Polarity	0	TEMP_SHUT_POL	0	Thermal shutdown interrupt polarity 0 = active high (asserted when temperature threshold is exceeded) 1 = active low

Table 75 Temperature Sensor Enable and GPIO/Interrupt Control

DIGITAL CORE FIFO ERROR STATUS DETECTION

The WM8994 monitors the DSP Core for error conditions which may occur if excessive digital processing demands are commanded and the processor cannot execute all the selected functions on the digital audio in real time. Under these conditions, the digital audio may become corrupted and the selected functions such as EQ, 3D Stereo Expansion, Dynamic Range Control may be compromised.

The Digital Core FIFO Error function is provided in order that the digital processing demands of different application configurations can be verified during product development.

The FIFO Error signal may be output directly on any GPIO pin by setting the respective GPIO registers as described in “GPIO Control”. Polarity inversion can be applied to this signal using the register bits described in Table 76.

The FIFO Error signal is an input to the Interrupt control circuit. An interrupt event is triggered on the rising and falling edges of the FIFO Error signal. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1865 (0749h) IRQ Polarity	12	FIFOS_ERR_POL	0	FIFO Error polarity 0 = active high (asserted under FIFO Error condition) 1 = active low

Table 76 Digital Core FIFO Error Status GPIO/Interrupt Control

CONTROL WRITE SEQUENCER STATUS DETECTION

The WM8994 Control Write Sequencer (WSEQ) can be used to execute a sequence of register write operations in response to a simple trigger event. When the Control Write Sequencer is executing a sequence, normal access to the register map via the Control Interface is restricted. See "Control Write Sequencer" for details of the Control Write Sequencer.

The WM8994 generates a signal indicating the status of the Control Write Sequencer, in order to signal to the host processor whether the Control Interface functionality is restricted due to an ongoing Control Sequence. The WSEQ_DONE flag indicates that the sequencer has completed the commanded sequence.

The Write Sequencer status may be output directly on any GPIO pin by setting the respective GPIO registers as described in "GPIO Control". Polarity inversion can be applied to this signal using the register bit described in Table 77.

The Write Sequencer status is an input to the Interrupt control circuit. An interrupt event is triggered on the falling edge only of the Write Sequencer status flag (ie. on completion of a Control Sequence). The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See "Interrupts" for more details of the Interrupt event handling.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1865 (0749h) IRQ Polarity	13	WSEQ_DONE_POL	0	Write Sequencer polarity 0 = active high (asserted when Control Sequence is Busy) 1 = active low

Table 77 Control Write Sequencer GPIO/Interrupt Control

LOGIC '1' AND LOGIC '0' OUTPUT

The WM8994 can be programmed to drive a logic high or logic low level on any GPIO pin by selecting the "GPIO Output" function as described in "GPIO Control". The output logic level is selected using the respective GPn_LVL bit.

Note that the polarity of the GPIO output is not affected by the GPn_POL registers.

INTERRUPT (IRQ) STATUS OUTPUT

The WM8994 has an Interrupt Controller which can be used to indicate when any selected Interrupt events occur. An interrupt can be generated by any of the events described throughout the GPIO function definition above. Individual interrupts may be masked in order to configure the Interrupt as required. See "Interrupts" for further details.

The Interrupt (IRQ) status may be output directly on any GPIO pin by setting the respective GPIO registers as described in "GPIO Control". Polarity inversion can be applied to this signal using the register bit described in Table 78.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1856 (0740h) Interrupt Control	0	IRQ_POL	0	Interrupt (IRQ) polarity 0 = active high 1 = active low

Table 78 GPIO/Interrupt (IRQ) Control

INTERRUPTS

The Interrupt Controller has multiple inputs. These include the GPIO input pins, the MICBIAS current detection circuits, FLL Lock circuits, SRC Lock circuit, Microphone activity detection, Over-temperature indication, Digital FIFO error detection and the Write Sequencer status flag. Any combination of these inputs can be used to trigger an Interrupt (IRQ) event.

There is an Interrupt Status field associated with each of the IRQ inputs. These fields are asserted whenever a logic edge (rising or falling) is detected on the respective input. The Interrupt Status fields are held in two registers, as described in Table 79. The status of the IRQ inputs can be read at any time from these register, or else in response to the Interrupt (IRQ) output being signalled via a GPIO pin.

Individual mask bits can select or deselect different functions from the Interrupt controller. These are listed within the Interrupt Status Mask registers, as described in Table 79. Note that the status fields remain valid, even when masked, but the masked bits will not cause the Interrupt (IRQ) output to be asserted.

The Interrupt (IRQ) output represents the logical 'OR' of all the unmasked IRQ inputs. The bits within the Interrupt Status registers are latching fields and, once they are set, they are not reset until a '1' is written to the respective register bit in the Interrupt Status register(s). The Interrupt (IRQ) output is not reset until each of the unmasked IRQ inputs has been reset.

The Interrupt (IRQ) flag may be output on a GPIO pin - see "General Purpose Input/Output". The polarity is configurable using the IRQ_POL register bit, as described in Table 78.

The Interrupt Controller register fields are described in Table 79.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1840 (0730h) Interrupt Status 1	10	GP11_EINT	0	GPIO11 Interrupt status 0 = GPIO11 Interrupt not set 1 = GPIO11 Interrupt set Note: Cleared when a '1' is written.
	9	GP10_EINT	0	GPIO10 Interrupt status 0 = GPIO10 Interrupt not set 1 = GPIO10 Interrupt set Note: Cleared when a '1' is written.
	8	GP9_EINT	0	GPIO9 Interrupt status 0 = GPIO9 Interrupt not set 1 = GPIO9 Interrupt set Note: Cleared when a '1' is written.
	7	GP8_EINT	0	GPIO8 Interrupt status 0 = GPIO8 Interrupt not set 1 = GPIO8 Interrupt set Note: Cleared when a '1' is written.
	6	GP7_EINT	0	GPIO7 Interrupt status 0 = GPIO7 Interrupt not set 1 = GPIO7 Interrupt set Note: Cleared when a '1' is written.
	5	GP6_EINT	0	GPIO6 Interrupt status 0 = GPIO6 Interrupt not set 1 = GPIO6 Interrupt set Note: Cleared when a '1' is written.
	4	GP5_EINT	0	GPIO5 Interrupt status 0 = GPIO5 Interrupt not set 1 = GPIO5 Interrupt set Note: Cleared when a '1' is written.
	3	GP4_EINT	0	GPIO4 Interrupt status 0 = GPIO4 Interrupt not set 1 = GPIO4 Interrupt set Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	2	GP3_EINT	0	GPIO3 Interrupt status 0 = GPIO3 Interrupt not set 1 = GPIO3 Interrupt set Note: Cleared when a '1' is written.
	1	GP2_EINT	0	GPIO2 Interrupt status 0 = GPIO2 Interrupt not set 1 = GPIO2 Interrupt set Note: Cleared when a '1' is written.
	0	GP1_EINT	0	GPIO1 Interrupt status 0 = GPIO1 Interrupt not set 1 = GPIO1 Interrupt set Note: Cleared when a '1' is written.
R1841 (0731h) Interrupt Status 2	13	WSEQ_DONE_EINT	0	Write Sequencer IRQ status 0 = Write Sequencer IRQ not set 1 = Write Sequencer IRQ set Note: Cleared when a '1' is written.
	13	FIFOS_ERR_EINT	0	Digital Core FIFO Error IRQ status 0 = FIFO Error IRQ not set 1 = FIFO Error IRQ set Note: Cleared when a '1' is written.
	11	DRC3_ACTDET_EINT	0	DRC3 Activity Detect IRQ status 0 = DRC3 Activity Detect IRQ not set 1 = DRC3 Activity Detect IRQ set Note: Cleared when a '1' is written.
	10	DRC2_ACTDET_EINT	0	DRC2 Activity Detect IRQ status 0 = DRC2 Activity Detect IRQ not set 1 = DRC2 Activity Detect IRQ set Note: Cleared when a '1' is written.
	9	DRC1_ACTDET_EINT	0	DRC1 Activity Detect IRQ status 0 = DRC1 Activity Detect IRQ not set 1 = DRC1 Activity Detect IRQ set Note: Cleared when a '1' is written.
	8	SRC2_LOCK_EINT	0	SRC2 Lock IRQ status 0 = SRC2 Lock IRQ not set 1 = SRC2 Lock IRQ set Note: Cleared when a '1' is written.
	7	SRC1_LOCK_EINT	0	SRC1 Lock IRQ status 0 = SRC1 Lock IRQ not set 1 = SRC1 Lock IRQ set Note: Cleared when a '1' is written.
	6	FLL2_LOCK_EINT	0	FLL2 Lock IRQ status 0 = FLL2 Lock IRQ not set 1 = FLL2 Lock IRQ set Note: Cleared when a '1' is written.
	5	FLL1_LOCK_EINT	0	FLL1 Lock IRQ status 0 = FLL1 Lock IRQ not set 1 = FLL1 Lock IRQ set Note: Cleared when a '1' is written.
	4	MIC2_SHRT_EINT	0	MICBIAS2 Short Circuit detect IRQ status 0 = Short Circuit current IRQ not set 1 = Short Circuit current IRQ set Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3	MIC2_DET_EINT	0	MICBIAS2 Current detect IRQ status 0 = Current detect IRQ not set 1 = Current detect IRQ set Note: Cleared when a '1' is written.
	2	MIC1_SHRT_EINT	0	MICBIAS1 Short Circuit detect IRQ status 0 = Short Circuit current IRQ not set 1 = Short Circuit current IRQ set Note: Cleared when a '1' is written.
	1	MIC1_DET_EINT	0	MICBIAS1 Current detect IRQ status 0 = Current detect IRQ not set 1 = Current detect IRQ set Note: Cleared when a '1' is written.
	0	TEMP_SHUT_EINT	0	Shutdown Temperature IRQ status 0 = Shutdown Temperature IRQ not set 1 = Shutdown Temperature IRQ set Note: Cleared when a '1' is written.
R1848 (0738h) Interrupt Status 1 Mask	10	IM_GP11_EINT	1	Interrupt mask for GPIO11 0 = Not masked 1 = Masked
	9	IM_GP10_EINT	1	Interrupt mask for GPIO10 0 = Not masked 1 = Masked
	8	IM_GP9_EINT	1	Interrupt mask for GPIO9 0 = Not masked 1 = Masked
	7	IM_GP8_EINT	1	Interrupt mask for GPIO8 0 = Not masked 1 = Masked
	6	IM_GP7_EINT	1	Interrupt mask for GPIO7 0 = Not masked 1 = Masked
	5	IM_GP6_EINT	1	Interrupt mask for GPIO6 0 = Not masked 1 = Masked
	4	IM_GP5_EINT	1	Interrupt mask for GPIO5 0 = Not masked 1 = Masked
	3	IM_GP4_EINT	1	Interrupt mask for GPIO4 0 = Not masked 1 = Masked
	2	IM_GP3_EINT	1	Interrupt mask for GPIO3 0 = Not masked 1 = Masked
	1	IM_GP2_EINT	1	Interrupt mask for GPIO2 0 = Not masked 1 = Masked
	0	IM_GP1_EINT	1	Interrupt mask for GPIO1 0 = Not masked 1 = Masked

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1849 (0739h) Interrupt Status 2 Mask	13	IM_WSEQ_ DONE_EINT	1	Interrupt mask for Write Sequencer 0 = Not masked 1 = Masked
	13	IM_FIFOS_ ERR_EINT	1	Interrupt mask for Digital Core FIFO Error 0 = Not masked 1 = Masked
	11	IM_DRC3_A CTDET_EIN T	1	Interrupt mask for DRC3 Activity Detect 0 = Not masked 1 = Masked
	10	IM_DRC2_A CTDET_EIN T	1	Interrupt mask for DRC2 Activity Detect 0 = Not masked 1 = Masked
	9	IM_DRC1_A CTDET_EIN T	1	Interrupt mask for DRC1 Activity Detect 0 = Not masked 1 = Masked
	8	IM_SRC2_L OCK_EINT	1	Interrupt mask for SRC2 Lock 0 = Not masked 1 = Masked
	7	IM_SRC1_L OCK_EINT	1	Interrupt mask for SRC1 Lock 0 = Not masked 1 = Masked
	6	IM_FLL2_L OCK_EINT	1	Interrupt mask for FLL2 Lock 0 = Not masked 1 = Masked
	5	IM_FLL1_L OCK_EINT	1	Interrupt mask for FLL1 Lock 0 = Not masked 1 = Masked
	4	IM_MIC2_S HRT_EINT	1	Interrupt mask for MICBIAS2 Short Circuit detect 0 = Not masked 1 = Masked
	3	IM_MIC2_D ET_EINT	1	Interrupt mask for MICBIAS2 Current detect 0 = Not masked 1 = Masked
	2	IM_MIC1_S HRT_EINT	1	Interrupt mask for MICBIAS1 Short Circuit detect 0 = Not masked 1 = Masked
	1	IM_MIC1_D ET_EINT	1	Interrupt mask for MICBIAS1 Current detect 0 = Not masked 1 = Masked
	0	IM_TEMP_S HUT_EINT	1	Interrupt mask for Shutdown Temperature 0 = Not masked 1 = Masked

Table 79 Interrupt Configuration

DIGITAL AUDIO INTERFACE

The WM8994 provides digital audio interfaces for inputting DAC data and outputting ADC or Digital Microphone data. Flexible routing options also allow digital audio to be switched or mixed between interfaces without involving any DAC or ADC.

The WM8994 provides two full audio interfaces, AIF1 and AIF2. A third interface, AIF3, is partially supported, using multiplexers to re-configure alternate connections to AIF1 or AIF2.

In the general case, the digital audio interface uses four pins:

- ADCDAT: ADC data output
- DACDAT: DAC data input
- LRCLK: Left/Right data alignment clock
- BCLK: Bit clock, for synchronisation

In master interface mode, the clock signals BCLK and LRCLK are outputs from the WM8994. In slave mode, these signals are inputs, as illustrated below.

As an option, a GPIO pin can be configured as the Left/Right clock for the ADC. In this case, the LRCLK pin is dedicated to the DAC, allowing the ADC and DAC to be clocked independently.

Four different audio data formats are supported each digital audio interface:

- Left justified
- Right justified
- I^2S
- DSP mode

All four of these modes are MSB first. They are described in the following sections. Refer to the "Electrical Characteristics" section for timing information.

Time Division Multiplexing (TDM) is available in all four data format modes. On AIF1, the WM8994 can transmit and receive data on two stereo pairs of timeslots simultaneously. On AIF2, the applicable timeslot pair is selectable using register control bits.

PCM operation is supported using the DSP mode.

MASTER AND SLAVE MODE OPERATION

The WM8994 digital audio interfaces can operate as a master or slave as shown in Figure 38 and Figure 39. The associated control bits are described in "Digital Audio Interface Control".

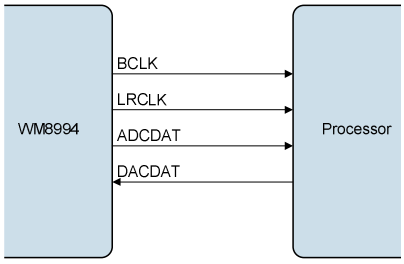


Figure 38 Master Mode

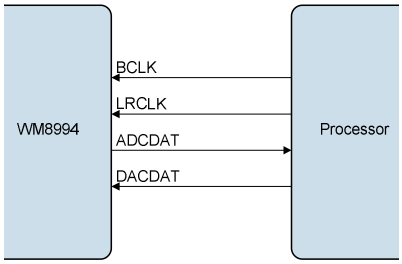


Figure 39 Slave Mode

OPERATION WITH TDM

Time division multiplexing (TDM) allows multiple devices to transfer data simultaneously on the same bus. The WM8994 ADCs and DACs support TDM in master and slave modes for all data formats and word lengths. TDM is enabled and configured using register bits defined in the "Digital Audio Interface Control" section.

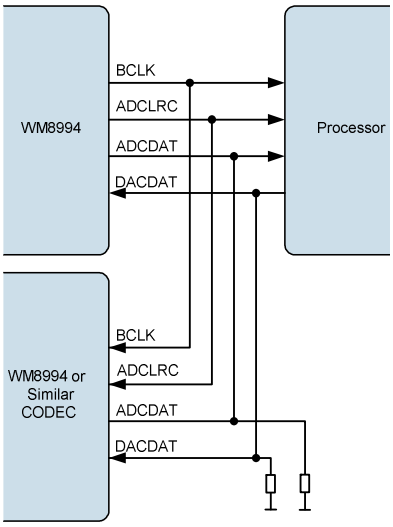


Figure 40 TDM with WM8994 as Master

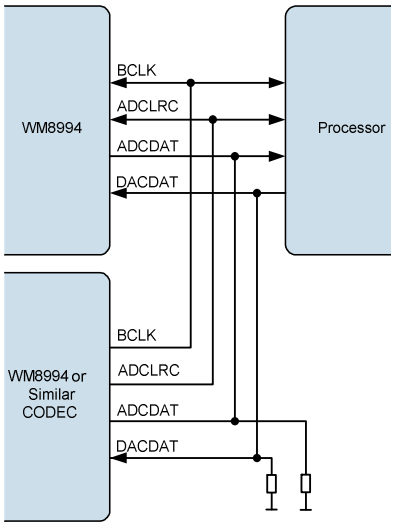


Figure 41 TDM with Other CODEC as Master

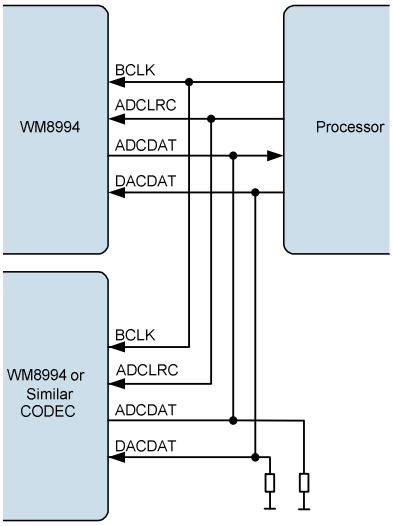


Figure 42 TDM with Processor as Master

Note: The WM8994 is a 24-bit device. If the user operates the WM8994 in 32-bit mode then the 8 LSBs will be ignored on the receiving side and not driven on the transmitting side. It is therefore recommended to add a pull-down resistor if necessary to the DACDAT line and the ADCDAT line in TDM mode.

AUDIO DATA FORMATS (NORMAL MODE)

In Right Justified mode, the LSB is available on the last rising edge of BCLK before a LRCLK transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCLK transition.

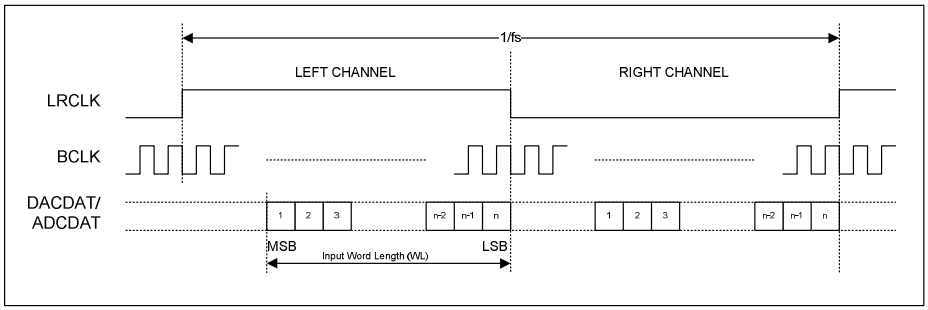


Figure 43 Right Justified Audio Interface (assuming n-bit word length)

In Left Justified mode, the MSB is available on the first rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.

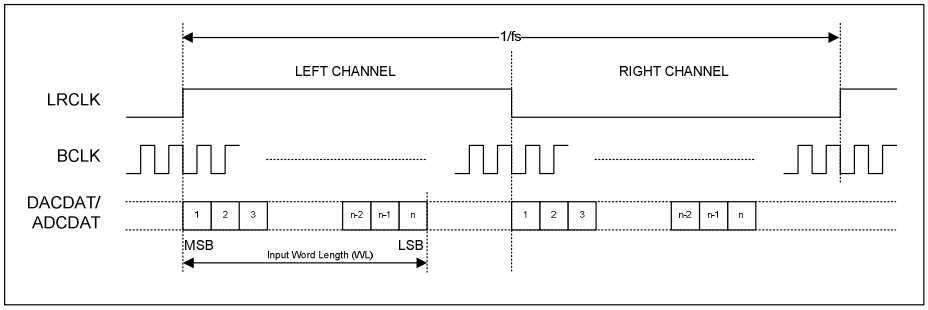


Figure 44 Left Justified Audio Interface (assuming n-bit word length)

In I^2S mode, the MSB is available on the second rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

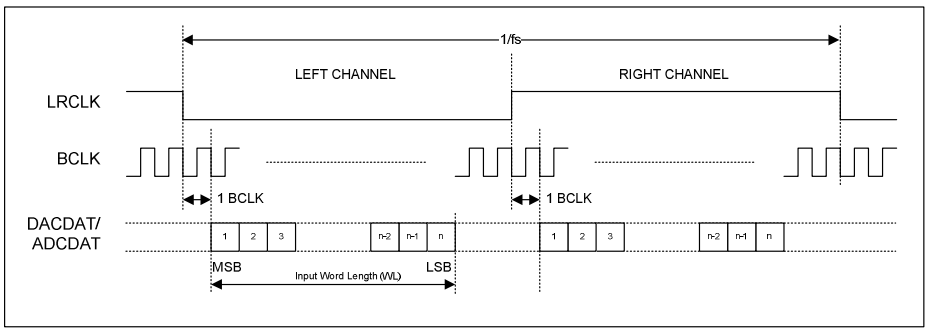


Figure 45 I2S Justified Audio Interface (assuming n-bit word length)

In DSP mode, the left channel MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of BCLK (selectable by AIF_LRCLK_INV) following a rising edge of LRCLK. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

In device master mode, the LRC output will resemble the frame pulse shown in Figure 46 and Figure 47. In device slave mode, Figure 48 and Figure 49, it is possible to use any length of frame pulse less than 1/fs, providing the falling edge of the frame pulse occurs greater than one BCLK period before the rising edge of the next frame pulse.

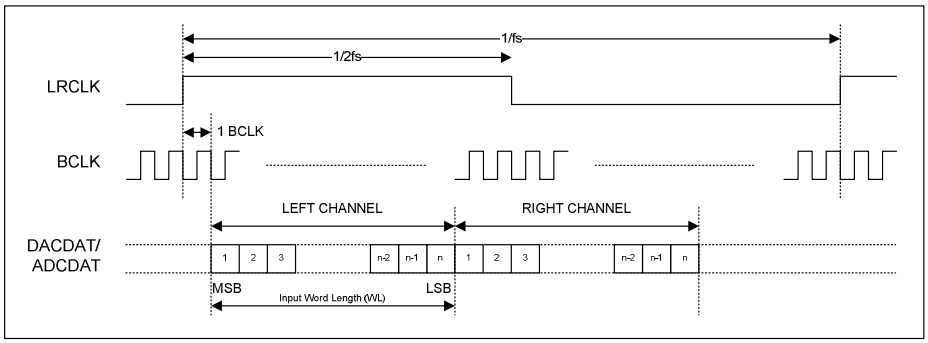


Figure 46 DSP Mode Audio Interface (mode A, AIF_LRCLK_INV=0, Master)

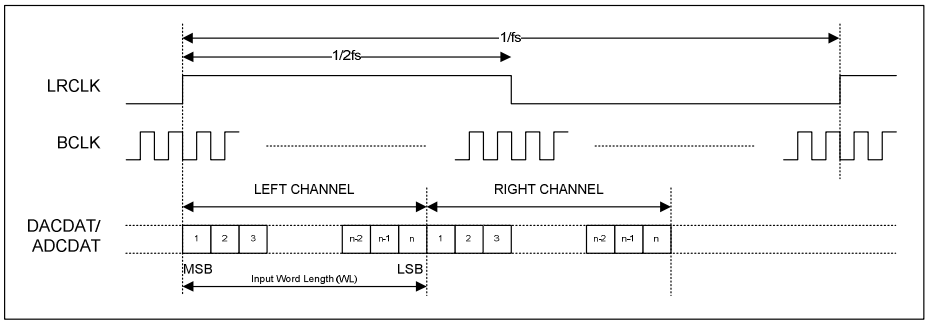


Figure 47 DSP Mode Audio Interface (mode B, AIF_LRCLK_INV=1, Master)

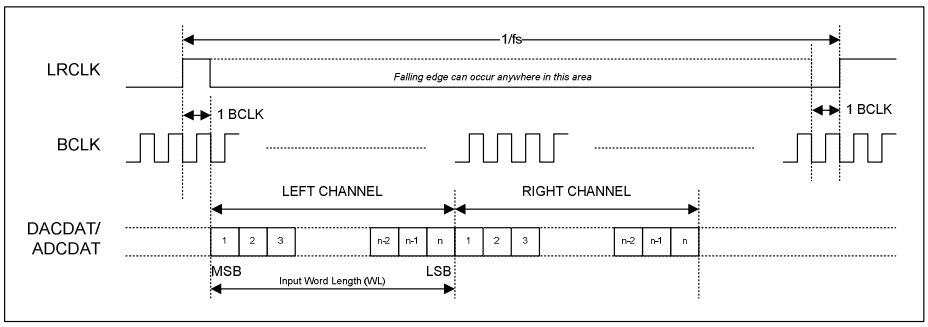


Figure 48 DSP Mode Audio Interface (mode A, AIF_LRCLK_INV=0, Slave)

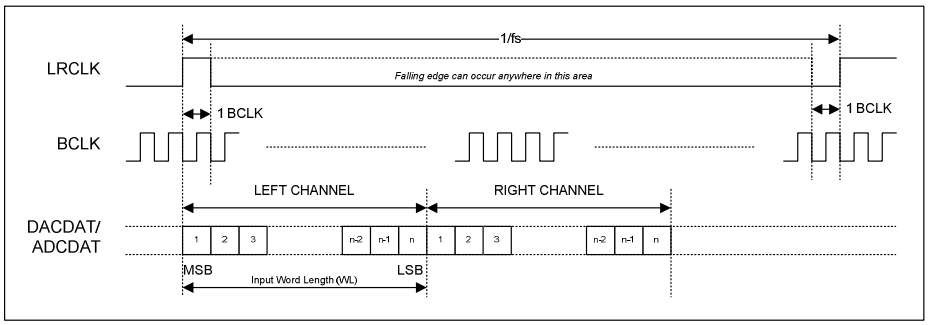


Figure 49 DSP Mode Audio Interface (mode B, AIF_LRCLK_INV=1, Slave)

PCM operation is supported in DSP interface mode. WM8994 ADC data that is output on the Left Channel will be read as mono PCM data by the receiving equipment. Mono PCM data received by the WM8994 will be treated as Left Channel data. This data may be routed to the Left/Right DACs using the control fields described in the “Digital Mixing” and “Digital Audio Interface Control” sections.

AUDIO DATA FORMATS (TDM MODE)

TDM is supported in master and slave modes. All audio interface data formats support time division multiplexing (TDM) for ADC and DAC data.

When TDM is enabled on AIF1, the WM8994 can transmit and receive data in both Slot 0 and Slot 1. In the case of AIF2, the required timeslot is selected using register control bits when TDM is enabled.

When TDM is enabled, the ADCDAT pin will be tri-stated immediately before and immediately after data transmission, to allow another ADC device to drive this signal line for the remainder of the sample period. Note that it is important that two ADC devices do not attempt to drive the data pin simultaneously. A short circuit may occur if the transmission time of the two ADC devices overlap with each other. See “Audio Interface Timing” for details of the ADCDAT output relative to BCLK signal. Note that it is possible to ensure a gap exists between transmissions by setting the transmitted word length to a value higher than the actual length of the data. For example, if 32-bit word length is selected where only 24-bit data is available, then the WM8994 interface will tri-state after transmission of the 24-bit data, ensuring a gap after the WM8994 TDM slot.

When TDM is enabled, BCLK frequency must be high enough to allow data from both time slots to be transferred. The relative timing of Slot 0 and Slot 1 depends upon the selected data format as shown in Figure 50 to Figure 54.

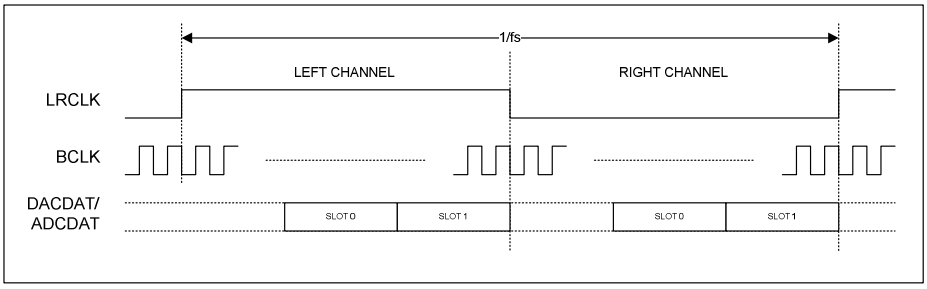


Figure 50 TDM in Right-Justified Mode

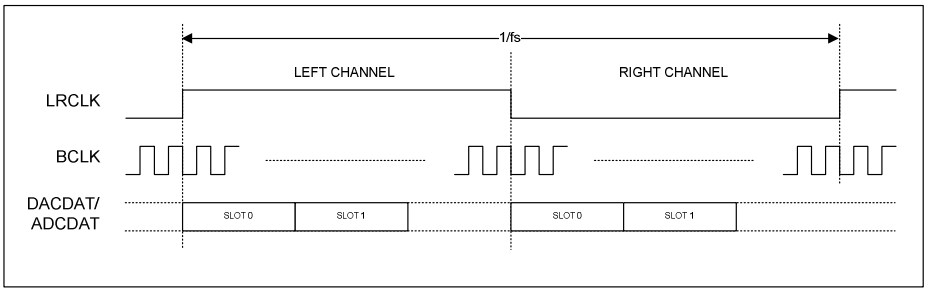


Figure 51 TDM in Left-Justified Mode

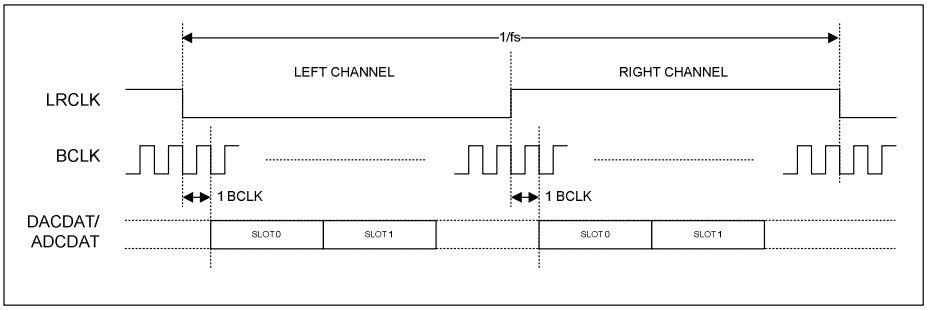


Figure 52 TDM in I²S Mode

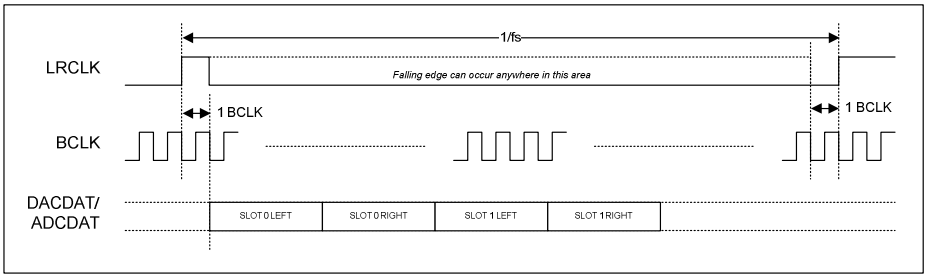


Figure 53 TDM in DSP Mode A

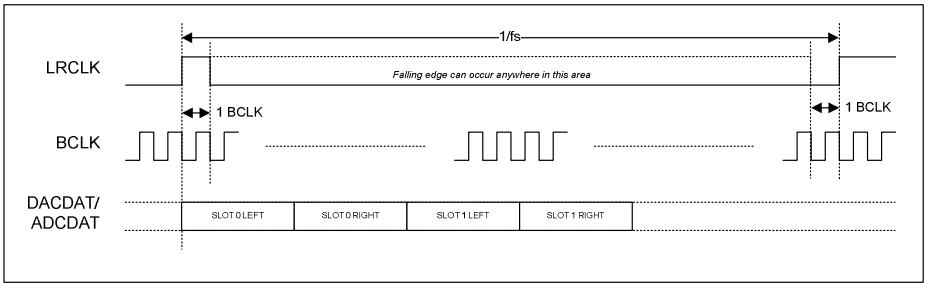


Figure 54 TDM in DSP Mode B

DIGITAL AUDIO INTERFACE CONTROL

This section describes the configuration of the WM8994 digital audio interface paths.

Each interface can be configured as Master or Slave, or can be tri-stated. Each input and output signal path can be independently enabled or disabled. AIF output (digital record) and AIF input (digital playback) paths can use a common Left/Right clock, or can use separate clocks for mixed sample rates.

Each interface supports flexible formats, word-length, TDM configuration, channel swapping and input path digital boost functions. 8-bit companding modes and digital loopback is also possible.

AIF1 - MASTER / SLAVE AND TRI-STATE CONTROL

The Digital Audio Interface AIF1 can operate in Master or Slave modes, selected by AIF1_MSTR. In Master mode, the BCLK1 and LRCLK1 signals are generated by the WM8994 when one or more AIF1 channels is enabled.

When AIF1_CLK_FRC is set in Master mode, then BCLK1 is output at all times, including when none of the AIF1 audio channels is enabled.

When AIF1_LRCLK_FRC is set in Master mode, then LRCLK1 is output at all times, including when none of the AIF1 audio channels is enabled.

The AIF1 interface can be tri-stated by setting the AIF1_TRI register. When this bit is set, then all of the AIF1 outputs are un-driven (high-impedance). Note that the ADCLRCLK1/GPIO1 pin is a configurable pin which may take different functions independent of AIF1. The AIF1_TRI register only controls the ADCLRCLK1/GPIO1 pin when its function is set to ADCLRCLK1. See “General Purpose Input/Output” to configure the GPIO1 pin.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R770 (0302h) AIF1 Master/Slave	15	AIF1_TRI	0	AIF1 Audio Interface tri-state 0 = AIF1 pins operate normally 1 = Tri-state all AIF1 interface pins Note that the GPIO1 pin is controlled by this register only when configured as ADCLRCLK1.
	14	AIF1_MSTR	0	AIF1 Audio Interface Master Mode Select 0 = Slave mode 1 = Master mode
	13	AIF1_CLK_FRC	0	Forces BCLK1 to be enabled when all AIF1 audio channels are disabled. 0 = Normal 1 = BCLK1 always enabled in Master mode
	12	AIF1_LRCLK_FRC	0	Forces LRCLK1 to be enabled when all AIF1 audio channels are disabled. 0 = Normal 1 = LRCLK1 always enabled in Master mode

Table 80 AIF1 Master / Slave and Tri-state Control

AIF1 - SIGNAL PATH ENABLE

The AIF1 interface supports four input channels and four output channels when TDM mode is enabled. The AIF1 interface supports two input channels and two output channels in normal mode (ie. TDM not enabled).

Each of the available channels can be enabled or disabled using the register bits defined in Table 81.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 (0004h) Power Management (4)	11	AIF1ADC2L_ENA	0	Enable AIF1ADC2 (Left) output path (AIF1, Timeslot 1) 0 = Disabled 1 = Enabled
	10	AIF1ADC2R_ENA	0	Enable AIF1ADC2 (Right) output path (AIF1, Timeslot 1) 0 = Disabled 1 = Enabled
	9	AIF1ADC1L_ENA	0	Enable AIF1ADC1 (Left) output path (AIF1, Timeslot 0) 0 = Disabled 1 = Enabled
	8	AIF1ADC1R_ENA	0	Enable AIF1ADC1 (Right) output path (AIF1, Timeslot 0) 0 = Disabled 1 = Enabled
R5 (0005h) Power Management (5)	11	AIF1DAC2L_ENA	0	Enable AIF1DAC2 (Left) input path (AIF1, Timeslot 1) 0 = Disabled 1 = Enabled
	10	AIF1DAC2R_ENA	0	Enable AIF1DAC2 (Right) input path (AIF1, Timeslot 1) 0 = Disabled 1 = Enabled
	9	AIF1DAC1L_ENA	0	Enable AIF1DAC1 (Left) input path (AIF1, Timeslot 0) 0 = Disabled 1 = Enabled
	8	AIF1DAC1R_ENA	0	Enable AIF1DAC1 (Right) input path (AIF1, Timeslot 0) 0 = Disabled 1 = Enabled

Table 81 AIF1 Signal Path Enable

AIF1 - BCLK AND LRCLK CONTROL

The BCLK1 frequency is controlled relative to AIF1CLK by the AIF1_BCLK_DIV divider. See “Clocking and Sample Rates” for details of the AIF1 clock, AIF1CLK.

The LRCLK1 frequency is controlled relative to BCLK1 by the AIF1DAC_RATE divider.

When the GPIO1 pin is configured as ADCLRCLK1, then the ADCLRCLK1 frequency is controlled relative to BCLK1 by the AIF1ADC_RATE divider. In this case, the ADCLRCLK1 is dedicated to AIF1 output, and the LRCLK1 pin is dedicated to AIF1 input, allowing different sample rates to be supported in the two paths. See “General Purpose Input/Output” for the configuration of GPIO1.

In Master mode, the LRCLK1 output is generated by the WM8994 when any of the AIF1 channels is enabled. In Slave mode, the LRCLK1 output is disabled by default to allow another digital audio interface to drive this pin. It is also possible to force the LRCLK1 signal to be output, using the AIF1DAC_LRCLK_DIR bit, allowing mixed master and slave modes.

When the GPIO1 pin is configured as ADCLRCLK1, then this output can be forced using the AIF1ADC_LRCLK_DIR bit.

The BCLK1 output can be inverted using the AIF1_BCLK_INV register bit. The LRCLK1 and ADCLRCLK1 output (when selected) can be inverted using the AIF1_LRCLK_INV register control.

The AIF1 clock generators are controlled as illustrated in Figure 55.

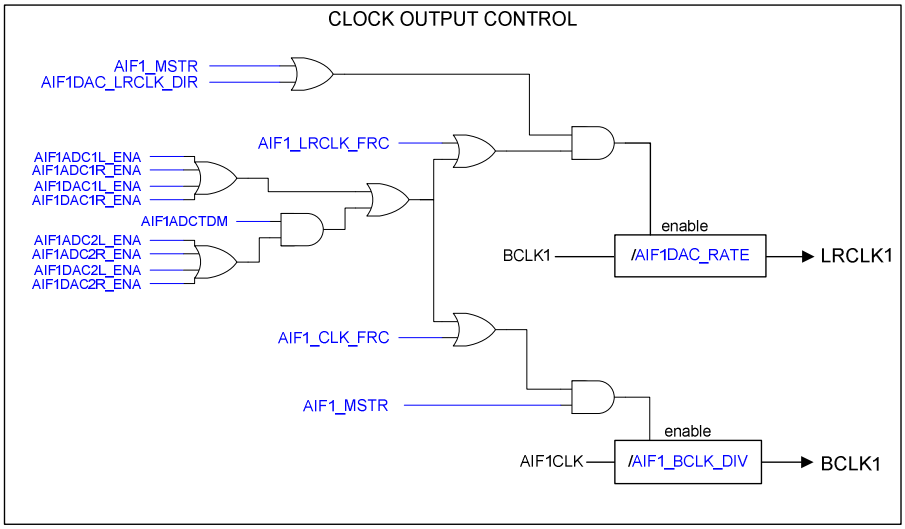


Figure 55 Audio Interface 1 - BCLK and LRCLK Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R768 (0300h) AIF1 Control (1)	8	AIF1_BCLK_INV	0	BCLK1 Invert 0 = BCLK1 not inverted 1 = BCLK1 inverted
	7	AIF1_LRCLK_INV	0	Right, left and I^2S modes – LRCLK1 polarity 0 = normal LRCLK1 polarity 1 = invert LRCLK1 polarity
				DSP Mode – mode A/B select 0 = MSB is available on 2nd BCLK1 rising edge after LRCLK1 rising edge (mode A) 1 = MSB is available on 1st BCLK1 rising edge after LRCLK1 rising edge (mode B)
R771 (0303h) AIF1 BCLK	7:4	AIF1_BCLK_DIV [3:0]	0100	BCLK1 Rate 0000 = AIF1CLK 0001 = AIF1CLK / 2 0010 = AIF1CLK / 4 0011 = AIF1CLK / 6 0100 = AIF1CLK / 8 0101 = AIF1CLK / 12 0110 = AIF1CLK / 16 0111 = AIF1CLK / 24 1000 = AIF1CLK / 32 1001 = AIF1CLK / 48 All other codes are Reserved
R772 (0304h) AIF1ADC LRCLK	11	AIF1ADC_LRCLK_DIR	0	Allows ADCLRCLK1 to be enabled in Slave mode 0 = Normal 1 = ADCLRCLK1 enabled in Slave mode

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	10:0	AIF1ADC_RATE [10:0]	040h	ADCLRCLK1 Rate ADCLRCLK1 clock output = BCLK1 / AIF1ADC_RATE Integer (LSB = 1) Valid from 8..2047
R773 (0305h) AIF1DAC LRCLK	11	AIF1DAC_LRCLK_DIR	0	Allows LRCLK1 to be enabled in Slave mode 0 = Normal 1 = LRCLK1 enabled in Slave mode
	10:0	AIF1DAC_RATE [10:0]	040h	LRCLK1 Rate LRCLK1 clock output = BCLK1 / AIF1DAC_RATE Integer (LSB = 1) Valid from 8..2047

Table 82 AIF1 BCLK and LRCLK Control

AIF1 - DIGITAL AUDIO DATA CONTROL

The register bits controlling the audio data format, word length, left/right channel selection and TDM control for AIF1 are described in Table 83.

A digital gain function is available at the audio interface input path to boost the DAC volume when a small signal is received on DACDAT1. This is controlled using the AIF1DAC_BOOST register. To prevent clipping, this function should not be used when the boosted data is expected to be greater than 0dBFS.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R768 (0300h) AIF1 Control (1)	15	AIF1ADCL_SRC	0	AIF1 Left Digital Audio interface source 0 = Left ADC data is output on left channel 1 = Right ADC data is output on left channel
	14	AIF1ADCR_SRC	1	AIF1 Right Digital Audio interface source 0 = Left ADC data is output on right channel 1 = Right ADC data is output on right channel
	13	AIF1ADC_TDM	0	AIF1 transmit (ADC) TDM Enable 0 = Normal ADCDAT1 operation 1 = TDM enabled on ADCDAT1
	6:5	AIF1_WL [1:0]	10	AIF1 Digital Audio Interface Word Length 00 = 16 bits 01 = 20 bits 10 = 24 bits 11 = 32 bits Note - 8-bit modes can be selected using the “Companding” control bits.
	4:3	AIF1_FMT [1:0]	10	AIF1 Digital Audio Interface Format 00 = Right justified 01 = Left justified 10 = I^2S Format 11 = DSP Mode
R769 (0301h) AIF1 Control (2)	15	AIF1DACL_SRC	0	AIF1 Left Receive Data Source Select 0 = Left DAC receives left interface data 1 = Left DAC receives right interface data
	14	AIF1DACR_SRC	1	AIF1 Right Receive Data Source Select 0 = Right DAC receives left interface data 1 = Right DAC receives right interface data

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	11:10	AIF1DAC_BOOST [1:0]	00	AIF1 Input Path Boost 00 = 0dB 01 = +6dB 10 = +12dB 11 = +18dB
R774 (0306h) AIF1 DAC Data	1	AIF1DACL_DAT_INV	0	AIF1 Left Receive Data Invert 0 = Not inverted 1 = Inverted
	0	AIF1DACR_DAT_INV	0	AIF1 Right Receive Data Invert 0 = Not inverted 1 = Inverted
R775 (0307h) AIF1 ADC Data	1	AIF1ADCL_DAT_INV	0	AIF1 Left Transmit Data Invert 0 = Not inverted 1 = Inverted
	0	AIF1ADCR_DAT_INV	0	AIF1 Right Transmit Data Invert 0 = Not inverted 1 = Inverted

Table 83 AIF1 Digital Audio Data Control

AIF1 - COMPANDING

The WM8994 supports A-law and μ-law companding on both transmit (ADC) and receive (DAC) sides of AIF1. This is configured using the register bits described in Table 84.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R769 (0301h) AIF1 Control (2)	4	AIF1DAC_COMP	0	AIF1 Receive Companding Enable 0 = disabled 1 = enabled
	3	AIF1DAC_COMPMODE	0	AIF1 Receive Companding Type 0 = μ-law 1 = A-law
	2	AIF1ADC_COMP	0	AIF1 Transmit Companding Enable 0 = disabled 1 = enabled
	1	AIF1ADC_COMPMODE	0	AIF1 Transmit Companding Type 0 = μ-law 1 = A-law

Table 84 AIF1 Companding

Companding involves using a piecewise linear approximation of the following equations (as set out by ITU-T G.711 standard) for data compression:

μ-law (where μ=255 for the U.S. and Japan):

$$F(x) = \ln(1 + \mu|x|) / \ln(1 + \mu) \quad \} \text{ for } -1 \le x \le 1$$

A-law (where A=87.6 for Europe):

$$F(x) = A|x| / (1 + \ln A) \quad \} \text{ for } x \le 1/A$$

$$F(x) = (1 + \ln A|x|) / (1 + \ln A) \quad \} \text{ for } 1/A \le x \le 1$$

The companded data is also inverted as recommended by the G.711 standard (all 8 bits are inverted for μ-law, all even data bits are inverted for A-law). The data will be transmitted as the first 8 MSBs of data.

Companding converts 13 bits (μ-law) or 12 bits (A-law) to 8 bits using non-linear quantization. This provides greater precision for low amplitude signals than for high amplitude signals, resulting in a greater usable dynamic range than 8 bit linear quantization. The companded signal is an 8-bit word comprising sign (1 bit), exponent (3 bits) and mantissa (4 bits).

AIF1 8-bit mode is selected whenever AIF1DAC_COMP=1 or AIF1ADC_COMP=1. The use of 8-bit data allows samples to be passed using as few as 8 BCLK1 cycles per LRCLK1 frame. When using DSP mode B, 8-bit data words may be transferred consecutively every 8 BCLK1 cycles.

AIF1 8-bit mode (without Companding) may be enabled by setting AIF1DAC_COMPMODE=1 or AIF1ADC_COMPMODE=1, when AIF1DAC_COMP=0 and AIF1ADC_COMP=0.

BIT7	BIT[6:4]	BIT[3:0]
SIGN	EXPONENT	MANTISSA

Table 85 8-bit Companded Word Composition

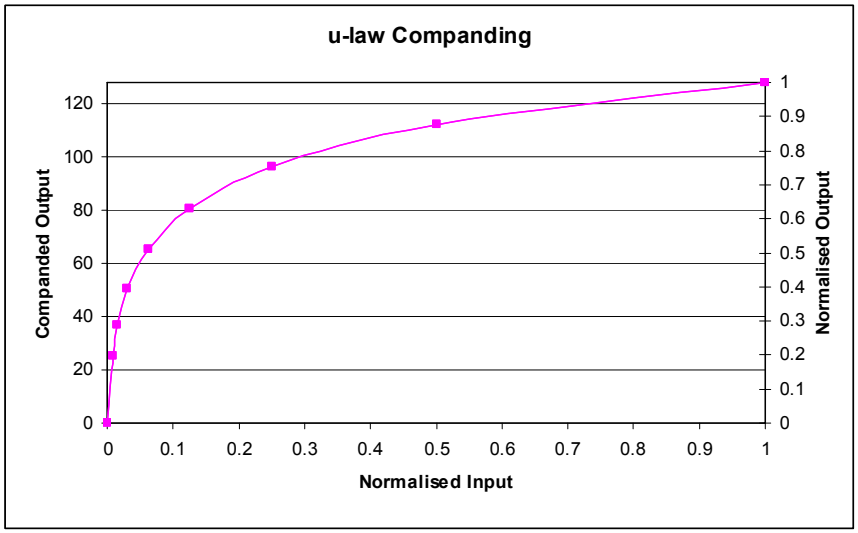


Figure 56 μ-Law Companding

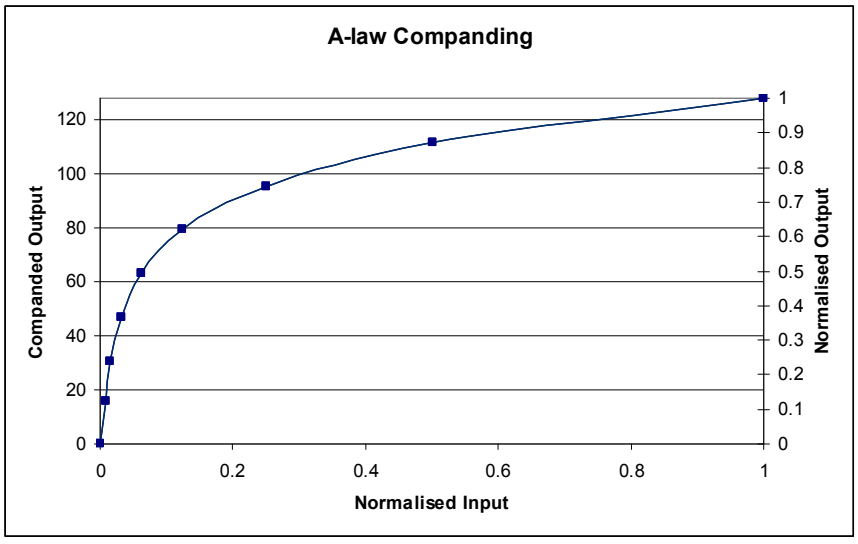


Figure 57 A-Law Companding

AIF1 - LOOPBACK

The AIF1 interface can provide a Loopback option. When the AIF1_LOOPBACK bit is set, then AIF1 digital audio output is routed to the AIF1 digital audio input. The normal input (DACDAT1) is not used when AIF1 Loopback is enabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R769 (0301h) AIF1 Control (2)	0	AIF1_LOOPBACK	0	AIF1 Digital Loopback Function 0 = No loopback 1 = Loopback enabled (ADCDAT1 data output is directly input to DACDAT1 data input).

Table 86 AIF1 Loopback

AIF2 - MASTER / SLAVE AND TRI-STATE CONTROL

The Digital Audio Interface AIF2 can operate in Master or Slave modes, selected by AIF2_MSTR. In Master mode, the BCLK2 and LRCLK2 signals are generated by the WM8994 when one or more AIF2 channels is enabled.

When AIF2_CLK_FRC is set in Master mode, then BCLK2 is output at all times, including when none of the AIF2 audio channels is enabled.

When AIF2_LRCLK_FRC is set in Master mode, then LRCLK2 is output at all times, including when none of the AIF2 audio channels is enabled.

Note that the AIF2 pins are also GPIO pins, whose function is configurable. These pins must be configured as AIF functions when used as audio interface pins. See “General Purpose Input/Output”.

The AIF2 interface can be tri-stated by setting the AIF2_TRI register. When this bit is set, then all of the AIF2 outputs are un-driven (high-impedance). The AIF2_TRI register only affects those pins which are configured for AIF2 functions; it does not affect pins which are configured for other functions.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R786 (0312h) AIF2 Master/Slave	15	AIF2_TRI	0	AIF2 Audio Interface tri-state 0 = AIF2 pins operate normally 1 = Tri-state all AIF2 interface pins Note that pins not configured as AIF2 functions are not affected by this register.
	14	AIF2_MSTR	0	AIF2 Audio Interface Master Mode Select 0 = Slave mode 1 = Master mode
	13	AIF2_CLK_FRC	0	Forces BCLK2 to be enabled when all AIF2 audio channels are disabled. 0 = Normal 1 = BCLK2 always enabled in Master mode
	12	AIF2_LRCLK_FRC	0	Forces LRCLK2 to be enabled when all AIF2 audio channels are disabled. 0 = Normal 1 = LRCLK2 always enabled in Master mode

Table 87 AIF2 Master / Slave and Tri-state Control

AIF2 - SIGNAL PATH ENABLE

The AIF2 interface supports two input channels and two output channels. Each of the available channels can be enabled or disabled using the register bits defined in Table 88.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 (0004h) Power Management (4)	13	AIF2ADCL_ ENA	0	Enable AIF2ADC (Left) output path 0 = Disabled 1 = Enabled
	12	AIF2ADCR_ ENA	0	Enable AIF2ADC (Right) output path 0 = Disabled 1 = Enabled
R5 (0005h) Power Management (5)	13	AIF2DACL_ ENA	0	Enable AIF2DAC (Left) input path 0 = Disabled 1 = Enabled
	12	AIF2DACR_ ENA	0	Enable AIF2DAC (Right) input path 0 = Disabled 1 = Enabled

Table 88 AIF2 Signal Path Enable

AIF2 - BCLK AND LRCLK CONTROL

The BCLK2 frequency is controlled relative to AIF2CLK by the AIF2_BCLK_DIV divider. See “Clocking and Sample Rates” for details of the AIF2 clock, AIF2CLK.

The LRCLK2 frequency is controlled relative to BCLK2 by the AIF2DAC_RATE divider.

When the GPIO6 pin is configured as ADCLRCLK2, then the ADCLRCLK2 frequency is controlled relative to BCLK2 by the AIF2ADC_RATE divider. In this case, the ADCLRCLK2 is dedicated to AIF2 output, and the LRCLK2 pin is dedicated to AIF2 input, allowing different sample rates to be supported in the two paths. See “General Purpose Input/Output” for the configuration of GPIO6.

In Master mode, the LRCLK2 output is generated by the WM8994 when any of the AIF2 channels is enabled. In Slave mode, the LRCLK2 output is disabled by default to allow another digital audio interface to drive this pin. It is also possible to force the LRCLK2 signal to be output, using the AIF2DAC_LRCLK_DIR bit, allowing mixed master and slave modes.

When the GPIO6 pin is configured as ADCLRCLK2, then this output can be forced using the AIF2ADC_LRCLK_DIR bit.

The BCLK2 output can be inverted using the AIF2_BCLK_INV register bit. The LRCLK2 and ADCLRCLK2 output (when selected) can be inverted using the AIF2_LRCLK_INV register control.

The AIF2 clock generators are controlled as illustrated in Figure 58.

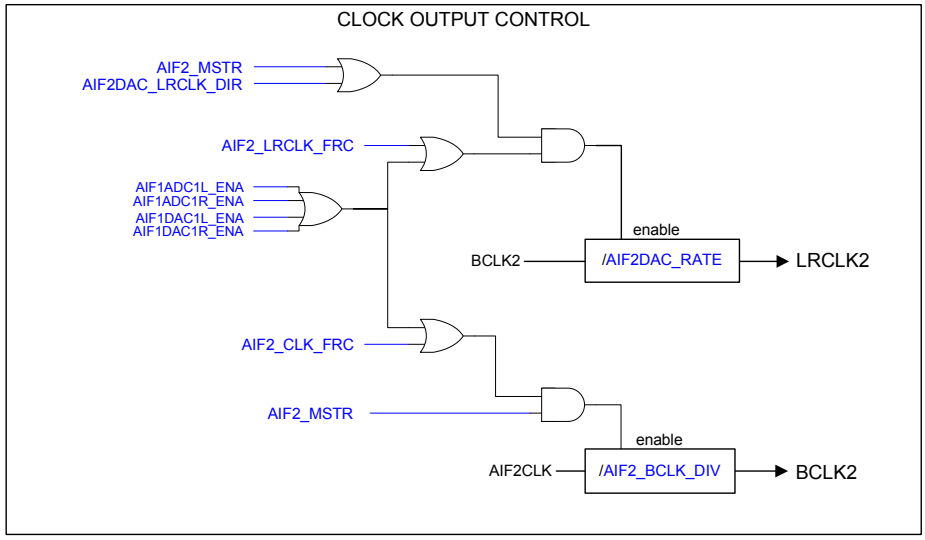


Figure 58 Audio Interface 2 - BCLK and LRCLK Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R784 (0310h) AIF2 Control (1)	8	AIF2_BCLK_INV	0	BCLK2 Invert 0 = BCLK2 not inverted 1 = BCLK2 inverted
	7	AIF2_LRCLK_INV	0	Right, left and I^2S modes – LRCLK2 polarity 0 = normal LRCLK2 polarity 1 = invert LRCLK2 polarity
				DSP Mode – mode A/B select 0 = MSB is available on 2nd BCLK2 rising edge after LRCLK2 rising edge (mode A) 1 = MSB is available on 1st BCLK2 rising edge after LRCLK2 rising edge (mode B)
R787 (0313h) AIF2 BCLK	7:4	AIF2_BCLK_DIV [3:0]	0100	BCLK2 Rate 0000 = AIF2CLK 0001 = AIF2CLK / 2 0010 = AIF2CLK / 4 0011 = AIF2CLK / 6 0100 = AIF2CLK / 8 0101 = AIF2CLK / 12 0110 = AIF2CLK / 16 0111 = AIF2CLK / 24 1000 = AIF2CLK / 32 1001 = AIF2CLK / 48 All other codes are Reserved
R788 (0314h) AIF2ADC LRCLK	11	AIF2ADC_LRCLK_DIR	0	Allows ADCLRCLK2 to be enabled in Slave mode 0 = Normal 1 = ADCLRCLK2 enabled in Slave mode
	10:0	AIF2ADC_RATE [10:0]	040h	ADCLRCLK2 Rate ADCLRCLK2 clock output = BCLK2 / AIF2ADC_RATE Integer (LSB = 1) Valid from 8..2047

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R789 (0315h) AIF2DAC LRCLK	11	AIF2DAC_LRCLK_DIR	0	Allows LRCLK2 to be enabled in Slave mode 0 = Normal 1 = LRCLK2 enabled in Slave mode
	10:0	AIF2DAC_RATE [10:0]	040h	LRCLK2 Rate LRCLK2 clock output = BCLK2 / AIF2DAC_RATE Integer (LSB = 1) Valid from 8..2047

Table 89 AIF2 BCLK and LRCLK Control

AIF2 - DIGITAL AUDIO DATA CONTROL

The register bits controlling the audio data format, word length, left/right channel selection and TDM control for AIF1 are described in Table 90.

A digital gain function is available at the audio interface input path to boost the DAC volume when a small signal is received on DACDAT2. This is controlled using the AIF2DAC_BOOST register. To prevent clipping, this function should not be used when the boosted data is expected to be greater than 0dBFS.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R784 (0310h) AIF2 Control (1)	15	AIF2ADCL_SRC	0	AIF2 Left Digital Audio interface source 0 = Left ADC data is output on left channel 1 = Right ADC data is output on left channel
	14	AIF2ADCR_SRC	1	AIF2 Right Digital Audio interface source 0 = Left ADC data is output on right channel 1 = Right ADC data is output on right channel
	13	AIF2ADC_TDM	0	AIF2 transmit (ADC) TDM Enable 0 = Normal ADCDAT2 operation 1 = TDM enabled on ADCDAT2
	12	AIF2ADC_TDM_CHAN	0	AIF2 transmit (ADC) TDM Slot Select 0 = Slot 0 1 = Slot 1
	6:5	AIF2_WL [1:0]	10	AIF2 Digital Audio Interface Word Length 00 = 16 bits 01 = 20 bits 10 = 24 bits 11 = 32 bits Note - 8-bit modes can be selected using the "Companding" control bits.
	4:3	AIF2_FMT [1:0]	10	AIF2 Digital Audio Interface Format 00 = Right justified 01 = Left justified 10 = I^2S Format 11 = DSP Mode
R785 (0311h) AIF2 Control (2)	15	AIF2DACL_SRC	0	AIF2 Left Receive Data Source Select 0 = Left DAC receives left interface data 1 = Left DAC receives right interface data
	14	AIF2DACR_SRC	1	AIF2 Right Receive Data Source Select 0 = Right DAC receives left interface data 1 = Right DAC receives right interface data
	13	AIF2DAC_TDM	0	AIF2 receive (DAC) TDM Enable 0 = Normal DACDAT2 operation 1 = TDM enabled on DACDAT2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	12	AIF2DAC_TDM_CHAN	0	AIF2 receive(DAC) TDM Slot Select 0 = Slot 0 1 = Slot 1
	11:10	AIF2DAC_BOOST [1:0]	00	AIF2 Input Path Boost 00 = 0dB 01 = +6dB 10 = +12dB 11 = +18dB
R790 (0316h) AIF2 DAC Data	1	AIF2DACL_DAT_INV	0	AIF2 Left Receive Data Invert 0 = Not inverted 1 = Inverted
	0	AIF2DACR_DAT_INV	0	AIF2 Right Receive Data Invert 0 = Not inverted 1 = Inverted
R791 (0317h) AIF2 ADC Data	1	AIF2ADCL_DAT_INV	0	AIF2 Left Transmit Data Invert 0 = Not inverted 1 = Inverted
	0	AIF2ADCR_DAT_INV	0	AIF2 Right Transmit Data Invert 0 = Not inverted 1 = Inverted

Table 90 AIF2 Digital Audio Data Control

AIF2 - COMPANDING

The WM8994 supports A-law and μ-law companding on both transmit (ADC) and receive (DAC) sides of AIF2. This is configured using the register bits described in Table 91.

For more details on Companding, see the Audio Interface AIF1 description above.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R785 (0311h) AIF2 Control (2)	4	AIF2DAC_COMP	0	AIF2 Receive Companding Enable 0 = disabled 1 = enabled
	3	AIF2DAC_COMPMODE	0	AIF2 Receive Companding Type 0 = μ-law 1 = A-law
	2	AIF2ADC_COMP	0	AIF2 Transmit Companding Enable 0 = disabled 1 = enabled
	1	AIF2ADC_COMPMODE	0	AIF2 Transmit Companding Type 0 = μ-law 1 = A-law

Table 91 AIF2 Companding

AIF2 - LOOPBACK

The AIF2 interface can provide a Loopback option. When the AIF2_LOOPBACK bit is set, then AIF2 digital audio output is routed to the AIF2 digital audio input. The normal input (DACDAT2) is not used when AIF2 Loopback is enabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R785 (0311h) AIF2 Control (2)	0	AIF2_LOOPBACK	0	AIF2 Digital Loopback Function 0 = No loopback 1 = Loopback enabled (ADCDAT2 data output is directly input to DACDAT2 data input).

Table 92 AIF2 Loopback

AUDIO INTERFACE AIF3 CONFIGURATION

The WM8994 provides two full audio interfaces, AIF1 and AIF2. A third interface, AIF3, is partially supported, using multiplexers to re-configure alternate connections to AIF1 or AIF2. The relevant multiplexers are illustrated in Figure 59.

Note that, in addition to providing alternate input / output pins to the audio interfaces AIF1 and AIF2, the multiplexers also provide the capability to link AIF3 pins directly to AIF2 pins, without involving the AIF2 interface processing resource.

All of the AIF3 connections are supported on pins which also provide GPIO functions. These pins must be configured as AIF functions when used as audio interface pins. See “General Purpose Input/Output”.

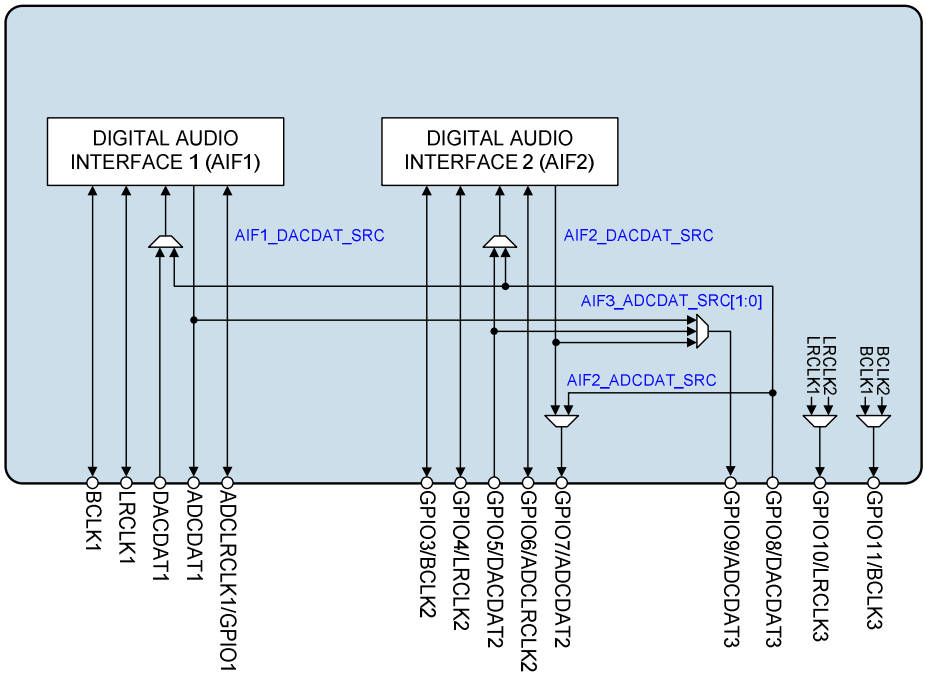


Figure 59 Audio Interface AIF3 Configuration

The GPIO8 pin also supports the DACDAT3 function. When configured as DACDAT3, this pin may be used as an alternate data input pin to AIF1 or AIF2. The data input source for AIF1 is selected using the AIF1_DACDAT_SRC register. The data input source for AIF2 is selected using the AIF2_DACDAT_SRC register.

The GPIO9 pin also supports the ADCDAT3 function. When configured as ADCDAT3, this pin may be used as an alternate data output pin to AIF1 or AIF2. It is also possible to route the DACDAT2 input pin to the ADCDAT3 output. The ADCDAT3 source is selected using the AIF3_ADCDAT_SRC register.

The DACDAT3 input pin referenced above may also be routed to the ADCDAT2 output. The ADCDAT2 source is selected using the AIF2_ADCDAT_SRC register.

The GPIO10 pin also supports the LRCLK3 function. When configured as LRCLK3, this pin outputs the LRCLK signal from AIF1 or AIF2. The applicable AIF source is determined automatically as defined in Table 93. Note that the LRCLK3 signal is also controlled by the logic illustrated in Figure 55 (AIF1) or Figure 58 (AIF2), depending on the selected AIF source.

The GPIO11 pin also supports the BCLK3 function. When configured as BCLK3, this pin outputs the BCLK signal from AIF1 or AIF2. The applicable AIF source is determined automatically as defined in Table 93. Note that the BCLK3 signal is also controlled by the logic illustrated in Figure 55 (AIF1) or Figure 58 (AIF2), depending on the selected AIF source.

CONDITION	DESCRIPTION
AIF1_DACDAT_SRC = 1 (DACDAT3 selected as AIF1 data input)	AIF1 selected as BCLK3 / LRCLK3 source
AIF3_ADCDAT_SRC[1:0] = 00 (AIF1 data output selected on ADCDAT3)	AIF1 selected as BCLK3 / LRCLK3 source
All other conditions	AIF2 selected as BCLK3 / LRCLK3 source

Table 93 BCLK3 / LRCLK3 Configuration

AIF3 interface can be tri-stated by setting the AIF3_TRIS register. When this bit is set, then all of the AIF3 outputs are un-driven (high-impedance). The AIF3_TRIS register only affects those pins which are configured for AIF3 functions; it does not affect pins which are configured for other functions.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (0006h) Power Management (6)	5	AIF3_TRIS	0	AIF3 Audio Interface tri-state 0 = AIF3 pins operate normally 1 = Tri-state all AIF3 interface pins Note that pins not configured as AIF3 functions are not affected by this register.
	4:3	AIF3_ADCDAT_SRC [1:0]	00	GPIO9/ADCDAT3 Source select 00 = AIF1 ADCDAT1 01 = AIF2 ADCDAT2 10 = GPIO5/DACDAT2 11 = Reserved Note that GPIO9 must be configured as ADCDAT3. For selection 11, the GPIO5 pin must also be configured as DACDAT2.
	2	AIF2_ADCDAT_SRC	0	GPIO7/ADCDAT2 Source select 0 = AIF2 ADCDAT2 1 = GPIO8/DACDAT3 Note that GPIO7 must be configured as ADCDAT2. For selection 1, the GPIO8 pin must also be configured as DACDAT3.
	1	AIF2_DACDAT_SRC	0	AIF2 DACDAT Source select 0 = GPIO5/DACDAT2 1 = GPIO8/DACDAT3 Note that the selected source must be configured as DACDAT2 or DACDAT3.
	0	AIF1_DACDAT_SRC	0	AIF1 DACDAT Source select 0 = DACDAT1 1 = GPIO8/DACDAT3 Note that, for selection 1, the GPIO8 pin must be configured as DACDAT3.

Table 94 Audio Interface AIF3 Configuration

DIGITAL PULL-UP AND PULL-DOWN

The WM8994 provides integrated pull-up and pull-down resistors on each of the DACDAT1, LRCLK1 and BCLK1 pins. This provides a flexible capability for interfacing with other devices. Each of the pull-up and pull-down resistors can be configured independently using the register bits described in Table 95.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1824 (0720h) Digital Pulls	5	DACDAT1_PU	0	DACDAT1 pull-up resistor enable 0 = pull-up disabled 1 = pull-up enabled
	4	DACDAT1_PD	0	DACDAT1 pull-down resistor enable 0 = pull-down disabled 1 = pull-down enabled
	3	DACLRCLK1_PU	0	LRCLK1 pull-up resistor enable 0 = pull-up disabled 1 = pull-up enabled
	2	DACLRCLK1_PD	0	LRCLK1 pull-down resistor enable 0 = pull-down disabled 1 = pull-down enabled
	1	BCLK1_PU	0	BCLK1 pull-up resistor enable 0 = pull-up disabled 1 = pull-up enabled
	0	BCLK1_PD	0	BCLK1 pull-down resistor enable 0 = pull-down disabled 1 = pull-down enabled

Table 95 Digital Pull-Up and Pull-Down Control

CLOCKING AND SAMPLE RATES

The WM8994 requires a clock for each of the Digital Audio Interfaces (AIF1 and AIF2). These may be derived from a common clock reference, or from independent references. Under typical clocking configurations, many commonly-used audio sample rates can be derived directly from the external reference; for additional flexibility, the WM8994 incorporates two Frequency Locked Loop (FLL) circuits perform frequency conversion and filtering.

External clock signals may be connected via MCLK1 and MCLK2. (Note that MCLK2 is an alternate function of the GPIO2 pin.) In AIF Slave modes, the BCLK or LRCLK signals may be used as a reference for the AIF clocks.

The clocks for the Audio Interfaces are referred to as AIF1CLK and AIF2CLK for AIF1 and AIF2 respectively. An additional internal clock, SYSCLK is derived from either AIF1CLK or AIF2CLK in order to support the DSP core functions, Class D switching amplifier, DC servo control, Control Write Sequencer and other internal functions.

The WM8994 provides integrated pull-up and pull-down resistors on the MCLK1 pin. This provides a flexible capability for interfacing with other devices. This is configured as described in Table 100.

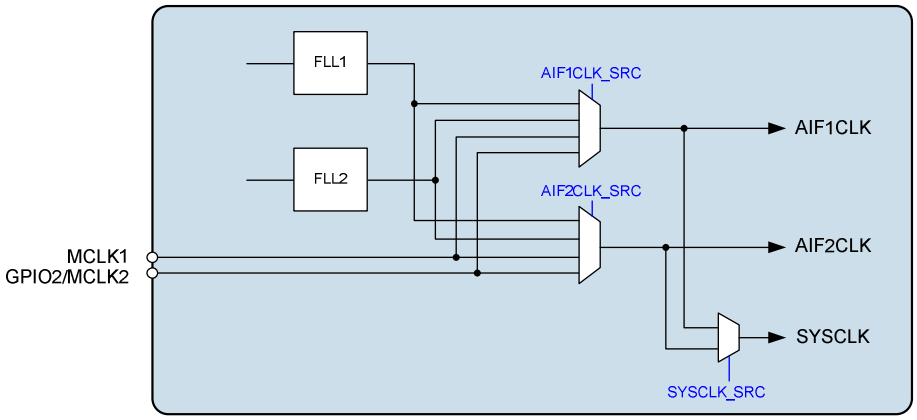


Figure 60 Audio Interface Clock Control

AIF1CLK ENABLE

The AIF1CLK_SRC register is used to select the AIF1CLK source. The source may be MCLK1, MCLK2, FLL1 or FLL2. If either of the Frequency Locked Loops is selected as the source, then the FLL(s) must be enabled and configured as described later.

The AIF1CLK clock may be adjusted by the AIF1CLK_DIV divider, which provides a divide-by-two option. The selected source may also be inverted by setting the AIF1CLK_INV bit.

The AIF1CLK is enabled by the register bit AIF1CLK_ENA. This bit should be set to 0 when reconfiguring the clock sources. It is not recommended to change AIF1CLK_SRC while the AIF1CLK_ENA bit is set.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R512 (0200h) AIF 1 Clocking (1)	4:3	AIF1CLK_SRC	00	AIF1CLK Source Select 00 = MCLK1 01 = MCLK2 10 = FLL1 11 = FLL2
	2	AIF1CLK_INV	0	AIF1CLK Invert 0 = AIF1CLK not inverted 1 = AIF1CLK inverted
	1	AIF1CLK_DIV	0	AIF1CLK Divider 0 = AIF1CLK 1 = AIF1CLK / 2
	0	AIF1CLK_ENA	0	AIF1CLK Enable 0 = Disabled 1 = Enabled

Table 96 AIF1 Clock Enable

AIF1CLK CONFIGURATION

The WM8994 supports a wide range of standard audio sample rates from 8kHz to 96kHz. The AIF1 clocking configuration is selected using 4 control fields, which are set according to the required AIF digital audio sample rate, and the ADC/DAC clocking rate.

The AIF1_SR register is set according to the AIF1 sample rate. Note that 88.2kHz and 96kHz modes are supported for AIF1 input (DAC playback) only.

The AIF1CLK_RATE register is set according to the ratio of AIF1CLK to the AIF1 sample rate. Note that minimum clocking ratios apply, as noted in Table 97.

The audio interface can support different sample rates for the input data (DAC path) and output data (ADC path) simultaneously. In the case, the AIF1_SR and AIF1CLK_RATE fields should be set according to the faster of the two sample rates.

When different sample rates are used for input data (DAC path) and output data (ADC path), the clocking of the slower path is set using AIF1DAC_DIV (if the AIF input path has the slower sample rate) or AIF1ADC_DIV (if the AIF output path has the slower sample rate). The appropriate divider is set according to the ratio of the two sample rates.

For example, if AIF1 input uses 48kHz sample rate, and AIF1 output uses 8kHz, then AIF1ADC_DIV should be set to 110b (divide by 6).

Note that the audio interface cannot support every possible combination of input and output sample rate simultaneously, but only where the ratio of the sample rates matches the available AIF1ADC_DIV or AIF1DAC_DIV divider settings.

Note that the WM8994 performs sample rate conversion, where necessary, to provide digital mixing and interconnectivity between the Audio Interfaces and the DSP Core functions. One stereo Sample Rate Converter (SRC) is provided for audio input; a second stereo SRC is provided for audio output. Each SRC is automatically configured on AIF1 or AIF2, depending on the selected Clocking and Sample Rate settings. The WM8994 cannot support configurations that would require SRC on the input or output paths of both interfaces simultaneously. See “Sample Rate Conversion” for further details.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R513 (0201h) AIF 1 Clocking (2)	5:3	AIF1DAC_DIV	000	Selects the AIF1 input path sample rate relative to AIF1CLK. 000 = AIF1CLK 001 = AIF1CLK / 1.5 010 = AIF1CLK / 2 011 = AIF1CLK / 3 100 = AIF1CLK / 4 101 = AIF1CLK / 5.5 110 = AIF1CLK / 6 111 = Reserved Note that AIF1DAC_DIV must be set to 000 if AIF1ADC_DIV > 000.
	2:0	AIF1ADC_DIV	000	Selects the AIF1 output path sample rate relative to AIF1CLK. 000 = AIF1CLK 001 = AIF1CLK / 1.5 010 = AIF1CLK / 2 011 = AIF1CLK / 3 100 = AIF1CLK / 4 101 = AIF1CLK / 5.5 110 = AIF1CLK / 6 111 = Reserved Note that AIF1ADC_DIV must be set to 000 if AIF1DAC_DIV > 000.
R528 (0210h) AIF1 Rate	7:4	AIF1_SR	1000	Selects the AIF1 Sample Rate (fs) 0000 = 8kHz 0001 = 11.025kHz 0010 = 12kHz 0011 = 16kHz 0100 = 22.05kHz 0101 = 24kHz 0110 = 32kHz 0111 = 44.1kHz 1000 = 48kHz 1001 = 88.2kHz 1010 = 96kHz All other codes = Reserved Note that 88.2kHz and 96kHz modes are supported for AIF1 input (DAC playback) only.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3:0	AIF1CLK_RATE	0011	Selects the AIF1CLK / fs ratio 0000 = 64 0001 = 128 0010 = 192 0011 = 256 0100 = 384 0101 = 512 0110 = 768 0111 = 1024 1000 = 1408 1001 = 1536 All other codes = Reserved For Stereo DAC (AIF1 input) modes, the rate must be 128 x fs or higher. For ADC (AIF1 output) modes, the rate must be 256 x fs or higher.

Table 97 AIF1 Clock Configuration

AIF2CLK ENABLE

The AIF2CLK_SRC register is used to select the AIF2CLK source. The source may be MCLK1, MCLK2, FLL1 or FLL2. If either of the Frequency Locked Loops is selected as the source, then the FLL(s) must be enabled and configured as described later.

The AIF2CLK clock may be adjusted by the AIF2CLK_DIV divider, which provides a divide-by-two option. The selected source may also be inverted by setting the AIF2CLK_INV bit.

The AIF2CLK is enabled by the register bit AIF2CLK_ENA. This bit should be set to 0 when reconfiguring the clock sources. It is not recommended to change AIF2CLK_SRC while the AIF2CLK_ENA bit is set.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R516 (0204h) AIF 2 Clocking (1)	4:3	AIF2CLK_SRC	00	AIF2CLK Source Select 00 = MCLK1 01 = MCLK2 10 = FLL1 11 = FLL2
	2	AIF2CLK_INV	0	AIF2CLK Invert 0 = AIF2CLK not inverted 1 = AIF2CLK inverted
	1	AIF2CLK_DIV	0	AIF2CLK Divider 0 = AIF2CLK 1 = AIF2CLK / 2
	0	AIF2CLK_ENA	0	AIF2CLK Enable 0 = Disabled 1 = Enabled

Table 98 AIF2 Clock Enable

AIF2CLK CONFIGURATION

The WM8994 supports a wide range of standard audio sample rates from 8kHz to 96kHz. The AIF2 clocking configuration is selected using 4 control fields, which are set according to the required AIF digital audio sample rate, and the ADC/DAC clocking rate.

The AIF2_SR register is set according to the AIF2 sample rate. Note that 88.2kHz and 96kHz modes are supported for AIF2 input (DAC playback) only.

The AIF2CLK_RATE register is set according to the ratio of AIF2CLK to the AIF2 sample rate. Note that minimum clocking ratios apply, as noted in Table 99.

The audio interface can support different sample rates for the input data (DAC path) and output data (ADC path) simultaneously. In the case, the AIF2_SR and AIF2CLK_RATE fields should be set according to the faster of the two sample rates.

When different sample rates are used for input data (DAC path) and output data (ADC path), the clocking of the slower path is set using AIF2DAC_DIV (if the AIF input path has the slower sample rate) or AIF2ADC_DIV (if the AIF output path has the slower sample rate). The appropriate divider is set according to the ratio of the two sample rates.

For example, if AIF2 input uses 48kHz sample rate, and AIF2 output uses 8kHz, then AIF2ADC_DIV should be set to 110b (divide by 6).

Note that the audio interface cannot support every possible combination of input and output sample rate simultaneously, but only where the ratio of the sample rates matches the available AIF2ADC_DIV or AIF2DAC_DIV divider settings.

Note that the WM8994 performs sample rate conversion, where necessary, to provide digital mixing and interconnectivity between the Audio Interfaces and the DSP Core functions. One stereo Sample Rate Converter (SRC) is provided for audio input; a second stereo SRC is provided for audio output. Each SRC is automatically configured on AIF1 or AIF2, depending on the selected Clocking and Sample Rate settings. The WM8994 cannot support configurations that would require SRC on the input or output paths of both interfaces simultaneously. See “Sample Rate Conversion” for further details.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R517 (0205h) AIF 2 Clocking (2)	5:3	AIF2DAC_DIV	000	Selects the AIF2 input path sample rate relative to AIF2CLK. 000 = AIF2CLK 001 = AIF2CLK / 1.5 010 = AIF2CLK / 2 011 = AIF2CLK / 3 100 = AIF2CLK / 4 101 = AIF2CLK / 5.5 110 = AIF2CLK / 6 111 = Reserved Note that AIF2DAC_DIV must be set to 000 if AIF2ADC_DIV > 000.
	2:0	AIF2ADC_DIV	000	Selects the AIF2 output path sample rate relative to AIF2CLK. 000 = AIF2CLK 001 = AIF2CLK / 1.5 010 = AIF2CLK / 2 011 = AIF2CLK / 3 100 = AIF2CLK / 4 101 = AIF2CLK / 5.5 110 = AIF2CLK / 6 111 = Reserved Note that AIF2ADC_DIV must be set to 000 if AIF2DAC_DIV > 000.
R529 (0211h) AIF2 Rate	7:4	AIF2_SR	1000	Selects the AIF2 Sample Rate (fs) 0000 = 8kHz 0001 = 11.025kHz 0010 = 12kHz 0011 = 16kHz 0100 = 22.05kHz 0101 = 24kHz 0110 = 32kHz 0111 = 44.1kHz 1000 = 48kHz 1001 = 88.2kHz 1010 = 96kHz All other codes = Reserved Note that 88.2kHz and 96kHz modes are supported for AIF2 input (DAC playback) only.
	3:0	AIF2CLK_RATE	0011	Selects the AIF2CLK / fs ratio 0000 = 64 0001 = 128 0010 = 192 0011 = 256 0100 = 384 0101 = 512 0110 = 768 0111 = 1024 1000 = 1408 1001 = 1536 All other codes = Reserved For Stereo DAC (AIF2 input) modes, the rate must be 128 x fs or higher. For ADC (AIF2 output) modes, the rate must be 256 x fs or higher.

Table 99 AIF2 Clock Configuration

MISCELLANEOUS CLOCK CONTROLS

SYSCLK provides clocking for all the WM8994 that are not supported by either of the Audio Interface clocks. SYSCLK clock is required to support DSP Core functions and also the Class D switching amplifier, DC servo control, Control Write Sequencer and other internal functions.

The SYSCLK_SRC register is used to select the SYSCLK source. The source may be AIF1CLK or AIF2CLK. It is recommended that DSP Core is clocked at the same rate as the active audio interface. If AIF1 and AIF2 are both active then, in most cases, the SYSCLK source should select the faster of the two AIF rates.

The clocking of the WM8994 digital mixer functions is enabled by setting DSP_FSINTCLK_ENA.

The clocking of the AIF1 DSP processing is enabled by setting DSP_FS1CLK_ENA.

The clocking of the AIF2 DSP processing is enabled by setting DSP_FS2CLK_ENA.

Two modes of ADC operation can be selected using the ADC_OSR128 bit; in 48kHz sample mode, setting the ADC_OSR128 bit results in 128x oversampling. This bit is enabled by default, giving best audio performance. De-selecting this bit gives 64x oversampling in 48kHz mode, resulting in decreased power consumption.

A high performance mode of DAC operation can be selected by setting the DAC_OSR128 bit; in 48kHz sample mode, the DAC_OSR128 feature results in 128x oversampling. Audio performance is improved, but power consumption is also increased.

A clock output (OPCLK) derived from SYSCLK may be output on a GPIO pin. This clock is enabled by register big OPCLK_ENA, and its frequency of this clock is controlled by OPCLK_DIV. See General Purpose Input/Output" to configure a GPIO pin for this function.

A slow clock (TOCLK) is derived internally in order to control volume update timeouts when the zero-cross option is selected. This clock is enabled by register bit TOCLK_ENA, and its frequency is controlled by TOCLK_DIV.

A de-bounce control is provided for GPIO inputs and for other functions that may be selected as GPIO outputs. The de-bounced clock frequency is controlled by DBCLK_DIV.

The WM8994 generates a 256kHz clock for internal functions; TOCLK and DBCLK are derived from this 256kHz clock. In order to generate this clock correctly when SYSCLK_SRC = 0, valid settings are required for AIF1_SR and AIF1CLK_RATE. To generate this clock correctly when SYSCLK_SRC = 1, valid settings are required for AIF2_SR and AIF2CLK_RATE.

The WM8994 Clocking is illustrated in Figure 61.

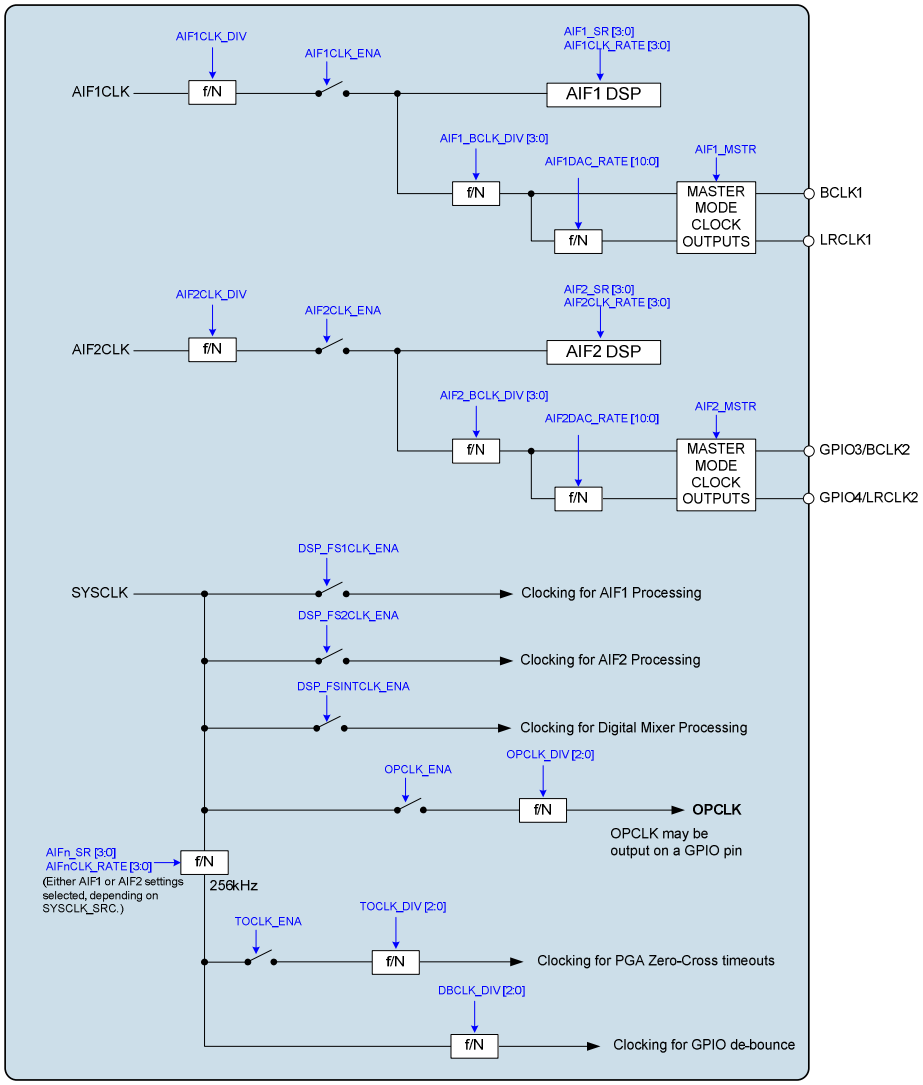


Figure 61 System Clocking

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (0002h) Power Management (2)	11	OPCLK_ENA	0	GPIO Clock Output (OPCLK) Enable 0 = Disabled 1 = Enabled
R520 (0208h) Clocking (1)	4	TOCLK_ENA	0	Slow Clock (TOCLK) Enable 0 = Disabled 1 = Enabled This clock is required for zero-cross timeout.
	3	DSP_FS1CLK_ENA	0	AIF1 Processing Clock Enable 0 = Disabled 1 = Enabled
	2	DSP_FS2CLK_ENA	0	AIF2 Processing Clock Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1	DSP_FSINTCLK_ENA	0	Digital Mixing Processor Clock Enable 0 = Disabled 1 = Enabled
	0	SYSCLK_SRC	0	SYSCLK Source Select 0 = AIF1CLK 1 = AIF2CLK
R521 (0209h) Clocking (2)	10:8	TOCLK_DIV	000	Slow Clock (TOCLK) Divider (Sets TOCLK rate relative to 256kHz.) 000 = Divide by 256 (1kHz) 001 = Divide by 512 (500Hz) 010 = Divide by 1024 (250Hz) 011 = Divide by 2048 (125Hz) 100 = Divide by 4096 (62.5Hz) 101 = Divide by 8192 (31.2Hz) 110 = Divide by 16384 (15.6Hz) 111 = Divide by 32768 (7.8Hz)
	6:4	DBCLK_DIV	000	De-bounce Clock (DBCLK) Divider (Sets DBCLK rate relative to 256kHz.) 000 = Divide by 256 (1kHz) 001 = Divide by 2048 (125Hz) 010 = Divide by 4096 (62.5Hz) 011 = Divide by 8192 (31.2Hz) 100 = Divide by 16384 (15.6Hz) 101 = Divide by 32768 (7.8Hz) 110 = Divide by 65536 (3.9Hz) 111 = Divide by 131072 (1.95Hz)
	2:0	OPCLK_DIV	000	GPIO Output Clock (OPCLK) Divider 0000 = SYSCLK 0001 = SYSCLK / 2 0010 = SYSCLK / 3 0011 = SYSCLK / 4 0100 = SYSCLK / 5.5 0101 = SYSCLK / 6 0110 = SYSCLK / 8 0111 = SYSCLK / 12 1000 = SYSCLK / 16 1001 to 1111 = Reserved
R1568 (0620h) Oversampling	1	ADC_OSR128	1	ADC Oversample Rate Select 0 = Disabled 1 = Enabled For 48kHz sample rate, the ADC oversample rate is 128fs when ADC_OSR128 = 1. The ADC oversample rate is 64fs when ADC_OSR128 = 0.
	0	DAC_OSR128	0	DAC Oversample Rate Select 0 = Disabled 1 = Enabled For 48kHz sample rate, the DAC oversample rate is 128fs when DAC_OSR128 = 1. The DAC oversample rate is 64fs when DAC_OSR128 = 0.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1824 (0720h) Digital Pulls	7	MCLK1_PU	0	MCLK1 pull-up resistor enable 0 = pull-up disabled 1 = pull-up enabled
	6	MCLK1_PD	0	MCLK1 pull-down resistor enable 0 = pull-down disabled 1 = pull-down enabled

Table 100 System Clocking

FREQUENCY LOCKED LOOP (FLL)

Two integrated FLLs are provided to support the clocking requirements of the WM8994. These can be enabled and configured independently according to the available reference clocks and the application requirements. The reference clock may be a high frequency (eg. 12.288MHz) or low frequency (eg. 32.768kHz).

The FLL is tolerant of jitter and may be used to generate a stable AIF clock from a less stable input reference. The FLL characteristics are summarised in “Electrical Characteristics”. Note that the FLL can be used to generate a free-running clock in the absence of an external reference source. This is described in the “Free-Running FLL Clock” section below.

The input reference for FLL1 is selected using FLL1_CLK_REF_SRC. The available options are MCLK1, MCLK2, BCLK1 or LRCLK1. The input reference for FLL2 is selected using FLL2_CLK_REF_SRC. The available options are MCLK1, MCLK2, BCLK2 or LRCLK2. The FLL input reference configuration is illustrated in Figure 62.

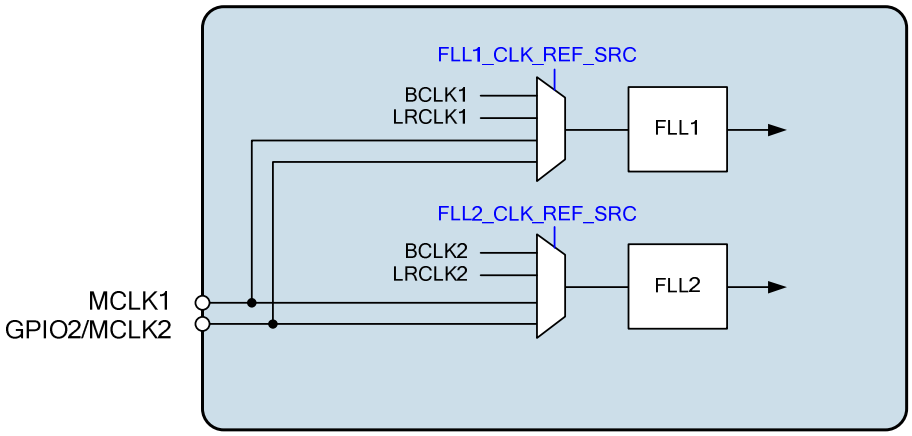


Figure 62 FLL Input Reference Selection

The following description is applicable to FLL1 and FLL2. The associated register control fields are described in Table 103 for FLL1 and Table 104 for FLL2.

The FLL is enabled using the FLL*n*_ENA register bit (where *n* = 1 for FLL1 and *n* = 2 for FLL2). Note that, when changing FLL settings, it is recommended that the digital circuit be disabled via FLL*n*_ENA and then re-enabled after the other register settings have been updated. When changing the input reference frequency F_{REF}, it is recommended that the FLL be reset by setting FLL*n*_ENA to 0.

The field FLL*n*_CLK_REF_DIV provides the option to divide the input reference (MCLK, BCLK or LRCLK) by 1, 2, 4 or 8. This field should be set to bring the reference down to 13.5MHz or below. For best performance, it is recommended that the highest possible frequency - within the 13.5MHz limit - should be selected.

The field FLL*n*_CTRL_RATE controls internal functions within the FLL; it is recommended that only the default setting be used for this parameter. FLL*n*_GAIN controls the internal loop gain and should be set to the recommended value quoted in Table 103.

The FLL output frequency is directly determined from FLL*n*_FRATIO, FLL*n*_OUTDIV and the real number represented by N.K. The integer value N is held in the FLL_N register field (LSB = 1), and is used in both Integer and Fractional Modes. The fractional portion, K, is only valid in Fractional Mode when enabled by the field FLL*n*_FRACN_ENA.

It is recommended that FLL*n*_FRACN_ENA is enabled at all times. Power consumption in the FLL is reduced in integer mode; however, the performance may also be reduced, with increased noise or jitter on the output.

If low power consumption is required, then FLL settings must be chosen where N.K is an integer (ie. FLL*n*_K = 0). In this case, the fractional mode can be disabled by setting FLL*n*_FRACN_ENA = 0.

For best FLL performance, a non-integer value of N.K is required, and fractional mode must be enabled by setting FLL*n*_FRACN_ENA = 1. The FLL settings must be adjusted, if necessary, to produce a non-integer value of N.K.

The FLL output frequency is generated according to the following equation:

$$F_{OUT} = (F_{VCO} / FLLn\_OUTDIV)$$

The FLL operating frequency, F_{VCO} is set according to the following equation:

$$F_{VCO} = (F_{REF} \times N.K \times FLLn\_FRATIO)$$

F_{REF} is the input frequency, as determined by FLL*n*_CLK_REF_DIV.

F_{VCO} must be in the range 90-100 MHz. Frequencies outside this range cannot be supported.

Note that the output frequencies that do not lie within the ranges quoted above cannot be guaranteed across the full range of device operating temperatures.

In order to follow the above requirements for F_{VCO}, the value of FLL*n*_OUTDIV should be selected according to the desired output F_{OUT}. The divider, FLL*n*_OUTDIV, must be set so that F_{VCO} is in the range 90-100MHz. The available divisions are integers from 4 to 64. Some typical settings of FLL*n*_OUTDIV are noted in Table 101.

OUTPUT FREQUENCY F_{OUT}	FLL*n*_OUTDIV
2.8125 MHz - 3.125 MHz	100000 (divide by 32)
3.75 MHz - 4.1667 MHz	011000 (divide by 24)
5.625 MHz - 6.25 MHz	001111 (divide by 16)
11.25 MHz - 12.5 MHz	000111 (divide by 8)
18 MHz - 20 MHz	000100 (divide by 5)
22.5 MHz - 25 MHz	000011 (divide by 4)

Table 101 Selection of FLL*n*_OUTDIV

The value of FLL_FRATIO should be selected as described in Table 102.

REFERENCE FREQUENCY F_{REF}	FLL*n*_FRATIO
1MHz - 13.5MHz	0h (divide by 1)
256kHz - 1MHz	1h (divide by 2)
128kHz - 256kHz	2h (divide by 4)
64kHz - 128kHz	3h (divide by 8)
Less than 64kHz	4h (divide by 16)

Table 102 Selection of FLL*n*_FRATIO

In order to determine the remaining FLL parameters, the FLL operating frequency, F_{VCO}, must be calculated, as given by the following equation:

$$F_{VCO} = (F_{OUT} \times FLLn\_OUTDIV)$$

The value of FLL*n*_N and FLL*n*_K can then be determined as follows:

$$N.K = F_{VCO} / (FLLn\_FRATIO \times F_{REF})$$

Note that F_{REF} is the input frequency, after division by FLL*n*_CLK_REF_DIV, where applicable.

In FLL Fractional Mode, the fractional portion of the N.K multiplier is held in the FLL*n*_K register field. This field is coded as a fixed point quantity, where the MSB has a weighting of 0.5. Note that, if desired, the value of this field may be calculated by multiplying K by 2^{16} and treating FLL*n*_K as an integer value, as illustrated in the following example:

If N.K = 8.192, then K = 0.192

Multiplying K by 2^{16} gives 0.192 x 65536 = 12582.912 (decimal)

Apply rounding to the nearest integer = 12583 (decimal) = 3127 (hex)

For best performance, FLL Fractional Mode should always be used. Therefore, if the calculations yield an integer value of N.K, then it is recommended to adjust FLL*n*_OUTDIV in order to obtain a non-integer value of N.K. Care must always be taken to ensure that the FLL operating frequency, F_{VCO}, is within its recommended limits of 90-100 MHz.

The FLL1 control registers are described in Table 103. The FLL2 control registers are described in Table 104. Example settings for a variety of reference frequencies and output frequencies are shown in Table 106.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R544 (0220h) FLL1 Control (1)	2	FLL1_FRACN_ENA	0	FLL1 Fractional enable 0 = Integer Mode 1 = Fractional Mode Fractional Mode (FLL1_FRACN_ENA=1 is recommended in all cases)
	0	FLL1_ENA	0	FLL1 Enable 0 = Disabled 1 = Enabled
R545 (0221h) FLL1 Control (2)	13:8	FLL1_OUTDIV [5:0]	000000	FLL1 F_{OUT} clock divider 000000 = Reserved 000001 = Reserved 000010 = Reserved 000011 = 4 000100 = 5 000101 = 6 … 111110 = 63 111111 = 64 ($F_{OUT} = F_{VCO}$ / FLL1_OUTDIV)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	6:4	FLL1_CTRL_RATE [2:0]	000	Frequency of the FLL1 control block 000 = F_{VCO} / 1 (Recommended value) 001 = F_{VCO} / 2 010 = F_{VCO} / 3 011 = F_{VCO} / 4 100 = F_{VCO} / 5 101 = F_{VCO} / 6 110 = F_{VCO} / 7 111 = F_{VCO} / 8 Recommended that these are not changed from default.
	2:0	FLL1_FRATIO [2:0]	000	FLL1 F_{VCO} clock divider 000 = 1 001 = 2 010 = 4 011 = 8 1XX = 16 000 recommended for high F_{REF} 011 recommended for low F_{REF}
R546 (0222h) FLL1 Control (3)	15:0	FLL1_K[15:0]	0000h	FLL1 Fractional multiply for F_{REF} (MSB = 0.5)
R547 (0223h) FLL1 Control (4)	14:5	FLL1_N[9:0]	000h	FLL1 Integer multiply for F_{REF} (LSB = 1)
	3:0	FLL1_GAIN [3:0]	0000	FLL1 Gain applied to error 0000 = x 1 (Recommended value) 0001 = x 2 0010 = x 4 0011 = x 8 0100 = x 16 0101 = x 32 0110 = x 64 0111 = x 128 1000 = x 256 Recommended that these are not changed from default.
R548 (0224h) FLL1 Control (5)	4:3	FLL1_CLK_REF_DIV [1:0]	00	FLL1 Clock Reference Divider 00 = MCLK / 1 01 = MCLK / 2 10 = MCLK / 4 11 = MCLK / 8 MCLK (or other input reference) must be divided down to <=13.5MHz. For lower power operation, the reference clock can be divided down further if desired.
	1:0	FLL1_CLK_REF_SRC [1:0]	00	FLL1 Clock source 00 = MCLK1 01 = MCLK2 10 = LRCLK1 11 = BCLK1

Table 103 FLL1 Register Map

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R576 (0240h) FLL2 Control (1)	2	FLL2_FRACN_ENA	0	FLL2 Fractional enable 0 = Integer Mode 1 = Fractional Mode Fractional Mode (FLL2_FRACN_ENA=1 is recommended in all cases)
	0	FLL2_ENA	0	FLL2 Enable 0 = Disabled 1 = Enabled
R577 (0241h) FLL2 Control (2)	13:8	FLL2_OUTDIV [5:0]	000000	FLL2 F_{OUT} clock divider 000000 = Reserved 000001 = Reserved 000010 = Reserved 000011 = 4 000100 = 5 000101 = 6 … 111110 = 63 111111 = 64 (F_{OUT} = F_{VCO} / FLL2_OUTDIV)
	6:4	FLL2_CTRL_RATE [2:0]	000	Frequency of the FLL2 control block 000 = F_{VCO} / 1 (Recommended value) 001 = F_{VCO} / 2 010 = F_{VCO} / 3 011 = F_{VCO} / 4 100 = F_{VCO} / 5 101 = F_{VCO} / 6 110 = F_{VCO} / 7 111 = F_{VCO} / 8 Recommended that these are not changed from default.
	2:0	FLL2_FRATIO [2:0]	000	FLL2 F_{VCO} clock divider 000 = 1 001 = 2 010 = 4 011 = 8 1XX = 16 000 recommended for high F_{REF} 011 recommended for low F_{REF}
R578 (0242h) FLL2 Control (3)	15:0	FLL2_K[15:0]	0000h	FLL2 Fractional multiply for F_{REF} (MSB = 0.5)
R579 (0243h) FLL2 Control (4)	14:5	FLL2_N[9:0]	000h	FLL2 Integer multiply for F_{REF} (LSB = 1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3:0	FLL2_GAIN [3:0]	0000	FLL2 Gain applied to error 0000 = x 1 (Recommended value) 0001 = x 2 0010 = x 4 0011 = x 8 0100 = x 16 0101 = x 32 0110 = x 64 0111 = x 128 1000 = x 256 Recommended that these are not changed from default.
R580 (0244h) FLL2 Control (5)	4:3	FLL2_CLK_REF _DIV [1:0]	00	FLL2 Clock Reference Divider 00 = MCLK / 1 01 = MCLK / 2 10 = MCLK / 4 11 = MCLK / 8 MCLK (or other input reference) must be divided down to <=13.5MHz. For lower power operation, the reference clock can be divided down further if desired.
	1:0	FLL2_CLK_REF _SRC [1:0]	00	FLL2 Clock source 00 = MCLK1 01 = MCLK2 10 = LRCLK2 11 = BCLK2

Table 104 FLL2 Register Map

FREE-RUNNING FLL CLOCK

The FLL can generate a clock signal even when no external reference is available. However, it should be noted that the accuracy of this clock is reduced, and a reference source should always be used where possible. Note that, in free-running modes, the FLL is not sufficiently accurate for hi-fi ADC or DAC applications. However, the free-running modes are suitable for clocking most other functions, including the Write Sequencer, Charge Pump, DC Servo and Class D loudspeaker driver.

If an accurate reference clock is initially available, then the FLL should be configured as described above. The FLL will continue to generate a stable output clock after the reference input is stopped or disconnected.

If no reference clock is available at the time of starting up the FLL, then an internal clock frequency of approximately 12MHz can be generated by implementing the following sequence:

- Enable the FLL Analogue Oscillator (FLLn_OSC_ENA = 1)
- Set the F_{OUT} clock divider to divide by 8 (FLLn_OUTDIV = 000111)
- Configure the oscillator frequency by setting FLLn_FRC_NCO = 1 and FLLn_FRC_NCO_VAL = 19h

Note that the free-running FLL mode is not suitable for hi-fi CODEC applications. In the absence of any reference clock, the FLL output is subject to a very wide tolerance; see “Electrical Characteristics” for details of the FLL accuracy.

Note that the free-running FLL clock is selected as SYSCLK using the registers noted in Figure 62.

The free-running FLL clock may be used to support analogue functions, for which the digital audio interface is not used, and there is no applicable Sample Rate (fs). When SYSCLK is required for circuits such the Class D, DC Servo, Control Write Sequencer or Charge Pump, then valid Sample Rate register settings are still required, even though the digital audio interface is not active.

For correct functionality when SYSCLK_SRC = 0, valid settings are required for AIF1_SR and AIF1CLK_RATE. In the case where SYSCLK_SRC = 1, then valid settings are required for AIF2_SR and AIF2CLK_RATE.

The control registers applicable to FLL free-running modes are described in Table 105.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R544 (0220h) FLL1 Control (1)	1	FLL1_OSC_ENA	0	FLL1 Oscillator enable 0 = Disabled 1 = Enabled (Note that this field is required for free-running FLL1 modes only)
R548 (0224h) FLL1 Control (5)	12:7	FLL1_FRC_NCO_VAL	19h	FLL1 Forced oscillator value Valid range is 000000 to 111111 0x19h (011001) = 12MHz approx (Note that this field is required for free-running FLL modes only)
	6	FLL1_FRC_NCO	0	FLL1 Forced control select 0 = Normal 1 = FLL1 oscillator controlled by FLL1_FRC_NCO_VAL (Note that this field is required for free-running FLL modes only)
R576 (0240h) FLL2 Control (1)	1	FLL2_OSC_ENA	0	FLL2 Oscillator enable 0 = Disabled 1 = Enabled (Note that this field is required for free-running FLL2 modes only)
	12:7	FLL2_FRC_NCO_VAL	19h	FLL2 Forced oscillator value Valid range is 000000 to 111111 0x19h (011001) = 12MHz approx (Note that this field is required for free-running FLL modes only)
R580 (0244h) FLL2 Control (5)	6	FLL2_FRC_NCO	0	FLL2 Forced control select 0 = Normal 1 = FLL2 oscillator controlled by FLL2_FRC_NCO_VAL (Note that this field is required for free-running FLL modes only)

Table 105 FLL Free-Running Mode

EXAMPLE FLL CALCULATION

The following example illustrates how to derive the FLL1 registers to generate 12.288 MHz output (F_{OUT}) from a 12.000 MHz reference clock (F_{REF}):

- Set FLL1_CLK_REF_DIV in order to generate F_{REF} <=13.5MHz:
  FLL1_CLK_REF_DIV = 00 (divide by 1)
- Set FLL1_CTRL_RATE to the recommended setting:
  FLL1_CTRL_RATE = 000 (divide by 1)
- Sett FLL1_GAIN to the recommended setting:
  FLL1_GAIN = 0000 (multiply by 1)

- Set FLL1_OUTDIV for the required output frequency as shown in Table 101:-
  F_{OUT} = 12.288 MHz, therefore FLL1_OUTDIV = 17h (divide by 8)
- Set FLL1_FRATIO for the given reference frequency as shown in Table 102:
  F_{REF} = 12MHz, therefore FLL1_FRATIO = 0h (divide by 1)
- Calculate F_{VCO} as given by $F_{VCO} = F_{OUT}$ x FLL1_OUTDIV:-
  F_{VCO} = 12.288 x 8 = 98.304MHz
- Calculate N.K as given by N.K = F_{VCO} / (FLL1_FRATIO x F_{REF}):
  N.K = 98.304 / (1 x 12) = 8.192
- Determine FLL1_N and FLL1_K from the integer and fractional portions of N.K:-
  FLL1_N is 8. FLL1_K is 0.192
- Confirm that N.K is a fractional quantity and set FLL1_FRACN_ENA:
  N.K is fractional. Set FLL1_FRACN_ENA = 1.
  Note that, if N.K is an integer, then an alternative value of FLL1_OUTDIV should be selected in order to produce a fractional value of N.K.
- Convert FLL1_K into integer format:
  0.192 x 65536 = 12582.912 (decimal).
- Round off to 12583 (decimal) and convert to hex:
  12583 (decimal) = 3127 (hex).
  FLL1_K = 3127h

EXAMPLE FLL SETTINGS

Table 106 provides example FLL settings for generating common SYSCLK frequencies from a variety of low and high frequency reference inputs.

F_{REF}	F_{OUT}	FLL*n*_CLK_REF_DIV	F_{VCO}	FLL*n*_N	FLL*n*_K	FLL*n*_FRATIO	FLL*n*_OUTDIV	FLL*n*_FRACN_ENA
32.000 kHz	12.288 MHz	Divide by 1 (0h)	98.304 MHz	384 (180h)	0 (0000h)	8 (3h)	8 (17h)	0
32.000 kHz	11.2896 MHz	Divide by 1 (0h)	90.3168 MHz	352 (160h)	0.8 (CCCCh)	8 (3h)	8 (17h)	1
32.768 kHz	12.288 MHz	Divide by 1 (0h)	98.304 MHz	187 (0BBh)	0.5 (8000h)	16 (4h)	8 (17h)	1
32.768 kHz	11.288576 MHz	Divide by 1 (0h)	90.308608 MHz	344 (158h)	0.5 (8000h)	8 (3h)	8 (17h)	1
32.768 kHz	11.2896 MHz	Divide by 1 (0h)	90.3168 MHz	344 (158h)	0.53125 (8800h)	8 (3h)	8 (17h)	1
48 kHz	12.288 MHz	Divide by 1 (0h)	98.304 MHz	256 (100h)	0 (0000h)	8 (3h)	8 (17h)	0
11.3636 MHz	12.368544 MHz	Divide by 1 (0h)	98.948354 MHz	8 (008h)	0.707483 (B51Dh)	1 (0h)	8 (17h)	1
12.000 MHz	12.288 MHz	Divide by 1 (0h)	98.3040 MHz	8 (008h)	0.192 (3126h)	1 (0h)	8 (17h)	1
12.000 MHz	11.289597 MHz	Divide by 1 (0h)	90.3168 MHz	7 (007h)	0.526398 (86C2h)	1 (0h)	8 (17h)	1
12.288 MHz	12.288 MHz	Divide by 1 (0h)	98.304 MHz	8 (008h)	0 (0000h)	1 (0h)	8 (17h)	0
12.288 MHz	11.2896 MHz	Divide by 1 (0h)	90.3168 MHz	7 (007h)	0.35 (599Ah)	1 (0h)	8 (17h)	1
13.000 MHz	12.287990 MHz	Divide by 1 (0h)	98.3040 MHz	7 (007h)	0.56184 (8FD5h)	1 (0h)	8 (17h)	1
13.000 MHz	11.289606 MHz	Divide by 1 (0h)	90.3168 MHz	6 (006h)	0.94745 (F28Ch)	1 (0h)	8 (17h)	1
19.200 MHz	12.287988 MHz	Divide by 2 (1h)	98.3039 MHz	10 (00Ah)	0.23999 (3D70h)	1 (0h)	8 (17h)	1
19.200 MHz	11.289588 MHz	Divide by 2 (1h)	90.3168 MHz	9 (009h)	0.40799 (6872h)	1 (0h)	8 (17h)	1

Table 106 Example FLL Settings

CONTROL INTERFACE

The WM8994 is controlled by writing to its control registers. Readback is available for all registers. The Control Interface can operate as either a 2-, 3- or 4-wire interface:

- 2-wire (I2C) mode uses pins SCLK and SDA
- 3-wire (SPI) mode uses pins $\overline{CS}$/ADDR, SCLK and SDA
- 4-wire (SPI) mode uses pins $\overline{CS}$/ADDR, SCLK, SDA and SDOUT

Readback is provided on the bi-directional pin SDA in 2-/3-wire modes. In 4-wire mode, the SDOUT function must be enabled on one of the GPIO pins (see "General Purpose Input/Output").

The WM8994 uses 15-bit register addresses and 16-bit data in all Control Interface modes.

SELECTION OF CONTROL INTERFACE MODE

The WM8994 Control Interface Mode is determined by the logic level on the CIFMODE pin, as shown in Table 107.

CIFMODE	INTERFACE FORMAT
Low	2 wire (I2C) Mode
High	3- or 4- wire (SPI) Modes

Table 107 Control Interface Mode Selection

In 2-wire (I2C) Control Interface mode, Auto-Increment mode may be selected. This enables multiple write and multiple read operations to be scheduled faster than is possible with single register operations. The auto-increment option is enabled when the AUTO_INC register bit is set. This bit is defined in Table 108. Auto-increment is disabled by default.

In SPI modes, 3-wire or 4-wire operation may be selected using the SPI_4WIRE register bit.

In 3-wire (SPI) mode, register readback is provided using the bi-directional pin SDA. During data output, the SDA pin can be configured as CMOS or Open Drain, using the SPI_CFG register bit.

In 4-wire (SPI) mode, register readback is provided using SDOUT. The SDOUT pin may be configured as CMOS or as 'Wired OR' using the SPI_CFG bit. In CMOS mode, SDOUT is driven low when not outputting register data. In 'Wired OR' mode, SDOUT is undriven (high impedance) when not outputting register data bits.

The Control Interface configuration bits are described in Table 108.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R257 (0101h) Control Interface	5	SPI_4WIRE	1	SPI control mode select 0 = 3-wire using bidirectional SDA 1 = 4-wire using SDOUT
	4	SPI_CFG	0	SDA/SDOUT pin configuration 0 = CMOS 1 = Open Drain (SPI_4WIRE = 0) 1 = Wired 'OR' (SPI_4WIRE = 1)
	2	AUTO_INC	1	Enables address auto-increment (applies to 2-wire I2C mode only) 0 = Disabled 1 = Enabled

Table 108 Control Interface Configuration

2-WIRE (I2C) CONTROL MODE

In 2-wire (I2C) mode, the WM8994 is a slave device on the control interface; SCLK is a clock input, while SDAT is a bi-directional data pin. To allow arbitration of multiple slaves (and/or multiple masters) on the same interface, the WM8994 transmits logic 1 by tri-stating the SDAT pin, rather than pulling it high. An external pull-up resistor is required to pull the SDAT line high so that the logic 1 can be recognised by the master.

In order to allow many devices to share a single 2-wire control bus, every device on the bus has a unique 7-bit device ID (this is not the same as the 8-bit address of each register in the WM8994). The device ID is selectable on the WM8994, using the CS/ADDR pin as shown in Table 109. The LSB of the Device ID is the Read/Write bit; this bit is set to logic 1 for "Read" and logic 0 for "Write".

CS/ADDR	DEVICE ID
Low	0011 0100 (34h)
High	0011 0110 (36h)

Table 109 Control Interface Device ID Selection

The WM8994 operates as a slave device only. The controller indicates the start of data transfer with a high to low transition on SDAT while SCLK remains high. This indicates that a device ID, register address and data will follow. The WM8994 responds to the start condition and shifts in the next eight bits on SDAT (7-bit device ID + Read/Write bit, MSB first). If the device ID received matches the device ID of the WM8994, then the WM8994 responds by pulling SDAT low on the next clock pulse (ACK). If the device ID is not recognised or the R/W bit is '1' when operating in write only mode, the WM8994 returns to the idle condition and waits for a new start condition and valid address.

If the device ID matches the device ID of the WM8994, the data transfer continues as described below. The controller indicates the end of data transfer with a low to high transition on SDAT while SCKL remains high. After receiving a complete address and data sequence the WM8994 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDAT changes while SCLK is high), the device returns to the idle condition.

The WM8994 supports the following read and write operations:

- Single write
- Single read
- Multiple write using auto-increment
- Multiple read using auto-increment

The sequence of signals associated with a single register write operation is illustrated in Figure 63.

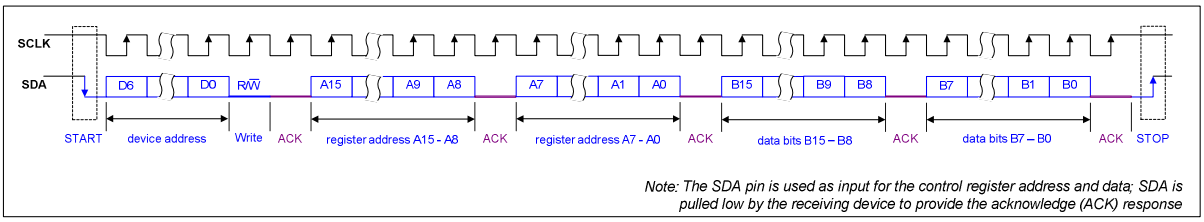


Figure 63 Control Interface 2-wire (I2C) Register Write

The sequence of signals associated with a single register read operation is illustrated in Figure 64.

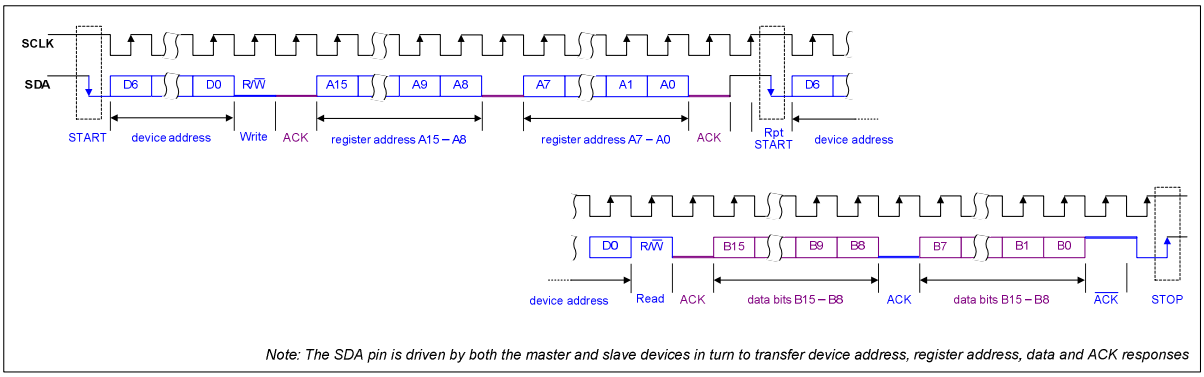


Figure 64 Control Interface 2-wire (I2C) Register Read

The Control Interface also supports other register operations, as listed above. The interface protocol for these operations is summarised below. The terminology used in the following figures is detailed in Table 110.

Note that, for multiple write and multiple read operations, the auto-increment option must be enabled. This feature is enabled by default, as noted in Table 108.

TERMINOLOGY	DESCRIPTION	
S	Start Condition	
Sr	Repeated start	
A	Acknowledge	
P	Stop Condition	
R/$\overline{W}$	ReadNotWrite	0 = Write 1 = Read
[White field]	Data flow from bus master to WM8994	
[Grey field]	Data flow from WM8994 to bus master	

Table 110 Control Interface Terminology

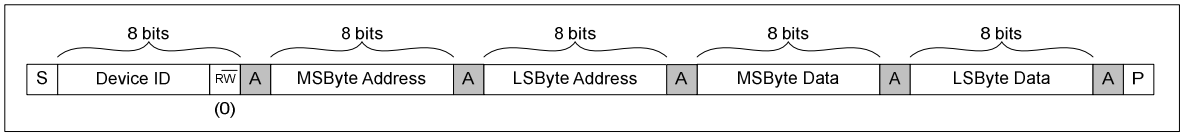


Figure 65 Single Register Write to Specified Address

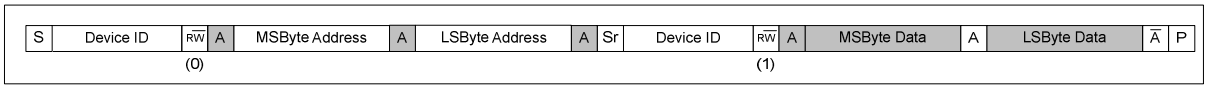


Figure 66 Single Register Read from Specified Address

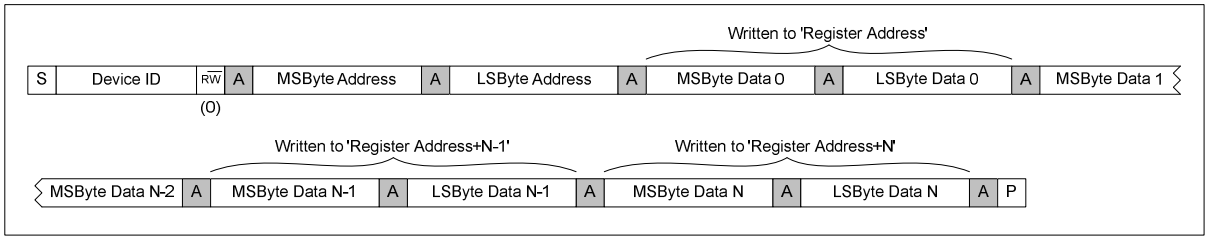


Figure 67 Multiple Register Write to Specified Address using Auto-increment

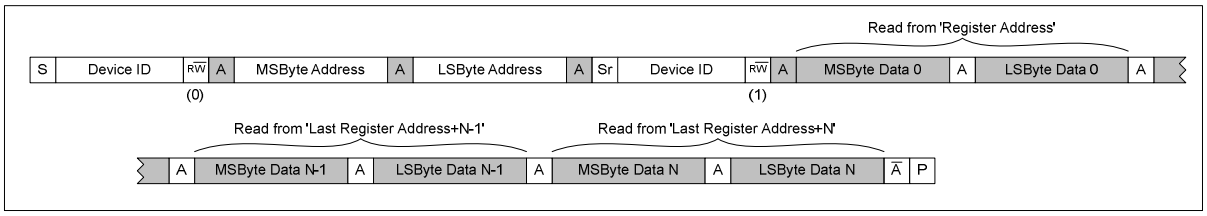


Figure 68 Multiple Register Read from Specified Address using Auto-increment

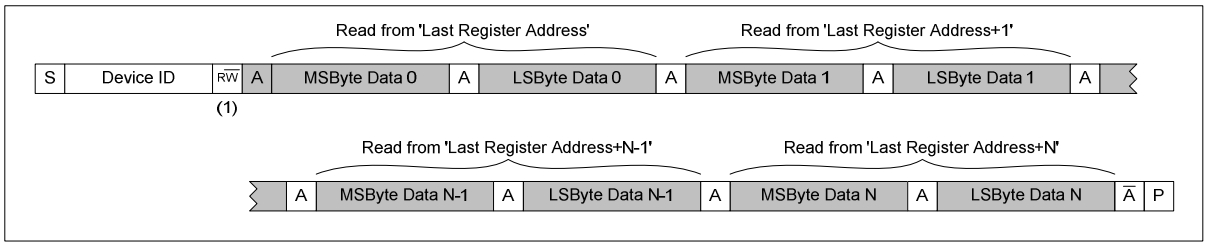


Figure 69 Multiple Register Read from Last Address using Auto-increment

Multiple Write and Multiple Read operations enable the host processor to access sequential blocks of the data in the WM8994 register map faster than is possible with single register operations. The auto-increment option is enabled when the AUTO_INC register bit is set. This bit is defined in Table 108. Auto-increment is enabled by default.

3-WIRE (SPI) CONTROL MODE

The 3-wire control interface uses the $\overline{CS}$, SCLK and SDA pins.

In 3-wire control mode, a control word consists of 32 bits. The first bit is the read/write bit (R/W), which is followed by 15 address bits (A14 to A0) that determine which control register is accessed. The remaining 16 bits (B15 to B0) are data bits, corresponding to the 16 bits in each control register.

In 3-wire mode, every rising edge of SCLK clocks in one data bit from the SDA pin. A rising edge on $\overline{CS}$ latches in a complete control word consisting of the last 32 bits.

In Write operations (R/W=0), all SDA bits are driven by the controlling device.

In Read operations (R/W=1), the SDA pin is driven by the controlling device to clock in the register address, after which the WM8994 drives the SDA pin to output the applicable data bits.

During data output, the SDA pin can be configured as CMOS or Open Drain, using the SPI_CFG register bit, as described in Table 108. In Open Drain configuration, an external pull-up resistor is required to pull the SDA line high so that the logic 1 can be recognised by the master.

The 3-wire control mode timing is illustrated in Figure 70.

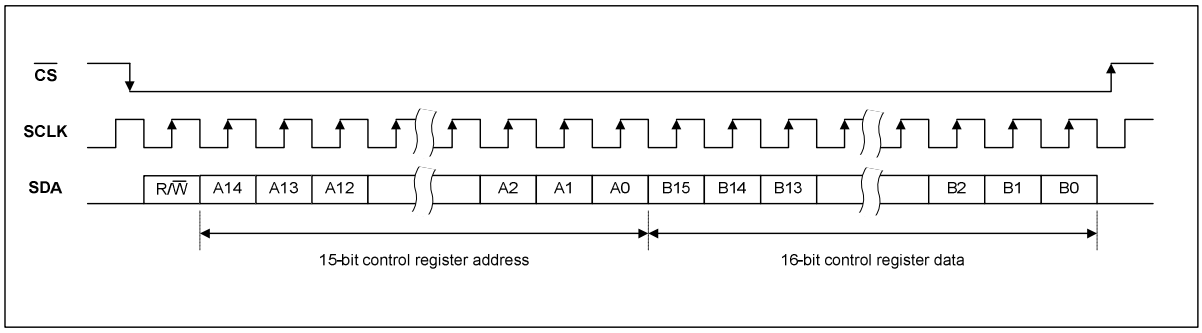


Figure 70 3-Wire Serial Control Interface

4-WIRE (SPI) CONTROL MODE

The 4-wire control interface uses the $\overline{CS}$, SCLK, SDA and SDOUT pins.

The SDOUT function must be enabled on one of the GPIO pins (see "General Purpose Input/Output").

The Data Output pin, SDOUT, can be configured as CMOS or 'Wired OR', as described in Table 108. In CMOS mode, SDOUT is driven low when not outputting register data bits. In 'Wired OR' mode, SDOUT is undriven (high impedance) when not outputting register data bits.

In Write operations (R/W=0), this mode is the same as 3-wire mode described above.

In Read operations (R/W=1), the SDATA pin is ignored following receipt of the valid register address. SDOUT is driven by the WM8994.

The 4-wire control mode timing is illustrated in Figure 71 and Figure 72.

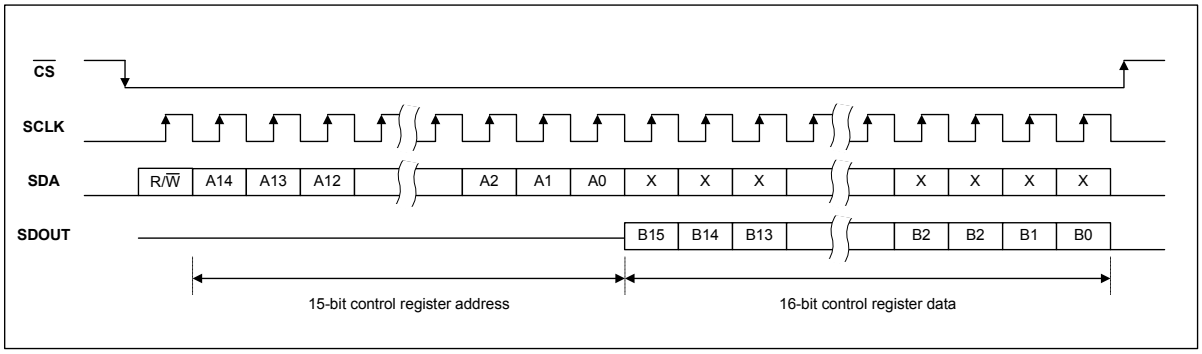


Figure 71 4-Wire Readback (CMOS)

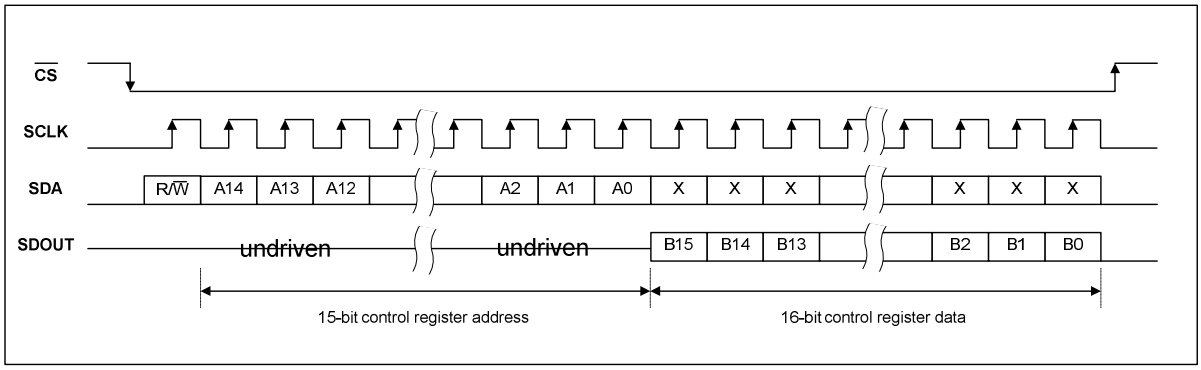


Figure 72 4-Wire Readback (Wired-'OR')

CONTROL WRITE SEQUENCER

The Control Write Sequencer is a programmable unit that forms part of the WM8994 control interface logic. It provides the ability to perform a sequence of register write operations with the minimum of demands on the host processor - the sequence may be initiated by a single operation from the host processor and then left to execute independently.

Default sequences for Start-Up of each output driver and Shut-Down are provided (see “Default Sequences” section). It is recommended that these default sequences are used unless changes become necessary.

When a sequence is initiated, the sequencer performs a series of pre-defined register writes. The host processor informs the sequencer of the start index of the required sequence within the sequencer’s memory. At each step of the sequence, the contents of the selected register fields are read from the sequencer’s memory and copied into the WM8994 control registers. This continues sequentially through the sequencer’s memory until an “End of Sequence” bit is encountered; at this point, the sequencer stops and an Interrupt status flag is asserted. For cases where the timing of the write sequence is important, a programmable delay can be set for specific steps within the sequence.

Note that the Control Write Sequencer’s internal clock is derived from the internal clock SYS_CLK which must be enabled as described in “Clocking and Sample Rates”. The clock division from SYS_CLK is handled transparently by the WM8994 without user intervention, provided that SYS_CLK is configured as specified in “Clocking and Sample Rates”.

INITIATING A SEQUENCE

The Register fields associated with running the Control Write Sequencer are described in Table 111. Note that the operation of the Control Write Sequencer also requires the internal clock SYS_CLK to be configured as described in “Clocking and Sample Rates”.

The Write Sequencer is enabled by setting the WSEQ_ENA bit. The start index of the required sequence must be written to the WSEQ_START_INDEX field.

The Write Sequencer stores up to 128 register write commands. These are defined in Registers R12288 to R12799. There are 4 registers used to define each of the 128 possible commands. The value of WSEQ_START_INDEX selects the registers applicable to the first write command in the selected sequence.

Setting the WSEQ_START bit initiates the sequencer at the given start index. The Write Sequencer can be interrupted by writing a logic 1 to the WSEQ_ABORT bit.

The current status of the Write Sequencer can be read using two further register fields - when the WSEQ_BUSY bit is asserted, this indicates that the Write Sequencer is busy. Note that, whilst the Control Write Sequencer is running a sequence (indicated by the WSEQ_BUSY bit), normal read/write operations to the Control Registers cannot be supported. The index of the current step in the Write Sequencer can be read from the WSEQ_CURRENT_INDEX field; this is an indicator of the sequencer’s progress. On completion of a sequence, this field holds the index of the last step within the last commanded sequence.

When the Write Sequencer reaches the end of a sequence, it asserts the WSEQ_DONE_EINT flag in Register R1841 (see Table 79). This flag can be used to generate an Interrupt Event on completion of the sequence. Note that the WSEQ_DONE_EINT flag is asserted to indicate that the WSEQ is NOT Busy.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R272 (0110h) Write Sequencer Ctrl (1)	15	WSEQ_ENA	0	Write Sequencer Enable. 0 = Disabled 1 = Enabled
	9	WSEQ_ABORT	0	Writing a 1 to this bit aborts the current sequence and returns control of the device back to the serial control interface.
	8	WSEQ_START	0	Writing a 1 to this bit starts the write sequencer at the index location selected by WSEQ_START_INDEX. The sequence continues until it reaches an "End of sequence" flag. At the end of the sequence, this bit will be reset by the Write Sequencer.
	6:0	WSEQ_START_INDEX [6:0]	000_0000	Sequence Start Index. This field determines the memory location of the first command in the selected sequence. There are 127 Write Sequencer RAM addresses: 00h = WSEQ_ADDR0 (R12288) 01h = WSEQ_ADDR1 (R12292) 02h = WSEQ_ADDR2 (R12296) …. 7Fh = WSEQ_ADDR127 (R12796)
R273 (0111h) Write Sequencer Ctrl (2)	8	WSEQ_BUSY (read only)	0	Sequencer Busy flag (Read Only). 0 = Sequencer idle 1 = Sequencer busy Note: it is not possible to write to control registers via the control interface while the Sequencer is Busy.
	6:0	WSEQ_CURRENT_INDEX [6:0] (read only)	000_0000	Sequence Current Index. This indicates the memory location of the most recently accessed command in the write sequencer memory. Coding is the same as WSEQ_START_INDEX.

Table 111 Write Sequencer Control - Initiating a Sequence

PROGRAMMING A SEQUENCE

A sequence consists of write operations to data bits (or groups of bits) within the control registers. Each write operation is defined by a block of 4 registers, which contain 6 fields as described in this section.

The block of 4 registers is the same for up to 128 steps held in the sequencer memory. Multiple sequences can be held in the memory at the same time; each sequence occupies its own range within the 128 available registers.

The following 6 fields are replicated 128 times - one for each of the sequencer's 128 steps. In the following descriptions, the term '*n*' is used to denote the step number, from 0 to 127.

WSEQ_ADDR*n* is a 14-bit field containing the Control Register Address in which the data should be written.

WSEQ_DATA*n* is an 8-bit field which contains the data to be written to the selected Control Register. The WSEQ_DATA_WIDTH*n* field determines how many of these bits are written to the selected register; the most significant bits (above the number indicated by WSEQ_DATA_WIDTH*n*) are ignored.

WSEQ_DATA_START*n* is a 4-bit field which identifies the LSB position within the selected Control Register to which the data should be written. For example, setting WSEQ_DATA_START*n* = 0100 will select bit 4 as the LSB position; in this case, 4-bit data would be written to bits 7:4.

WSEQ_DATA_WIDTH*n* is a 3-bit field which identifies the width of the data block to be written. This enables selected portions of a Control Register to be updated without any concern for other bits within the same register, eliminating the need for read-modify-write procedures. Values of 0 to 7 correspond to data widths of 1 to 8 respectively. For example, setting WSEQ_DATA_WIDTH*n* = 010 will cause a 3-bit data block to be written. Note that the maximum value of this field corresponds to an 8-bit data block; writing to register fields greater than 8 bits wide must be performed using two separate operations of the Control Write Sequencer.

WSEQ_DELAY*n* is a 4-bit field which controls the waiting time between the current step and the next step in the sequence i.e. the delay occurs after the write in which it was called. The total delay time per step (including execution) is defined below, giving a useful range of execution/delay times from 562µs up to 2.048s per step:

$$T = k \times (2^{WSEQ\_DELAY} + 8)$$

where k = 62.5µs (under recommended operating conditions)

WSEQ_EOS*n* is a 1-bit field which indicates the End of Sequence. If this bit is set, then the Control Write Sequencer will automatically stop after this step has been executed.

The register definitions for Step 0 are described in Table 112. The equivalent definitions also apply to Step 1 through to Step 127, in the subsequent register address locations.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12288 (3000h) Write Sequencer 0	13:0	WSEQ_ADDR 0 [13:0]	0000h	Control Register Address to be written to in this sequence step.
R12289 (3001h) Write Sequencer 1	7:0	WSEQ_DATA 0 [7:0]	00h	Data to be written in this sequence step. When the data width is less than 8 bits, then one or more of the MSBs of WSEQ_DATA*n* are ignored. It is recommended that unused bits be set to 0.
R12290 (3002h) Write Sequencer 2	10:8	WSEQ_DATA _WIDTH0 [2:0]	000	Width of the data block written in this sequence step. 000 = 1 bit 001 = 2 bits 010 = 3 bits 011 = 4 bits 100 = 5 bits 101 = 6 bits 110 = 7 bits 111 = 8 bits
	3:0	WSEQ_DATA _START0 [3:0]	0000	Bit position of the LSB of the data block written in this sequence step. 0000 = Bit 0 … 1111 = Bit 15
R12291 (3003h) Write Sequencer 3	8	WSEQ_EOS0	0	End of Sequence flag. This bit indicates whether the Control Write Sequencer should stop after executing this step. 0 = Not end of sequence 1 = End of sequence (Stop the sequencer after this step).
	3:0	WSEQ_DELA Y0 [3:0]	0000	Time delay after executing this step. Total time per step (including execution) = 62.5µs × (2^{WSEQ_DELAY} + 8)

Table 112 Write Sequencer Control - Programming a Sequence

Note that a 'Dummy' write can be inserted into a control sequence by commanding the sequencer to write a value of 0 to bit 0 of Register R255 (00FFh). This is effectively a write to a non-existent register location. This can be used in order to create placeholders ready for easy adaptation of a control sequence. For example, a sequence could be defined to power-up a mono signal path from DACL to headphone, with a 'dummy' write included to leave space for easy modification to a stereo signal path configuration. Dummy writes can also be used in order to implement additional time delays between register writes. Dummy writes are included in both of the Headphone start-up sequences - see Table 113 and Table 114.

In summary, the Control Register to be written is set by the WSEQ_ADDR*n* field. The data bits that are written are determined by a combination of WSEQ_DATA_START*n*, WSEQ_DATA_WIDTH*n* and WSEQ_DATA*n*. This is illustrated below for an example case of writing to the VMID_SEL field within Register R1 (0001h).

In this example, the Start Position is bit 01 (WSEQ_DATA_START*n* = 0001b) and the Data width is 2 bits (WSEQ_DATA_WIDTH*n* = 0001b). With these settings, the Control Write Sequencer would update the Control Register R1 [2:1] with the contents of WSEQ_DATA*n* [1:0].

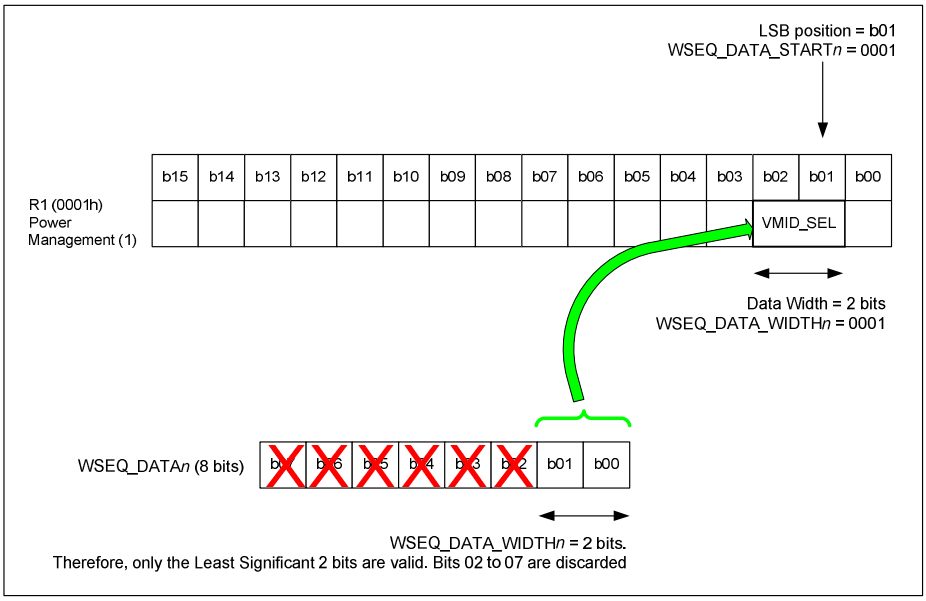


Figure 73 Control Write Sequencer Example

DEFAULT SEQUENCES

When the WM8994 is powered up, a number of Control Write Sequences are available through default settings in the sequencer memory locations. The pre-programmed default settings include Start-Up and Shut-Down sequences for each of the output drivers. Note that the default sequences do not include audio signal path or gain setting configuration; this must be implemented prior to scheduling any of the default Start-Up sequences.

The entire sequencer memory may be programmed to users' own settings at any time, as described in "Programming a Sequence". Users' own settings remain in memory regardless of WSEQ_ENA, and are not affected by software resets (i.e. writing to Register R0). However, any non-default sequences are lost when the device is powered down.

The following default control sequences are provided:

1. Headphone Cold Start-Up - This sequence powers up the headphone driver and charge pump. It commands the DC Servo to perform offset correction. It enables the master bias required for analogue functions. This sequence is intended for enabling the headphone output after initial power-on, when DC offset correction has not previously been run.

2. Headphone Warm Start-Up - This sequence is similar to the Headphone Cold Start-Up, but does not include the DC Servo operation. This sequence is intended for fast enabling of the

headphone output when DC offset correction has previously been scheduled and provided the analogue gain settings have not been updated since scheduling the DC offset correction.

3. Speaker Start-Up - This sequence powers up the stereo speaker driver. It also enables the master bias required for analogue functions.

4. Earpiece Start-Up - This sequence powers up the earpiece driver. It also enables the master bias required for analogue functions. The soft-start VMID option is used in order to suppress pops when the driver is enabled. This sequence is intended for enabling the earpiece driver when the master bias has not previously been enabled.

5. Line Output Start-Up - This sequence powers up the line outputs. Active discharge of the line outputs is selected, followed by the soft-start VMID enable, followed by selection of the master bias and un-muting of the line outputs. This sequence is intended for enabling the line drivers when the master bias has not previously been enabled.

6. Speaker and Headphone Fast Shut-Down - This sequence implements a fast shutdown of the speaker and headphone drivers. It also disables the DC Servo and charge pump circuits, and disables the analogue bias circuits using the soft-start (ramp) feature. This sequence is intended as a shut-down sequence when only the speaker or headphone drivers are enabled.

7. Generic Shut-Down - This sequence shuts down all of the WM8994 output drivers, DC Servo, charge pump and analogue bias circuits. It is similar to the Fast Shut-Down sequence, with the additional control of the earpiece and line output drivers. Active discharge of the line outputs is included and all drivers are disabled as part of this sequence.

Specific details of each of these sequences is provided below.

Headphone Cold Start-Up

The Headphone Cold Start-Up sequence is initiated by writing 8100h to Register 272 (0110h). This single operation starts the Control Write Sequencer at Index Address 0 (00h) and executes the sequence defined in Table 113.

This sequence takes approximately 296ms to run.

WSEQ INDEX	REGISTER ADDRESS	WIDTH	START	DATA	DELAY	EOS	DESCRIPTION
0 (00h)	R57 (0039h)	5 bits	Bit 2	1Bh	0h	0b	STARTUP_BIAS_ENA = 1 VMID_BUF_ENA = 1 VMID_RAMP[1:0] = 11b (delay = 0.5625ms)
1 (01h)	R1 (0001h)	3 bits	Bit 0	03h	9h	0b	BIAS_ENA = 1 VMID_SEL[1:0] = 01b (delay = 32.5ms)
2 (02h)	R76 (004Ch)	1 bit	Bit 15	01h	6h	0b	CP_ENA = 1 (delay = 4.5ms)
3 (03h)	R1 (0001h)	2 bits	Bit 8	03h	0h	0b	HPOUT1R_ENA = 1 HPOUT1L_ENA = 1 (delay = 0.5625ms)
4 (04h)	R96 (0060h)	5 bits	Bit 1	11h	0h	0b	HPOUT1R_DLY = 1 HPOUT1L_DLY = 1 (delay = 0.5625ms)
5 (05h)	R84 (0054h)	6 bits	Bit 0	33h	Ch	0b	DCS_ENA_CHAN_0 = 1 DCS_ENA_CHAN_1 = 1 DCS_TRIG_STARTUP_0 = 1 DCS_TRIG_STARTUP_1 = 1 (delay = 256.5ms)
6 (06h)	R255 (00FFh)	1 bit	Bit 0	00h	0h	0b	Dummy Write for expansion (delay = 0.5625ms)

WSEQ INDEX	REGISTER ADDRESS	WIDTH	START	DATA	DELAY	EOS	DESCRIPTION
7 (07h)	R96 (0060h)	6 bits	Bit 2	3Bh	0h	1b	HPOUT1R_OUTP = 1 HPOUT1R_RMV_SHORT =1 HPOUT1_DLY = 1 HPOUT1L_OUTP = 1 HPOUT1L_RMV_SHORT = 1 (delay = 0.5625ms)

Table 113 Headphone Cold Start-Up Default Sequence

Headphone Warm Start-Up

The Headphone Warm Start-Up sequence can be initiated by writing 0108h to Register 73 (49h). This single operation starts the Control Write Sequencer at Index Address 8 (08h) and executes the sequence defined in Table 114.

This sequence takes approximately 40ms to run.

WSEQ INDEX	REGISTER ADDRESS	WIDTH	START	DATA	DELAY	EOS	DESCRIPTION
8 (08h)	R57 (0039h)	5 bits	Bit 2	1Bh	0h	0b	STARTUP_BIAS_ENA = 1 VMID_BUF_ENA = 1 VMID_RAMP[1:0] = 11b (delay = 0.5625ms)
9 (09h)	R1 (0001h)	3 bits	Bit 0	03h	9h	0b	BIAS_ENA = 1 VMID_SEL[1:0] = 01b (delay = 32.5ms)
10 (0Ah)	R76 (004Ch)	1 bits	Bit 15	01h	6h	0b	CP_ENA = 1 (delay = 4.5ms)
11 (0Bh)	R1 (0001h)	2 bits	Bit 8	03h	0h	0b	HPOUT1R_ENA = 1 HPOUT1L_ENA = 1 (delay = 0.5625ms)
12 (0Ch)	R96 (0060h)	5 bits	Bit 1	11h	0h	0b	HPOUT1R_DLY = 1 HPOUT1L_DLY = 1 (delay = 0.5625ms)
13 (0Dh)	R84 (0054h)	2 bits	Bit 0	03h	0h	0b	DCS_ENA_CHAN_0 = 1 DCS_ENA_CHAN_1 = 1 (delay = 0.5625ms)
14 (0Eh)	R255 (00FFh)	1 bits	Bit 0	00h	0h	0b	Dummy Write for expansion (delay = 0.5625ms)
15 (0Fh)	R96 (0060h)	6 bits	Bit 2	3Bh	0h	1b	HPOUT1R_OUTP = 1 HPOUT1R_RMV_SHORT =1 HPOUT1_DLY = 1 HPOUT1L_OUTP = 1 HPOUT1L_RMV_SHORT = 1 (delay = 0.5625ms)

Table 114 Headphone Warm Start-Up Default Sequence

Speaker Start-Up

The Speaker Start-Up sequence can be initiated by writing 8110h to Register 272 (0110h). This single operation starts the Control Write Sequencer at Index Address 16 (10h) and executes the sequence defined in Table 115.

This sequence takes approximately 34ms to run.

WSEQ INDEX	REGISTER ADDRESS	WIDTH	START	DATA	DELAY	EOS	DESCRIPTION
16 (10h)	R57 (39h)	5 bits	Bit 2	1Bh	0h	0b	STARTUP_BIAS_ENA = 1 VMID_BUF_ENA = 1 VMID_RAMP[1:0] = 11b (delay = 0.5625ms)
17 (11h)	R1 (01h)	3 bits	Bit 0	03h	9h	0b	BIAS_ENA = 1 VMID_SEL[1:0] = 01b (delay = 32.5ms)
18 (12h)	R1 (01h)	2 bits	Bit 12	03h	0h	1b	SPKOUTL_ENA = 1 SPKOUTR_ENE = 1 (delay = 0.5625ms)

Table 115 Speaker Start-Up Default Sequence

Earpiece Start-Up

The Earpiece Start-Up sequence can be initiated by writing 8113h to Register 272 (0110h). This single operation starts the Control Write Sequencer at Index Address 19 (13h) and executes the sequence defined in Table 116.

This sequence takes approximately 259ms to run.

WSEQ INDEX	REGISTER ADDRESS	WIDTH	START	DATA	DELAY	EOS	DESCRIPTION
19 (13h)	R57 (39h)	6 bits	Bit 1	27h	0h	0b	BIAS_SRC = 1 STARTUP_BIAS_ENA = 1 VMID_BUF_ENA = 1 VMID_RAMP[1:0] = 10b (delay = 0.5625ms)
20 (14h)	R56 (38h)	1 bit	Bit 6	01h	0h	0b	HPOUT2_IN_ENA = 1 (delay = 0.5625ms)
21 (15h)	R31 (1Fh)	1 bit	Bit 5	00h	0h	1b	HPOUT2_MUTE = 0 (delay = 0.5625ms)
22 (16h)	R1 (01h)	1 bit	Bit 11	01h	0h	0b	HPOUT2_ENA = 1 (delay = 0.5625ms)
23 (17h)	R1 (01h)	3 bits	Bit 0	03h	Ch	0b	BIAS_ENA = 1 VMID_SEL[1:0] = 01b (delay = 256.5ms)
24 (18h)	R57 (39h)	1 bit	Bit 1	00h	0h	0b	BIAS_SRC = 0 (delay = 0.5625ms)

Table 116 Earpiece Start-Up Default Sequence

Line Output Start-Up

The Line Output Start-Up sequence can be initiated by writing 8119h to Register 272 (0110h). This single operation starts the Control Write Sequencer at Index Address 25 (19h) and executes the sequence defined in Table 117.

This sequence takes approximately 517ms to run.

WSEQ INDEX	REGISTER ADDRESS	WIDTH	START	DATA	DELAY	EOS	DESCRIPTION
25 (19h)	R56 (38h)	2 bits	Bit 4	03h	0h	0b	LINEOUT2_DISCH = 1 LINEOUT1_DISCH = 1 (delay = 0.5625ms)
26 (1Ah)	R57 (39h)	6 bits	Bit 1	27h	0h	0b	BIAS_SRC = 1 STARTUP_BIAS_ENA = 1 VMID_BUF_ENA = 1 VMID_RAMP[1:0] = 10b (delay = 0.5625ms)
27 (1Bh)	R56 (38h)	1 bit	Bit 7	01h	0h	0b	LINEOUT_VMID_BUF_ENA = 1 (delay = 0.5625ms)
28 (1Ch)	R3 (03h)	4 bits	Bit 10	0Fh	0h	0b	LINEOUT2P_ENA = 1 LINEOUT2N_ENA = 1 LINEOUT1P_ENA = 1 LINEOUT1N_ENA = 1 (delay = 0.5625ms)
29 (1Dh)	R56 (38h)	2 bits	Bit 4	00h	0h	0b	LINEOUT2_DISCH = 0 LINEOUT1_DISCH = 0 (delay = 0.5625ms)
30 (1Eh)	R1 (01h)	3 bits	Bit 0	03h	Dh	0b	BIAS_ENA = 1 VMID_SEL = 01b (delay = 512.5ms)
31 (1Fh)	R57 (39h)	1 bit	Bit 1	00h	0h	0b	BIAS_SRC = 0 (delay = 0.5625ms)
32 (20h)	R30 (1Eh)	2 bits	Bit 5	00h	0h	0b	LINEOUT1P_MUTE = 0 LINEOUT1N_MUTE = 0 (delay = 0.5625ms)
33 (21h)	R30 (1Eh)	2 bits	Bit 1	00h	0h	1b	LINEOUT2P_MUTE = 0 LINEOUT2N_MUTE = 0 (delay = 0.5625ms)

Table 117 Line Output Start-Up Default Sequence

Speaker and Headphone Fast Shut-Down

The Speaker and Headphone Fast Shut-Down sequence can be initiated by writing 8122h to Register 272 (0110h). This single operation starts the Control Write Sequencer at Index Address 34 (22h) and executes the sequence defined in Table 118.

This sequence takes approximately 37ms to run.

WSEQ INDEX	REGISTER ADDRESS	WIDTH	START	DATA	DELAY	EOS	DESCRIPTION
34 (22h)	R96 (60h)	7 bits	Bit 1	00h	0h	0b	HPOUT1R_DLY = 0 HPOUT1R_OUTP = 0 HPOUT1R_RMV_SHORT = 0 HPOUT1L_DLY = 0 HPOUT1L_OUTP = 0 HPOUT1L_RMV_SHORT = 0 (delay = 0.5625ms)
35 (23h)	R84 (54h)	2 bits	Bit 0	00h	0h	0b	DCS_ENA_CHAN_0 = 0 DCS_ENA_CHAN_1 = 0 (delay = 0.5625ms)
36 (24h)	R1 (01h)	2 bits	Bit 8	00h	0h	0b	HPOUT1R_ENA = 0 HPOUT1L_ENA = 0 (delay = 0.5625ms)
37 (25h)	R76 (4Ch)	1 bit	Bit 15	00h	0h	0b	CP_ENA = 0 (delay = 0.5625ms)
38 (26h)	R1 (01h)	2 bits	Bit 12	00h	0h	0b	SPKOUTL_ENA = 0 SPKOUTR_ENA = 0 (delay = 0.5625ms)
39 (27h)	R57 (39h)	6 bits	Bit 1	37h	0h	0b	BIAS_SRC = 1 STARTUP_BIAS_ENA = 1 VMID_BUF_ENA = 1 VMID_RAMP[1:0] = 11b (delay = 0.5625ms)
40 (28h)	R1 (01h)	3 bits	Bit 0	00h	9h	0b	BIAS_ENA = 0 VMID_SEL = 00b (delay = 32.5ms)
41 (29h)	R57 (39h)	6 bits	Bit 1	00h	0h	1b	BIAS_SRC = 0 STARTUP_BIAS_ENA = 0 VMID_BUF_ENA = 0 VMID_RAMP[1:0] = 00b (delay = 0.5625ms)

Table 118 Speaker and Headphone Fast Shut-Down Default Sequence

Generic Shut-Down

The Generic Shut-Down sequence can be initiated by writing 812Ah to Register 272 (0110h). This single operation starts the Control Write Sequencer at Index Address 42 (2Ah) and executes the sequence defined in Table 119.

This sequence takes approximately 522ms to run.

WSEQ INDEX	REGISTER ADDRESS	WIDTH	START	DATA	DELAY	EOS	DESCRIPTION
42 (2Ah)	R31 (1Fh)	1 bit	Bit 5	01h	0h	0b	HPOUT2_MUTE = 1 (delay = 0.5625ms)
43 (2Bh)	R30 (1Eh)	6 bits	Bit 1	33h	0h	0b	LINEOUT2P_MUTE = 1 LINEOUT2N_MUTE = 1 LINEOUT1P_MUTE = 1 LINEOUT1N_MUTE = 1 (delay = 0.5625ms)
44 (2Ch)	R96 (60h)	7 bits	Bit 1	00h	0h	0b	HPOUT1R_DLY = 0 HPOUT1R_OUTP = 0 HPOUT1R_RMV_SHORT = 0 HPOUT1L_DLY = 0 HPOUT1L_OUTP = 0 HPOUT1L_RMV_SHORT = 0 (delay = 0.5625ms)
45 (2Dh)	R84 (54h)	2 bits	Bit 0	00h	0h	0b	DCS_ENA_CHAN_0 = 0 DCS_ENA_CHAN_1 = 0 (delay = 0.5625ms)
46 (2Eh)	R1 (01h)	2 bits	Bit 8	00h	0h	0b	HPOUT1R_ENA = 0 HPOUT1L_ENA = 0 (delay = 0.5625ms)
47 (2Fh)	R76 (4Ch)	1 bit	Bit 15	00h	0h	0b	CP_ENA = 0 (delay = 0.5625ms)
48 (30h)	R1 (01h)	2 bits	Bit 12	00h	0h	0b	SPKOUTL_ENA = 0 SPKOUTR_ENA = 0 (delay = 0.5625ms)
49 (31h)	R57 (39h)	6 bits	Bit 1	17h	0h	0b	BIAS_SRC = 1 STARTUP_BIAS_ENA = 1 VMID_BUF_ENA = 1 VMID_RAMP[1:0] = 01b (delay = 0.5625ms)
50 (32h)	R1 (01h)	3 bits	Bit 0	00h	Dh	0b	BIAS_ENA = 0 VMID_SEL = 00b (delay = 512.5ms)
51 (33h)	R1 (01h)	1 bit	Bit 11	00h	0h	0b	HPOUT2_ENA = 0 (delay = 0.5625ms)
52 (34h)	R56 (38h)	2 bits	Bit 4	03h	0h	0b	LINEOUT2_DISCH = 1 LINEOUT1_DISCH = 1 (delay = 0.5625ms)
53 (35h)	R55 (37h)	1 bit	Bit 0	01h	0h	0b	VROI = 1 (delay = 0.5625ms)
54 (36h)	R56 (38h)	1 bit	Bit 6	00h	0h	0b	HPOUT2_IN_ENA =0 (delay = 0.5625ms)
55 (37h)	R3 (03h)	4 bits	Bit 10	00h	0h	0b	LINEOUT2P_ENA = 0 LINEOUT2N_ENA = 0 LINEOUT1P_ENA = 0 LINEOUT1N_ENA = 0 (delay = 0.5625ms)

WSEQ INDEX	REGISTER ADDRESS	WIDTH	START	DATA	DELAY	EOS	DESCRIPTION
56 (38h)	R56 (38h)	1 bit	Bit 7	00h	0h	0b	LINEOUT_VMID_BUF_ENA = 0 (delay = 0.5625ms)
57 (39h)	R55 (37h)	1 bit	Bit 0	00h	0h	0b	VROI = 0 (delay = 0.5625ms)
58 (3Ah)	R57 (39h)	6 bits	Bit 1	00h	0h	1b	BIAS_SRC = 0 STARTUP_BIAS_ENA = 0 VMID_BUF_ENA = 0 VMID_RAMP[1:0] = 00b (delay = 0.5625ms)

Table 119 Generic Shut-Down Default Sequence

POWER SEQUENCES AND POP SUPPRESSION CONTROL

The WM8994 incorporates a number of features, including Wolfson's SilentSwitch™ technology, designed to suppress pops normally associated with Start-Up, Shut-Down or signal path control. To achieve maximum benefit from these features, careful attention is required to the sequence and timing of these controls. Note that, under the recommended usage conditions of the WM8994, these features will be configured by running the default Start-Up and Shut-Down sequences as described in the "Control Write Sequencer" section. In these cases, the user does not need to set these register fields directly. Additional bias controls, also pre-programmed into Control Write Sequencer, are described in the "Reference Voltages and Master Bias" section.

DISABLED LINE OUTPUT CONTROL

The line outputs are biased to VMID in normal operation. In order to avoid audible pops caused by a disabled signal path dropping to AGND, the WM8994 can maintain these connections at VMID when the relevant output stage is disabled. This is achieved by connecting a buffered VMID reference to the output. The buffered VMID reference is enabled by setting VMID_BUF_ENA. The output resistance can be either 500Ω or 20kΩ, depending on the VROI register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R55 (0037h) Additional Control	0	VROI	0	Buffered VMID to Analogue Line Output Resistance (Disabled Outputs) 0 = 20kΩ from buffered VMID to output 1 = 500Ω from buffered VMID to output
R57 (0039h) AntiPOP2	3	VMID_BUF_ENA	0	VMID Buffer Enable 0 = Disabled 1 = Enabled

Table 120 Disabled Line Output Control

LINE OUTPUT DISCHARGE CONTROL

The line output paths can be actively discharged to AGND through internal resistors if desired. This is desirable at start-up in order to achieve a known output stage condition prior to enabling the soft-start VMID reference voltage. This is also desirable in shut-down to prevent the external connections from being affected by the internal circuits. The line outputs LINEOUT1P and LINEOUT1N are discharged to AGND by setting LINEOUT1_DISCH. The line outputs LINEOUT2P and LINEOUT2N are discharged to AGND by setting LINEOUT2_DISCH.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R56 (0038h) AntiPOP1	5	LINEOUT1_DISCH	0	Discharges LINEOUT1P and LINEOUT1N outputs via approx 4kΩ resistor 0 = Not active 1 = Actively discharging LINEOUT1P and LINEOUT1N
	4	LINEOUT2_DISCH	0	Discharges LINEOUT2P and LINEOUT2N outputs via approx 4kΩ resistor 0 = Not active 1 = Actively discharging LINEOUT2P and LINEOUT2N

Table 121 Line Output Discharge Control

VMID REFERENCE DISCHARGE CONTROL

The VMID reference can be actively discharged to AGND through internal resistors. This is desirable at start-up in order to achieve a known initial condition prior to enabling the soft-start VMID reference; this ensures maximum suppression of audible pops associated with start-up. VMID is discharged by setting VMID_DISCH.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R57 (0039h) AntiPOP2	0	VMID_DISCH	0	Connects VMID to ground 0 = Disabled 1 = Enabled

Table 122 VMID Reference Discharge Control

INPUT VMID CLAMPS

The analogue inputs can be clamped to Vmid using the INPUTS_CLAMP bit described below. This allows pre-charging of the input AC coupling capacitors during power-up, avoiding long delays when using headphone bypass paths. Note that all eight inputs are clamped using the same control bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R21 (15h) Input Mixer (1)	6	INPUTS_CLAMP	0	Input pad VMID clamp 0 = Clamp de-activated 1 = Clamp activated

Table 123 Input VMID Clamps

HEADPHONE ENABLE/DISABLE

The ground-referenced headphone outputs implement Wolfson's SilentSwitch™ technology to minimise pop noise associated with enabling and disabling. HPOUT1L and HPOUT1R are shorted to AGND by default while the individual driver stages are enabled. As a final step the short circuit is then removed on each of these paths by setting the applicable fields HPOUT1L_RMV_SHORT and HPOUT1R_RMV_SHORT.

The ground-referenced Headphone output drivers are designed to suppress pops and clicks when enabled or disabled. However, it is necessary to control the drivers in accordance with a defined sequence in start-up and shut-down to achieve the pop suppression. It is also necessary to schedule the DC Servo offset correction at the appropriate point in the sequence (see "DC Servo"). Table 124 and Table 125 describe the recommended sequences for enabling and disabling these output drivers.

SEQUENCE	HEADPHONE ENABLE
Step 1	HPOUT1L_ENA = 1 HPOUT1R_ENA = 1
Step 2	HPOUT1L_DLY = 1 HPOUT1R_DLY = 1
Step 3	DC offset correction
Step 4	HPOUT1L_OUTP = 1 HPOUT1L_RMV_SHORT = 1 HPOUT1R_OUTP = 1 HPOUT1R_RMV_SHORT = 1

Table 124 Headphone Output Enable Sequence

SEQUENCE	HEADPHONE DISABLE
Step 1	HPOUT1L_RMV_SHORT = 0 HPOUT1L_DLY = 0 HPOUT1L_OUTP = 0 HPOUT1R_RMV_SHORT = 0 HPOUT1R_DLY = 0 HPOUT1R_OUTP = 0
Step 2	HPOUT1L_ENA = 0 HPOUT1R_ENA = 0

Table 125 Headphone Output Disable Sequence

The register bits relating to pop suppression control are defined in Table 126.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (0001h) Power Management (1)	9	HPOUT1L_ENA	0	Enables HPOUT1L input stage 0 = Disabled 1 = Enabled Note: When HPOUT1_AUTO_PU is set, the HPOUT1L_ENA bit automatically enables all stages of the left headphone driver
	8	HPOUT1R_ENA	0	Enables HPOUT1R input stage 0 = Disabled 1 = Enabled Note: When HPOUT1_AUTO_PU is set, the HPOUT1R_ENA bit automatically enables all stages of the right headphone driver
R96 (0060h) Analogue HP (1)	7	HPOUT1L_RMV_SHORT	0	Removes HPOUT1L short 0 = HPOUT1L short enabled 1 = HPOUT1L short removed Note: Remove short after output stage has been enabled.
	6	HPOUT1L_OUTP	0	Enables HPOUT1L output stage 0 = Disabled 1 = Enabled Note: Set after offset correction is complete
	5	HPOUT1L_DLY	0	Enables HPOUT1L intermediate stage 0 = Disabled 1 = Enabled Note: Set with at least 20us delay to HPOUT1L_ENA
	3	HPOUT1R_RMV_SHORT	0	Removes HPOUT1R short 0 = HPOUT1R short enabled 1 = HPOUT1R short removed Note: Remove short after output stage has been enabled.
	2	HPOUT1R_OUTP	0	Enables HPOUT1R output stage 0 = Disabled 1 = Enabled Note: Set after offset correction is complete

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1	HPOUT1R_DLY	0	Enables HPOUT1R intermediate stage 0 = Disabled 1 = Enabled Note: Set with at least 20us delay to HPOUT1R_ENA

Table 126 Pop Suppression Control

EXAMPLE CONTROL SEQUENCES

The default control sequences (see "Control Write Sequencer") contain only the register writes necessary to enable or disable specific output drivers. It is therefore necessary to configure the signal path and gain settings before commanding any of the default start-up sequences.

Table 127 describes an example control sequence to enable the direct DAC to Headphone path. This involves DAC enable, signal path configuration and mute control, together with the default "Headphone Cold Start-Up" sequence. Table 128 describes an example control sequence to disable the direct DAC to Headphone path. Note that these sequences are provided for guidance only; Application software should be verified and tailored to ensure optimum performance.

REGISTER	VALUE	DESCRIPTION
R5 (0005h)	0003h	Enable DAC1L and DAC1R
R45 (002Dh)	0100h	Enable path from DAC1L to HPOUT1L
R46 (002Eh)	0100h	Enable path from DAC1R to HPOUT1R
R272 (0110h)	8100h	Initiate Control Write Sequencer (Headphone 'cold' Start-Up sequence)
		Delay 300ms Note: Delay must inserted in the sequence to allow the Control Write Sequencer to finish. Any control interface writes to the CODEC will be ignored while the Control Write Sequencer is running.
R1056 (0420h)	0000h	Soft un-mute DAC1L and DAC1R

Table 127 DAC to Headphone Direct Start-Up Sequence

REGISTER	VALUE	DESCRIPTION
R1056 (0420h)	0200h	Soft mute DAC1L and DAC1R
R272 (0110h)	812Ah	Initiate Control Write Sequencer at Index Address 42 (Generic Shut-Down)
		Delay 525ms Note: Delay must inserted in the sequence to allow the Control Write Sequencer to finish. Any control interface writes to the CODEC will be ignored while the Control Write Sequencer is running.
R45 (002Dh)	0000h	Disable path from DAC1L to HPOUT1L
R46 (002Eh)	0000h	Disable path from DAC1R to HPOUT1R
R5 (0005h)	0000h	Disable DAC1L and DAC1R

Table 128 DAC to Headphone Direct Shut-Down Sequence

CHARGE PUMP

The WM8994 incorporates a dual-mode Charge Pump which generates the supply rails for the headphone output drivers, HPOUT1L and HPOUT1R. The Charge Pump has a single supply input, CPVDD, and generates split rails CPVOUTP and CPVOUTN according to the selected mode of operation. The Charge Pump connections are illustrated in Figure 74 (see "Electrical Characteristics" for external component values). An input decoupling capacitor may also be required at CPVDD, depending upon the system configuration.

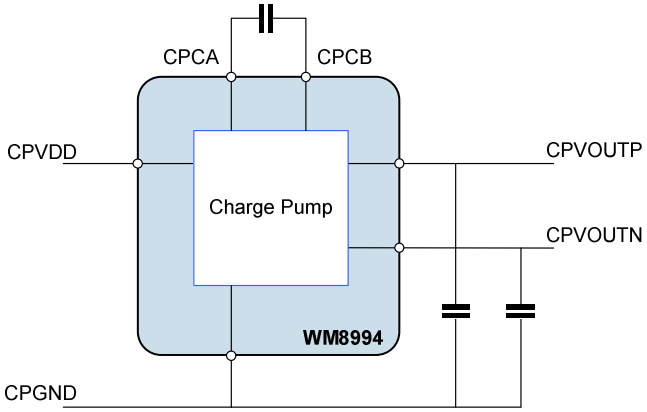


Figure 74 Charge Pump External Connections

The Charge Pump is enabled by setting the CP_ENA bit. When enabled, the charge pump adjusts the output voltages (VPOS and VNEG) as well as the switching frequency in order to optimise the power consumption according to the operating conditions. This can take two forms, which are selected using the CP_DYN_PWR register bit.

- Register control (CP_DYN_PWR = 0)
- Dynamic control (CP_DYN_PWR = 1)

Under Register control, the HPOUT1L_VOL and HPOUT1R_VOL register settings are used to control the charge pump mode of operation.

Under Dynamic control, the audio signal level in the digital audio interface is used to control the charge pump mode of operation. The CP_DYN_SRC_SEL register determines which of the digital signal paths is used for this function - this may be AIF1 Timeslot 0, AIF Timeslot 1 or AIF2. The CP_DYN_SRC_SEL should be set according to the active source for the HPOUT1L and HPOUT1R outputs.

The Dynamic Charge Pump Control mode is the Wolfson 'Class W' mode, which allows the power consumption to be optimised in real time, but can only be used if a single AIF source is the only signal source. The Class W mode should not be used if any of the bypass paths are used to feed analogue inputs into the output signal path, or if more than one AIF source is used to feed the headphone output via the Digital Mixers.

Under the recommended usage conditions of the WM8994, the Charge Pump will be enabled by running the default headphone Start-Up sequence as described in the "Control Write Sequencer" section. (Similarly, it will be disabled by running the Shut-Down sequence.) In these cases, the user does not need to write to the CP_ENA bit. The Charge Pump operating mode defaults to Register control; Dynamic control may be selected by setting the CP_DYN_PWR register bit, if appropriate.

Note that the charge pump clock is derived from internal clock SYSCLK; either MCLK or the FLL output selectable using the SYSCLK_SRC bit. Under normal circumstances an external clock signal must be present for the charge pump to function. However, the FLL has a free-running mode that does not require an external clock but will generate an internal clock suitable for running the charge pump. The clock division from SYSCLK is handled transparently by the WM8994 without user intervention, as long as SYSCLK and sample rates are set correctly. Refer to the "Clocking and Sample Rates" section for more detail on the FLL and clocking configuration.

The Charge Pump control fields are described in Table 129.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R76 (004Ch) Charge Pump 1	15	CP_ENA	0	Enable charge-pump digits 0 = disable 1 = enable
R81 (0051h) Class W (1)	9:8	CP_DYN_SRC_SEL	00	Selects the digital audio source for envelope tracking 00 = AIF1, DAC Timeslot 0 01 = AIF1, DAC Timeslot 1 10 = AIF2, DAC data 11 = Reserved
	0	CP_DYN_PWR	0	Enable dynamic charge pump power control 0 = charge pump controlled by volume register settings 1 = charge pump controlled by real-time audio level

Table 129 Charge Pump Control

DC SERVO

The WM8994 provides a DC servo circuit on the headphone outputs HPOUT1L and HPOUT1R in order to remove DC offset from these ground-referenced outputs. When enabled, the DC servo ensures that the DC level of these outputs remains within 1mV of ground. Removal of the DC offset is important because any deviation from GND at the output pin will cause current to flow through the load under quiescent conditions, resulting in increased power consumption. Additionally, the presence of DC offsets can result in audible pops and clicks at power up and power down.

The recommended usage of the DC Servo is initialised by running the default Start-Up sequence as described in the “Control Write Sequencer” section. The default Start-Up sequence executes a series of DC offset corrections, after which the measured offset correction is maintained on the headphone output channels. If a different usage is required, eg. if a periodic DC offset correction is required, then the default Start-Up sequence may be modified according to specific requirements. The relevant control fields are described in the following paragraphs and are defined in Table 130.

DC SERVO ENABLE AND START-UP

The DC Servo circuit is enabled on HPOUT1L and HPOUT1R by setting DCS_ENA_CHAN_1 and DCS_ENA_CHAN_0 respectively. When the DC Servo is enabled, the DC offset correction can be commanded in a number of different ways, including single-shot and periodically recurring events.

Writing a logic 1 to DCS_TRIG_STARTUP_*n* initiates a series of DC offset measurements and applies the necessary correction to the associated output; (‘n’ = 1 for Left channel, 0 for Right channel). On completion, the headphone output will be within 1mV of AGND. This is the DC Servo mode selected by the default Start-Up sequence. Completion of the DC offset correction triggered in this way is indicated by the DCS_STARTUP_COMPLETE field, as described in Table 130. Typically, this operation takes 86ms per channel.

Writing a logic 1 to DCS_TRIG_DAC_WR_*n* causes the DC offset correction to be set to the value contained in the DCS_DAC_WR_VAL_*n* fields in Register R87. This mode is useful if the required offset correction has already been determined and stored; it is faster than the DCS_TRIG_STARTUP_*n* mode, but relies on the accuracy of the stored settings. Completion of the DC offset correction triggered in this way is indicated by the DCS_DAC_WR_COMPLETE field, as described in Table 130. Typically, this operation takes 2ms per channel.

When using either of the DC Servo options above, the status of the DC offset correction process is indicated by the DCS_CAL_COMPLETE field; this is the logical OR of the DCS_STARTUP_COMPLETE and DCS_DAC_WR_COMPLETE fields.

The DC Servo control fields associated with start-up operation are described in Table 130. It is important to note that, to minimise audible pops/clicks, the Start-Up and DAC Write modes of DC Servo operation should be commanded as part of a control sequence which includes muting and shorting of the headphone outputs; a suitable sequence is defined in the default Start-Up sequence.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R84 (0054h) DC Servo (1)	5	DCS_TRIG_START UP_1	0	Writing 1 to this bit selects Start-Up DC Servo mode for HPOUT1L. In readback, a value of 1 indicates that the DC Servo Start-Up correction is in progress.
	4	DCS_TRIG_START UP_0	0	Writing 1 to this bit selects Start-Up DC Servo mode for HPOUT1R. In readback, a value of 1 indicates that the DC Servo Start-Up correction is in progress.
	3	DCS_TRIG_DAC_W R_0	0	Writing 1 to this bit selects DAC Write DC Servo mode for HPOUT1L. In readback, a value of 1 indicates that the DC Servo DAC Write correction is in progress.
	2	DCS_TRIG_DAC_W R_0	0	Writing 1 to this bit selects DAC Write DC Servo mode for HPOUT1R. In readback, a value of 1 indicates that the DC Servo DAC Write correction is in progress.
	1	DCS_ENA_CHAN_1	0	DC Servo enable for HPOUT1L 0 = disabled 1 = enabled
	0	DCS_ENA_CHAN_0	0	DC Servo enable for HPOUT1R 0 = disabled 1 = enabled
R87 (0057h) DC Servo (4)	15:8	DCS_DAC_WR_VA L_1 [7:0]	00h	DC Offset value for HPOUT1L in DAC Write DC Servo mode. Two's complement format. LSB is 0.25mV. Range is +/-32mV
	7:0	DCS_DAC_WR_VA L_0 [7:0]	00h	DC Offset value for HPOUT1R in DAC Write DC Servo mode. Two's complement format. LSB is 0.25mV. Range is +/-32mV
R88 (0058h) DC Servo Readback	9:8	DCS_CAL_COMPL ETE [1:0]	00	DC Servo Complete status 00 = DAC Write or Start-Up DC Servo mode not completed. 01 = DAC Write or Start-Up DC Servo mode complete on HPOUT1R only. 10 = DAC Write or Start-Up DC Servo mode complete on HPOUT1L only. 11 = DAC Write or Start-Up DC Servo mode complete on HPOUT1L and HPOUT1R.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	5:4	DCS_DAC_WR_COMPLETE [1:0]	00	DC Servo DAC Write status 00 = DAC Write DC Servo mode not completed. 01 = DAC Write DC Servo mode complete on HPOUT1R only. 10 = DAC Write DC Servo mode complete on HPOUT1L only. 11 = DAC Write DC Servo mode complete on HPOUT1L and HPOUT1R.
	1:0	DCS_STARTUP_COMPLETE [1:0]	00	DC Servo Start-Up status 00 = Start-Up DC Servo mode not completed. 01 = Start-Up DC Servo mode complete on HPOUT1R only. 10 = Start-Up DC Servo mode complete on HPOUT1L only. 11 = Start-Up DC Servo mode complete on HPOUT1L and HPOUT1R.

Table 130 DC Servo Enable and Start-Up Modes

DC SERVO ACTIVE MODES

The DC Servo modes described above are suitable for initialising the DC offset correction circuit on the Headphone outputs as part of a controlled start-up sequence which is executed before the signal path is fully enabled. Additional modes are available for use whilst the signal path is active; these modes may be of benefit following a large change in signal gain, which can lead to a change in DC offset level. Periodic updates may also be desirable to remove slow drifts in DC offset caused by changes in parameters such as device temperature.

The DC Servo circuit is enabled on HPOUT1L and HPOUT1R by setting DCS_ENA_CHAN_1 and DCS_ENA_CHAN_0 respectively, as described earlier in Table 130.

Writing a logic 1 to DCS_TRIG_SINGLE_*n* initiates a single DC offset measurement and adjustment to the associated output; ('n' = 1 for Left channel, 0 for Right channel). This will adjust the DC offset correction on the selected channel by no more than 1LSB (0.25mV).

Setting DCS_TIMER_PERIOD_01 to a non-zero value will cause a single DC offset measurement and adjustment to be scheduled on a periodic basis. Periodic rates ranging from every 0.52s to in excess of 2hours can be selected.

Writing a logic 1 to DCS_TRIG_SERIES_*n* initiates a series of DC offset measurements and applies the necessary correction to the associated output. The number of DC Servo operations performed is determined by DCS_SERIES_NO_01. A maximum of 128 operations may be selected, though a much lower value will be sufficient in most applications.

The DC Servo control fields associated with active modes (suitable for use on a signal path that is in active use) are described in Table 131.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R84 (0054h) DC Servo (1)	13	DCS_TRIG_SINGLE_1	0	Writing 1 to this bit selects a single DC offset correction for HPOUT1L. In readback, a value of 1 indicates that the DC Servo single correction is in progress.
	12	DCS_TRIG_SINGLE_0	0	Writing 1 to this bit selects a single DC offset correction for HPOUT1R. In readback, a value of 1 indicates that the DC Servo single correction is in progress.
	9	DCS_TRIG_SERIES_1	0	Writing 1 to this bit selects a series of DC offset corrections for HPOUT1L. In readback, a value of 1 indicates that the DC Servo DAC Write correction is in progress.
	8	DCS_TRIG_SERIES_0	0	Writing 1 to this bit selects a series of DC offset corrections for HPOUT1R. In readback, a value of 1 indicates that the DC Servo DAC Write correction is in progress.
R85 (0055h) DC Servo (2)	11:5	DCS_SERIES_NO_01 [6:0]	010 1010	Number of DC Servo updates to perform in a series event. 0 = 1 updates 1 = 2 updates ... 127 = 128 updates
	3:0	DCS_TIMER_PERIOD_01 [3:0]	1010	Time between periodic updates. Time is calculated as 0.251s x (2^PERIOD) 0000 = Off 0001 = 0.502s 1010 = 257s (4min 17s) 1111 = 8224s (2hr 17ms)

Table 131 DC Servo Active Modes

DC SERVO READBACK

The current DC offset value for each Headphone output channel can be read from Registers R89 and R90, as described in Table 132. Note that these values may form the basis of settings that are subsequently used by the DC Servo in DAC Write mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R91 (005Bh) DC Servo ANA (1)	7:0	DCS_IDAC_VAL_1	00h	Readback value for HPOUT1L. Two's complement format. LSB is 0.25mV. Range is +/-32mV
R92 (005Ch) DC Servo ANA (2)	7:0	DCS_IDAC_VAL_0	00h	Readback value for HPOUT1R. Two's complement format. LSB is 0.25mV. Range is +/-32mV

Table 132 DC Servo Readback

REFERENCE VOLTAGES AND MASTER BIAS

This section describes the analogue reference voltage and bias current controls. It also describes the VMID soft-start circuit for pop suppressed start-up and shut-down. Note that, under the recommended usage conditions of the WM8994, these features will be configured by running the default Start-Up and Shut-Down sequences as described in the "Control Write Sequencer" section. In these cases, the user does not need to set these register fields directly.

The analogue circuits in the WM8994 require a mid-rail analogue reference voltage, VMID. This reference is generated from AVDD1 via a programmable resistor chain. Together with the external VMID decoupling capacitor, the programmable resistor chain results in a slow, normal or fast charging characteristic on VMID. This is controlled by VMID_SEL[1:0], and can be used to optimise the reference for normal operation, low power standby or for fast start-up as described in Table 133.

The analogue circuits in the WM8994 require a bias current. The normal bias current is enabled by setting BIAS_ENA. Note that the normal bias current source requires VMID to be enabled also.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (0001h) Power Management (1)	2:1	VMID_SEL [1:0]	00	VMID Divider Enable and Select 00 = VMID disabled (for OFF mode) 01 = 2 x 40kΩ divider (for normal operation) 10 = 2 x 240kΩ divider (for low power standby) 11 = 2 x 5kΩ divider (for fast start-up)
	0	BIAS_ENA	0	Enables the Normal bias current generator (for all analogue functions) 0 = Disabled 1 = Enabled

Table 133 Reference Voltages and Master Bias Enable

A pop-suppressed start-up requires VMID to be enabled smoothly, without the step change normally associated with the initial stage of the VMID capacitor charging. A pop-suppressed start-up also requires the analogue bias current to be enabled throughout the signal path prior to the VMID reference voltage being applied. The WM8994 incorporates pop-suppression circuits which address these requirements.

An alternate bias current source (Start-Up Bias) is provided for pop-free start-up; this is enabled by the STARTUP_BIAS_ENA register bit. The start-up bias is selected (in place of the normal bias) using the BIAS_SRC bit. It is recommended that the start-up bias is used during start-up, before switching back to the higher quality, normal bias.

A soft-start circuit is provided in order to control the switch-on of the VMID reference. The soft-start control circuit offers two slew rates for enabling the VMID reference; these are selected and enabled by VMID_RAMP. When the soft-start circuit is enabled prior to enabling VMID_SEL, the reference voltage rises smoothly, without the step change that would otherwise occur. It is recommended that the soft-start circuit and the output signal path be enabled before VMID is enabled by VMID_SEL.

A soft shut-down is provided, using the soft-start control circuit and the start-up bias current generator. The soft shut-down of VMID is achieved by setting VMID_RAMP, STARTUP_BIAS_ENA and BIAS_SRC to select the start-up bias current and soft-start circuit prior to setting VMID_SEL=00.

The VMID soft-start register controls are defined in Table 134.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R57 (0039h) AntiPOP2	6:5	VMID_RAMP [1:0]	10	VMID soft start enable / slew rate control 00 = Normal slow start 01 = Normal fast start 10 = Soft slow start 11 = Soft fast start
	2	STARTUP_BIAS_ENA	0	Enables the Start-Up bias current generator 0 = Disabled 1 = Enabled
	1	BIAS_SRC	1	Selects the bias current source 0 = Normal bias 1 = Start-Up bias

Table 134 Soft Start Control

POWER MANAGEMENT

The WM8994 has control registers that allow users to select which functions are active. For minimum power consumption, unused functions should be disabled. To minimise pop or click noise, it is important to enable or disable functions in the correct order. See “Power Sequences and Pop Suppression Control” for further details of recommended control sequences.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (0001h) Power Management (1)	13	SPKOUTR_ENA	0	SPKMIXR Mixer, SPKRVOL PGA and SPKOUTR Output Enable 0 = Disabled 1 = Enabled
	12	SPKOUTL_ENA	0	SPKMIXL Mixer, SPKLVOL PGA and SPKOUTL Output Enable 0 = Disabled 1 = Enabled
	11	HPOUT2_ENA	0	HPOUT2 and HPOUT2MIX Enable 0 = Disabled 1 = Enabled
	9	HPOUT1L_ENA	0	Enables HPOUT1L input stage 0 = Disabled 1 = Enabled Note: When HPOUT1_AUTO_PU is set, the HPOUT1L_ENA bit automatically enables all stages of the left headphone driver
	8	HPOUT1R_ENA	0	Enables HPOUT1R input stage 0 = Disabled 1 = Enabled Note: When HPOUT1_AUTO_PU is set, the HPOUT1R_ENA bit automatically enables all stages of the right headphone driver
	5	MICB2_ENA	0	Microphone Bias 2 Enable 0 = OFF (high impedance output) 1 = ON
	4	MICB1_ENA	0	Microphone Bias 1 Enable 0 = OFF (high impedance output) 1 = ON
	2:1	VMID_SEL [1:0]	00	VMID Divider Enable and Select 00 = VMID disabled (for OFF mode) 01 = 2 x 40kΩ divider (Normal mode) 10 = 2 x 240kΩ divider (Standby mode) 11 = 2 x 5kΩ divider (for fast start-up)
	0	BIAS_ENA	0	Enables the Normal bias current generator (for all analogue functions) 0 = Disabled 1 = Enabled
R2 (0002h) Power Management (2)	14	TSHUT_ENA	0	Thermal Sensor Enable 0 = Disabled 1 = Enabled
	13	TSHUT_OPDIS	1	Thermal Shutdown Control (Causes audio outputs to be disabled if an over-temperature occurs. The thermal sensor must also be enabled.) 0 = Disabled 1 = Enabled
	11	OPCLK_ENA	0	GPIO Clock Output (OPCLK) Enable

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
				0 = Disabled 1 = Enabled
	9	MIXINL_ENA	0	Left Input Mixer Enable (Enables MIXINL and RXVOICE input to MIXINL) 0 = Disabled 1 = Enabled
	8	MIXINR_ENA	0	Right Input Mixer Enable (Enables MIXINR and RXVOICE input to MIXINR) 0 = Disabled 1 = Enabled
	7	IN2L_ENA	0	IN2L Input PGA Enable 0 = Disabled 1 = Enabled
	6	IN1L_ENA	0	IN1L Input PGA Enable 0 = Disabled 1 = Enabled
	5	IN2R_ENA	0	IN2R Input PGA Enable 0 = Disabled 1 = Enabled
	4	IN1R_ENA	0	IN1R Input PGA Enable 0 = Disabled 1 = Enabled
R3 (0003h) Power Management (3)	13	LINEOUT1N_ENA	0	LINEOUT1N Line Out and LINEOUT1NMIX Enable 0 = Disabled 1 = Enabled
	12	LINEOUT1P_ENA	0	LINEOUT1P Line Out and LINEOUT1PMIX Enable 0 = Disabled 1 = Enabled
	11	LINEOUT2N_ENA	0	LINEOUT2N Line Out and LINEOUT2NMIX Enable 0 = Disabled 1 = Enabled
	10	LINEOUT2P_ENA	0	LINEOUT2P Line Out and LINEOUT2PMIX Enable 0 = Disabled 1 = Enabled
	9	SPKRVOL_ENA	0	SPKMIXR Mixer and SPKRVOL PGA Enable 0 = Disabled 1 = Enabled Note that SPKMIXR and SPKRVOL are also enabled when SPKOUTR_ENA is set.
	8	SPKLVOL_ENA	0	SPKMIXL Mixer and SPKLVOL PGA Enable 0 = Disabled 1 = Enabled Note that SPKMIXL and SPKLVOL are also enabled when SPKOUTL_ENA is set.
	7	MIXOUTLVOL_ENA	0	MIXOUTL Left Volume Control Enable 0 = Disabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
				1 = Enabled
	6	MIXOUTRVOL_ENA	0	MIXOUTR Right Volume Control Enable 0 = Disabled 1 = Enabled
	5	MIXOUTL_ENA	0	MIXOUTL Left Output Mixer Enable 0 = Disabled 1 = Enabled
	4	MIXOUTR_ENA	0	MIXOUTR Right Output Mixer Enable 0 = Disabled 1 = Enabled
R4 (0004h) Power Management (4)	13	AIF2ADCL_ENA	0	Enable AIF2ADC (Left) output path 0 = Disabled 1 = Enabled
	12	AIF2ADCR_ENA	0	Enable AIF2ADC (Right) output path 0 = Disabled 1 = Enabled
	11	AIF1ADC2L_ENA	0	Enable AIF1ADC2 (Left) output path (AIF1, Timeslot 1) 0 = Disabled 1 = Enabled
	10	AIF1ADC2R_ENA	0	Enable AIF1ADC2 (Right) output path (AIF1, Timeslot 1) 0 = Disabled 1 = Enabled
	9	AIF1ADC1L_ENA	0	Enable AIF1ADC1 (Left) output path (AIF1, Timeslot 0) 0 = Disabled 1 = Enabled
	8	AIF1ADC1L_ENA	0	Enable AIF1ADC1 (Right) output path (AIF1, Timeslot 0) 0 = Disabled 1 = Enabled
	5	DMIC2L_ENA	0	Digital microphone DMICDAT2 Left channel enable 0 = Disabled 1 = Enabled
	4	DMIC2R_ENA	0	Digital microphone DMICDAT2 Right channel enable 0 = Disabled 1 = Enabled
	3	DMIC1L_ENA	0	Digital microphone DMICDAT1 Left channel enable 0 = Disabled 1 = Enabled
	2	DMIC1R_ENA	0	Digital microphone DMICDAT1 Right channel enable 0 = Disabled 1 = Enabled
	1	ADCL_ENA	0	Left ADC Enable 0 = ADC disabled 1 = ADC enabled
	0	ADCR_ENA	0	Right ADC Enable 0 = ADC disabled 1 = ADC enabled
R5 (0005h)	13	AIF2DACL_ENA	0	Enable AIF2DAC (Left) input path

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
Power Management (5)				0 = Disabled 1 = Enabled
	12	AIF2DACR_ENA	0	Enable AIF2DAC (Right) input path 0 = Disabled 1 = Enabled
	11	AIF1DAC2L_ENA	0	Enable AIF1DAC2 (Left) input path (AIF1, Timeslot 1) 0 = Disabled 1 = Enabled
	10	AIF1DAC2R_ENA	0	Enable AIF1DAC2 (Right) input path (AIF1, Timeslot 1) 0 = Disabled 1 = Enabled
	9	AIF1DAC1L_ENA	0	Enable AIF1DAC1 (Left) input path (AIF1, Timeslot 0) 0 = Disabled 1 = Enabled
	8	AIF1DAC1R_ENA	0	Enable AIF1DAC1 (Right) input path (AIF1, Timeslot 0) 0 = Disabled 1 = Enabled
	3	DAC2L_ENA	0	Left DAC2 Enable 0 = DAC disabled 1 = DAC enabled
	2	DAC2R_ENA	0	Right DAC2 Enable 0 = DAC disabled 1 = DAC enabled
	1	DAC1L_ENA	0	Left DAC1 Enable 0 = DAC disabled 1 = DAC enabled
	0	DAC1R_ENA	0	Right DAC1 Enable 0 = DAC disabled 1 = DAC enabled
R76 (004Ch) Charge Pump 1	15	CP_ENA	0	Enable charge-pump digits 0 = disable 1 = enable Note: Default value of R76[14:0] (0x1F25h) must not be changed when enabling/disabling the Charge Pump
R84 (0054h) DC Servo 0	1	DCS_ENA_CHAN_1	0	DC Servo enable for HPOUT1L 0 = disabled 1 = enabled
	0	DCS_ENA_CHAN_0	0	DC Servo enable for HPOUT1R 0 = disabled 1 = enabled
R272 (0110h) Write Sequencer Ctrl (1)	8	WSEQ_ENA	0	Write Sequencer Enable. 0 = Disabled 1 = Enabled

Table 135 Power Management

THERMAL SHUTDOWN

The WM8994 incorporates a temperature sensor which detects when the device temperature is within normal limits or if the device is approaching a hazardous temperature condition. The temperature sensor can be configured to automatically disable the audio outputs of the WM8994 in response to an overtemperature condition (approximately 150ºC).

The temperature status can be output directly on a GPIO pin, as described in the "General Purpose Input/Output" section. The temperature sensor can also be used to generate Interrupt events, as described in the "Interrupts" section.

The temperature sensor is enabled by setting the TSHUT_ENA register bit. When the TSHUT_OPDIS is also set, then a device over-temperature condition will cause the speaker outputs (SPKOUTL and SPKOUTR) of the WM8994 to be disabled; this response is likely to prevent any damage to the device attributable to the large currents of the output drivers.

Note that, to prevent pops and clicks, TSHUT_ENA and TSHUT_OPDIS should only be updated whilst the speaker and headphone outputs are disabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (0002h) Power Management (2)	14	TSHUT_ENA	1	Thermal sensor enable 0 = disabled 1 = enabled
	13	TSHUT_OPDIS	1	Thermal shutdown control (Causes audio outputs to be disabled if an overtemperature occurs. The thermal sensor must also be enabled.) 0 = disabled 1 = enabled

Table 136 Thermal Shutdown

POWER ON RESET

The WM8994 includes Power-On Reset (POR) circuits, which are used to reset the digital logic into a default state after power up. The POR circuits derive their output from AVDD1, AVDD2 and DCVDD. The internal $\overline{POR}$ signal is asserted low when AVDD1, AVDD2 and DCVDD are all below minimum thresholds.

The specific behaviour of the circuit will vary, depending on relative timing of the supply voltages. Typical scenarios are illustrated in Figure 75 and Figure 76.

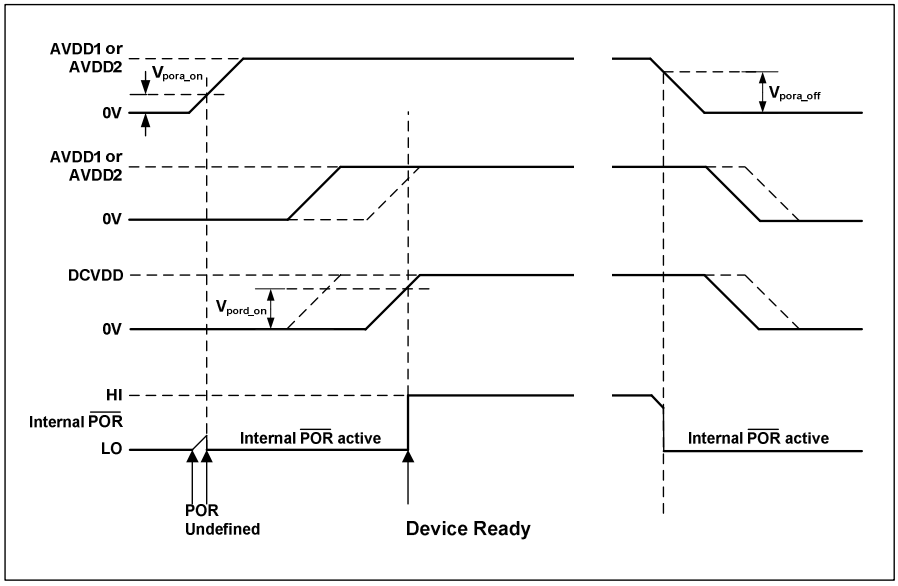


Figure 75 Power On Reset timing – AVDD1/2 enabled first

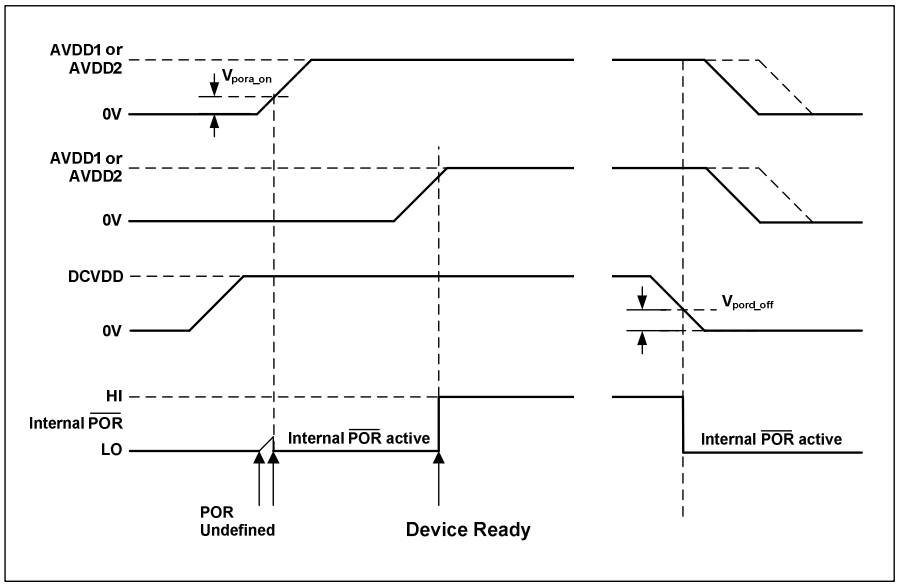


Figure 76 Power On Reset timing - DCVDD enabled first

The $\overline{POR}$ signal is undefined until AVDD1 or AVDD2 has exceeded the minimum threshold, V_{pora_on} Once this threshold has been exceeded, $\overline{POR}$ is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. Once AVDD1, AVDD2 and DCVDD have all reached their respective power on thresholds, $\overline{POR}$ is released high, all registers are in their default state, and writes to the control interface may take place.

Note that a minimum power-on reset period, T_{POR}, applies even if AVDD1, AVDD2 and DCVDD have zero rise time. (This specification is guaranteed by design rather than test.)

On power down, $\overline{POR}$ is asserted low when any of AVDD1, AVDD2 or DCVDD falls below their respective power-down thresholds.

Typical Power-On Reset parameters for the WM8994 are defined in Table 137.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
V_{pora_on}	Power-On threshold (AVDD1 or AVDD2)		1.52		V
V_{pora_off}	Power-Off threshold (AVDD1 or AVDD2)		1.5		V
V_{pord_on}	Power-On threshold (DCVDD)		0.92		V
V_{pord_off}	Power-Off threshold (DCVDD)		0.9		V
T_{POR}	Minimum Power-On Reset period		TBD		s

Table 137 Typical Power-On Reset parameters

SOFTWARE RESET AND DEVICE ID

The device ID can be read back from register 0. Writing to this register will reset the device.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (00h) Software Reset	15:0	SW_RESET [15:0]	8994h	Writing to this register resets all registers to their default state. Reading from this register will indicate device family ID 8994h.

Table 138 Chip Reset and ID

REGISTER MAP

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R0 (0h)	Software Reset	SW_RESET[15:0]																8994h
R1 (1h)	Power Management (1)	0	0	SPKOUTR_ENA	SPKOUTL_ENA	HPOUT2_ENA	0	HPOUT1L_ENA	HPOUT1R_ENA	0	0	MICB2_ENA	MICB1_ENA	0	VMID_SEL[1:0]		BIAS_ENA	0000h
R2 (2h)	Power Management (2)	0	TSHUT_ENA	TSHUT_OPDIS	0	OPCLK_ENA	0	MIXINL_ENA	MIXINR_ENA	IN2L_ENA	IN1L_ENA	IN2R_ENA	IN1R_ENA	0	0	0	0	6000h
R3 (3h)	Power Management (3)	0	0	LINEOUT1N_ENA	LINEOUT1P_ENA	LINEOUT2N_ENA	LINEOUT2P_ENA	SPKRVOL_ENA	SPKLVOL_ENA	MIXOUTLVOL_ENA	MIXOUTRVOL_ENA	MIXOUTL_ENA	MIXOUTR_ENA	0	0	0	0	0000h
R4 (4h)	Power Management (4)	0	0	AIF2ADCL_ENA	AIF2ADCR_ENA	AIF1ADC2L_ENA	AIF1ADC2R_ENA	AIF1ADC1L_ENA	AIF1ADC1R_ENA	0	0	DMIC2L_ENA	DMIC2R_ENA	DMIC1L_ENA	DMIC1R_ENA	ADCL_ENA	ADCR_ENA	0000h
R5 (5h)	Power Management (5)	0	0	AIF2DACL_ENA	AIF2DACR_ENA	AIF1DAC2L_ENA	AIF1DAC2R_ENA	AIF1DAC1L_ENA	AIF1DAC1R_ENA	0	0	0	0	DAC2L_ENA	DAC2R_ENA	DAC1L_ENA	DAC1R_ENA	0000h
R6 (6h)	Power Management (6)	0	0	0	0	0	0	0	0	0	0	AIF3_TRIS	AIF3_ADCDAT_SRC[1:0]		AIF2_ADCDAT_SRC	AIF2_DACDAT_SRC	AIF1_DACDAT_SRC	0000h
R21 (15h)	Input Mixer (1)	0	0	0	0	0	0	0	0	0	INPUTS_CLAMP	0	0	0	0	0	0	0000h
R24 (18h)	Left Line Input 1&2 Volume	0	0	0	0	0	0	0	IN1_VU	IN1L_MUTE	IN1L_ZC	0	IN1L_VOL[4:0]					008Bh
R25 (19h)	Left Line Input 3&4 Volume	0	0	0	0	0	0	0	IN2_VU	IN2L_MUTE	IN2L_ZC	0	IN2L_VOL[4:0]					008Bh
R26 (1Ah)	Right Line Input 1&2 Volume	0	0	0	0	0	0	0	IN1_VU	IN1R_MUTE	IN1R_ZC	0	IN1R_VOL[4:0]					008Bh
R27 (1Bh)	Right Line Input 3&4 Volume	0	0	0	0	0	0	0	IN2_VU	IN2R_MUTE	IN2R_ZC	0	IN2R_VOL[4:0]					008Bh
R28 (1Ch)	Left Output Volume	0	0	0	0	0	0	0	HPOUT1_VU	HPOUT1L_ZC	HPOUT1L_MUTE_N	HPOUT1L_VOL[5:0]						006Dh
R29 (1Dh)	Right Output Volume	0	0	0	0	0	0	0	HPOUT1_VU	HPOUT1R_ZC	HPOUT1R_MUTE_N	HPOUT1R_VOL[5:0]						006Dh
R30 (1Eh)	Line Outputs Volume	0	0	0	0	0	0	0	0	0	LINEOUT1N_MUTE	LINEOUT1P_MUTE	LINEOUT1_VOL	0	LINEOUT2N_MUTE	LINEOUT2P_MUTE	LINEOUT2_VOL	0066h
R31 (1Fh)	HPOUT2 Volume	0	0	0	0	0	0	0	0	0	0	HPOUT2_MUTE	HPOUT2_VOL	0	0	0	0	0020h
R32 (20h)	Left OPGA Volume	0	0	0	0	0	0	0	MIXOUT_VU	MIXOUTL_ZC	MIXOUTL_MUTE_N	MIXOUTL_VOL[5:0]						0079h
R33 (21h)	Right OPGA Volume	0	0	0	0	0	0	0	MIXOUT_VU	MIXOUTR_ZC	MIXOUTR_MUTE_N	MIXOUTR_VOL[5:0]						0079h
R34 (22h)	SPKMIXL Attenuation	0	0	0	0	0	0	0	0	0	DAC2L_SPKMIXL_VOL	MIXINL_SPKMIXL_VOL	IN1LP_SPKMIXL_VOL	MIXOUTL_SPKMIXL_VOL	DAC1L_SPKMIXL_VOL	SPKMIXL_VOL[1:0]		0003h
R35 (23h)	SPKMIXR Attenuation	0	0	0	0	0	0	0	SPKOUT_CLASSAB	0	DAC2R_SPKMIXR_VOL	MIXINR_SPKMIXR_VOL	IN1RP_SPKMIXR_VOL	MIXOUTR_SPKMIXR_VOL	DAC1R_SPKMIXR_VOL	SPKMIXR_VOL[1:0]		0003h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R36 (24h)	SPKOUT Mixers	0	0	0	0	0	0	0	0	0	0	IN2LP_TO_SPKOUTL	SPKMIXL_TO_SPKOUTL	SPKMIXR_TO_SPKOUTL	IN2LP_TO_SPKOUTR	SPKMIXL_TO_SPKOUTR	SPKMIXR_TO_SPKOUTR	0011h
R37 (25h)	ClassD	0	0	0	0	0	0	0	1	0	1	SPKOUTL_BOOST[2:0]			SPKOUTR_BOOST[2:0]			0140h
R38 (26h)	Speaker Volume Left	0	0	0	0	0	0	0	SPKOUT_VU	SPKOUTL_ZC	SPKOUTL_MUTE_N	SPKOUTL_VOL[5:0]						0079h
R39 (27h)	Speaker Volume Right	0	0	0	0	0	0	0	SPKOUT_VU	SPKOUTR_ZC	SPKOUTR_MUTE_N	SPKOUTR_VOL[5:0]						0079h
R40 (28h)	Input Mixer (2)	0	0	0	0	0	0	0	0	IN2LP_TO_IN2L	IN2LN_TO_IN2L	IN1LP_TO_IN1L	IN1LN_TO_IN1L	IN2RP_TO_IN2R	IN2RN_TO_IN2R	IN1RP_TO_IN1R	IN1RN_TO_IN1R	0000h
R41 (29h)	Input Mixer (3)	0	0	0	0	0	0	0	IN2L_TO_MIXINL	IN2L_MIXINL_VOL	0	IN1L_TO_MIXINL	IN1L_MIXINL_VOL	0	MIXOUTL_MIXINL_VOL[2:0]			0000h
R42 (2Ah)	Input Mixer (4)	0	0	0	0	0	0	0	IN2R_TO_MIXINR	IN2R_MIXINR_VOL	0	IN1R_TO_MIXINR	IN1R_MIXINR_VOL	0	MIXOUTR_MIXINR_VOL[2:0]			0000h
R43 (2Bh)	Input Mixer (5)	0	0	0	0	0	0	0	IN1LP_MIXINL_VOL[2:0]			0	0	0	IN2LP_MIXINL_VOL[2:0]			0000h
R44 (2Ch)	Input Mixer (6)	0	0	0	0	0	0	0	IN1RP_MIXINR_VOL[2:0]			0	0	0	IN2LP_MIXINR_VOL[2:0]			0000h
R45 (2Dh)	Output Mixer (1)	0	0	0	0	0	0	0	DAC1L_TO_HPOUT1L	MIXINR_TO_MIXOUTL	MIXINL_TO_MIXOUTL	IN2RN_TO_MIXOUTL	IN2LN_TO_MIXOUTL	IN1R_TO_MIXOUTL	IN1L_TO_MIXOUTL	IN2LP_TO_MIXOUTL	DAC1L_TO_MIXOUTL	0000h
R46 (2Eh)	Output Mixer (2)	0	0	0	0	0	0	0	DAC1R_TO_HPOUT1R	MIXINL_TO_MIXOUTR	MIXINR_TO_MIXOUTR	IN2LN_TO_MIXOUTR	IN2RN_TO_MIXOUTR	IN1L_TO_MIXOUTR	IN1R_TO_MIXOUTR	IN2RP_TO_MIXOUTR	DAC1R_TO_MIXOUTR	0000h
R47 (2Fh)	Output Mixer (3)	0	0	0	0	IN2LP_MIXOUTL_VOL[2:0]			IN2LN_MIXOUTL_VOL[2:0]			IN1R_MIXOUTL_VOL[2:0]			IN1L_MIXOUTL_VOL[2:0]			0000h
R48 (30h)	Output Mixer (4)	0	0	0	0	IN2RP_MIXOUTR_VOL[2:0]			IN2RN_MIXOUTR_VOL[2:0]			IN1L_MIXOUTR_VOL[2:0]			IN1R_MIXOUTR_VOL[2:0]			0000h
R49 (31h)	Output Mixer (5)	0	0	0	0	DACL_MIXOUTL_VOL[2:0]			IN2RN_MIXOUTL_VOL[2:0]			MIXINR_MIXOUTL_VOL[2:0]			MIXINL_MIXOUTL_VOL[2:0]			0000h
R50 (32h)	Output Mixer (6)	0	0	0	0	DACR_MIXOUTR_VOL[2:0]			IN2LN_MIXOUTR_VOL[2:0]			MIXINL_MIXOUTR_VOL[2:0]			MIXINR_MIXOUTR_VOL[2:0]			0000h
R51 (33h)	HPOUT2 Mixer	0	0	0	0	0	0	0	0	0	0	IN2LRP_TO_HPOUT2	MIXOUTLVOL_TO_HPOUT2	MIXOUTRVOL_TO_HPOUT2	0	0	0	0000h
R52 (34h)	Line Mixer (1)	0	0	0	0	0	0	0	0	0	MIXOUTL_TO_LINEOUT1N	MIXOUTR_TO_LINEOUT1N	LINEOUT1_MODE	0	IN1R_TO_LINEOUT1P	IN1L_TO_LINEOUT1P	MIXOUTL_TO_LINEOUT1P	0000h
R53 (35h)	Line Mixer (2)	0	0	0	0	0	0	0	0	0	MIXOUTR_TO_LINEOUT2N	MIXOUTL_TO_LINEOUT2N	LINEOUT2_MODE	0	IN1L_TO_LINEOUT2P	IN1R_TO_LINEOUT2P	MIXOUTR_TO_LINEOUT2P	0000h
R54 (36h)	Speaker Mixer	0	0	0	0	0	0	DAC2L_TO_SPKMIXL	DAC2R_TO_SPKMIXR	MIXINL_TO_SPKMIXL	MIXINR_TO_SPKMIXR	IN1LP_TO_SPKMIXL	IN1RP_TO_SPKMIXR	MIXOUTL_TO_SPKMIXL	MIXOUTR_TO_SPKMIXR	DAC1L_TO_SPKMIXL	DAC1R_TO_SPKMIXR	0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R55 (37h)	Additional Control	0	0	0	0	0	0	0	0	LINEOUT1_FB	LINEOUT2_FB	0	0	0	0	0	VROI	0000h
R56 (38h)	AntiPOP (1)	0	0	0	0	0	0	0	0	LINEOUT_VMID_BUF_ENA	HPOUT2_IN_ENA	LINEOUT1_DISCH	LINEOUT2_DISCH	0	0	0	0	0000h
R57 (39h)	AntiPOP (2)	0	0	0	0	0	0	0	0	0	VMID_RAMP[1:0]		0	VMID_BUF_ENA	START_UP_BIAS_ENA	BIAS_SRC	VMID_DISCH	0000h
R58 (3Ah)	MICBIAS	0	0	0	0	0	0	0	0	MICD_SCTHR[1:0]		MICD_THR[2:0]			MICD_ENA	MICB2_LVL	MICB1_LVL	0000h
R59 (3Bh)	LDO 1	0	0	0	0	0	0	0	0	0	0	0	0	LDO1_VSEL[2:0]			LDO1_DISCH	000Dh
R60 (3Ch)	LDO 2	0	0	0	0	0	0	0	0	0	0	0	0	0	LDO2_VSEL[1:0]		LDO2_DISCH	0003h
R76 (4Ch)	Charge Pump (1)	CP_ENA	0	0	1	1	1	1	1	0	0	1	0	0	1	0	1	1F25h
R81 (51h)	Class W (1)	0	0	0	0	0	0	CP_DYN_SRC_SEL[1:0]		0	0	0	0	0	1	0	CP_DYN_PWR	0004h
R84 (54h)	DC Servo (1)	0	0	DCS_TRIG_SINGLE_1	DCS_TRIG_SINGLE_0	0	0	DCS_TRIG_SERIES_1	DCS_TRIG_SERIES_0	0	0	DCS_TRIG_STARTUP_1	DCS_TRIG_STARTUP_0	DCS_TRIG_DAC_WR_1	DCS_TRIG_DAC_WR_0	DCS_ENA_CHAN_1	DCS_ENA_CHAN_0	0000h
R85 (55h)	DC Servo (2)	0	0	0	0	DCS_SERIES_NO_01[6:0]							0	DCS_TIMER_PERIOD_01[3:0]				054Ah
R87 (57h)	DC Servo (4)	DCS_DAC_WR_VAL_1[7:0]								DCS_DAC_WR_VAL_0[7:0]								0000h
R88 (58h)	DC Servo Readback	0	0	0	0	0	0	DCS_CAL_COMPLETE[1:0]		0	0	DCS_DAC_WR_COMPLETE[1:0]		0	0	DCS_STARTUP_COMPLETE[1:0]		0000h
R91 (5Bh)	DC Servo ANA (1)	0	0	0	0	0	0	0	0	DCS_IDAC_VAL_1[7:0]								0000h
R92 (5Ch)	DC Servo ANA (2)	0	0	0	0	0	0	0	0	DCS_IDAC_VAL_0[7:0]								0000h
R96 (60h)	Analogue HP (1)	0	0	0	0	0	0	0	0	HPOUT1L_RMV_SHORT	HPOUT1L_OUTP	HPOUT1L_DLY	0	HPOUT1R_RMV_SHORT	HPOUT1R_OUTP	HPOUT1R_DLY	0	0000h
R257 (101h)	Control Interface	REG_SYNC	0	0	0	0	0	0	0	0	SPI_CONTRD	SPI_4WIRE	SPI_CFG	0	AUTO_INC	0	0	8004h
R272 (110h)	Write Sequencer Ctrl (1)	WSEQ_ENA	0	0	0	0	0	WSEQ_ABORT	WSEQ_START	0	WSEQ_START_INDEX[6:0]							0000h
R273 (111h)	Write Sequencer Ctrl (2)	0	0	0	0	0	0	0	WSEQ_BUSY	0	WSEQ_CURRENT_INDEX[6:0]							0000h
R512 (200h)	AIF1 Clocking (1)	0	0	0	0	0	0	0	0	0	0	0	AIF1CLK_SRC[1:0]		AIF1CLK_INV	AIF1CLK_DIV	AIF1CLK_ENA	0000h
R513 (201h)	AIF1 Clocking (2)	0	0	0	0	0	0	0	0	0	0	AIF1DAC_DIV[2:0]			AIF1ADC_DIV[2:0]			0000h
R516 (204h)	AIF2 Clocking (1)	0	0	0	0	0	0	0	0	0	0	0	AIF2CLK_SRC[1:0]		AIF2CLK_INV	AIF2CLK_DIV	AIF2CLK_ENA	0000h
R517 (205h)	AIF2 Clocking (2)	0	0	0	0	0	0	0	0	0	0	AIF2DAC_DIV[2:0]			AIF2ADC_DIV[2:0]			0000h
R520 (208h)	Clocking (1)	0	0	0	0	0	0	0	0	0	0	0	TOCLK_ENA	DSP_FS1CLK_ENA	DSP_FS2CLK_ENA	DSP_FSINTCLK_ENA	SYSCLK_SRC	0000h
R521 (209h)	Clocking (2)	0	0	0	0	0	TOCLK_DIV[2:0]			0	DBCLK_DIV[2:0]			0	OPCLK_DIV[2:0]			0000h
R528 (210h)	AIF1 Rate	0	0	0	0	0	0	0	0	AIF1_SR[3:0]				AIF1CLK_RATE[3:0]				0083h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R529 (211h)	AIF2 Rate	0	0	0	0	0	0	0	0	AIF2_SR[3:0]				AIF2CLK_RATE[3:0]				0083h
R530 (212h)	Rate Status	0	0	0	0	0	0	0	0	0	0	0	0	SR_ERROR[3:0]				0000h
R544 (220h)	FLL1 Control (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	FLL1_FRACN_ENA	FLL1_OSC_ENA	FLL1_ENA	0000h
R545 (221h)	FLL1 Control (2)	0	0	FLL1_OUTDIV[5:0]						0	FLL1_CTRL_RATE[2:0]			0	FLL1_FRATIO[2:0]			0000h
R546 (222h)	FLL1 Control (3)	FLL1_K[15:0]																0000h
R547 (223h)	FLL1 Control (4)	0	FLL1_N[9:0]										0	FLL1_GAIN[3:0]				0000h
R548 (224h)	FLL1 Control (5)	0	0	0	FLL1_FRC_NCO_VAL[5:0]						FLL1_FRC_NCO	0	FLL1_CLK_REF_DIV[1:0]		0	FLL1_CLK_REF_SRC[1:0]		0C80h
R576 (240h)	FLL2 Control (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	FLL2_FRACN_ENA	FLL2_OSC_ENA	FLL2_ENA	0000h
R577 (241h)	FLL2 Control (2)	0	0	FLL2_OUTDIV[5:0]						0	FLL2_CTRL_RATE[2:0]			0	FLL2_FRATIO[2:0]			0000h
R578 (242h)	FLL2 Control (3)	FLL2_K[15:0]																0000h
R579 (243h)	FLL2 Control (4)	0	FLL2_N[9:0]										0	FLL2_GAIN[3:0]				0000h
R580 (244h)	FLL2 Control (5)	0	0	0	FLL2_FRC_NCO_VAL[5:0]						FLL2_FRC_NCO	0	FLL2_CLK_REF_DIV[1:0]		0	FLL2_CLK_REF_SRC[1:0]		0C80h
R768 (300h)	AIF1 Control (1)	AIF1ADCL_SRC	AIF1ADCR_SRC	AIF1ADC_TDM	0	0	0	0	AIF1_BCLK_INV	AIF1_LRCLK_INV	AIF1_WL[1:0]		AIF1_FMT[1:0]		0	0	0	4050h
R769 (301h)	AIF1 Control (2)	AIF1DACL_SRC	AIF1DACR_SRC	0	0	AIF1DAC_BOOST[1:0]		0	0	0	0	0	AIF1DAC_COMP	AIF1DAC_COMPMODE	AIF1ADC_COMP	AIF1ADC_COMPMODE	AIF1_LOOPBACK	4000h
R770 (302h)	AIF1 Master/Slave	AIF1_TRI	AIF1_MSTR	AIF1_CLK_FRC	AIF1_LRCLK_FRC	0	0	0	0	0	0	0	0	0	0	0	0	0000h
R771 (303h)	AIF1 BCLK	0	0	0	0	0	0	0	0	AIF1_BCLK_DIV[3:0]				0	0	0	0	0040h
R772 (304h)	AIF1ADC LRCLK	0	0	0	0	AIF1ADC_LRCLK_DIR	AIF1ADC_RATE[10:0]											0040h
R773 (305h)	AIF1DAC LRCLK	0	0	0	0	AIF1DAC_LRCLK_DIR	AIF1DAC_RATE[10:0]											0040h
R774 (306h)	AIF1DAC Data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF1DACL_DAT_INV	AIF1DACR_DAT_INV	0000h
R775 (307h)	AIF1ADC Data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF1ADCL_DAT_INV	AIF1ADCR_DAT_INV	0000h
R784 (310h)	AIF2 Control (1)	AIF2ADCL_SRC	AIF2ADCR_SRC	AIF2ADC_TDM	AIF2ADC_TDM_CHAN	0	0	0	AIF2_BCLK_INV	AIF2_LRCLK_INV	AIF2_WL[1:0]		AIF2_FMT[1:0]		0	0	0	4050h
R785 (311h)	AIF2 Control (2)	AIF2DACL_SRC	AIF2DACR_SRC	AIF2DAC_TDM	AIF2DAC_TDM_CHAN	AIF2DAC_BOOST[1:0]		0	0	0	0	0	AIF2DAC_COMP	AIF2DAC_COMPMODE	AIF2ADC_COMP	AIF2ADC_COMPMODE	AIF2_LOOPBACK	4000h
R786 (312h)	AIF2 Master/Slave	AIF2_TRI	AIF2_MSTR	AIF2_CLK_FRC	AIF2_LRCLK_FRC	0	0	0	0	0	0	0	0	0	0	0	0	0000h
R787 (313h)	AIF2 BCLK	0	0	0	0	0	0	0	0	AIF2_BCLK_DIV[3:0]				0	0	0	0	0040h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R788 (314h)	AIF2ADC LRCLK	0	0	0	0	AIF2ADC_LRCLK_DIR	AIF2ADC_RATE[10:0]											0040h
R789 (315h)	AIF2DAC LRCLK	0	0	0	0	AIF2DAC_LRCLK_DIR	AIF2DAC_RATE[10:0]											0040h
R790 (316h)	AIF2DAC Data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF2DACL_DAT_INV	AIF2DACR_DAT_INV	0000h
R791 (317h)	AIF2ADC Data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF2ADCL_DAT_INV	AIF2ADCR_DAT_INV	0000h
R1024 (400h)	AIF1 ADC1 Left Volume	0	0	0	0	0	0	0	AIF1ADC1_VU	AIF1ADC1L_VOL[7:0]								00C0h
R1025 (401h)	AIF1 ADC1 Right Volume	0	0	0	0	0	0	0	AIF1ADC1_VU	AIF1ADC1R_VOL[7:0]								00C0h
R1026 (402h)	AIF1 DAC1 Left Volume	0	0	0	0	0	0	0	AIF1DAC1_VU	AIF1DAC1L_VOL[7:0]								00C0h
R1027 (403h)	AIF1 DAC1 Right Volume	0	0	0	0	0	0	0	AIF1DAC1_VU	AIF1DAC1R_VOL[7:0]								00C0h
R1028 (404h)	AIF1 ADC2 Left Volume	0	0	0	0	0	0	0	AIF1ADC2_VU	AIF1ADC2L_VOL[7:0]								00C0h
R1029 (405h)	AIF1 ADC2 Right Volume	0	0	0	0	0	0	0	AIF1ADC2_VU	AIF1ADC2R_VOL[7:0]								00C0h
R1030 (406h)	AIF1 DAC2 Left Volume	0	0	0	0	0	0	0	AIF1DAC2_VU	AIF1DAC2L_VOL[7:0]								00C0h
R1031 (407h)	AIF1 DAC2 Right Volume	0	0	0	0	0	0	0	AIF1DAC2_VU	AIF1DAC2R_VOL[7:0]								00C0h
R1040 (410h)	AIF1 ADC1 Filters	0	AIF1ADC1_HPF_CUT[1:0]		AIF1ADC1L_HPF	AIF1ADC1R_HPF	0	0	0	0	0	0	0	0	0	0	0	0000h
R1041 (411h)	AIF1 ADC2 Filters	0	AIF1ADC2_HPF_CUT[1:0]		AIF1ADC2L_HPF	AIF1ADC2R_HPF	0	0	0	0	0	0	0	0	0	0	0	0000h
R1056 (420h)	AIF1 DAC1 Filters (1)	0	0	0	0	0	0	AIF1DAC1_MUTE	0	AIF1DAC1_MONO	0	AIF1DAC1_MUTERATE	AIF1DAC1_UNMUTE_RAMP	0	AIF1DAC1_DEEMP[1:0]		0	0200h
R1057 (421h)	AIF1 DAC1 Filters (2)	0	0	AIF1DAC1_3D_GAIN[4:0]					AIF1DAC1_3D_ENA	0	0	0	1	0	0	0	0	0010h
R1058 (422h)	AIF1 DAC2 Filters (1)	0	0	0	0	0	0	AIF1DAC2_MUTE	0	AIF1DAC2_MONO	0	AIF1DAC2_MUTERATE	AIF1DAC2_UNMUTE_RAMP	0	AIF1DAC2_DEEMP[1:0]		0	0200h
R1059 (423h)	AIF1 DAC2 Filters (2)	0	0	AIF1DAC2_3D_GAIN[4:0]					AIF1DAC2_3D_ENA	0	0	0	1	0	0	0	0	0010h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R1088 (440h)	AIF1 DRC1 (1)	AIF1DRC1_SIG_DET_RMS[4:0]					AIF1DRC1_SIG_DET_PK[1:0]		AIF1DRC1_NG_ENA	AIF1DRC1_SIG_DET_MODE	AIF1DRC1_SIG_DET	AIF1DRC1_KNEE2_OP_ENA	AIF1DRC1_QR	AIF1DRC1_ANTICLIP	AIF1DAC1_DRC_ENA	AIF1ADC1L_DRC_ENA	AIF1ADC1R_DRC_ENA	0098h
R1089 (441h)	AIF1 DRC1 (2)	0	0	0	AIF1DRC1_ATK[3:0]				AIF1DRC1_DCY[3:0]				AIF1DRC1_MINGAIN[2:0]			AIF1DRC1_MAXGAIN[1:0]		0845h
R1090 (442h)	AIF1 DRC1 (3)	AIF1DRC1_NG_MINGAIN[3:0]				AIF1DRC1_NG_EXP[1:0]		AIF1DRC1_QR_THR[1:0]		AIF1DRC1_QR_DCY[1:0]		AIF1DRC1_HI_COMP[2:0]			AIF1DRC1_LO_COMP[2:0]			0000h
R1091 (443h)	AIF1 DRC1 (4)	0	0	0	0	0	AIF1DRC1_KNEE_IP[5:0]						AIF1DRC1_KNEE_OP[4:0]					0000h
R1092 (444h)	AIF1 DRC1 (5)	0	0	0	0	0	0	AIF1DRC1_KNEE2_IP[4:0]					AIF1DRC1_KNEE2_OP[4:0]					0000h
R1104 (450h)	AIF1 DRC2 (1)	AIF1DRC2_SIG_DET_RMS[4:0]					AIF1DRC2_SIG_DET_PK[1:0]		AIF1DRC2_NG_ENA	AIF1DRC2_SIG_DET_MODE	AIF1DRC2_SIG_DET	AIF1DRC2_KNEE2_OP_ENA	AIF1DRC2_QR	AIF1DRC2_ANTICLIP	AIF1DAC2_DRC_ENA	AIF1ADC2L_DRC_ENA	AIF1ADC2R_DRC_ENA	0098h
R1105 (451h)	AIF1 DRC2 (2)	0	0	0	AIF1DRC2_ATK[3:0]				AIF1DRC2_DCY[3:0]				AIF1DRC2_MINGAIN[2:0]			AIF1DRC2_MAXGAIN[1:0]		0845h
R1106 (452h)	AIF1 DRC2 (3)	AIF1DRC2_NG_MINGAIN[3:0]				AIF1DRC2_NG_EXP[1:0]		AIF1DRC2_QR_THR[1:0]		AIF1DRC2_QR_DCY[1:0]		AIF1DRC2_HI_COMP[2:0]			AIF1DRC2_LO_COMP[2:0]			0000h
R1107 (453h)	AIF1 DRC2 (4)	0	0	0	0	0	AIF1DRC2_KNEE_IP[5:0]						AIF1DRC2_KNEE_OP[4:0]					0000h
R1108 (454h)	AIF1 DRC2 (5)	0	0	0	0	0	0	AIF1DRC2_KNEE2_IP[4:0]					AIF1DRC2_KNEE2_OP[4:0]					0000h
R1152 (480h)	AIF1 DAC1 EQ Gains (1)	AIF1DAC1_EQ_B1_GAIN[4:0]					AIF1DAC1_EQ_B2_GAIN[4:0]					AIF1DAC1_EQ_B3_GAIN[4:0]					AIF1DAC1_EQ_ENA	6318h
R1153 (481h)	AIF1 DAC1 EQ Gains (2)	AIF1DAC1_EQ_B4_GAIN[4:0]					AIF1DAC1_EQ_B5_GAIN[4:0]					0	0	0	0	0	0	6300h
R1154 (482h)	AIF1 DAC1 EQ Band 1 A	AIF1DAC1_EQ_B1_A[15:0]																0FCAh
R1155 (483h)	AIF1 DAC1 EQ Band 1 B	AIF1DAC1_EQ_B1_B[15:0]																0400h
R1156 (484h)	AIF1 DAC1 EQ Band 1 PG	AIF1DAC1_EQ_B1_PG[15:0]																00D8h
R1157 (485h)	AIF1 DAC1 EQ Band 2 A	AIF1DAC1_EQ_B2_A[15:0]																1EB5h
R1158 (486h)	AIF1 DAC1 EQ Band 2 B	AIF1DAC1_EQ_B2_B[15:0]																F145h
R1159 (487h)	AIF1 DAC1 EQ Band 2 C	AIF1DAC1_EQ_B2_C[15:0]																0B75h
R1160 (488h)	AIF1 DAC1 EQ Band 2 PG	AIF1DAC1_EQ_B2_PG[15:0]																01C5h
R1161 (489h)	AIF1 DAC1 EQ Band 3 A	AIF1DAC1_EQ_B3_A[15:0]																1C58h
R1162 (48Ah)	AIF1 DAC1 EQ Band 3 B	AIF1DAC1_EQ_B3_B[15:0]																F373h
R1163 (48Bh)	AIF1 DAC1 EQ Band 3 C	AIF1DAC1_EQ_B3_C[15:0]																0A54h
R1164 (48Ch)	AIF1 DAC1 EQ Band 3 PG	AIF1DAC1_EQ_B3_PG[15:0]																0558h
R1165 (48Dh)	AIF1 DAC1 EQ Band 4 A	AIF1DAC1_EQ_B4_A[15:0]																168Eh
R1166 (48Eh)	AIF1 DAC1 EQ Band 4 B	AIF1DAC1_EQ_B4_B[15:0]																F829h
R1167 (48Fh)	AIF1 DAC1 EQ Band 4 C	AIF1DAC1_EQ_B4_C[15:0]																07ADh
R1168 (490h)	AIF1 DAC1 EQ Band 4 PG	AIF1DAC1_EQ_B4_PG[15:0]																1103h
R1169 (491h)	AIF1 DAC1 EQ Band 5 A	AIF1DAC1_EQ_B5_A[15:0]																0564h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R1170 (492h)	AIF1 DAC1 EQ Band 5 B	AIF1DAC1_EQ_B5_B[15:0]																0559h
R1171 (493h)	AIF1 DAC1 EQ Band 5 PG	AIF1DAC1_EQ_B5_PG[15:0]																4000h
R1184 (4A0h)	AIF1 DAC2 EQ Gains (1)	AIF1DAC2_EQ_B1_GAIN[4:0]					AIF1DAC2_EQ_B2_GAIN[4:0]					AIF1DAC2_EQ_B3_GAIN[4:0]					AIF1DAC2_EQ_ENA	6318h
R1185 (4A1h)	AIF1 DAC2 EQ Gains (2)	AIF1DAC2_EQ_B4_GAIN[4:0]					AIF1DAC2_EQ_B5_GAIN[4:0]					0	0	0	0	0	0	6300h
R1186 (4A2h)	AIF1 DAC2 EQ Band 1 A	AIF1DAC2_EQ_B1_A[15:0]																0FCAh
R1187 (4A3h)	AIF1 DAC2 EQ Band 1 B	AIF1DAC2_EQ_B1_B[15:0]																0400h
R1188 (4A4h)	AIF1 DAC2 EQ Band 1 PG	AIF1DAC2_EQ_B1_PG[15:0]																00D8h
R1189 (4A5h)	AIF1 DAC2 EQ Band 2 A	AIF1DAC2_EQ_B2_A[15:0]																1EB5h
R1190 (4A6h)	AIF1 DAC2 EQ Band 2 B	AIF1DAC2_EQ_B2_B[15:0]																F145h
R1191 (4A7h)	AIF1 DAC2 EQ Band 2 C	AIF1DAC2_EQ_B2_C[15:0]																0B75h
R1192 (4A8h)	AIF1 DAC2 EQ Band 2 PG	AIF1DAC2_EQ_B2_PG[15:0]																01C5h
R1193 (4A9h)	AIF1 DAC2 EQ Band 3 A	AIF1DAC2_EQ_B3_A[15:0]																1C58h
R1194 (4AAh)	AIF1 DAC2 EQ Band 3 B	AIF1DAC2_EQ_B3_B[15:0]																F373h
R1195 (4ABh)	AIF1 DAC2 EQ Band 3 C	AIF1DAC2_EQ_B3_C[15:0]																0A54h
R1196 (4ACh)	AIF1 DAC2 EQ Band 3 PG	AIF1DAC2_EQ_B3_PG[15:0]																0558h
R1197 (4ADh)	AIF1 DAC2 EQ Band 4 A	AIF1DAC2_EQ_B4_A[15:0]																168Eh
R1198 (4AEh)	AIF1 DAC2 EQ Band 4 B	AIF1DAC2_EQ_B4_B[15:0]																F829h
R1199 (4AFh)	AIF1 DAC2 EQ Band 4 C	AIF1DAC2_EQ_B4_C[15:0]																07ADh
R1200 (4B0h)	AIF1 DAC2 EQ Band 4 PG	AIF1DAC2_EQ_B4_PG[15:0]																1103h
R1201 (4B1h)	AIF1 DAC2 EQ Band 5 A	AIF1DAC2_EQ_B5_A[15:0]																0564h
R1202 (4B2h)	AIF1 DAC2 EQ Band 5 B	AIF1DAC2_EQ_B5_B[15:0]																0559h
R1203 (4B3h)	AIF1 DAC2 EQ Band 5 PG	AIF1DAC2_EQ_B5_PG[15:0]																4000h
R1280 (500h)	AIF2 ADC Left Volume	0	0	0	0	0	0	0	AIF2ADC_VU	AIF2ADCL_VOL[7:0]								00C0h
R1281 (501h)	AIF2 ADC Right Volume	0	0	0	0	0	0	0	AIF2ADC_VU	AIF2ADCR_VOL[7:0]								00C0h
R1282 (502h)	AIF2 DAC Left Volume	0	0	0	0	0	0	0	AIF2DAC_VU	AIF2DACL_VOL[7:0]								00C0h
R1283 (503h)	AIF2 DAC Right Volume	0	0	0	0	0	0	0	AIF2DAC_VU	AIF2DACR_VOL[7:0]								00C0h
R1296 (510h)	AIF2 ADC Filters	AIF2ADC_4FS	AIF2ADC_HPF_CUT[1:0]		AIF2ADCL_HPF	AIF2ADCR_HPF	0	0	0	0	0	0	0	0	0	0	0	0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R1312 (520h)	AIF2 DAC Filters (1)	0	0	0	0	0	0	AIF2DAC_MUTE	0	AIF2DAC_MONO	0	AIF2DAC_MUTERATE	AIF2DAC_UNMUTE_RAMP	0	AIF2DAC_DEEMP[1:0]		0	0200h
R1313 (521h)	AIF2 DAC Filters (2)	0	0	AIF2DAC_3D_GAIN[4:0]					AIF2DAC_3D_ENA	0	0	0	1	0	0	0	0	0010h
R1344 (540h)	AIF2 DRC (1)	AIF2DRC_SIG_DET_RMS[4:0]					AIF2DRC_SIG_DET_PK[1:0]		AIF2DRC_NG_ENA	AIF2DRC_SIG_DET_MODE	AIF2DRC_SIG_DET	AIF2DRC_KNEE2_OP_ENA	AIF2DRC_QR	AIF2DRC_ANTICLIP	AIF2DAC_DRC_ENA	AIF2ADCL_DRC_ENA	AIF2ADCR_DRC_ENA	0098h
R1345 (541h)	AIF2 DRC (2)	0	0	0	AIF2DRC_ATK[3:0]				AIF2DRC_DCY[3:0]				AIF2DRC_MINGAIN[2:0]			AIF2DRC_MAXGAIN[1:0]		0845h
R1346 (542h)	AIF2 DRC (3)	AIF2DRC_NG_MINGAIN[3:0]				AIF2DRC_NG_EXP[1:0]		AIF2DRC_QR_THR[1:0]		AIF2DRC_QR_DCY[1:0]		AIF2DRC_HI_COMP[2:0]			AIF2DRC_LO_COMP[2:0]			0000h
R1347 (543h)	AIF2 DRC (4)	0	0	0	0	0	AIF2DRC_KNEE_IP[5:0]						AIF2DRC_KNEE_OP[4:0]					0000h
R1348 (544h)	AIF2 DRC (5)	0	0	0	0	0	0	AIF2DRC_KNEE2_IP[4:0]					AIF2DRC_KNEE2_OP[4:0]					0000h
R1408 (580h)	AIF2 EQ Gains (1)	AIF2DAC_EQ_B1_GAIN[4:0]					AIF2DAC_EQ_B2_GAIN[4:0]					AIF2DAC_EQ_B3_GAIN[4:0]					AIF2DAC_EQ_ENA	6318h
R1409 (581h)	AIF2 EQ Gains (2)	AIF2DAC_EQ_B4_GAIN[4:0]					AIF2DAC_EQ_B5_GAIN[4:0]					0	0	0	0	0	0	6300h
R1410 (582h)	AIF2 EQ Band 1 A	AIF2DAC_EQ_B1_A[15:0]																0FCAh
R1411 (583h)	AIF2 EQ Band 1 B	AIF2DAC_EQ_B1_B[15:0]																0400h
R1412 (584h)	AIF2 EQ Band 1 PG	AIF2DAC_EQ_B1_PG[15:0]																00D8h
R1413 (585h)	AIF2 EQ Band 2 A	AIF2DAC_EQ_B2_A[15:0]																1EB5h
R1414 (586h)	AIF2 EQ Band 2 B	AIF2DAC_EQ_B2_B[15:0]																F145h
R1415 (587h)	AIF2 EQ Band 2 C	AIF2DAC_EQ_B2_C[15:0]																0B75h
R1416 (588h)	AIF2 EQ Band 2 PG	AIF2DAC_EQ_B2_PG[15:0]																01C5h
R1417 (589h)	AIF2 EQ Band 3 A	AIF2DAC_EQ_B3_A[15:0]																1C58h
R1418 (58Ah)	AIF2 EQ Band 3 B	AIF2DAC_EQ_B3_B[15:0]																F373h
R1419 (58Bh)	AIF2 EQ Band 3 C	AIF2DAC_EQ_B3_C[15:0]																0A54h
R1420 (58Ch)	AIF2 EQ Band 3 PG	AIF2DAC_EQ_B3_PG[15:0]																0558h
R1421 (58Dh)	AIF2 EQ Band 4 A	AIF2DAC_EQ_B4_A[15:0]																168Eh
R1422 (58Eh)	AIF2 EQ Band 4 B	AIF2DAC_EQ_B4_B[15:0]																F829h
R1423 (58Fh)	AIF2 EQ Band 4 C	AIF2DAC_EQ_B4_C[15:0]																07ADh
R1424 (590h)	AIF2 EQ Band 4 PG	AIF2DAC_EQ_B4_PG[15:0]																1103h
R1425 (591h)	AIF2 EQ Band 5 A	AIF2DAC_EQ_B5_A[15:0]																0564h
R1426 (592h)	AIF2 EQ Band 5 B	AIF2DAC_EQ_B5_B[15:0]																0559h
R1427 (593h)	AIF2 EQ Band 5 PG	AIF2DAC_EQ_B5_PG[15:0]																4000h
R1536 (600h)	DAC1 Mixer Volumes	0	0	0	0	0	0	0	ADC2_DAC1_VOL[3:0]				0	ADC1_DAC1_VOL[3:0]				0000h
R1537 (601h)	DAC1 Left Mixer Routing	0	0	0	0	0	0	0	0	0	0	ADC2_TO_DAC1L	ADC1_TO_DAC1L	0	AIF2DACL_TO_DAC1L	AIF1DAC2L_TO_DAC1L	AIF1DAC1L_TO_DAC1L	0000h
R1538 (602h)	DAC1 Right Mixer Routing	0	0	0	0	0	0	0	0	0	0	ADC2_TO_DAC1R	ADC1_TO_DAC1R	0	AIF2DACR_TO_DAC1R	AIF1DAC2R_TO_DAC1R	AIF1DAC1R_TO_DAC1R	0000h
R1539 (603h)	DAC2 Mixer Volumes	0	0	0	0	0	0	0	ADC2_DAC2_VOL[3:0]				0	ADC1_DAC2_VOL[3:0]				0000h
R1540 (604h)	DAC2 Left Mixer Routing	0	0	0	0	0	0	0	0	0	0	ADC2_TO_DAC2L	ADC1_TO_DAC2L	0	AIF2DACL_TO_DAC2L	AIF1DAC2L_TO_DAC2L	AIF1DAC1L_TO_DAC2L	0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R1541 (605h)	DAC2 Right Mixer Routing	0	0	0	0	0	0	0	0	0	0	ADC2_TO_DAC2R	ADC1_TO_DAC2R	0	AIF2DACR_TO_DAC2R	AIF1DAC2R_TO_DAC2R	AIF1DAC1R_TO_DAC2R	0000h
R1542 (606h)	AIF1 ADC1 Left Mixer Routing	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ADC1L_TO_AIF1ADC1L	AIF2DACL_TO_AIF1ADC1L	0000h
R1543 (607h)	AIF1 ADC1 Right Mixer Routing	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ADC1R_TO_AIF1ADC1R	AIF2DACR_TO_AIF1ADC1R	0000h
R1544 (608h)	AIF1 ADC2 Left Mixer Routing	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ADC2L_TO_AIF1ADC2L	AIF2DACL_TO_AIF1ADC2L	0000h
R1545 (609h)	AIF1 ADC2 Right mixer Routing	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ADC2R_TO_AIF1ADC2R	AIF2DACR_TO_AIF1ADC2R	0000h
R1552 (610h)	DAC1 Left Volume	0	0	0	0	0	0	DAC1L_MUTE	DAC1_VU	DAC1L_VOL[7:0]								02C0h
R1553 (611h)	DAC1 Right Volume	0	0	0	0	0	0	DAC1R_MUTE	DAC1_VU	DAC1R_VOL[7:0]								02C0h
R1554 (612h)	DAC2 Left Volume	0	0	0	0	0	0	DAC2L_MUTE	DAC2_VU	DAC2L_VOL[7:0]								02C0h
R1555 (613h)	DAC2 Right Volume	0	0	0	0	0	0	DAC2R_MUTE	DAC2_VU	DAC2R_VOL[7:0]								02C0h
R1556 (614h)	DAC Softmute	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DAC_SOFTMUTEMODE	DAC_MUTERATE	0000h
R1568 (620h)	Oversampling	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ADC_OSR128	DAC_OSR128	0002h
R1569 (621h)	Sidetone	0	0	0	0	0	0	ST_HPF_CUT[2:0]			ST_HPF	0	0	0	0	ST2_SEL	ST1_SEL	0000h
R1792 (700h)	GPIO 1	GP1_DIR	GP1_PU	GP1_PD	0	0	GP1_POL	GP1_OP_CFG	GP1_DB	0	GP1_LVL	0	GP1_FN[4:0]					A100h
R1793 (701h)	GPIO 2	1	GP2_PU	GP2_PD	0	0	GP2_POL	GP2_OP_CFG	1	0	GP2_LVL	0	GP2_FN[4:0]					A101h
R1794 (702h)	GPIO 3	GP3_DIR	GP3_PU	GP3_PD	0	0	GP3_POL	GP3_OP_CFG	GP3_DB	0	GP3_LVL	0	GP3_FN[4:0]					A101h
R1795 (703h)	GPIO 4	GP4_DIR	GP4_PU	GP4_PD	0	0	GP4_POL	GP4_OP_CFG	GP4_DB	0	GP4_LVL	0	GP4_FN[4:0]					A101h
R1796 (704h)	GPIO 5	GP5_DIR	GP5_PU	GP5_PD	0	0	GP5_POL	GP5_OP_CFG	GP5_DB	0	GP5_LVL	0	GP5_FN[4:0]					A101h
R1797 (705h)	GPIO 6	GP6_DIR	GP6_PU	GP6_PD	0	0	GP6_POL	GP6_OP_CFG	GP6_DB	0	GP6_LVL	0	GP6_FN[4:0]					A101h
R1798 (706h)	GPIO 7	GP7_DIR	GP7_PU	GP7_PD	0	0	GP7_POL	GP7_OP_CFG	GP7_DB	0	GP7_LVL	0	GP7_FN[4:0]					A101h
R1799 (707h)	GPIO 8	GP8_DIR	GP8_PU	GP8_PD	0	0	GP8_POL	GP8_OP_CFG	GP8_DB	0	GP8_LVL	0	GP8_FN[4:0]					A101h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R1800 (708h)	GPIO 9	GP9_DIR	GP9_PU	GP9_PD	0	0	GP9_POL	GP9_OP_CFG	GP9_DB	0	GP9_LVL	0	GP9_FN[4:0]					A101h
R1801 (709h)	GPIO 10	GP10_DIR	GP10_PU	GP10_PD	0	0	GP10_POL	GP10_OP_CFG	GP10_DB	0	GP10_LVL	0	GP10_FN[4:0]					A101h
R1802 (70Ah)	GPIO 11	GP11_DIR	GP11_PU	GP11_PD	0	0	GP11_POL	GP11_OP_CFG	GP11_DB	0	GP11_LVL	0	GP11_FN[4:0]					A101h
R1824 (720h)	Digital Pulls	0	0	0	0	DMICDAT2_PU	DMICDAT2_PD	DMICDAT1_PU	DMICDAT1_PD	MCLK1_PU	MCLK1_PD	DACDAT1_PU	DACDAT1_PD	DACLRCLK1_PU	DACLRCLK1_PD	BCLK1_PU	BCLK1_PD	0000h
R1840 (730h)	Interrupt Status 1	0	0	0	0	0	GP11_EINT	GP10_EINT	GP9_EINT	GP8_EINT	GP7_EINT	GP6_EINT	GP5_EINT	GP4_EINT	GP3_EINT	GP2_EINT	GP1_EINT	0000h
R1841 (731h)	Interrupt Status 2	0	0	WSEQ_DONE_EINT	FIFOS_ERR_EINT	DRC3_ACTDET_EINT	DRC2_ACTDET_EINT	DRC1_ACTDET_EINT	SRC2_LOCK_EINT	SRC1_LOCK_EINT	FLL2_LOCK_EINT	FLL1_LOCK_EINT	MIC2_SHRT_EINT	MIC2_DET_EINT	MIC1_SHRT_EINT	MIC1_DET_EINT	TEMP_SHUT_EINT	0000h
R1848 (738h)	Interrupt Status 1 Mask	0	0	0	0	0	IM_GP11_EINT	IM_GP10_EINT	IM_GP9_EINT	IM_GP8_EINT	IM_GP7_EINT	IM_GP6_EINT	IM_GP5_EINT	IM_GP4_EINT	IM_GP3_EINT	IM_GP2_EINT	IM_GP1_EINT	07FFh
R1849 (739h)	Interrupt Status 2 Mask	0	0	IM_WSEQ_DONE_EINT	IM_FIFOS_ERR_EINT	IM_DRC3_ACTDET_EINT	IM_DRC2_ACTDET_EINT	IM_DRC1_ACTDET_EINT	IM_SRC2_LOCK_EINT	IM_SRC1_LOCK_EINT	IM_FL2_LOCK_EINT	IM_FL1_LOCK_EINT	IM_MIC2_SHRT_EINT	IM_MIC2_DET_EINT	IM_MIC1_SHRT_EINT	IM_MIC1_DET_EINT	IM_TEMP_SHUT_EINT	3FFFh
R1856 (740h)	Interrupt Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	IRQ_POL	0000h
R1864 (748h)	IRQ Debounce	0	0	0	0	0	0	0	0	0	0	0	MIC2_SHRT_DB	MIC2_DET_DB	MIC1_SHRT_DB	MIC1_DET_DB	TEMP_SHUT_DB	001Fh
R1865 (749h)	IRQ Polarity	0	0	WSEQ_DONE_POL	FIFOS_ERR_POL	DRC3_ACTDET_POL	DRC2_ACTDET_POL	DRC1_ACTDET_POL	SRC2_LOCK_POL	SRC1_LOCK_POL	FLL2_LOCK_POL	FLL1_LOCK_POL	MIC2_SHRT_POL	MIC2_DET_POL	MIC1_SHRT_POL	MIC1_DET_POL	TEMP_SHUT_POL	0000h

REGISTER BITS BY ADDRESS

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R0 (00h) Software Reset	15:0	SW_RESET[15:0]	1000_1001_1001_0100	Writing to this register resets all registers to their default state. Reading from this register will indicate device family ID 8994h.	

Register 00h Software Reset

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1 (01h) Power Management (1)	13	SPKOUTR_ENA	0	SPKMIXR Mixer, SPKRVOL PGA and SPKOUTR Output Enable 0 = Disabled 1 = Enabled	
	12	SPKOUTL_ENA	0	SPKMIXL Mixer, SPKLVOL PGA and SPKOUTL Output Enable 0 = Disabled 1 = Enabled	
	11	HPOUT2_ENA	0	HPOUT2 Output Stage Enable 0 = Disabled 1 = Enabled	
	9	HPOUT1L_ENA	0	Enables HPOUT1L input stage 0 = Disabled 1 = Enabled Note: When HPOUT1_AUTO_PU is set, the HPOUT1L_ENA bit automatically enables all stages of the left headphone driver	
	8	HPOUT1R_ENA	0	Enables HPOUT1R input stage 0 = Disabled 1 = Enabled Note: When HPOUT1_AUTO_PU is set, the HPOUT1R_ENA bit automatically enables all stages of the right headphone driver	
	5	MICB2_ENA	0	Microphone Bias 2 Enable 0 = OFF (high impedance output) 1 = ON	
	4	MICB1_ENA	0	Microphone Bias 1 Enable 0 = OFF (high impedance output) 1 = ON	
	2:1	VMID_SEL[1:0]	00	VMID Divider Enable and Select 00 = VMID disabled (for OFF mode) 01 = 2 x 40kohm divider (for normal operation) 10 = 2 x 240kohm divider (for low power standby) 11 = 2 x 5kohm divider (for fast start-up)	
	0	BIAS_ENA	0	Enables the Normal bias current generator (for all analogue functions) 0 = Disabled 1 = Enabled	

Register 01h Power Management (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R2 (02h) Power Management (2)	14	TSHUT_ENA	1	Thermal sensor enable 0 = disabled 1 = enabled	
	13	TSHUT_OPDIS	1	Thermal shutdown control (Causes audio outputs to be disabled if an overtemperature occurs. The thermal sensor must also be enabled.) 0 = disabled 1 = enabled	
	11	OPCLK_ENA	0	GPIO Clock Output (OPCLK) Enable 0 = Disabled 1 = Enabled	
	9	MIXINL_ENA	0	Left Input Mixer Enable (Enables MIXINL and RXVOICE input to MIXINL) 0 = Disabled 1 = Enabled	
	8	MIXINR_ENA	0	Right Input Mixer Enable (Enables MIXINR and RXVOICE input to MIXINR) 0 = Disabled 1 = Enabled	
	7	IN2L_ENA	0	IN2L Input PGA Enable 0 = Disabled 1 = Enabled	
	6	IN1L_ENA	0	IN1L Input PGA Enable 0 = Disabled 1 = Enabled	
	5	IN2R_ENA	0	IN2R Input PGA Enable 0 = Disabled 1 = Enabled	
	4	IN1R_ENA	0	IN1R Input PGA Enable 0 = Disabled 1 = Enabled	

Register 02h Power Management (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R3 (03h) Power Management (3)	13	LINEOUT1N_ENA	0	LINEOUT1N Line Out and LINEOUT1NMIX Enable 0 = Disabled 1 = Enabled	
	12	LINEOUT1P_ENA	0	LINEOUT1P Line Out and LINEOUT1PMIX Enable 0 = Disabled 1 = Enabled	
	11	LINEOUT2N_ENA	0	LINEOUT2N Line Out and LINEOUT2NMIX Enable 0 = Disabled 1 = Enabled	
	10	LINEOUT2P_ENA	0	LINEOUT2P Line Out and LINEOUT2PMIX Enable 0 = Disabled 1 = Enabled	
	9	SPKRVOL_ENA	0	SPKMIXR Mixer and SPKRVOL PGA Enable 0 = Disabled 1 = Enabled Note that SPKMIXR and SPKRVOL are also enabled when SPKOUTR_ENA is set.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	8	SPKLVOL_ENA	0	SPKMIXL Mixer and SPKLVOL PGA Enable 0 = Disabled 1 = Enabled Note that SPKMIXL and SPKLVOL are also enabled when SPKOUTL_ENA is set.	
	7	MIXOUTLVOL_ENA	0	MIXOUTL Left Volume Control Enable 0 = Disabled 1 = Enabled	
	6	MIXOUTRVOL_ENA	0	MIXOUTR Right Volume Control Enable 0 = Disabled 1 = Enabled	
	5	MIXOUTL_ENA	0	MIXOUTL Left Output Mixer Enable 0 = Disabled 1 = Enabled	
	4	MIXOUTR_ENA	0	MIXOUTR Right Output Mixer Enable 0 = Disabled 1 = Enabled	

Register 03h Power Management (3)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R4 (04h) Power Management (4)	13	AIF2ADCL_ENA	0	Enable AIF2ADC (Left) output path 0 = Disabled 1 = Enabled	
	12	AIF2ADCR_ENA	0	Enable AIF2ADC (Right) output path 0 = Disabled 1 = Enabled	
	11	AIF1ADC2L_ENA	0	Enable AIF1ADC2 (Left) output path (AIF1, Timeslot 1) 0 = Disabled 1 = Enabled	
	10	AIF1ADC2R_ENA	0	Enable AIF1ADC2 (Right) output path (AIF1, Timeslot 1) 0 = Disabled 1 = Enabled	
	9	AIF1ADC1L_ENA	0	Enable AIF1ADC1 (Left) output path (AIF1, Timeslot 0) 0 = Disabled 1 = Enabled	
	8	AIF1ADC1R_ENA	0	Enable AIF1ADC1 (Right) output path (AIF1, Timeslot 0) 0 = Disabled 1 = Enabled	
	5	DMIC2L_ENA	0	Digital microphone DMICDAT2 Left channel enable 0 = Disabled 1 = Enabled	
	4	DMIC2R_ENA	0	Digital microphone DMICDAT2 Right channel enable 0 = Disabled 1 = Enabled	
	3	DMIC1L_ENA	0	Digital microphone DMICDAT1 Left channel enable 0 = Disabled 1 = Enabled	
	2	DMIC1R_ENA	0	Digital microphone DMICDAT1 Right channel enable 0 = Disabled 1 = Enabled	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	1	ADCL_ENA	0	Left ADC Enable 0 = ADC disabled 1 = ADC enabled	
	0	ADCR_ENA	0	Right ADC Enable 0 = ADC disabled 1 = ADC enabled	

Register 04h Power Management (4)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R5 (05h) Power Management (5)	13	AIF2DACL_ENA	0	Enable AIF2DAC (Left) input path 0 = Disabled 1 = Enabled	
	12	AIF2DACR_ENA	0	Enable AIF2DAC (Right) input path 0 = Disabled 1 = Enabled	
	11	AIF1DAC2L_ENA	0	Enable AIF1DAC2 (Left) input path (AIF1, Timeslot 1) 0 = Disabled 1 = Enabled	
	10	AIF1DAC2R_ENA	0	Enable AIF1DAC2 (Right) input path (AIF1, Timeslot 1) 0 = Disabled 1 = Enabled	
	9	AIF1DAC1L_ENA	0	Enable AIF1DAC1 (Left) input path (AIF1, Timeslot 0) 0 = Disabled 1 = Enabled	
	8	AIF1DAC1R_ENA	0	Enable AIF1DAC1 (Right) input path (AIF1, Timeslot 0) 0 = Disabled 1 = Enabled	
	3	DAC2L_ENA	0	Left DAC2 Enable 0 = Disabled 1 = Enabled	
	2	DAC2R_ENA	0	Right DAC2 Enable 0 = Disabled 1 = Enabled	
	1	DAC1L_ENA	0	Left DAC1 Enable 0 = Disabled 1 = Enabled	
	0	DAC1R_ENA	0	Right DAC1 Enable 0 = Disabled 1 = Enabled	

Register 05h Power Management (5)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R6 (06h) Power Management (6)	5	AIF3_TRIS	0	AIF3 Audio Interface tri-state 0 = AIF3 pins operate normally 1 = Tri-state all AIF3 interface pins Note that pins not configured as AIF3 functions are not affected by this register.	
	4:3	AIF3_ADCDAT_SRC[1:0]	00	GPIO9/ADCDAT3 Source select 00 = AIF1 ADCDAT1 01 = AIF2 ADCDAT2	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				10 = GPIO5/DACDAT2 11 = Reserved Note that GPIO9 must be configured as ADCDAT3. For selection 11, the GPIO5 pin must also be configured as DACDAT2.	
	2	AIF2_ADCDAT_SRC	0	GPIO7/ADCDAT2 Source select 0 = AIF2 ADCDAT2 1 = GPIO8/DACDAT3 Note that GPIO7 must be configured as ADCDAT2. For selection 1, the GPIO8 pin must also be configured as DACDAT3.	
	1	AIF2_DACDAT_SRC	0	AIF2 DACDAT Source select 0 = GPIO5/DACDAT2 1 = GPIO8/DACDAT3 Note that the selected source must be configured as DACDAT2 or DACDAT3.	
	0	AIF1_DACDAT_SRC	0	AIF1 DACDAT Source select 0 = DACDAT1 1 = GPIO8/DACDAT3 Note that, for selection 1, the GPIO8 pin must be configured as DACDAT3.	

Register 06h Power Management (6)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R21 (15h) Input Mixer (1)	6	INPUTS_CLAMP	0	Input pad VMID clamp 0 = Clamp de-activated 1 = Clamp activated	

Register 15h Input Mixer (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R24 (18h) Left Line Input 1&2 Volume	8	IN1_VU	0	Input PGA Volume Update Writing a 1 to this bit will cause IN1L and IN1R input PGA volumes to be updated simultaneously	
	7	IN1L_MUTE	1	IN1L PGA Mute 0 = Disable Mute 1 = Enable Mute	
	6	IN1L_ZC	0	IN1L PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only	
	4:0	IN1L_VOL[4:0]	0_1011	IN1L Volume 00000 = -16.5dB 00001 = -15dB ... 11110 = +28.5dB 11111 = +30dB	

Register 18h Left Line Input 1&2 Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R25 (19h) Left Line Input 3&4 Volume	8	IN2_VU	0	Input PGA Volume Update Writing a 1 to this bit will cause IN2L and IN2R input PGA volumes to be updated simultaneously	
	7	IN2L_MUTE	1	IN2L PGA Mute 0 = Disable Mute 1 = Enable Mute	
	6	IN2L_ZC	0	IN2L PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only	
	4:0	IN2L_VOL[4:0]	0_1011	IN2L Volume 00000 = -16.5dB 00001 = -15dB ... 11110 = +28.5dB 11111 = +30dB	

Register 19h Left Line Input 3&4 Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R26 (1Ah) Right Line Input 1&2 Volume	8	IN1_VU	0	Input PGA Volume Update Writing a 1 to this bit will cause IN1L and IN1R input PGA volumes to be updated simultaneously	
	7	IN1R_MUTE	1	IN1R PGA Mute 0 = Disable Mute 1 = Enable Mute	
	6	IN1R_ZC	0	IN1R PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only	
	4:0	IN1R_VOL[4:0]	0_1011	IN1R Volume 00000 = -16.5dB 00001 = -15dB ... 11110 = +28.5dB 11111 = +30dB	

Register 1Ah Right Line Input 1&2 Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R27 (1Bh) Right Line Input 3&4 Volume	8	IN2_VU	0	Input PGA Volume Update Writing a 1 to this bit will cause IN2L and IN2R input PGA volumes to be updated simultaneously	
	7	IN2R_MUTE	1	IN2R PGA Mute 0 = Disable Mute 1 = Enable Mute	
	6	IN2R_ZC	0	IN2R PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4:0	IN2R_VOL[4:0]	0_1011	IN2R Volume 00000 = -16.5dB 00001 = -15dB ... 11110 = +28.5dB 11111 = +30dB	

Register 1Bh Right Line Input 3&4 Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R28 (1Ch) Left Output Volume	8	HPOUT1_VU	0	Headphone Output PGA Volume Update Writing a 1 to this bit will update HPOUT1LVOL and HPOUT1RVOL volumes simultaneously.	
	7	HPOUT1L_ZC	0	HPOUT1LVOL (Left Headphone Output PGA) Zero Cross Enable 0 = Zero cross disabled 1 = Zero cross enabled	
	6	HPOUT1L_MUTE_N	1	HPOUT1LVOL (Left Headphone Output PGA) Mute 0 = Mute 1 = Un-mute	
	5:0	HPOUT1L_VOL[5:0]	10_1101	HPOUT1LVOL (Left Headphone Output PGA) Volume -57dB to +6dB in 1dB steps 00_0000 = -57dB 00_0001 = -56dB … (1dB steps) 11_1111 = +6dB	

Register 1Ch Left Output Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R29 (1Dh) Right Output Volume	8	HPOUT1_VU	0	Headphone Output PGA Volume Update Writing a 1 to this bit will update HPOUT1LVOL and HPOUT1RVOL volumes simultaneously.	
	7	HPOUT1R_ZC	0	HPOUT1RVOL (Right Headphone Output PGA) Zero Cross Enable 0 = Zero cross disabled 1 = Zero cross enabled	
	6	HPOUT1R_MUTE_N	1	HPOUT1RVOL (Right Headphone Output PGA) Mute 0 = Mute 1 = Un-mute	
	5:0	HPOUT1R_VOL[5:0]	10_1101	HPOUT1RVOL (Right Headphone Output PGA) Volume -57dB to +6dB in 1dB steps 00_0000 = -57dB 00_0001 = -56dB … (1dB steps) 11_1111 = +6dB	

Register 1Dh Right Output Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30 (1Eh) Line Outputs Volume	6	LINEOUT1N_MUTE	1	LINEOUT1N Line Output Mute 0 = Un-mute 1 = Mute	
	5	LINEOUT1P_MUTE	1	LINEOUT1P Line Output Mute 0 = Un-mute 1 = Mute	
	4	LINEOUT1_VOL	0	LINEOUT1 Line Output Volume 0 = 0dB 1 = -6dB Applies to both LINEOUT1N and LINEOUT1P	
	2	LINEOUT2N_MUTE	1	LINEOUT2N Line Output Mute 0 = Un-mute 1 = Mute	
	1	LINEOUT2P_MUTE	1	LINEOUT2P Line Output Mute 0 = Un-mute 1 = Mute	
	0	LINEOUT2_VOL	0	LINEOUT2 Line Output Volume 0 = 0dB 1 = -6dB Applies to both LINEOUT2N and LINEOUT2P	

Register 1Eh Line Outputs Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R31 (1Fh) HPOUT2 Volume	5	HPOUT2_MUTE	1	HPOUT2 (Earpiece Driver) Mute 0 = Un-mute 1 = Mute	
	4	HPOUT2_VOL	0	HPOUT2 (Earpiece Driver) Volume 0 = 0dB 1 = -6dB	

Register 1Fh HPOUT2 Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R32 (20h) Left OPGA Volume	8	MIXOUT_VU	0	Mixer Output PGA Volume Update Writing a 1 to this bit will update MIXOUTLVOL and MIXOUTRVOL volumes simultaneously.	
	7	MIXOUTL_ZC	0	MIXOUTLVOL (Left Mixer Output PGA) Zero Cross Enable 0 = Zero cross disabled 1 = Zero cross enabled	
	6	MIXOUTL_MUTE_N	1	MIXOUTLVOL (Left Mixer Output PGA) Mute 0 = Mute 1 = Un-mute	
	5:0	MIXOUTL_VOL [5:0]	11_1001	MIXOUTLVOL (Left Mixer Output PGA) Volume -57dB to +6dB in 1dB steps 00_0000 = -57dB 00_0001 = -56dB … (1dB steps) 11_1111 = +6dB	

Register 20h Left OPGA Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R33 (21h) Right OPGA Volume	8	MIXOUT_VU	0	Mixer Output PGA Volume Update Writing a 1 to this bit will update MIXOUTLVOL and MIXOUTRVOL volumes simultaneously.	
	7	MIXOUTR_ZC	0	MIXOUTRVOL (Right Mixer Output PGA) Zero Cross Enable 0 = Zero cross disabled 1 = Zero cross enabled	
	6	MIXOUTR_MUTE_N	1	MIXOUTLVOL (Right Mixer Output PGA) Mute 0 = Mute 1 = Un-mute	
	5:0	MIXOUTR_VOL[5:0]	11_1001	MIXOUTRVOL (Right Mixer Output PGA) Volume -57dB to +6dB in 1dB steps 00_0000 = -57dB 00_0001 = -56dB … (1dB steps) 11_1111 = +6dB	

Register 21h Right OPGA Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R34 (22h) SPKMIXL Attenuation	6	DAC2L_SPKMIXL_VOL	0	Left DAC2 to SPKMIXL Fine Volume Control 0 = 0dB 1 = -3dB	
	5	MIXINL_SPKMIXL_VOL	0	MIXINL (Left ADC bypass) to SPKMIXL Fine Volume Control 0 = 0dB 1 = -3dB	
	4	IN1LP_SPKMIXL_VOL	0	IN1LP to SPKMIXL Fine Volume Control 0 = 0dB 1 = -3dB	
	3	MIXOUTL_SPKMIXL_VOL	0	Left Mixer Output to SPKMIXL Fine Volume Control 0 = 0dB 1 = -3dB	
	2	DAC1L_SPKMIXL_VOL	0	Left DAC1 to SPKMIXL Fine Volume Control 0 = 0dB 1 = -3dB	
	1:0	SPKMIXL_VOL[1:0]	11	Left Speaker Mixer Volume Control 00 = 0dB 01 = -6dB 10 = -12dB 11 = mute	

Register 22h SPKMIXL Attenuation

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R35 (23h) SPKMIXR Attenuation	8	SPKOUT_CLASSAB	0	Speaker Class AB Mode Enable 0 = Class D mode 1 = Class AB mode	
	6	DAC2R_SPKMIXR_VOL	0	Right DAC2 to SPKMIXR Fine Volume Control 0 = 0dB 1 = -3dB	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	5	MIXINR_SPKMIXR_VOL	0	MIXINR (Right ADC bypass) to SPKMIXR Fine Volume Control 0 = 0dB 1 = -3dB	
	4	IN1RP_SPKMIXR_VOL	0	IN1RP to SPKMIXR Fine Volume Control 0 = 0dB 1 = -3dB	
	3	MIXOUTR_SPKMIXR_VOL	0	Right Mixer Output to SPKMIXR Fine Volume Control 0 = 0dB 1 = -3dB	
	2	DAC1R_SPKMIXR_VOL	0	Right DAC1 to SPKMIXR Fine Volume Control 0 = 0dB 1 = -3dB	
	1:0	SPKMIXR_VOL[1:0]	11	Right Speaker Mixer Volume Control 00 = 0dB 01 = -6dB 10 = -12dB 11 = mute	

Register 23h SPKMIXR Attenuation

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R36 (24h) SPKOUT Mixers	5	IN2LP_TO_SPKOUTL	0	Differential Input (IN2RP/IN2LP) to Left Speaker Mute 0 = Mute 1 = Un-mute	
	4	SPKMIXL_TO_SPKOUTL	1	SPKMIXL Left Speaker Mixer to Left Speaker Mute 0 = Mute 1 = Un-mute	
	3	SPKMIXR_TO_SPKOUTL	0	SPKMIXR Right Speaker Mixer to Left Speaker Mute 0 = Mute 1 = Un-mute	
	2	IN2LP_TO_SPKOUTR	0	Differential Input (IN2RP/IN2LP) to Right Speaker Mute 0 = Mute 1 = Un-mute	
	1	SPKMIXL_TO_SPKOUTR	0	SPKMIXL Left Speaker Mixer to Right Speaker Mute 0 = Mute 1 = Un-mute	
	0	SPKMIXR_TO_SPKOUTR	1	SPKMIXR Right Speaker Mixer to Right Speaker Mute 0 = Mute 1 = Un-mute	

Register 24h SPKOUT Mixers

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R37 (25h) ClassD	5:3	SPKOUTL_BOOST[2:0]	000	Left Speaker Gain Boost 000 = 1.00x boost (+0dB) 001 = 1.19x boost (+1.5dB) 010 = 1.41x boost (+3.0dB) 011 = 1.68x boost (+4.5dB) 100 = 2.00x boost (+6.0dB) 101 = 2.37x boost (+7.5dB) 110 = 2.81x boost (+9.0dB) 111 = 3.98x boost (+12.0dB)	
	2:0	SPKOUTR_BOOST[2:0]	000	Right Speaker Gain Boost 000 = 1.00x boost (+0dB) 001 = 1.19x boost (+1.5dB) 010 = 1.41x boost (+3.0dB) 011 = 1.68x boost (+4.5dB) 100 = 2.00x boost (+6.0dB) 101 = 2.37x boost (+7.5dB) 110 = 2.81x boost (+9.0dB) 111 = 3.98x boost (+12.0dB)	

Register 25h ClassD

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R38 (26h) Speaker Volume Left	8	SPKOUT_VU	0	Speaker Output PGA Volume Update Writing a 1 to this bit will update SPKLVOL and SPKRVOL volumes simultaneously.	
	7	SPKOUTL_ZC	0	SPKLVOL (Left Speaker Output PGA) Zero Cross Enable 0 = Zero cross disabled 1 = Zero cross enabled	
	6	SPKOUTL_MUTE_N	1	SPKLVOL (Left Speaker Output PGA) Mute 0 = Mute 1 = Un-mute	
	5:0	SPKOUTL_VOL[5:0]	11_1001	SPKLVOL (Left Speaker Output PGA) Volume -57dB to +6dB in 1dB steps 00_0000 = -57dB 00_0001 = -56dB … (1dB steps) 11_1111 = +6dB	

Register 26h Speaker Volume Left

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R39 (27h) Speaker Volume Right	8	SPKOUT_VU	0	Speaker PGA Volume Update Writing a 1 to this bit will update SPKLVOL and SPKRVOL volumes simultaneously.	
	7	SPKOUTR_ZC	0	SPKRVOL (Right Speaker Output PGA) Zero Cross Enable 0 = Zero cross disabled 1 = Zero cross enabled	
	6	SPKOUTR_MUTE_N	1	SPKRVOL (Right Speaker Output PGA) Mute 0 = Mute 1 = Un-mute	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	5:0	SPKOUTR_VOL[5:0]	11_1001	SPKRVOL (Right Speaker Output PGA) Volume -57dB to +6dB in 1dB steps 00_0000 = -57dB 00_0001 = -56dB … (1dB steps) 11_1111 = +6dB	

Register 27h Speaker Volume Right

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R40 (28h) Input Mixer (2)	7	IN2LP_TO_IN2L	0	IN2L PGA Non-Inverting Input Select 0 = Connected to VMID 1 = Connected to IN2LP	
	6	IN2LN_TO_IN2L	0	IN2L PGA Inverting Input Select 0 = Not connected 1 = Connected to IN2LN	
	5	IN1LP_TO_IN1L	0	IN1L PGA Non-Inverting Input Select 0 = Connected to VMID 1 = Connected to IN1LP	
	4	IN1LN_TO_IN1L	0	IN1L PGA Inverting Input Select 0 = Not connected 1 = Connected to IN1LN	
	3	IN2RP_TO_IN2R	0	IN2R PGA Non-Inverting Input Select 0 = Connected to VMID 1 = Connected to IN2RP	
	2	IN2RN_TO_IN2R	0	IN2R PGA Inverting Input Select 0 = Not connected 1 = Connected to IN2RN	
	1	IN1RP_TO_IN1R	0	IN1R PGA Non-Inverting Input Select 0 = Connected to VMID 1 = Connected to IN1RP	
	0	IN1RN_TO_IN1R	0	IN1R PGA Inverting Input Select 0 = Not connected 1 = Connected to IN1RN	

Register 28h Input Mixer (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R41 (29h) Input Mixer (3)	8	IN2L_TO_MIXINL	0	IN2L PGA Output to MIXINL Mute 0 = Mute 1 = Un-Mute	
	7	IN2L_MIXINL_VOL	0	IN2L PGA Output to MIXINL Gain 0 = 0dB 1 = +30dB	
	5	IN1L_TO_MIXINL	0	IN1L PGA Output to MIXINL Mute 0 = Mute 1 = Un-Mute	
	4	IN1L_MIXINL_VOL	0	IN1L PGA Output to MIXINL Gain 0 = 0dB 1 = +30dB	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	2:0	MIXOUTL_MIXINL_VOL[2:0]	000	Record Path MIXOUTL to MIXINL Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB	

Register 29h Input Mixer (3)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R42 (2Ah) Input Mixer (4)	8	IN2R_TO_MIXINR	0	IN2R PGA Output to MIXINR Mute 0 = Mute 1 = Un-Mute	
	7	IN2R_MIXINR_VOL	0	IN2R PGA Output to MIXINR Gain 0 = 0dB 1 = +30dB	
	5	IN1R_TO_MIXINR	0	IN1R PGA Output to MIXINR Mute 0 = Mute 1 = Un-Mute	
	4	IN1R_MIXINR_VOL	0	IN1R PGA Output to MIXINR Gain 0 = 0dB 1 = +30dB	
	2:0	MIXOUTR_MIXINR_VOL[2:0]	000	Record Path MIXOUTR to MIXINR Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB	

Register 2Ah Input Mixer (4)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R43 (2Bh) Input Mixer (5)	8:6	IN1LP_MIXINL_VOL[2:0]	000	IN1LP Pin (PGA Bypass) to MIXINL Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	2:0	IN2LP_MIXINL_VOL[2:0]	000	RXVOICE (VRXN/VRXP) Differential Input to MIXINL Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB	

Register 2Bh Input Mixer (5)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R44 (2Ch) Input Mixer (6)	8:6	IN1RP_MIXINR_VOL[2:0]	000	IN1RP Pin (PGA Bypass) to MIXINR Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB	
	2:0	IN2LP_MIXINR_VOL[2:0]	000	RXVOICE (VRXN/VRXP) Differential Input to MIXINR Gain and Mute 000 = Mute 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB	

Register 2Ch Input Mixer (6)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R45 (2Dh) Output Mixer (1)	8	DAC1L_TO_HPOUT1L	0	HPOUT1LVOL (Left Headphone Output PGA) Input Select 0 = MIXOUTL 1 = DAC1L	
	7	MIXINR_TO_MIXOUTL	0	MIXINR Output (Right ADC bypass) to MIXOUTL Mute 0 = Mute 1 = Un-mute	
	6	MIXINL_TO_MIXOUTL	0	MIXINL Output (Left ADC bypass) to MIXOUTL Mute 0 = Mute 1 = Un-mute	
	5	IN2RN_TO_MIXOUTL	0	IN2RN to MIXOUTL Mute 0 = Mute 1 = Un-mute	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4	IN2LN_TO_MIXOUTL	0	IN2LN to MIXOUTL Mute 0 = Mute 1 = Un-mute	
	3	IN1R_TO_MIXOUTL	0	IN1R PGA Output to MIXOUTL Mute 0 = Mute 1 = Un-mute	
	2	IN1L_TO_MIXOUTL	0	IN1L PGA Output to MIXOUTL Mute 0 = Mute 1 = Un-mute	
	1	IN2LP_TO_MIXOUTL	0	IN2LP to MIXOUTL Mute 0 = Mute 1 = Un-mute	
	0	DAC1L_TO_MIXOUTL	0	Left DAC1 to MIXOUTL Mute 0 = Mute 1 = Un-mute	

Register 2Dh Output Mixer (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R46 (2Eh) Output Mixer (2)	8	DAC1R_TO_HPOUT1R	0	HPOUT1RVOL (Right Headphone Output PGA) Input Select 0 = MIXOUTR 1 = DAC1R	
	7	MIXINL_TO_MIXOUTR	0	MIXINL Output (Left ADC bypass) to MIXOUTR Mute 0 = Mute 1 = Un-mute	
	6	MIXINR_TO_MIXOUTR	0	MIXINR Output (Right ADC bypass) to MIXOUTR Mute 0 = Mute 1 = Un-mute	
	5	IN2LN_TO_MIXOUTR	0	IN2LN to MIXOUTR Mute 0 = Mute 1 = Un-mute	
	4	IN2RN_TO_MIXOUTR	0	IN2RN to MIXOUTR Mute 0 = Mute 1 = Un-mute	
	3	IN1L_TO_MIXOUTR	0	IN1L PGA Output to MIXOUTR Mute 0 = Mute 1 = Un-mute	
	2	IN1R_TO_MIXOUTR	0	IN1R PGA Output to MIXOUTR Mute 0 = Mute 1 = Un-mute	
	1	IN2RP_TO_MIXOUTR	0	IN2RP to MIXOUTR Mute 0 = Mute 1 = Un-mute	
	0	DAC1R_TO_MIXOUTR	0	Right DAC1 to MIXOUTR Mute 0 = Mute 1 = Un-mute	

Register 2Eh Output Mixer (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R47 (2Fh) Output Mixer (3)	11:9	IN2LP_MIXOUTL_VOL[2:0]	000	IN2LP to MIXOUTL Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB	
	8:6	IN2LN_MIXOUTL_VOL[2:0]	000	IN2LN to MIXOUTL Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB	
	5:3	IN1R_MIXOUTL_VOL[2:0]	000	IN1R PGA Output to MIXOUTL Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB	
	2:0	IN1L_MIXOUTL_VOL[2:0]	000	IN1L PGA Output to MIXOUTL Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB	

Register 2Fh Output Mixer (3)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R48 (30h) Output Mixer (4)	11:9	IN2RP_MIXOUTR_VOL[2:0]	000	IN2RP to MIXOUTR Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB	
	8:6	IN2RN_MIXOUTR_VOL[2:0]	000	IN2RN to MIXOUTR Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB	
	5:3	IN1L_MIXOUTR_VOL[2:0]	000	IN1L PGA Output to MIXOUTR Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB	
	2:0	IN1R_MIXOUTR_VOL[2:0]	000	IN1R PGA Output to MIXOUTR Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB	

Register 30h Output Mixer (4)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R49 (31h) Output Mixer (5)	11:9	DACL_MIXOUTL_VOL[2:0]	000	Left DAC1 to MIXOUTL Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB	
	8:6	IN2RN_MIXOUTL_VOL[2:0]	000	IN2RN to MIXOUTL Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB	
	5:3	MIXINR_MIXOUTL_VOL[2:0]	000	MIXINR Output (Right ADC bypass) to MIXOUTL Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB	
	2:0	MIXINL_MIXOUTL_VOL[2:0]	000	MIXINL Output (Left ADC bypass) to MIXOUTL Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB	

Register 31h Output Mixer (5)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R50 (32h) Output Mixer (6)	11:9	DACR_MIXOUTR_VOL[2:0]	000	Right DAC1 to MIXOUTR Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB	
	8:6	IN2LN_MIXOUTR_VOL[2:0]	000	IN2LN to MIXOUTR Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB	
	5:3	MIXINL_MIXOUTR_VOL[2:0]	000	MIXINL Output (Left ADC bypass) to MIXOUTR Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	2:0	MIXINR_MIXOUTR_VOL[2:0]	000	MIXINR Output (Right ADC bypass) to MIXOUTR Volume 0dB to -21dB in 3dB steps 000 = 0dB 001 = -3dB …(3dB steps) 111 = -21dB	

Register 32h Output Mixer (6)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R51 (33h) HPOUT2 Mixer	5	IN2LRP_TO_HPOUT2	0	Differential Input (IN2RP/IN2LP) to Earpiece Driver 0 = Mute 1 = Un-mute	
	4	MIXOUTLVOL_TO_HPOUT2	0	MIXOUTLVOL (Left Output Mixer PGA) to Earpiece Driver 0 = Mute 1 = Un-mute	
	3	MIXOUTRVOL_TO_HPOUT2	0	MIXOUTRVOL (Right Output Mixer PGA) to Earpiece Driver 0 = Mute 1 = Un-mute	

Register 33h HPOUT2 Mixer

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R52 (34h) Line Mixer (1)	6	MIXOUTL_TO_LINEOUT1N	0	MIXOUTL to Single-Ended Line Output on LINEOUT1N 0 = Mute 1 = Un-mute (LINEOUT1_MODE = 1)	
	5	MIXOUTR_TO_LINEOUT1N	0	MIXOUTR to Single-Ended Line Output on LINEOUT1N 0 = Mute 1 = Un-mute (LINEOUT1_MODE = 1)	
	4	LINEOUT1_MODE	0	LINEOUT1 Mode Select 0 = Differential 1 = Single-Ended	
	2	IN1R_TO_LINEOUT1P	0	IN1R Input PGA to Differential Line Output on LINEOUT1 0 = Mute 1 = Un-mute (LINEOUT1_MODE = 0)	
	1	IN1L_TO_LINEOUT1P	0	IN1L Input PGA to Differential Line Output on LINEOUT1 0 = Mute 1 = Un-mute (LINEOUT1_MODE = 0)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	0	MIXOUTL_TO_LINEOUT1P	0	Differential Mode (LINEOUT1_MODE = 0): MIXOUTL to Differential Output on LINEOUT1 0 = Mute 1 = Un-mute Single Ended Mode (LINEOUT1_MODE = 1): MIXOUTL to Single-Ended Line Output on LINEOUT1P 0 = Mute 1 = Un-mute	

Register 34h Line Mixer (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R53 (35h) Line Mixer (2)	6	MIXOUTR_TO_LINEOUT2N	0	MIXOUTR to Single-Ended Line Output on LINEOUT2N 0 = Mute 1 = Un-mute (LINEOUT2_MODE = 1)	
	5	MIXOUTL_TO_LINEOUT2N	0	MIXOUTL to Single-Ended Line Output on LINEOUT2N 0 = Mute 1 = Un-mute (LINEOUT2_MODE = 1)	
	4	LINEOUT2_MODE	0	LINEOUT2 Mode Select 0 = Differential 1 = Single-Ended	
	2	IN1L_TO_LINEOUT2P	0	IN1L Input PGA to Differential Line Output on LINEOUT2 0 = Mute 1 = Un-mute (LINEOUT2_MODE = 0)	
	1	IN1R_TO_LINEOUT2P	0	IN1R Input PGA to Differential Line Output on LINEOUT2 0 = Mute 1 = Un-mute (LINEOUT2_MODE = 0)	
	0	MIXOUTR_TO_LINEOUT2P	0	Differential Mode (LINEOUT2_MODE = 0): MIXOUTR to Differential Output on LINEOUT2 0 = Mute 1 = Un-mute Single-Ended Mode (LINEOUT2_MODE = 0): MIXOUTR to Single-Ended Line Output on LINEOUT2P 0 = Mute 1 = Un-mute	

Register 35h Line Mixer (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R54 (36h) Speaker Mixer	9	DAC2L_TO_SPKMIXL	0	Left DAC2 to SPKMIXL Mute 0 = Mute 1 = Un-mute	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	8	DAC2R_TO_SPKMIXR	0	Right DAC2 to SPKMIXR Mute 0 = Mute 1 = Un-mute	
	7	MIXINL_TO_SPKMIXL	0	MIXINL (Left ADC bypass) to SPKMIXL Mute 0 = Mute 1 = Un-mute	
	6	MIXINR_TO_SPKMIXR	0	MIXINR (Right ADC bypass) to SPKMIXR Mute 0 = Mute 1 = Un-mute	
	5	IN1LP_TO_SPKMIXL	0	IN1LP to SPKMIXL Mute 0 = Mute 1 = Un-mute	
	4	IN1RP_TO_SPKMIXR	0	IN1RP to SPKMIXR Mute 0 = Mute 1 = Un-mute	
	3	MIXOUTL_TO_SPKMIXL	0	Left Mixer Output to SPKMIXL Mute 0 = Mute 1 = Un-mute	
	2	MIXOUTR_TO_SPKMIXR	0	Right Mixer Output to SPKMIXR Mute 0 = Mute 1 = Un-mute	
	1	DAC1L_TO_SPKMIXL	0	Left DAC1 to SPKMIXL Mute 0 = Mute 1 = Un-mute	
	0	DAC1R_TO_SPKMIXR	0	Right DAC1 to SPKMIXR Mute 0 = Mute 1 = Un-mute	

Register 36h Speaker Mixer

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R55 (37h) Additional Control	7	LINEOUT1_FB	0	Enable ground loop noise feedback on LINEOUT1 0 = Disabled 1 = Enabled	
	6	LINEOUT2_FB	0	Enable ground loop noise feedback on LINEOUT2 0 = Disabled 1 = Enabled	
	0	VROI	0	Buffered VMID to Analogue Line Output Resistance (Disabled Outputs) 0 = 20kohm from buffered VMID to output 1 = 500ohm from buffered VMID to output	

Register 37h Additional Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R56 (38h) AntiPOP (1)	7	LINEOUT_VMID_BUF_ENA	0	Enables VMID reference for line outputs in single-ended mode 0 = Disabled 1 = Enabled	
	6	HPOUT2_IN_ENA	0	HPOUT2MIX Mixer and Input Stage Enable 0 = Disabled 1 = Enabled	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	5	LINEOUT1_DISCH	0	Discharges LINEOUT1P and LINEOUT1N outputs via approx 4k□ resistor 0 = Not active 1 = Actively discharging LINEOUT1P and LINEOUT1N	
	4	LINEOUT2_DISCH	0	Discharges LINEOUT2P and LINEOUT2N outputs via approx 4k□ resistor 0 = Not active 1 = Actively discharging LINEOUT2P and LINEOUT2N	

Register 38h AntiPOP (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R57 (39h) AntiPOP (2)	6:5	VMID_RAMP[1:0]	00	VMID soft start enable / slew rate control 00 = Normal slow start 01 = Normal fast start 10 = Soft slow start 11 = Soft fast start	
	3	VMID_BUF_ENA	0	VMID Buffer Enable 0 = Disabled 1 = Enabled	
	2	STARTUP_BIAS_ENA	0	Enables the Start-Up bias current generator 0 = Disabled 1 = Enabled	
	1	BIAS_SRC	0	Selects the bias current source 0 = Normal bias 1 = Start-Up bias	
	0	VMID_DISCH	0	Connects VMID to ground 0 = Disabled 1 = Enabled	

Register 39h AntiPOP (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R58 (3Ah) MICBIAS	7:6	MICD_SCTHR[1:0]	00	MICBIAS Short Circuit Current threshold 00 = 300uA 01 = 600uA 10 = 1200uA 11 = 2400uA These values are for AVDD1=3.0V and scale proportionally with AVDD1.	
	5:3	MICD_THR[2:0]	000	MICBIAS Current Detect threshold 00 = 150uA 01 = 300uA 10 = 600uA 11 = 1200uA These values are for AVDD1=3.0V and scale proportionally with AVDD1.	
	2	MICD_ENA	0	MICBIAS Current Detect / Short Circuit Threshold enable 0 = disabled 1 = enabled	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	1	MICB2_LVL	0	Microphone Bias 2 Voltage Control 0 = 0.9 * AVDD1 1 = 0.65 * AVDD1	
	0	MICB1_LVL	0	Microphone Bias 1 Voltage Control 0 = 0.9 * AVDD1 1 = 0.65 * AVDD1	

Register 3Ah MICBIAS

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R59 (3Bh) LDO 1	3:1	LDO1_VSEL[2:0]	110	LDO1 Output Voltage Select 2.4V to 3.1V in 100mV steps 000 = 2.4V 001 = 2.5V 010 = 2.6V 011 = 2.7V 100 = 2.8V 101 = 2.9V 110 = 3.0V 111 = 3.1V	
	0	LDO1_DISCH	1	LDO1 Discharge Select 0 = LDO1 floating when disabled 1 = LDO1 discharged when disabled	

Register 3Bh LDO 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R60 (3Ch) LDO 2	2:1	LDO2_VSEL[1:0]	01	LDO2 Output Voltage Select 0.9V to 1.2V in 100mV steps 00 = 0.9V 01 = 1.0V 10 = 1.1V 11 = 1.2V	
	0	LDO2_DISCH	1	LDO2 Discharge Select 0 = LDO2 floating when disabled 1 = LDO2 discharged when disabled	

Register 3Ch LDO 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R76 (4Ch) Charge Pump (1)	15	CP_ENA	0	Enable charge-pump digits 0 = disable 1 = enable	

Register 4Ch Charge Pump (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R81 (51h) Class W (1)	9:8	CP_DYN_SRC_SEL[1:0]	00	Selects the digital audio source for envelope tracking 00 = AIF1, DAC Timeslot 0 01 = AIF1, DAC Timeslot 1 10 = AIF2, DAC data 11 = Reserved	
	0	CP_DYN_PWR	0	Enable dynamic charge pump power control 0 = charge pump controlled by volume register settings 1 = charge pump controlled by real-time audio level	

Register 51h Class W (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R84 (54h) DC Servo (1)	13	DCS_TRIG_SINGLE_1	0	Writing 1 to this bit selects a single DC offset correction for HPOUT1L. In readback, a value of 1 indicates that the DC Servo single correction is in progress.	
	12	DCS_TRIG_SINGLE_0	0	Writing 1 to this bit selects a single DC offset correction for HPOUT1R. In readback, a value of 1 indicates that the DC Servo single correction is in progress.	
	9	DCS_TRIG_SERIES_1	0	Writing 1 to this bit selects a series of DC offset corrections for HPOUT1L. In readback, a value of 1 indicates that the DC Servo DAC Write correction is in progress.	
	8	DCS_TRIG_SERIES_0	0	Writing 1 to this bit selects a series of DC offset corrections for HPOUT1R. In readback, a value of 1 indicates that the DC Servo DAC Write correction is in progress.	
	5	DCS_TRIG_STARTUP_1	0	Writing 1 to this bit selects Start-Up DC Servo mode for HPOUT1L. In readback, a value of 1 indicates that the DC Servo Start-Up correction is in progress.	
	4	DCS_TRIG_STARTUP_0	0	Writing 1 to this bit selects Start-Up DC Servo mode for HPOUT1R. In readback, a value of 1 indicates that the DC Servo Start-Up correction is in progress.	
	3	DCS_TRIG_DAC_WR_1	0	Writing 1 to this bit selects DAC Write DC Servo mode for HPOUT1L. In readback, a value of 1 indicates that the DC Servo DAC Write correction is in progress.	
	2	DCS_TRIG_DAC_WR_0	0	Writing 1 to this bit selects DAC Write DC Servo mode for HPOUT1R. In readback, a value of 1 indicates that the DC Servo DAC Write correction is in progress.	
	1	DCS_ENA_CHAN_1	0	DC Servo enable for HPOUT1L 0 = disabled 1 = enabled	
	0	DCS_ENA_CHAN_0	0	DC Servo enable for HPOUT1R 0 = disabled 1 = enabled	

Register 54h DC Servo (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R85 (55h) DC Servo (2)	11:5	DCS_SERIES_NO_01[6:0]	010_1010	Number of DC Servo updates to perform in a series event. 0 = 1 updates 1 = 2 updates ... 127 = 128 updates	
	3:0	DCS_TIMER_PERIOD_01[3:0]	1010	Time between periodic updates. Time is calculated as 0.251s x (2^PERIOD) 0000 = Off 0001 = 0.502s 1010 = 257s (4min 17s) 1111 = 8224s (2hr 17ms)	

Register 55h DC Servo (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R87 (57h) DC Servo (4)	15:8	DCS_DAC_WR_VAL_1[7:0]	0000_0000	DC Offset value for HPOUT1L in DAC Write DC Servo mode. Two's complement format. LSB is 0.25mV. Range is +/-32mV	
	7:0	DCS_DAC_WR_VAL_0[7:0]	0000_0000	DC Offset value for HPOUT1R in DAC Write DC Servo mode. Two's complement format. LSB is 0.25mV. Range is +/-32mV	

Register 57h DC Servo (4)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R88 (58h) DC Servo Readback	9:8	DCS_CAL_COMPLETE[1:0]	00	DC Servo Complete status 00 = DAC Write or Start-Up DC Servo mode not completed. 01 = DAC Write or Start-Up DC Servo mode complete on HPOUT1R only. 10 = DAC Write or Start-Up DC Servo mode complete on HPOUT1L only. 11 = DAC Write or Start-Up DC Servo mode complete on HPOUT1L and HPOUT1R.	
	5:4	DCS_DAC_WR_COMPLETE[1:0]	00	DC Servo DAC Write status 00 = DAC Write DC Servo mode not completed. 01 = DAC Write DC Servo mode complete on HPOUT1R only. 10 = DAC Write DC Servo mode complete on HPOUT1L only. 11 = DAC Write DC Servo mode complete on HPOUT1L and HPOUT1R.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	1:0	DCS_STARTUP_COMPLETE[1:0]	00	DC Servo Start-Up status 00 = Start-Up DC Servo mode not completed. 01 = Start-Up DC Servo mode complete on HPOUT1R only. 10 = Start-Up DC Servo mode complete on HPOUT1L only. 11 = Start-Up DC Servo mode complete on HPOUT1L and HPOUT1R.	

Register 58h DC Servo Readback

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R91 (5Bh) DC Servo ANA (1)	7:0	DCS_IDAC_VAL_1[7:0]	0000_0000	Readback value for HPOUT1L. Two's complement format. LSB is 0.25mV. Range is +/-32mV	

Register 5Bh DC Servo ANA (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R92 (5Ch) DC Servo ANA (2)	7:0	DCS_IDAC_VAL_0[7:0]	0000_0000	Readback value for HPOUT1R. Two's complement format. LSB is 0.25mV. Range is +/-32mV	

Register 5Ch DC Servo ANA (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R96 (60h) Analogue HP (1)	7	HPOUT1L_RMV_SHORT	0	Removes HPOUT1L short 0 = HPOUT1L short enabled 1 = HPOUT1L short removed Note: Remove short after output stage has been enabled.	
	6	HPOUT1L_OUTP	0	Enables HPOUT1L output stage 0 = Disabled 1 = Enabled Note: Set after offset correction is complete	
	5	HPOUT1L_DLY	0	Enables HPOUT1L intermediate stage 0 = Disabled 1 = Enabled Note: Set with at least 20us delay to HPOUT1L_ENA	
	3	HPOUT1R_RMV_SHORT	0	Removes HPOUT1R short 0 = HPOUT1R short enabled 1 = HPOUT1R short removed Note: Remove short after output stage has been enabled.	
	2	HPOUT1R_OUTP	0	Enables HPOUT1R output stage 0 = Disabled 1 = Enabled Note: Set after offset correction is complete	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	1	HPOUT1R_DLY	0	Enables HPOUT1R intermediate stage 0 = Disabled 1 = Enabled Note: Set with at least 20us delay to HPOUT1R_ENA	

Register 60h Analogue HP (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R257 (0101h) Control Interface	15	REG_SYNC	1	Control whether control writes are internally synchronoused to SYS_CLK, thereby avoiding cross-clock domain issues for multi-bit registers, such as volume controls. Normally this is handled automatically by the state of SYS_CLK_ENA, bit this allows the synchroniser to be disabled manually. 0: Synchroniser always disabled 1: Synchroniser enabled when SYS_CLK_ENA=1	
	6	SPI_CONTRD	0	Enable continuous read mode in SPI 3/4-wire 0: Disabled 1: Enabled	
	5	SPI_4WIRE	0	SPI control mode select 0 = 3-wire using bidirectional SDA 1 = 4-wire using SDOUT	
	4	SPI_CFG	0	SDA/SDOUT pin configuration 0 = CMOS 1 = Open Drain (SPI_4WIRE = 0) 1 = Wired 'OR' (SPI_4WIRE = 1)	
	2	AUTO_INC	1	Enables address auto-increment (applies to 2-wire I2C mode only) 0 = Disabled 1 = Enabled	

Register 0101h Control Interface

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R272 (0110h) Write Sequencer Ctrl (1)	15	WSEQ_ENA	0	Write Sequencer Enable. 0 = Disabled 1 = Enabled	
	9	WSEQ_ABORT	0	Writing a 1 to this bit aborts the current sequence and returns control of the device back to the serial control interface.	
	8	WSEQ_START	0	Writing a 1 to this bit starts the write sequencer at the index location selected by WSEQ_START_INDEX. The sequence continues until it reaches an "End of sequence" flag. At the end of the sequence, this bit will be reset by the Write Sequencer.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	6:0	WSEQ_START_INDEX[6:0]	000_0000	Sequence Start Index. This field determines the memory location of the first command in the selected sequence. There are 127 Write Sequencer RAM addresses: 00h = WSEQ_ADDR0 (R12288) 01h = WSEQ_ADDR1 (R12292) 02h = WSEQ_ADDR2 (R12296) …. 7Fh = WSEQ_ADDR127 (R12796)	

Register 0110h Write Sequencer Ctrl (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R273 (0111h) Write Sequencer Ctrl (2)	8	WSEQ_BUSY	0	Sequencer Busy flag (Read Only). 0 = Sequencer idle 1 = Sequencer busy Note: it is not possible to write to control registers via the control interface while the Sequencer is Busy.	
	6:0	WSEQ_CURRENT_INDEX[6:0]	000_0000	Sequence Current Index. This indicates the memory location of the most recently accessed command in the write sequencer memory. Coding is the same as WSEQ_START_INDEX.	

Register 0111h Write Sequencer Ctrl (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R512 (0200h) AIF1 Clocking (1)	4:3	AIF1CLK_SRC[1:0]	00	AIF1CLK Source Select 00 = MCLK1 01 = MCLK2 10 = FLL1 11 = FLL2	
	2	AIF1CLK_INV	0	AIF1CLK Invert 0 = AIF1CLK not inverted 1 = AIF1CLK inverted	
	1	AIF1CLK_DIV	0	AIF1CLK Divider 0 = AIF1CLK 1 = AIF1CLK / 2	
	0	AIF1CLK_ENA	0	AIF1CLK Enable 0 = Disabled 1 = Enabled	

Register 0200h AIF1 Clocking (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R513 (0201h) AIF1 Clocking (2)	5:3	AIF1DAC_DIV[2:0]	000	Selects the AIF1 input path sample rate relative to AIF1CLK. 000 = AIF1CLK 001 = AIF1CLK / 1.5 010 = AIF1CLK / 2 011 = AIF1CLK / 3 100 = AIF1CLK / 4 101 = AIF1CLK / 5.5 110 = AIF1CLK / 6 111 = Reserved Note that AIF1DAC_DIV must be set to 000 if AIF1ADC_DIV > 000.	
	2:0	AIF1ADC_DIV[2:0]	000	Selects the AIF1 output path sample rate relative to AIF1CLK. 000 = AIF1CLK 001 = AIF1CLK / 1.5 010 = AIF1CLK / 2 011 = AIF1CLK / 3 100 = AIF1CLK / 4 101 = AIF1CLK / 5.5 110 = AIF1CLK / 6 111 = Reserved Note that AIF1ADC_DIV must be set to 000 if AIF1DAC_DIV > 000.	

Register 0201h AIF1 Clocking (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R516 (0204h) AIF2 Clocking (1)	4:3	AIF2CLK_SRC[1:0]	00	AIF2CLK Source Select 00 = MCLK1 01 = MCLK2 10 = FLL1 11 = FLL2	
	2	AIF2CLK_INV	0	AIF2CLK Invert 0 = AIF2CLK not inverted 1 = AIF2CLK inverted	
	1	AIF2CLK_DIV	0	AIF2CLK Divider 0 = AIF2CLK 1 = AIF2CLK / 2	
	0	AIF2CLK_ENA	0	AIF2CLK Enable 0 = Disabled 1 = Enabled	

Register 0204h AIF2 Clocking (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R517 (0205h) AIF2 Clocking (2)	5:3	AIF2DAC_DIV[2:0]	000	Selects the AIF2 input path sample rate relative to AIF2CLK. 000 = AIF2CLK 001 = AIF2CLK / 1.5 010 = AIF2CLK / 2 011 = AIF2CLK / 3 100 = AIF2CLK / 4 101 = AIF2CLK / 5.5 110 = AIF2CLK / 6 111 = Reserved Note that AIF2DAC_DIV must be set to 000 if AIF2ADC_DIV > 000.	
	2:0	AIF2ADC_DIV[2:0]	000	Selects the AIF2 output path sample rate relative to AIF2CLK. 000 = AIF2CLK 001 = AIF2CLK / 1.5 010 = AIF2CLK / 2 011 = AIF2CLK / 3 100 = AIF2CLK / 4 101 = AIF2CLK / 5.5 110 = AIF2CLK / 6 111 = Reserved Note that AIF2ADC_DIV must be set to 000 if AIF2DAC_DIV > 000.	

Register 0205h AIF2 Clocking (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R520 (0208h) Clocking (1)	4	TOCLK_ENA	0	Slow Clock (TOCLK) Enable 0 = Disabled 1 = Enabled This clock is required for zero-cross timeout.	
	3	DSP_FS1CLK_ENA	0	AIF1 Processing Clock Enable 0 = Disabled 1 = Enabled	
	2	DSP_FS2CLK_ENA	0	AIF2 Processing Clock Enable 0 = Disabled 1 = Enabled	
	1	DSP_FSINTCLK_ENA	0	Digital Mixing Processor Clock Enable 0 = Disabled 1 = Enabled	
	0	SYSCLK_SRC	0	SYSCLK Source Select 0 = AIF1CLK 1 = AIF2CLK	

Register 0208h Clocking (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R521 (0209h) Clocking (2)	10:8	TOCLK_DIV[2:0]	000	Slow Clock (TOCLK) Divider (Sets TOCLK rate relative to 256kHz.) 000 = Divide by 256 (1kHz) 001 = Divide by 512 (500Hz) 010 = Divide by 1024 (250Hz) 011 = Divide by 2048 (125Hz) 100 = Divide by 4096 (62.5Hz) 101 = Divide by 8192 (31.2Hz) 110 = Divide by 16384 (15.6Hz) 111 = Divide by 32768 (7.8Hz)	
	6:4	DBCLK_DIV[2:0]	000	De-bounce Clock (DBCLK) Divider (Sets DBCLK rate relative to 256kHz.) 000 = Divide by 256 (1kHz) 001 = Divide by 2048 (125Hz) 010 = Divide by 4096 (62.5Hz) 011 = Divide by 8192 (31.2Hz) 100 = Divide by 16384 (15.6Hz) 101 = Divide by 32768 (7.8Hz) 110 = Divide by 65536 (3.9Hz) 111 = Divide by 131072 (1.95Hz)	
	2:0	OPCLK_DIV[2:0]	000	GPIO Output Clock (OPCLK) Divider 000 = SYSCLK 001 = SYSCLK / 2 010 = SYSCLK / 3 011 = SYSCLK / 4 100 = SYSCLK / 6 101 = SYSCLK / 8 110 = SYSCLK / 12 111 = SYSCLK / 16	

Register 0209h Clocking (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R528 (0210h) AIF1 Rate	7:4	AIF1_SR[3:0]	1000	Selects the AIF1 Sample Rate (fs) 0000 = 8kHz 0001 = 11.025kHz 0010 = 12kHz 0011 = 16kHz 0100 = 22.05kHz 0101 = 24kHz 0110 = 32kHz 0111 = 44.1kHz 1000 = 48kHz 1001 = 88.2kHz 1010 = 96kHz All other codes = Reserved Note that 88.2kHz and 96kHz modes are supported for AIF1 input (DAC playback) only.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	3:0	AIF1CLK_RATE[3:0]	0011	Selects the AIF1CLK / fs ratio 0000 = 64 0001 = 128 0010 = 192 0011 = 256 0100 = 384 0101 = 512 0110 = 768 0111 = 1024 1000 = 1408 1001 = 1536 All other codes = Reserved For Stereo DAC (AIF1 input) modes, the rate must be 128 x fs or higher. For ADC (AIF1 output) modes, the rate must be 256 x fs or higher.	

Register 0210h AIF1 Rate

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R529 (0211h) AIF2 Rate	7:4	AIF2_SR[3:0]	1000	Selects the AIF2 Sample Rate (fs) 0000 = 8kHz 0001 = 11.025kHz 0010 = 12kHz 0011 = 16kHz 0100 = 22.05kHz 0101 = 24kHz 0110 = 32kHz 0111 = 44.1kHz 1000 = 48kHz 1001 = 88.2kHz 1010 = 96kHz All other codes = Reserved Note that 88.2kHz and 96kHz modes are supported for AIF2 input (DAC playback) only.	
	3:0	AIF2CLK_RATE[3:0]	0011	Selects the AIF2CLK / fs ratio 0000 = 64 0001 = 128 0010 = 192 0011 = 256 0100 = 384 0101 = 512 0110 = 768 0111 = 1024 1000 = 1408 1001 = 1536 All other codes = Reserved For Stereo DAC (AIF2 input) modes, the rate must be 128 x fs or higher. For ADC (AIF2 output) modes, the rate must be 256 x fs or higher.	

Register 0211h AIF2 Rate

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R530 (0212h) Rate Status	3:0	SR_ERROR[3:0]	0000	Sample Rate Configuration status Indicates an error with the register settings related to sample rate configuration 0000 = No errors 0001 = Invalid sample rate 0010 = Invalid AIF divide 0011 = ADC and DAC divides both set in an interface 0100 = Invalid combination of AIF divides and sample-rate 0101 = Invalid set of enables for 96kHz mode 0110 = Invalid SYSCLK rate (derived from AIF1CLK_RATE or AIF2CLK_RATE) 0111 = Mixed ADC and DAC rates in SYSCLK AIF when AIFs are asynchronous 1000 = Invalid combination of sample rates when both AIFs are from the same clock source 1001 = Invalid combination of mixed ADC/DAC AIFs when both from the same clock source 1010 = AIF1DAC2 (Timeslot 1) ports enabled when SRCs connected to AIF1	

Register 0212h Rate Status

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R544 (0220h) FLL1 Control (1)	2	FLL1_FRACN_ENA	0	FLL1 Fractional enable 0 = Integer Mode 1 = Fractional Mode Fractional Mode (FLL1_FRACN_ENA=1 is recommended in all cases)	
	1	FLL1_OSC_ENA	0	FLL1 Oscillator enable 0 = Disabled 1 = Enabled (Note that this field is required for free-running FLL1 modes only)	
	0	FLL1_ENA	0	FLL1 Enable 0 = Disabled 1 = Enabled	

Register 0220h FLL1 Control (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R545 (0221h) FLL1 Control (2)	13:8	FLL1_OUTDIV[5:0]	00_0000	FLL1 FOUT clock divider 000000 = Reserved 000001 = Reserved 000010 = Reserved 000011 = 4 000100 = 5 000101 = 6 … 111110 = 63 111111 = 64 (FOUT = FVCO / FLL1_OUTDIV)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	6:4	FLL1_CTRL_RATE[2:0]	000	Frequency of the FLL1 control block 000 = FVCO / 1 (Recommended value) 001 = FVCO / 2 010 = FVCO / 3 011 = FVCO / 4 100 = FVCO / 5 101 = FVCO / 6 110 = FVCO / 7 111 = FVCO / 8 Recommended that these are not changed from default.	
	2:0	FLL1_FRATIO[2:0]	000	FLL1 FVCO clock divider 000 = 1 001 = 2 010 = 4 011 = 8 1XX = 16 000 recommended for high FREF 011 recommended for low FREF	

Register 0221h FLL1 Control (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R546 (0222h) FLL1 Control (3)	15:0	FLL1_K[15:0]	0000_0000_0000_0000	FLL1 Fractional multiply for FREF (MSB = 0.5)	

Register 0222h FLL1 Control (3)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R547 (0223h) FLL1 Control (4)	14:5	FLL1_N[9:0]	00_0000_0000	FLL1 Integer multiply for FREF (LSB = 1)	
	3:0	FLL1_GAIN[3:0]	0000	FLL1 Gain applied to error 0000 = x 1 (Recommended value) 0001 = x 2 0010 = x 4 0011 = x 8 0100 = x 16 0101 = x 32 0110 = x 64 0111 = x 128 1000 = x 256 Recommended that these are not changed from default.	

Register 0223h FLL1 Control (4)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R548 (0224h) FLL1 Control (5)	12:7	FLL1_FRC_NCO_VAL[5:0]	01_1001	FLL1 Forced oscillator value Valid range is 000000 to 111111 0x19h (011001) = 12MHz approx (Note that this field is required for free-running FLL modes only)	
	6	FLL1_FRC_NCO	0	FLL1 Forced control select 0 = Normal 1 = FLL1 oscillator controlled by FLL1_FRC_NCO_VAL (Note that this field is required for free-running FLL modes only)	
	4:3	FLL1_CLK_REF_DIV[1:0]	00	FLL1 Clock Reference Divider 00 = MCLK / 1 01 = MCLK / 2 10 = MCLK / 4 11 = MCLK / 8 MCLK (or other input reference) must be divided down to <=13.5MHz. For lower power operation, the reference clock can be divided down further if desired.	
	1:0	FLL1_CLK_REF_SRC[1:0]	00	FLL1 Clock source 00 = MCLK1 01 = MCLK2 10 = LRCLK1 11 = BCLK1	

Register 0224h FLL1 Control (5)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R576 (0240h) FLL2 Control (1)	2	FLL2_FRACN_ENA	0	FLL2 Fractional enable 0 = Integer Mode 1 = Fractional Mode Fractional Mode (FLL2_FRACN_ENA=1 is recommended in all cases)	
	1	FLL2_OSC_ENA	0	FLL2 Oscillator enable 0 = Disabled 1 = Enabled (Note that this field is required for free-running FLL2 modes only)	
	0	FLL2_ENA	0	FLL2 Enable 0 = Disabled 1 = Enabled	

Register 0240h FLL2 Control (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R577 (0241h) FLL2 Control (2)	13:8	FLL2_OUTDIV[5:0]	00_0000	FLL2 FOUT clock divider 000000 = Reserved 000001 = Reserved 000010 = Reserved 000011 = 4 000100 = 5 000101 = 6 … 111110 = 63 111111 = 64 (FOUT = FVCO / FLL2_OUTDIV)	
	6:4	FLL2_CTRL_RATE[2:0]	000	Frequency of the FLL2 control block 000 = FVCO / 1 (Recommended value) 001 = FVCO / 2 010 = FVCO / 3 011 = FVCO / 4 100 = FVCO / 5 101 = FVCO / 6 110 = FVCO / 7 111 = FVCO / 8 Recommended that these are not changed from default.	
	2:0	FLL2_FRATIO[2:0]	000	FLL2 FVCO clock divider 000 = 1 001 = 2 010 = 4 011 = 8 1XX = 16 000 recommended for high FREF 011 recommended for low FREF	

Register 0241h FLL2 Control (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R578 (0242h) FLL2 Control (3)	15:0	FLL2_K[15:0]	0000_0000_0000_0000	FLL2 Fractional multiply for FREF (MSB = 0.5)	

Register 0242h FLL2 Control (3)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R579 (0243h) FLL2 Control (4)	14:5	FLL2_N[9:0]	00_0000_0000	FLL2 Integer multiply for FREF (LSB = 1)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	3:0	FLL2_GAIN[3:0]	0000	FLL2 Gain applied to error 0000 = x 1 (Recommended value) 0001 = x 2 0010 = x 4 0011 = x 8 0100 = x 16 0101 = x 32 0110 = x 64 0111 = x 128 1000 = x 256 Recommended that these are not changed from default.	

Register 0243h FLL2 Control (4)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R580 (0244h) FLL2 Control (5)	12:7	FLL2_FRC_NCO_VAL[5:0]	01_1001	FLL2 Forced oscillator value Valid range is 000000 to 111111 0x19h (011001) = 12MHz approx (Note that this field is required for free-running FLL modes only)	
	6	FLL2_FRC_NCO	0	FLL2 Forced control select 0 = Normal 1 = FLL2 oscillator controlled by FLL2_FRC_NCO_VAL (Note that this field is required for free-running FLL modes only)	
	4:3	FLL2_CLK_REF_DIV[1:0]	00	FLL2 Clock Reference Divider 00 = MCLK / 1 01 = MCLK / 2 10 = MCLK / 4 11 = MCLK / 8 MCLK (or other input reference) must be divided down to <=13.5MHz. For lower power operation, the reference clock can be divided down further if desired.	
	1:0	FLL2_CLK_REF_SRC[1:0]	00	FLL2 Clock source 00 = MCLK1 01 = MCLK2 10 = LRCLK2 11 = BCLK2	

Register 0244h FLL2 Control (5)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R768 (0300h) AIF1 Control (1)	15	AIF1ADCL_SRC	0	AIF1 Left Digital Audio interface source 0 = Left ADC data is output on left channel 1 = Right ADC data is output on left channel	
	14	AIF1ADCR_SRC	1	AIF1 Right Digital Audio interface source 0 = Left ADC data is output on right channel 1 = Right ADC data is output on right channel	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	13	AIF1ADC_TDM	0	AIF1 transmit (ADC) TDM Enable 0 = Normal ADCDAT1 operation 1 = TDM enabled on ADCDAT1	
	8	AIF1_BCLK_INV	0	BCLK1 Invert 0 = BCLK1 not inverted 1 = BCLK1 inverted	
	7	AIF1_LRCLK_INV	0	Right, left and I2S modes – LRCLK1 polarity 0 = normal LRCLK1 polarity 1 = invert LRCLK1 polarity DSP Mode – mode A/B select 0 = MSB is available on 2nd BCLK1 rising edge after LRCLK1 rising edge (mode A) 1 = MSB is available on 1st BCLK1 rising edge after LRCLK1 rising edge (mode B)	
	6:5	AIF1_WL[1:0]	10	AIF1 Digital Audio Interface Word Length 00 = 16 bits 01 = 20 bits 10 = 24 bits 11 = 32 bits Note - 8-bit modes can be selected using the "Companding" control bits.	
	4:3	AIF1_FMT[1:0]	10	AIF1 Digital Audio Interface Format 00 = Right justified 01 = Left justified 10 = I2S Format 11 = DSP Mode	

Register 0300h AIF1 Control (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R769 (0301h) AIF1 Control (2)	15	AIF1DACL_SRC	0	AIF1 Left Receive Data Source Select 0 = Left DAC receives left interface data 1 = Left DAC receives right interface data	
	14	AIF1DACR_SRC	1	AIF1 Right Receive Data Source Select 0 = Right DAC receives left interface data 1 = Right DAC receives right interface data	
	11:10	AIF1DAC_BOOST[1:0]	00	AIF1 Input Path Boost 00 = 0dB 01 = +6dB 10 = +12dB 11 = +18dB	
	4	AIF1DAC_COMP	0	AIF1 Receive Companding Enable 0 = disabled 1 = enabled	
	3	AIF1DAC_COMPMODE	0	AIF1 Receive Companding Type 0 = μ-law 1 = A-law	
	2	AIF1ADC_COMP	0	AIF1 Transmit Companding Enable 0 = disabled 1 = enabled	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	1	AIF1ADC_COMPMODE	0	AIF1 Transmit Companding Type 0 = µ-law 1 = A-law	
	0	AIF1_LOOPBACK	0	AIF1 Digital Loopback Function 0 = No loopback 1 = Loopback enabled (ADCDAT1 data output is directly input to DACDAT1 data input).	

Register 0301h AIF1 Control (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R770 (0302h) AIF1 Master/Slave	15	AIF1_TRI	0	AIF1 Audio Interface tri-state 0 = AIF1 pins operate normally 1 = Tri-state all AIF1 interface pins Note that the GPIO1 pin is controlled by this register only when configured as ADCLRCLK1.	
	14	AIF1_MSTR	0	AIF1 Audio Interface Master Mode Select 0 = Slave mode 1 = Master mode	
	13	AIF1_CLK_FRC	0	Forces BCLK1 to be enabled when all AIF1 audio channels are disabled. 0 = Normal 1 = BCLK1 always enabled in Master mode	
	12	AIF1_LRCLK_FRC	0	Forces LRCLK1 to be enabled when all AIF1 audio channels are disabled. 0 = Normal 1 = LRCLK1 always enabled in Master mode	

Register 0302h AIF1 Master/Slave

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R771 (0303h) AIF1 BCLK	7:4	AIF1_BCLK_DIV[3:0]	0100	BCLK1 Rate 0000 = AIF1CLK 0001 = AIF1CLK / 2 0010 = AIF1CLK / 4 0011 = AIF1CLK / 6 0100 = AIF1CLK / 8 0101 = AIF1CLK / 12 0110 = AIF1CLK / 16 0111 = AIF1CLK / 24 1000 = AIF1CLK / 32 1001 = AIF1CLK / 48 All other codes are Reserved	

Register 0303h AIF1 BCLK

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R772 (0304h) AIF1ADC LRCLK	11	AIF1ADC_LRCLK_DIR	0	Allows ADCLRCLK1 to be enabled in Slave mode 0 = Normal 1 = ADCLRCLK1 enabled in Slave mode	
	10:0	AIF1ADC_RATE[10:0]	000_0100_0000	ADCLRCLK1 Rate ADCLRCLK1 clock output = BCLK1 / AIF1ADC_RATE Integer (LSB = 1) Valid from 8..2047	

Register 0304h AIF1ADC LRCLK

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R773 (0305h) AIF1DAC LRCLK	11	AIF1DAC_LRCLK_DIR	0	Allows LRCLK1 to be enabled in Slave mode 0 = Normal 1 = LRCLK1 enabled in Slave mode	
	10:0	AIF1DAC_RATE[10:0]	000_0100_0000	LRCLK1 Rate LRCLK1 clock output = BCLK1 / AIF1DAC_RATE Integer (LSB = 1) Valid from 8..2047	

Register 0305h AIF1DAC LRCLK

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R774 (0306h) AIF1DAC Data	1	AIF1DACL_DAT_INV	0	AIF1 Left Receive Data Invert 0 = Not inverted 1 = Inverted	
	0	AIF1DACR_DAT_INV	0	AIF1 Right Receive Data Invert 0 = Not inverted 1 = Inverted	

Register 0306h AIF1DAC Data

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R775 (0307h) AIF1ADC Data	1	AIF1ADCL_DAT_INV	0	AIF1 Left Transmit Data Invert 0 = Not inverted 1 = Inverted	
	0	AIF1ADCR_DAT_INV	0	AIF1 Right Transmit Data Invert 0 = Not inverted 1 = Inverted	

Register 0307h AIF1ADC Data

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R784 (0310h) AIF2 Control (1)	15	AIF2ADCL_SRC	0	AIF2 Left Digital Audio interface source 0 = Left ADC data is output on left channel 1 = Right ADC data is output on left channel	
	14	AIF2ADCR_SRC	1	AIF2 Right Digital Audio interface source 0 = Left ADC data is output on right channel 1 = Right ADC data is output on right channel	
	13	AIF2ADC_TDM	0	AIF2 transmit (ADC) TDM Enable 0 = Normal ADCDAT2 operation 1 = TDM enabled on ADCDAT2	
	12	AIF2ADC_TDM_CHAN	0	AIF2 transmit (ADC) TDM Slot Select 0 = Slot 0 1 = Slot 1	
	8	AIF2_BCLK_INV	0	BCLK2 Invert 0 = BCLK2 not inverted 1 = BCLK2 inverted	
	7	AIF2_LRCLK_INV	0	Right, left and I2S modes – LRCLK2 polarity 0 = normal LRCLK2 polarity 1 = invert LRCLK2 polarity DSP Mode – mode A/B select 0 = MSB is available on 2nd BCLK2 rising edge after LRCLK2 rising edge (mode A) 1 = MSB is available on 1st BCLK2 rising edge after LRCLK2 rising edge (mode B)	
	6:5	AIF2_WL[1:0]	10	AIF2 Digital Audio Interface Word Length 00 = 16 bits 01 = 20 bits 10 = 24 bits 11 = 32 bits Note - 8-bit modes can be selected using the "Companding" control bits.	
	4:3	AIF2_FMT[1:0]	10	AIF2 Digital Audio Interface Format 00 = Right justified 01 = Left justified 10 = I2S Format 11 = DSP Mode	

Register 0310h AIF2 Control (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R785 (0311h) AIF2 Control (2)	15	AIF2DACL_SRC	0	AIF2 Left Receive Data Source Select 0 = Left DAC receives left interface data 1 = Left DAC receives right interface data	
	14	AIF2DACR_SRC	1	AIF2 Right Receive Data Source Select 0 = Right DAC receives left interface data 1 = Right DAC receives right interface data	
	13	AIF2DAC_TDM	0	AIF2 receive (DAC) TDM Enable 0 = Normal DACDAT2 operation 1 = TDM enabled on DACDAT2	
	12	AIF2DAC_TDM_CHAN	0	AIF2 receive(DAC) TDM Slot Select 0 = Slot 0 1 = Slot 1	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	11:10	AIF2DAC_BOOST[1:0]	00	AIF2 Input Path Boost 00 = 0dB 01 = +6dB 10 = +12dB 11 = +18dB	
	4	AIF2DAC_COMP	0	AIF2 Receive Companding Enable 0 = disabled 1 = enabled	
	3	AIF2DAC_COMPMODE	0	AIF2 Receive Companding Type 0 = µ-law 1 = A-law	
	2	AIF2ADC_COMP	0	AIF2 Transmit Companding Enable 0 = disabled 1 = enabled	
	1	AIF2ADC_COMPMODE	0	AIF2 Transmit Companding Type 0 = µ-law 1 = A-law	
	0	AIF2_LOOPBACK	0	AIF2 Digital Loopback Function 0 = No loopback 1 = Loopback enabled (ADCDAT2 data output is directly input to DACDAT2 data input).	

Register 0311h AIF2 Control (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R786 (0312h) AIF2 Master/Slave	15	AIF2_TRI	0	AIF2 Audio Interface tri-state 0 = AIF2 pins operate normally 1 = Tri-state all AIF2 interface pins Note that pins not configured as AIF2 functions are not affected by this register.	
	14	AIF2_MSTR	0	AIF2 Audio Interface Master Mode Select 0 = Slave mode 1 = Master mode	
	13	AIF2_CLK_FRC	0	Forces BCLK2 to be enabled when all AIF2 audio channels are disabled. 0 = Normal 1 = BCLK2 always enabled in Master mode	
	12	AIF2_LRCLK_FRC	0	Forces LRCLK2 to be enabled when all AIF2 audio channels are disabled. 0 = Normal 1 = LRCLK2 always enabled in Master mode	

Register 0312h AIF2 Master/Slave

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R787 (0313h) AIF2 BCLK	7:4	AIF2_BCLK_DIV[3:0]	0100	BCLK2 Rate 0000 = AIF2CLK 0001 = AIF2CLK / 2 0010 = AIF2CLK / 4 0011 = AIF2CLK / 6 0100 = AIF2CLK / 8 0101 = AIF2CLK / 12 0110 = AIF2CLK / 16 0111 = AIF2CLK / 24 1000 = AIF2CLK / 32 1001 = AIF2CLK / 48 All other codes are Reserved	

Register 0313h AIF2 BCLK

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R788 (0314h) AIF2ADC LRCLK	11	AIF2ADC_LRCLK_DIR	0	Allows ADCLRCLK2 to be enabled in Slave mode 0 = Normal 1 = ADCLRCLK2 enabled in Slave mode	
	10:0	AIF2ADC_RATE[10:0]	000_0100_0000	ADCLRCLK2 Rate ADCLRCLK2 clock output = BCLK2 / AIF2ADC_RATE Integer (LSB = 1) Valid from 8..2047	

Register 0314h AIF2ADC LRCLK

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R789 (0315h) AIF2DAC LRCLK	11	AIF2DAC_LRCLK_DIR	0	Allows LRCLK2 to be enabled in Slave mode 0 = Normal 1 = LRCLK2 enabled in Slave mode	
	10:0	AIF2DAC_RATE[10:0]	000_0100_0000	LRCLK2 Rate LRCLK2 clock output = BCLK2 / AIF2DAC_RATE Integer (LSB = 1) Valid from 8..2047	

Register 0315h AIF2DAC LRCLK

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R790 (0316h) AIF2DAC Data	1	AIF2DACL_DAT_INV	0	AIF2 Left Receive Data Invert 0 = Not inverted 1 = Inverted	
	0	AIF2DACR_DAT_INV	0	AIF2 Right Receive Data Invert 0 = Not inverted 1 = Inverted	

Register 0316h AIF2DAC Data

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R791 (0317h) AIF2ADC Data	1	AIF2ADCL_DAT_INV	0	AIF2 Left Transmit Data Invert 0 = Not inverted 1 = Inverted	
	0	AIF2ADCR_DAT_INV	0	AIF2 Right Transmit Data Invert 0 = Not inverted 1 = Inverted	

Register 0317h AIF2ADC Data

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1024 (0400h) AIF1 ADC1 Left Volume	8	AIF1ADC1_VU	0	AIF1ADC1 output path (AIF1, Timeslot 0) Volume Update Writing a 1 to this bit will cause the AIF1ADC1L and AIF1ADC1R volume to be updated simultaneously	
	7:0	AIF1ADC1L_VOL[7:0]	1100_0000	AIF1ADC1 (Left) output path (AIF1, Timeslot 0) Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) EFh = +17.625dB	

Register 0400h AIF1 ADC1 Left Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1025 (0401h) AIF1 ADC1 Right Volume	8	AIF1ADC1_VU	0	AIF1ADC1 output path (AIF1, Timeslot 0) Volume Update Writing a 1 to this bit will cause the AIF1ADC1L and AIF1ADC1R volume to be updated simultaneously	
	7:0	AIF1ADC1R_VOL[7:0]	1100_0000	AIF1ADC1 (Right) output path (AIF1, Timeslot 0) Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) EFh = +17.625dB	

Register 0401h AIF1 ADC1 Right Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1026 (0402h) AIF1 DAC1 Left Volume	8	AIF1DAC1_VU	0	AIF1DAC1 input path (AIF1, Timeslot 0) Volume Update Writing a 1 to this bit will cause the AIF1DAC1L and AIF1DAC1R volume to be updated simultaneously	
	7:0	AIF1DAC1L_VOL[7:0]	1100_0000	AIF1DAC1 (Left) input path (AIF1, Timeslot 0) Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB	

Register 0402h AIF1 DAC1 Left Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1027 (0403h) AIF1 DAC1 Right Volume	8	AIF1DAC1_VU	0	AIF1DAC1 input path (AIF1, Timeslot 0) Volume Update Writing a 1 to this bit will cause the AIF1DAC1L and AIF1DAC1R volume to be updated simultaneously	
	7:0	AIF1DAC1R_VOL[7:0]	1100_0000	AIF1DAC1 (Right) input path (AIF1, Timeslot 0) Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB	

Register 0403h AIF1 DAC1 Right Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1028 (0404h) AIF1 ADC2 Left Volume	8	AIF1ADC2_VU	0	AIF1ADC2 output path (AIF1, Timeslot 1) Volume Update Writing a 1 to this bit will cause the AIF1ADC2L and AIF1ADC2R volume to be updated simultaneously	
	7:0	AIF1ADC2L_VOL[7:0]	1100_0000	AIF1ADC2 (Left) output path (AIF1, Timeslot 1) Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) EFh = +17.625dB	

Register 0404h AIF1 ADC2 Left Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1029 (0405h) AIF1 ADC2 Right Volume	8	AIF1ADC2_VU	0	AIF1ADC2 output path (AIF1, Timeslot 1) Volume Update Writing a 1 to this bit will cause the AIF1ADC2L and AIF1ADC2R volume to be updated simultaneously	
	7:0	AIF1ADC2R_VOL[7:0]	1100_0000	AIF1ADC2 (Right) output path (AIF1, Timeslot 1) Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) EFh = +17.625dB	

Register 0405h AIF1 ADC2 Right Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1030 (0406h) AIF1 DAC2 Left Volume	8	AIF1DAC2_VU	0	AIF1DAC2 input path (AIF1, Timeslot 1) Volume Update Writing a 1 to this bit will cause the AIF1DAC2L and AIF1DAC2R volume to be updated simultaneously	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	7:0	AIF1DAC2L_VOL[7:0]	1100_0000	AIF1DAC2 (Left) input path (AIF1, Timeslot 1) Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB	

Register 0406h AIF1 DAC2 Left Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1031 (0407h) AIF1 DAC2 Right Volume	8	AIF1DAC2_VU	0	AIF1DAC2 input path (AIF1, Timeslot 1) Volume Update Writing a 1 to this bit will cause the AIF1DAC2L and AIF1DAC2R volume to be updated simultaneously	
	7:0	AIF1DAC2R_VOL[7:0]	1100_0000	AIF1DAC2 (Right) input path (AIF1, Timeslot 1) Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB	

Register 0407h AIF1 DAC2 Right Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1040 (0410h) AIF1 ADC1 Filters	14:13	AIF1ADC1_HPF_CUT[1:0]	00	AIF1ADC1 output path (AIF1, Timeslot 0) Digital HPF cut-off frequency (fc) 00 = Hi-fi mode (fc = 4Hz at fs = 48kHz) 01 = Voice mode 1 (fc = 127Hz at fs = 8kHz) 10 = Voice mode 2 (fc = 130Hz at fs = 8kHz) 11 = Voice mode 3 (fc = 267Hz at fs = 8kHz)	
	12	AIF1ADC1L_HPF	0	AIF1ADC1 (Left) output path (AIF1, Timeslot 0) Digital HPF Enable 0 = Disabled 1 = Enabled	
	11	AIF1ADC1R_HPF	0	AIF1ADC1 (Right) output path (AIF1, Timeslot 0) Digital HPF Enable 0 = Disabled 1 = Enabled	

Register 0410h AIF1 ADC1 Filters

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1041 (0411h) AIF1 ADC2 Filters	14:13	AIF1ADC2_HPF_CUT[1:0]	00	AIF1ADC2 output path (AIF1, Timeslot 1) Digital HPF cut-off frequency (fc) 00 = Hi-fi mode (fc = 4Hz at fs = 48kHz) 01 = Voice mode 1 (fc = 127Hz at fs = 8kHz) 10 = Voice mode 2 (fc = 130Hz at fs = 8kHz) 11 = Voice mode 3 (fc = 267Hz at fs = 8kHz)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	12	AIF1ADC2L_HPF	0	AIF1ADC2 (Left) output path (AIF1, Timeslot 1) Digital HPF Enable 0 = Disabled 1 = Enabled	
	11	AIF1ADC2R_HPF	0	AIF1ADC2 (Right) output path (AIF1, Timeslot 1) Digital HPF Enable 0 = Disabled 1 = Enabled	

Register 0411h AIF1 ADC2 Filters

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1056 (0420h) AIF1 DAC1 Filters (1)	9	AIF1DAC1_MUTE	1	AIF1DAC1 input path (AIF1, Timeslot 0) Soft Mute Control 0 = Un-mute 1 = Mute	
	7	AIF1DAC1_MONO	0	AIF1DAC1 input path (AIF1, Timeslot 0) Mono Mix Control 0 = Disabled 1 = Enabled	
	5	AIF1DAC1_MUTERATE	0	AIF1DAC1 input path (AIF1, Timeslot 0) Soft Mute Ramp Rate 0 = Fast ramp (fs/2, maximum ramp time is 10.7ms at fs=48k) 1 = Slow ramp (fs/32, maximum ramp time is 171ms at fs=48k) (Note: ramp rate scales with sample rate.)	
	4	AIF1DAC1_UNMUTE_RAMP	0	AIF1DAC1 input path (AIF1, Timeslot 0) Unmute Ramp select 0 = Disabling soft-mute (AIF1DAC1_MUTE=0) will cause the volume to change immediately to AIF1DAC1L_VOL and AIF1DAC1R_VOL settings 1 = Disabling soft-mute (AIF1DAC1_MUTE=0) will cause the DAC volume to ramp up gradually to the AIF1DAC1L_VOL and AIF1DAC1R_VOL settings	
	2:1	AIF1DAC1_DEEMP[1:0]	00	AIF1DAC1 input path (AIF1, Timeslot 0) De-Emphasis Control 00 = No de-emphasis 01 = 32kHz sample rate 10 = 44.1kHz sample rate 11 = 48kHz sample rate	

Register 0420h AIF1 DAC1 Filters (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1057 (0421h) AIF1 DAC1 Filters (2)	13:9	AIF1DAC1_3D_GAIN[4:0]	0_0000	AIF1DAC1 playback path (AIF1, Timeslot 0) 3D Stereo depth 00000 = Off 00001 = Minimum (-16dB) …(0.915dB steps) 11111 = Maximum (+11.5dB)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	8	AIF1DAC1_3D_ENA	0	Enable 3D Stereo in AIF1DAC1 playback path (AIF1, Timeslot 0) 0 = Disabled 1 = Enabled	

Register 0421h AIF1 DAC1 Filters (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1058 (0422h) AIF1 DAC2 Filters (1)	9	AIF1DAC2_MUTE	1	AIF1DAC2 input path (AIF1, Timeslot 1) Soft Mute Control 0 = Un-mute 1 = Mute	
	7	AIF1DAC2_MONO	0	AIF1DAC2 input path (AIF1, Timeslot 1) Mono Mix Control 0 = Disabled 1 = Enabled	
	5	AIF1DAC2_MUTERATE	0	AIF1DAC2 input path (AIF1, Timeslot 1) Soft Mute Ramp Rate 0 = Fast ramp (fs/2, maximum ramp time is 10.7ms at fs=48k) 1 = Slow ramp (fs/32, maximum ramp time is 171ms at fs=48k) (Note: ramp rate scales with sample rate.)	
	4	AIF1DAC2_UNMUTE_RAMP	0	AIF1DAC2 input path (AIF1, Timeslot 1) Unmute Ramp select 0 = Disabling soft-mute (AIF1DAC2_MUTE=0) will cause the volume to change immediately to AIF1DAC2L_VOL and AIF1DAC2R_VOL settings 1 = Disabling soft-mute (AIF1DAC2_MUTE=0) will cause the DAC volume to ramp up gradually to the AIF1DAC2L_VOL and AIF1DAC2R_VOL settings	
	2:1	AIF1DAC2_DEEMP[1:0]	00	AIF1DAC2 input path (AIF1, Timeslot 1) De-Emphasis Control 00 = No de-emphasis 01 = 32kHz sample rate 10 = 44.1kHz sample rate 11 = 48kHz sample rate	

Register 0422h AIF1 DAC2 Filters (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1059 (0423h) AIF1 DAC2 Filters (2)	13:9	AIF1DAC2_3D_GAIN[4:0]	0_0000	AIF1DAC2 playback path (AIF1, Timeslot 1) 3D Stereo depth 00000 = Off 00001 = Minimum (-16dB) …(0.915dB steps) 11111 = Maximum (+11.5dB)	
	8	AIF1DAC2_3D_ENA	0	Enable 3D Stereo in AIF1DAC2 playback path (AIF1, Timeslot 1) 0 = Disabled 1 = Enabled	

Register 0423h AIF1 DAC2 Filters (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1088 (0440h) AIF1 DRC1 (1)	15:11	AIF1DRC1_SIG_DET_RMS[4:0]	0_0000	AIF1 DRC1 Signal Detect RMS Threshold. This is the RMS signal level for signal detect to be indicated when AIF1DRC1_SIG_DET_MODE=0. 00000 = -30dB 00001 = -31.5dB …. (1.5dB steps) 11110 = -75dB 11111 = -76.5dB	
	10:9	AIF1DRC1_SIG_DET_PK[1:0]	00	AIF1 DRC1 Signal Detect Peak Threshold. This is the Peak/RMS ratio, or Crest Factor, level for signal detect to be indicated when AIF1DRC1_SIG_DET_MODE=1. 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB	
	8	AIF1DRC1_NG_ENA	0	AIF1 DRC1 Noise Gate Enable 0 = Disabled 1 = Enabled	
	7	AIF1DRC1_SIG_DET_MODE	1	AIF1 DRC1 Signal Detect Mode 0 = RMS threshold mode 1 = Peak threshold mode	
	6	AIF1DRC1_SIG_DET	0	AIF1 DRC1 Signal Detect Enable 0 = Disabled 1 = Enabled	
	5	AIF1DRC1_KNEE2_OP_ENA	0	AIF1 DRC1 KNEE2_OP Enable 0 = Disabled 1 = Enabled	
	4	AIF1DRC1_QR	1	AIF1 DRC1 Quick-release Enable 0 = Disabled 1 = Enabled	
	3	AIF1DRC1_ANTICLIP	1	AIF1 DRC1 Anti-clip Enable 0 = Disabled 1 = Enabled	
	2	AIF1DAC1_DRC_ENA	0	Enable DRC in AIF1DAC1 playback path (AIF1, Timeslot 0) 0 = Disabled 1 = Enabled	
	1	AIF1ADC1L_DRC_ENA	0	Enable DRC in AIF1ADC1 (Left) record path (AIF1, Timeslot 0) 0 = Disabled 1 = Enabled	
	0	AIF1ADC1R_DRC_ENA	0	Enable DRC in AIF1ADC1 (Right) record path (AIF1, Timeslot 0) 0 = Disabled 1 = Enabled	

Register 0440h AIF1 DRC1 (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1089 (0441h) AIF1 DRC1 (2)	12:9	AIF1DRC1_ATK[3:0]	0100	AIF1 DRC1 Gain attack rate (seconds/6dB) 0000 = Reserved 0001 = 181us 0010 = 363us 0011 = 726us 0100 = 1.45ms 0101 = 2.9ms 0110 = 5.8ms 0111 = 11.6ms 1000 = 23.2ms 1001 = 46.4ms 1010 = 92.8ms 1011 = 185.6ms 1100-1111 = Reserved	
	8:5	AIF1DRC1_DCY[3:0]	0010	AIF1 DRC1 Gain decay rate (seconds/6dB) 0000 = 186ms 0001 = 372ms 0010 = 743ms 0011 = 1.49s 0100 = 2.97s 0101 = 5.94s 0110 = 11.89s 0111 = 23.78s 1000 = 47.56s 1001-1111 = Reserved	
	4:2	AIF1DRC1_MINGAIN[2:0]	001	AIF1 DRC1 Minimum gain to attenuate audio signals 000 = 0dB 001 = -12dB (default) 010 = -18dB 011 = -24dB 100 = -36dB 101 = Reserved 11X = Reserved	
	1:0	AIF1DRC1_MAXGAIN[1:0]	01	AIF1 DRC1 Maximum gain to boost audio signals (dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 36dB	

Register 0441h AIF1 DRC1 (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1090 (0442h) AIF1 DRC1 (3)	15:12	AIF1DRC1_NG_MINGAIN[3:0]	0000	AIF1 DRC1 Minimum gain to attenuate audio signals when the noise gate is active. 0000 = -36dB 0001 = -30dB 0010 = -24dB 0011 = -18dB 0100 = -12dB 0101 = -6dB 0110 = 0dB 0111 = 6dB 1000 = 12dB 1001 = 18dB 1010 = 24dB 1011 = 30dB 1100 = 36dB 1101 to 1111 = Reserved	
	11:10	AIF1DRC1_NG_EXP[1:0]	00	AIF1 DRC1 Noise Gate slope 00 = 1 (no expansion) 01 = 2 10 = 4 11 = 8	
	9:8	AIF1DRC1_QR_THR[1:0]	00	AIF1 DRC1 Quick-release threshold (crest factor in dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB	
	7:6	AIF1DRC1_QR_DCY[1:0]	00	AIF1 DRC1 Quick-release decay rate (seconds/6dB) 00 = 0.725ms 01 = 1.45ms 10 = 5.8ms 11 = reserved	
	5:3	AIF1DRC1_HI_COMP[2:0]	000	AIF1 DRC1 Compressor slope (upper region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 0 110 = Reserved 111 = Reserved	
	2:0	AIF1DRC1_LO_COMP[2:0]	000	AIF1 DRC1 Compressor slope (lower region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 0 101 = Reserved 11X = Reserved	

Register 0442h AIF1 DRC1 (3)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1091 (0443h) AIF1 DRC1 (4)	10:5	AIF1DRC1_KNEE_IP[5:0]	00_0000	AIF1 DRC1 Input signal level at the Compressor 'Knee'. 000000 = 0dB 000001 = -0.75dB 000010 = -1.5dB … (-0.75dB steps) 111100 = -45dB 111101 = Reserved 11111X = Reserved	
	4:0	AIF1DRC1_KNEE_OP[4:0]	0_0000	AIF1 DRC1 Output signal at the Compressor 'Knee'. 00000 = 0dB 00001 = -0.75dB 00010 = -1.5dB … (-0.75dB steps) 11110 = -22.5dB 11111 = Reserved	

Register 0443h AIF1 DRC1 (4)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1092 (0444h) AIF1 DRC1 (5)	9:5	AIF1DRC1_KNEE2_IP[4:0]	0_0000	AIF1 DRC1 Input signal level at the Noise Gate threshold 'Knee2'. 00000 = -36dB 00001 = -37.5dB 00010 = -39dB … (-1.5dB steps) 11110 = -81dB 11111 = -82.5dB Only applicable when DRC_NG_ENA = 1.	
	4:0	AIF1DRC1_KNEE2_OP[4:0]	0_0000	AIF1 DRC1 Output signal at the Noise Gate threshold 'Knee2'. 00000 = -30dB 00001 = -31.5dB 00010 = -33dB … (-1.5dB steps) 11110 = -75dB 11111 = -76.5dB Only applicable when DRC_KNEE2_OP_ENA = 1.	

Register 0444h AIF1 DRC1 (5)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1104 (0450h) AIF1 DRC2 (1)	15:11	AIF1DRC2_SIG_DET_RMS[4:0]	0_0000	AIF1 DRC2 Signal Detect RMS Threshold. This is the RMS signal level for signal detect to be indicated when AIF1DRC2_SIG_DET_MODE=0. 00000 = -30dB 00001 = -31.5dB …. (1.5dB steps) 11110 = -75dB 11111 = -76.5dB	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	10:9	AIF1DRC2_SIG_DET_PK[1:0]	00	AIF1 DRC2 Signal Detect Peak Threshold. This is the Peak/RMS ratio, or Crest Factor, level for signal detect to be indicated when AIF1DRC2_SIG_DET_MODE=1. 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB	
	8	AIF1DRC2_NG_ENA	0	AIF1 DRC2 Noise Gate Enable 0 = Disabled 1 = Enabled	
	7	AIF1DRC2_SIG_DET_MODE	1	AIF1 DRC2 Signal Detect Mode 0 = RMS threshold mode 1 = Peak threshold mode	
	6	AIF1DRC2_SIG_DET	0	AIF1 DRC2 Signal Detect Enable 0 = Disabled 1 = Enabled	
	5	AIF1DRC2_KNEE2_OP_ENA	0	AIF1 DRC2 KNEE2_OP Enable 0 = Disabled 1 = Enabled	
	4	AIF1DRC2_QR	1	AIF1 DRC2 Quick-release Enable 0 = Disabled 1 = Enabled	
	3	AIF1DRC2_ANTICLIP	1	AIF1 DRC2 Anti-clip Enable 0 = Disabled 1 = Enabled	
	2	AIF1DAC2_DRC_ENA	0	Enable DRC in AIF1DAC2 playback path (AIF1, Timeslot 1) 0 = Disabled 1 = Enabled	
	1	AIF1ADC2L_DRC_ENA	0	Enable DRC in AIF1ADC2 (Left) record path (AIF1, Timeslot 1) 0 = Disabled 1 = Enabled	
	0	AIF1ADC2R_DRC_ENA	0	Enable DRC in AIF1ADC2 (Right) record path (AIF1, Timeslot 1) 0 = Disabled 1 = Enabled	

Register 0450h AIF1 DRC2 (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1105 (0451h) AIF1 DRC2 (2)	12:9	AIF1DRC2_ATK[3:0]	0100	AIF1 DRC2 Gain attack rate (seconds/6dB) 0000 = Reserved 0001 = 181us 0010 = 363us 0011 = 726us 0100 = 1.45ms 0101 = 2.9ms 0110 = 5.8ms 0111 = 11.6ms 1000 = 23.2ms 1001 = 46.4ms 1010 = 92.8ms 1011 = 185.6ms 1100-1111 = Reserved	
	8:5	AIF1DRC2_DCY[3:0]	0010	AIF1 DRC2 Gain decay rate (seconds/6dB) 0000 = 186ms 0001 = 372ms 0010 = 743ms 0011 = 1.49s 0100 = 2.97s 0101 = 5.94s 0110 = 11.89s 0111 = 23.78s 1000 = 47.56s 1001-1111 = Reserved	
	4:2	AIF1DRC2_MINGAIN[2:0]	001	AIF1 DRC2 Minimum gain to attenuate audio signals 000 = 0dB 001 = -12dB (default) 010 = -18dB 011 = -24dB 100 = -36dB 101 = Reserved 11X = Reserved	
	1:0	AIF1DRC2_MAXGAIN[1:0]	01	AIF1 DRC2 Maximum gain to boost audio signals (dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 36dB	

Register 0451h AIF1 DRC2 (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1106 (0452h) AIF1 DRC2 (3)	15:12	AIF1DRC2_NG_MINGAIN[3:0]	0000	AIF1 DRC2 Minimum gain to attenuate audio signals when the noise gate is active. 0000 = -36dB 0001 = -30dB 0010 = -24dB 0011 = -18dB 0100 = -12dB 0101 = -6dB 0110 = 0dB 0111 = 6dB 1000 = 12dB 1001 = 18dB 1010 = 24dB 1011 = 30dB 1100 = 36dB 1101 to 1111 = Reserved	
	11:10	AIF1DRC2_NG_EXP[1:0]	00	AIF1 DRC2 Noise Gate slope 00 = 1 (no expansion) 01 = 2 10 = 4 11 = 8	
	9:8	AIF1DRC2_QR_THR[1:0]	00	AIF1 DRC2 Quick-release threshold (crest factor in dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB	
	7:6	AIF1DRC2_QR_DCY[1:0]	00	AIF1 DRC2 Quick-release decay rate (seconds/6dB) 00 = 0.725ms 01 = 1.45ms 10 = 5.8ms 11 = reserved	
	5:3	AIF1DRC2_HI_COMP[2:0]	000	AIF1 DRC2 Compressor slope (upper region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 0 110 = Reserved 111 = Reserved	
	2:0	AIF1DRC2_LO_COMP[2:0]	000	AIF1 DRC2 Compressor slope (lower region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 0 101 = Reserved 11X = Reserved	

Register 0452h AIF1 DRC2 (3)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1107 (0453h) AIF1 DRC2 (4)	10:5	AIF1DRC2_KNEE_IP[5:0]	00_0000	AIF1 DRC2 Input signal level at the Compressor 'Knee'. 000000 = 0dB 000001 = -0.75dB 000010 = -1.5dB … (-0.75dB steps) 111100 = -45dB 111101 = Reserved 11111X = Reserved	
	4:0	AIF1DRC2_KNEE_OP[4:0]	0_0000	AIF1 DRC2 Output signal at the Compressor 'Knee'. 00000 = 0dB 00001 = -0.75dB 00010 = -1.5dB … (-0.75dB steps) 11110 = -22.5dB 11111 = Reserved	

Register 0453h AIF1 DRC2 (4)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1108 (0454h) AIF1 DRC2 (5)	9:5	AIF1DRC2_KNEE2_IP[4:0]	0_0000	AIF1 DRC2 Input signal level at the Noise Gate threshold 'Knee2'. 00000 = -36dB 00001 = -37.5dB 00010 = -39dB … (-1.5dB steps) 11110 = -81dB 11111 = -82.5dB Only applicable when DRC_NG_ENA = 1.	
	4:0	AIF1DRC2_KNEE2_OP[4:0]	0_0000	AIF1 DRC2 Output signal at the Noise Gate threshold 'Knee2'. 00000 = -30dB 00001 = -31.5dB 00010 = -33dB … (-1.5dB steps) 11110 = -75dB 11111 = -76.5dB Only applicable when DRC_KNEE2_OP_ENA = 1.	

Register 0454h AIF1 DRC2 (5)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1152 (0480h) AIF1 DAC1 EQ Gains (1)	15:11	AIF1DAC1_EQ_B1_GAIN[4:0]	0_1100	AIF1DAC1 (AIF1, Timeslot 0) EQ Band 1 Gain 00000 = -12dB 00001 = -11dB … 10111 = +11dB 11000 = +12dB 11001 to 11111 Reserved	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	10:6	AIF1DAC1_EQ_B2_GAIN[4:0]	0_1100	AIF1DAC1 (AIF1, Timeslot 0) EQ Band 2 Gain 00000 = -12dB 00001 = -11dB … 10111 = +11dB 11000 = +12dB 11001 to 11111 Reserved	
	5:1	AIF1DAC1_EQ_B3_GAIN[4:0]	0_1100	AIF1DAC1 (AIF1, Timeslot 0) EQ Band 3 Gain 00000 = -12dB 00001 = -11dB … 10111 = +11dB 11000 = +12dB 11001 to 11111 Reserved	
	0	AIF1DAC1_EQ_ENA	0	Enable EQ in AIF1DAC1 playback path (AIF1, Timeslot 0) 0 = Disabled 1 = Enabled	

Register 0480h AIF1 DAC1 EQ Gains (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1153 (0481h) AIF1 DAC1 EQ Gains (2)	15:11	AIF1DAC1_EQ_B4_GAIN[4:0]	0_1100	AIF1DAC1 (AIF1, Timeslot 0) EQ Band 4 Gain 00000 = -12dB 00001 = -11dB … 10111 = +11dB 11000 = +12dB 11001 to 11111 Reserved	
	10:6	AIF1DAC1_EQ_B5_GAIN[4:0]	0_1100	AIF1DAC1 (AIF1, Timeslot 0) EQ Band 5 Gain 00000 = -12dB 00001 = -11dB … 10111 = +11dB 11000 = +12dB 11001 to 11111 Reserved	

Register 0481h AIF1 DAC1 EQ Gains (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1154 (0482h) AIF1 DAC1 EQ Band 1 A	15:0	AIF1DAC1_EQ_B1_A[15:0]	0000_1111_1100_1010	EQ Band 1 Coefficient A	

Register 0482h AIF1 DAC1 EQ Band 1 A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1155 (0483h) AIF1 DAC1 EQ Band 1 B	15:0	AIF1DAC1_EQ_B1_B[15:0]	0000_0100_0000_0000	EQ Band 1 Coefficient B	

Register 0483h AIF1 DAC1 EQ Band 1 B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1156 (0484h) AIF1 DAC1 EQ Band 1 PG	15:0	AIF1DAC1_EQ_B1_PG[15:0]	0000_0000_1101_1000	EQ Band 1 Coefficient PG	

Register 0484h AIF1 DAC1 EQ Band 1 PG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1157 (0485h) AIF1 DAC1 EQ Band 2 A	15:0	AIF1DAC1_EQ_B2_A[15:0]	0001_1110_1011_0101	EQ Band 2 Coefficient A	

Register 0485h AIF1 DAC1 EQ Band 2 A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1158 (0486h) AIF1 DAC1 EQ Band 2 B	15:0	AIF1DAC1_EQ_B2_B[15:0]	1111_0001_0100_0101	EQ Band 2 Coefficient B	

Register 0486h AIF1 DAC1 EQ Band 2 B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1159 (0487h) AIF1 DAC1 EQ Band 2 C	15:0	AIF1DAC1_EQ_B2_C[15:0]	0000_1011_0111_0101	EQ Band 2 Coefficient C	

Register 0487h AIF1 DAC1 EQ Band 2 C

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1160 (0488h) AIF1 DAC1 EQ Band 2 PG	15:0	AIF1DAC1_EQ_B2_PG[15:0]	0000_0001_1100_0101	EQ Band 2 Coefficient PG	

Register 0488h AIF1 DAC1 EQ Band 2 PG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1161 (0489h) AIF1 DAC1 EQ Band 3 A	15:0	AIF1DAC1_EQ_B3_A[15:0]	0001_1100_0101_1000	EQ Band 3 Coefficient A	

Register 0489h AIF1 DAC1 EQ Band 3 A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1162 (048Ah) AIF1 DAC1 EQ Band 3 B	15:0	AIF1DAC1_EQ_B3_B[15:0]	1111_0011_0111_0011	EQ Band 3 Coefficient B	

Register 048Ah AIF1 DAC1 EQ Band 3 B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1163 (048Bh) AIF1 DAC1 EQ Band 3 C	15:0	AIF1DAC1_EQ_B3_C[15:0]	0000_1010_0101_0100	EQ Band 3 Coefficient C	

Register 048Bh AIF1 DAC1 EQ Band 3 C

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1164 (048Ch) AIF1 DAC1 EQ Band 3 PG	15:0	AIF1DAC1_EQ_B3_PG[15:0]	0000_0101_0101_1000	EQ Band 3 Coefficient PG	

Register 048Ch AIF1 DAC1 EQ Band 3 PG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1165 (048Dh) AIF1 DAC1 EQ Band 4 A	15:0	AIF1DAC1_EQ_B4_A[15:0]	0001_0110_1000_1110	EQ Band 4 Coefficient A	

Register 048Dh AIF1 DAC1 EQ Band 4 A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1166 (048Eh) AIF1 DAC1 EQ Band 4 B	15:0	AIF1DAC1_EQ_B4_B[15:0]	1111_1000_0010_1001	EQ Band 4 Coefficient B	

Register 048Eh AIF1 DAC1 EQ Band 4 B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1167 (048Fh) AIF1 DAC1 EQ Band 4 C	15:0	AIF1DAC1_EQ_B4_C[15:0]	0000_0111_1010_1101	EQ Band 4 Coefficient C	

Register 048Fh AIF1 DAC1 EQ Band 4 C

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1168 (0490h) AIF1 DAC1 EQ Band 4 PG	15:0	AIF1DAC1_EQ_B4_PG[15:0]	0001_0001_0000_0011	EQ Band 4 Coefficient C	

Register 0490h AIF1 DAC1 EQ Band 4 PG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1169 (0491h) AIF1 DAC1 EQ Band 5 A	15:0	AIF1DAC1_EQ_B5_A[15:0]	0000_0101_0110_0100	EQ Band 5 Coefficient A	

Register 0491h AIF1 DAC1 EQ Band 5 A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1170 (0492h) AIF1 DAC1 EQ Band 5 B	15:0	AIF1DAC1_EQ_B5_B[15:0]	0000_0101_0101_1001	EQ Band 5 Coefficient B	

Register 0492h AIF1 DAC1 EQ Band 5 B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1171 (0493h) AIF1 DAC1 EQ Band 5 PG	15:0	AIF1DAC1_EQ_B5_PG[15:0]	0100_0000_0000_0000	EQ Band 5 Coefficient PG	

Register 0493h AIF1 DAC1 EQ Band 5 PG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1184 (04A0h) AIF1 DAC2 EQ Gains (1)	15:11	AIF1DAC2_EQ_B1_GAIN[4:0]	0_1100	AIF1DAC2 (AIF1, Timeslot 1) EQ Band 1 Gain 00000 = -12dB 00001 = -11dB … 10111 = +11dB 11000 = +12dB 11001 to 11111 Reserved	
	10:6	AIF1DAC2_EQ_B2_GAIN[4:0]	0_1100	AIF1DAC2 (AIF1, Timeslot 1) EQ Band 2 Gain 00000 = -12dB 00001 = -11dB … 10111 = +11dB 11000 = +12dB 11001 to 11111 Reserved	
	5:1	AIF1DAC2_EQ_B3_GAIN[4:0]	0_1100	AIF1DAC2 (AIF1, Timeslot 1) EQ Band 3 Gain 00000 = -12dB 00001 = -11dB … 10111 = +11dB 11000 = +12dB 11001 to 11111 Reserved	
	0	AIF1DAC2_EQ_ENA	0	Enable EQ in AIF1DAC2 playback path (AIF1, Timeslot 1) 0 = Disabled 1 = Enabled	

Register 04A0h AIF1 DAC2 EQ Gains (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1185 (04A1h) AIF1 DAC2 EQ Gains (2)	15:11	AIF1DAC2_EQ_B4_GAIN[4:0]	0_1100	AIF1DAC2 (AIF1, Timeslot 1) EQ Band 4 Gain 00000 = -12dB 00001 = -11dB … 10111 = +11dB 11000 = +12dB 11001 to 11111 Reserved	
	10:6	AIF1DAC2_EQ_B5_GAIN[4:0]	0_1100	AIF1DAC2 (AIF1, Timeslot 1) EQ Band 5 Gain 00000 = -12dB 00001 = -11dB … 10111 = +11dB 11000 = +12dB 11001 to 11111 Reserved	

Register 04A1h AIF1 DAC2 EQ Gains (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1186 (04A2h) AIF1 DAC2 EQ Band 1 A	15:0	AIF1DAC2_EQ_B1_A[15:0]	0000_1111_1100_1010	EQ Band 1 Coefficient A	

Register 04A2h AIF1 DAC2 EQ Band 1 A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1187 (04A3h) AIF1 DAC2 EQ Band 1 B	15:0	AIF1DAC2_EQ_B1_B[15:0]	0000_0100_0000_0000	EQ Band 1 Coefficient B	

Register 04A3h AIF1 DAC2 EQ Band 1 B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1188 (04A4h) AIF1 DAC2 EQ Band 1 PG	15:0	AIF1DAC2_EQ_B1_PG[15:0]	0000_0000_1101_1000	EQ Band 1 Coefficient PG	

Register 04A4h AIF1 DAC2 EQ Band 1 PG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1189 (04A5h) AIF1 DAC2 EQ Band 2 A	15:0	AIF1DAC2_EQ_B2_A[15:0]	0001_1110_1011_0101	EQ Band 2 Coefficient A	

Register 04A5h AIF1 DAC2 EQ Band 2 A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1190 (04A6h) AIF1 DAC2 EQ Band 2 B	15:0	AIF1DAC2_EQ_B2_B[15:0]	1111_0001_0100_0101	EQ Band 2 Coefficient B	

Register 04A6h AIF1 DAC2 EQ Band 2 B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1191 (04A7h) AIF1 DAC2 EQ Band 2 C	15:0	AIF1DAC2_EQ_B2_C[15:0]	0000_1011_0111_0101	EQ Band 2 Coefficient C	

Register 04A7h AIF1 DAC2 EQ Band 2 C

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1192 (04A8h) AIF1 DAC2 EQ Band 2 PG	15:0	AIF1DAC2_EQ_B2_PG[15:0]	0000_0001_1100_0101	EQ Band 2 Coefficient PG	

Register 04A8h AIF1 DAC2 EQ Band 2 PG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1193 (04A9h) AIF1 DAC2 EQ Band 3 A	15:0	AIF1DAC2_EQ_B3_A[15:0]	0001_1100_0101_1000	EQ Band 3 Coefficient A	

Register 04A9h AIF1 DAC2 EQ Band 3 A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1194 (04AAh) AIF1 DAC2 EQ Band 3 B	15:0	AIF1DAC2_EQ_B3_B[15:0]	1111_0011_0111_0011	EQ Band 3 Coefficient B	

Register 04AAh AIF1 DAC2 EQ Band 3 B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1195 (04ABh) AIF1 DAC2 EQ Band 3 C	15:0	AIF1DAC2_EQ_B3_C[15:0]	0000_1010_0101_0100	EQ Band 3 Coefficient C	

Register 04ABh AIF1 DAC2 EQ Band 3 C

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1196 (04ACh) AIF1 DAC2 EQ Band 3 PG	15:0	AIF1DAC2_EQ_B3_PG[15:0]	0000_0101_0101_1000	EQ Band 3 Coefficient PG	

Register 04ACh AIF1 DAC2 EQ Band 3 PG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1197 (04ADh) AIF1 DAC2 EQ Band 4 A	15:0	AIF1DAC2_EQ_B4_A[15:0]	0001_0110_1000_1110	EQ Band 4 Coefficient A	

Register 04ADh AIF1 DAC2 EQ Band 4 A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1198 (04AEh) AIF1 DAC2 EQ Band 4 B	15:0	AIF1DAC2_EQ_B4_B[15:0]	1111_1000_0010_1001	EQ Band 4 Coefficient B	

Register 04AEh AIF1 DAC2 EQ Band 4 B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1199 (04AFh) AIF1 DAC2 EQ Band 4 C	15:0	AIF1DAC2_EQ_B4_C[15:0]	0000_0111_1010_1101	EQ Band 4 Coefficient C	

Register 04AFh AIF1 DAC2 EQ Band 4 C

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1200 (04B0h) AIF1 DAC2 EQ Band 4 PG	15:0	AIF1DAC2_EQ_B4_PG[15:0]	0001_0001_0000_0011	EQ Band 4 Coefficient C	

Register 04B0h AIF1 DAC2 EQ Band 4 PG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1201 (04B1h) AIF1 DAC2 EQ Band 5 A	15:0	AIF1DAC2_EQ_B5_A[15:0]	0000_0101_0110_0100	EQ Band 5 Coefficient A	

Register 04B1h AIF1 DAC2 EQ Band 5 A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1202 (04B2h) AIF1 DAC2 EQ Band 5 B	15:0	AIF1DAC2_EQ_B5_B[15:0]	0000_0101_0101_1001	EQ Band 5 Coefficient B	

Register 04B2h AIF1 DAC2 EQ Band 5 B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1203 (04B3h) AIF1 DAC2 EQ Band 5 PG	15:0	AIF1DAC2_EQ_B5_PG[15:0]	0100_0000_0000_0000	EQ Band 5 Coefficient PG	

Register 04B3h AIF1 DAC2 EQ Band 5 PG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1280 (0500h) AIF2 ADC Left Volume	8	AIF2ADC_VU	0	AIF2ADC output path Volume Update Writing a 1 to this bit will cause the AIF2ADCL and AIF2ADCR volume to be updated simultaneously	
	7:0	AIF2ADCL_VOL[7:0]	1100_0000	AIF2ADC (Left) output path Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) EFh = +17.625dB	

Register 0500h AIF2 ADC Left Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1281 (0501h) AIF2 ADC Right Volume	8	AIF2ADC_VU	0	AIF2ADC output path Volume Update Writing a 1 to this bit will cause the AIF2ADCL and AIF2ADCR volume to be updated simultaneously	
	7:0	AIF2ADCR_VOL[7:0]	1100_0000	AIF2ADC (Right) output path Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) EFh = +17.625dB	

Register 0501h AIF2 ADC Right Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1282 (0502h) AIF2 DAC Left Volume	8	AIF2DAC_VU	0	AIF2DAC input path Volume Update Writing a 1 to this bit will cause the AIF2DACL and AIF2DACR volume to be updated simultaneously	
	7:0	AIF2DACL_VOL[7:0]	1100_0000	AIF2DAC (Left) input path Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB	

Register 0502h AIF2 DAC Left Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1283 (0503h) AIF2 DAC Right Volume	8	AIF2DAC_VU	0	AIF2DAC input path Volume Update Writing a 1 to this bit will cause the AIF2DACL and AIF2DACR volume to be updated simultaneously	
	7:0	AIF2DACR_VOL[7:0]	1100_0000	AIF2DAC (Right) input path Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB	

Register 0503h AIF2 DAC Right Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1296 (0510h) AIF2 ADC Filters	15	AIF2ADC_4FS	0	[No description available]	
	14:13	AIF2ADC_HPF_CUT[1:0]	00	AIF2ADC output path Digital HPF Cut-Off Frequency (fc) 00 = Hi-fi mode (fc = 4Hz at fs = 48kHz) 01 = Voice mode 1 (fc = 127Hz at fs = 8kHz) 10 = Voice mode 2 (fc = 130Hz at fs = 8kHz) 11 = Voice mode 3 (fc = 267Hz at fs = 8kHz)	
	12	AIF2ADCL_HPF	0	AIF2ADC (Left) output path Digital HPF Enable 0 = Disabled 1 = Enabled	
	11	AIF2ADCR_HPF	0	AIF2ADC (Right) output path Digital HPF Enable 0 = Disabled 1 = Enabled	

Register 0510h AIF2 ADC Filters

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1312 (0520h) AIF2 DAC Filters (1)	9	AIF2DAC_MUTE	1	AIF2DAC input path Soft Mute Control 0 = Un-mute 1 = Mute	
	7	AIF2DAC_MONO	0	AIF2DAC input path Mono Mix Control 0 = Disabled 1 = Enabled	
	5	AIF2DAC_MUTERATE	0	AIF2DAC input path Soft Mute Ramp Rate 0 = Fast ramp (fs/2, maximum ramp time is 10.7ms at fs=48k) 1 = Slow ramp (fs/32, maximum ramp time is 171ms at fs=48k) (Note: ramp rate scales with sample rate.)	
	4	AIF2DAC_UNMUTE_RAMP	0	AIF2DAC input path Unmute Ramp select 0 = Disabling soft-mute (AIF2DAC_MUTE=0) will cause the volume to change immediately to AIF2DACL_VOL and AIF2DACR_VOL settings 1 = Disabling soft-mute (AIF2DAC_MUTE=0) will cause the DAC volume to ramp up gradually to the AIF2DACL_VOL and AIF2DACR_VOL settings	
	2:1	AIF2DAC_DEEMP[1:0]	00	AIF2DAC input path De-Emphasis Control 00 = No de-emphasis 01 = 32kHz sample rate 10 = 44.1kHz sample rate 11 = 48kHz sample rate	

Register 0520h AIF2 DAC Filters (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1313 (0521h) AIF2 DAC Filters (2)	13:9	AIF2DAC_3D_GAIN[4:0]	0_0000	AIF2DAC playback path 3D Stereo depth 00000 = Off 00001 = Minimum (-16dB) …(0.915dB steps) 11111 = Maximum (+11.5dB)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	8	AIF2DAC_3D_ENA	0	Enable 3D Stereo in AIF2DAC playback path 0 = Disabled 1 = Enabled	

Register 0521h AIF2 DAC Filters (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1344 (0540h) AIF2 DRC (1)	15:11	AIF2DRC_SIG_DET_RMS[4:0]	0_0000	AIF2 DRC Signal Detect RMS Threshold. This is the RMS signal level for signal detect to be indicated when AIF2DRC_SIG_DET_MODE=0. 00000 = -30dB 00001 = -31.5dB …. (1.5dB steps) 11110 = -75dB 11111 = -76.5dB	
	10:9	AIF2DRC_SIG_DET_PK[1:0]	00	AIF2 DRC Signal Detect Peak Threshold. This is the Peak/RMS ratio, or Crest Factor, level for signal detect to be indicated when AIF2DRC_SIG_DET_MODE=1. 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB	
	8	AIF2DRC_NG_ENA	0	AIF2 DRC Noise Gate Enable 0 = Disabled 1 = Enabled	
	7	AIF2DRC_SIG_DET_MODE	1	AIF2 DRC Signal Detect Mode 0 = RMS threshold mode 1 = Peak threshold mode	
	6	AIF2DRC_SIG_DET	0	AIF2 DRC Signal Detect Enable 0 = Disabled 1 = Enabled	
	5	AIF2DRC_KNEE2_OP_ENA	0	AIF2 DRC KNEE2_OP Enable 0 = Disabled 1 = Enabled	
	4	AIF2DRC_QR	1	AIF2 DRC Quick-release Enable 0 = Disabled 1 = Enabled	
	3	AIF2DRC_ANTICLIP	1	AIF2 DRC Anti-clip Enable 0 = Disabled 1 = Enabled	
	2	AIF2DAC_DRC_ENA	0	Enable DRC in AIF2DAC playback path 0 = Disabled 1 = Enabled	
	1	AIF2ADCL_DRC_ENA	0	Enable DRC in AIF2ADC (Left) record path 0 = Disabled 1 = Enabled	
	0	AIF2ADCR_DRC_ENA	0	Enable DRC in AIF2ADC (Right) record path 0 = Disabled 1 = Enabled	

Register 0540h AIF2 DRC (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1345 (0541h) AIF2 DRC (2)	12:9	AIF2DRC_ATK [3:0]	0100	AIF2 DRC Gain attack rate (seconds/6dB) 0000 = Reserved 0001 = 181us 0010 = 363us 0011 = 726us 0100 = 1.45ms 0101 = 2.9ms 0110 = 5.8ms 0111 = 11.6ms 1000 = 23.2ms 1001 = 46.4ms 1010 = 92.8ms 1011 = 185.6ms 1100-1111 = Reserved	
	8:5	AIF2DRC_DCY [3:0]	0010	AIF2 DRC Gain decay rate (seconds/6dB) 0000 = 186ms 0001 = 372ms 0010 = 743ms 0011 = 1.49s 0100 = 2.97s 0101 = 5.94s 0110 = 11.89s 0111 = 23.78s 1000 = 47.56s 1001-1111 = Reserved	
	4:2	AIF2DRC_MIN GAIN[2:0]	001	AIF2 DRC Minimum gain to attenuate audio signals 000 = 0dB 001 = -12dB (default) 010 = -18dB 011 = -24dB 100 = -36dB 101 = Reserved 11X = Reserved	
	1:0	AIF2DRC_MAX GAIN[1:0]	01	AIF2 DRC Maximum gain to boost audio signals (dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 36dB	

Register 0541h AIF2 DRC (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1346 (0542h) AIF2 DRC (3)	15:12	AIF2DRC_NG_MINGAIN[3:0]	0000	AIF2 DRC Minimum gain to attenuate audio signals when the noise gate is active. 0000 = -36dB 0001 = -30dB 0010 = -24dB 0011 = -18dB 0100 = -12dB 0101 = -6dB 0110 = 0dB 0111 = 6dB 1000 = 12dB 1001 = 18dB 1010 = 24dB 1011 = 30dB 1100 = 36dB 1101 to 1111 = Reserved	
	11:10	AIF2DRC_NG_EXP[1:0]	00	AIF2 DRC Noise Gate slope 00 = 1 (no expansion) 01 = 2 10 = 4 11 = 8	
	9:8	AIF2DRC_QR_THR[1:0]	00	AIF2 DRC Quick-release threshold (crest factor in dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB	
	7:6	AIF2DRC_QR_DCY[1:0]	00	AIF2 DRC Quick-release decay rate (seconds/6dB) 00 = 0.725ms 01 = 1.45ms 10 = 5.8ms 11 = reserved	
	5:3	AIF2DRC_HI_COMP[2:0]	000	AIF2 DRC Compressor slope (upper region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 0 110 = Reserved 111 = Reserved	
	2:0	AIF2DRC_LO_COMP[2:0]	000	AIF2 DRC Compressor slope (lower region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 0 101 = Reserved 11X = Reserved	

Register 0542h AIF2 DRC (3)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1347 (0543h) AIF2 DRC (4)	10:5	AIF2DRC_KNEE_IP[5:0]	00_0000	AIF2 DRC Input signal level at the Compressor 'Knee'. 000000 = 0dB 000001 = -0.75dB 000010 = -1.5dB … (-0.75dB steps) 111100 = -45dB 111101 = Reserved 11111X = Reserved	
	4:0	AIF2DRC_KNEE_OP[4:0]	0_0000	AIF2 DRC Output signal at the Compressor 'Knee'. 00000 = 0dB 00001 = -0.75dB 00010 = -1.5dB … (-0.75dB steps) 11110 = -22.5dB 11111 = Reserved	

Register 0543h AIF2 DRC (4)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1348 (0544h) AIF2 DRC (5)	9:5	AIF2DRC_KNEE2_IP[4:0]	0_0000	AIF2 DRC Input signal level at the Noise Gate threshold 'Knee2'. 00000 = -36dB 00001 = -37.5dB 00010 = -39dB … (-1.5dB steps) 11110 = -81dB 11111 = -82.5dB Only applicable when DRC_NG_ENA = 1.	
	4:0	AIF2DRC_KNEE2_OP[4:0]	0_0000	AIF2 DRC Output signal at the Noise Gate threshold 'Knee2'. 00000 = -30dB 00001 = -31.5dB 00010 = -33dB … (-1.5dB steps) 11110 = -75dB 11111 = -76.5dB Only applicable when DRC_KNEE2_OP_ENA = 1.	

Register 0544h AIF2 DRC (5)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1408 (0580h) AIF2 EQ Gains (1)	15:11	AIF2DAC_EQ_B1_GAIN[4:0]	0_1100	AIF2 EQ Band 1 Gain	
	10:6	AIF2DAC_EQ_B2_GAIN[4:0]	0_1100	AIF2EQ Band 2 Gain	
	5:1	AIF2DAC_EQ_B3_GAIN[4:0]	0_1100	AIF2EQ Band 3 Gain	
	0	AIF2DAC_EQ_ENA	0	Enable EQ in AIF2DAC playback path 0 = Disabled 1 = Enabled	

Register 0580h AIF2 EQ Gains (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1409 (0581h) AIF2 EQ Gains (2)	15:11	AIF2DAC_EQ_B4_GAIN[4:0]	0_1100	AIF2EQ Band 4 Gain	
	10:6	AIF2DAC_EQ_B5_GAIN[4:0]	0_1100	AIF2EQ Band 5 Gain	

Register 0581h AIF2 EQ Gains (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1410 (0582h) AIF2 EQ Band 1 A	15:0	AIF2DAC_EQ_B1_A[15:0]	0000_1111_1100_1010	EQ Band 1 Coefficient A	

Register 0582h AIF2 EQ Band 1 A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1411 (0583h) AIF2 EQ Band 1 B	15:0	AIF2DAC_EQ_B1_B[15:0]	0000_0100_0000_0000	EQ Band 1 Coefficient B	

Register 0583h AIF2 EQ Band 1 B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1412 (0584h) AIF2 EQ Band 1 PG	15:0	AIF2DAC_EQ_B1_PG[15:0]	0000_0000_1101_1000	EQ Band 1 Coefficient PG	

Register 0584h AIF2 EQ Band 1 PG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1413 (0585h) AIF2 EQ Band 2 A	15:0	AIF2DAC_EQ_B2_A[15:0]	0001_1110_1011_0101	EQ Band 2 Coefficient A	

Register 0585h AIF2 EQ Band 2 A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1414 (0586h) AIF2 EQ Band 2 B	15:0	AIF2DAC_EQ_B2_B[15:0]	1111_0001_0100_0101	EQ Band 2 Coefficient B	

Register 0586h AIF2 EQ Band 2 B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1415 (0587h) AIF2 EQ Band 2 C	15:0	AIF2DAC_EQ_B2_C[15:0]	0000_1011_0111_0101	EQ Band 2 Coefficient C	

Register 0587h AIF2 EQ Band 2 C

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1416 (0588h) AIF2 EQ Band 2 PG	15:0	AIF2DAC_EQ_B2_PG[15:0]	0000_0001_1100_0101	EQ Band 2 Coefficient PG	

Register 0588h AIF2 EQ Band 2 PG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1417 (0589h) AIF2 EQ Band 3 A	15:0	AIF2DAC_EQ_B3_A[15:0]	0001_1100_0101_1000	EQ Band 3 Coefficient A	

Register 0589h AIF2 EQ Band 3 A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1418 (058Ah) AIF2 EQ Band 3 B	15:0	AIF2DAC_EQ_B3_B[15:0]	1111_0011_0111_0011	EQ Band 3 Coefficient B	

Register 058Ah AIF2 EQ Band 3 B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1419 (058Bh) AIF2 EQ Band 3 C	15:0	AIF2DAC_EQ_B3_C[15:0]	0000_1010_0101_0100	EQ Band 3 Coefficient C	

Register 058Bh AIF2 EQ Band 3 C

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1420 (058Ch) AIF2 EQ Band 3 PG	15:0	AIF2DAC_EQ_B3_PG[15:0]	0000_0101_0101_1000	EQ Band 3 Coefficient PG	

Register 058Ch AIF2 EQ Band 3 PG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1421 (058Dh) AIF2 EQ Band 4 A	15:0	AIF2DAC_EQ_B4_A[15:0]	0001_0110_1000_1110	EQ Band 4 Coefficient A	

Register 058Dh AIF2 EQ Band 4 A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1422 (058Eh) AIF2 EQ Band 4 B	15:0	AIF2DAC_EQ_B4_B[15:0]	1111_1000_0010_1001	EQ Band 4 Coefficient B	

Register 058Eh AIF2 EQ Band 4 B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1423 (058Fh) AIF2 EQ Band 4 C	15:0	AIF2DAC_EQ_B4_C[15:0]	0000_0111_1010_1101	EQ Band 4 Coefficient C	

Register 058Fh AIF2 EQ Band 4 C

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1424 (0590h) AIF2 EQ Band 4 PG	15:0	AIF2DAC_EQ_B4_PG[15:0]	0001_0001_0000_0011	EQ Band 4 Coefficient PG	

Register 0590h AIF2 EQ Band 4 PG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1425 (0591h) AIF2 EQ Band 5 A	15:0	AIF2DAC_EQ_B5_A[15:0]	0000_0101_0110_0100	EQ Band 5 Coefficient A	

Register 0591h AIF2 EQ Band 5 A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1426 (0592h) AIF2 EQ Band 5 B	15:0	AIF2DAC_EQ_B5_B[15:0]	0000_0101_0101_1001	EQ Band 5 Coefficient B	

Register 0592h AIF2 EQ Band 5 B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1427 (0593h) AIF2 EQ Band 5 PG	15:0	AIF2DAC_EQ_B5_PG[15:0]	0100_0000_0000_0000	EQ Band 5 Coefficient PG	

Register 0593h AIF2 EQ Band 5 PG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1536 (0600h) DAC1 Mixer Volumes	8:5	ADC2_DAC1_VOL[3:0]	0000	Sidetone ST2 to DAC1L and DAC1R Volume 0000 = -36dB 0001 = -33dB …. (3dB steps) 1011 = -3dB 1100 = 0dB	
	3:0	ADC1_DAC1_VOL[3:0]	0000	Sidetone ST1 to DAC1L and DAC1R Volume 0000 = -36dB 0001 = -33dB …. (3dB steps) 1011 = -3dB 1100 = 0dB	

Register 0600h DAC1 Mixer Volumes

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1537 (0601h) DAC1 Left Mixer Routing	5	ADC2_TO_DAC1L	0	Enable Sidetone ST2 to DAC1L 0 = Disabled 1 = Enabled	
	4	ADC1_TO_DAC1L	0	Enable Sidetone ST1 to DAC1L 0 = Disabled 1 = Enabled	
	2	AIF2DACL_TO_DAC1L	0	Enable AIF2 (Left) to DAC1L 0 = Disabled 1 = Enabled	
	1	AIF1DAC2L_TO_DAC1L	0	Enable AIF1 (Timeslot 1, Left) to DAC1L 0 = Disabled 1 = Enabled	
	0	AIF1DAC1L_TO_DAC1L	0	Enable AIF1 (Timeslot 0, Left) to DAC1L 0 = Disabled 1 = Enabled	

Register 0601h DAC1 Left Mixer Routing

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1538 (0602h) DAC1 Right Mixer Routing	5	ADC2_TO_DAC1R	0	Enable Sidetone ST2 to DAC1R 0 = Disabled 1 = Enabled	
	4	ADC1_TO_DAC1R	0	Enable Sidetone ST1 to DAC1R 0 = Disabled 1 = Enabled	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	2	AIF2DACR_TO_DAC1R	0	Enable AIF2 (Right) to DAC1R 0 = Disabled 1 = Enabled	
	1	AIF1DAC2R_TO_DAC1R	0	Enable AIF1 (Timeslot 1, Right) to DAC1R 0 = Disabled 1 = Enabled	
	0	AIF1DAC1R_TO_DAC1R	0	Enable AIF1 (Timeslot 0, Right) to DAC1R 0 = Disabled 1 = Enabled	

Register 0602h DAC1 Right Mixer Routing

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1539 (0603h) DAC2 Mixer Volumes	8:5	ADC2_DAC2_VOL[3:0]	0000	Sidetone ST2 to DAC2L and DAC2R Volume 0000 = -36dB 0001 = -33dB …. (3dB steps) 1011 = -3dB 1100 = 0dB	
	3:0	ADC1_DAC2_VOL[3:0]	0000	Sidetone ST1 to DAC2L and DAC2R Volume 0000 = -36dB 0001 = -33dB …. (3dB steps) 1011 = -3dB 1100 = 0dB	

Register 0603h DAC2 Mixer Volumes

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1540 (0604h) DAC2 Left Mixer Routing	5	ADC2_TO_DAC2L	0	Enable Sidetone ST2 to DAC2L 0 = Disabled 1 = Enabled	
	4	ADC1_TO_DAC2L	0	Enable Sidetone ST1 to DAC2L 0 = Disabled 1 = Enabled	
	2	AIF2DACL_TO_DAC2L	0	Enable AIF2 (Left) to DAC2L 0 = Disabled 1 = Enabled	
	1	AIF1DAC2L_TO_DAC2L	0	Enable AIF1 (Timeslot 1, Left) to DAC2L 0 = Disabled 1 = Enabled	
	0	AIF1DAC1L_TO_DAC2L	0	Enable AIF1 (Timeslot 0, Left) to DAC2L 0 = Disabled 1 = Enabled	

Register 0604h DAC2 Left Mixer Routing

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1541 (0605h) DAC2 Right Mixer Routing	5	ADC2_TO_DAC2R	0	Enable Sidetone ST2 to DAC2R 0 = Disabled 1 = Enabled	
	4	ADC1_TO_DAC2R	0	Enable Sidetone ST1 to DAC2R 0 = Disabled 1 = Enabled	
	2	AIF2DACR_TO_DAC2R	0	Enable AIF2 (Right) to DAC2R 0 = Disabled 1 = Enabled	
	1	AIF1DAC2R_TO_DAC2R	0	Enable AIF1 (Timeslot 1, Right) to DAC2R 0 = Disabled 1 = Enabled	
	0	AIF1DAC1R_TO_DAC2R	0	Enable AIF1 (Timeslot 0, Right) to DAC2R 0 = Disabled 1 = Enabled	

Register 0605h DAC2 Right Mixer Routing

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1542 (0606h) AIF1 ADC1 Left Mixer Routing	1	ADC1L_TO_AIF1ADC1L	0	Enable ADCL / DMIC1 (Left) to AIF1 (Timeslot 0, Left) output 0 = Disabled 1 = Enabled	
	0	AIF2DACL_TO_AIF1ADC1L	0	Enable AIF2 (Left) to AIF1 (Timeslot 0, Left) output 0 = Disabled 1 = Enabled	

Register 0606h AIF1 ADC1 Left Mixer Routing

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1543 (0607h) AIF1 ADC1 Right Mixer Routing	1	ADC1R_TO_AIF1ADC1R	0	Enable ADCR / DMIC1 (Right) to AIF1 (Timeslot 0, Right) output 0 = Disabled 1 = Enabled	
	0	AIF2DACR_TO_AIF1ADC1R	0	Enable AIF2 (Right) to AIF1 (Timeslot 0, Right) output 0 = Disabled 1 = Enabled	

Register 0607h AIF1 ADC1 Right Mixer Routing

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1544 (0608h) AIF1 ADC2 Left Mixer Routing	1	ADC2L_TO_AIF1ADC2L	0	Enable DMIC2 (Left) to AIF1 (Timeslot 1, Left) output 0 = Disabled 1 = Enabled	
	0	AIF2DACL_TO_AIF1ADC2L	0	Enable AIF2 (Left) to AIF1 (Timeslot 1, Left) output 0 = Disabled 1 = Enabled	

Register 0608h AIF1 ADC2 Left Mixer Routing

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1545 (0609h) AIF1 ADC2 Right mixer Routing	1	ADC2R_TO_AIF1ADC2R	0	Enable DMIC2 (Right) to AIF1 (Timeslot 1, Right) output 0 = Disabled 1 = Enabled	
	0	AIF2DACR_TO_AIF1ADC2R	0	Enable AIF2 (Right) to AIF1 (Timeslot 1, Right) output 0 = Disabled 1 = Enabled	

Register 0609h AIF1 ADC2 Right mixer Routing

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1552 (0610h) DAC1 Left Volume	9	DAC1L_MUTE	1	DAC1L Soft Mute Control 0 = DAC Un-mute 1 = DAC Mute	
	8	DAC1_VU	0	DAC1L and DAC1R Volume Update Writing a 1 to this bit will cause the DAC1L and DAC1R volume to be updated simultaneously	
	7:0	DAC1L_VOL[7:0]	1100_0000	DAC1L Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB	

Register 0610h DAC1 Left Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1553 (0611h) DAC1 Right Volume	9	DAC1R_MUTE	1	DAC1R Soft Mute Control 0 = DAC Un-mute 1 = DAC Mute	
	8	DAC1_VU	0	DAC1L and DAC1R Volume Update Writing a 1 to this bit will cause the DAC1L and DAC1R volume to be updated simultaneously	
	7:0	DAC1R_VOL[7:0]	1100_0000	DAC1R Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB	

Register 0611h DAC1 Right Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1554 (0612h) DAC2 Left Volume	9	DAC2L_MUTE	1	DAC2L Soft Mute Control 0 = DAC Un-mute 1 = DAC Mute	
	8	DAC2_VU	0	DAC2L and DAC2R Volume Update Writing a 1 to this bit will cause the DAC2L and DAC2R volume to be updated simultaneously	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	7:0	DAC2L_VOL[7:0]	1100_0000	DAC2L Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB	

Register 0612h DAC2 Left Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1555 (0613h) DAC2 Right Volume	9	DAC2R_MUTE	1	DAC2R Soft Mute Control 0 = DAC Un-mute 1 = DAC Mute	
	8	DAC2_VU	0	DAC2R and DAC2R Volume Update Writing a 1 to this bit will cause the DAC2R and DAC2R volume to be updated simultaneously	
	7:0	DAC2R_VOL[7:0]	1100_0000	DAC2R Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB	

Register 0613h DAC2 Right Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1556 (0614h) DAC Softmute	1	DAC_SOFTMUTEMODE	0	DAC Unmute Ramp select 0 = Disabling soft-mute (DAC[1/2][L/R]_MUTE=0) will cause the DAC volume to change immediately to DAC[1/2][L/R]_VOL settings 1 = Disabling soft-mute (DAC[1/2][L/R]_MUTE=0) will cause the DAC volume to ramp up gradually to the DAC[1/2][L/R]_VOL settings	
	0	DAC_MUTERATE	0	DAC Soft Mute Ramp Rate 0 = Fast ramp (fs/2, maximum ramp time is 10.7ms at fs=48k) 1 = Slow ramp (fs/32, maximum ramp time is 171ms at fs=48k) (Note: ramp rate scales with sample rate.)	

Register 0614h DAC Softmute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1568 (0620h) Oversampling	1	ADC_OSR128	1	ADC Oversample Rate Select 0 = Disabled 1 = Enabled For 48kHz sample rate, the ADC oversample rate is 128fs when ADC_OSR128 = 1. The ADC oversample rate is 64fs when ADC_OSR128 = 0.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	0	DAC_OSR128	0	DAC Oversample Rate Select 0 = Disabled 1 = Enabled For 48kHz sample rate, the DAC oversample rate is 128fs when DAC_OSR128 = 1. The DAC oversample rate is 64fs when DAC_OSR128 = 0.	

Register 0620h Oversampling

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1569 (0621h) Sidetone	9:7	ST_HPF_CUT[2:0]	000	Sidetone HPF cut-off frequency (relative to 44.1kHz sample rate) 000 = 2.7kHz 001 = 1.35kHz 010 = 675Hz 011 = 370Hz 100 = 180Hz 101 = 90Hz 110 = 45Hz 111 = Reserved Note - the cut-off frequencies scale with the Digital Mixing (SYSCLK) clocking rate. The quoted figures apply to 44.1kHz sample rate.	
	6	ST_HPF	0	Digital Sidetone HPF Select 0 = Disabled 1 = Enabled	
	1	ST2_SEL	0	Select source for sidetone ST2 path 0 = DMIC2 (Left) 1 = DMIC2 (Right)	
	0	ST1_SEL	0	Select source for sidetone ST1 path 0 = ADCL / DMIC1 (Left) 1 = ADCR / DMIC1 (Right)	

Register 0621h Sidetone

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1792 (0700h) GPIO 1	15	GP1_DIR	1	GPIO1 Pin Direction 0 = Output 1 = Input	
	14	GP1_PU	0	GPIO1 Pull-Up Enable 0 = Disabled 1 = Enabled	
	13	GP1_PD	1	GPIO1 Pull-Down Enable 0 = Disabled 1 = Enabled	
	10	GP1_POL	0	GPIO1 Polarity Select 0 = Non-inverted (Active High) 1 = Inverted (Active Low)	
	9	GP1_OP_CFG	0	GPIO1 Output Configuration 0 = CMOS 1 = Open Drain	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	8	GP1_DB	1	GPIO1 Input De-bounce 0 = Disabled 1 = Enabled	
	6	GP1_LVL	0	GPIO1 level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP1_POL is set, and GP1_DIR = 1 (GPIO input), the GP1_LVL register contains the opposite logic level to the external pin.	
	4:0	GP1_FN[4:0]	0_0000	GPIO1 function. 00000 = ADCLRCLK1 00001 = Logic level input / output 00010 = SDOUT 00011 = IRQ 00100 = Temperature sensor status 00101 = MICBIAS1 current detect 00110 = MICBIAS1 short circuit detect 00111 = MICBIAS2 current detect 01000 = MICBIAS2 short circuit detect 01001 = FLL1 Lock 01010 = FLL2 Lock 01011 = SRC1 Lock 01100 = SRC2 Lock 01101 = DRC1 (AIF1) activity detect 01110 = DRC2 (AIF1) activity detect 01111 = DRC3 (AIF2) activity detect 10000 = Write sequencer status 10001 = FIFO error indicator 10010 = OPCLK 10011 - 11111 = Reserved	

Register 0700h GPIO 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1793 (0701h) GPIO 2	14	GP2_PU	0	GPIO2 Pull-Up Enable 0 = Disabled 1 = Enabled	
	13	GP2_PD	1	GPIO2 Pull-Down Enable 0 = Disabled 1 = Enabled	
	10	GP2_POL	0	GPIO2 Polarity Select 0 = Non-inverted (Active High) 1 = Inverted (Active Low)	
	9	GP2_OP_CFG	0	GPIO2 Output Configuration 0 = CMOS 1 = Open Drain	
	6	GP2_LVL	0	GPIO2 level. Read from this bit to read GPIO input level. When GP2_POL is set, and GP2_DIR = 1 (GPIO input), the GP2_LVL register contains the opposite logic level to the external pin.	
	4:0	GP2_FN[4:0]	0_0001	GPIO2 function. 00000 = MCLK2 00001 = Logic level input	

Register 0701h GPIO 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1794 (0702h) GPIO 3	15	GP3_DIR	1	GPIO3 Pin Direction 0 = Output 1 = Input	
	14	GP3_PU	0	GPIO3 Pull-Up Enable 0 = Disabled 1 = Enabled	
	13	GP3_PD	1	GPIO3 Pull-Down Enable 0 = Disabled 1 = Enabled	
	10	GP3_POL	0	GPIO3 Polarity Select 0 = Non-inverted (Active High) 1 = Inverted (Active Low)	
	9	GP3_OP_CFG	0	GPIO3 Output Configuration 0 = CMOS 1 = Open Drain	
	8	GP3_DB	1	GPIO3 Input De-bounce 0 = Disabled 1 = Enabled	
	6	GP3_LVL	0	GPIO3 level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP3_POL is set, and GP3_DIR = 1 (GPIO input), the GP3_LVL register contains the opposite logic level to the external pin.	
	4:0	GP3_FN[4:0]	0_0001	GPIO3 function. 00000 = BCLK2 00001 = Logic level input / output 00010 = SDOUT 00011 = IRQ 00100 = Temperature sensor status 00101 = MICBIAS1 current detect 00110 = MICBIAS1 short circuit detect 00111 = MICBIAS2 current detect 01000 = MICBIAS2 short circuit detect 01001 = FLL1 Lock 01010 = FLL2 Lock 01011 = SRC1 Lock 01100 = SRC2 Lock 01101 = DRC1 (AIF1) activity detect 01110 = DRC2 (AIF1) activity detect 01111 = DRC3 (AIF2) activity detect 10000 = Write sequencer status 10001 = FIFO error indicator 10010 = OPCLK 10011 - 11111 = Reserved	

Register 0702h GPIO 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1795 (0703h) GPIO 4	15	GP4_DIR	1	GPIO4 Pin Direction 0 = Output 1 = Input	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	14	GP4_PU	0	GPIO4 Pull-Up Enable 0 = Disabled 1 = Enabled	
	13	GP4_PD	1	GPIO4 Pull-Down Enable 0 = Disabled 1 = Enabled	
	10	GP4_POL	0	GPIO4 Polarity Select 0 = Non-inverted (Active High) 1 = Inverted (Active Low)	
	9	GP4_OP_CFG	0	GPIO4 Output Configuration 0 = CMOS 1 = Open Drain	
	8	GP4_DB	1	GPIO4 Input De-bounce 0 = Disabled 1 = Enabled	
	6	GP4_LVL	0	GPIO4 level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP4_POL is set, and GP4_DIR = 1 (GPIO input), the GP4_LVL register contains the opposite logic level to the external pin.	
	4:0	GP4_FN[4:0]	0_0001	GPIO4 function. 00000 = DACLRCLK2 00001 = Logic level input / output 00010 = SDOUT 00011 = IRQ 00100 = Temperature sensor status 00101 = MICBIAS1 current detect 00110 = MICBIAS1 short circuit detect 00111 = MICBIAS2 current detect 01000 = MICBIAS2 short circuit detect 01001 = FLL1 Lock 01010 = FLL2 Lock 01011 = SRC1 Lock 01100 = SRC2 Lock 01101 = DRC1 (AIF1) activity detect 01110 = DRC2 (AIF1) activity detect 01111 = DRC3 (AIF2) activity detect 10000 = Write sequencer status 10001 = FIFO error indicator 10010 = OPCLK 10011 - 11111 = Reserved	

Register 0703h GPIO 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1796 (0704h) GPIO 5	15	GP5_DIR	1	GPIO5 Pin Direction 0 = Output 1 = Input	
	14	GP5_PU	0	GPIO5 Pull-Up Enable 0 = Disabled 1 = Enabled	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	13	GP5_PD	1	GPIO5 Pull-Down Enable 0 = Disabled 1 = Enabled	
	10	GP5_POL	0	GPIO5 Polarity Select 0 = Non-inverted (Active High) 1 = Inverted (Active Low)	
	9	GP5_OP_CFG	0	GPIO5 Output Configuration 0 = CMOS 1 = Open Drain	
	8	GP5_DB	1	GPIO5 Input De-bounce 0 = Disabled 1 = Enabled	
	6	GP5_LVL	0	GPIO5 level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP5_POL is set, and GP5_DIR = 1 (GPIO input), the GP5_LVL register contains the opposite logic level to the external pin.	
	4:0	GP5_FN[4:0]	0_0001	GPIO5 function. 00000 = DACDAT2 00001 = Logic level input / output 00010 = SDOUT 00011 = IRQ 00100 = Temperature sensor status 00101 = MICBIAS1 current detect 00110 = MICBIAS1 short circuit detect 00111 = MICBIAS2 current detect 01000 = MICBIAS2 short circuit detect 01001 = FLL1 Lock 01010 = FLL2 Lock 01011 = SRC1 Lock 01100 = SRC2 Lock 01101 = DRC1 (AIF1) activity detect 01110 = DRC2 (AIF1) activity detect 01111 = DRC3 (AIF2) activity detect 10000 = Write sequencer status 10001 = FIFO error indicator 10010 = OPCLK 10011 - 11111 = Reserved	

Register 0704h GPIO 5

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1797 (0705h) GPIO 6	15	GP6_DIR	1	GPIO6 Pin Direction 0 = Output 1 = Input	
	14	GP6_PU	0	GPIO6 Pull-Up Enable 0 = Disabled 1 = Enabled	
	13	GP6_PD	1	GPIO6 Pull-Down Enable 0 = Disabled 1 = Enabled	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	10	GP6_POL	0	GPIO6 Polarity Select 0 = Non-inverted (Active High) 1 = Inverted (Active Low)	
	9	GP6_OP_CFG	0	GPIO6 Output Configuration 0 = CMOS 1 = Open Drain	
	8	GP6_DB	1	GPIO6 Input De-bounce 0 = Disabled 1 = Enabled	
	6	GP6_LVL	0	GPIO6 level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP6_POL is set, and GP6_DIR = 1 (GPIO input), the GP6_LVL register contains the opposite logic level to the external pin.	
	4:0	GP6_FN[4:0]	0_0001	GPIO6 function. 00000 = ADCLRCLK2 00001 = Logic level input / output 00010 = SDOUT 00011 = IRQ 00100 = Temperature sensor status 00101 = MICBIAS1 current detect 00110 = MICBIAS1 short circuit detect 00111 = MICBIAS2 current detect 01000 = MICBIAS2 short circuit detect 01001 = FLL1 Lock 01010 = FLL2 Lock 01011 = SRC1 Lock 01100 = SRC2 Lock 01101 = DRC1 (AIF1) activity detect 01110 = DRC2 (AIF1) activity detect 01111 = DRC3 (AIF2) activity detect 10000 = Write sequencer status 10001 = FIFO error indicator 10010 = OPCLK 10011 - 11111 = Reserved	

Register 0705h GPIO 6

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1798 (0706h) GPIO 7	15	GP7_DIR	1	GPIO7 Pin Direction 0 = Output 1 = Input	
	14	GP7_PU	0	GPIO7 Pull-Up Enable 0 = Disabled 1 = Enabled	
	13	GP7_PD	1	GPIO7 Pull-Down Enable 0 = Disabled 1 = Enabled	
	10	GP7_POL	0	GPIO7 Polarity Select 0 = Non-inverted (Active High) 1 = Inverted (Active Low)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	9	GP7_OP_CFG	0	GPIO7 Output Configuration 0 = CMOS 1 = Open Drain	
	8	GP7_DB	1	GPIO7 Input De-bounce 0 = Disabled 1 = Enabled	
	6	GP7_LVL	0	GPIO7 level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP7_POL is set, and GP7_DIR = 1 (GPIO input), the GP7_LVL register contains the opposite logic level to the external pin.	
	4:0	GP7_FN[4:0]	0_0001	GPIO7 function. 00000 = ADCDAT2 00001 = Logic level input / output 00010 = SDOUT 00011 = IRQ 00100 = Temperature sensor status 00101 = MICBIAS1 current detect 00110 = MICBIAS1 short circuit detect 00111 = MICBIAS2 current detect 01000 = MICBIAS2 short circuit detect 01001 = FLL1 Lock 01010 = FLL2 Lock 01011 = SRC1 Lock 01100 = SRC2 Lock 01101 = DRC1 (AIF1) activity detect 01110 = DRC2 (AIF1) activity detect 01111 = DRC3 (AIF2) activity detect 10000 = Write sequencer status 10001 = FIFO error indicator 10010 = OPCLK 10011 - 11111 = Reserved	

Register 0706h GPIO 7

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1799 (0707h) GPIO 8	15	GP8_DIR	1	GPIO8 Pin Direction 0 = Output 1 = Input	
	14	GP8_PU	0	GPIO8 Pull-Up Enable 0 = Disabled 1 = Enabled	
	13	GP8_PD	1	GPIO8 Pull-Down Enable 0 = Disabled 1 = Enabled	
	10	GP8_POL	0	GPIO8 Polarity Select 0 = Non-inverted (Active High) 1 = Inverted (Active Low)	
	9	GP8_OP_CFG	0	GPIO8 Output Configuration 0 = CMOS 1 = Open Drain	
	8	GP8_DB	1	GPIO8 Input De-bounce 0 = Disabled	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1 = Enabled	
	6	GP8_LVL	0	GPIO8 level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP8_POL is set, and GP8_DIR = 1 (GPIO input), the GP8_LVL register contains the opposite logic level to the external pin.	
	4:0	GP8_FN[4:0]	0_0001	GPIO8 function. 00000 = DACDAT3 00001 = Logic level input / output 00010 = SDOUT 00011 = IRQ 00100 = Temperature sensor status 00101 = MICBIAS1 current detect 00110 = MICBIAS1 short circuit detect 00111 = MICBIAS2 current detect 01000 = MICBIAS2 short circuit detect 01001 = FLL1 Lock 01010 = FLL2 Lock 01011 = SRC1 Lock 01100 = SRC2 Lock 01101 = DRC1 (AIF1) activity detect 01110 = DRC2 (AIF1) activity detect 01111 = DRC3 (AIF2) activity detect 10000 = Write sequencer status 10001 = FIFO error indicator 10010 = OPCLK 10011 - 11111 = Reserved	

Register 0707h GPIO 8

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1800 (0708h) GPIO 9	15	GP9_DIR	1	GPIO9 Pin Direction 0 = Output 1 = Input	
	14	GP9_PU	0	GPIO9 Pull-Up Enable 0 = Disabled 1 = Enabled	
	13	GP9_PD	1	GPIO9 Pull-Down Enable 0 = Disabled 1 = Enabled	
	10	GP9_POL	0	GPIO9 Polarity Select 0 = Non-inverted (Active High) 1 = Inverted (Active Low)	
	9	GP9_OP_CFG	0	GPIO9 Output Configuration 0 = CMOS 1 = Open Drain	
	8	GP9_DB	1	GPIO9 Input De-bounce 0 = Disabled 1 = Enabled	
	6	GP9_LVL	0	GPIO9 level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP9_POL is set, and GP9_DIR = 1 (GPIO input), the GP9_LVL register contains the opposite logic level to the external pin.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4:0	GP9_FN[4:0]	0_0001	GPIO9 function. 00000 = ADCDAT3 00001 = Logic level input / output 00010 = SDOUT 00011 = IRQ 00100 = Temperature sensor status 00101 = MICBIAS1 current detect 00110 = MICBIAS1 short circuit detect 00111 = MICBIAS2 current detect 01000 = MICBIAS2 short circuit detect 01001 = FLL1 Lock 01010 = FLL2 Lock 01011 = SRC1 Lock 01100 = SRC2 Lock 01101 = DRC1 (AIF1) activity detect 01110 = DRC2 (AIF1) activity detect 01111 = DRC3 (AIF2) activity detect 10000 = Write sequencer status 10001 = FIFO error indicator 10010 = OPCLK 10011 - 11111 = Reserved	

Register 0708h GPIO 9

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1801 (0709h) GPIO 10	15	GP10_DIR	1	GPIO10 Pin Direction 0 = Output 1 = Input	
	14	GP10_PU	0	GPIO10 Pull-Up Enable 0 = Disabled 1 = Enabled	
	13	GP10_PD	1	GPIO10 Pull-Down Enable 0 = Disabled 1 = Enabled	
	10	GP10_POL	0	GPIO10 Polarity Select 0 = Non-inverted (Active High) 1 = Inverted (Active Low)	
	9	GP10_OP_CFG	0	GPIO10 Output Configuration 0 = CMOS 1 = Open Drain	
	8	GP10_DB	1	GPIO10 Input De-bounce 0 = Disabled 1 = Enabled	
	6	GP10_LVL	0	GPIO10 level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP10_POL is set, and GP10_DIR = 1 (GPIO input), the GP10_LVL register contains the opposite logic level to the external pin.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4:0	GP10_FN[4:0]	0_0001	GPIO10 function. 00000 = LRCLK3 00001 = Logic level input / output 00010 = SDOUT 00011 = IRQ 00100 = Temperature sensor status 00101 = MICBIAS1 current detect 00110 = MICBIAS1 short circuit detect 00111 = MICBIAS2 current detect 01000 = MICBIAS2 short circuit detect 01001 = FLL1 Lock 01010 = FLL2 Lock 01011 = SRC1 Lock 01100 = SRC2 Lock 01101 = DRC1 (AIF1) activity detect 01110 = DRC2 (AIF1) activity detect 01111 = DRC3 (AIF2) activity detect 10000 = Write sequencer status 10001 = FIFO error indicator 10010 = OPCLK 10011 - 11111 = Reserved	

Register 0709h GPIO 10

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1802 (070Ah) GPIO 11	15	GP11_DIR	1	GPIO11 Pin Direction 0 = Output 1 = Input	
	14	GP11_PU	0	GPIO11 Pull-Up Enable 0 = Disabled 1 = Enabled	
	13	GP11_PD	1	GPIO11 Pull-Down Enable 0 = Disabled 1 = Enabled	
	10	GP11_POL	0	GPIO11 Polarity Select 0 = Non-inverted (Active High) 1 = Inverted (Active Low)	
	9	GP11_OP_CFG	0	GPIO11 Output Configuration 0 = CMOS 1 = Open Drain	
	8	GP11_DB	1	GPIO11 Input De-bounce 0 = Disabled 1 = Enabled	
	6	GP11_LVL	0	GPIO11 level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP11_POL is set, and GP11_DIR = 1 (GPIO input), the GP11_LVL register contains the opposite logic level to the external pin.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4:0	GP11_FN[4:0]	0_0001	GPIO11 function. 00000 = BCLK3 00001 = Logic level input / output 00010 = SDOUT 00011 = IRQ 00100 = Temperature sensor status 00101 = MICBIAS1 current detect 00110 = MICBIAS1 short circuit detect 00111 = MICBIAS2 current detect 01000 = MICBIAS2 short circuit detect 01001 = FLL1 Lock 01010 = FLL2 Lock 01011 = SRC1 Lock 01100 = SRC2 Lock 01101 = DRC1 (AIF1) activity detect 01110 = DRC2 (AIF1) activity detect 01111 = DRC3 (AIF2) activity detect 10000 = Write sequencer status 10001 = FIFO error indicator 10010 = OPCLK 10011 - 11111 = Reserved	

Register 070Ah GPIO 11

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1824 (0720h) Digital Pulls	11	DMICDAT2_PU	0	DMICDAT2 Pull-Up enable 0 = Disabled 1 = Enabled	
	10	DMICDAT2_PD	0	DMICDAT2 Pull-Down enable 0 = Disabled 1 = Enabled	
	9	DMICDAT1_PU	0	DMICDAT1 Pull-Up enable 0 = Disabled 1 = Enabled	
	8	DMICDAT1_PD	0	DMICDAT1 Pull-Down enable 0 = Disabled 1 = Enabled	
	7	MCLK1_PU	0	MCLK1 pull-up resistor enable 0 = pull-up disabled 1 = pull-up enabled	
	6	MCLK1_PD	0	MCLK1 pull-down resistor enable 0 = pull-down disabled 1 = pull-down enabled	
	5	DACDAT1_PU	0	DACDAT1 pull-up resistor enable 0 = pull-up disabled 1 = pull-up enabled	
	4	DACDAT1_PD	0	DACDAT1 pull-down resistor enable 0 = pull-down disabled 1 = pull-down enabled	
	3	DACLRCLK1_PU	0	LRCLK1 pull-up resistor enable 0 = pull-up disabled 1 = pull-up enabled	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	2	DACLRCLK1_PD	0	LRCLK1 pull-down resistor enable 0 = pull-down disabled 1 = pull-down enabled	
	1	BCLK1_PU	0	BCLK1 pull-up resistor enable 0 = pull-up disabled 1 = pull-up enabled	
	0	BCLK1_PD	0	BCLK1 pull-down resistor enable 0 = pull-down disabled 1 = pull-down enabled	

Register 0720h Digital Pulls

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1840 (0730h) Interrupt Status 1	10	GP11_EINT	0	GPIO11 Interrupt status 0 = GPIO11 Interrupt not set 1 = GPIO11 Interrupt set Note: Cleared when a '1' is written.	
	9	GP10_EINT	0	GPIO10 Interrupt status 0 = GPIO10 Interrupt not set 1 = GPIO10 Interrupt set Note: Cleared when a '1' is written.	
	8	GP9_EINT	0	GPIO9 Interrupt status 0 = GPIO9 Interrupt not set 1 = GPIO9 Interrupt set Note: Cleared when a '1' is written.	
	7	GP8_EINT	0	GPIO8 Interrupt status 0 = GPIO8 Interrupt not set 1 = GPIO8 Interrupt set Note: Cleared when a '1' is written.	
	6	GP7_EINT	0	GPIO7 Interrupt status 0 = GPIO7 Interrupt not set 1 = GPIO7 Interrupt set Note: Cleared when a '1' is written.	
	5	GP6_EINT	0	GPIO6 Interrupt status 0 = GPIO6 Interrupt not set 1 = GPIO6 Interrupt set Note: Cleared when a '1' is written.	
	4	GP5_EINT	0	GPIO5 Interrupt status 0 = GPIO5 Interrupt not set 1 = GPIO5 Interrupt set Note: Cleared when a '1' is written.	
	3	GP4_EINT	0	GPIO4 Interrupt status 0 = GPIO4 Interrupt not set 1 = GPIO4 Interrupt set Note: Cleared when a '1' is written.	
	2	GP3_EINT	0	GPIO3 Interrupt status 0 = GPIO3 Interrupt not set 1 = GPIO3 Interrupt set Note: Cleared when a '1' is written.	
	1	GP2_EINT	0	GPIO2 Interrupt status 0 = GPIO2 Interrupt not set 1 = GPIO2 Interrupt set Note: Cleared when a '1' is written.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	0	GP1_EINT	0	GPIO1 Interrupt status 0 = GPIO1 Interrupt not set 1 = GPIO1 Interrupt set Note: Cleared when a '1' is written.	

Register 0730h Interrupt Status 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1841 (0731h) Interrupt Status 2	13	WSEQ_DONE_EINT	0	Write Sequencer IRQ status 0 = Write Sequencer IRQ not set 1 = Write Sequencer IRQ set Note: Cleared when a '1' is written.	
	12	FIFOS_ERR_EINT	0	Digital Core FIFO Error IRQ status 0 = FIFO Error IRQ not set 1 = FIFO Error IRQ set Note: Cleared when a '1' is written.	
	11	DRC3_ACTDET_EINT	0	DRC3 Activity Detect IRQ status 0 = DRC3 Activity Detect IRQ not set 1 = DRC3 Activity Detect IRQ set Note: Cleared when a '1' is written.	
	10	DRC2_ACTDET_EINT	0	DRC2 Activity Detect IRQ status 0 = DRC2 Activity Detect IRQ not set 1 = DRC2 Activity Detect IRQ set Note: Cleared when a '1' is written.	
	9	DRC1_ACTDET_EINT	0	DRC1 Activity Detect IRQ status 0 = DRC1 Activity Detect IRQ not set 1 = DRC1 Activity Detect IRQ set Note: Cleared when a '1' is written.	
	8	SRC2_LOCK_EINT	0	SRC2 Lock IRQ status 0 = SRC2 Lock IRQ not set 1 = SRC2 Lock IRQ set Note: Cleared when a '1' is written.	
	7	SRC1_LOCK_EINT	0	SRC1 Lock IRQ status 0 = SRC1 Lock IRQ not set 1 = SRC1 Lock IRQ set Note: Cleared when a '1' is written.	
	6	FLL2_LOCK_EINT	0	FLL2 Lock IRQ status 0 = FLL2 Lock IRQ not set 1 = FLL2 Lock IRQ set Note: Cleared when a '1' is written.	
	5	FLL1_LOCK_EINT	0	FLL1 Lock IRQ status 0 = FLL1 Lock IRQ not set 1 = FLL1 Lock IRQ set Note: Cleared when a '1' is written.	
	4	MIC2_SHRT_EINT	0	MICBIAS2 Short Circuit detect IRQ status 0 = Short Circuit current IRQ not set 1 = Short Circuit current IRQ set Note: Cleared when a '1' is written.	
	3	MIC2_DET_EINT	0	MICBIAS2 Current detect IRQ status 0 = Current detect IRQ not set 1 = Current detect IRQ set Note: Cleared when a '1' is written.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	2	MIC1_SHRT_EINT	0	MICBIAS1 Short Circuit detect IRQ status 0 = Short Circuit current IRQ not set 1 = Short Circuit current IRQ set Note: Cleared when a '1' is written.	
	1	MIC1_DET_EINT	0	MICBIAS1 Current detect IRQ status 0 = Current detect IRQ not set 1 = Current detect IRQ set Note: Cleared when a '1' is written.	
	0	TEMP_SHUT_EINT	0	Shutdown Temperature IRQ status 0 = Shutdown Temperature IRQ not set 1 = Shutdown Temperature IRQ set Note: Cleared when a '1' is written.	

Register 0731h Interrupt Status 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1848 (0738h) Interrupt Status 1 Mask	10	IM_GP11_EINT	1	Interrupt mask for GPIO11 0 = Not masked 1 = Masked	
	9	IM_GP10_EINT	1	Interrupt mask for GPIO10 0 = Not masked 1 = Masked	
	8	IM_GP9_EINT	1	Interrupt mask for GPIO9 0 = Not masked 1 = Masked	
	7	IM_GP8_EINT	1	Interrupt mask for GPIO8 0 = Not masked 1 = Masked	
	6	IM_GP7_EINT	1	Interrupt mask for GPIO7 0 = Not masked 1 = Masked	
	5	IM_GP6_EINT	1	Interrupt mask for GPIO6 0 = Not masked 1 = Masked	
	4	IM_GP5_EINT	1	Interrupt mask for GPIO5 0 = Not masked 1 = Masked	
	3	IM_GP4_EINT	1	Interrupt mask for GPIO4 0 = Not masked 1 = Masked	
	2	IM_GP3_EINT	1	Interrupt mask for GPIO3 0 = Not masked 1 = Masked	
	1	IM_GP2_EINT	1	Interrupt mask for GPIO2 0 = Not masked 1 = Masked	
	0	IM_GP1_EINT	1	Interrupt mask for GPIO1 0 = Not masked 1 = Masked	

Register 0738h Interrupt Status 1 Mask

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1849 (0739h) Interrupt Status 2 Mask	13	IM_WSEQ_DONE_EINT	1	Interrupt mask for Write Sequencer 0 = Not masked 1 = Masked	
	12	IM_FIFOS_ERR_EINT	1	Interrupt mask for Digital Core FIFO Error 0 = Not masked 1 = Masked	
	11	IM_DRC3_ACTDET_EINT	1	Interrupt mask for DRC3 Activity Detect 0 = Not masked 1 = Masked	
	10	IM_DRC2_ACTDET_EINT	1	Interrupt mask for DRC2 Activity Detect 0 = Not masked 1 = Masked	
	9	IM_DRC1_ACTDET_EINT	1	Interrupt mask for DRC1 Activity Detect 0 = Not masked 1 = Masked	
	8	IM_SRC2_LOCK_EINT	1	Interrupt mask for SRC2 Lock 0 = Not masked 1 = Masked	
	7	IM_SRC1_LOCK_EINT	1	Interrupt mask for SRC1 Lock 0 = Not masked 1 = Masked	
	6	IM_FLL2_LOCK_EINT	1	Interrupt mask for FLL2 Lock 0 = Not masked 1 = Masked	
	5	IM_FLL1_LOCK_EINT	1	Interrupt mask for FLL1 Lock 0 = Not masked 1 = Masked	
	4	IM_MIC2_SHRT_EINT	1	Interrupt mask for MICBIAS2 Short Circuit detect 0 = Not masked 1 = Masked	
	3	IM_MIC2_DET_EINT	1	Interrupt mask for MICBIAS2 Current detect 0 = Not masked 1 = Masked	
	2	IM_MIC1_SHRT_EINT	1	Interrupt mask for MICBIAS1 Short Circuit detect 0 = Not masked 1 = Masked	
	1	IM_MIC1_DET_EINT	1	Interrupt mask for MICBIAS1 Current detect 0 = Not masked 1 = Masked	
	0	IM_TEMP_SHUT_EINT	1	Interrupt mask for Shutdown Temperature 0 = Not masked 1 = Masked	

Register 0739h Interrupt Status 2 Mask

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1856 (0740h) Interrupt Control	0	IRQ_POL	0	Interrupt (IRQ) polarity 0 = active high 1 = active low	

Register 0740h Interrupt Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1864 (0748h) IRQ Debounce	4	MIC2_SHRT_DB	1	MICBIAS2 Short Circuit de-bounce 0 = disabled 1 = enabled	
	3	MIC2_DET_DB	1	MICBIAS2 Current Detect de-bounce 0 = disabled 1 = enabled	
	2	MIC1_SHRT_DB	1	MICBIAS1 Short Circuit de-bounce 0 = disabled 1 = enabled	
	1	MIC1_DET_DB	1	MICBIAS1 Current Detect de-bounce 0 = disabled 1 = enabled	
	0	TEMP_SHUT_DB	1	Thermal shutdown de-bounce 0 = disabled 1 = enabled	

Register 0748h IRQ Debounce

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1865 (0749h) IRQ Polarity	13	WSEQ_DONE_POL	0	Write Sequencer polarity 0 = active high (asserted when Control Sequence is Busy) 1 = active low	
	12	FIFOS_ERR_POL	0	FIFO Error polarity 0 = active high (asserted under FIFO Error condition) 1 = active low	
	11	DRC3_ACTDET_POL	0	DRC3 Activity Detect polarity 0 = active high (asserted when DRC3 activity is detected) 1 = active low	
	10	DRC2_ACTDET_POL	0	DRC2 Activity Detect polarity 0 = active high (asserted when DRC2 activity is detected) 1 = active low	
	9	DRC1_ACTDET_POL	0	DRC1 Activity Detect polarity 0 = active high (asserted when DRC1 activity is detected) 1 = active low	
	8	SRC2_LOCK_POL	0	SRC2 Lock polarity 0 = active high (asserted when SRC2 locked) 1 = active low	
	7	SRC1_LOCK_POL	0	SRC1 Lock polarity 0 = active high (asserted when SRC1 locked) 1 = active low	
	6	FLL2_LOCK_POL	0	FLL2 Lock polarity 0 = active high (asserted when FLL2 locked) 1 = active low	
	5	FLL1_LOCK_POL	0	FLL1 Lock polarity 0 = active high (asserted when FLL1 locked) 1 = active low	
	4	MIC2_SHRT_POL	0	MICBIAS2 Short Circuit polarity 0 = active high (asserted when MICD_SCTHR is exceeded) 1 = active low	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	3	MIC2_DET_POL	0	MICBIAS2 Current Detect polarity 0 = active high (asserted when MICD_THR is exceeded) 1 = active low	
	2	MIC1_SHRT_POL	0	MICBIAS1 Short Circuit polarity 0 = active high (asserted when MICD_SCTHR is exceeded) 1 = active low	
	1	MIC1_DET_POL	0	MICBIAS1 Current Detect polarity 0 = active high (asserted when MICD_THR is exceeded) 1 = active low	
	0	TEMP_SHUT_POL	0	Thermal shutdown interrupt polarity 0 = active high (asserted when temperature threshold is exceeded) 1 = active low	

Register 0749h IRQ Polarity

DIGITAL FILTER CHARACTERISTICS

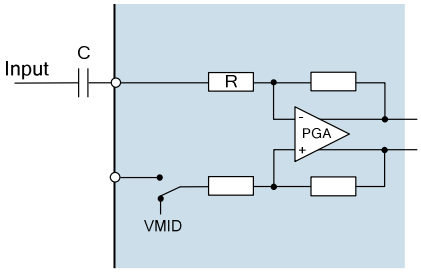
Data to follow

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

AUDIO INPUT PATHS

The WM8994 provides 8 analogue audio inputs. Each of these inputs is referenced to the internal DC reference, VMID. A DC blocking capacitor is required for each input pin used in the target application. The choice of capacitor is determined by the filter that is formed between that capacitor and the input impedance of the input pin. The circuit is illustrated in Figure 77.



$$Fc = \frac{1}{2\pi RC}$$

Fc = high pass 3dB cut-off frequency

Figure 77 Audio Input Path DC Blocking Capacitor

If the input impedance is known, and the cut-off frequency is known, then the minimum capacitor value may be derived easily. However, it can be seen from the representation in Figure 77 that the input impedance is not fixed in all applications but can vary with gain and boost amplifier settings. The choice of capacitor for a 20Hz cut-off frequency is shown in Table 139 for different input impedance conditions. The applicable input impedance can be found in the "Electrical Characteristics" section of this datasheet.

INPUT IMPEDANCE	MINIMUM CAPACITANCE FOR 20HZ PASS BAND
2kΩ	4 µF
15kΩ	0.5 µF
30kΩ	0.27 µF
60kΩ	0.13 µF

Table 139 Audio Input DC Blocking Capacitors

Using the figures in Table 139, it follows that a 1µF capacitance for all input connections will give good results in most cases. Tantalum electrolytic capacitors are particularly suitable as they offer high stability in a small package size.

Ceramic equivalents are a cost effective alternative to the superior tantalum packages, but care must be taken to ensure the desired capacitance is maintained at the AVDD1 operating voltage. Also, ceramic capacitors may show microphonic effects, where vibrations and mechanical conditions give rise to electrical signals. This is particularly problematic for microphone input paths where a large signal gain is required.

A single capacitor is required for a line input or single-ended microphone connection. In the case of a differential microphone connection, a DC blocking capacitor is required on both input pins.

HEADPHONE OUTPUT PATH

The headphone output on WM8994 is ground referenced and therefore does not require the large, expensive capacitors necessary for VMID reference solutions. For best audio performance, it is recommended to connect a zobel network to the audio output pins. This network should comprise of a 100nF capacitor and 20ohm resistor in series with each other (see "Analogue Outputs" section).

These components have the effect of dampening high frequency oscillations or instabilities that can arise outside the audio band under certain conditions. Possible sources of these instabilities include the inductive load of a headphone coil or an active load in the form of an external line amplifier.

EARPIECE DRIVER OUTPUT PATH

The earpiece driver on HPOUT2P and HPOUTN is designed as a 32ohm BTL speaker driver. The outputs are referenced to the internal DC reference VMID, but direct connection to the speaker is possible because of the BTL configuration. There is no requirement for DC blocking capacitors.

LINE OUTPUT PATHS

The WM8994 provides four line outputs (LINEOUT1P, LINEOUT1N, LINEOUT2P and LINEOUT2N). Each of these outputs is referenced to the internal DC reference, VMID. In any the case where a line output is used in a single-ended configuration (i.e. referenced to AGND), a DC blocking capacitor will be required in order to remove the DC bias. In the case where a pair of line outputs is configured as a BTL differential pair, then the DC blocking capacitor should be omitted.

The choice of capacitor is determined from the filter that is formed between the capacitor and the load impedance – see Figure 78.

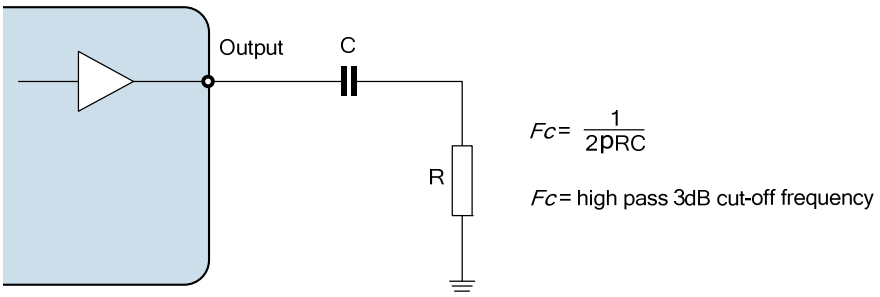


Figure 78 Line Output Path Components

LOAD IMPEDANCE	MINIMUM CAPACITANCE FOR 20HZ PASS BAND
10kΩ	0.8 µF
47kΩ	0.17 µF

Table 140 Line Output Frequency Cut-Off

Using the figures in Table 140, it follows that that a 1µF capacitance would be a suitable choice for a line load. Tantalum electrolytic capacitors are again particularly suitable but ceramic equivalents are a cost effective alternative. Care must be taken to ensure the desired capacitance is maintained at the appropriate operating voltage.

POWER SUPPLY DECOUPLING

Electrical coupling exists particularly in digital logic systems where switching in one sub-system causes fluctuations on the power supply. This effect occurs because the inductance of the power supply acts in opposition to the changes in current flow that are caused by the logic switching. The resultant variations (or 'spikes') in the power supply voltage can cause malfunctions and unintentional behavior in other components. A decoupling (or 'bypass') capacitor can be used as an energy storage component which will provide power to the decoupled circuit for the duration of these power supply variations, protecting it from malfunctions that could otherwise arise.

Coupling also occurs in a lower frequency form when ripple is present on the power supply rail caused by changes in the load current or by limitations of the power supply regulation method. In audio components such as the WM8994, these variations can alter the performance of the signal path, leading to degradation in signal quality. A decoupling (or 'bypass') capacitor can be used to

filter these effects, by presenting the ripple voltage with a low impedance path that does not affect the circuit to be decoupled.

These coupling effects are addressed by placing a capacitor between the supply rail and the corresponding ground reference. In the case of systems comprising multiple power supply rails, decoupling should be provided on each rail.

The recommended power supply decoupling capacitors for WM8994 are listed below in Table 141.

POWER SUPPLY	DECOUPLING CAPACITOR
LDO1VDD, LDO2VDD, DBVDD, AVDD2	0.1µF ceramic
AVDD1, DCVDD, SPKVDD1, SPKVDD2	0.1µF ceramic (see Note)
CPVDD	4.7µF ceramic
VMIDC	4.7µF ceramic

Table 141 Power Supply Decoupling Capacitors

Note: 0.1µF is required with 4.7µF a guide to the total required power rail capacitance, including that at the regulator output.

All decoupling capacitors should be placed as close as possible to the WM8994 device. The connection between AGND, the AVDD1 decoupling capacitor and the main system ground should be made at a single point as close as possible to the AGND ball of the WM8994.

The VMID capacitor is not, technically, a decoupling capacitor. However, it does serve a similar purpose in filtering noise on the VMID reference. The connection between AGND, the VMID decoupling capacitor and the main system ground should be made at a single point as close as possible to the AGND ball of the WM8994.

Due to the wide tolerance of many types of ceramic capacitors, care must be taken to ensure that the selected components provide the required capacitance across the required temperature and voltage ranges in the intended application. For most application the use of ceramic capacitors with capacitor dielectric X5R is recommended.

MICROPHONE BIAS CIRCUIT

The WM8994 is designed to interface easily with up to four microphones. These may be connected in single-ended or differential configurations. The single-ended method allows greater capability for the connection of multiple audio sources simultaneously, whilst the differential method provides better performance due to its rejection of common-mode noise.

In either configuration, the microphone requires a bias current (electret condenser microphones) or voltage supply (silicon microphones), which can be provided by MICBIAS1 or MICBIAS2. These are generated by identical output-compensated amplifiers, which require an external capacitor in order to guarantee accuracy and stability. The recommended capacitance is 4.7µF, although it may be possible to reduce this to 1µF if the analogue supply (AVDD1) is not too noisy. A ceramic type is a suitable choice here, providing that care is taken to choose a component that exhibits this capacitance at the intended MICBIAS voltage.

Note that the MICBIAS voltage may be adjusted using register control to suit the requirements of the microphone. Also note the WM8994 supports a maximum current of 2.4mA per MICBIAS pin. If more than one microphone is connected to a single MICBIAS pin, the combined current of these must not exceed 2.4mA.

A current-limiting resistor is also required when using an electret condenser microphone (ECM). The resistance should be chosen according to the minimum operating impedance of the microphone and MICBIAS voltage so that the maximum bias current of the WM8994 is not exceeded. Wolfson recommends a 2.2kΩ current limiting resistor as it provides compatibility with a wide range of microphone models.

Figure 79 illustrates the recommended single-ended and differential microphone connections for the WM8994.

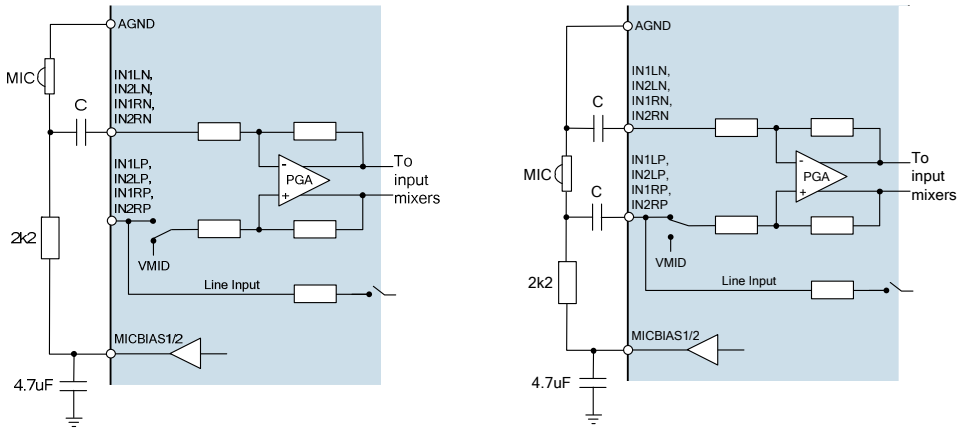


Figure 79 Single-Ended and Differential Microphone Connections

CLASS D SPEAKER CONNECTIONS

The WM8994 incorporates two Class D/AB 1W speaker drivers. By default, the speaker drivers operate in Class D mode, which offers high amplifier efficiency at large signal levels. As the Class D output is a pulse width modulated signal, the choice of speakers and tracking of signals is critical for ensuring good performance and reducing EMI in this mode.

The efficiency of the speaker drivers is affected by the series resistance between the WM8994 and the speaker (e.g. PCB track loss and inductor ESR) as shown in Figure 80. This resistance should be as low as possible to maximise efficiency.

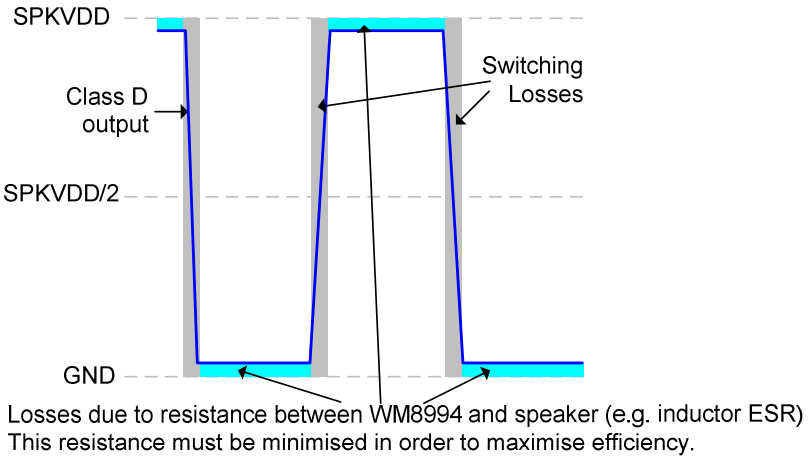


Figure 80 Speaker Connection Losses

The Class D output requires external filtering in order to recreate the audio signal. This may be implemented using a 2nd order LC or 1st order RC filter, or else may be achieved by using a loudspeaker whose internal inductance provides the required filter response. An LC or RC filter should be used if the loudspeaker characteristics are unknown or unsuitable, or if the length of the loudspeaker connection is likely to lead to EMI problems.

In applications where it is necessary to provide Class D filter components, a 2nd order LC filter is the recommended solution as it provides more attenuation at higher frequencies and minimises power dissipated in the filter when compared to a first order RC filter (lower ESR). This maximises both rejection of unwanted switching frequencies and overall speaker efficiency. A suitable implementation is illustrated in Figure 81.

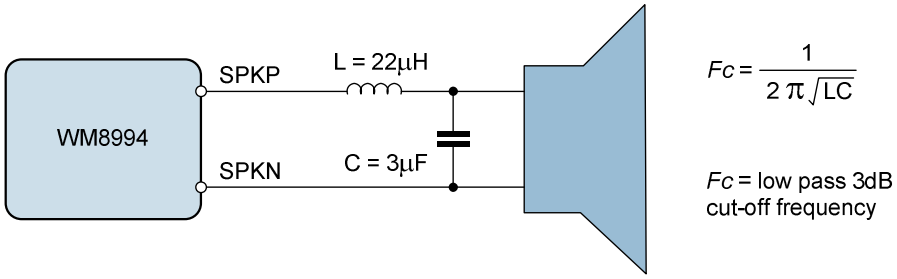


Figure 81 Class D Output Filter Components

A simple equivalent circuit of a loudspeaker consists of a serially connected resistor and inductor, as shown in Figure 82. This circuit provides a low pass filter for the speaker output. If the loudspeaker characteristics are suitable, then the loudspeaker itself can be used in place of the filter components described earlier. This is known as 'filterless' operation.

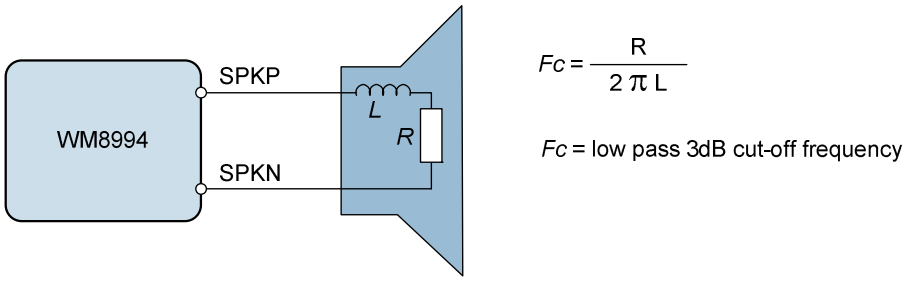


Figure 82 Speaker Equivalent Circuit for Filterless Operation

For filterless Class D operation, it is important to ensure that a speaker with suitable inductance is chosen. For example, if we know the speaker impedance is 8Ω and the desired cut-off frequency is 20kHz, then the optimum speaker inductance may be calculated as:

$$L = \frac{R}{2\pi Fc} = \frac{8\Omega}{2\pi * 20kHz} = 64\mu H$$

8Ω loudspeakers typically have an inductance in the range 20µH to 100µH, however, it should be noted that a loudspeaker inductance will not be constant across the relevant frequencies for Class D operation (up to and beyond the Class D switching frequency). Care should be taken to ensure that the cut-off frequency of the loudspeaker's filtering is low enough to suppress the high frequency energy of the Class D switching and, in so doing, to prevent speaker damage. The Class D outputs of the WM8994 operate at much higher frequencies than is recommended for most speakers and it must be ensured that the cut-off frequency is low enough to protect the speaker.

RECOMMENDED EXTERNAL COMPONENTS DIAGRAM

Figure 83 and Figure 84 below provide a summary of recommended external components for WM8994. Note that these diagrams do not include any components that are specific to the end application e.g. they do not include filtering on the speaker outputs (assume filterless class D operation), RF decoupling, or RF filtering for pins which connect to the external world i.e. headphone or speaker outputs.

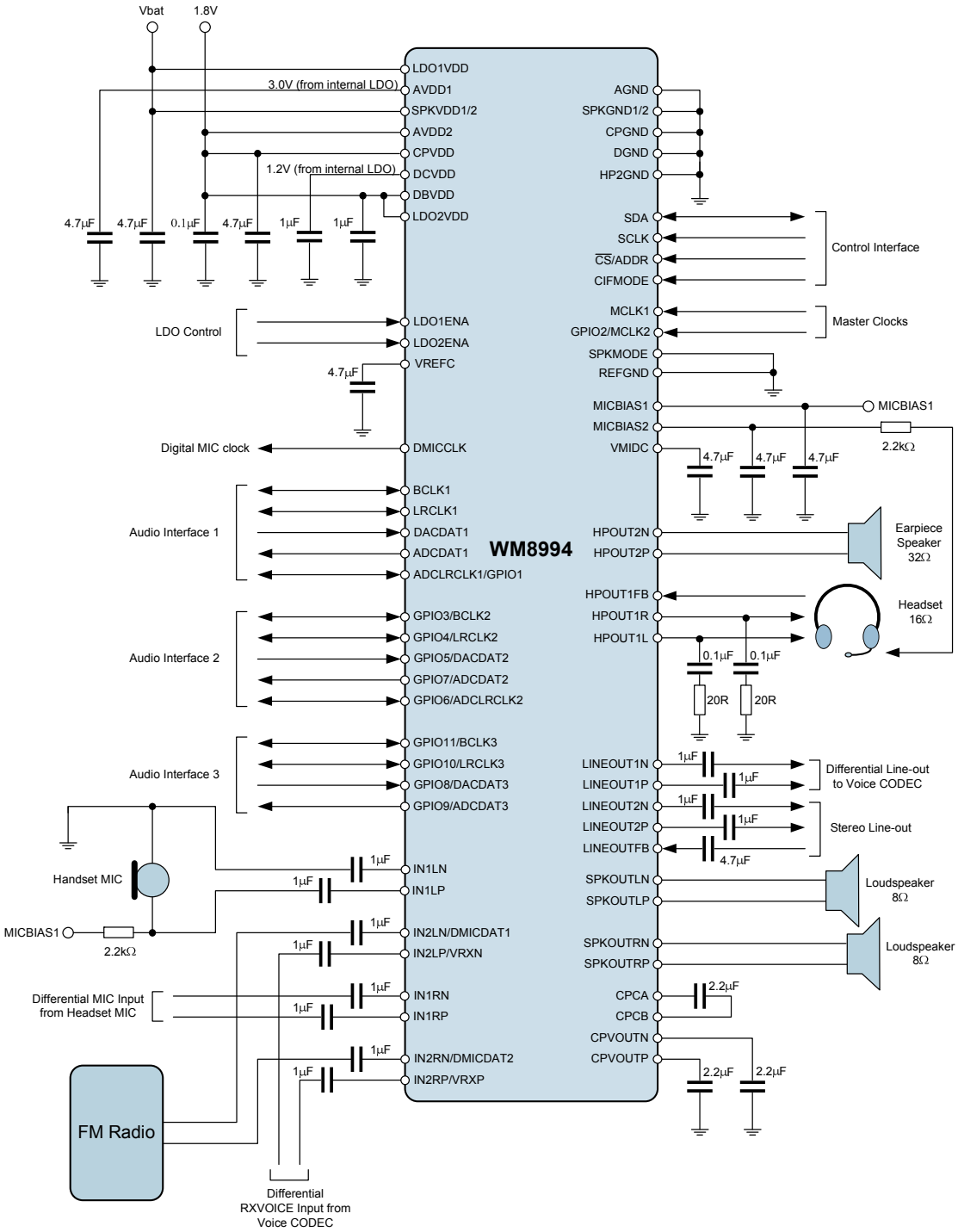


Figure 83 Recommended External Components Diagram – Analogue Hub Architecture

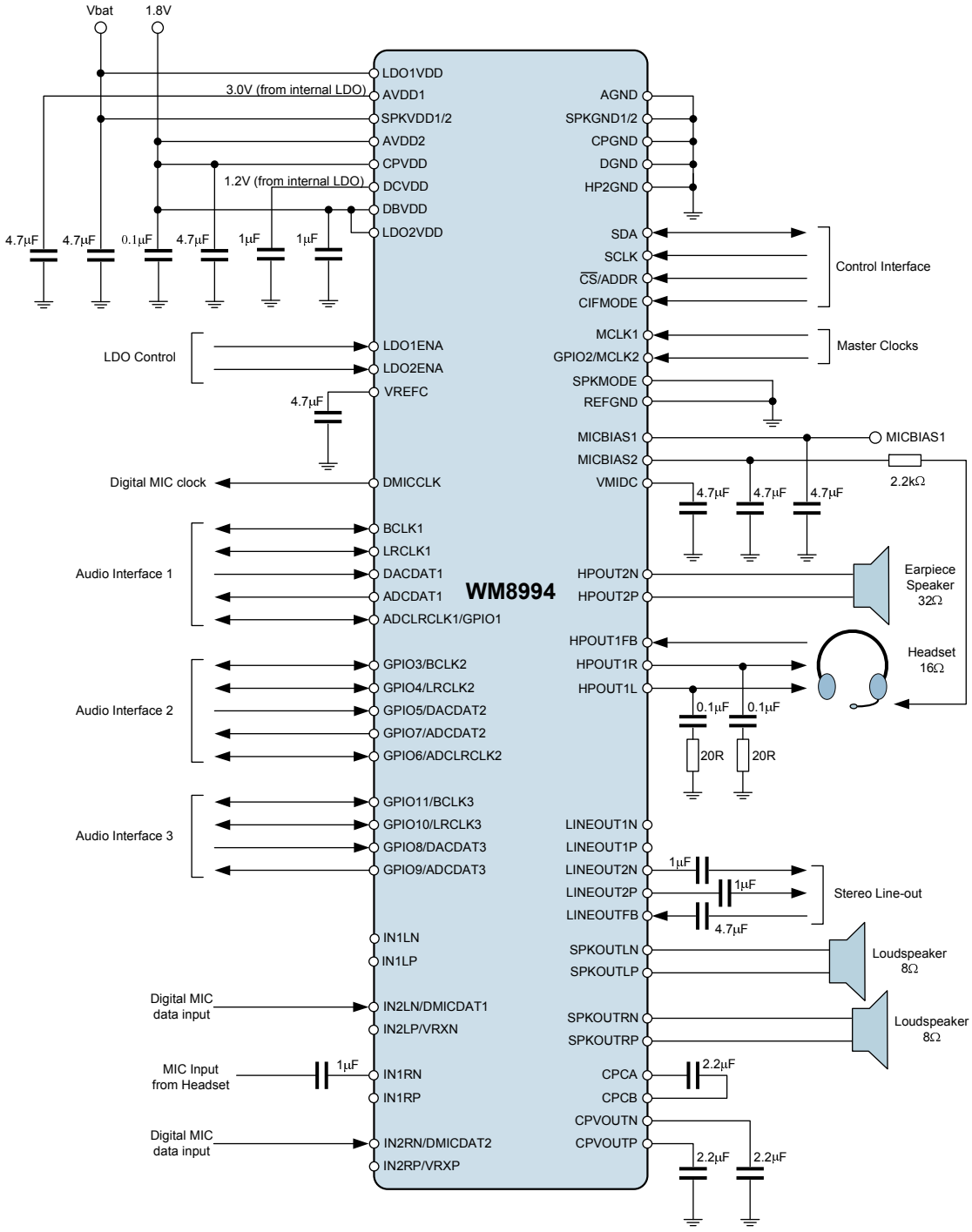


Figure 84 Recommended External Components Diagram – Digital Hub Architecture

PCB LAYOUT CONSIDERATIONS

Poor PCB layout will degrade the performance and be a contributory factor in EMI, ground bounce and resistive voltage losses. All external components should be placed as close to the WM8994 device as possible, with current loop areas kept as small as possible. Specific factors relating to Class D loudspeaker connection are detailed below.

CLASS D LOUDSPEAKER CONNECTION

Long, exposed PCB tracks or connection wires will emit EMI. The distance between the WM8994 and the loudspeaker should therefore be kept as short as possible. Where speakers are connected to the PCB via a cable form, it is recommended that a shielded twisted pair cable is used. The shield should be connected to the main system, with care taken to ensure ground loops are avoided.

Further reduction in EMI can be achieved using PCB ground (or VDD) planes and also by using passive LC components to filter the Class D switching waveform. When passive filtering is used, low ESR components should be chosen in order to minimise the series resistance between the WM8994 and the speaker, maximising the power efficiency.

LC passive filtering will usually be effective at reducing EMI at frequencies up to around 30MHz. To reduce emissions at higher frequencies, ferrite beads can also be used. These should be positioned as close to the device as possible.

These techniques for EMI reduction are illustrated in Figure 85.

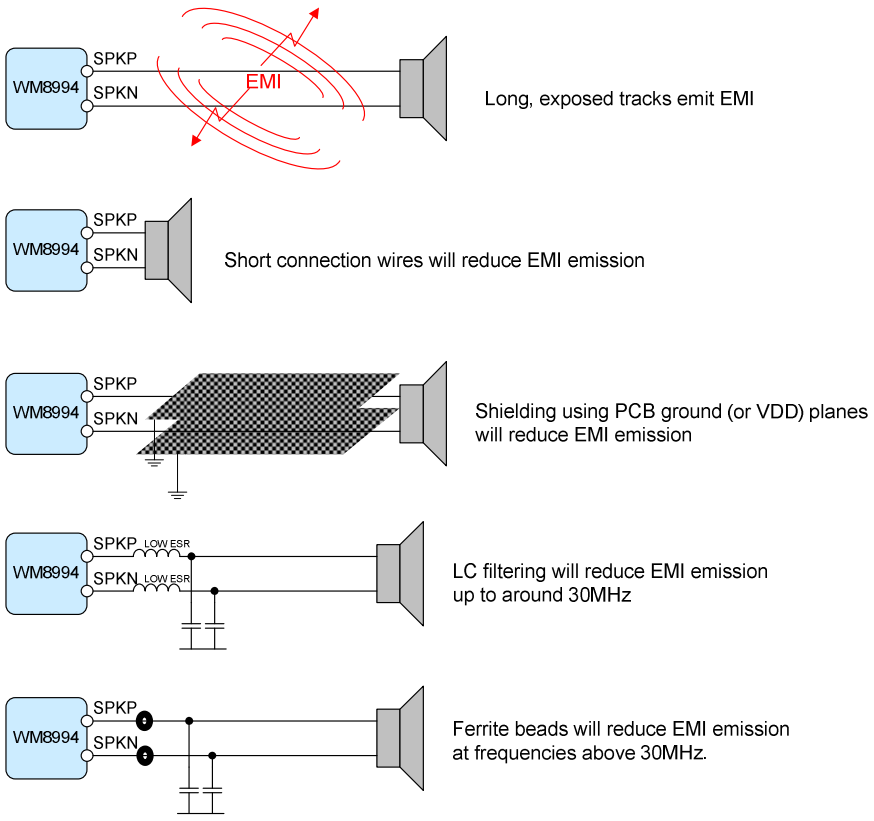
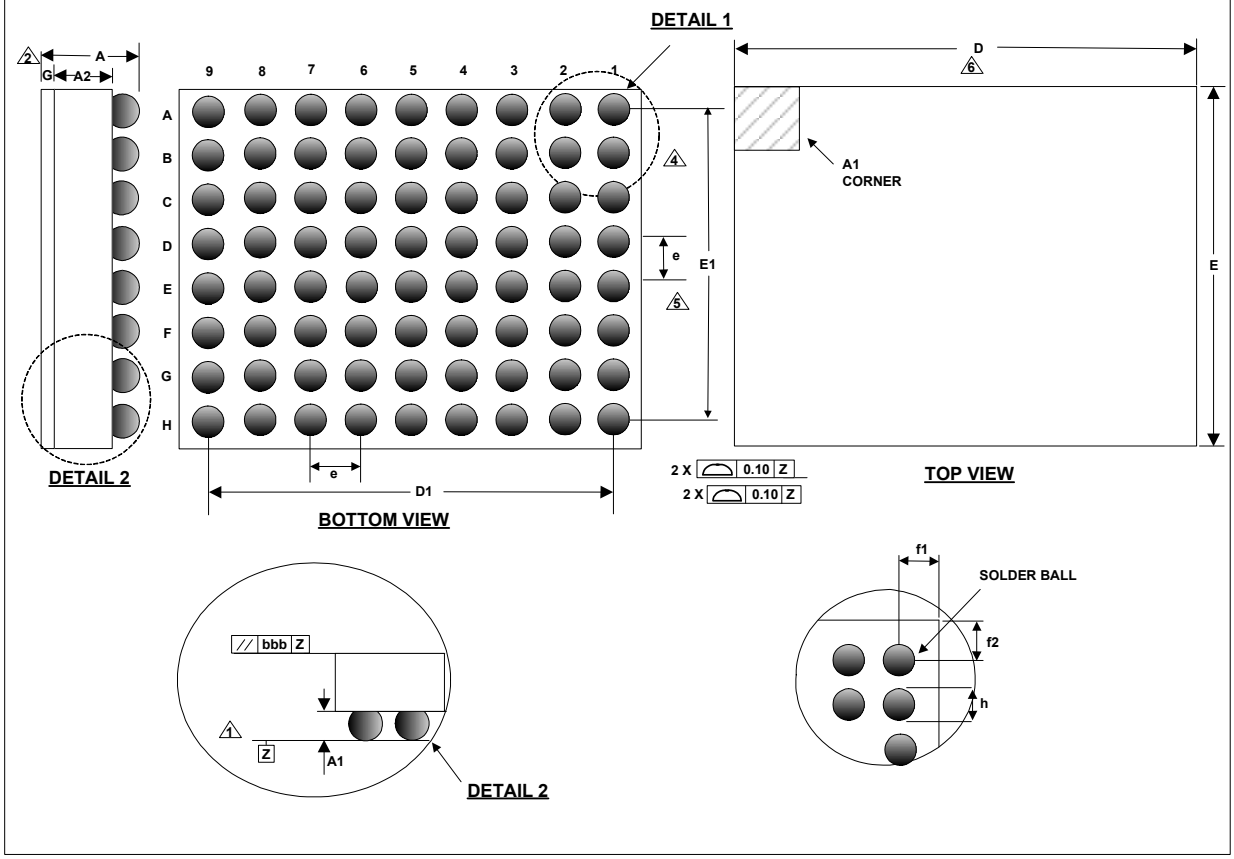


Figure 85 EMI Reduction Techniques

PACKAGE DIMENSIONS

B: 72 BALL W-CSP PACKAGE 4.511 x 4.023 x 0.7 mm BODY, 0.50 mm BALL PITCH **DM068.A**



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.615	0.7	0.785	
A1	0.219	0.244	0.269	
A2	0.361	0.386	0.411	
D		4.511 BSC		
D1		4.00 BSC		
E		4.023 BSC		
E1		3.50 BSC		
e		0.50 BSC		5
f1	0.236 BSC			
f2	0.242 BSC			
g	0.035	0.070	0.105	
h		0.314 BSC		

NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. THIS DIMENSION INCLUDES STAND-OFF HEIGHT 'A1' AND BACKSIDE COATING.
3. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
4. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
5. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
6. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
7. FOLLOWS JEDEC DESIGN GUIDE MO-211-C.

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