DIGITAL CIRCUITS LAB

EXP-8 Clock_LED_Divider

In this lab, we used dataflow & behavioural modeling.

October 10,2024

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Pen-Paper Design:

Clock Source Frequency	FPGA Pin no.
1 Hz CLK	55
50 MHz CLK	26
Ext CLK	27
10 MHz CLK	29

Figure 2: Pin-mapping for on-board Clock Sources

Switch	FPGA Pin no.	LED	FPGA Pin no.
SW 8	47	LED 8	60
SW 7	46	LED 7	59
SW 6	45	LED 6	58
SW 5	44	LED 5	57
SW 4	43	LED 4	56
SW 3	41	LED 3	54
SW 2	39	LED 2	52
SW 1	38	LED 1	50

Figure 3: Pin-mapping for on-board Switches and LED's

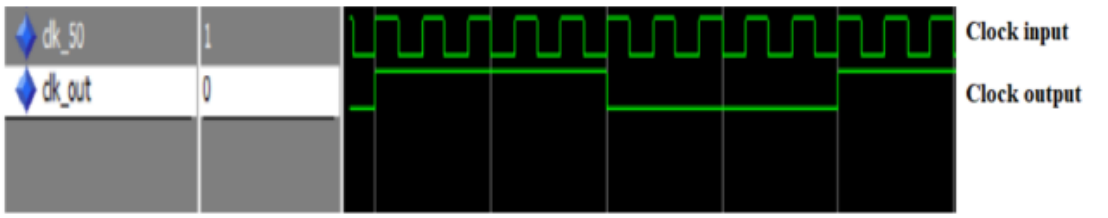
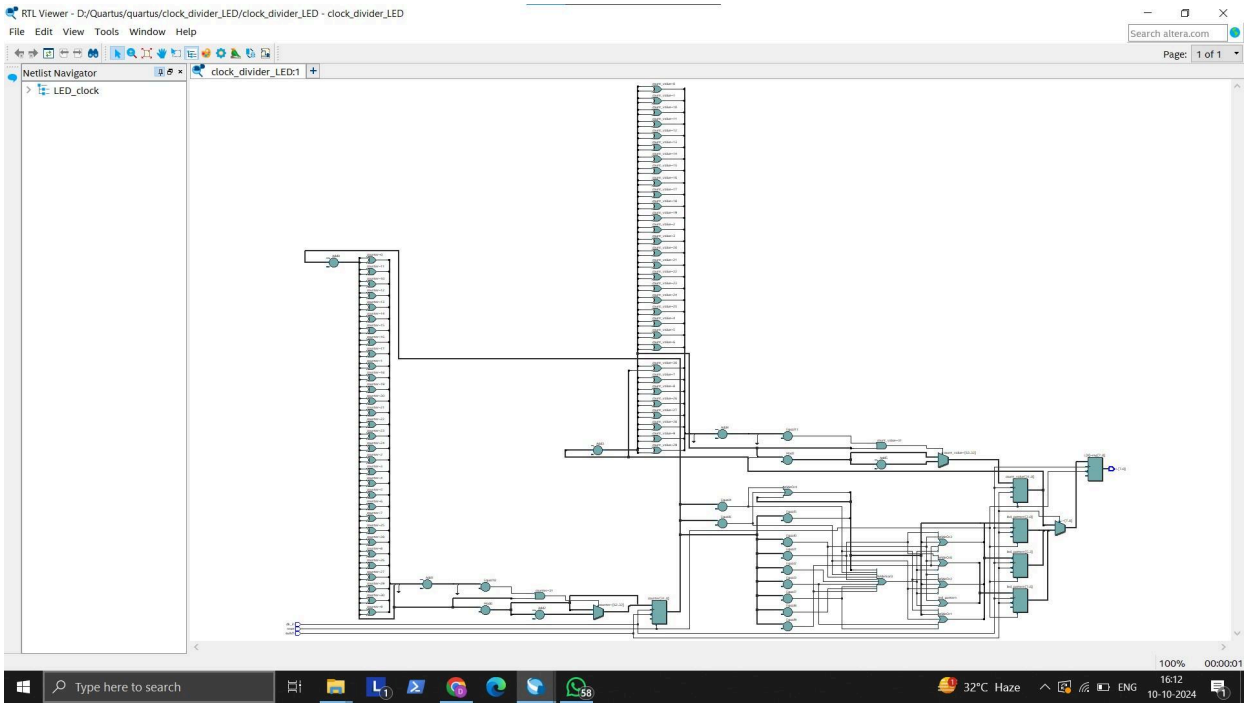
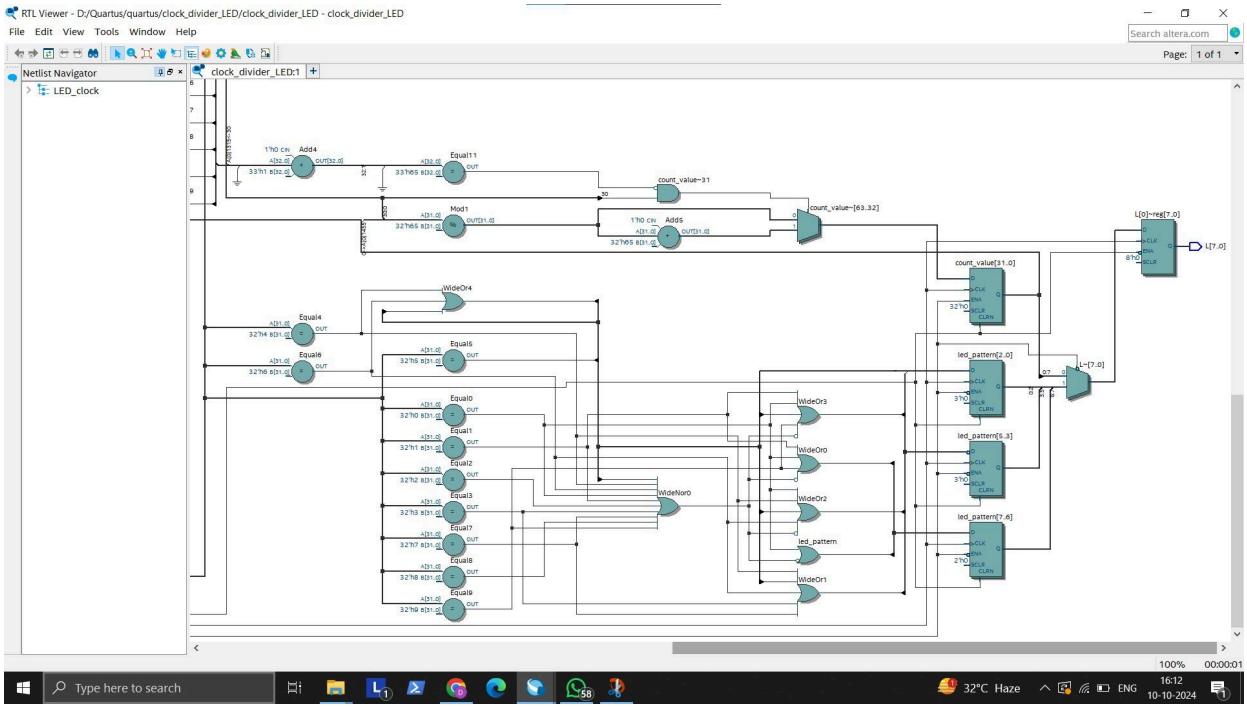
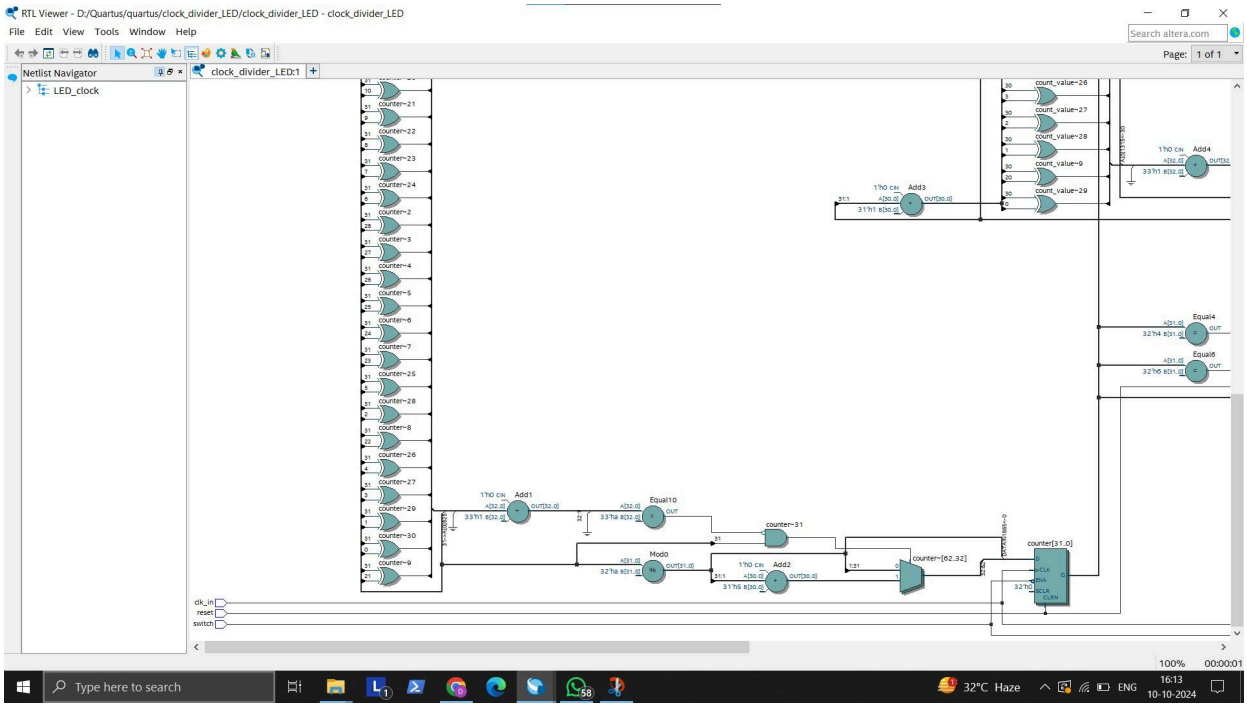


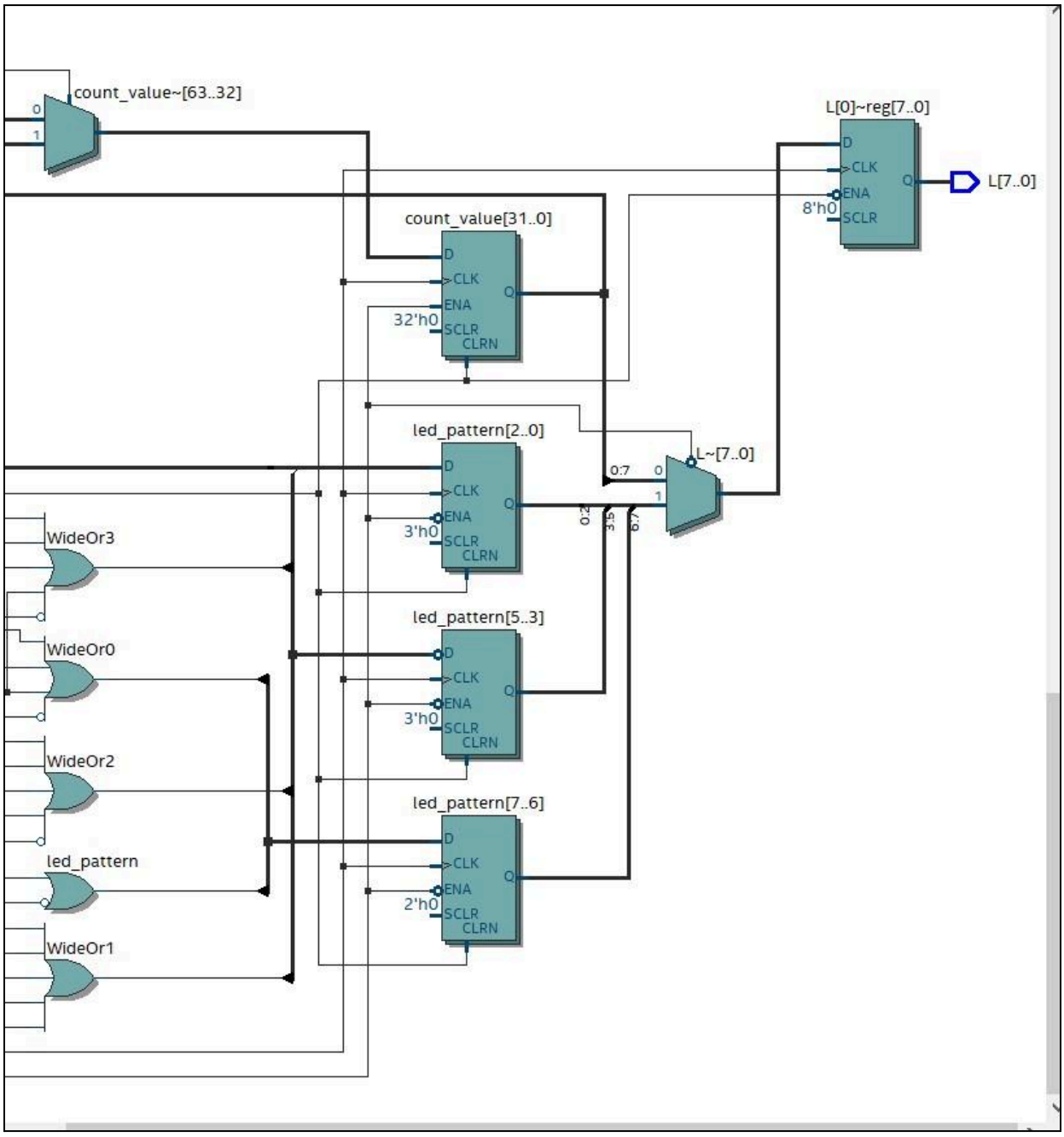
Figure 1: Waveform

Netlists & Simulation Wave:

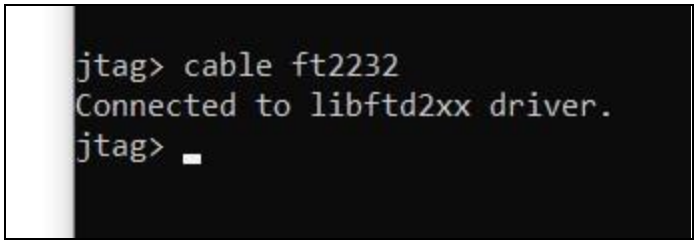



RTL Viewer - D:/Quartus/quartus/clock_divider_LED/clock_divider_LED - clock_divider_LED
File Edit View Tools Window Help
Search altera.com
Page: 1 of 1
Netlist Navigator
LED_clock
clock_divider_LED:1
Add4
Equal11
count_value~31
Mod1
Add5
count_value~[63..32]
L[0]~reg[7..0]
L[7..0]
count_value[31..0]
WideOr4
Equal4
Equal5
Equal6
Equal0
Equal1
Equal2
Equal3
Equal7
Equal8
Equal9
WideNor0
WideOr3
WideOr0
WideOr2
led_pattern
WideOr1
led_pattern[2..0]
led_pattern[5..3]
led_pattern[7..6]
L~[7..0]
100%
00:00:01
Type here to search
32°C Haze
ENG
16:12
10-10-2024


RTL Viewer - D:/Quartus/quartus/clock_divider_LED/clock_divider_LED - clock_divider_LED
File Edit View Tools Window Help
Search altera.com
Page: 1 of 1
Netlist Navigator
LED_clock
clock_divider_LED:1
counter~21
counter~22
counter~23
counter~24
counter~2
counter~3
counter~4
counter~5
counter~6
counter~7
counter~25
counter~28
counter~8
counter~26
counter~27
counter~29
counter~30
counter~9
Add1
Equal10
counter~31
Mod0
Add2
counter~[62..32]
counter[31..0]
count_value~26
count_value~27
count_value~28
count_value~9
count_value~29
Add3
Add4
Equal4
Equal6
clk_in
reset
switch
100%
00:00:01
Type here to search
32°C Haze
ENG
16:13
10-10-2024

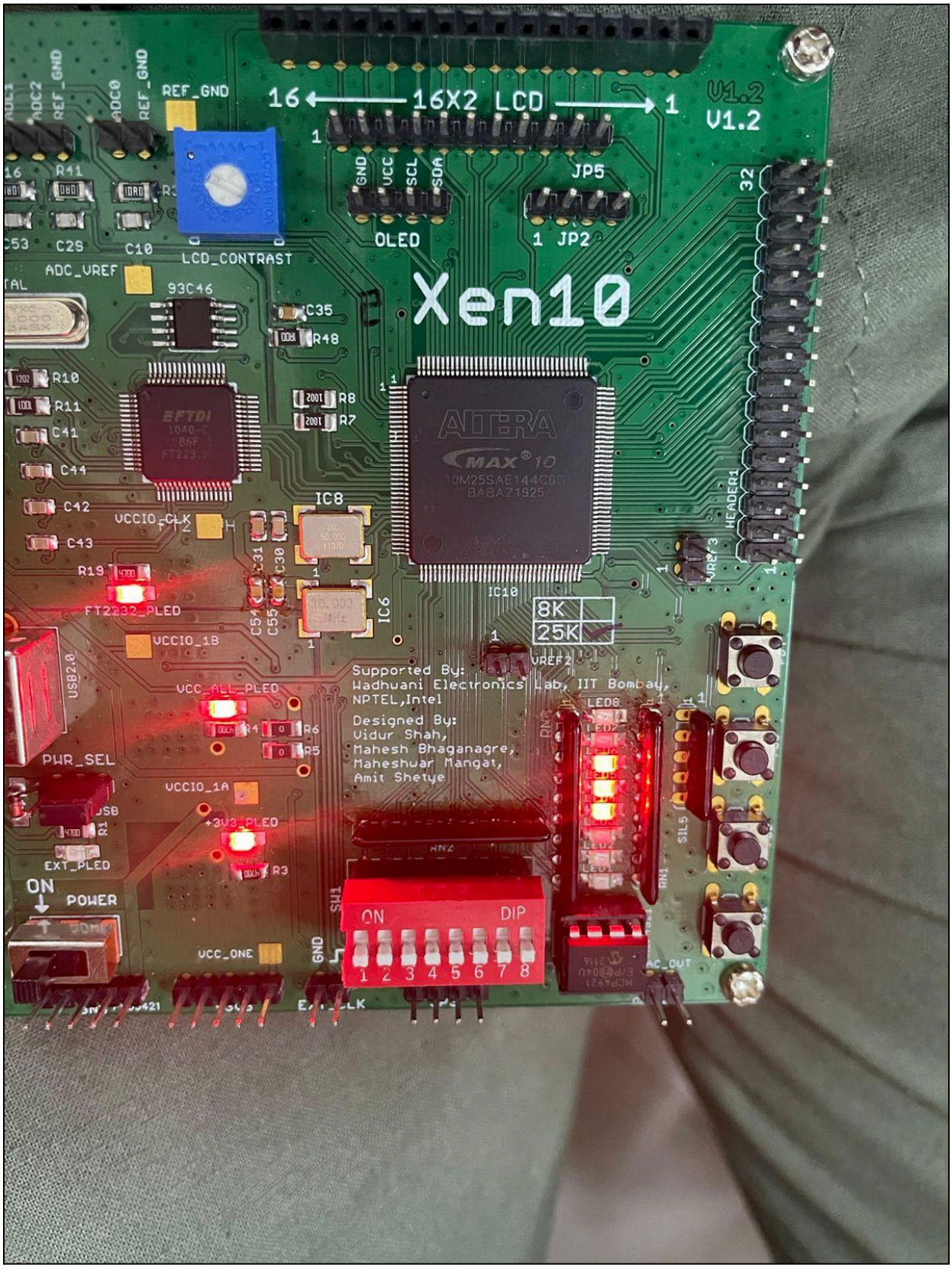


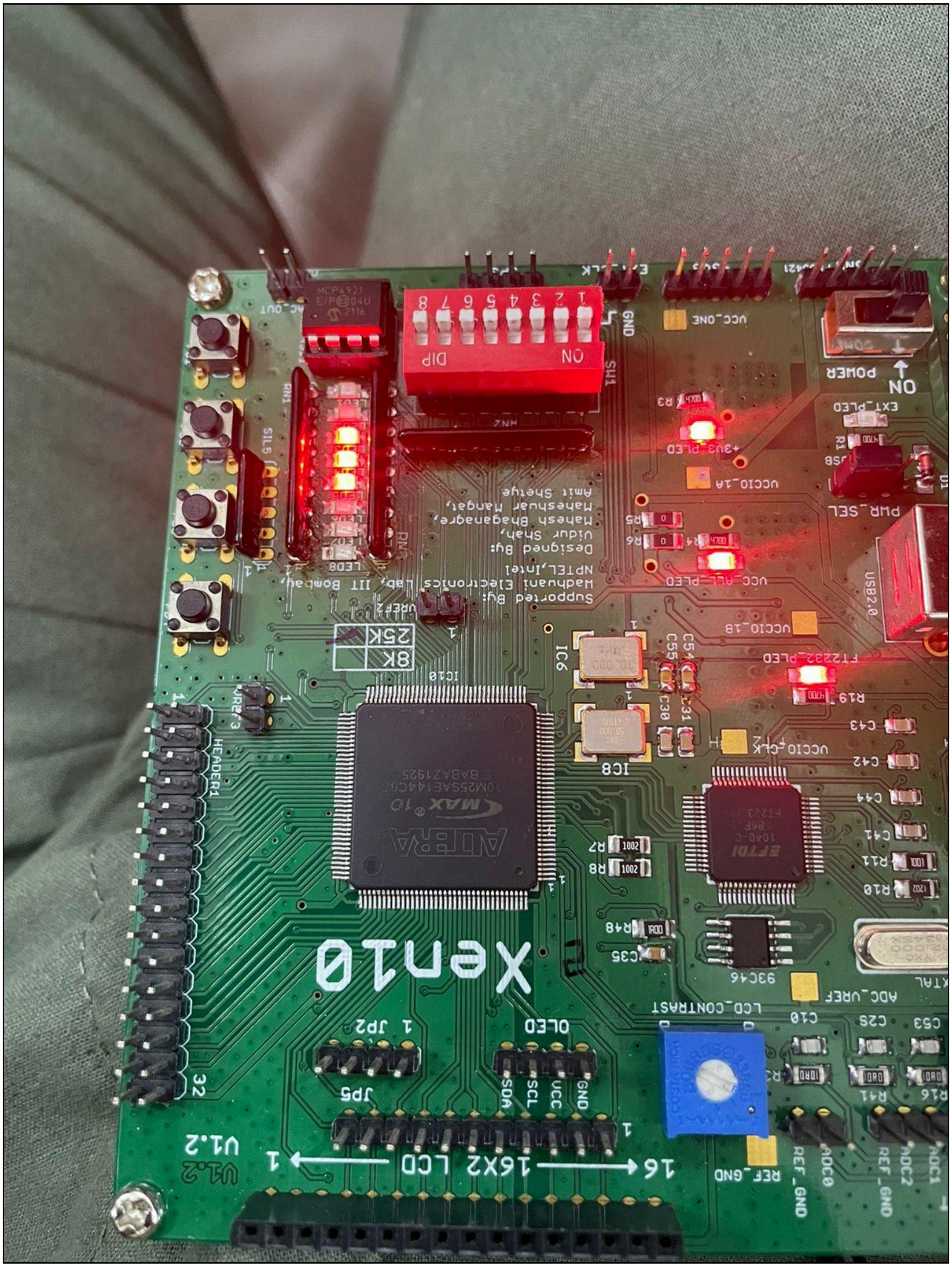
Testing Terminal:



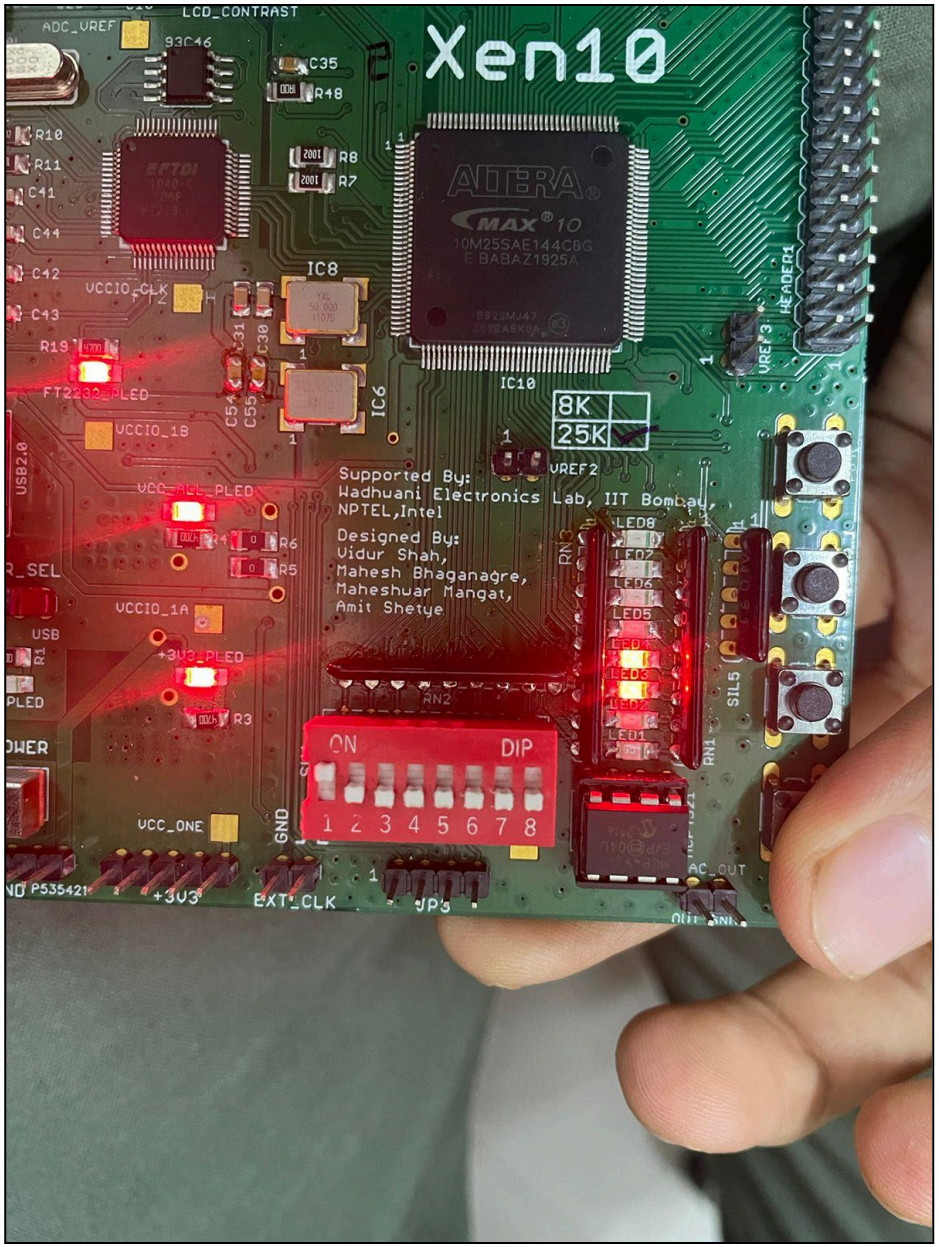

```
jtag> detect
IR length: 10
Chain length: 1
Device Id: 00000011000110000100000011011101 (0x00000000031840DD)
  Manufacturer: Altera
  Part(0):         10M25SAE144
  Stepping:     1
  Filename:     d:\quartus\quartus\majority_circuit\xen10_files\urjtag_max10\urjtag\data/altera/10m25sae144/10M25SAE144
jtag>
```

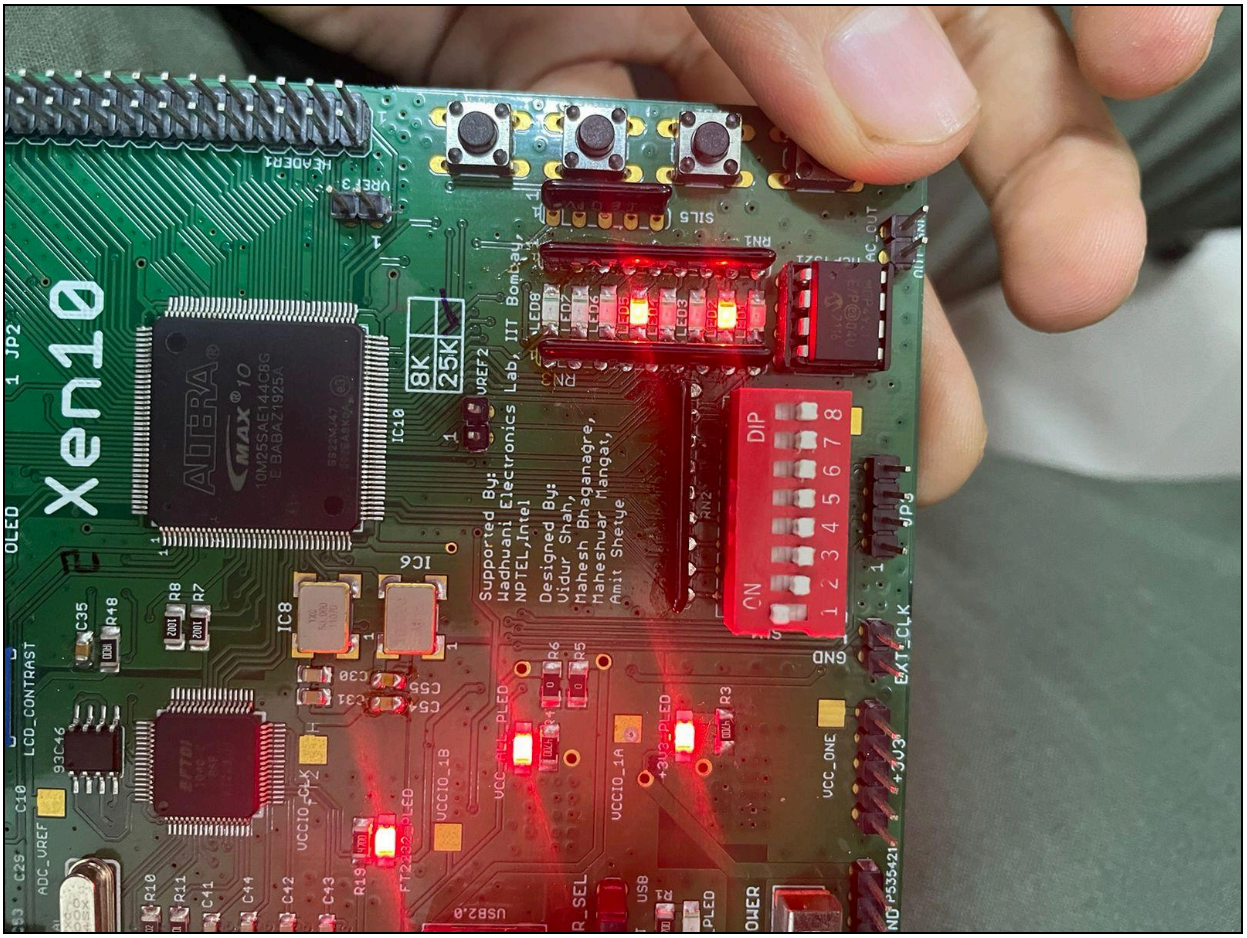
XEN10 Board Images:

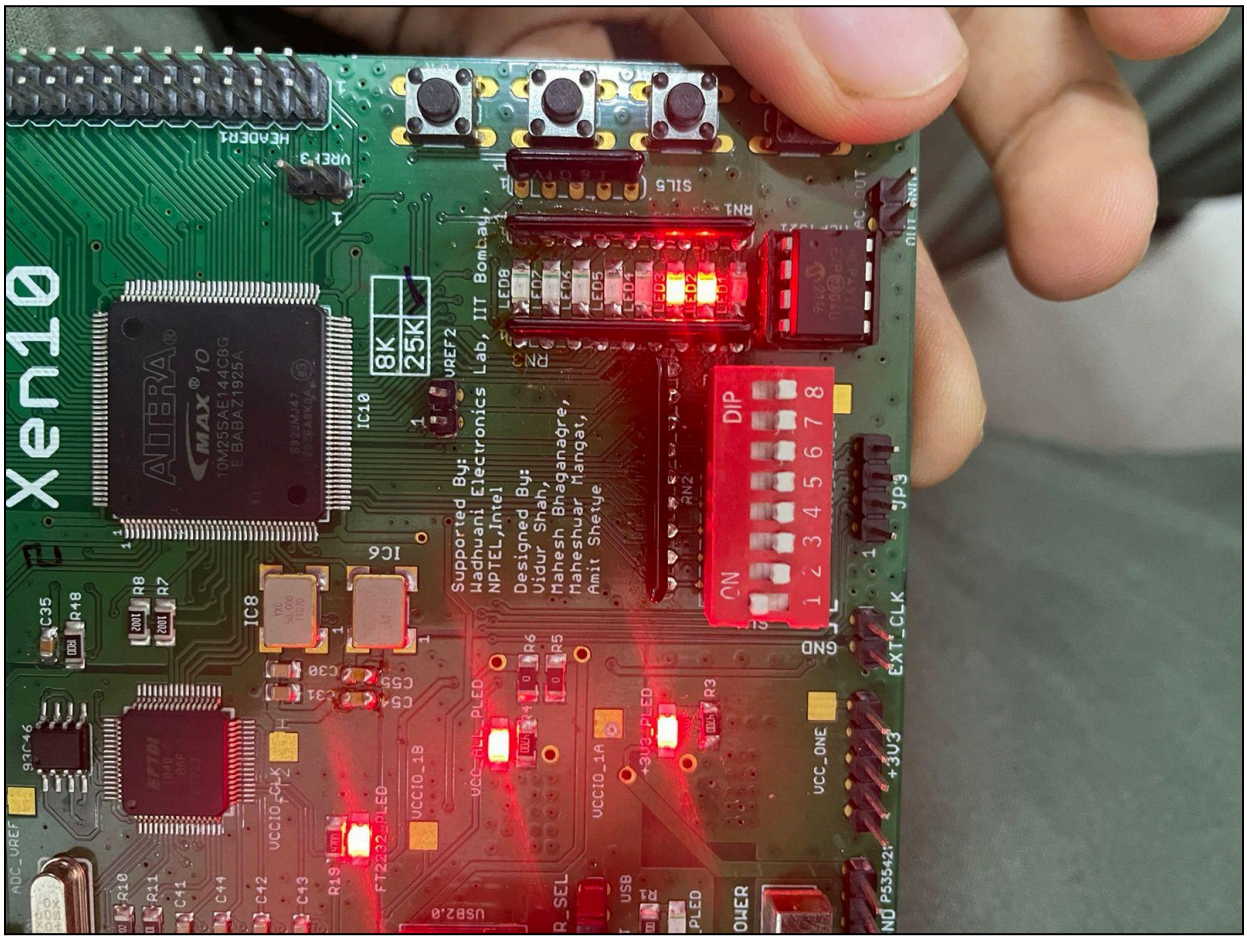

Xen10
16X2 LCD
V1.2
V1.2
OLED
JP5
JP2
LCD_CONTRAST
ADC_VREF
93C46
ALTERA
MAX 10
10M25SAE144C8
BABAZ1925
FTDI
FT2232_PLED
VCCIO_1B
VCCIO_1A
VCC_ALL_PLED
+3V3_PLED
EXT_PLED
PWR_SEL
POWER
ON
VCC_ONE
HEADER1
8K
25K
Supported By:
Wadhuani Electronics Lab, IIT Bombay,
NPTEL,Intel
Designed By:
Vidur Shah,
Mahesh Bhaganagre,
Maheshwar Mangat,
Amit Shetye
DIP
1 2 3 4 5 6 7 8



xen10
1 JP2
OLED
SDA
SCL
VCC
GND
JP5
1 ← 16X2 LCD → 16
V1.2
LCD_CONTRAST
ADC_VREF
REF_GND
ADC0
ADC2
ADC1
DIP
ON


Xen10
LCD_CONTRAST
ADC_VREF
93C46
C35
R48
R10
R11
C41
C44
C42
C43
R8
R7
IC8
VCCIO_CLK
R19
FT2232_PLED
VCCIO_1B
C54
C55
C30
C31
IC6
IC10
8K
25K
VREF2
VREF3
HEADER11
USB2.0
VCC_ALL_PLED
R6
R5
Supported By:
Wadhuani Electronics Lab, IIT Bombay,
NPTEL,Intel
Designed By:
Vidur Shah,
Mahesh Bhaganagre,
Maheshuar Mangat,
Amit Shetye
LED8
LED7
LED6
LED5
LED4
LED3
LED2
LED1
RN
RN2
RN1
SIL5
VCCIO_1A
USB
+3V3_PLED
R3
ON
DIP
1 2 3 4 5 6 7 8
VCC_ONE
GND
+3V3
EXT_CLK
JP3
AC_OUT


Xen10
Supported By:
Wadhwani Electronics Lab, IIT Bombay,
NPTEL,Intel
Designed By:
Vidur Shah,
Mahesh Bhaganagre,
Maheshuar Mangat,
Amit Shetye
DIP
ON
1 2 3 4 5 6 7 8
8K
25K



In this experiment, we successfully implemented a counter using inbuilt LED on XEN10 board.