EE214 HomeWork Assignment
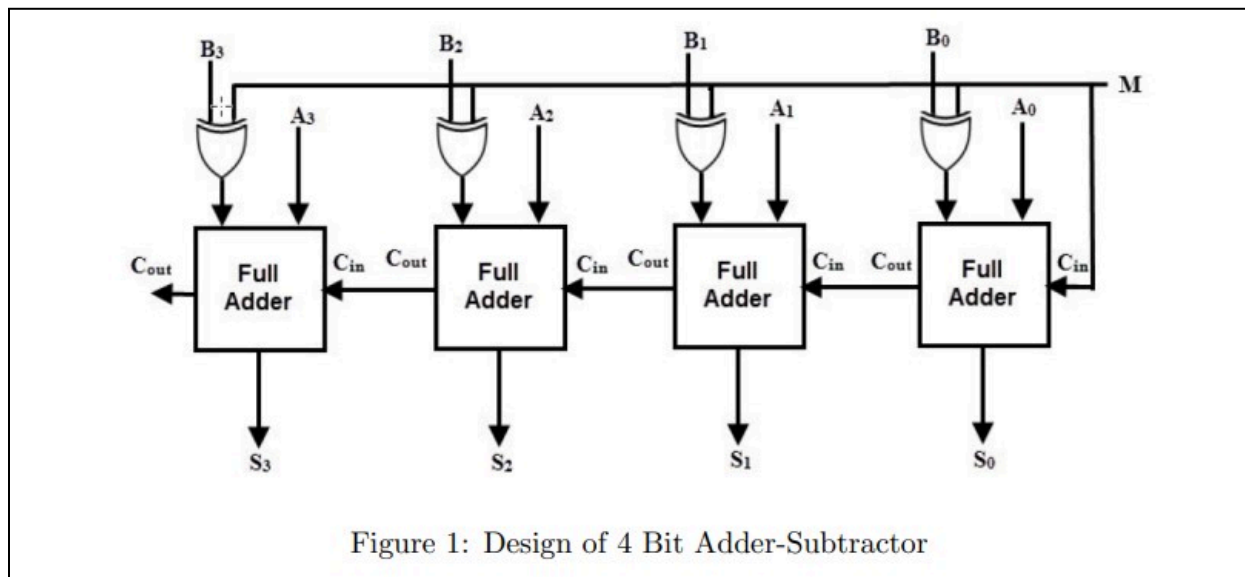
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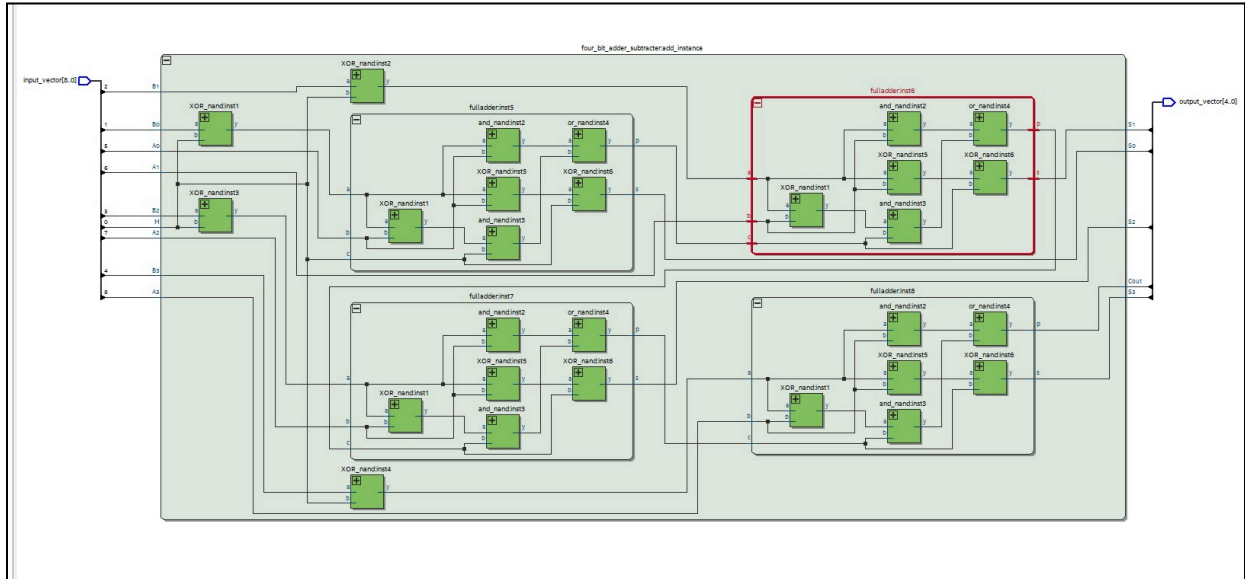
4-bit Adder Subtractor

PenPaper Design:

- The Pen Paper Design was given in the assignment itself, i didn't draw it in my notebook, instead i used this given design itself.

Figure 1: Design of 4 Bit Adder-Subtractor

Netlist:

- Shown below is the netlist of my code architecture. I have used XOR gate and Fulladder made by me earlier in this code.

Wave Simulation:

- The Wave Simulation of my 4 bit adder subtractor is attached below. All test cases passed(Success).