

DIGITAL CIRCUITS LAB

EXP-4 ALU

In this lab, we used behavioral and dataflow modeling instead of structural modeling.

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Pen-Paper Design:

There are no gates used in the code as such. Thus, there is no pen paper design for our code. This is what the dataflow of the code looks like as given in the problem statement.

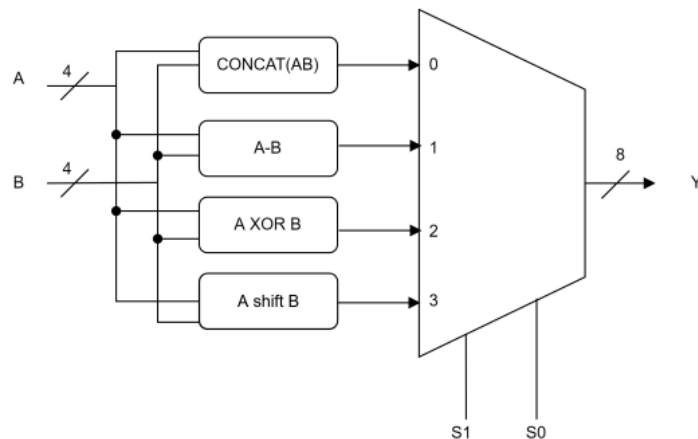
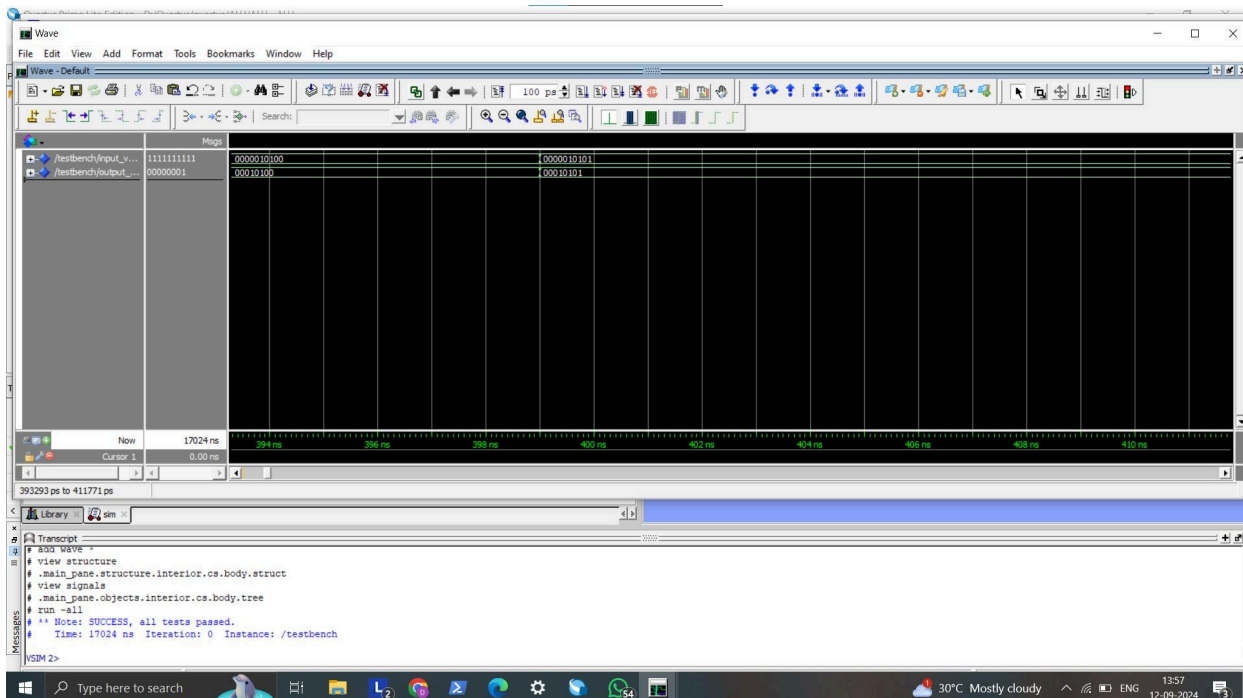
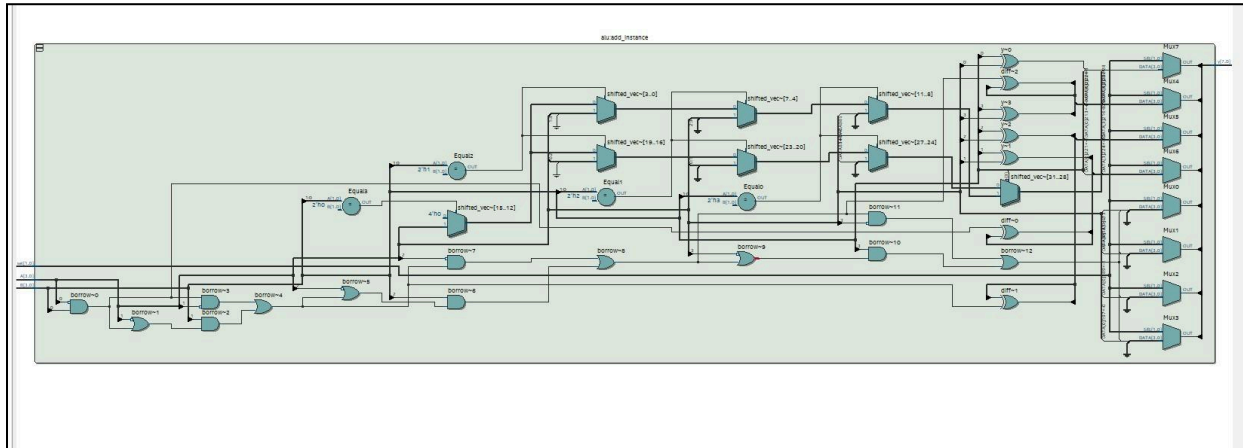


Figure 1: ALU with 4 functions

S1 S0	ALU Output
0 0	Concatenate two 4-bit inputs A and B
0 1	Performs A-B Operation
1 0	Performs A xor B Operation
1 1	Shift A by B bits [B3 - 0(left)/1(right)] [B2 - unused] [B1 B0 - no. of bits to be shifted]

Netlists & Simulation Wave:



Testing Terminal:

```
jtag> cable ft2232
Connected to libftd2xx driver.
jtag> _
```

```
jtag> detect
IR length: 10
Chain length: 1
Device Id: 00000011000110000100000011011101 (0x0000000031840DD)
Manufacturer: Altera
Part(0):      10M25SAE144
Stepping:     1
Filename:     d:\quartus\quartus\majority_circuit\xen10_files\urjtag_max10\urjtag\data\altera/10m25sae144/10M25SAE144
jtag> _
```

Command Prompt:

Input command: *scan_vjtag.exe TRACEFILE.txt out.txt*

Output:

```
{'type': 6, 'id': 67330064, 'description': b'Dual RS232-HS A', 'serial': b'A'}
```

ScanChain Outputs:

File	Edit	Format	View	Help
0000000000	00000000	Success		
0000000001	00000001	Success		
0000000010	00000010	Success		
0000000011	00000011	Success		
0000000100	00000100	Success		
0000000101	00000101	Success		
0000000110	00000110	Success		
0000000111	00000111	Success		
0000001000	00001000	Success		
0000001001	00001001	Success		
0000001010	00001010	Success		
0000001011	00001011	Success		
0000001100	00001100	Success		
0000001101	00001101	Success		
0000001110	00001110	Success		
0000001111	00001111	Success		
0000010000	00010000	Success		
0000010001	00010001	Success		
0000010010	00010010	Success		
0000010011	00010011	Success		
0000010100	00010100	Success		

Success in scanchain out file for the ALU lab experiment.