DIGITAL CIRCUITS LAB

EXP-4 ALU

In this lab, we used behavioral and dataflow modeling instead of structural modeling.

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Pen-Paper Design:

There are no gates used in the code as such. Thus, there is no pen paper design for our code. This is what the dataflow of the code looks like as given in the problem statement.

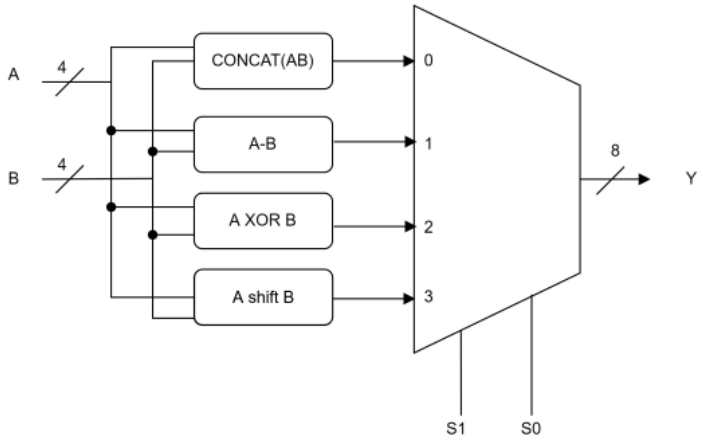
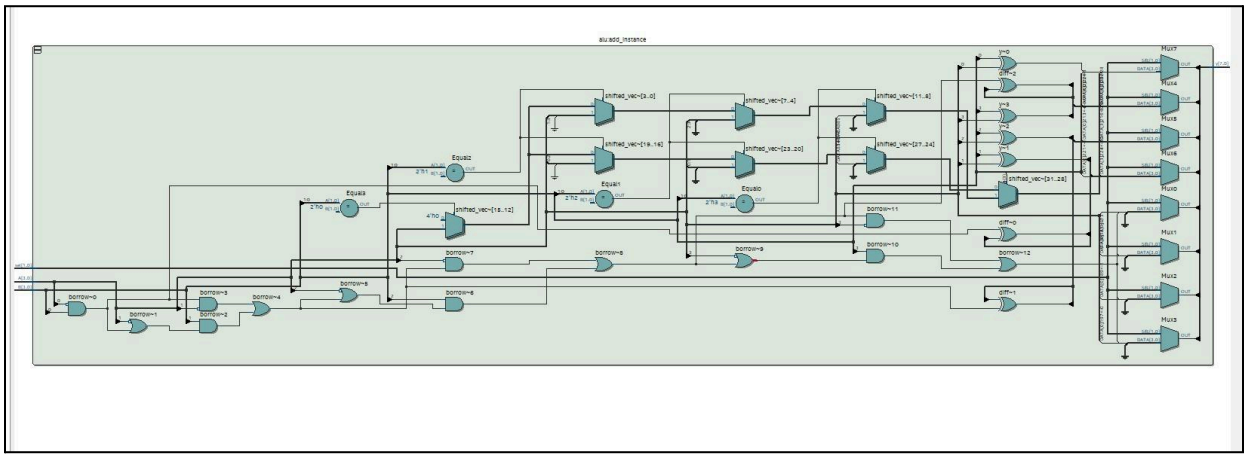
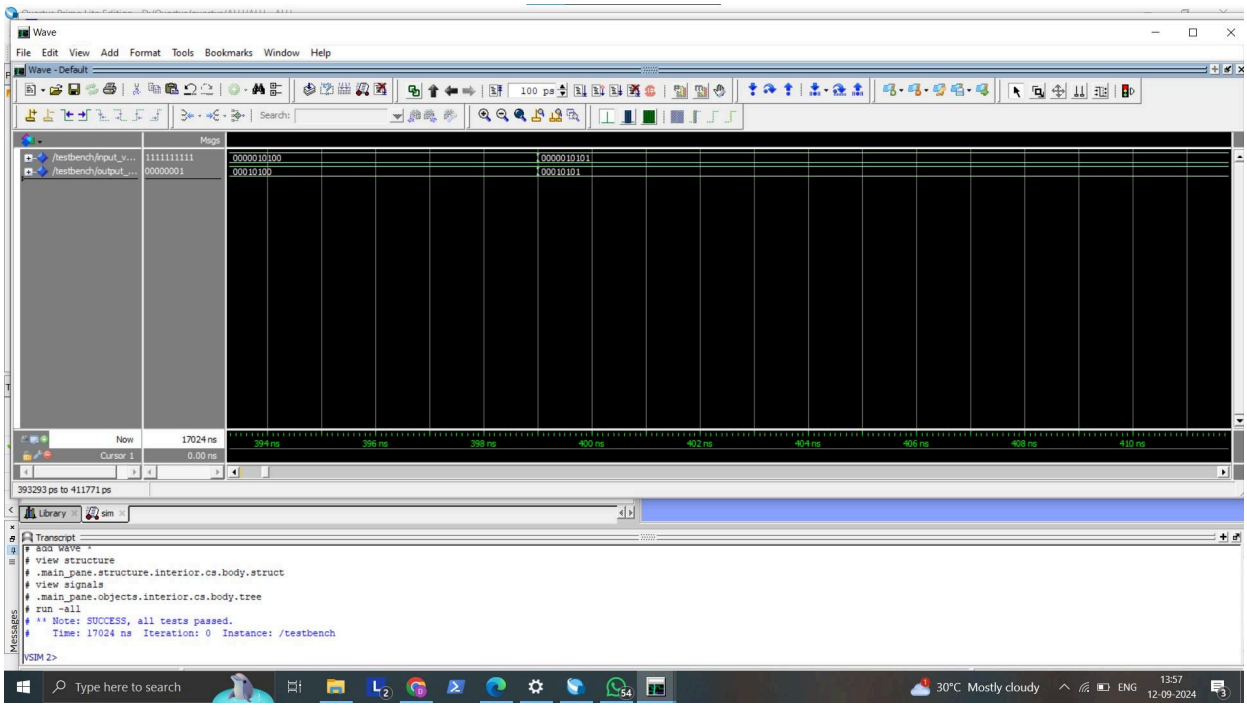


Figure 1: ALU with 4 functions

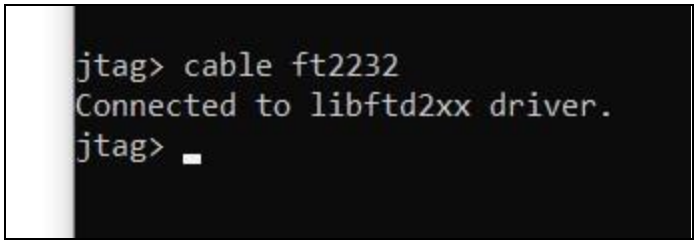
S1 S0	ALU Output
0 0	Concatenate two 4-bit inputs A and B
0 1	Performs A-B Operation
1 0	Performs A xor B Operation
1 1	Shift A by B bits [B3 - 0(left)/1(right)] [B2 - unused] [B1 B0 - no. of bits to be shifted]

Netlists & Simulation Wave:





Testing Terminal:




```
jtag> detect
IR length: 10
Chain length: 1
Device Id: 00000011000110000100000011011101 (0x00000000031840DD)
  Manufacturer: Altera
  Part(0):         10M25SAE144
  Stepping:     1
  Filename:     d:\quartus\quartus\majority_circuit\xen10_files\urjtag_max10\urjtag\data/altera/10m25sae144/10M25SAE144
jtag>
```

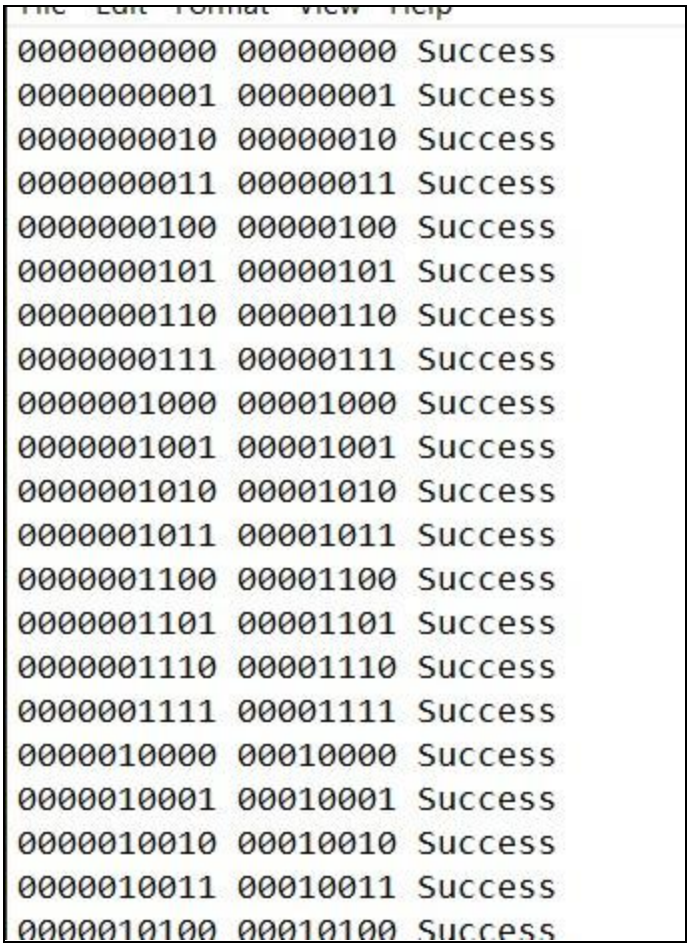
Command Prompt:

Input command: *scan_vjtag.exe TRACEFILE.txt out.txt*

Output:

```
{'type': 6, 'id': 67330064, 'description': b'Dual RS232-HS A', 'serial': b'A'}
```

ScanChain Outputs:



Success in scanchain out file for the ALU lab experiment.