Pen Paper Designs:

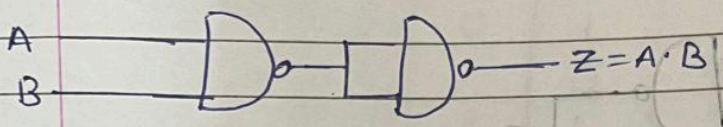
8/8/24

M T W T F S S
Page No.: YOUVA
Date:

(I) Designing circuits using universal NAND gate.

PROBLEM SET-1

(i) AND GATE (A·B)

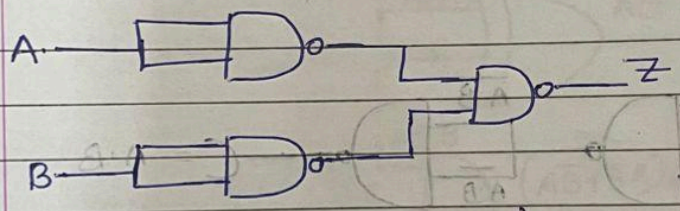


(2 NAND gates required)

TRUTH TABLE

A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

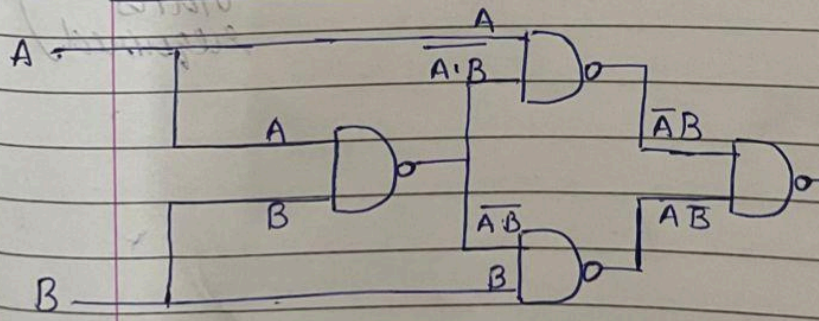
(ii) OR GATE (A + B)



(3 NAND Gates required)

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1

(iii) XOR GATE ($\bar{A}B + \bar{B}A$)



(4 NAND Gates Required)

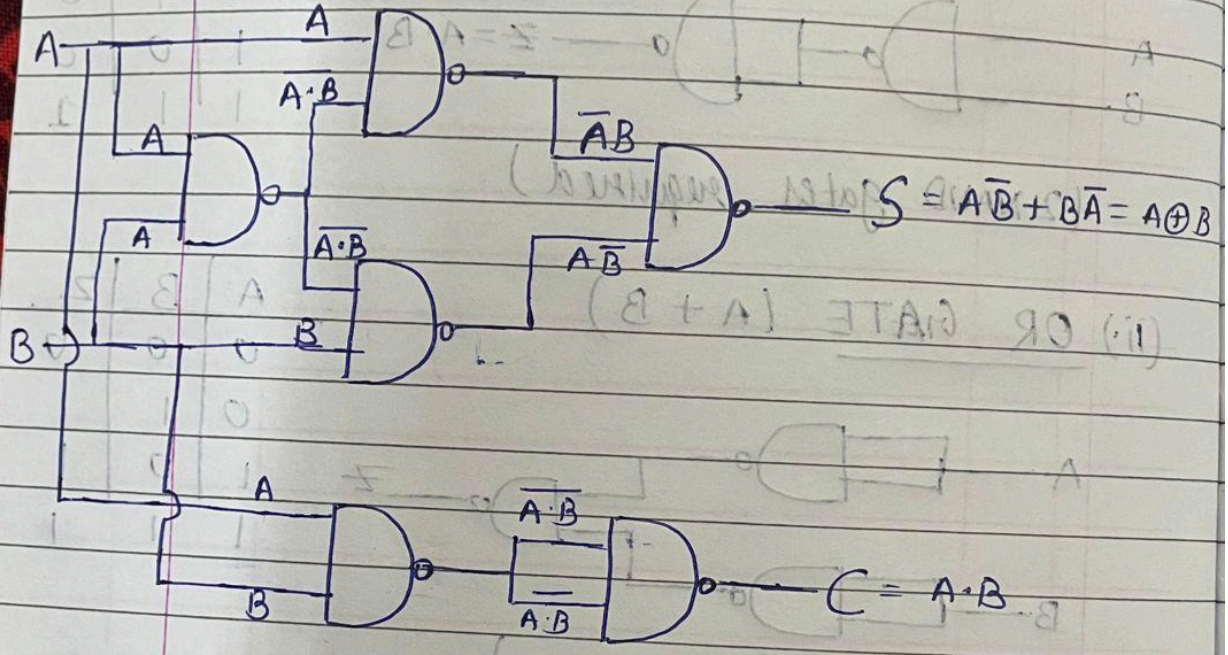
A	B	Z
0	0	0
0	1	1
1	0	1
1	1	0

(iv) Half Adder

$S = A \oplus B$

$C = A \cdot B$

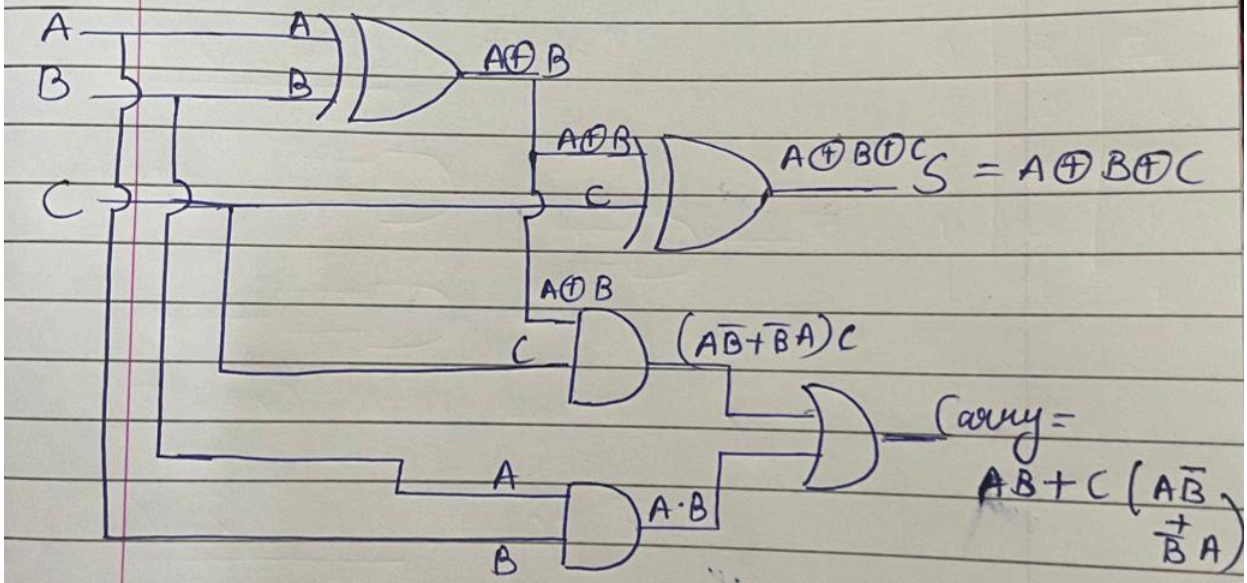
A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



(1 XOR + 1 AND GATES
= 4 NAND + 2 NAND = 6 NAND Gates required.)

(v) Full Adder :-

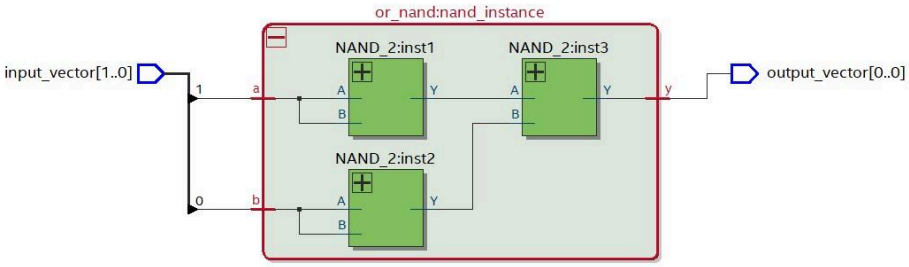
A	B	C	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

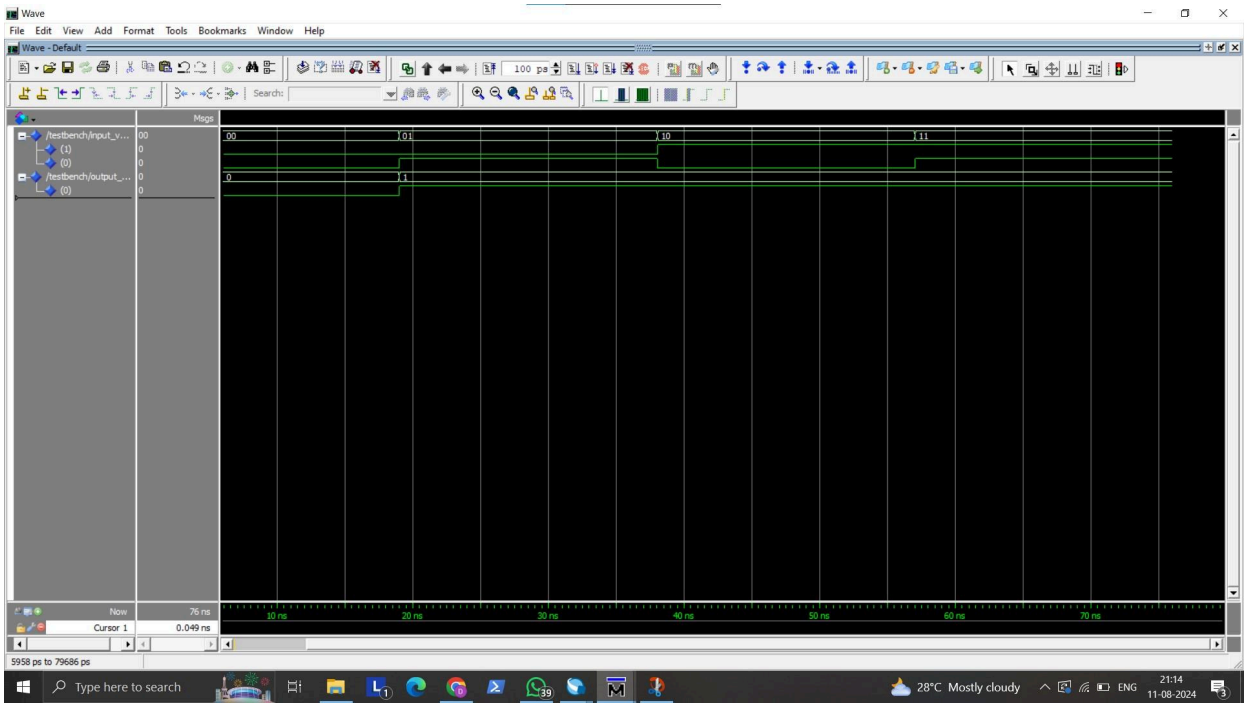


Added

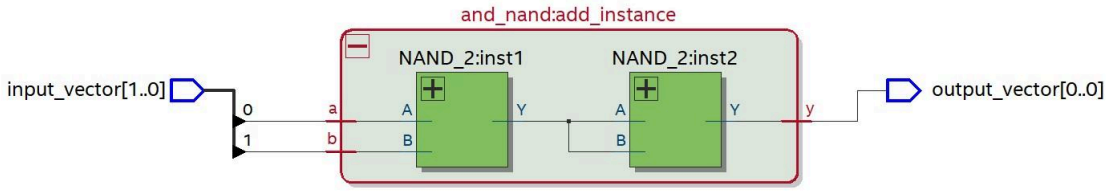
NETLISTS & SIMULATIONS-

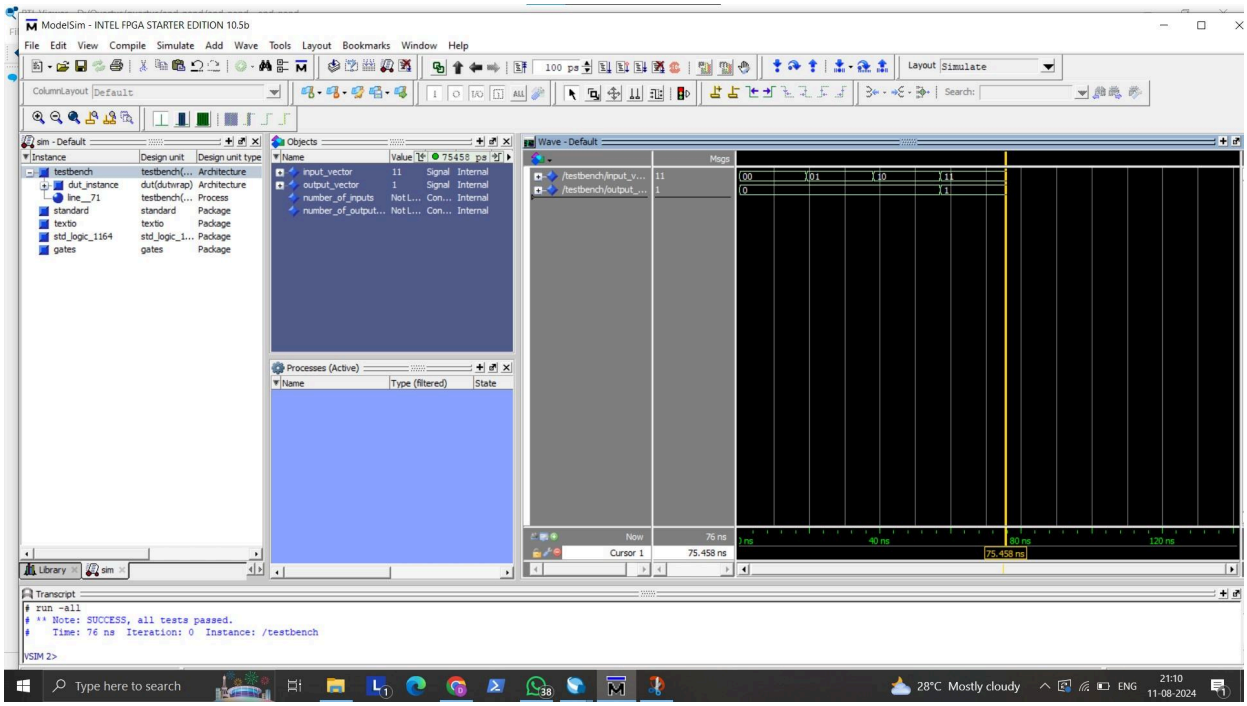
OR GATE:



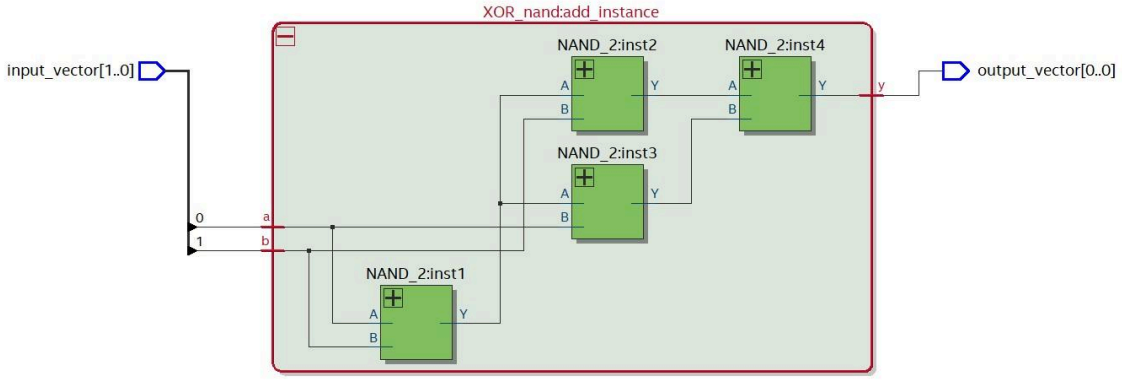


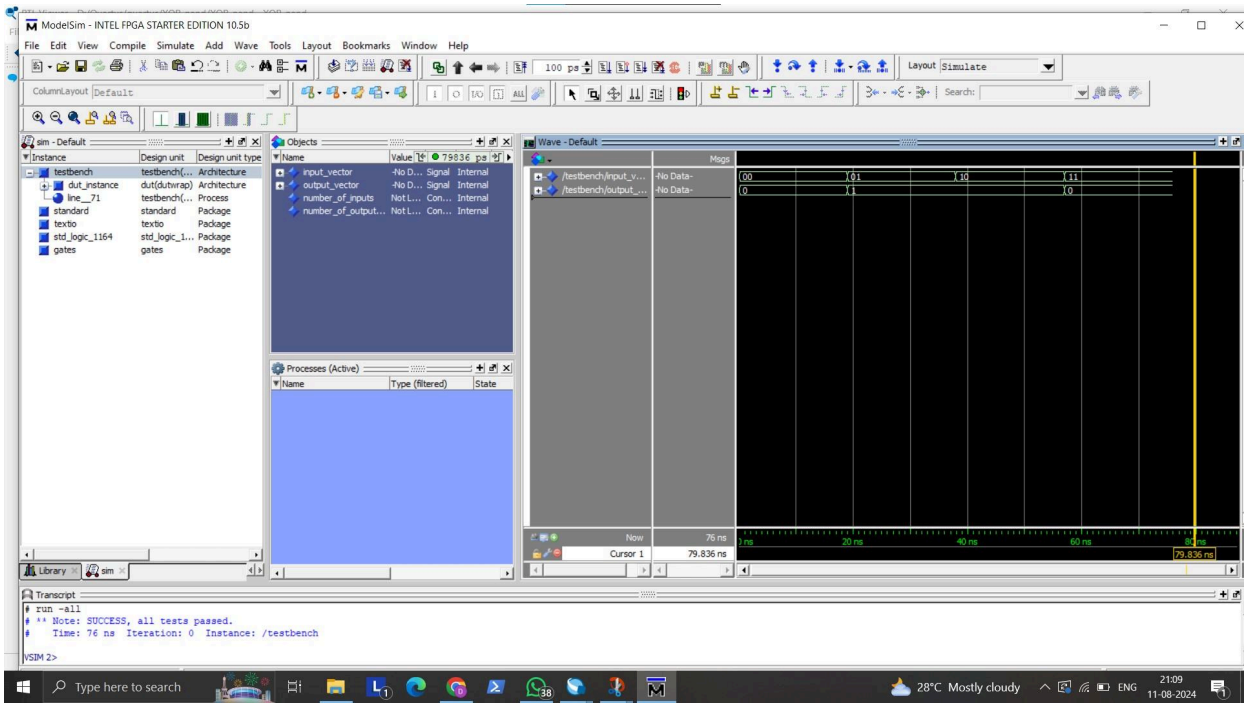
AND GATE:


and_nand:add_instance
NAND_2:inst1
NAND_2:inst2
input_vector[1..0]
output_vector[0..0]
0
1
a
b
A
B
Y
y

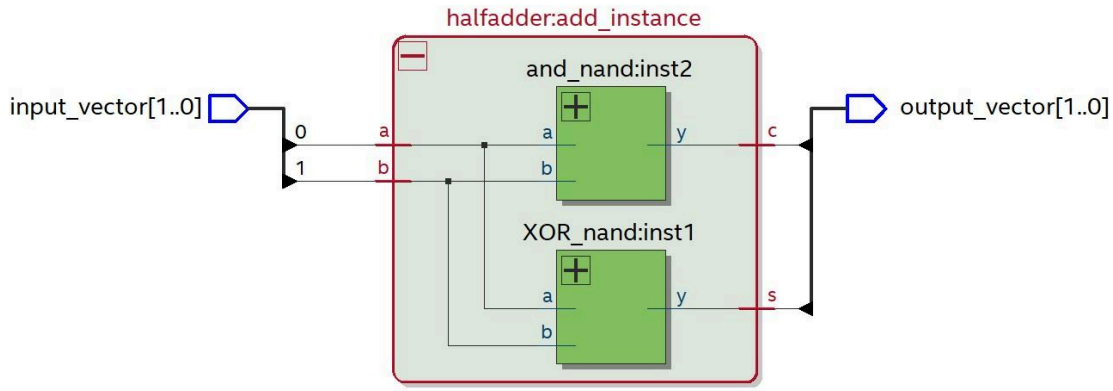

ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Objects
Wave - Default
Processes (Active)
Transcript
run -all
** Note: SUCCESS, all tests passed.
Time: 76 ns Iteration: 0 Instance: /testbench
VSIM 2>
Type here to search
28°C Mostly cloudy
ENG
21:10
11-08-2024

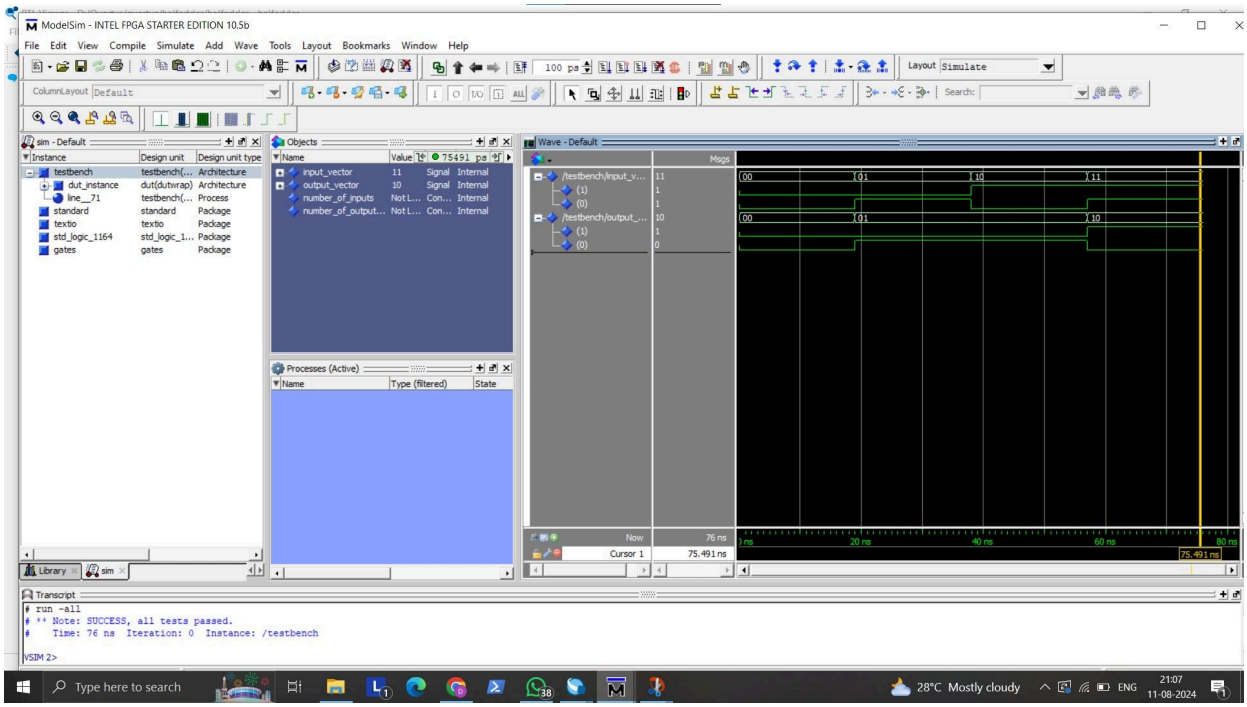
XOR GATE:


XOR_nand:add_instance
input_vector[1..0]
output_vector[0..0]
NAND_2:inst2
NAND_2:inst4
NAND_2:inst3
NAND_2:inst1
A
B
Y
a
b
y
0
1

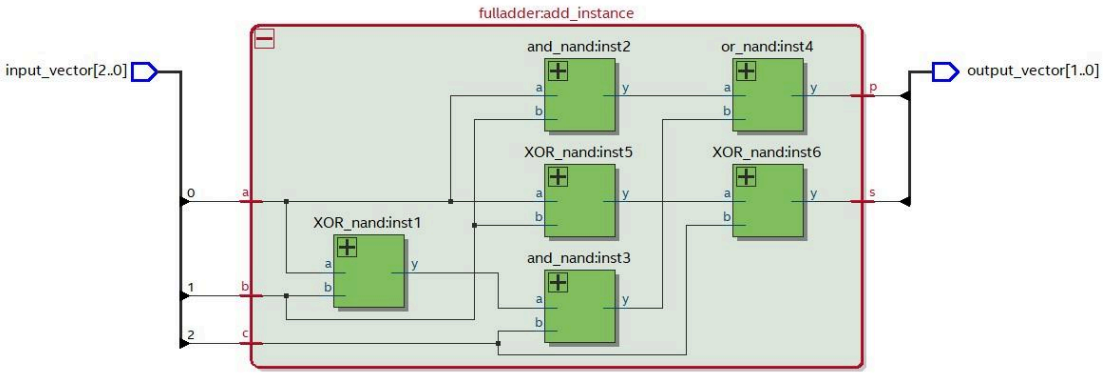

ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Wave - Default
Transcript
run -all
** Note: SUCCESS, all tests passed.
Time: 76 ns Iteration: 0 Instance: /testbench
VSIM 2>
Type here to search
28°C Mostly cloudy
ENG
21:09
11-08-2024

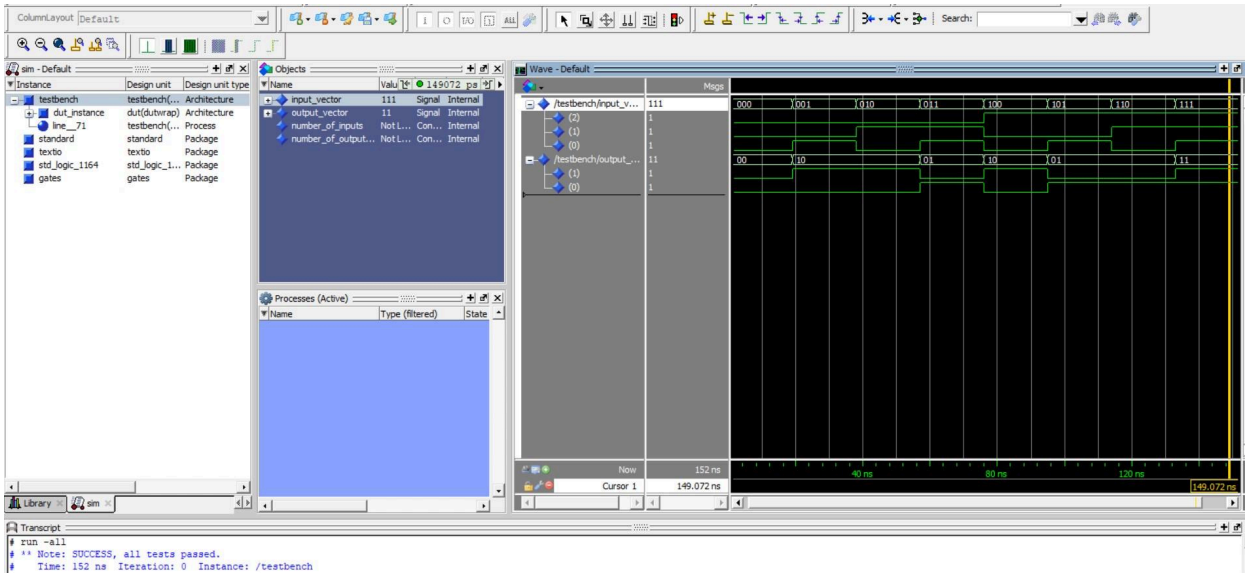
HALF ADDER:


halfadder:add_instance
and_nand:inst2
XOR_nand:inst1
input_vector[1..0]
output_vector[1..0]
0
1
a
b
c
s
y


ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Transcript
run -all
** Note: SUCCESS, all tests passed.
Time: 76 ns Iteration: 0 Instance: /testbench
VSIM 2>
Type here to search
28°C Mostly cloudy
ENG
21:07
11-08-2024

FULL ADDER:


fulladder:add_instance
input_vector[2..0]
output_vector[1..0]
and_nand:inst2
or_nand:inst4
XOR_nand:inst5
XOR_nand:inst6
XOR_nand:inst1
and_nand:inst3
0
1
2
a
b
c
y
p
s


sim - Default
Objects
Wave - Default
Processes (Active)
Transcript
run -all
** Note: SUCCESS, all tests passed.
Time: 152 ns Iteration: 0 Instance: /testbench