DIGITAL CIRCUITS LAB

EXP-6 Dflipflop

In this lab, we used dataflow modeling instead of structural modeling.

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Pen-Paper Design:

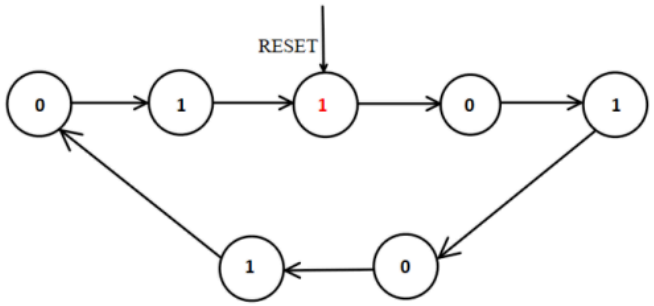

Figure 1: Sequence Generator

- Determine number of bits required to distinguish the states individually.
- Draw a state diagram to generate the states so that LSB of the states will generate the required sequence.
- Draw a state table consisting of Present State, Nest State and D FlipFlop inputs.

Present State(Qn..Q1 Q0)	Next State(N_Qn..N_Q1 N_Q0)	Dn...D1 D0
one state	next state	DFF inputs
–	–	–

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Problem Set 5

Q_0	Q_1	Q_2	Q_0^+	Q_1^+	Q_2^+			
Q_A	Q_B	Q_C	Q_A^+	Q_B^+	Q_C^+	D_A	D_B	D_C
1	0	0	0	0	0	0	0	0
0	0	0	1	0	1	1	0	1
1	0	1	0	0	1	0	0	1
0	0	1	1	1	0	1	1	0
1	1	0	0	1	0	0	1	0
0	1	0	1	1	1	1	1	1
1	1	1	1	0	0	1	0	0
0	1	1	0	0	0	0	0	1

Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	D_2	D_1	D_0
0	0	1	0	0	0	0	0	0
0	0	0	0	1	1	0	1	1
0	1	1	0	1	0	0	1	0
0	1	0	1	0	1	1	0	1
1	0	1	1	0	0	1	0	0
1	0	0	1	1	1	1	1	1
1	1	1	0	0	1	0	0	1
1	1	0	0	0	1	0	0	1

$D_0 \Rightarrow$

Q_0 \ Q_2Q_1	$\bar{Q}_2\bar{Q}_1$	$\bar{Q}_2Q_1$	Q_2Q_1	$Q_2\bar{Q}_1$
$\bar{Q}_0$	1	1	1	1
Q_0	0	0	1	0

$D_0 = Q_2Q_1 + \bar{Q}_0$

$D_1 \Rightarrow$

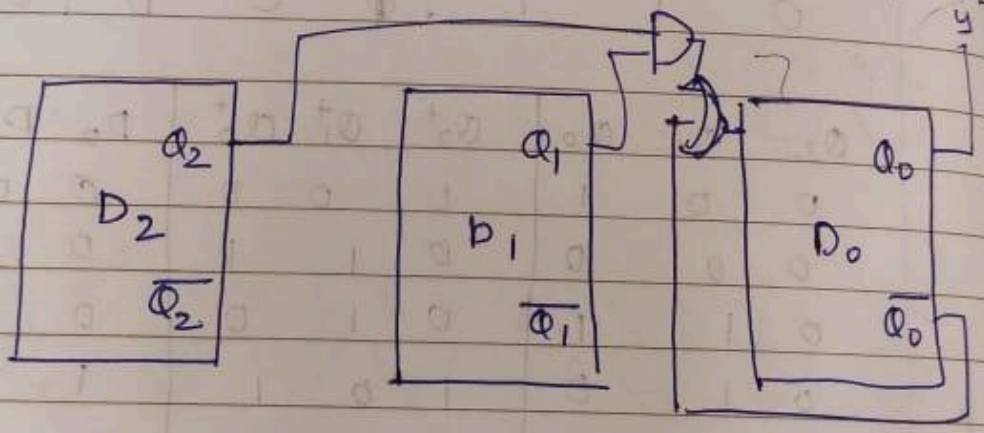
Q_2 \ Q_1Q_0	$\overline{Q_1}\,\overline{Q_0}$	$\overline{Q_1}\,Q_0$	Q_1Q_0	$Q_1\overline{Q_0}$
$\overline{Q_2}$	1	0	1	0
Q_2	1	0	0	0

$$D_1 = Q_1Q_0\overline{Q_2} + \overline{Q_1}Q_0$$

$D_2 \Rightarrow$

Q_2 \ Q_1Q_0	$\overline{Q_1}\,\overline{Q_0}$	$\overline{Q_1}\,Q_0$	Q_1Q_0	$Q_1\overline{Q_0}$
$\overline{Q_2}$	0	0	0	1
Q_2	1	1	0	0

$$D_2 = Q_2\overline{Q_1} + Q_1\overline{Q_0}\,\overline{Q_2}$$



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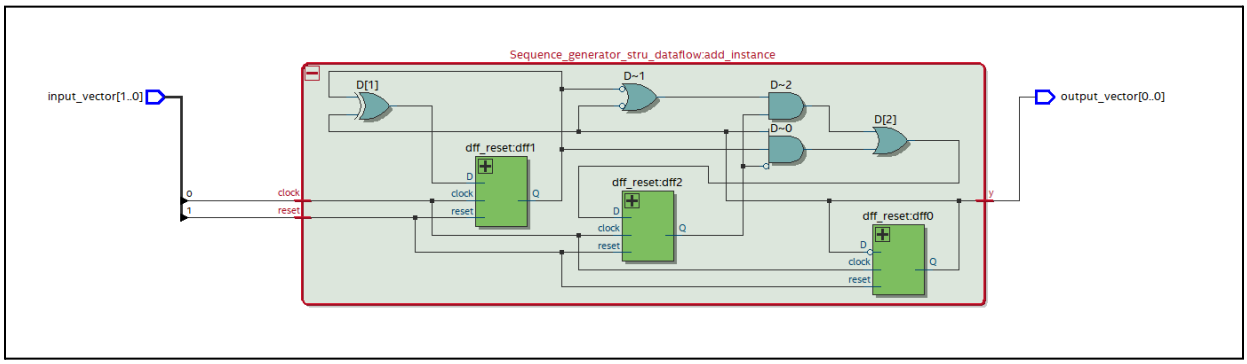
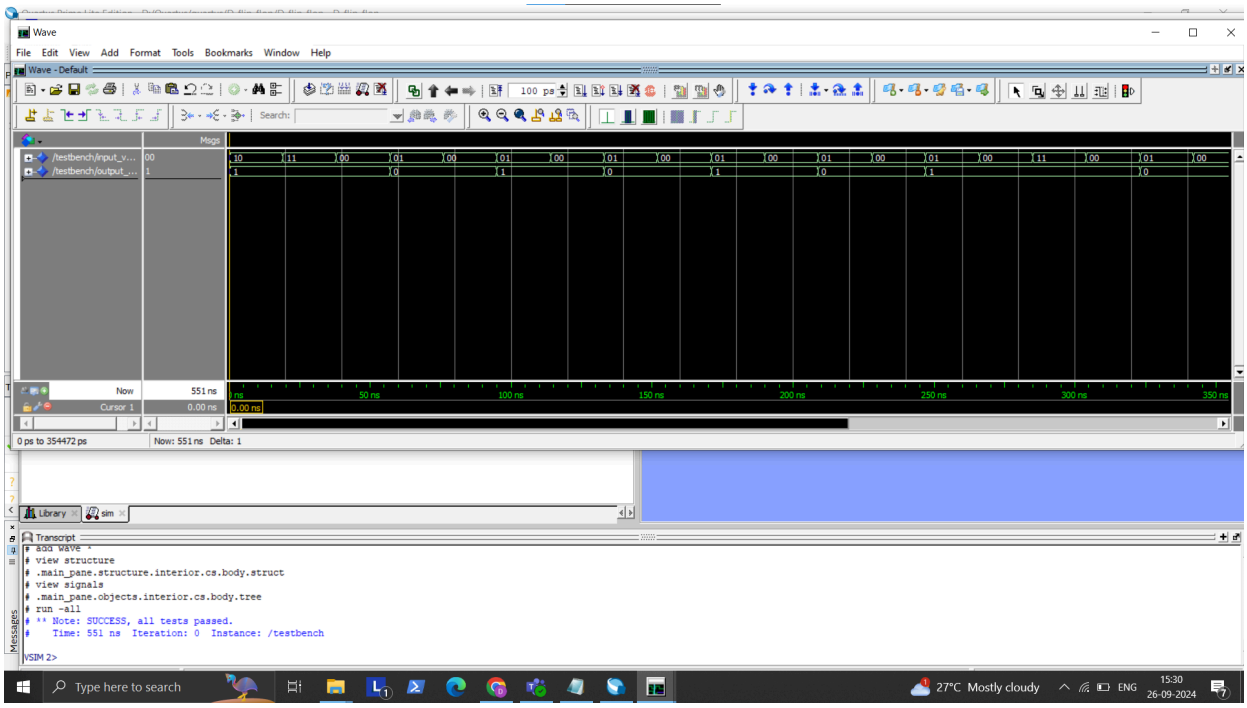
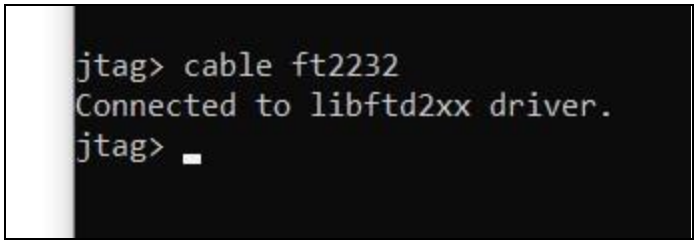
Netlists & Simulation Wave:





Testing Terminal:




```
jtag> detect
IR length: 10
Chain length: 1
Device Id: 00000011000110000100000011011101 (0x00000000031840DD)
  Manufacturer: Altera
  Part(0):         10M25SAE144
  Stepping:     1
  Filename:     d:\quartus\quartus\majority_circuit\xen10_files\urjtag_max10\urjtag\data/altera/10m25sae144/10M25SAE144
jtag>
```

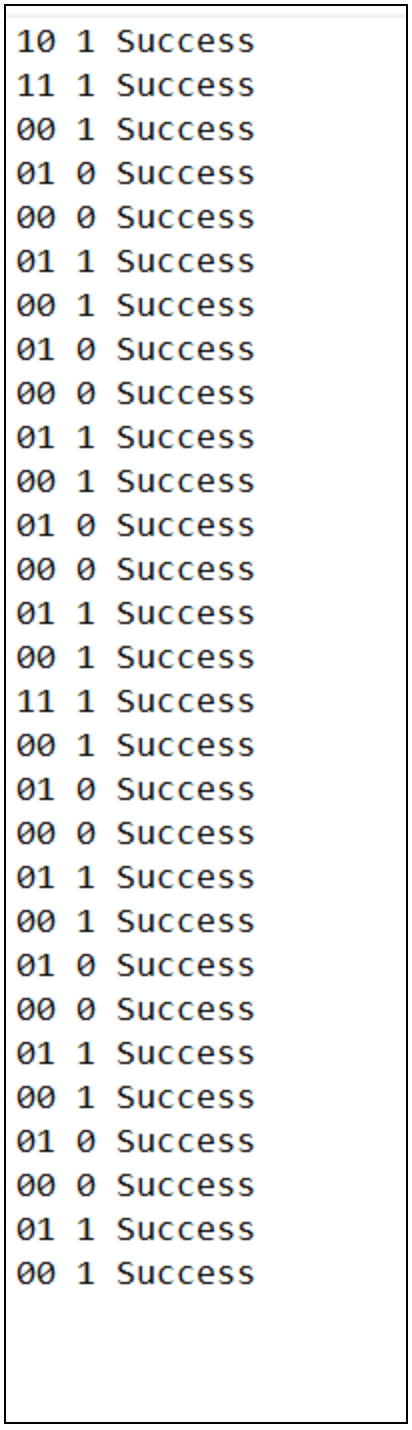
Command Prompt:

Input command: *scan_vjtag.exe TRACEFILE.txt out.txt*

Output:

```
{'type': 6, 'id': 67330064, 'description': b'Dual RS232-HS A', 'serial': b'A'}
```

ScanChain Outputs:



Success in scanchain out file for the D_flip_flop lab experiment.