DIGITAL CIRCUITS LAB

EXP-9 Traffic Controller

In this lab, we used dataflow & behavioural modeling.

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Pen-Paper Design:

Clock Source Frequency	FPGA Pin no.
1 Hz CLK	55
50 MHz CLK	26
Ext CLK	27
10 MHz CLK	29

Figure 2: Pin-mapping for on-board Clock Sources

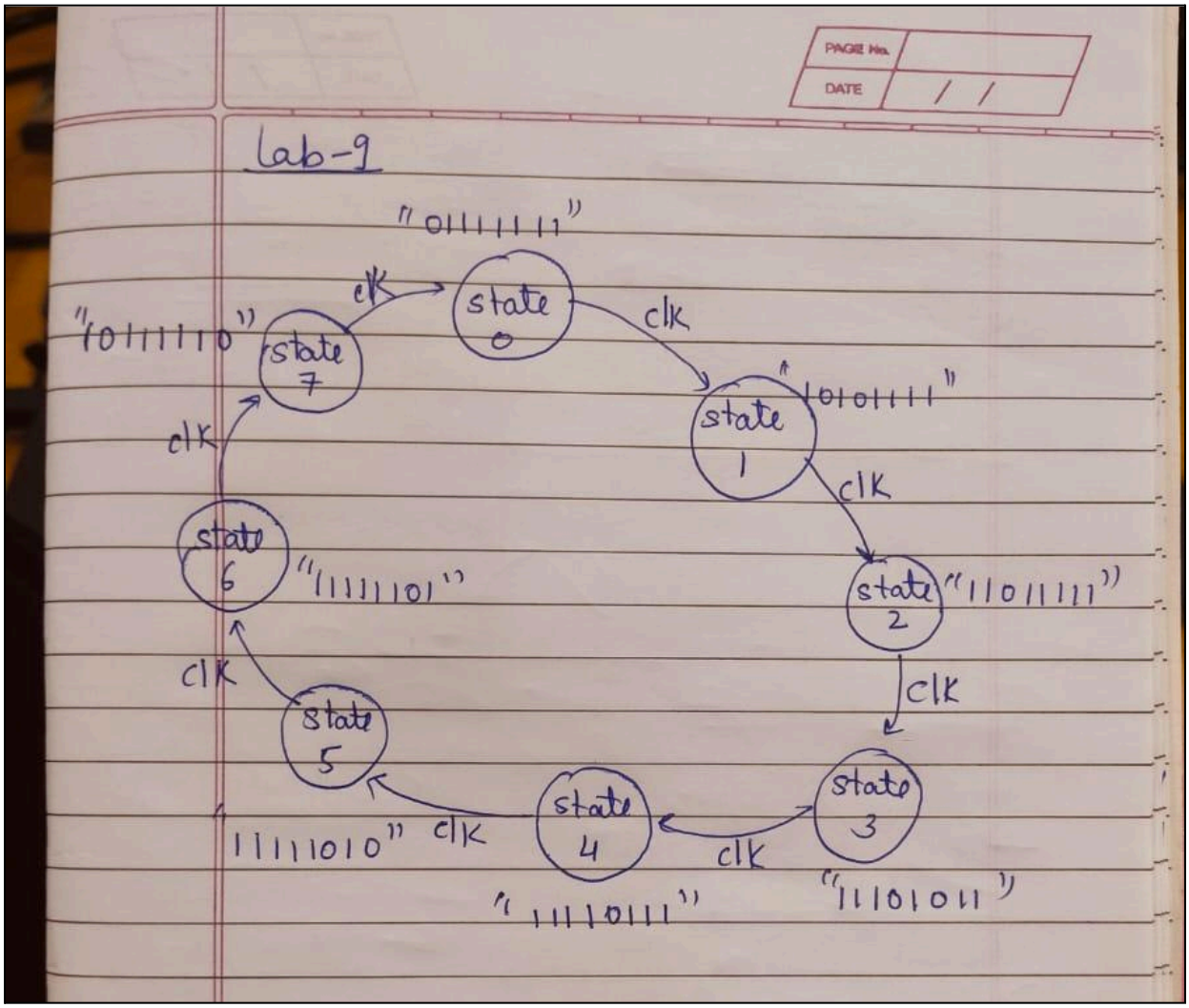
Switch	FPGA Pin no.	LED	FPGA Pin no.
SW 8	47	LED 8	60
SW 7	46	LED 7	59
SW 6	45	LED 6	58
SW 5	44	LED 5	57
SW 4	43	LED 4	56
SW 3	41	LED 3	54
SW 2	39	LED 2	52
SW 1	38	LED 1	50

Figure 3: Pin-mapping for on-board Switches and LED's

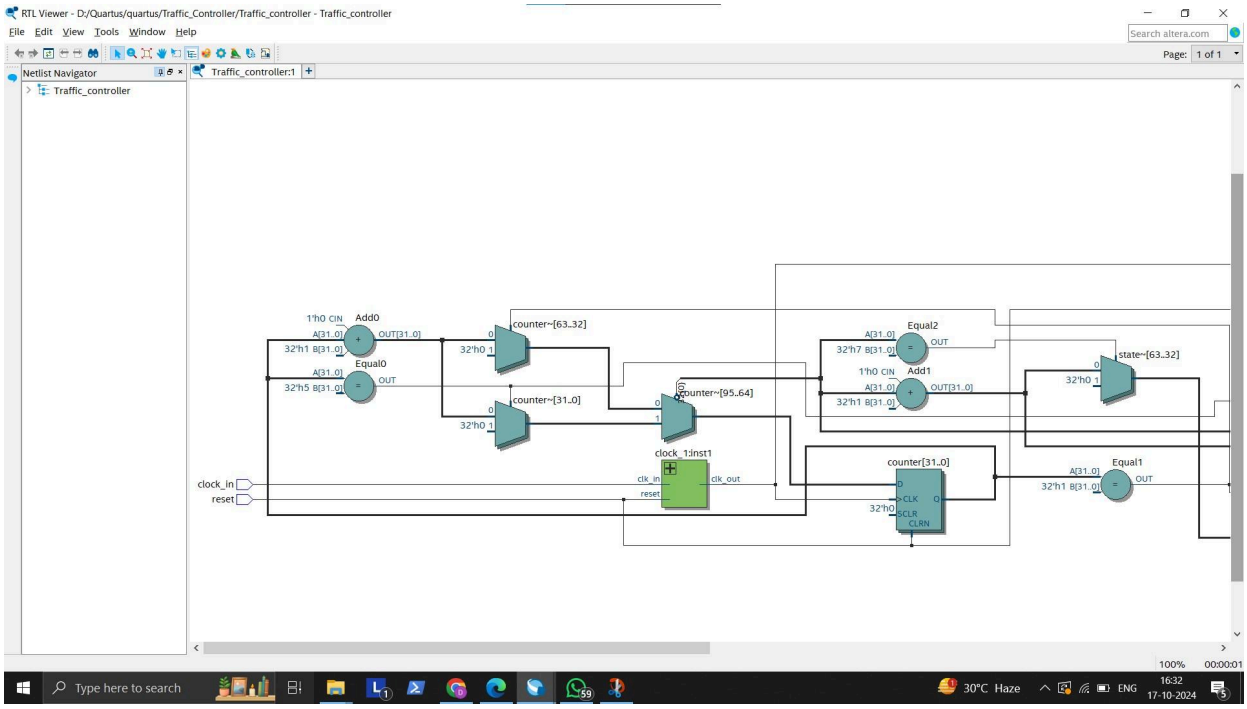
Signal Value	North_1	North_0
RED = 0; YELLOW = 0; GREEN = 1;	0	1
RED = 0; YELLOW = 1; GREEN = 0;	1	0
RED = 1; YELLOW = 0; GREEN = 0;	1	1

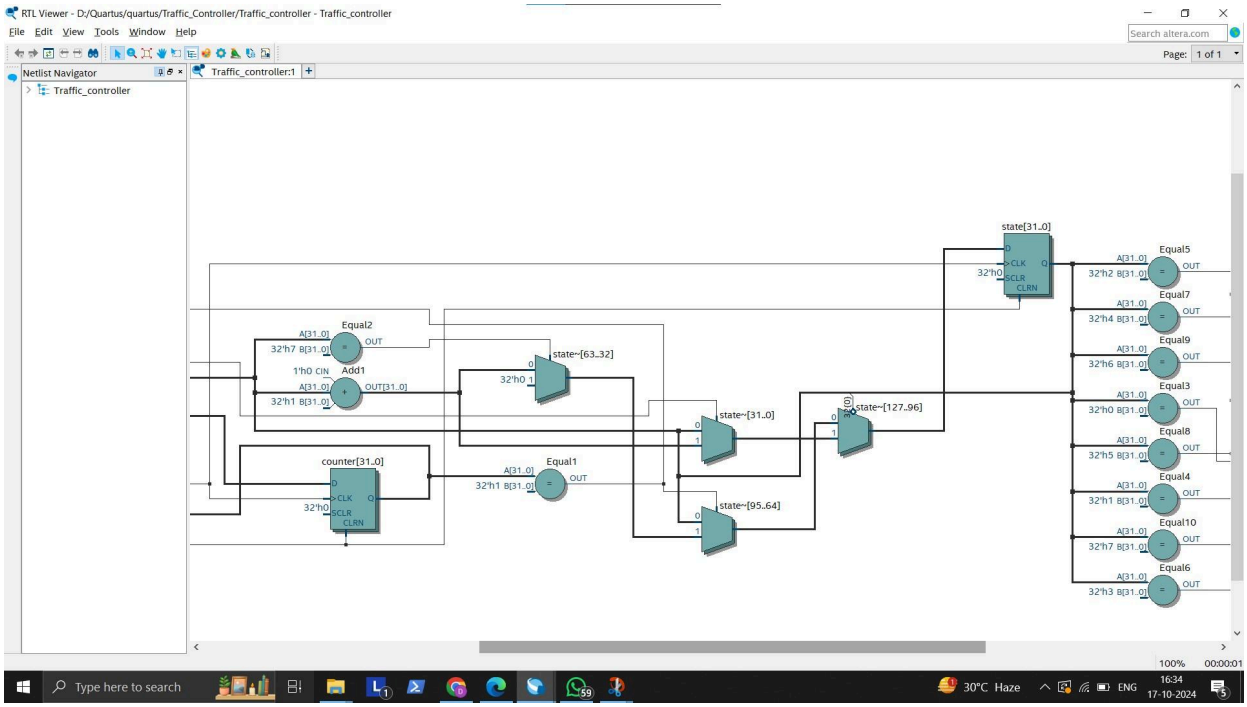
$$North\_1 \implies LED[1] \quad North\_0 \implies LED[0]$$
$$East\_1 \implies LED[3] \quad East\_0 \implies LED[2]$$
$$South\_1 \implies LED[5] \quad South\_0 \implies LED[4]$$
$$West\_1 \implies LED[7] \quad West\_0 \implies LED[6]$$

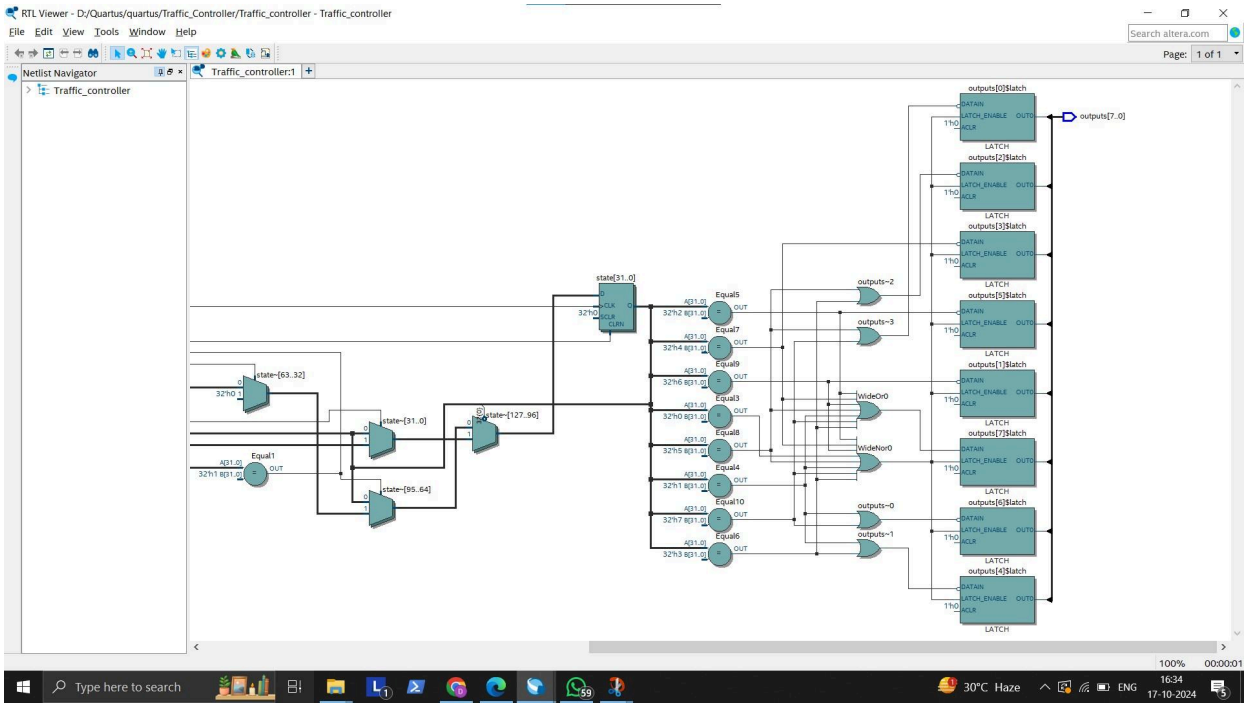
Direction	t=0s	t=5s	t=6s	t=11s	t=12s	t=17s	t=18s	t=23s
North	GREEN	YELLOW	RED	RED	RED	RED	RED	YELLOW
East	RED	YELLOW	GREEN	YELLOW	RED	RED	RED	RED
South	RED	RED	RED	YELLOW	GREEN	YELLOW	RED	RED
West	RED	RED	RED	RED	RED	YELLOW	GREEN	YELLOW


PAGE No.
DATE
lab-9
"01111111"
state 0
clk
"10111110"
state 7
clk
state 1
"10101111"
clk
clk
state 6
"11111101"
state 2
"11011111"
clk
clk
state 5
state 3
"11111010"
clk
state 4
clk
"11110111"
"11101011"

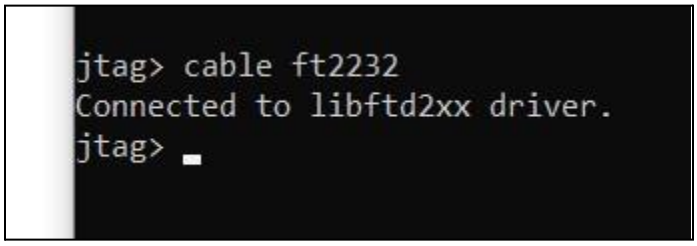
Netlists & Simulation Wave:


RTL Viewer - D:/Quartus/quartus/Traffic_Controller/Traffic_controller - Traffic_controller
File Edit View Tools Window Help
Netlist Navigator
Traffic_controller
Traffic_controller:1
Add0
Equal0
counter~[63..32]
counter~[31..0]
counter~[95..64]
clock_1:inst1
clock_in
reset
Equal2
Add1
state~[63..32]
counter[31..0]
Equal1
100%
00:00:01
Type here to search
30°C Haze
ENG
16:32
17-10-2024


RTL Viewer - D:/Quartus/quartus/Traffic_Controller/Traffic_controller - Traffic_controller
File Edit View Tools Window Help
Netlist Navigator
Traffic_controller
Traffic_controller:1
state[31..0]
Equal5
Equal7
Equal9
Equal3
Equal8
Equal4
Equal10
Equal6
Equal2
Add1
state~[63..32]
state~[31..0]
state~[127..96]
state~[95..64]
counter[31..0]
Equal1
100%
00:00:01
Type here to search
30°C Haze
ENG
16:34
17-10-2024



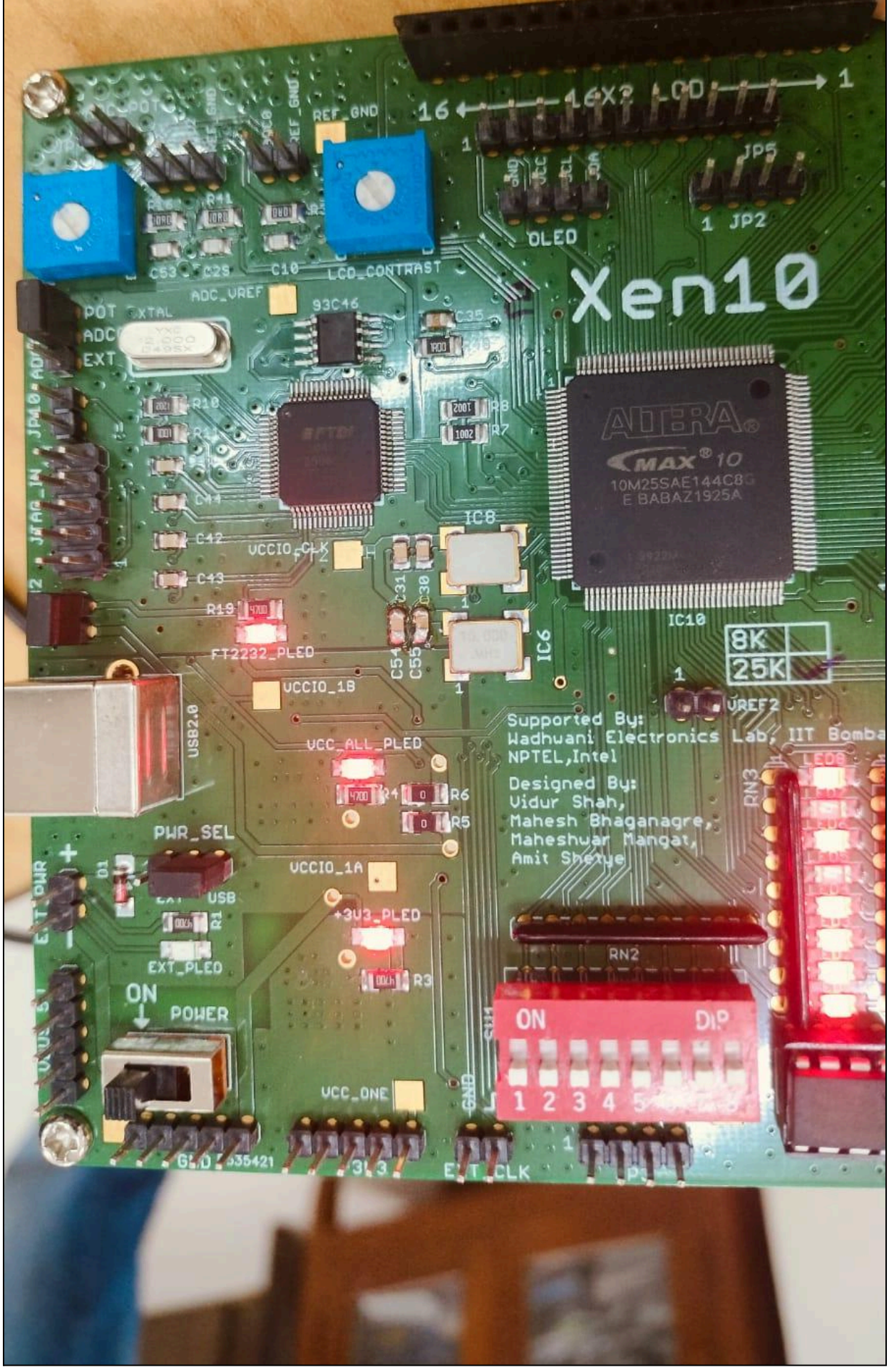
Testing Terminal:

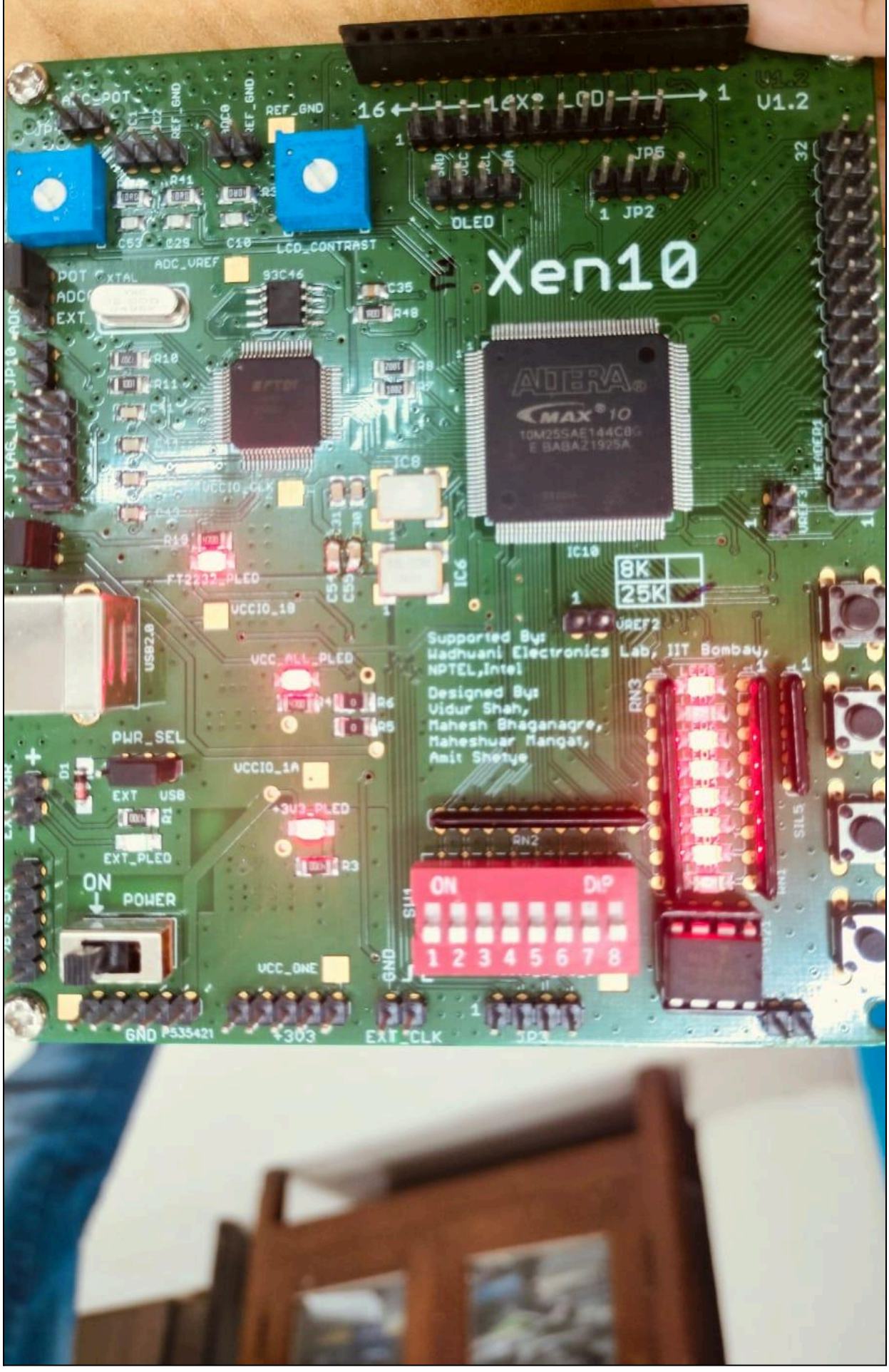



```
jtag> detect
IR length: 10
Chain length: 1
Device Id: 00000011000110000100000011011101 (0x00000000031840DD)
  Manufacturer: Altera
  Part(0):         10M25SAE144
  Stepping:     1
  Filename:     d:\quartus\quartus\majority_circuit\xen10_files\urjtag_max10\urjtag\data/altera/10m25sae144/10M25SAE144
jtag>
```

XEN10 Board Images:


Xen10
V1.2
16X2 LCD
OLED
JP5
JP2
LCD_CONTRAST
ADC_VREF
93C46
ALTERA
MAX 10
10M25SAE144C8G
E BABA21925A
IC10
8K
25K
VREF2
Supported By:
Wadhwani Electronics Lab, IIT Bombay,
NPTEL,Intel
Designed By:
Vidur Shah,
Mahesh Bhaganagre,
Maheshwar Mangat,
Amit Shetye
PWR_SEL
EXT
USB
EXT_PLED
ON
POWER
VCC_ONE
GND
+3V3
EXT_CLK
RN2
RN3
ON
DIP
1 2 3 4 5 6 7 8


Xen10
16X2 LCD
OLED
JP5
JP2
REF_GND
LCD_CONTRAST
ADC_VREF
93C46
XTAL
ALTERA
MAX 10
10M25SAE144C8G
E BABAZ1925A
IC8
IC10
IC6
8K
25K
VREF2
VCCIO_CLK
VCCIO_1B
VCCIO_1A
FT2232_PLED
VCC_ALL_PLED
+3V3_PLED
EXT_PLED
PWR_SEL
EXT_PWR
USB2.0
ON
POWER
VCC_ONE
RN2
RN3
DIP
Supported By:
Wadhuani Electronics Lab, IIT Bomba
NPTEL,Intel
Designed By:
Vidur Shah,
Mahesh Bhaganagre,
Maheshwar Mangat,
Amit Shetye


Xen10
U1.2
Ex. LCD
OLED
JP5
JP2
LCD_CONTRAST
ADC_VREF
93C46
MAX 10
10M25SAE144C8G
E BABA21925A
8K
25K
VREF2
Supported By:
Wadhwani Electronics Lab, IIT Bombay,
NPTEL,Intel
Designed By:
Vidur Shah,
Mahesh Bhaganagre,
Maheshwar Mangat,
Amit Shetye
PWR_SEL
EXT
USB
EXT_PLED
ON
POWER
VCC_ONE
GND
EXT_CLK
DIP
1 2 3 4 5 6 7 8


Xen10
16 ← 1ext. LCD → 1
JP5
JP2
OLED
LCD_CONTRAST
REF_GND
ADC_VREF
93C46
MAX 10
8K
25K
Supported By
Wadhwani Electronics Lab, IIT Bombay,
NPTEL,Intel
Designed By
Vidur Shah,
Mahesh Bhaganagre,
Maheshwar Mangat,
Amit Shahu
PWR_SEL
USB
EXT
ON
POWER
DIP
ON
1 2 3 4 5 6 7 8

In this experiment, we successfully implemented a traffic signal simulation using inbuilt LED on XEN10 board.