

1. Write down main features of 8085 microprocessor.

- It is an 8 bit microprocessor.
- It is manufactured with N-MOS technology.
- It has 16-bit address bus and hence can address up to $2^{16} = 65536$ bytes (64KB) memory locations through A0-A15
- The first 8 lines of address bus and 8 lines of data bus are multiplexed AD0 – AD7
- Data bus is a group of 8 lines D0 – D7
- It supports external interrupt request. .
- A 16 bit program counters (PC)
- A 16 bit stack pointer (SP)
- Six 8-bit general purpose register arranged in pairs: BC, DE, HL.
- It requires a signal +5V power supply and operates at 3.2 MHZ single phase clock.
- It is enclosed with 40 pins DIP (Dual in line package).

2. Explain 8085 microprocessor architecture.

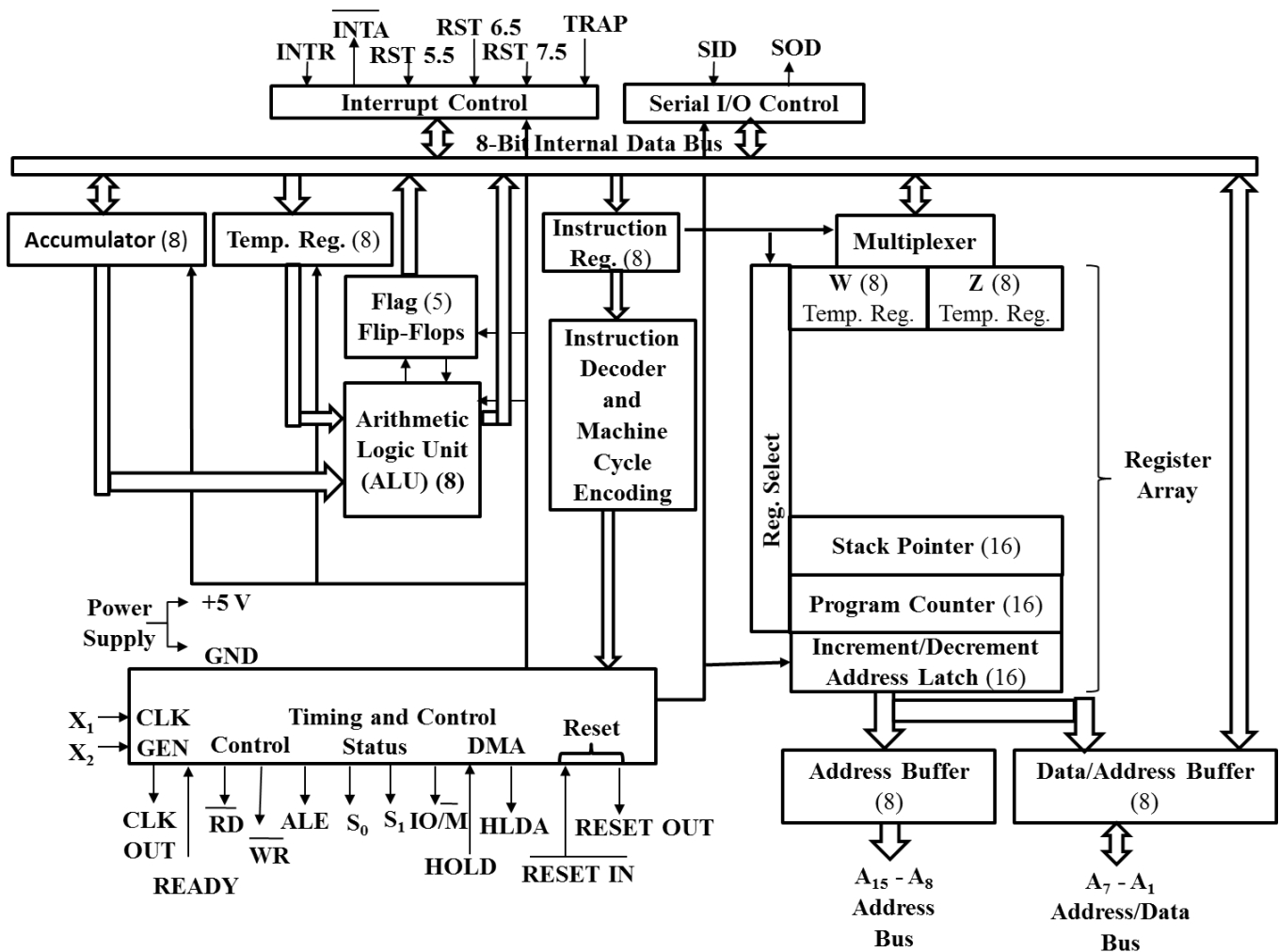


Figure: 8085 microprocessor architecture.

The architecture of microprocessor 8085 can be divided into seven parts as follows:

Register Unit:

General Purpose Data Register

- 8085 has six general purpose data registers to store 8-bit data.
- These registers are named as B, C, D, E, H and L as shown in fig. 1.
- The user can use these registers to store or copy a data temporarily during the execution of a program by using data transfer instructions.
- These registers are of 8 bits but whenever the microprocessor has to handle 16-bit data, these registers can be combined as register pairs – BC, DE and HL.
- There are two internal registers – W and X. These registers are only for internal operation like execution of CALL and XCHG instructions and not available to the user.

Program Counter (PC)

- 16-bit register deals with sequencing the execution of instructions.
- This register is a memory pointer.
- Memory locations have 16-bit addresses which are why this is a 16-bit register.
- The microprocessor uses this register to sequence the execution of the instructions.
- The function of the program counter is to point to the memory address from which the next byte is to be fetched.
- When a byte (machine code) is being fetched, the program counter is incremented by one to point to the next memory location.

Stack Pointer (SP)

- SP is also a 16-bit register used as a memory pointer.
- It points to a memory location in R/W memory, called the stack.
- The beginning of the stack is defined by loading 16-bit address in the stack pointer.

MUX/DEMUX unit

- This unit is used to select a register out of all the available registers.
- This unit behaves as a MUX when data is going from the register to the internal data bus.
- It behaves as a DEMUX when data is coming to a register from the internal data bus of the microprocessor.
- The register select will behave as the function selection lines of the MUX/DEMUX.

Address Buffer Register & Data/Address Buffer Register

- These registers hold the address/data, received from PC/internal data bus and then load the external address and data buses.
- These registers actually behave as the buffer stage between the microprocessor and external system buses.

Control Unit:

- The control unit generates signals within microprocessor to carry out the instruction, which has been decoded.
- In reality it causes connections between blocks of the microprocessor to be opened or closed, so that the data goes where it is required and the ALU operations occur.

- The control unit itself consists of three parts; the instruction registers (IR), instruction decoder and machine cycle encoder and timing and control unit.

Instruction Register

- This register holds the machine code of the instruction.
- When microprocessor executes a program it reads the opcode from the memory, this opcode is stored in the instruction register.

Instruction Decoder & Machine Cycle Encoder

- The IR sends the machine code to this unit.
- This unit, as its name suggests, decodes the opcode and finds out what is to be done in response of the coming opcode and how many machine cycles are required to execute this instruction.

Timing & Control unit

- The control unit generates signals within microprocessor to carry out the instruction, which has been decoded.
- In reality, it causes certain connections between blocks of the microprocessor to be opened or closed, so that the data goes where it is required and the ALU operations occur.

Arithmetic & Logical Unit:

- The ALU performs the actual numerical and logical operation such as 'add', 'subtract', 'AND', 'OR', etc.
- ALU uses data from memory and from accumulator to perform the arithmetic operations and always stores the result of the operation in accumulator.
- ALU consists of accumulator, flag register and temporary register.

Accumulator

- The accumulator is an 8-bit register that is a part of ALU.
- This register is used to store 8-bit data and perform arithmetical and logical operations.
- The result of an operation is stored in the accumulator.
- It is also identified as register A.

Flags register

- Flag register includes five flip-flops, which are set or reset after an operation according to the data conditions of the result in the accumulator and other registers.
- They are called zero (Z), carry (CY), sign (S), parity (P) and auxiliary carry (AC) flags; their bit positions in the flag register are shown in fig.
- The microprocessor uses these flags to set and test data conditions.

Interrupt Control

- The interrupt control unit has 5 interrupt inputs TRAP, RST 7.5, RST 6.5, RST 5.5 & INTR and one acknowledge signal INTA.
- It controls the interrupt activity of 8085 microprocessor.

Serial IO control

- 8085 serial IO control provides two lines, SOD and SID for serial communication.

- The serial output data (SOD) line is used to send data serially and serial input data line (SID) is used to receive data serially.

3. Explain Flags Registers in 8085

- Flag register includes five flip-flops, which are set or reset after an operation according to the data conditions of the result in the accumulator and other registers.
- They are called zero (Z), carry (CY), sign (S), parity (P) and auxiliary carry (AC) flags; their bit positions in the flag register are shown in fig.
- The microprocessor uses these flags to set and test data conditions.

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
S	Z		AC		P		CY

Figure: Flags registers in 8085.

- The flags are stored in the 8-bit register so that the programmer can examine these flags by accessing the register through an instruction.
- These flags have critical importance in the decision-making process of the microprocessor.
- The conditions (set or reset) of the flags are tested through the software instructions.
- For instance, JC (jump on carry) is implemented to change the sequence of a program when CY flag is set.

Z (Zero) Flag:

- This flag indicates whether the result of mathematical or logical operation is zero or not.
- If the result of the current operation is zero, then this flag will be set, otherwise reset.

CY (Carry) Flag:

- This flag indicates, whether, during an addition or subtraction operation, carry or borrow is generated or not, if generated then this flag bit will be set.

AC (Auxiliary Carry) Flag:

- It shows carry propagation from D3 position to D4 position.

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	1	1	0	0
0	0	1	0	1	0	1	1
1	0	1	1	0	1	1	1

Figure: Auxiliary Carry.

- As shown in the fig., a carry is generated from D3 bit position and propagates to the D4 position. This carry is called auxiliary carry.

S (Sign) Flag:

- Sign flag indicates whether the result of a mathematical operation is negative or positive.
- If the result is positive, then this flag will reset and if the result is negative this flag will be set.
- This bit, in fact, is a replica of the D7 bit.

P (Parity) Flag:

- Parity is the number of 1's in a number.
- If the number of 1's in a number is even then that number is known as even parity number.
- If the number of 1's in a number is odd then that number is known as an odd parity number.
- This flag indicates whether the current result is of even parity (set) or of odd parity (reset).

4. Explain 8085 pin diagram.

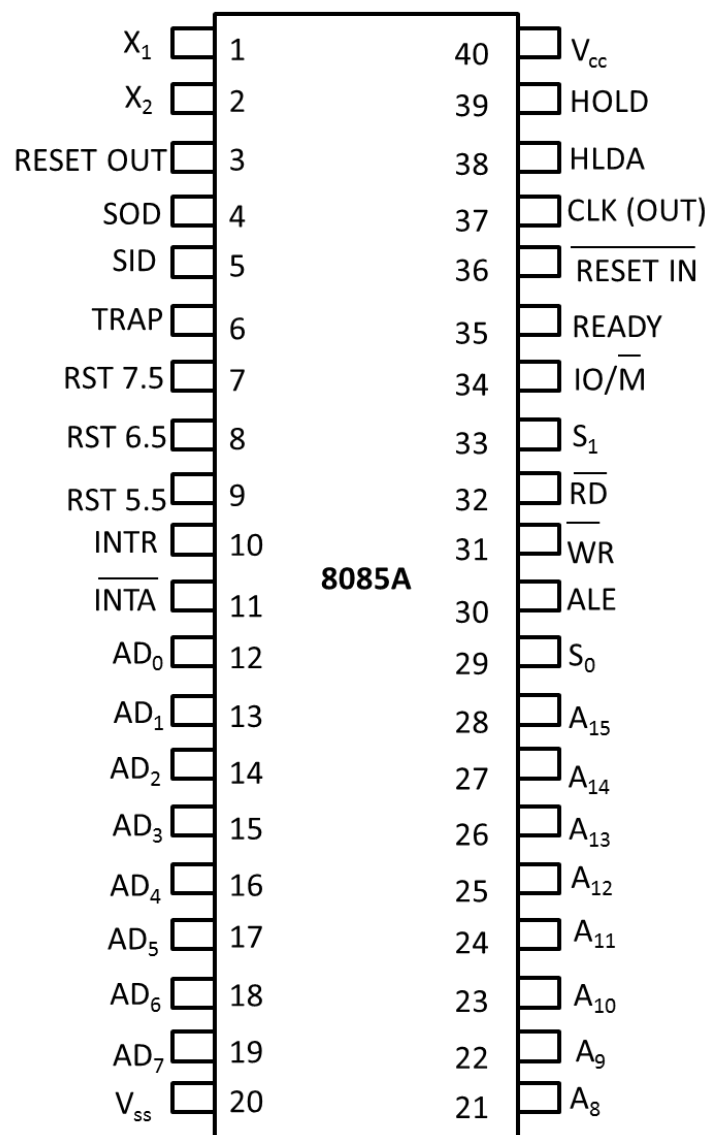


Figure: 8085 pin diagram.

- All signals can be classified into six groups:

1. Address Bus
2. Data Bus
3. Control & Status Signals
4. Power Supply & Frequency signals
5. Externally initiated signals
6. Serial I/O Ports

1) Address Bus (pin 12 to 28)

- 16 signal lines are used as address bus.
- However these lines are split into two segments: $A_{15} - A_8$ and $AD_7 - AD_0$
- $A_{15} - A_8$ are unidirectional and are used to carry high-order address of 16-bit address.
- $AD_7 - AD_0$ are used for dual purpose.

2) Data Bus/ Multiplexed Address (pin 12 to 19)

- Signal lines $AD_7 - AD_0$ are bidirectional and serve dual purpose.
- They are used as low-order address bus as well as data bus.
- The low order address bus can be separate from these signals by using a latch.

3) Control & Status Signals

- To identify nature of operation
- Two Control Signals
 - 1) RD' (Read-pin 32)
 - ✓ This is a read control signal (active low)
 - ✓ This signal indicates that the selected I/O or Memory device is to be read & data are available on data bus.
 - 2) WR' (Write-pin 31)
 - ✓ This is a write control signal (active low)
 - ✓ This signal indicates that the selected I/O or Memory device is to be write.
- Three Status Signals
 - 1) S_1 (pin 33)
 - 2) S_0 (pin 29)
 - ✓ S_1 and S_0 status signals can identify various operations, but they are rarely used in small systems.

S_1	S_0	Mode
0	0	HLT
0	1	WRITE
1	0	READ
1	1	OPCODE FETCH

- 3) IO/M' (pin 34)
 - ✓ This is a status signal used to differentiate I/O and memory operation
 - ✓ When it is high, it indicates an I/O operation
 - ✓ When it is low, it indicates a memory operation
 - ✓ This signal is combined with RD' and WR' to generate I/O & memory control signals
- To indicate beginning of operation
 - One Special Signal called ALE (Address Latch Enable-Pin 30)

- This is positive going pulse generated every time the 8085 begins an operation (machine cycle)
- It indicates that the bits on AD7-AD0 are address bits
- This signal is used primarily to latch the low-address from multiplexed bus & generate a separate set of address lines A7-A0.

4) Power Supply & Frequency Signal

- V_{cc} → Pin no. 40, +5V Supply
- V_{ss} → Pin no.20, Ground Reference
- X1, X2 → Pin no.1 & 2, Crystal Oscillator is connected at these two pins. The frequency is internally divided by two;
 - Therefore, to operate a system at 3MHz, the crystal should have a frequency of 6MHz.
- CLK (OUT) → Clock output. Pin No.37: This signal can be used as the system clock for other devices.

5) Externally Initiated Signals including Interrupts

- INTR (Input) → Interrupt Request. It is used as general purpose interrupt
- INTA' (Output) → Interrupt Acknowledge. It is used to acknowledge an interrupt.
- RST7.5, RST6.5, RST5.5 (Input) → Restart Interrupts.
 - These are vector interrupts that transfer the program control to specific memory locations.
 - They have higher priorities than INTR interrupt.
 - Among these 3 interrupts, the priority order is RST7.5, RST6.5, RST5.5
- TRAP (Input) → This is a non maskable interrupt & has the highest priority.
- HOLD (Input) → This signal indicates that a peripheral such as DMA Controller is requesting the use of address & data buses
- HLDA (Output) → Hold Acknowledge. This signal acknowledges the HOLD request
- READY (Input) → This signal is used to delay the microprocessor read or write cycles until a low-responding peripheral is ready to send or accept data. When the signal goes low, the microprocessor waits for an integral no. of clock cycles until it goes high.
- RESET IN' (Input) → When the signal on this pin goes low, the Program Counter is set to zero, the buses are tri-stated & microprocessor is reset.
- RESET OUT (Output) → This signal indicates that microprocessor is being reset. The signal can be used to reset other devices.

6) Serial I/O Ports

- Two pins for serial transmission
 - 1) SID (Serial Input Data-pin 5)
 - 2) SOD (Serial Output Data-pin 4)
- In serial transmission, data bits are sent over a single line, one bit at a time.

5. Explain Instruction Cycle

- Instruction Cycle is defined as time required to complete execution of an instruction.
- 8085 instruction cycle consists of 1 to 6 Machine Cycles or 1 to 6 operations.

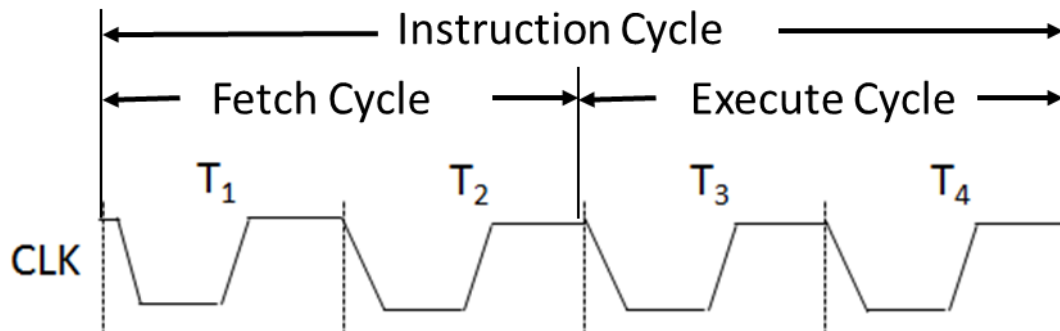


Figure: Instruction Cycle.

6. Explain Machine Cycle

- Machine Cycle is defined as time required by the microprocessor to complete operation of accessing memory device or I/O device.
- This cycle may consist 3 to 6 T-states.
- The basic microprocessor operation such as reading a byte from I/O port or writing a byte to memory is called as machine cycle.

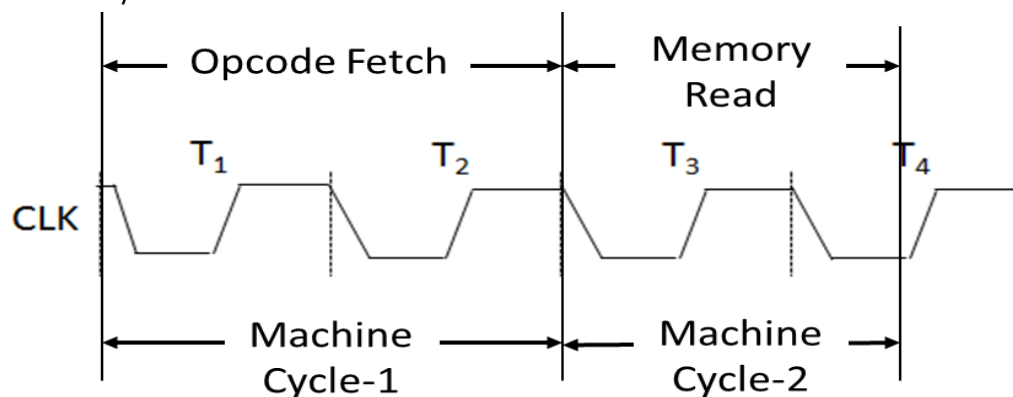


Figure: Machine Cycle.

7. Explain T-States

- T-States are defined as one subdivision of operation performed in one clock period.
- These sub divisions are internal states synchronized with system clock & each T-state is precisely equal to one clock period.

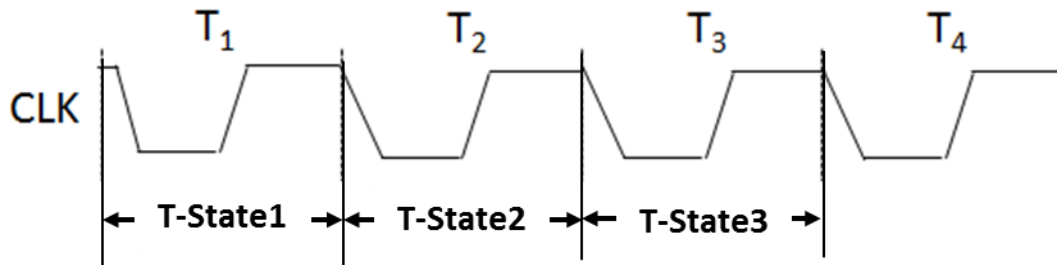


Figure: T-States.

8. Compare Instruction Cycle, Machine Cycle and T-States

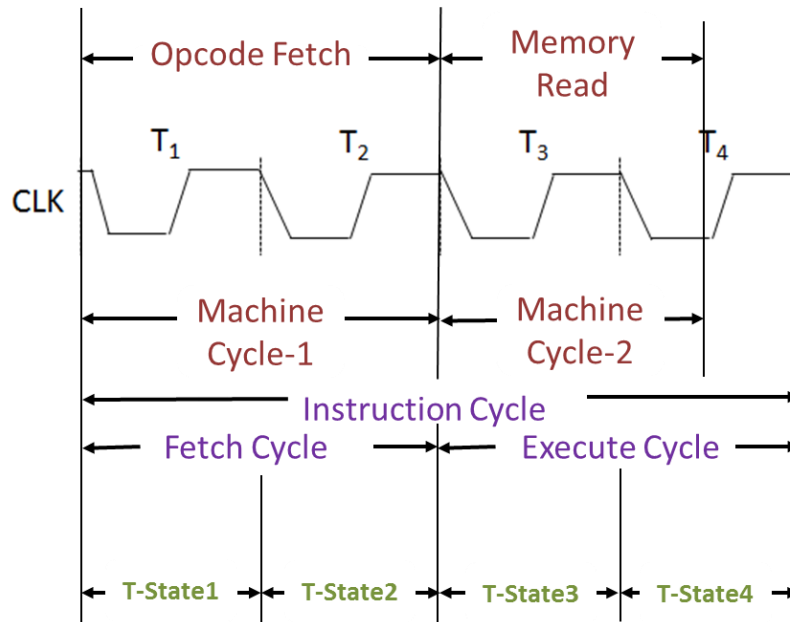


Figure: Comparison between Instruction Cycle, Machine Cycle and T-States.

- Instruction Cycle: Time required to complete execution of an instruction.
- Machine Cycle: Time required by the microprocessor to complete an operation.
- T-States: One subdivision of operation performed in one clock period.

9. Explain 8085 Programming Model

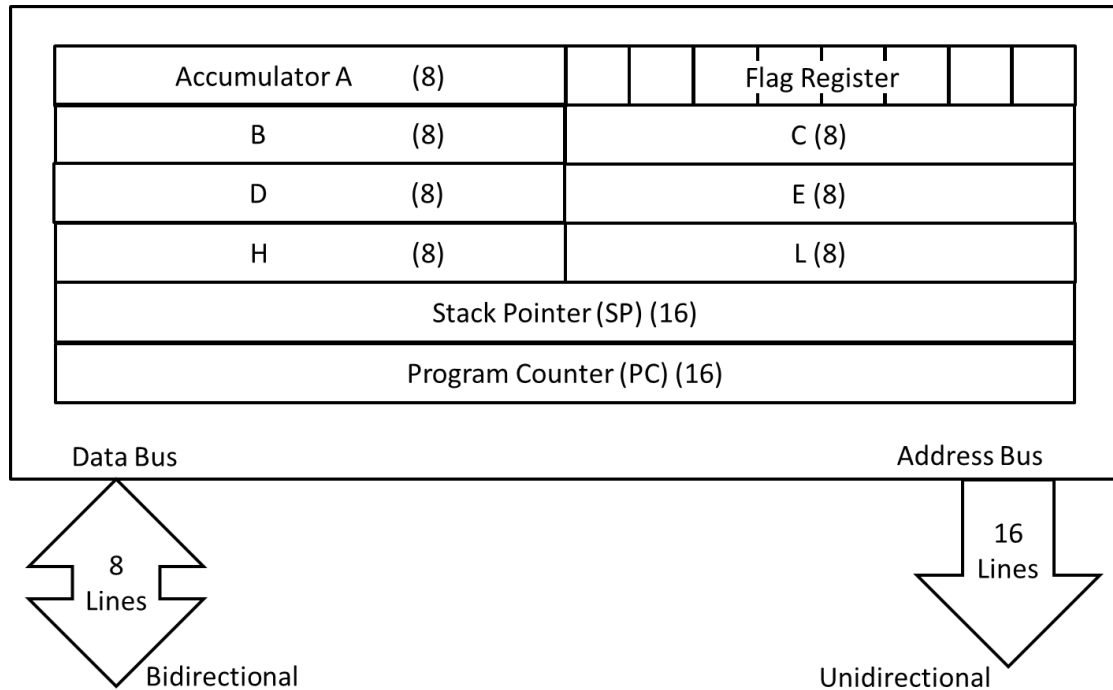


Figure: 8085 Programming Model.

Registers

- 6 general purpose registers to store 8-bit data B, C, D, E, H & L.
- Can be combined as register pairs – BC, DE, and HL to perform 16-bit operations.
- Used to store or copy data using data copy instructions.

Accumulator

- 8 - bit register, identified as A
- Part of ALU
- Used to store 8-bit data to perform arithmetic & logical operations.
- Result of operation is stored in it.

Flag Register

- ALU has 5 Flag Register that set/reset after an operation according to data conditions of the result in accumulator & other registers.
- Helpful in decision making process of Microprocessor
- Conditions are tested through software instructions
- For e.g.
- JC (Jump on Carry) is implemented to change the sequence of program when CY is set.

Program Counter

- 16-bit registers used to hold memory addresses.
- Size is 16-bits because memory addresses are of 16-bits.

- Microprocessor uses PC register to sequence the execution of instructions.
- Its function is to point to memory address from which next byte is to be fetched.
- When a byte is being fetched, PC is incremented by 1 to point to next memory location.

Stack Pointer

- Used as memory pointer
- Points to the memory location in R/W memory, called Stack.
- Beginning of stack is defined by loading a 16-bit address in the stack pointer.

10. Explain Bus Organization of 8085

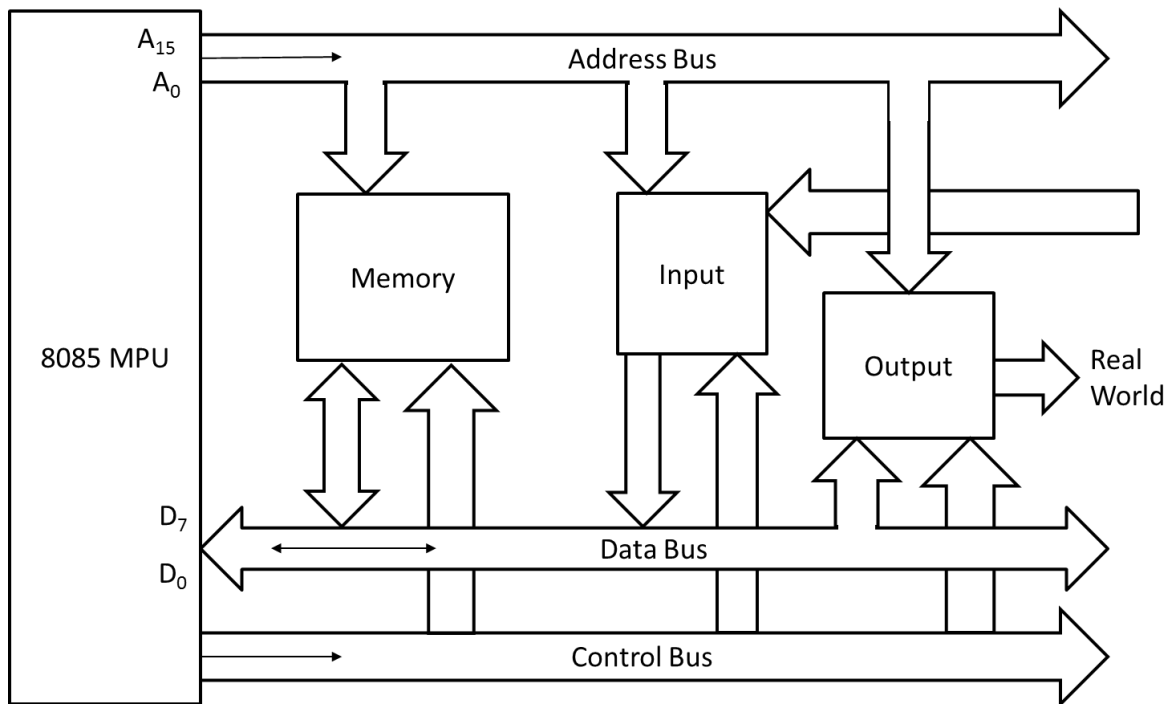


Figure: Bus Organization of 8085.

Address Bus

- Group of 16 lines generally identified as A₀ to A₁₅.
- It is unidirectional i.e. bits flow from microprocessor to peripheral devices.
- 16 address lines are capable of addressing 65536 memory locations.
- So, 8085 has 64K memory locations.

Data Bus

- Group of 8 lines identified as D₀ to D₇.
- They are bidirectional i.e. data flow in both directions between microprocessor, memory & peripheral.
- 8 data lines enable microprocessor to manipulate data ranging from 00H to FFH (28=256 numbers).
- Largest number appear on data bus is 1111 1111 => (255)₁₀.
- As Data bus is of 8-bit, 8085 is known as 8-bit Microprocessor.

Control Bus

- It comprises of various single lines that carry synchronization, timing & control signals.

- These signals are used to identify a device type with which MPU intends to communicate.

11. Explain Demultiplexing AD0-AD7

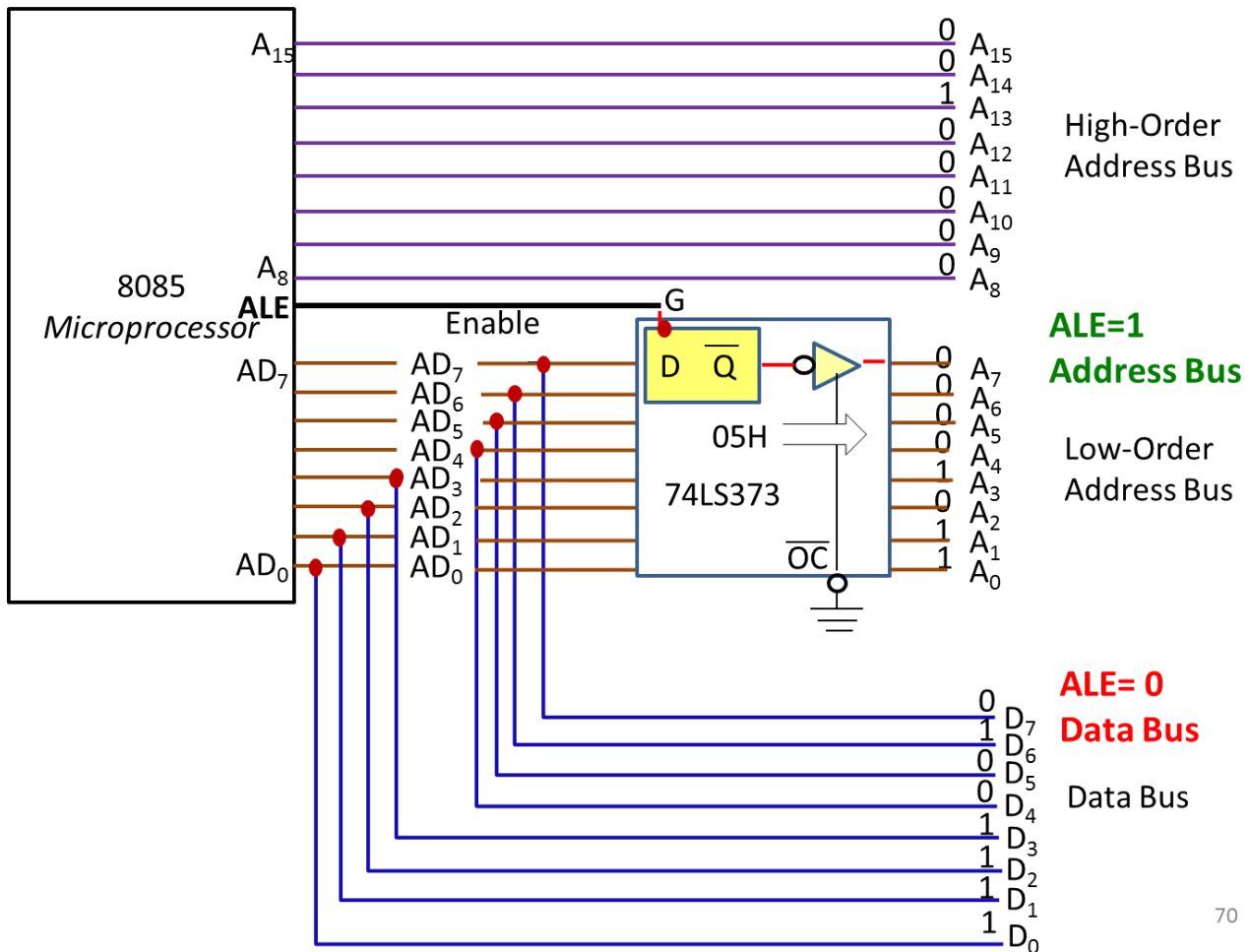


Figure: Demultiplexing AD0-AD7.

- The higher-order bus remains on the bus for three clock periods. However, the low-order address is lost after the first clock period.
- This address need to be latched and used for identifying the memory address. If the bus AD7-AD0 is used to identify the memory location (2005H), the address will change to 204FH after the first clock period.
- Figure shows a schematic that uses a latch and the ALE signal to demultiplex the bus.
- The bus AD7-AD0 is connected as the input to the latch.
- The ALE signal is connected to the Enable pin of the latch, and the output control signal of the latch is grounded.
- Figure shows that the ALE goes high during T1. And during T1 address of lower-order address bus is store into the latch.

12. Explain Memory Interfacing

- When we are executing any instruction, we need the microprocessor to access the memory for reading instruction codes and the data stored in the memory.
- For this, both the memory and the microprocessor requires some signals to read/write to/from registers.
- The interfacing circuit therefore should be designed in such a way that it matches the memory signal requirements with the signals of the microprocessor.

Memory Read Cycle

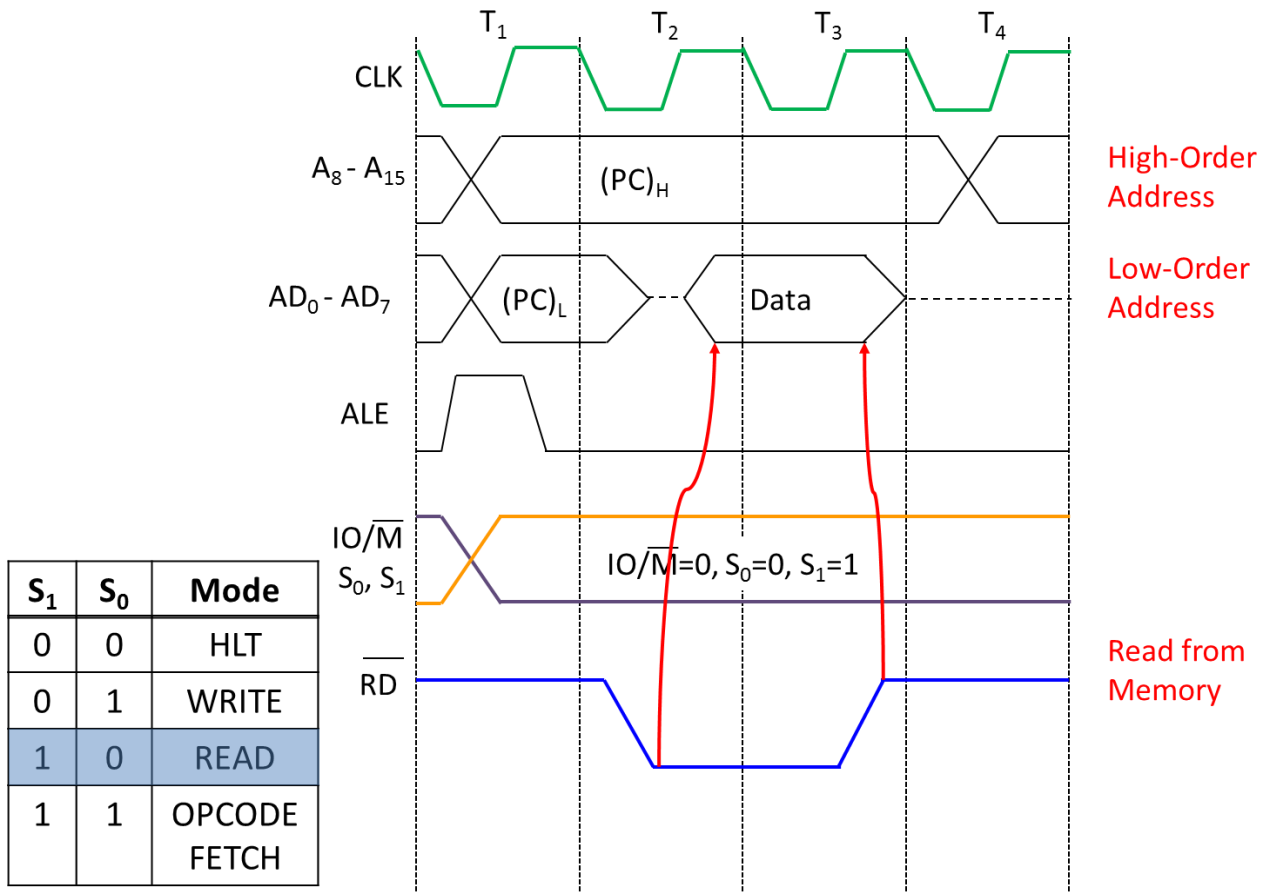


Figure: Memory Read Cycle.

- It is used to fetch one byte from the memory.
- It requires 3 T-States.
- It can be used to fetch operand or data from the memory.
- During T₁, A₈-A₁₅ contains higher byte of address. At the same time ALE is high. Therefore Lower byte of address A₀-A₇ is selected from AD₀-AD₇.
- Since it is memory ready operation, IO/ \overline{M} (bar) goes low.
- During T₂ ALE goes low, RD (bar) goes low. Address is removed from AD₀-AD₇ and data D₀-D₇ appears on AD₀-AD₇.
- During T₃, Data remains on AD₀-AD₇ till RD (bar) is at low signal.

Memory Write Cycle

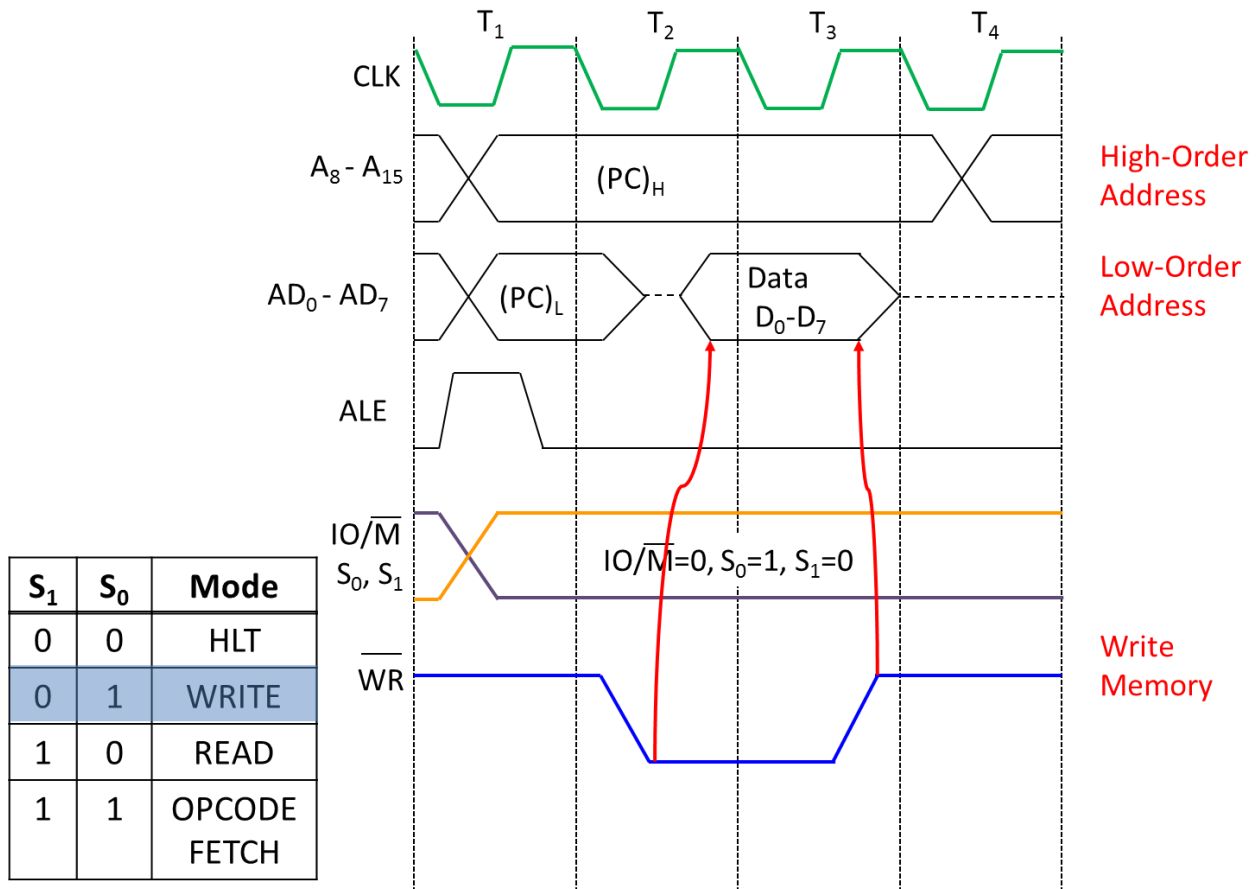


Figure: Memory Write Cycle.

- It is used to send one byte into memory.
- It requires 3 T-States.
- During T1, ALE is high and contains lower address A0-A7 from AD0-AD7.
- A8-A15 contains higher byte of address.
- As it is memory operation, IO/M (bar) goes low.
- During T2, ALE goes low, WR (bar) goes low and Address is removed from AD0-AD7 and then data appears on AD0-AD7.
- Data remains on AD0-AD7 till WR (bar) is low.

13. Explain how Control Signals Generated in 8085

Operation	IO/M'	RD'	WR'
MEMR'	0	0	X
MEMW'	0	X	0
IOR'	1	0	X
IOW'	1	X	0

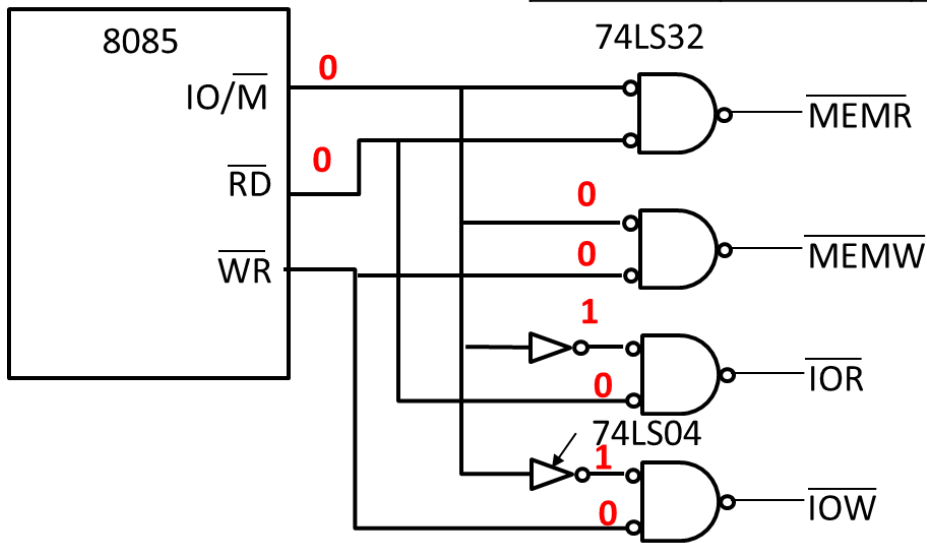


Figure: Control Signals Generated in 8085.

- Figure shows that four different control signals are generated by combining the signals RD (bar), WR (bar), and IO/M (bar).
- The signal IO/M (bar) goes low for the memory operation. This signal is ANDed with RD (bar) and WR (bar) signals using the 74LS32 quadruple two-input OR gates, as shown in figure 4.5.
- The OR gates are functionally connected as negative NAND gates. When both input signals go low, the output of the gates goes low and generates MEMR (bar) and MEMW (bar) control signals.
- When the IO/M (bar) signal goes high, it indicates the peripheral I/O operation.
- Figure shows that this signal is complemented using the Hex inverter 74LS04 and ANDed with the RD (bar) and WR (bar) signals to generate IOR (bar) and IOW (bar) control signals.