

# Computer Organization and Architecture

Grp: 82

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## Instruction class format and instruction encoding

### 1. TR- Instruction :

Op Code (5 bit)	rs (5 bit)	rt (5 bit)	DC (13 bit)	Func (4 bit)
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Op Code	Instruction	Function code
00001	Add	0000
00001	Comp	0001
00001	Shift left logical variable	0010
00001	Shift right logical variable	0011
00001	Shift right arithmetic variable	0100
00001	AND	0101
00001	XOR	0110
00001	Diff	0111

### 2. RI- Instruction :

Op Code (5 bit)	rs (5 bit)	Immidiata val (18 bit)	Func (4 bit)
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Op Code	Instruction	Function code
00010	Add immediate	0000
00010	Comp immediate	0001
00010	Shift left logical	0010
00010	Shift right logical	0011
00010	Shift right arithmetic	0100

### 3. M- Instruction :

Op Code (5 bit)	rs (5 bit)	rt (5 bit)	Offset (16 bit)	Func (1 bit)
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Op Code	Instruction	Function code
00100	Load Word	0
00100	Store Word	1

### 4. B- Instruction :

Op Code (5 bit)	Address (23 bit)	Func (4 bit)
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Op Code	Instruction	Function code
01000	Unconditional branch	0000
01000	Branch Register	0001
01000	Branch and link	0010
01000	Branch on Carry	0011
01000	Branch on No Carry	0100

### 5. BR- Instruction :

Op Code (5 bit)	rs (5 bit)	Address (19 bit)	Func (3 bit)
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Op Code	Instruction	Function code
10000	Branch on less than 0	000
10000	Branch on flag zero	001
10000	Branch on flag not zero	010

## Truth Table for Control Unit

Ins[31:27]	Ins[1:0]	Branch Control Signal	Sign Extension Control	ALU operation	ALU source	Memory Read	Memory Write	Register Write
00001	XX	00	0000	0001	0	X	X	XX1
00010	XX	00	0001	0010	1	X	X	XX1
00100	X0	00	0010	0100	1	1	0	X10
00100	X1	00	0010	0100	1	0	1	X00
01000	0X	01	0100	0000	0	X	X	0X0
01000	1X	01	0100	0000	0	X	X	1X0
10000	X	10	1000	1000	0	X	X	XX0

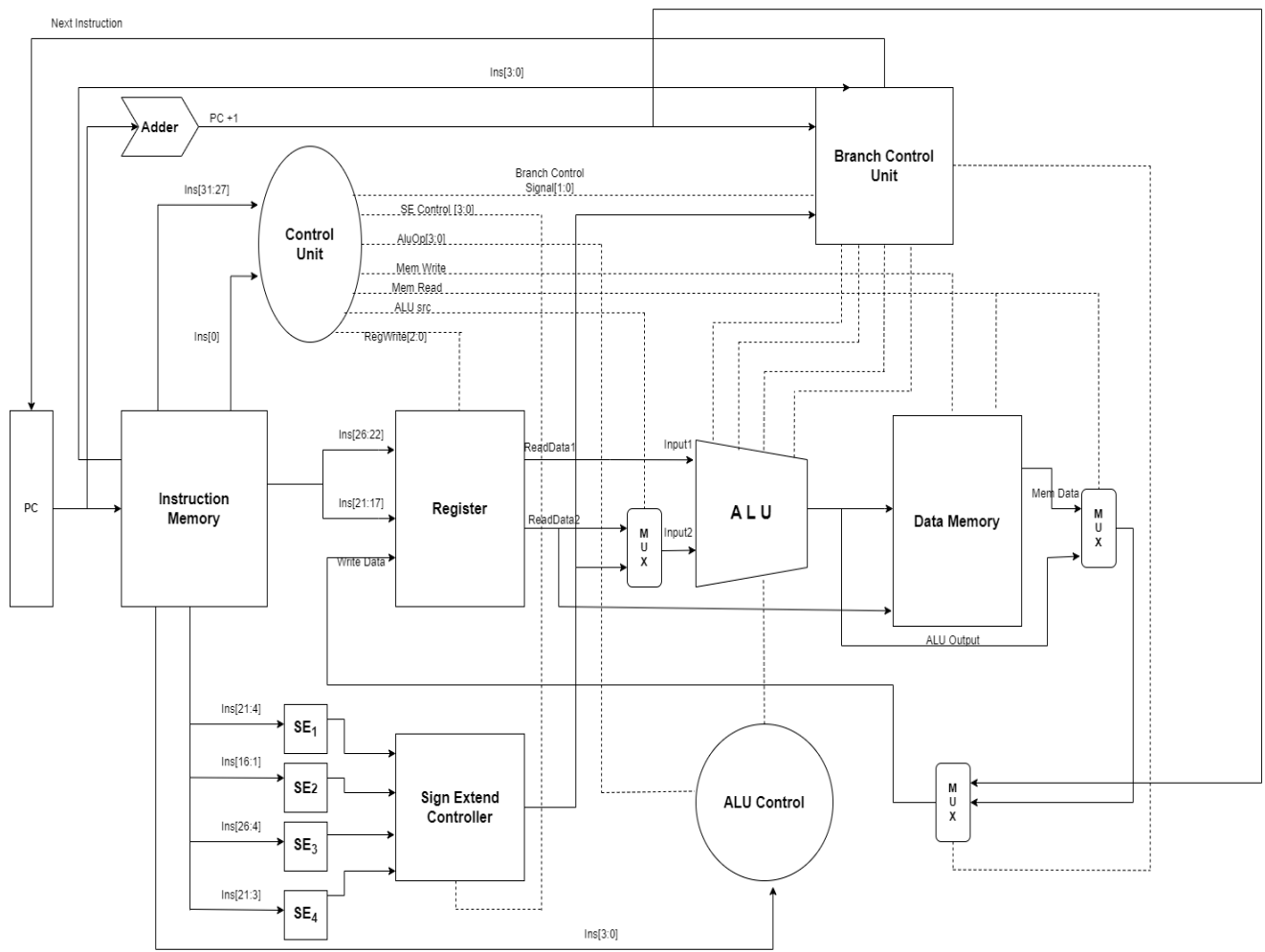
Truth Table for Control Unit

Here Ins[31:27] is the opcode

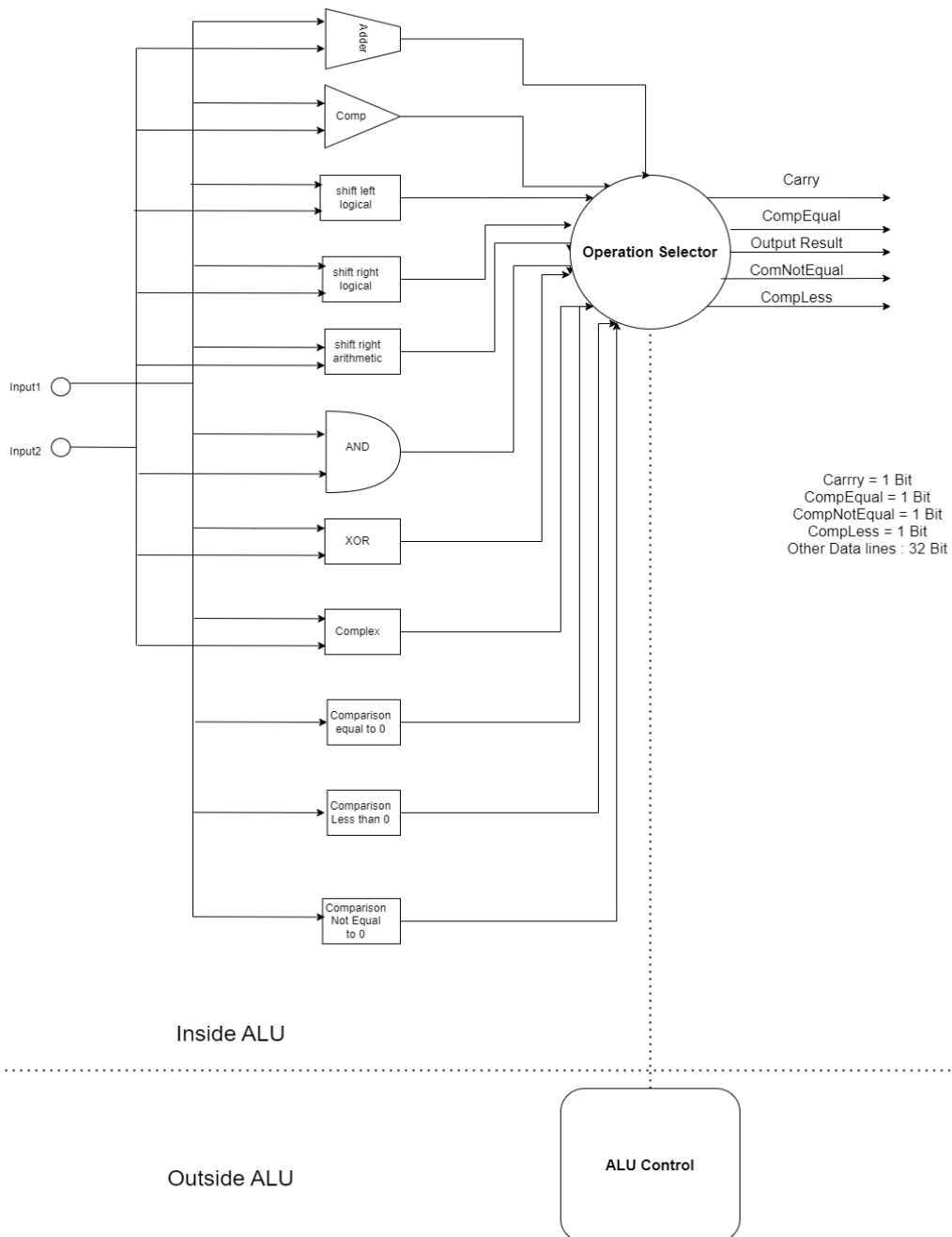
Ins[1:0] are the last two bits of function code

The X denotes don't care signals which are zero by default

# miniRISC Architecture Diagram



# ALU Datapath Diagram



[Google Drive Link to the ISE Project](#)