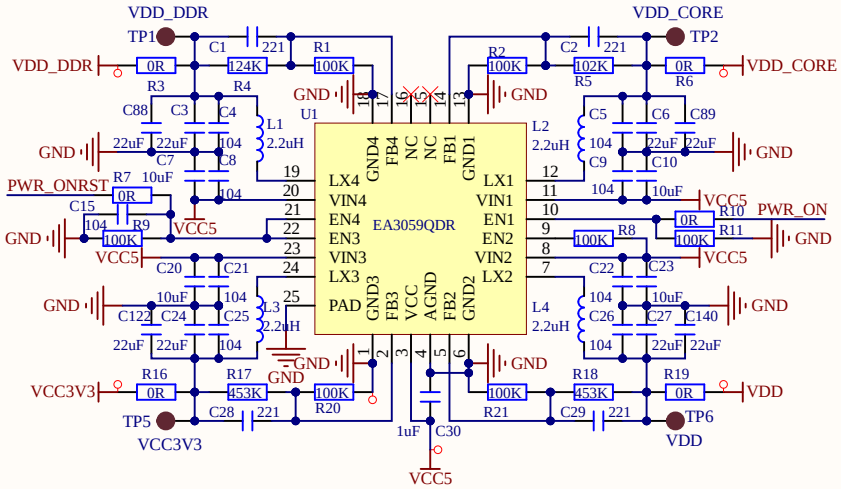
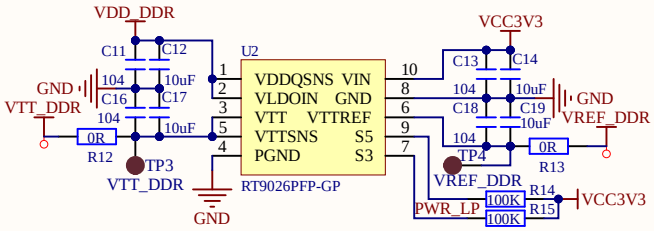
VDD_DDR=1.345V VDD_CORE=1.212V
VCC3V3=3.31V VDD=3.31V



VTT_DDR=1.35/2=0.67V
VREF_DDR=1.35/2=0.67V



Title: PMIC_POWER.SchDoc		
Project: ATK-CLMP157B_V1.4.PrjPcb		
Size: A4	Author: lycreturn@ALIENTEK	
Date: 2021/6/9	Version: V1.0	Sheet: 1 of 10

正点原子

Title: STM32MP157_ABC.SchDoc		
Project: ATK-CLMP157B_V1.4.PrjPcb		
Size: A4	Author: lycreturn@ALIENTEK	
Date: 2021/6/9	Version: V1.0	Sheet: 2 of 10

正点原子

U3B

NAND_D2	PD0	C10
NAND_D3	PD1	B10
SDMMC1_CMD	PD2	D12
SDMMC2_D7	PD3	B11
NAND_NOE	PD4	C9
NAND_NWE	PD5	A9
NAND_NWAIT	PD6	L3
SDMMC3_D3	PD7	F10
USART3_TX	PD8	M1
USART3_RX	PD9	M2
uSD_DETECT	PD10	A8
NAND_CLE	PD11	AB9
NAND_ALE	PD12	W12
LCD_BL	PD13	V14
NAND_D0	PD14	M3
NAND_D1	PD15	L1
SAI2_MCLKA	PE0	C5
DCMI_RESET	PE1	D7
ETH_TXD3	PE2	Y2
SDMMC2_CK	PE3	A10
SDMMC1_CKIN	PE4	F15
SDMMC2_D6	PE5	C12
DCMI_D7	PE6	E9
NAND_D4	PE7	W10
NAND_D5	PE8	Y12
NAND_D6	PE9	W11
NAND_D7	PE10	W14
DCMI_PWDN	PE11	D5
SAI2_SCKB	PE12	E4
SAI2_FSB	PE13	A4
SAI2_MCLKB	PE14	B4
T_MISO	PE15	C4
SDMMC3_D0	PF0	E10
SDMMC3_CMD	PF1	B9
SDMMC1_D0DIR	PF2	F13
	PF3	V3
SDMMC3_D1	PF4	F9
SDMMC3_D2	PF5	D9
QSPI_BK1_IO3	PF6	AA11
QSPI_BK1_IO2	PF7	AA10
QSPI_BK1_IO0	PF8	AB10
QSPI_BK1_IO1	PF9	AB11
QSPI_CLK	PF10	V12
SAI2_SDB	PF11	W8
	PF12	V8
	PF13	W7
	PF14	V7
	PF15	W6

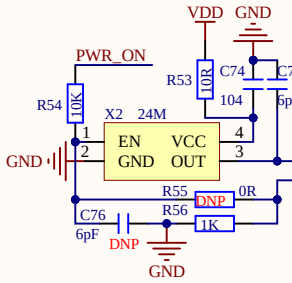
PD0/I2C6_I2C5_SDA/DFSDM1_CKIN6/SAI3_SCK_A/UART4_RX/FDCAN1_RX/SDMMC3_CMD/DFSDM1_DATIN7/FMC_D2/FMC_DA2
PD1/I2C6_I2C5_SCL/DFSDM1_DATIN6/SAI3_SD_A/UART4_TX/FDCAN1_TX/SDMMC3_D0/DFSDM1_CKIN7/FMC_D3/FMC_DA3
PD2/TIM3_ETR/I2C5_SMBA/UART4_RX/UART5_RX/SDMMC1_CMD/DCMI_D11
PD3/HDP5/DFSDM1_CKOUT/SPI2_SCK/I2S2_CK/DFSDM1_DATIN0/UART2_CTS_NSS/SDMMC1_SDMMC2_D123DIR/SDMMC1_SDMMC2_D7/FMC_CLK/DCMI_D5/LCD_G7
PD4/SAI3_FS_A/USART2_RTS_DE/SDMMC3_D1/DFSDM1_CKIN0/FMC_NOE
PD5/USART2_TX/SDMMC3_D2/FMC_NWE
PD6/TIM16_CH1N/SAI1_D1/DFSDM1_CKIN4_DATIN1/SPI3_MOSI/I2S3_SDO/SAI1_SD_A/USART2_RX/FMC_NWAIT/DCMI_D10/LCD_B2
PD7/DFSDM1_DATIN4_CKIN1/I2C2_SCL/USART2_CK/SPDIFRX_IN0/SDMMC3_D3/FMC_NE1
PD8/DFSDM1_CKIN3/SAI3_SCK_B/USART3_TX/SPDIFRX_IN1/FMC_D13/FMC_DA13/LCD_B7
PD9/DFSDM1_DATIN3/SAI3_SD_B/USART3_RX/FMC_D14/FMC_DA14/DCMI_HSYNC/LCD_B0
PD10/RTC_REFIN/TIM16_BKIN/DFSDM1_CKOUT/I2C5_SMBA/SPI3_MISO/I2S3_SDI/SAI3_FS_B/USART3_CK/FMC_D15/FMC_DA15/LCD_B3
PD11/LPTIM2_IN2/I2C4_I2C1_SMBA/USART3_CTS_NSS/QUADSPI_BK1_IO0/SAI2_SD_A/FMC_CLE/FMC_A16
PD12/LPTIM1_LPTIM2_IN1/TIM4_CH1/I2C4_I2C1_SCL/USART3_RTS_DE/QUADSPI_BK1_IO1/SAI2_FS_A/FMC_ALE/FMC_A17
PD13/LPTIM1_OUT/TIM4_CH2/I2C4_I2C1_SDA/I2S3_MCK/QUADSPI_BK1_IO3/SAI2_SCK_A/FMC_A18
PD14/TIM4_CH3/SAI3_MCLK_B/UART8_CTS/FMC_D0/FMC_DA0
PD15/TIM4_CH4/SAI3_MCLK_A/UART8_CTS/FMC_D1/FMC_DA1/LCD_R1

PE0/LPTIM1_LPTIM2_ETR/TIM4_ETR/SPI3_SCK/I2S3_CK/SAI4_MCLK_B/UART8_RX/SAI2_MCLK_A/FMC_NBL0/DCMI_D2
PE1/LPTIM1_IN2/I2S2_MCK/SAI3_SD_B/UART8_TX/FMC_NBL1/DCMI_D3
PE2/SAI1_CK1/I2C4_SCL/SPI4_SCK/SAI1_MCLK_A/QUADSPI_BK1_IO2/ETH1_GMII_MII_RGMII_TXD3/FMC_A23
PE3/TIM15_BKIN/SAI1_SD_B/SDMMC2_CK/FMC_A19
PE4/SAI1_D2/DFSDM1_DATIN3/TIM15_CH1N/SPI4_NSS/SAI1_FS_A/SDMMC1_SDMMC2_CKIN/SDMMC1_SDMMC2_D4/FMC_A20/DCMI_D4/LCD_B0
PE5/SAI1_CK2/DFSDM1_CKIN3/TIM15_CH1/SPI4_MISO/SAI1_SCK_A/SDMMC1_SDMMC2_D0DIR/SDMMC1_SDMMC2_D6/FMC_A21/DMIC_D6/LCD_G0
PE6/TIM1_BKIN2/SAI1_D1/TIM15_CH2/SPI4_MOSI/SAI1_SD_A/SDMMC2_D0/SDMMC1_D2/SAI2_MCLK_B/FMC_A22/DCMI_D7/LCD_G1
PE7/TIM1_TIM3_ETR/DFSDM1_DATIN2/UART7_RX/QUADSPI_BK2_IO0/FMC_D4/FMC_DA4
PE8/TIM1_CH1N/DFSDM1_CKIN2/UART7_TX/QUADSPI_BK2_IO1/FMC_D5/FMC_DA5
PE9/TIM1_CH1/DFSDM1_CKOUT/UART7_RTS_DE/QUADSPI_BK2_IO2/FMC_D6/FMC_DA6
PE10/TIM1_CH2N/DFSDM1_DATIN4/UART7_CTS/QUADSPI_BK2_IO3/FMC_D7/FMC_DA7
PE11/TIM1_CH2/DFSDM1_CKIN4/SPI4_NSS/USART6_CK/SAI2_SD_B/FMC_D8/FMC_DA8/DCMI_D4/LCD_G3
PE12/TIM1_CH3N/DFSDM1_DATIN5/SPI4_SCK/SDMMC1_D0DIR/SAI2_SCK_B/FMC_D9/FMC_DA9/LCD_B4
PE13/HDP2/TIM1_CH3/DFSDM1_CKIN5/SPI4_MISO/SAI2_FS_B/FMC_D10/FMC_DA10/DCMI_D6/LCD_DE
PE14/TIM1_CH4/SPI4_MOSI/UART8_RTS_DE/SAI2_MCLK_B/SDMMC1_D123DIR/FMC_D11/FMC_DA11/LCD_G0/LCD_CLK
PE15/HDP3/TIM1_BKIN/TIM15_BKIN/USART2_CTS_NSS/UART8_CTS/FMC_NCE2/FMC_D12/FMC_DA12/LCD_R7

PF0/I2C2_SDA/SDMMC3_D0_CKIN/FMC_A0
PF1/I2C2_SCL/SDMMC3_CMD_CDIR/FMC_A1
PF2/I2C2_SMBA/SDMMC1_SDMMC2_SDMMC3_D0DIR/FMC_A2
PF3/ETH1_GMII_MII_TX_ER/FMC_A3
PF4/USART2_RX/SDMMC3_D1/SDMMC3_D123DIR/FMC_A4
PF5/USART2_TX/SDMMC3_D2/FMC_A5
PF6/TIM16_CH1/SPI5_NSS/SAI1_SD_B/UART7_RX/QUADSPI_BK1_IO3/SAI4_SCK_B
PF7/TIM17_CH1/SPI5_SCK/SAI1_MCLK_B/UART7_TX/QUADSPI_BK1_IO2
PF8/TIM16_CH1N/SPI5_MISO/SAI1_SCK_B/UART7_RTS_DE/TIM13_CH1/QUADSPI_BK1_IO0
PF9/TIM17_CH1N/SPI5_MOSI/SAI1_FS_B/UART7_CTS/TIM14_CH1/QUADSPI_BK1_IO1
PF10/TIM16_BKIN/SAI1_D3/SAI1_SAI4_D4/QUADSPI_CLK/SAI4_D3/DCMI_D11/LCD_DE
PF11/SPI5_MOSI/SAI2_SD_B/DCMI_D12/LCD_G5/ADC1_INP2
PF12/ETH1_GMII_RXD4/FMC_A6/ADC1_INP6_INN2
PF13/DFSDM1_DATIN6_DATIN3/I2C1_I2C4_SMBA/ETH1_GMII_RXD5/FMC_A7/ADC2_INP2
PF14/DFSDM1_CKIN6/I2C1_I2C4_SCL/ETH1_GMII_RXD6/FMC_A8/ADC2_INP6_INN2
PF15/I2C1_I2C4_SDA/ETH1_GMII_RXD7/FMC_A9

STM32MP175DAA1

Title: STM32MP157_DEF.SchDoc			正点原子
Project: ATK-CLMP157B_V1.4.PrjPcb			
Size: A4	Author: lycreturn@ALIENTEK		
Date: 2021/6/9	Version: V1.0	Sheet: 3 of 10	



U3C

ETH_MDINT	PG0	W5
	PG1	Y4
MCO2	PG2	W4
	PG3	U4
ETH_GTX_CLK	PG4	AB4
ETH_CLK125	PG5	U8
SDMMC2_CMD	PG6	D11
QSPI_BK2_IO3	PG7	Y11
ETH_CLK	PG8	Y8
NAND_NCE	PG9	W15
QSPI_BK2_IO2	PG10	AA9
UART4_TX	PG11	U11
SPDIF_RX	PG12	J4
ETH_TXD0	PG13	AA1
ETH_TXD1	PG14	AA2
SDMMC3_CK	PG15	D10
		T1
		T2
QSPI_BK2_IO0	PH2	AB7
QSPI_BK2_IO1	PH3	Y6
I2C2_SCL	PH4	A3
I2C2_SDA	PH5	A2
	PH6	V11
	PH7	W2
DCMI_HSYNC	PH8	D6
DCMI_D0	PH9	E6
DCMI_D1	PH10	B1
DCMI_D2	PH11	B3
DCMI_D3	PH12	F5
CAN1_TX	PH13	D3
DCMI_D4	PH14	C2
CT_RST	PH15	C1
	PI0	D1
CT_INT	PI1	E2
	PI2	E1
	PI3	E3
DCMI_D5	PI4	J6
SAI2_SCKA	PI5	F2
SAI2_SDA	PI6	G5
SAI2_FSA	PI7	F1
	PI8	N1
CAN1_RX	PI9	J5
ETH_NRST	PI10	W1
MCO1	PI11	T3
LCD_HSYNC	PI12	H2
LCD_VSYNC	PI13	H1
LCD_CLK	PI14	D2
LCD_R0	PI15	F3

PG0/DFSDM1_DATIN0/ETH1_GMII_TXD4/FMC_A10
PG1/ETH1_GMII_TXD5/FMC_A11
PG2/MCO2/TIM8_BKIN/ETH1_GMII_TXD6/FMC_A12
PG3/TIM8_BKIN2/DFSDM1_CKIN1/ETH1_GMII_TXD7/FMC_A13
PG4/TIM1_BKIN2/ETH1_GMII_RGMII_GTX_CLK/FMC_A14
PG5/TIM1_ETR/ETH1_GMII_RGMII_CLK125/FMC_A15
PG6/TIM17_BKIN/SDMMC2_CMD/DCMI_D12/LCD_R7
PG7/SAI1_MCLK_A/USART6_CK/USART8_RTS_DE/QUADSPI_CLK/QUADSPI_BK2_IO3/DCMI_D13/LCD_CLK
PG8/TIM2_CH1/TIM2_TIM8_ETR/ETH_CLK/SPI6_NSS/SAI4_D2/USART6_RTS_DE/USART3_NSS_DE/SPDIFRX_IN2/SAI4_FS_A/ETH1_PPS_OUT/LCD_G7
PG9/DBTRGO/USART6_RX/SPDIFRX_IN3/QUADSPI_BK2_IO2/SAI2_FS_B/FMC_NCE/FMC_NE2/DCMI_VSYNC/LCD_R1
PG10/UART8_CTS/LCD_G3/SAI2_SD_B/QUADSPI_BK2_IO2/FMC_NE3/DCMI_D2/LCD_B2
PG11/USART1_UART4_TX/SPDIFRX_IN0/ETH1_GMII_MII_RMII_TX_EN/ETH1_RGMII_TX_CTL/DCMI_D3/LCD_B3
PG12/LPTIM1_IN1/SPI6_MISO/SAI4_CK2/USART6_RTS_DE/SPDIFRX_IN1/LCD_B4/SAI4_SCK_A/ETH1_PHY_INTN/FMC_NE4/LCD_B1
PG13/LPTIM1_OUT/SAI1_CK2/SAI4_CK1/SPI6_SCK/SAI1_SCK_A/USART6_CTS_NSS/SAI4_MCLK_A/ETH1_GMII_MII_RGMII_RMII_TXD0/FMC_A24/LCD_R0
PG14/LPTIM1_ETR/SPI6_MOSI/SAI4_D1/USART6_TX/QUADSPI_BK2_IO3/SAI4_SD_A/ETH1_GMII_MII_RGMII_RMII_TXD1/FMC_A25/LCD_B0
PG15/SAI1_D2/I2C2_SDA/SAI1_FS_A/USART6_CTS_NSS/SDMMC3_CK/DCMI_D13

PH0-OSC_IN
PH1-OSC_OUT
PH2/LPTIM1_IN2/QUADSPI_BK2_IO0/ETH1_GMII_MII_CRS/LCD_R0
PH3/DFSDM1_CKIN4/QUADSPI_BK2_IO1/SAI2_MCLK_B/ETH1_GMII_MII_COL/LCD_R1
PH4/I2C2_SCL/LCD_G5/LCD_G4
PH5/I2C2_SDA/SPI5_NSS/SAI4_SD_B
PH6/TIM12_CH1/I2C2_SMBA/SPI5_SCK/ETH1_MII_RGMII_RXD2/MDIOS_MDIO/DCMI_D8
PH7/I2C3_SCL/SPI5_MISO/ETH1_GMII_MII_RGMII_RXD3/MDIOS_MDC/DCMI_D9
PH8/TIM5_ETR/I2C3_SDA/DCMI_HSYNC/LCD_R2
PH9/TIM12_CH2/I2C3_SMBA/DCMI_D0/LCD_R3
PH10/TIM5_CH1/I2C4_SMBA/I2C1_SMBA/DCMI_D1/LCD_R4
PH11/TIM5_CH2/I2C4_SCL/I2C1_SCL/DCMI_D2/LCD_R5
PH12/HDP2/TIM5_CH3/I2C4_SDA/I2C1_SDA/DCMI_D3/LCD_R6
PH13/TIM8_CH1N/UART4_TX/FDCAN1_TX/LCD_G2
PH14/TIM8_CH2N/UART4_RX/FDCAN1_RX/DCMI_D4/LCD_G3
PH15/TIM8_CH3N/DCMI_D11/LCD_G4

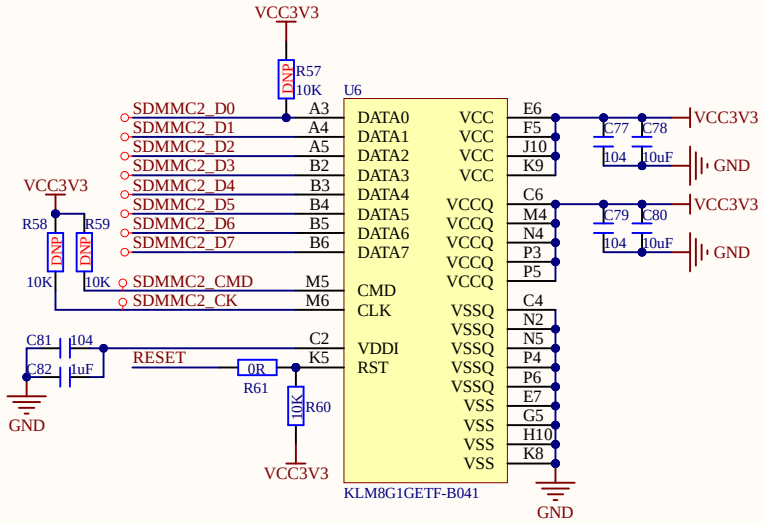
PI0/TIM5_CH4/SPI2_NSS_WS/DCMI_D13/LCD_G5
PI1/TIM8_BKIN2/SPI2_SCK_CK/DCMI_D8/LCD_G6
PI2/TIM8_CH4/SPI2_MISO/I2S2_SDI/DCMI_D9/LCD_G7
PI3/TIM8_ETR/SPI2_MOSI/I2S2_SDO/DCMI_D10
PI4/TIM8_BKIN/SAI2_MCLK_A/DCMI_D5/LCD_B4
PI5/TIM8_CH1/SAI2_SCK_A/DCMI_VSYNC/LCD_B5
PI6/TIM8_CH2/SAI2_SD_A/DCMI_D6/LCD_B6
PI7/TIM8_CH3/SAI2_FS_A/DCMI_D7/LCD_B7
PI8/RTC_OUT2_LSCO/TAMP_IN2/TAMP_OUT3/WKUP4
PI9/HDP1/UART4_RX/FDCAN1_RX/LCD_VSYNC
PI10/HDP0/USART3_CTS_NSS/ETH1_GMII_MII_RX_ER/LCD_HSYNC
PI11/MCO1/I2S_CKIN/LCD_G6/WKUP5
PI12/HDP0/LCD_HSYNC
PI13/HDP1/LCD_VSYNC
PI14/LCD_CLK
PI15/LCD_G2/LCD_R0

STM32MP175DAA1

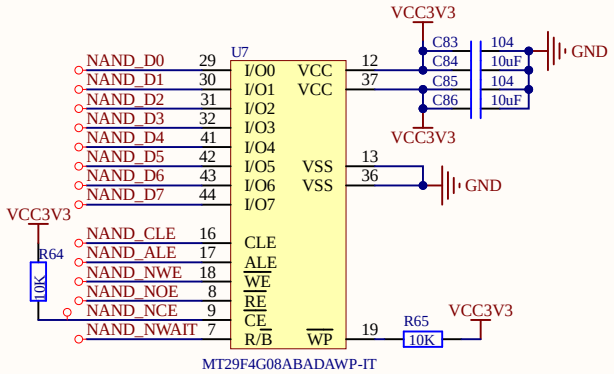
Title: STM32MP157_GHI.SchDoc		
Project: ATK-CLMP157B_V1.4.PrjPcb		
Size: A4	Author: lycreturn@ALIENTEK	
Date: 2021/6/9	Version: V1.0	Sheet: 4 of 10

正点原子

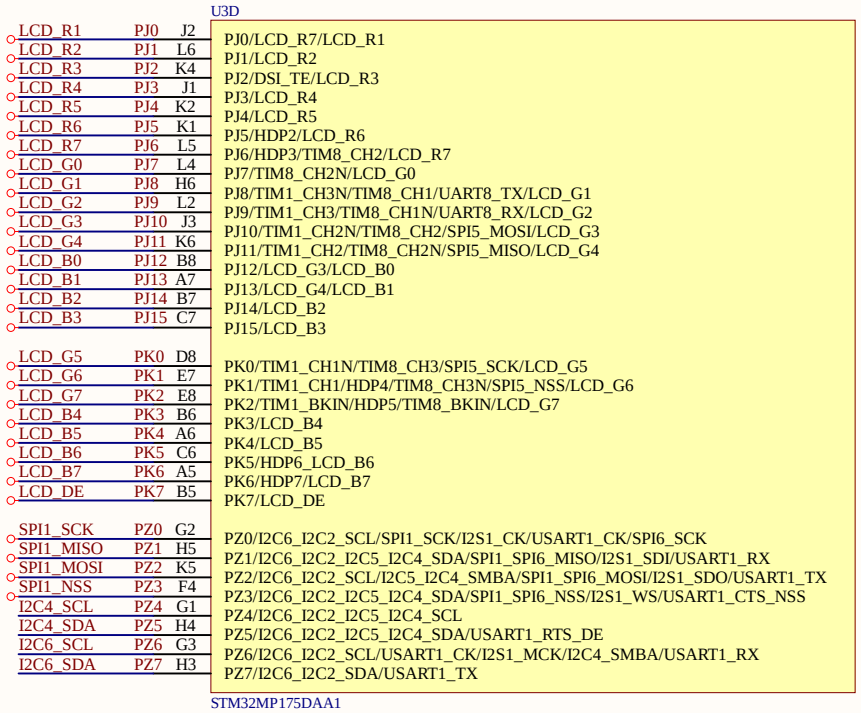
EMMC



NAND

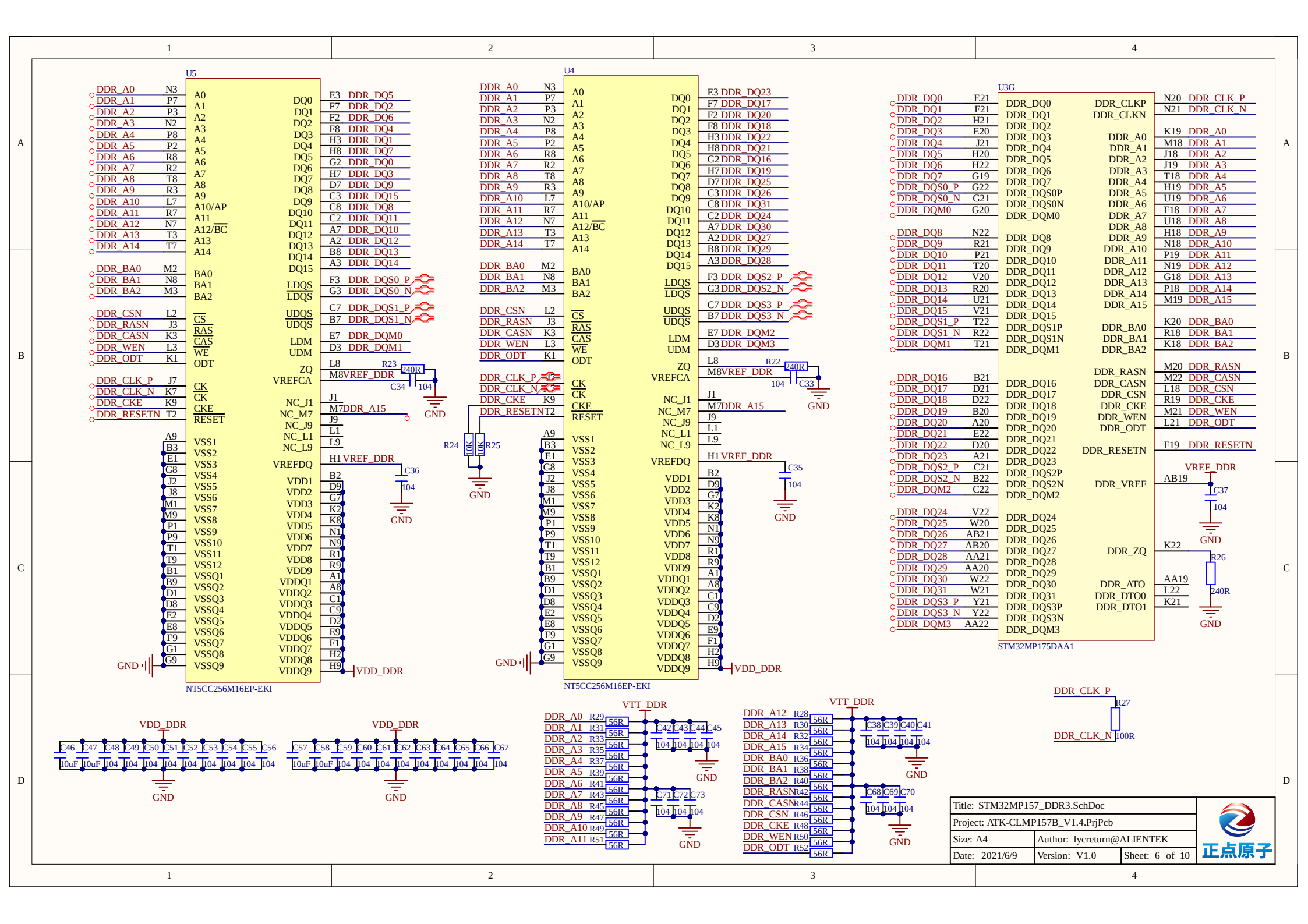


STM32MP157_JKZ

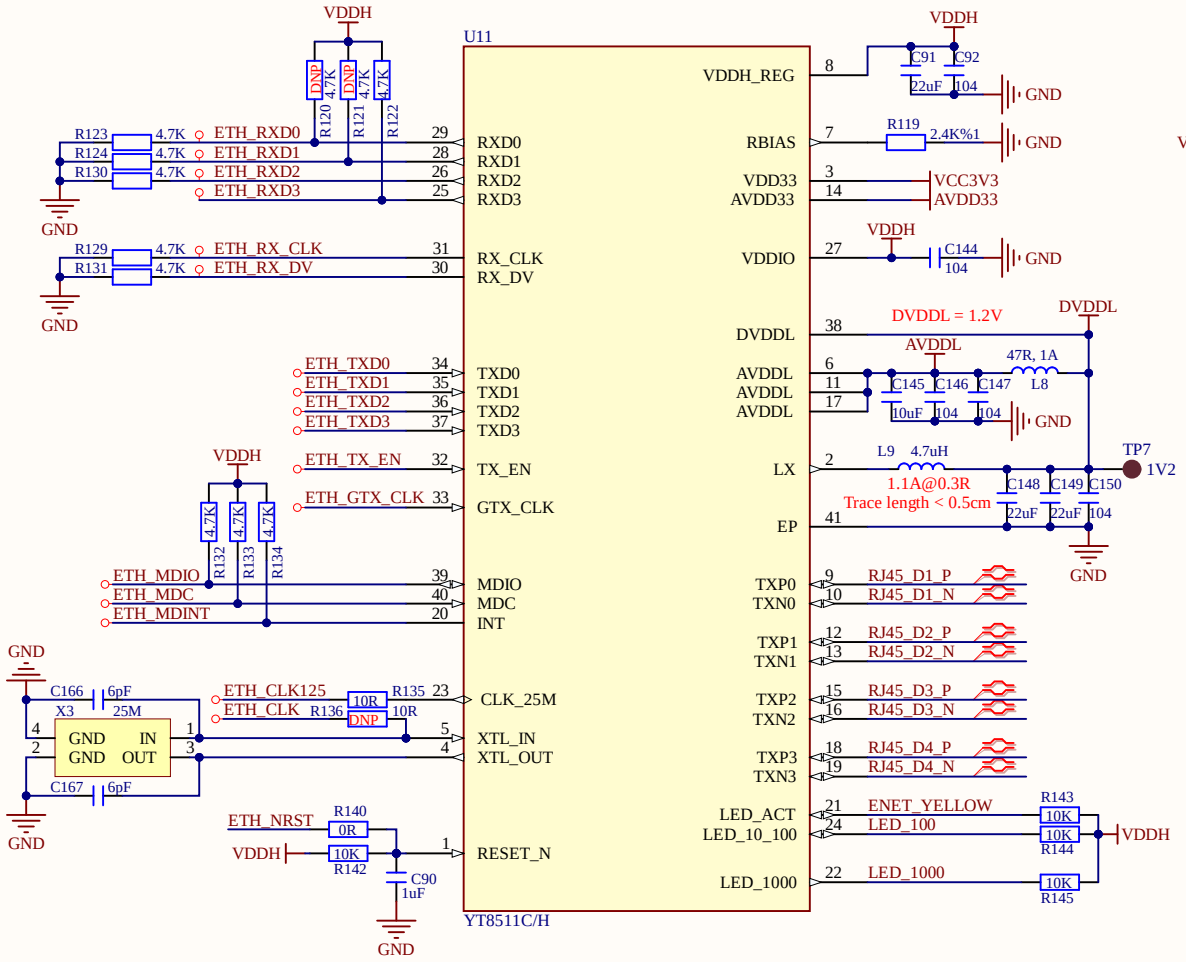


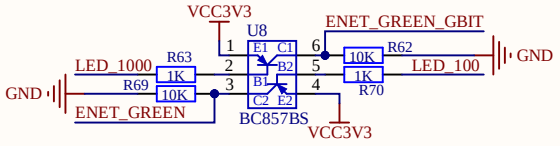
Title: STM32MP157_JKZ&FLASH.SchDoc		
Project: ATK-CLMP157B_V1.4.PrjPcb		
Size: A4	Author: lycreturn@ALIENTEK	
Date: 2021/6/9	Version: V1.0	Sheet: 5 of 10

正点原子


U5
NT5CC256M16EP-EKI
U4
NT5CC256M16EP-EKI
U3G
STM32MP175DAA1
VDD_DDR
VTT_DDR
GND
Title: STM32MP157_DDR3.SchDoc
Project: ATK-CLMP157B_V1.4.PrjPcb
Size: A4
Author: lycreturn@ALIENTEK
Date: 2021/6/9
Version: V1.0
Sheet: 6 of 10
正点原子

10/100/1000M NET





Power on Strapping Pins

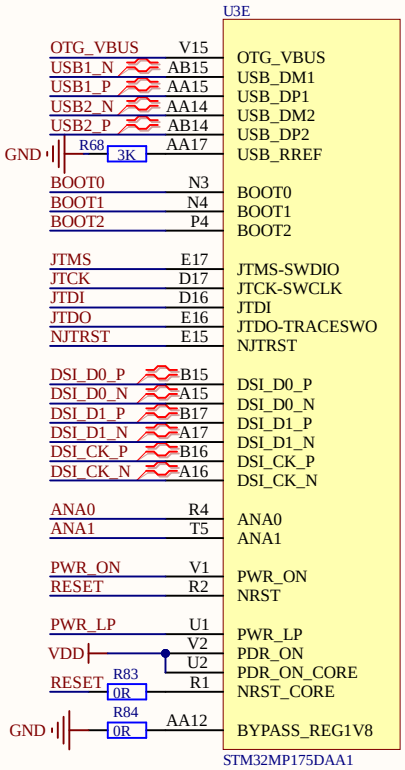
LED_ACT(IPU) RXD1(IPD) RXD0(IPD)	PHY_ADDR(2) PHY_ADDR(1) PHY_ADDR(0)	PHY Addr=00000+PHYA(2:0)		PHY address 00100b
RXD3(IPD) LED_1000(IPU)	MODE_SEL(1) MODE_SEL(0)	01=force low power mode; 11=normal mode;		Normal mode
RXD2(IPD)	PLLON	0=PLL OFF in hibernation;	1=PLL ON in hibernation;	PLL OFF in hibernation
RX_DV(IPD)	3.3V/2.5V_SEL	0=RGMll 1O 3.3V;	1=RGMll 1O 2.5V;	3.3V RGMII
LED_10_100(IPU)	RXC_delay_en	0=RXC delay disable;	1=RXC delay enable;	RXC delay enable
RX_CLK(IPD)	CLK_25M_en	0=CLK_25M enable;	1=CLK_25M disable;	CLK_25M output enable

YT8511C的100M和1000M指示灯低电平有效，而底板是高电平有效，故在此对这2个信号进行反向。

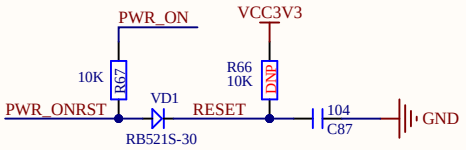
Title: STM32MP157_NET.SchDoc		
Project: ATK-CLMP157B_V1.4.PrjPcb		
Size: A4	Author: lycreturn@ALIENTEK	
Date: 2021/6/9	Version: V1.0	Sheet: 7 of 10

正点原子

USB&DSI&JTAG



RESET



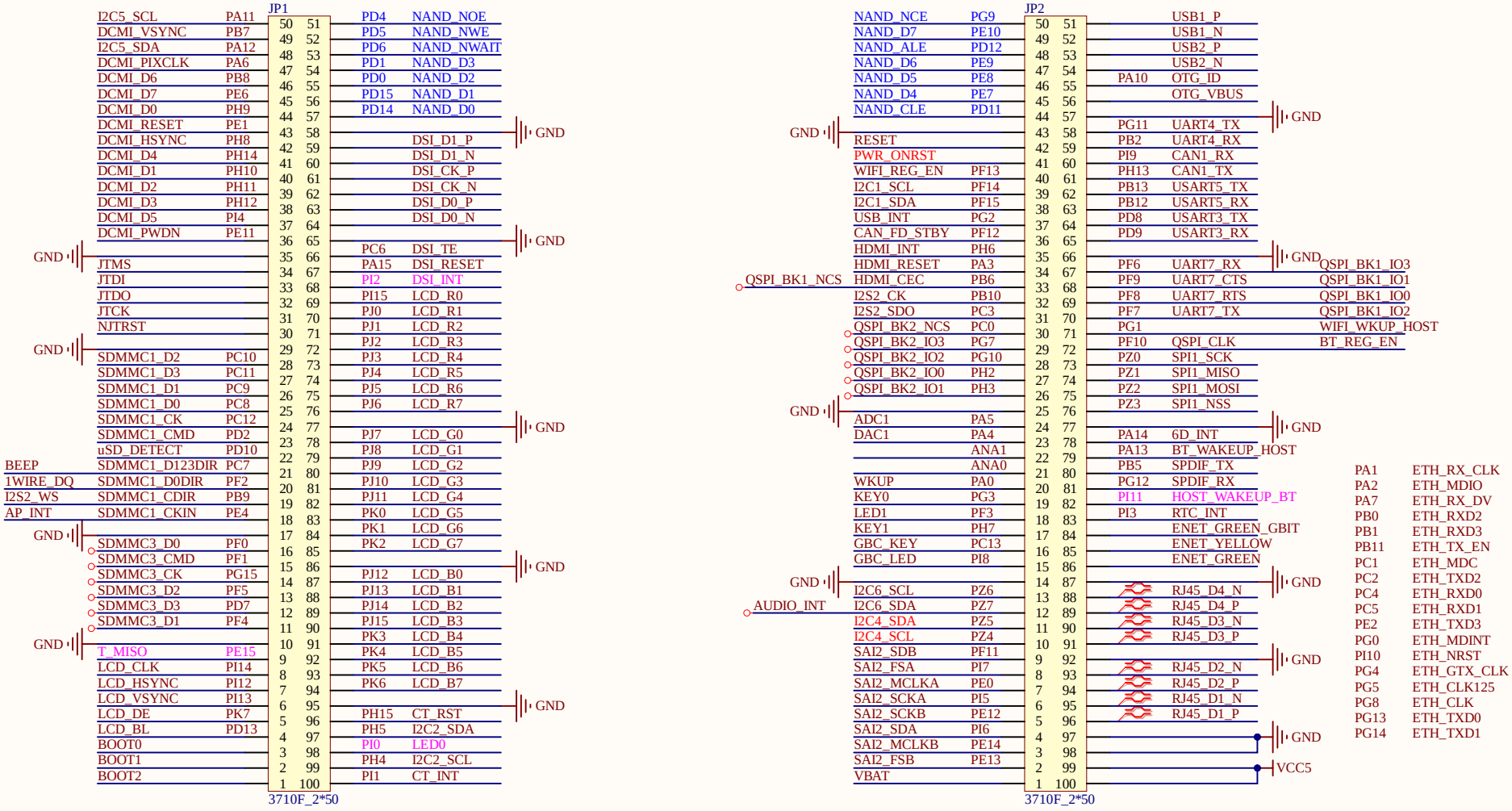
LED

ESD&FKT

ESD FKT
ESD FKT
ESD FKT

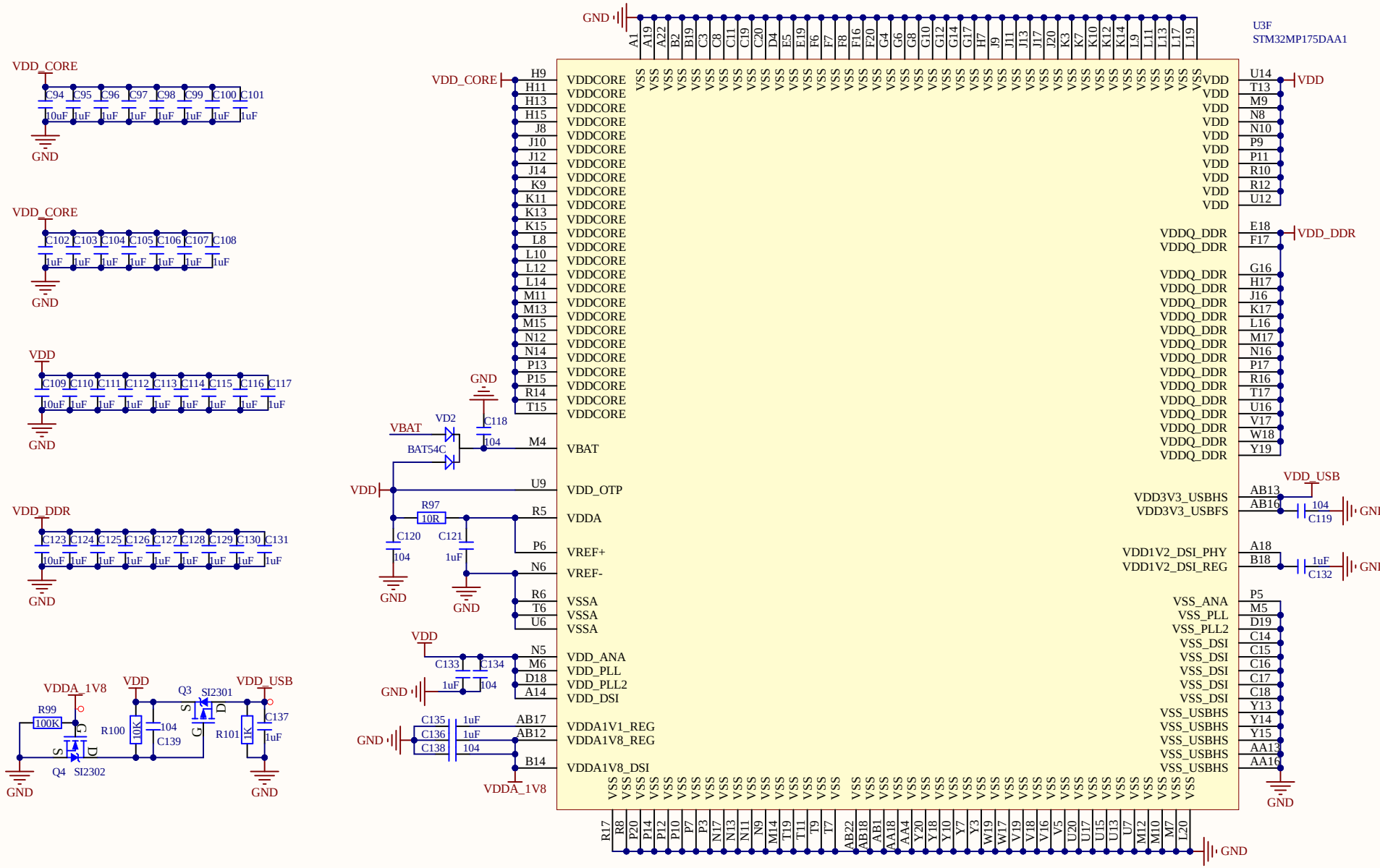
Title: STM32MP157_OTHER.SchDoc		
Project: ATK-CLMP157B_V1.4.PrjPcb		
Size: A4	Author: lycreturn@ALIENTEK	
Date: 2021/6/9	Version: V1.0	Sheet: 8 of 10

正点原子



Title: STM32MP157_PINOUT.SchDoc		
Project: ATK-CLMP157B_V1.4.PrjPcb		
Size: A4	Author: lycreturn@ALIENTEK	
Date: 2021/6/9	Version: V1.0	Sheet: 9 of 10

正点原子


U3F
STM32MP175DAA1
VDD_CORE
VDD_DDR
VDD_USB
VDD
VBAT
VDDA_1V8
GND
BAT54C
VD2
R97
10R
R99
100K
R100
10K
R101
1K
Q3
SI2301
Q4
SI2302
VDDCORE
VDDQ_DDR
VDD3V3_USBHS
VDD3V3_USBFS
VDD1V2_DSI_PHY
VDD1V2_DSI_REG
VDD_OTP
VDDA
VREF+
VREF-
VSSA
VDD_ANA
VDD_PLL
VDD_PLL2
VDD_DSI
VDDA1V1_REG
VDDA1V8_REG
VDDA1V8_DSI
VSS_ANA
VSS_PLL
VSS_PLL2
VSS_DSI
VSS_USBHS
VSS
Title: STM32MP157_POWER.SchDoc
Project: ATK-CLMP157B_V1.4.PrjPcb
Size: A4
Author: lycreturn@ALIENTEK
Date: 2021/6/9
Version: V1.0
Sheet: 10 of 10
正点原子