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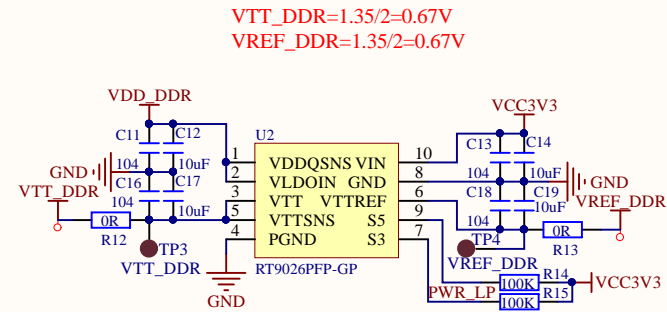
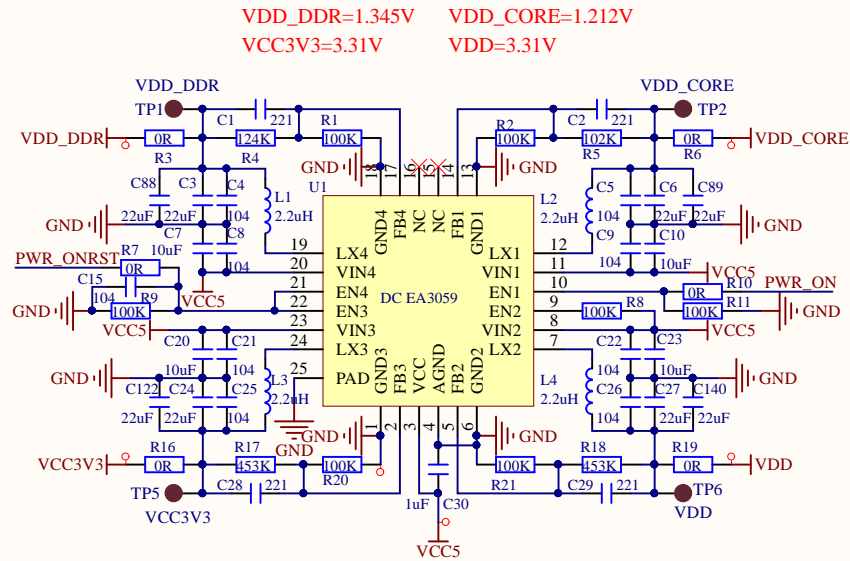
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A

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Project: STM32MP157_Core_V1.2.PrjPcb			
Size: A4	Author: lycreturn@ALIENTEK		
Date: 2021-06-09	Version: V1.0	Sheet: 1 of 10	

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U3A

PA0_WKUP	PA0	AA3	PA0/TIM2_TIM5_CH1/TIM2_TIM8_ETR/TIM15_BKIN/USART2_CTS_NSS/UART4_TX/SDMMC2_CMD/SAI2_SD_B/ETH1_GMII_MII_CRS/ADC1_INP16/WKUP1
ETH_RX_CLK	PA1	V4	PA1/ETH_CLK/TIM2_TIM5_CH2/LPTIM3_OUT/TIM15_CH1N/USART2_RTS_DE/UART4_RX/QUADSPI_BK1_IO3/SAI2_MCLK_B/ETH1_GMII_MII_RGMII_RX_CLK/ETH1_RMII_REF_CLK/LCD_R2/ADC1_INP17_INN16
ETH_MDIO	PA2	AB2	PA2/TIM2_TIM5_CH3/LPTIM4_OUT/TIM15_CH1/USART2_TX/SAI2_SCK_B/SDMMC2_D0DIR/ETH1_MDIO/MDIOS_MDIO/LCD_R1/ADC1_INP14/WKUP2
	PA3	T4	PA3/TIM2_TIM5_CH4/LPTIM5_OUT/TIM15_OUT/USART2_RX/LCD_B2/ETH1_GMII_MII_COL/LCD_B5/ADC1_INP15/PVD_IN
ADC118_DAC1	PA4	V6	PA4/HDP0/TIM5_ETR/SAI4_D2/SPI1_SPI3_SPI6_NSS/I2S1_I2S3_WS/USART2_CK/SAI4_FS_A/DCMI_HSYNC/LCD_VSYNC/ADC1_ADC2_INP18/DAC_OUT1
ADC119_DAC2	PA5	U5	PA5/TIM2_CH1/TIM2_ETR/TIM8_CH1N/SAI4_CK1/SPI1_SPI6_SCK/I2S1_CK/SAI4_MCLK_A/LCD_R2/ADC1_ADC2_INP19_INN18/DAC_OUT
DCMI_PIXCLK	PA6	W9	PA6/TIM1_TIN8_BKIN/TIM3_CH1/SAI4_CK2/SPI1_SPI6_MISO/I2S1_SDI/TIM13_CH1/MDIOS_MDC/SAI4_SCK_A/DCMI_PIXCLK/LCD_G2/ADC1_ADC2_INP3
ETH_RX_DV	PA7	Y9	PA7/TIM1_TIM8_CH1N/TIM3_CH2/SAI4_D1/SPI1_SPI6_MOSI/I2S1_SDO/TIM14_CH1/QUADSPI_CLK/ETH1_GMII_MII_RMII_RX_DV/ETH1_RGMII_RX_CTL/SAI4_SD_A/ADC1_ADC2_INP7_INN3
SDMMC2_D4	PA8	B13	PA8/MCO1/TIM1_CH1/TIM8_BKIN2/I2C3_SCL/SPI3_MOSI/I2S3_SDO/USART1_CK/SDMMC2_CKIN/SDMMC2_D4/OTG_FS_SOF/OTG_HS_SOF/SAI4_SD_B/UART7_RX/LCD_R6
SDMMC2_D5	PA9	A11	PA9/TIM1_CH2/I2C3_SMBA/SPI2_SCK/I2S2_CK/USART1_TX/SDMMC2_CDIR/SDMMC2_D5/DCMI_D0/LCD_R5
OTG_ID	PA10	Y17	PA10/TIM1_CH3/SPI3_NSS/I2S3_WS/USART1_RX/MDIOS_MDIO/SAI4_FS_B/DCMI_D1/LCD_B1/OTG_FS_HS_ID
I2C5_SCL	PA11	Y16	PA11/TIM1_CH4/I2C6_I2C5_SCL/SPI2_NSS/I2S2_WS/UART4_RX/USART1_USART1_NSS/FDCAN1_RX/LCD_R4/OTG_FS_DM
I2C5_SDA	PA12	W16	PA12/TIM1_ETR/I2C6_SDA/I2C5_SDA/UART4_TX/USART1_RTS_DE/SAI2_FS_B/FDCAN1_TX/LCD_R5/OTG_FS_DP
	PA13	W3	PA13/DBTRGO/DBTRGI/MCO1/UART4_TX/BOOTFAILN
	PA14	R3	PA14/DBTRGO/DBTRGI/MCO2
DSI_RESET	PA15	E11	PA15/DBTRGI/TIM2_CH1_ETR/SAI4_D2/SDMMC1_CDIR/CEC/SPI1_SPI3_SPI6_NSS/I2S1_I2S3_WS/UART4_RTS_DE/SDMMC1_SDMMC2_D5/SDMMC2_CDIR/SAI4_FS_A/UART7_TX/LCD_R1
ETH_RXD2	PB0	AB5	PB0/TIM1_TIM8_CH2N/TIM3_CH3/DFSDM1_CKOUT/UART4_CTS/LCD_R3/ETH1_GMII_MII_RGMII_RXD2/MDIOS_MDIO/LCD_G1/ADC1_INP9_INN5/ADC2_INP9_INN5
ETH_RXD3	PB1	AA5	PB1/TIM1_TIM8_CH3N/TIM3_CH4/DFSDM1_DATIN1/LCD_R6/ETH1_GMII_MII_RGMII_RXD3/MDIOS_MDC/LCD_G0/ADC1_ADC2_INP5
UART4_RX	PB2	V13	PB2/RTC_OUT2/SAI1_D1/DFSDM1_CKIN1/USART1_RX/I2S_CKIN/SAI1_SD_A/SPI3_MOSI/I2S3_SDO/UART4_RX/QUADSPI_CLK
SDMMC2_D2	PB3	A12	PB3/TIM2_CH2/SAI4_CK1/SPI1_SPI3_SPI6_SCK/I2S1_I2S3_CK/SDMMC2_D2/SAI4_MCLK_A/UART7_RX
SDMMC2_D3	PB4	C13	PB4/TIM16_BKIN/TIM3_CH1/SAI4_CK2/SPI1_SPI3_SPI6_MISO/I2S1_I2S3_SDI/I2S2_WS/SDMMC2_D3/SAI4_SCK_A/UART7_TX
SPDIF_TX	PB5	AA8	PB5/ETH_CLK/TIM17_BKIN/TIM3_CH2/SAI4_D1/I2C1_I2C4_SMBA/SPI1_SPI3_SPI6_MOSI/I2S1_I2S3_SDO/FDCAN2_RX/SAI4_SD_A/ETH1_PPS_OUT/UART5_RX/DCMI_D10/LCD_G7
HDMI_CEC	PB6	W13	PB6/TIM16_CH1N/TIM4_CH1/I2C1_I2C4_SCL/CEC/USART1_TX/FDCAN2_TX/QUADSPI_BK1_NCS/DFSDM1_DATIN5_UART5_TX/DCMI_D5
DCMI_VSYNC	PB7	F11	PB7/TIM17_CH1N/TIM4_CH2/I2C1_I2C4_SDA/USART1_RX/SDMMC2_D1/DFSDM1_CKIN5_FMC_NL/DCMI_VSYNC
DCMI_D6	PB8	AB8	PB8/HDP6/TIM16_CH1/TIM4_CH3/DFSDM1_CKIN7/SDMMC1_SDMMC2_CKIN/I2C1_I2C4_SCL/UART4_RX/FDCAN1_RX/SDMMC1_SDMMC2_D4/ETH1_GMII_MII_RGMII_TXD3/DCMI_D6/LCD_B6
SDMMC1_CDIR	PB9	F12	PB9/HDP7/TIM17_CH1/TIM4_CH4/DFSDM1_DATIN7/I2C1_I2C4_SDA/SPI2_NSS/I2S2_WS/SDMMC1_SDMMC2_CDIR/UART4_TX/FDCAN1_TX/SDMMC1_SDMMC2_D5/DCMI_D7/LCD_B7
	PB10	V9	PB10/TIM2_CH3/LPTIM2_IN1/I2C2_SCL/SPI2_SCK/I2S2_CK/DFSDM1_DATIN7/USART3_TX/QUADSPI_BK1_NCS/ETH1_GMII_MII_RX_ER/LCD_G4
ETH_TX_EN	PB11	Y5	PB11/TIM2_CH4/LPTIM2_ETR/I2C2_SDA/DFSDM1_CKIN7/USART3_RX/ETH1_GMII_MII_RMII_TX_EN/ETH1_RGMII_EX_CTL/DSI_DE/LCD_G5
USART5_RX	PB12	AA7	PB12/TIM1_BKIN/I2C6_I2C2_SMBA/SPI2_NSS/I2S2_WS/DFSDM1_DATIN1/USART3_CK_RX/FDCAN2_RX/ETH1_GMII_MII_RGMII_RMII_TXD0/UART5_RX
USART5_TX	PB13	V10	PB13/TIM1_CH1N/DFSDM1_CKOUT/LPTIM2_OUT/SPI2_SCK/I2S2_CK/DFSDM1_CKIN1/USART3_CTS_NSS/FDCAN2_TX/ETH1_GMII_MII_RGMII_RMII_TXD1/UART5_TX
SDMMC2_D0	PB14	A13	PB14/TIM1_TIM8_CH2N/TIM12_CH1/USART1_TX/SPI2_MISO/I2S2_SDI/DFSDM1_DATIN2/USART3_RTS_DE/SDMMC2_D0
SDMMC2_D1	PB15	B12	PB15/RTC_REFIN/TIM1_TIM8_CH3N/TIM12_CH2/USART1_RX/SPI2_MOSI/I2S2_SDO/DFSDM1_CKIN2/SDMMC2_D1
QSPI_BK2_NCS	PC0	U10	PC0/DFSDM1_CKIN0_DATIN4/LPTIM2_IN2/SAI2_FS_B/QUADSPI_BK2_NCS/LCD_R5/ADC1_ADC2_INP10
ETH_MDC	PC1	AB3	PC1/SAI1_D1/DFSDM1_DATIN0_CKIN4/SPI2_MOSI/I2S2_SDO/SAI1_SD_A/SDMMC2_CK/ETH1_MDC/MDIOS_MDC/ADC1_INP11_INN10/ADC2_INP11_INN10/TAMP_IN3/WKUP6
ETH_TXD2	PC2	Y1	PC2/DFSDM1_CKIN1_CKOUT/SPI2_MISO/I2S2_SDI/ETH1_GMII_MII_RGMII_TXD2/DCMI_PIXCLK/ADC1_INP12_INN11
	PC3	U3	PC3/DFSDM1_DATAIN1/SPI2_MOSI/I2S2_SDO/ETH1_GMII_MII_TX_CLK/ADC1_INP13_INN12
ETH_RXD0	PC4	AB6	PC4/DFSDM1_CKIN2/I2S1_MCK/SPDIFRX_IN2/ETH1_GMII_MII_RGMII_RMII_RXD0/ADC1_ADC2_INP4
ETH_RXD1	PC5	AA6	PC5/SAI1_D3/DFSDM1_DATIN2/SAI1_SAI4_D4/SPDIFRX_IN3/ETH1_GMII_MII_RGMII_RMII_RXD1/SAI4_D3/ADC1_INP8_INN4/ADC2_INP8_INN4
DSI_TE	PC6	E13	PC6/HDP1/TIM3_TIM8_CH1/DFSDM1_CKIN3/I2S2_MCK/USART6_TX/SDMMC1_D0DIR/SDMMC1_SDMMC2_D6/DSI_TE/DCMI_D0/LCD_HSYNC
SDMMC1_D123DIR	PC7	D13	PC7/HDP4/TIM3_TIM8_CH2/DFSDM1_DATIN3/I2S3_MCK/USART6_RX/SDMMC1_SDMMC2_D123DIR/SDMMC1_SDMMC2_D7/DCMI_D1/LCD_G6
SDMMC1_D0	PC8	E14	PC8/TIM3_TIM8_CH3/UART4_TX/USART6_CK/UART5_RTS_DE/SDMMC1_D0/DCMI_D2
SDMMC1_D1	PC9	D14	PC9/TIM3_TIM8_CH4/I2C3_SDA/I2S_CKIN/UART5_CTS/QUADSPI_BK1_IO0/SDMMC1_D1/DCMI_D3/LCD_B2
SDMMC1_D2	PC10	F14	PC10/DFSDM1_CKIN5/SPI3_SCK/I2S3_CK/USART3_RX/UART4_TX/QUADSPI_BK1_IO1/SAI4_MCLK_B/SDMMC1_D2/DCMI_D8/LCD_R2
SDMMC1_D3	PC11	D15	PC11/DFSDM1_DATIN5/SPI3_MISO/I2S3_SDI/USART3_RX/UART4_RX/QUADSPI_BK2_NCS/SAI4_SCK_B/SDMMC1_D3/DCMI_D4
SDMMC1_CK	PC12	E12	PC12/MCO2/SAI4_D3/SPI3_MOSI/I2S3_SDO/USART3_CK/UART5_TX/SAI4_SD_B/SDMMC1_CK/DCMI_D9
	PC13	N2	PC13/RTC_OUT1_TS_LSCO/TAMP_IN1_OUT2_OUT3/WKUP3
	P1		PC14-OSC32_IN
	P2		PC15-OSC32_OUT

32.768KHz

STM32MP157DAA1

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Size: A4	Author: lycreturn@ALIENTEK		
Date: 2021-06-09	Version: V1.0	Sheet: 2 of 10	

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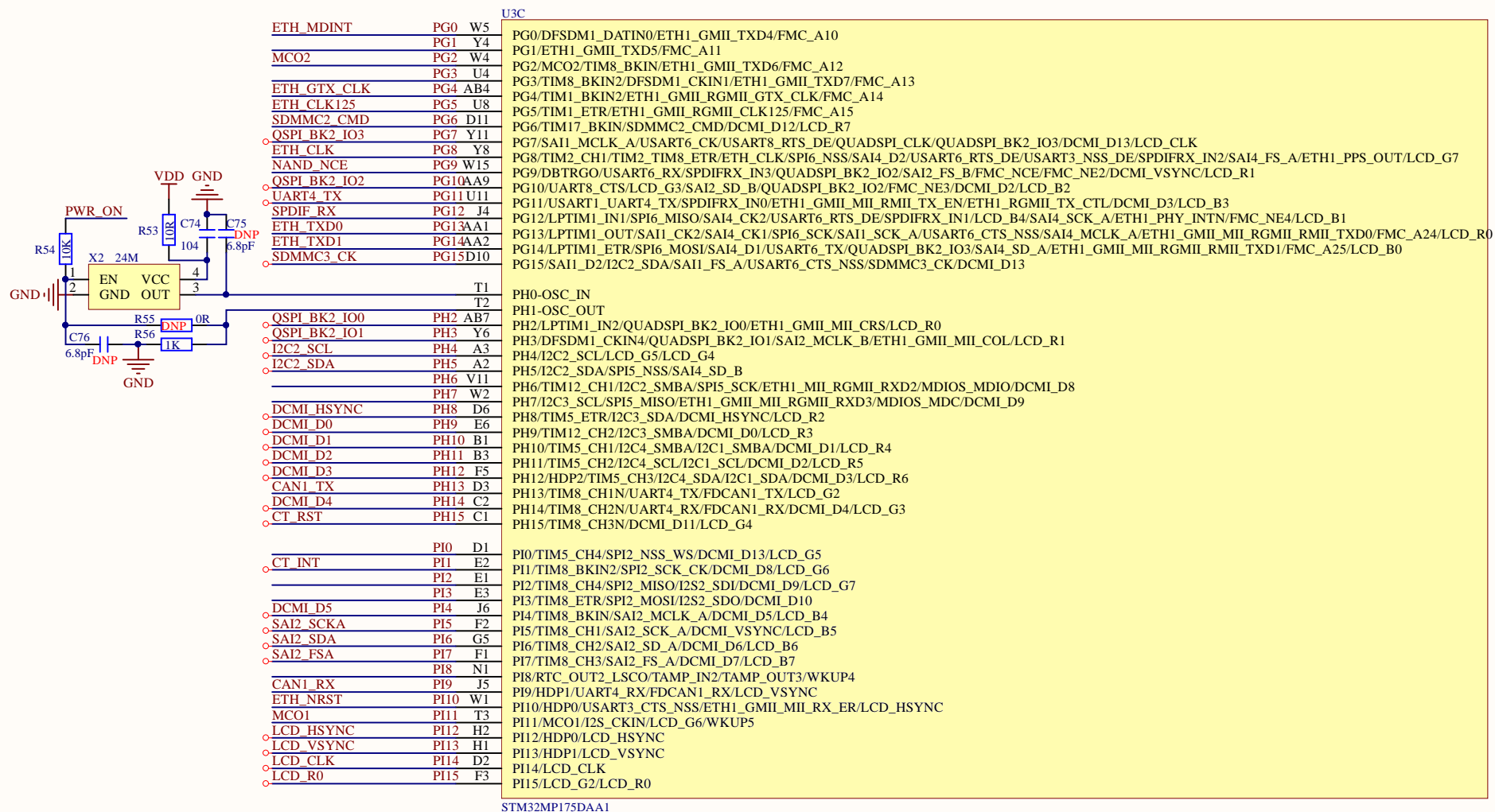
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NAND_D2	PD0	C10	PD0/I2C6_I2C5_SDA/DFSDM1_CKIN6/SAI3_SCK_A/UART4_RX/FDCAN1_RX/SDMMC3_CMD/DFSDM1_DATIN7/FMC_D2/FMC_DA2
NAND_D3	PD1	B10	PD1/I2C6_I2C5_SCL/DFSDM1_DATIN6/SAI3_SD_A/UART4_TX/FDCAN1_TX/SDMMC3_D0/DFSDM1_CKIN7/FMC_D3/FMC_DA3
SDMMC1_CMD	PD2	D12	PD2/TIM3_ETR/I2C5_SMBA/UART4_RX/UART5_RX/SDMMC1_CMD/DCMI_D11
SDMMC2_D7	PD3	B11	PD3/HDP5/DFSDM1_CKOUT/SPI2_SCK/I2S2_CK/DFSDM1_DATIN0/UART2_CTS_NSS/SDMMC1_SDMMC2_D123DIR/SDMMC1_SDMMC2_D7/FMC_CLK/DCMI_D5/LCD_G7
NAND_NOE	PD4	C9	PD4/SAI3_FS_A/USART2_RTS_DE/SDMMC3_D1/DFSDM1_CKIN0/FMC_NOE
NAND_NWE	PD5	A9	PD5/USART2_TX/SDMMC3_D2/FMC_NWE
NAND_NWAIT	PD6	L3	PD6/TIM16_CH1N/SAI1_D1/DFSDM1_CKIN4_DATIN1/SPI3_MOSI/I2S3_SDO/SAI1_SD_A/USART2_RX/FMC_NWAIT/DCMI_D10/LCD_B2
SDMMC3_D3	PD7	F10	PD7/DFSDM1_DATIN4_CKIN1/I2C2_SCL/USART2_CK/SPDIFRX_IN0/SDMMC3_D3/FMC_NE1
USART3_TX	PD8	M1	PD8/DFSDM1_CKIN3/SAI3_SCK_B/USART3_TX/SPDIFRX_IN1/FMC_D13/FMC_DA13/LCD_B7
USART3_RX	PD9	M2	PD9/DFSDM1_DATIN3/SAI3_SD_B/USART3_RX/FMC_D14/FMC_DA14/DCMI_HSYNC/LCD_B0
uSD_DETECT	PD10	A8	PD10/RTC_REFIN/TIM16_BKIN/DFSDM1_CKOUT/I2C5_SMBA/SPI3_MISO/I2S3_SDI/SAI3_FS_B/USART3_CK/FMC_D15/FMC_DA15/LCD_B3
NAND_CLE	PD11	AB9	PD11/LPTIM2_IN2/I2C4_I2C1_SMBA/USART3_CTS_NSS/QUADSPI_BK1_IO0/SAI2_SD_A/FMC_CLE/FMC_A16
NAND_ALE	PD12	W12	PD12/LPTIM1_LPTIM2_IN1/TIM4_CH1/I2C4_I2C1_SCL/USART3_RTS_DE/QUADSPI_BK1_IO1/SAI2_FS_A/FMC_ALE/FMC_A17
LCD_BL	PD13	V14	PD13/LPTIM1_OUT/TIM4_CH2/I2C4_I2C1_SDA/I2S3_MCK/QUADSPI_BK1_IO3/SAI2_SCK_A/FMC_A18
NAND_D0	PD14	M3	PD14/TIM4_CH3/SAI3_MCLK_B/UART8_CTS/FMC_D0/FMC_DA0
NAND_D1	PD15	L1	PD15/TIM4_CH4/SAI3_MCLK_A/UART8_CTS/FMC_D1/FMC_DA1/LCD_R1
SAI2_MCLKA	PE0	C5	PE0/LPTIM1_LPTIM2_ETR/TIM4_ETR/SPI3_SCK/I2S3_CK/SAI4_MCLK_B/UART8_RX/SAI2_MCLK_A/FMC_NBL0/DCMI_D2
DCMI_RESET	PE1	D7	PE1/LPTIM1_IN2/I2S2_MCK/SAI3_SD_B/UART8_TX/FMC_NBL1/DCMI_D3
ETH_TXD3	PE2	Y2	PE2/SAI1_CK1/I2C4_SCL/SPI4_SCK/SAI1_MCLK_A/QUADSPI_BK1_IO2/ETH1_GMII_MII_RGMII_TXD3/FMC_A23
SDMMC2_CK	PE3	A10	PE3/TIM15_BKIN/SAI1_SD_B/SDMMC2_CK/FMC_A19
SDMMC1_CKIN	PE4	F15	PE4/SAI1_D2/DFSDM1_DATIN3/TIM15_CH1N/SPI4_NSS/SAI1_FS_A/SDMMC1_SDMMC2_CKIN/SDMMC1_SDMMC2_D4/FMC_A20/DCMI_D4/LCD_B0
SDMMC2_D6	PE5	C12	PE5/SAI1_CK2/DFSDM1_CKIN3/TIM15_CH1/SPI4_MISO/SAI1_SCK_A/SDMMC1_SDMMC2_D0DIR/SDMMC1_SDMMC2_D6/FMC_A21/DMIC_D6/LCD_G0
DCMI_D7	PE6	E9	PE6/TIM1_BKIN2/SAI1_D1/TIM15_CH2/SPI4_MOSI/SAI1_SD_A/SDMMC2_D0/SDMMC1_D2/SAI2_MCLK_B/FMC_A22/DCMI_D7/LCD_G1
NAND_D4	PE7	W10	PE7/TIM1_TIM3_ETR/DFSDM1_DATIN2/UART7_RX/QUADSPI_BK2_IO0/FMC_D4/FMC_DA4
NAND_D5	PE8	Y12	PE8/TIM1_CH1N/DFSDM1_CKIN2/UART7_TX/QUADSPI_BK2_IO1/FMC_D5/FMC_DA5
NAND_D6	PE9	W11	PE9/TIM1_CH1/DFSDM1_CKOUT/UART7_RTS_DE/QUADSPI_BK2_IO2/FMC_D6/FMC_DA6
NAND_D7	PE10	W14	PE10/TIM1_CH2N/DFSDM1_DATIN4/UART7_CTS/QUADSPI_BK2_IO3/FMC_D7/FMC_DA7
DCMI_PWDN	PE11	D5	PE11/TIM1_CH2/DFSDM1_CKIN4/SPI4_NSS/USART6_CK/SAI2_SD_B/FMC_D8/FMC_DA8/DCMI_D4/LCD_G3
SAI2_SCKB	PE12	E4	PE12/TIM1_CH3N/DFSDM1_DATIN5/SPI4_SCK/SDMMC1_D0DIR/SAI2_SCK_B/FMC_D9/FMC_DA9/LCD_B4
SAI2_FSB	PE13	A4	PE13/HDP2/TIM1_CH3/DFSDM1_CKIN5/SPI4_MISO/SAI2_FS_B/FMC_D10/FMC_DA10/DCMI_D6/LCD_DE
SAI2_MCLKB	PE14	B4	PE14/TIM1_CH4/SPI4_MOSI/UART8_RTS_DE/SAI2_MCLK_B/SDMMC1_D123DIR/FMC_D11/FMC_DA11/LCD_G0/LCD_CLK
T_MISO	PE15	C4	PE15/HDP3/TIM1_BKIN/TIM15_BKIN/USART2_CTS_NSS/UART8_CTS/FMC_NCE2/FMC_D12/FMC_DA12/LCD_R7
SDMMC3_D0	PF0	E10	PF0/I2C2_SDA/SDMMC3_D0_CKIN/FMC_A0
SDMMC3_CMD	PF1	B9	PF1/I2C2_SCL/SDMMC3_CMD_CDIR/FMC_A1
SDMMC1_D0DIR	PF2	F13	PF2/I2C2_SMBA/SDMMC1_SDMMC2_SDMMC3_D0DIR/FMC_A2
SDMMC3_D1	PF3	V3	PF3/ETH1_GMII_MII_TX_ER/FMC_A3
SDMMC3_D2	PF4	F9	PF4/USART2_RX/SDMMC3_D1/SDMMC3_D123DIR/FMC_A4
QSPI_BK1_IO3	PF5	D9	PF5/USART2_TX/SDMMC3_D2/FMC_A5
QSPI_BK1_IO2	PF6	AA11	PF6/TIM16_CH1/SPI5_NSS/SAI1_SD_B/UART7_RX/QUADSPI_BK1_IO3/SAI4_SCK_B
QSPI_BK1_IO2	PF7	AA10	PF7/TIM17_CH1/SPI5_SCK/SAI1_MCLK_B/UART7_TX/QUADSPI_BK1_IO2
QSPI_BK1_IO0	PF8	AB10	PF8/TIM16_CH1N/SPI5_MISO/SAI1_SCK_B/UART7_RTS_DE/TIM13_CH1/QUADSPI_BK1_IO0
QSPI_BK1_IO1	PF9	AB11	PF9/TIM17_CH1N/SPI5_MOSI/SAI1_FS_B/UART7_CTS/TIM14_CH1/QUADSPI_BK1_IO1
QSPI_CLK	PF10	V12	PF10/TIM16_BKIN/SAI1_D3/SAI1_SAI4_D4/QUADSPI_CLK/SAI4_D3/DCMI_D11/LCD_DE
SAI2_SDB	PF11	W8	PF11/SPI5_MOSI/SAI2_SD_B/DCMI_D12/LCD_G5/ADC1_INP2
	PF12	V8	PF12/ETH1_GMII_RXD4/FMC_A6/ADC1_INP6_INN2
	PF13	W7	PF13/DFSDM1_DATIN6_DATIN3/I2C1_I2C4_SMBA/ETH1_GMII_RXD5/FMC_A7/ADC2_INP2
	PF14	V7	PF14/DFSDM1_CKIN6/I2C1_I2C4_SCL/ETH1_GMII_RXD6/FMC_A8/ADC2_INP6_INN2
	PF15	W6	PF15/I2C1_I2C4_SDA/ETH1_GMII_RXD7/FMC_A9

STM32MP175DAA1

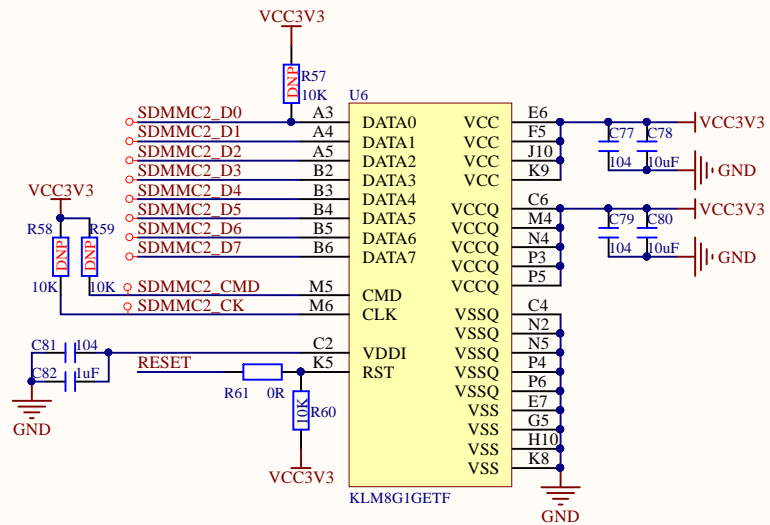
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Size: A4	Author: lycreturn@ALIENTEK		
Date: 2021-06-09	Version: V1.0	Sheet: 3 of 10	



STM32MP157DAA1

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Date: 2021-06-09	Version: V1.0	Sheet: 4 of 10	

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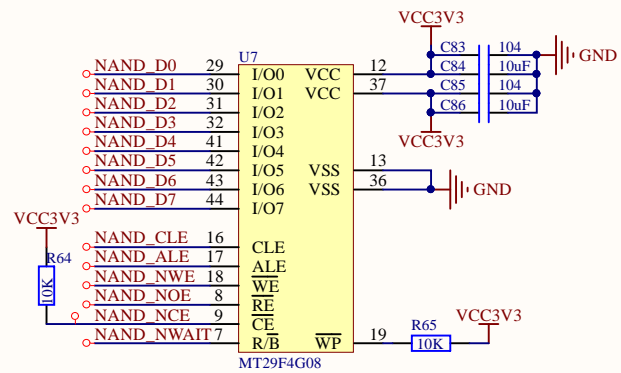


STM32MP157_JKZ

U3D		
LCD_R1	PJ0	J2
LCD_R2	PJ1	L6
LCD_R3	PJ2	K4
LCD_R4	PJ3	J1
LCD_R5	PJ4	K2
LCD_R6	PJ5	K1
LCD_R7	PJ6	L5
LCD_G0	PJ7	L4
LCD_G1	PJ8	H6
LCD_G2	PJ9	L2
LCD_G3	PJ10	J3
LCD_G4	PJ11	K6
LCD_B0	PJ12	B8
LCD_B1	PJ13	A7
LCD_B2	PJ14	B7
LCD_B3	PJ15	C7
LCD_G5	PK0	D8
LCD_G6	PK1	E7
LCD_G7	PK2	E8
LCD_B4	PK3	B6
LCD_B5	PK4	A6
LCD_B6	PK5	C6
LCD_B7	PK6	A5
LCD_DE	PK7	B5
SPI1_SCK	PZ0	G2
SPI1_MISO	PZ1	H5
SPI1_MOSI	PZ2	K5
SPI1_NSS	PZ3	F4
I2C4_SCL	PZ4	G1
I2C4_SDA	PZ5	H4
I2C6_SCL	PZ6	G3
I2C6_SDA	PZ7	H3

STM32MP175DAA1

NAND



Title: STM32MP157_JKZ&FLASH.SchDoc			Cannot open file D:\Program Files\Altium\My Template\正点L OGO竖.png
Project: STM32MP157_Core_V1.2.PrjPcb			
Size: A4	Author: lycerturn@ALIENTEK		
Date: 2021-06-09	Version: V1.0	Sheet: 5 of 10	

1

2

3

4

U5

U4

U3G

DDR_A0 N3
DDR_A1 P7
DDR_A2 P3
DDR_A3 N2
DDR_A4 P8
DDR_A5 P2
DDR_A6 R8
DDR_A7 R2
DDR_A8 T8
DDR_A9 R3
DDR_A10 L7
DDR_A11 R7
DDR_A12 N7
DDR_A13 T3
DDR_A14 T7

DDR_BA0 M2
DDR_BA1 N8
DDR_BA2 M3

DDR_CSN L2
DDR_RASN J3
DDR_CASN K3
DDR_WEN L3
DDR_ODT K1

DDR_CLK_P J7
DDR_CLK_N K7
DDR_CKE K9
DDR_RESETN T2

A9 VSS1
B3 VSS2
E1 VSS3
G8 VSS4
J2 VSS5
J8 VSS6
M1 VSS7
M9 VSS8
P1 VSS9
P9 VSS10
T1 VSS11
T9 VSS12
B1 VSSQ1
B9 VSSQ2
D1 VSSQ3
D8 VSSQ4
E2 VSSQ5
E8 VSSQ6
F9 VSSQ7
G1 VSSQ8
G9 VSSQ9

CK
CKE
RESET

NC_J1
NC_M7
NC_J9
NC_L1
NC_L9

VREFCA
VREFDQ
VDD1
VDD2
VDD3
VDD4
VDD5
VDD6
VDD7
VDD8
VDD9
VDDQ1
VDDQ2
VDDQ3
VDDQ4
VDDQ5
VDDQ6
VDDQ7
VDDQ8
VDDQ9

E3 DDR_DQ5
F7 DDR_DQ2
F2 DDR_DQ6
F8 DDR_DQ4
H3 DDR_DQ1
H8 DDR_DQ7
G2 DDR_DQ0
H7 DDR_DQ3
D7 DDR_DQ9
C3 DDR_DQ15
C8 DDR_DQ8
C2 DDR_DQ11
A7 DDR_DQ10
A2 DDR_DQ12
B8 DDR_DQ13
A3 DDR_DQ14

F3 DDR_DQS0_P
G3 DDR_DQS0_N
C7 DDR_DQS1_P
B7 DDR_DQS1_N
E7 DDR_DQM0
D3 DDR_DQM1

UDQS
UDQS
LDM
UDM

ZQ
VREFCA
M8VREF_DDR
J1 M7DDR_A15
J9
L1
L9

H1 VREF_DDR
B2
D9
G7
K2
K8
N1
N9
R1
R9
A1
A8
C1
C9
D2
E9
F1
H2
H9

VDD1
VDD2
VDD3
VDD4
VDD5
VDD6
VDD7
VDD8
VDD9
VDDQ1
VDDQ2
VDDQ3
VDDQ4
VDDQ5
VDDQ6
VDDQ7
VDDQ8
VDDQ9

DDR_A0 N3
DDR_A1 P7
DDR_A2 P3
DDR_A3 N2
DDR_A4 P8
DDR_A5 P2
DDR_A6 R8
DDR_A7 R2
DDR_A8 T8
DDR_A9 R3
DDR_A10 L7
DDR_A11 R7
DDR_A12 N7
DDR_A13 T3
DDR_A14 T7

DDR_BA0 M2
DDR_BA1 N8
DDR_BA2 M3

DDR_CSN L2
DDR_RASN J3
DDR_CASN K3
DDR_WEN L3
DDR_ODT K1

DDR_CLK_P
DDR_CLK_N
DDR_CKE
DDR_RESETN

CK
CKE
RESET

A9 VSS1
B3 VSS2
E1 VSS3
G8 VSS4
J2 VSS5
J8 VSS6
M1 VSS7
M9 VSS8
P1 VSS9
P9 VSS10
T1 VSS11
T9 VSS12
B1 VSSQ1
B9 VSSQ2
D1 VSSQ3
D8 VSSQ4
E2 VSSQ5
E8 VSSQ6
F9 VSSQ7
G1 VSSQ8
G9 VSSQ9

MT41K256M16TW

A0 DQ0
A1 DQ1
A2 DQ2
A3 DQ3
A4 DQ4
A5 DQ5
A6 DQ6
A7 DQ7
A8 DQ8
A9 DQ9
A10 DQ10
A11 DQ11
A12 DQ12
A13 DQ13
A14 DQ14
A15 DQ15

BA0
BA1
BA2

CS
RAS
CAS
WE
ODT

CK
CKE
RESET

NC_J1
NC_M7
NC_J9
NC_L1
NC_L9

VREFCA
VREFDQ
VDD1
VDD2
VDD3
VDD4
VDD5
VDD6
VDD7
VDD8
VDD9
VDDQ1
VDDQ2
VDDQ3
VDDQ4
VDDQ5
VDDQ6
VDDQ7
VDDQ8
VDDQ9

MT41K256M16TW

E3 DDR_DQ23
F7 DDR_DQ17
F2 DDR_DQ20
F8 DDR_DQ18
H3 DDR_DQ22
H8 DDR_DQ21
G2 DDR_DQ16
H7 DDR_DQ19
D7 DDR_DQ25
C3 DDR_DQ26
C8 DDR_DQ31
C2 DDR_DQ24
A7 DDR_DQ30
A2 DDR_DQ27
B8 DDR_DQ29
A3 DDR_DQ28

F3 DDR_DQS2_P
G3 DDR_DQS2_N
C7 DDR_DQS3_P
B7 DDR_DQS3_N
E7 DDR_DQM2
D3 DDR_DQM3

UDQS
UDQS
LDM
UDM

ZQ
VREFCA
M8VREF_DDR
J1 M7DDR_A15
J9
L1
L9

H1 VREF_DDR
B2
D9
G7
K2
K8
N1
N9
R1
R9
A1
A8
C1
C9
D2
E9
F1
H2
H9

VDD1
VDD2
VDD3
VDD4
VDD5
VDD6
VDD7
VDD8
VDD9
VDDQ1
VDDQ2
VDDQ3
VDDQ4
VDDQ5
VDDQ6
VDDQ7
VDDQ8
VDDQ9

MT41K256M16TW

DDR_DQ0 E21
DDR_DQ1 F21
DDR_DQ2 H21
DDR_DQ3 E20
DDR_DQ4 J21
DDR_DQ5 H20
DDR_DQ6 H22
DDR_DQ7 G19
DDR_DQS0_P G22
DDR_DQS0_N G21
DDR_DQM0 G20

DDR_DQ8 N22
DDR_DQ9 R21
DDR_DQ10 P21
DDR_DQ11 T20
DDR_DQ12 V20
DDR_DQ13 R20
DDR_DQ14 U21
DDR_DQ15 V21
DDR_DQS1_P T22
DDR_DQS1_N R22
DDR_DQM1 T21

UDQS
UDQS
LDM
UDM

ZQ
VREFCA
M8VREF_DDR
J1 M7DDR_A15
J9
L1
L9

H1 VREF_DDR
B2
D9
G7
K2
K8
N1
N9
R1
R9
A1
A8
C1
C9
D2
E9
F1
H2
H9

VDD1
VDD2
VDD3
VDD4
VDD5
VDD6
VDD7
VDD8
VDD9
VDDQ1
VDDQ2
VDDQ3
VDDQ4
VDDQ5
VDDQ6
VDDQ7
VDDQ8
VDDQ9

MT41K256M16TW

DDR_CLK_P
DDR_CLK_N
DDR_CKE
DDR_RESETN

CK
CKE
RESET

NC_J1
NC_M7
NC_J9
NC_L1
NC_L9

VREFCA
VREFDQ
VDD1
VDD2
VDD3
VDD4
VDD5
VDD6
VDD7
VDD8
VDD9
VDDQ1
VDDQ2
VDDQ3
VDDQ4
VDDQ5
VDDQ6
VDDQ7
VDDQ8
VDDQ9

H1 VREF_DDR
B2
D9
G7
K2
K8
N1
N9
R1
R9
A1
A8
C1
C9
D2
E9
F1
H2
H9

VDD1
VDD2
VDD3
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VDD5
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VDDQ1
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VDDQ8
VDDQ9

MT41K256M16TW

1

2

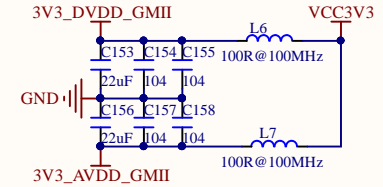
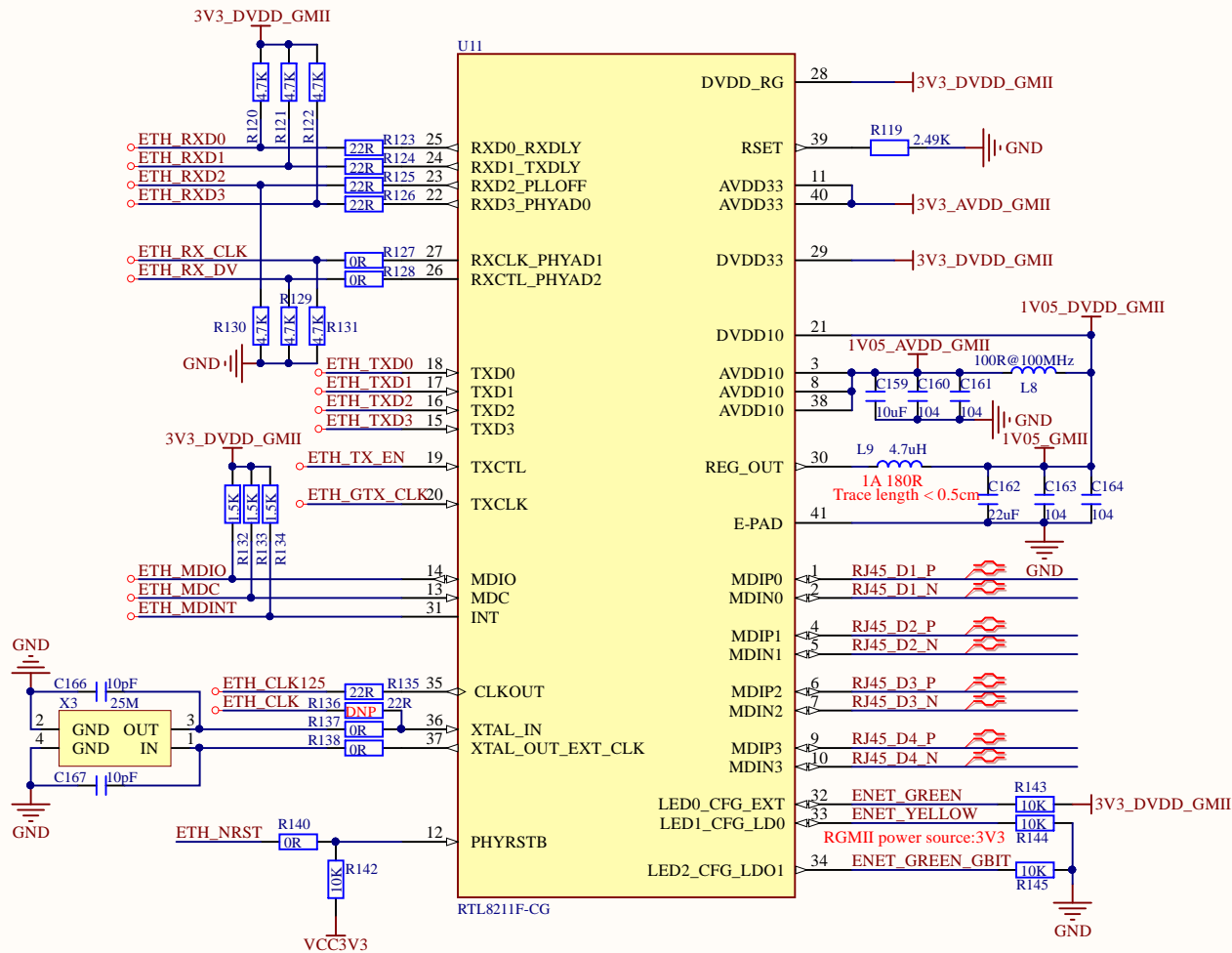
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4

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Project: STM32MP157_Core_V1.2.PrjPcb			
Size: A4	Author: lycreturn@ALIENTEK		
Date: 2021-06-09	Version: V1.0	Sheet: 6 of 10	

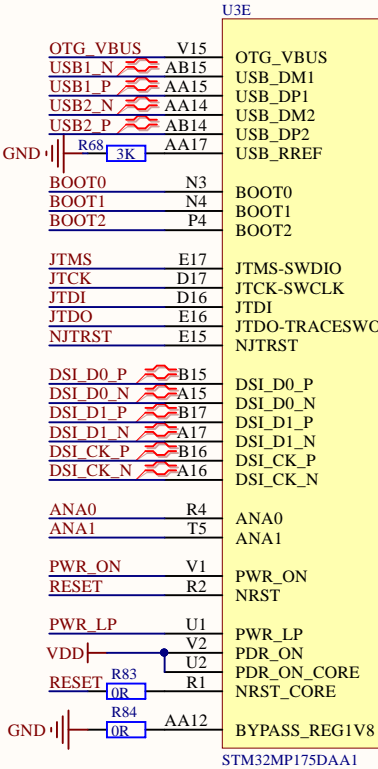
10/100/1000M NET

TXC/RXC: delay 2ns
PHY Address:0x01

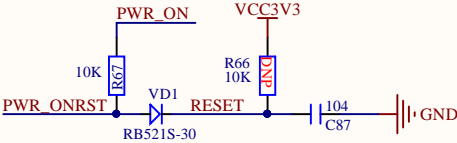


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Project: STM32MP157_Core_V1.2.PrjPcb			
Size: A4	Author: lycreturn@ALIENTEK		
Date: 2021-06-09	Version: V1.0	Sheet: 8 of 10	

USB&DSI&JTAG



RESET



LED



ESD&FKT

ESD FKT
ESD FKT
ESD FKT

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Date: 2021-06-09	Version: V1.0	Sheet: 9 of 10	

