BG95&BG77-QuecOpen Application Note

LPWA Module Series

Rev. BG95&BG77-QuecOpen _Application_Note_V1.1

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GENERAL NOTES

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About the Document

Revision History

Revision	Date	Author	Description
1.0	2019-08-30	Justice HAN/ Hyman DING	Initial
1.1	2019-01-21	Egbert XU/ Justice HAN/	1. Changed the pin tables of BG95. 2. Added Chapter 6.2.

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1 Introduction

This document mainly introduces BG95&BG77-QuecOpen solutions, including QuecOpen solution introduction, the step of constructing the compilation environment in the operating system of Windows and Linux, how to compile user application in related QuecOpen SDK and how to run and update their own application.

NOTE

In this document, BG95 refers to the corresponding module series models, including BG95M1, BG95M2 and BG95M3 models.

2 BG95&BG77-QuecOpen Solution Overview

2.1. General Overview

Quectel BG95&BG77 have rich on-chip resources. If customers use this module as a standard module, the external MCU can communicate with module by AT commands. Based on QuecOpen solution, module could provide the corresponding hardware resources, including ROM & RAM, and also provide some peripheral devices, including UART, SPI and IIC. At the same time, the module also has corresponding Software Development Kit (SDK) to help customers simplify application development.

QuecOpen provides an infrastructure for applications to dynamically load modules that are built from the resident component of the application. Each module is built independently with a common preamble structure attached in the binary. The preamble contains various details about the module, including:

- A single thread entry point
- Stack size priority
- Module ID
- Callback thread stack size/priority and so on.

2.2. QuecOpen Architecture

The following diagram shows the architecture of QuecOpen solution.

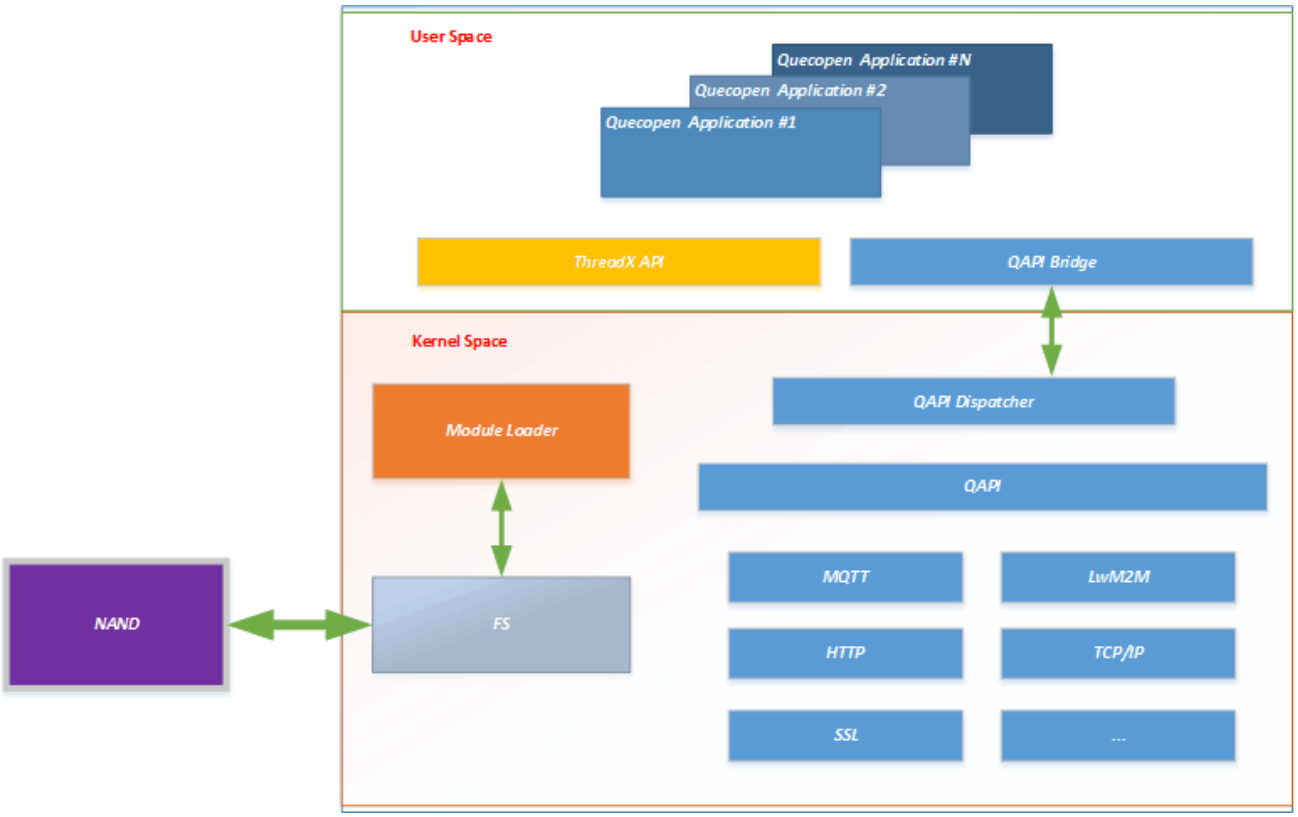

Figure 1: Architecture of QuecOpen solution

NOTES

1. Quectel recommends that customers use a single QuecOpen application for the sake of secure storage of their application image, as it is easier to maintain, so we provide ROM storage for image in this way. If customers need to use more than one QuecOpen application, the other images can only be stored and loaded from the file system.
2. Storing customer application binary image in ROM area is still under development.

3 Constructing Compiling Environment

BG95&BG77-QuecOpen solutions only support the LLVM compiler, which is provided by Qualcomm™. Customers can request this compiler from Quectel.

Table 1: Compiling Environment Requirement

Component	Source or Binary Only	Toolchain Required for Building Source	Supported Build Hosts
QuecOpen SDK	Source	LLVM 4.0.3	Windows™ 7/ Windows™ 10/ Linux

3.1. LLVM Installation

Before install LLVM, please request this LLVM compiler tool package from Quectel.

3.2. Download and Install Python

3.2.1. Download Python

Open the Python download page shown as below to download the corresponding revision of Python for Windows/Linux: https://www.python.org/download/releases/2.7/.

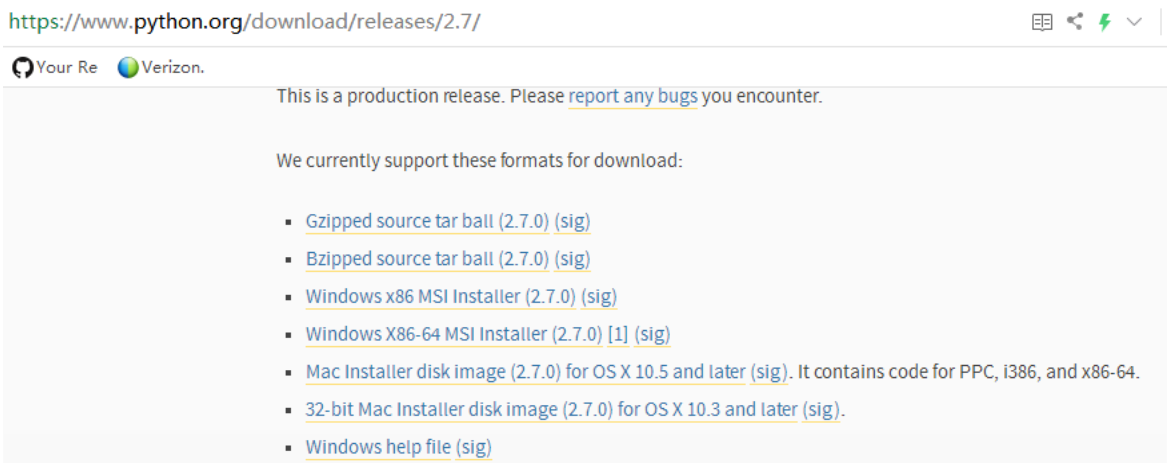

Figure 2: Python Download Page Screenshot

Download x86/x86-64 versions as needed.

3.2.2. Install Python

After download is completed, please follow the steps illustrated below to finish installation.

Step 1: Run "**Python-2.7.0.msi**" program and also please choose a few installation parameters, then click "**Next**".

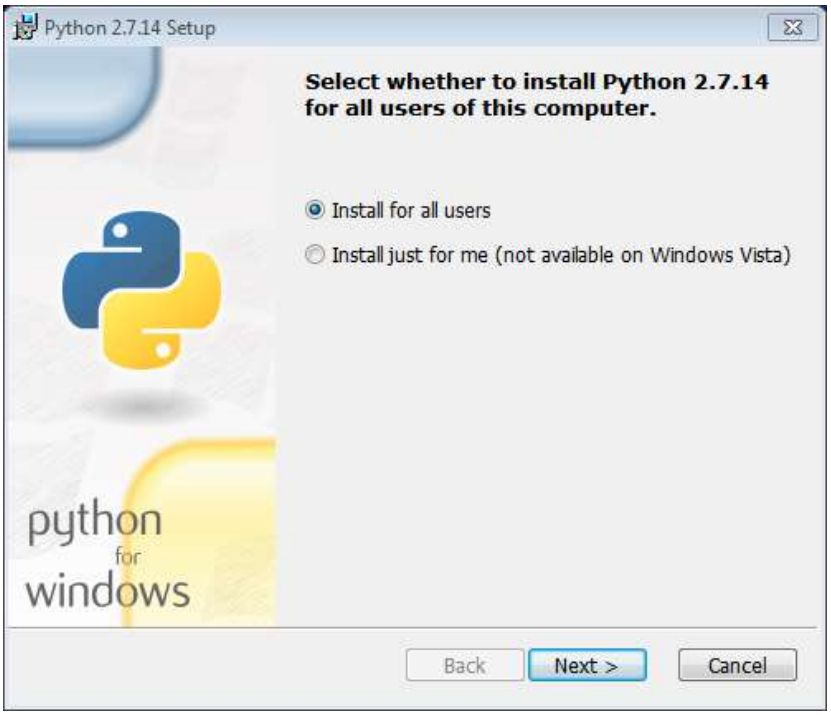

Figure 3: Python Setup

Step 2: Select the directory where Python is to be installed.

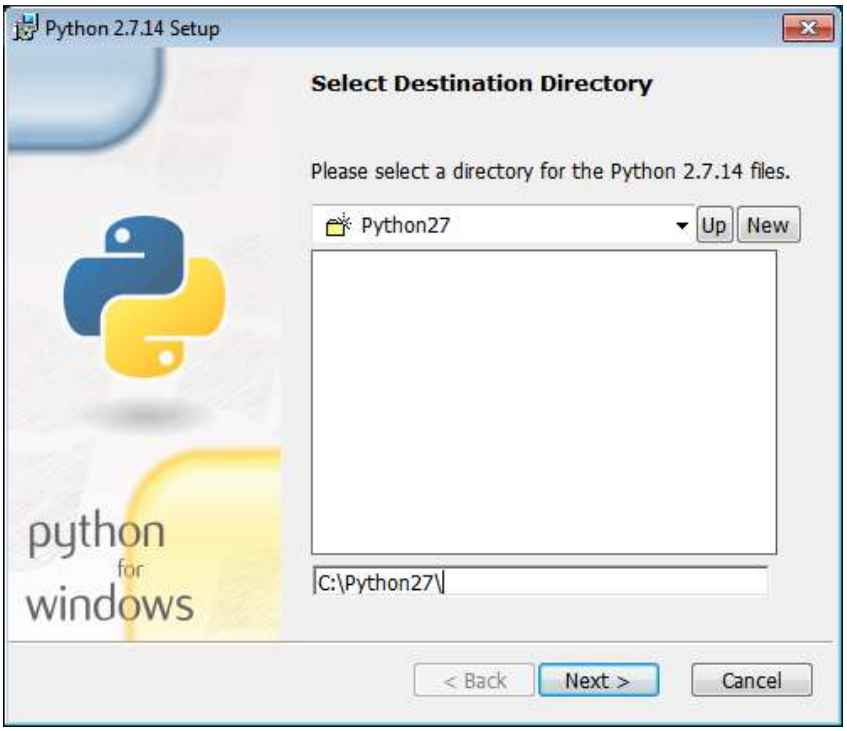

Figure 4: Select Installation Directory

Step 3: Options for customization. Please keep the default options.

Figure 5: Options for Customization

Step 4: Please wait during installation process.

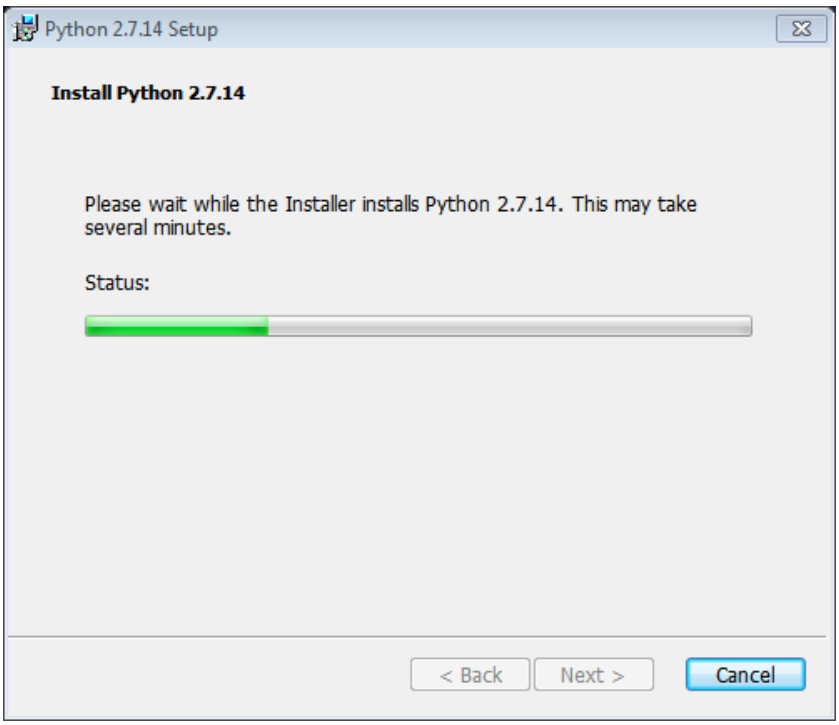

Figure 6: Installing

Step 5: Complete installation.

Figure 7: Installation Completed

4 Building QuecOpen Application

4.1. QuecOpen SDK Package

The following shows the folder structure of *Quectel_BG95_QuecOpen_SDK_Package* which is created for non-licensed customers.

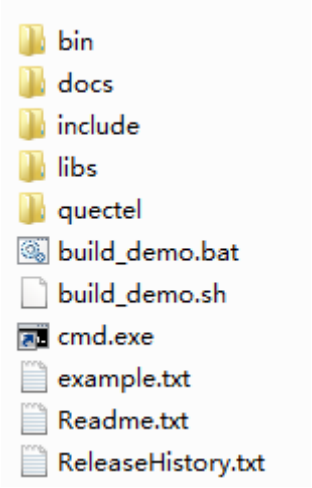

Figure 8: Folder Structure of BG95-QuecOpen SDK Package

Table 2: Description of BG95-QuecOpen SDK Package Directories

Directories	Description/Function
bin	Application will be created in this folder after successful compilation
docs	QuecOpen related documents
include	Header files needed for compilation provided by Quectel
libs	Required libraries should be copied here
quectel	Quectel example source codes
build_demo.bat	Batch script for building Quectel example
build_demo.sh	Shell script for building Quectel example

example.txt	Configuration file for compilation options of examples
Readme.txt	Key information for QuecOpen SDK package
ReleaseHistory.txt	Release history of SDK package

4.2. Building QuecOpen User Application

Before application building, customers must set a correct path for the compiler tools in the build script.

In *build_demo.bat*:

```
set TOOL_PATH_ROOT=C:\compile_tools
set TOOLCHAIN_PATH=%TOOL_PATH_ROOT%\LLVM\4.0.3\bin
set
TOOLCHAIN_PATH_STANDARdS=%TOOL_PATH_ROOT%\LLVM\4.0.3\armv7m-none-eabi\libc\include
set LLVMLIB=%TOOL_PATH_ROOT%\LLVM\4.0.3\lib\clang\4.0.3\lib
set LLVMLINK_PATH=%TOOL_PATH_ROOT%\LLVM\4.0.3\tools\bin
set PYTHON_PATH=%TOOL_PATH_ROOT%\Python27\python.exe
```

To build the example codes in the *Quectel_BG95_QuecOpen_SDK_Package*, customers just need to run the following command from command line in Windows OS:

The following help commands can be used to know which examples are supported in this SDK package:

```
help build in Windows:
build_demo.bat llvm help
```

After input the help command, tips shown as below will be available:

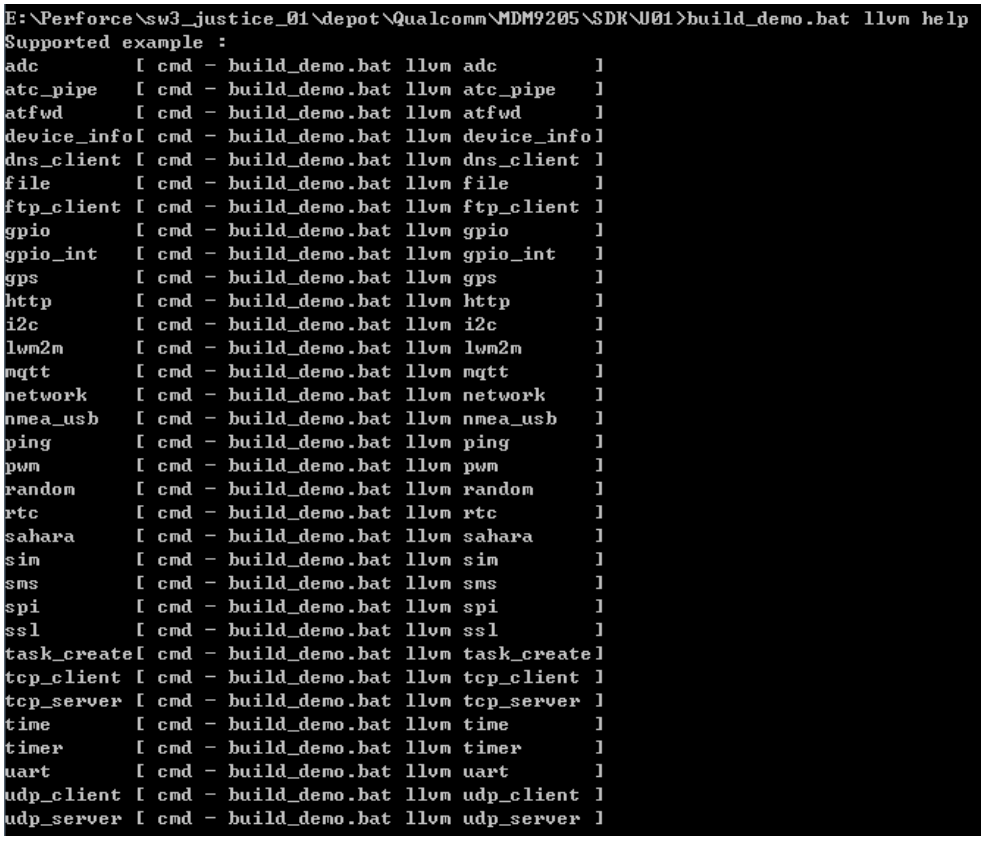

Figure 9: Help Tips in Windows OS

NOTE

The above sample list screenshot is only for reference, please refer to SDK for specific contents.

Take UART compilation as an example:
In Windows:

New build:
build_demo.bat llvm uart

Clean build:
build_demo.bat llvm -c

Once the build process is completed, the application binary (e.g., *quectel_demo_uart.bin*) will be created under the path/*bin*.

4.3. Running QuecOpen Application

There are two methods to run QuecOpen application in BG95&BG77, one is to load binary image by alternating file systems, and the other is to load binary image from flash, which is under development.

4.3.1. Load Binary Image by Alternate File Systems

To run the QuecOpen application binary file with the method of loading binary image by alternate file systems, customers only need to upload the application binary image and *oem_app_path.ini* into the alternate file systems of BG95&BG77 by QEFS explorer, manually or with FILE AT commands.

File oem_app_path.ini contains the name of application binary image. This file must be stored in the */datatx/* directory. And only binary files under /datax/ directory can be loaded. Take UART application as an example, the content of *oem_app_path.ini* should be *quectel_demo_uart.bin*.

After uploading these two files into alternate file systems, reboot BG95&BG77 and the application binary image will be loaded into RAM and started by the Module Loader.

4.3.2. Loading Binary Image from Flash

To run the QuecOpen application binary file with the method of loading binary image from NAND flash, refer to *Quectel_BG95&BG77-QuecOpen_NAND_Flash_Loading_Application_Notes* for details.

5 Updating QuecOpen Application

This section will be updated in a future release.

6 BG95&BG77-QuecOpen Pin Mapping

This section mainly introduces the GPIO mapping of the BG95&BG77-QuecOpen, also including the mapping of related peripherals, such as UART, IIC, SPI and so on.

Table 3: Definition of I/O Parameters

Type	Description
IO	Bidirectional
DI	Digital Input
DO	Digital Output
PI	Power Input
PO	Power Output
AI	Analog Input
AO	Analog Output
OD	Open Drain
BCMOS	Bidirectional digital with CMOS input
PU	Pull-Up
PD	Pull-Down

6.1. Pin Mapping of BG95

The following tables show the pin definition, and GPIO pull up/down resistance of BG95-QuecOpen module. This table also includes the mapping of related peripherals

Table 4: BG95 Multiplexing Pins

Pin Name	Pin No.	Function1	Function2	Function3	Function4	Reset[1)]	Interrupt	Boot
GPIO1	4	GPIO_24	/	/	/	B-PD	No	No
GPIO2	5	GPIO_21	/	/	/	B-PD	Yes	No
GPIO3	6	GPIO_22	/	/	/	B-PD	Yes	No
GPIO4	7	GPIO_23	/	/	/	B-PD	No	No
GPIO5	18	GPIO_3	/	/	I2C1_SCL	B-PD	No	No
GPIO6	19	GPIO_2	/	/	I2C1_SDA	B-PD	Yes	No
GPIO7	22	GPIO_1	UART1_RXD	/	/	B-PD	Yes	No
GPIO8	23	GPIO_0	UART1_TXD	/	/	B-PD	Yes	No
GPIO9	25	GPIO_6	/	SPI1_CS_N	/	B-PD	Yes	No
GPIO10	26	GPIO_7	/	SPI1_CLK	/	B-PD	No	No
GPIO11	27	GPIO_4	UART3_TXD	SPI1_MOSI	/	B-PD	Yes	Yes
GPIO12	28	GPIO_5	UART3_RXD	SPI1_MISO	/	B-PD	Yes	No
GPIO13	40	GPIO_15	/	SPI2_CLK	/	B-PD	No	No
GPIO14	41	GPIO_14	/	SPI2_CS_N	/	B-PD	Yes	No
GPIO15	64	GPIO_12	UART2_TXD	SPI2_MOSI	/	B-PD	No	No
GPIO16	65	GPIO_13	UART2_RXD	SPI2_MISO	/	B-PD	Yes	No
GPIO17	66	GPIO_50	PWM	/	/	B-PD	Yes	No
GPIO18	85	GPIO_52	/	/	/	B-PD	Yes	No
GPIO19*	86	GPIO_36	/	/	/	B-PD	Yes	No
GPIO20*	87	GPIO_40	/	/	/	B-PD	No	No
GPIO21*	88	GPIO_41	/	/	/	B-PD	No	No

NOTES

1. Functions 1, function 2, function 3 and function 4 will take effect only after software configuration.
2. [1)] Please refer to ***Table 3*** for more details about the symbol description.
3. "*" means under development.
4. "/" means not supported.

6.1.1. GPIOs

BG95-QuecOpen supports 21 GPIOs. Customers can configure each GPIO by QAPI in their own applications. As an output function, customers can configure the driver strength for specified GPIO.

6.1.2. UART Interfaces

BG95 provides four UART interfaces: Main UART, UART1, UART2 and UART3.

- Main UART interface can only be used for AT command communication.
- UART1, UART2 and UART3 interfaces are used for communication and data transmission with peripheral, and can also be multiplexed into other functions.

The following tables show the pin definition of the four UART interfaces.

Table 5: BG95 Pin Definition of Main UART Interface

Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DTR	30	DI	Data terminal ready (sleep mode control)	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
RXD	34	DI	Receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
TXD	35	DO	Transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.
CTS	36	DO	Clear to send	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.

RTS	37	DI	Request to send	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
DCD	38	DO	Data carrier detection	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.
RI	39	DO	Ring indication signal	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.

NOTE

Main UART interface is only used for AT Command communication. It cannot be configured or used in customers own application.

Table 6: BG95 Pin Definition of UART1 Interface

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4
GPIO7	22	DI	GPIO_1	UART1_RXD	/	/
GPIO8	23	DO	GPIO_0	UART1_TXD	/	/

NOTES

1. In QuecOpen application, use *QT_QAPI_UART_PORT_01* to select and configure UART1.
2. UART1 interface does not support flow control.

Table 7: BG95 Pin Definition of UART2 Interface

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4
GPIO15	64	DO	GPIO_12	UART2_TXD	SPI2_MOSI	/
GPIO16	65	DI	GPIO_13	UART2_RXD	SPI2_MISO	/

NOTES

1. In QuecOpen application, use *QT_QAPI_UART_PORT_02* to select and configure UART2.
2. UART2 interface does not support flow control.

Table 8: BG95 Pin Definition of UART3 Interface

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4
GPIO11	27	DO	GPIO_4	UART3_TXD	SPI1_MOSI	/
GPIO12	28	DI	GPIO_5	UART3_RXD	SPI1_MISO	/

NOTES

1. In QuecOpen application, use *QT_QAPI_UART_PORT_03* to select and configure UART3.
2. UART3 interface does not support flow control.

6.1.3. I2C Interfaces

BG95-QuecOpen provides one Inter-Integrated Circuit (I2C) interface for communication, which support high-speed mode and do not support multi-master. I2C interface uses GPIOs configured as open-drain outputs, and the pull-up resistors should be provided externally.

The following tables show the pin definition.

Table 9: BG95 Pin Definition of I2C1 Interface

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4
GPIO5	18	IO	GPIO_3	/	/	I2C1_SCL
GPIO6	19	IO	GPIO_2	/	/	I2C1_SDA

NOTE

In QuecOpen application, use *QT_QAPI_I2CM_PORT_01* to select and configure I2C1.

6.1.4. SPI Interfaces

BG95-QuecOpen provides two SPI interfaces which support only master mode with a maximum clock frequency up to 50MHz.

The following tables show the pin definition.

Table 10: BG95 Pin Definition of SPI1 Interface

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4
GPIO9	25	IO	GPIO_6	/	SPI1_CS_N	/
GPIO10	26	IO	GPIO_7	/	SPI1_CLK	/
GPIO11	27	IO	GPIO_4	UART3_TXD	SPI1_MOSI	/
GPIO12	28	IO	GPIO_5	UART3_RXD	SPI1_MISO	/

NOTE

In QuecOpen application, use *QT_QAPI_SPIM_PORT_01* to select and configure SPI1.

Table 11: BG95 Pin Definition of SPI2 Interface

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4
GPIO13	40	IO	GPIO_15	/	SPI2_CLK	/
GPIO14	41	IO	GPIO_14	/	SPI2_CS_N	/
GPIO64	64	IO	GPIO_12	UART2_TXD	SPI2_MOSI	/
GPIO65	65	IO	GPIO_13	UART2_RXD	SPI2_MISO	/

NOTE

In QuecOpen Application, use *QT_QAPI_SPIM_PORT_02* to select and configure SPI2.

6.2. Pin Mapping of BG77

6.2.1. GPIOs

BG77-QuecOpen supports 34 GPIOs. Customers can configure each GPIO by QAPI in their own applications. As an output function, customers can configure the driver strength for specified GPIO.

Table 12: BG77 Multiplexing Pins

Pin Name	Pin No.	Function1	Function2	Function3	Function4	Reset[1)]	Interrupt	Boot
GPIO1	1	GPIO_14	/	SPI2_CS_N	/	B-PD	Yes	No
GPIO2	2	GPIO_22	/	/	/	B-PD	Yes	No
GPIO3	3	GPIO_24	/	/	/	B-PD	No	No
GPIO4	4	GPIO_13	UART2_RXD	SPI2_MISO	/	B-PD	Yes	No
GPIO5	5	GPIO_2	/	/	I2C1_SDA	B-PD	Yes	No
GPIO6	8	GPIO_5	UART3_RXD	SPI1_MISO		B-PD	Yes	No
GPIO7	9	GPIO_7		SPI1_CLK	/	B-PD	No	No
GPIO8	33	GPIO_52	PWM	/	/	B-PD	Yes	No
GPIO9	34	GPIO_23	/		/	B-PD	No	No
GPIO10	35	GPIO_21	/		/	B-PD	Yes	No
GPIO11	36	GPIO_12	UART2_TXD	SPI2_MOSI	/	B-PD	No	No
GPIO12	37	GPIO_3	/	/	I2C1_SCL	B-PD	No	No
GPIO13	40	GPIO_4	UART3_TXD	SPI1_MOSI	/	B-PD	Yes	Yes
GPIO14	41	GPIO_27	/		/	B-PD	Yes	No
GPIO15	48	GPIO_33			/	B-PD	No	No
GPIO16	49	GPIO_34			/	B-PD	No	No
GPIO17	50	GPIO_36		/	/	B-PD	Yes	No
GPIO18	51	GPIO_37	/	/	/	B-PD	No	No
GPIO19	57	GPIO_15	/	SPI2_CLK	/	B-PD	No	No
GPIO20	60	GPIO_0	UART1_TXD	/	/	B-PD	Yes	No
GPIO21	61	GPIO_1	UART1_RXD	/	/	B-PD	Yes	No

GPIO22	63	GPIO_6	/	SPI1_CS_N	/	B-PD	Yes	No
GPIO23	67	GPIO_31	/	/	/	B-PD	No	No
GPIO24	68	GPIO_38	/	/	/	B-PD	No	Yes
GPIO25	69	GPIO_51	/	/	/	B-PD	Yes	No
GPIO26	70	GPIO_35	/	/	/	B-PD	No	No
GPIO27	71	GPIO_42	/	/	/	B-PD	No	No
GPIO28	77	GPIO_28	/	/	/	B-PD	Yes	No
GPIO29	80	GPIO_32	/	/	/	B-PD	No	Yes
GPIO30	81	GPIO_40	/	/	/	B-PD	No	No
GPIO31	82	GPIO_47	/	/	/	B-PD	Yes	No
GPIO32	91	GPIO_45	/	/	/	B-PD	No	No
GPIO33	92	GPIO_46	/	/	/	B-PD	Yes	No
GPIO34	93	GPIO_50	/	/	/	B-PD	Yes	No

NOTES

1. Functions 1, function 2, function 3 and function 4 will take effect only after software configuration.
2. [1)] Please refer to ***Table 3*** for more details about the symbol description.
3. "*" means under development.
4. "/" means not supported.

6.2.2. UART Interfaces

BG77 provides four UART interfaces: Main UART, UART1, UART2 and UART3.

- Main UART interface can only be used for AT command communication.
- UART1, UART2 and UART3 interfaces are used for communication and data transmission with peripheral, and can also be multiplexed into other functions.

The following tables show the pin definition of the four UART interfaces.

Table 13: BG77 Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
DTR	62	DI	Data terminal ready (sleep mode control)	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
RXD	6	DI	Receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
TXD	7	DO	Transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.
CTS	39	DO	Clear to send	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.
RTS	38	DI	Request to send	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
DCD	90	DO	Data carrier detection	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.
RI	76	DO	Ring indication signal	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.

NOTE

Main UART interface is only used for AT Command communication. It cannot be configured or used in customers own application.

Table 14: BG77 Pin Definition of UART1 Interface

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4
GPIO21	61	DI	GPIO_1	UART1_RXD	/	/
GPIO20	60	DO	GPIO_0	UART1_TXD	/	/

NOTES

1. In QuecOpen application, use *QT_QAPI_UART_PORT_01* to select and configure UART1.
2. UART1 interface does not support flow control.

Table 15: BG77 Pin Definition of UART2 Interface

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4
GPIO11	36	DO	GPIO_12	UART2_TXD	SPI2_MOSI	/
GPIO4	4	DI	GPIO_13	UART2_RXD	SPI2_MISO	/

NOTES

1. In QuecOpen application, use *QT_QAPI_UART_PORT_02* to select and configure UART2.
2. UART2 interface does not support flow control.

Table 16: BG77 Pin Definition of UART3 Interface

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4
GPIO13	40	DO	GPIO_4	UART3_TXD	SPI1_MOSI	/
GPIO6	8	DI	GPIO_5	UART3_RXD	SPI1_MISO	/

NOTES

1. In QuecOpen application, use *QT_QAPI_UART_PORT_03* to select and configure UART3.
2. UART3 interface does not support flow control.

6.2.3. I2C Interfaces

BG77-QuecOpen provides one Inter-Integrated Circuit (I2C) interface for communication, which support high-speed mode and do not support multi-master. I2C interface uses GPIOs configured as open-drain outputs, and the pull-up resistors should be provided externally.

The following table show the pin definition.

Table 17: BG77 Pin Definition of I2C1 Interface

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4
GPIO12	37	IO	GPIO_3	/	／	I2C1_SCL
GPIO5	5	IO	GPIO_2	/	/	I2C1_SDA

NOTE

In QuecOpen application, use *QT_QAPI_I2CM_PORT_01* to select and configure I2C1.

6.2.4. SPI Interfaces

BG77-QuecOpen provides two SPI interfaces which support only master mode with a maximum clock frequency up to 50MHz.

The following tables show the pin definition.

Table 18: BG77 Pin Definition of SPI1 Interface

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4
GPIO22	63	IO	GPIO_6	/	SPI1_CS_N	/
GPIO7	9	IO	GPIO_7	/	SPI1_CLK	/
GPIO13	40	IO	GPIO_4	UART3_TXD	SPI1_MOSI	/
GPIO6	8	IO	GPIO_5	UART3_RXD	SPI1_MISO	/

NOTE

In QuecOpen application, use *QT_QAPI_SPIM_PORT_01* to select and configure SPI1.

Table 19: BG77 Pin Definition of SPI2 Interface

Pin Name	Pin No.	I/O	Function 0	Function 1	Function 2	Function 3
GPIO19	57	IO	GPIO_15	/	SPI2_CLK	/
GPIO1	1	IO	GPIO_14	/	SPI2_CS_N	/
GPIO11	36	IO	GPIO_12	UART2_TXD	SPI2_MOSI	/

GPIO4	4	IO	GPIO_13	UART2_RXD	SPI2_MISO	/

NOTE

In QuecOpen Application, use *QT_QAPI_SPIM_PORT_02* to select and configure SPI2.

7 Available Memory Mapping for QuecOpen Application

BG95&BG77 have fine-tuned the memory space division of products to meet the diverse needs of customers, including the ROM space and RAM space.

Quectel provides four areas for customers to use in QuecOpen solutions:

Figure 10: Memory Space for QuecOpen App

ROM for QuecOpen application: Used to store customer QuecOpen application image.
ROM for configuration: Used to store the key configuration data for customer QuecOpen application.
FS: Used to store customer some temporary configuration, files or application log.
RAM: RAM space.

Table 20: Available Memory Mapping for QuecOpen Application

SKT	ROM for QuecOpen Application (MB)	ROM for QuecOpen Configuration (KB)	File System	RAM SIZE
BG95-M1	1.5	128	4.5	3
BG95-M2	1.5	128	2.5	3
BG77	1.5	128	2.5	3
BG95-M3	1.25	128	1.5	2.5

NOTE

All data table are under condition without VoLTE/Audio function.

8 Appendix A References

Table 21: Related Documents

SN	Document Name	Remark
[1]	Quectel_BG95_QEFS_Explorer_User_Guide	QEFS Explorer tool user guide
[2]	Quectel_BG95_Hardware_Design	BG95 QuecOpen Hardware Design
[3]	80-p8101-32_d_qualcomm_application_programming_interface_for_mdm9206_tx_3.2	Qualcomm QAPI Specification
[4]	Quectel_BG95&BG77_AT_Commands_Manual	Quectel BG95&BG77 AT Commands Manual

Table 22: Terms and Abbreviations

Abbreviation	Description
API	Application Programming Interface
HTTP	Hyper Text Transfer Protocol
OS	Operating System
QAPI	Qualcomm™ Application Programming Interface
GPIO	General-Purpose Input/Output
MCU	Microcontroller Unit
RAM	Random Access Memory
ROM	Read Only Memory
SDK	Software Development Kit
SPI	Serial Peripheral Interface