



# Computer and control systems department

Faculty of Engineering

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## Digital logic system for product classification and pricing in a smart factory

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## **Abstract:**

The project is a logic digital system simulation designed to model a factory equipped with two IR sensors placed at different heights. The lower sensor detects short products, while the higher sensor detects tall products. Each product type has a fixed price: \$2 for the taller product (B) and \$1 for the shorter product (A). The system classifies the products based on the signals from the IR sensors.

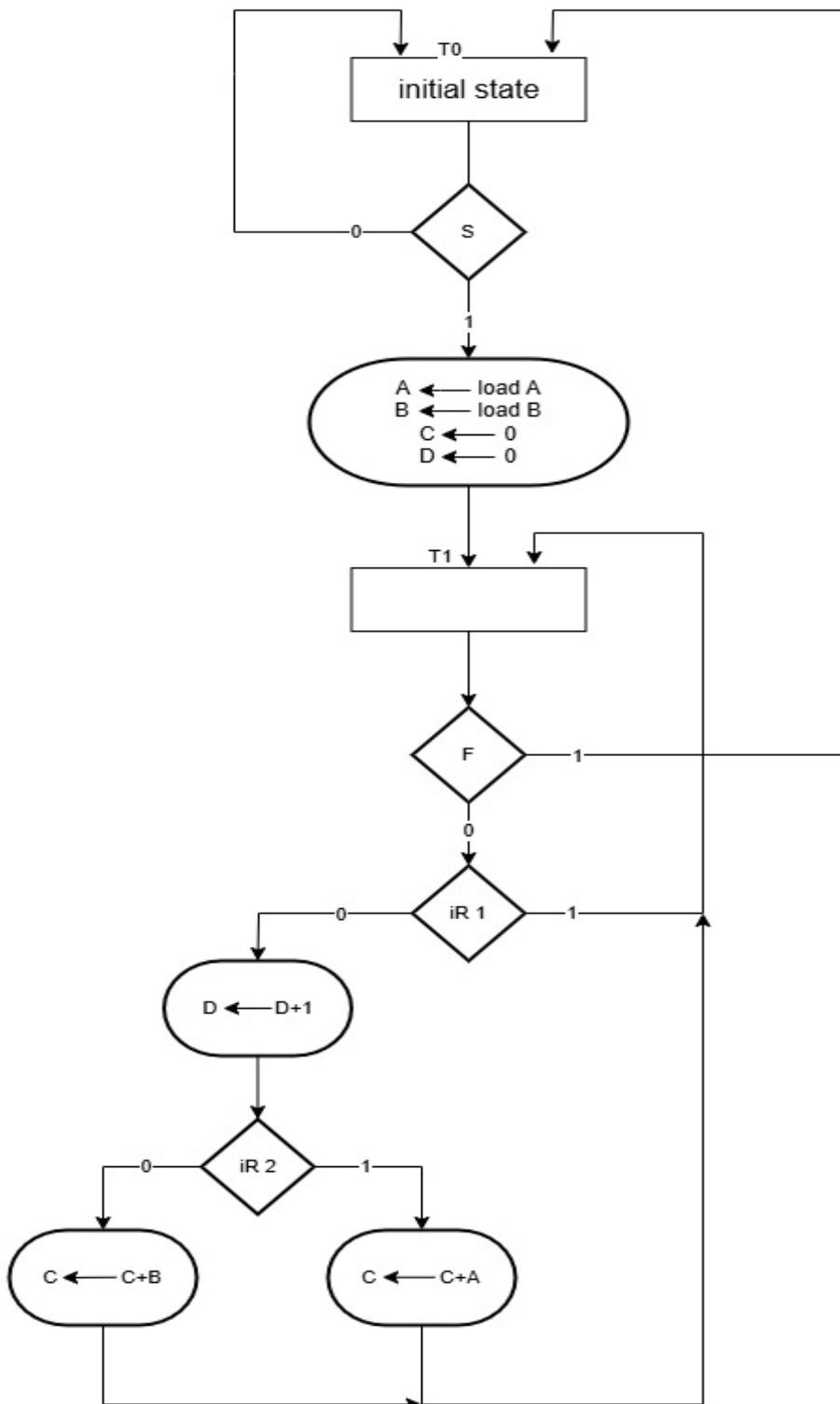
A register (C) stores the total price of all sold items, calculated using a full adder circuit. The adder takes two inputs: the previous total stored in register C and the price of the current item. To determine the current price, a multiplexer is used with its inputs holding the prices of the two product types.

The multiplexer selects the appropriate price based on the signal from the sensors via the select line.

Additionally, a counter keeps track of the total number of items sold, displaying the count on a 7-segment display. The system also includes a clock pulse (CP) generated by a 555 timer IC to synchronize operations. This setup ensures accurate product classification, pricing, and tracking, enhancing efficiency in a simulated factory environment.

# System Modeling:

## 1. ASM Chart



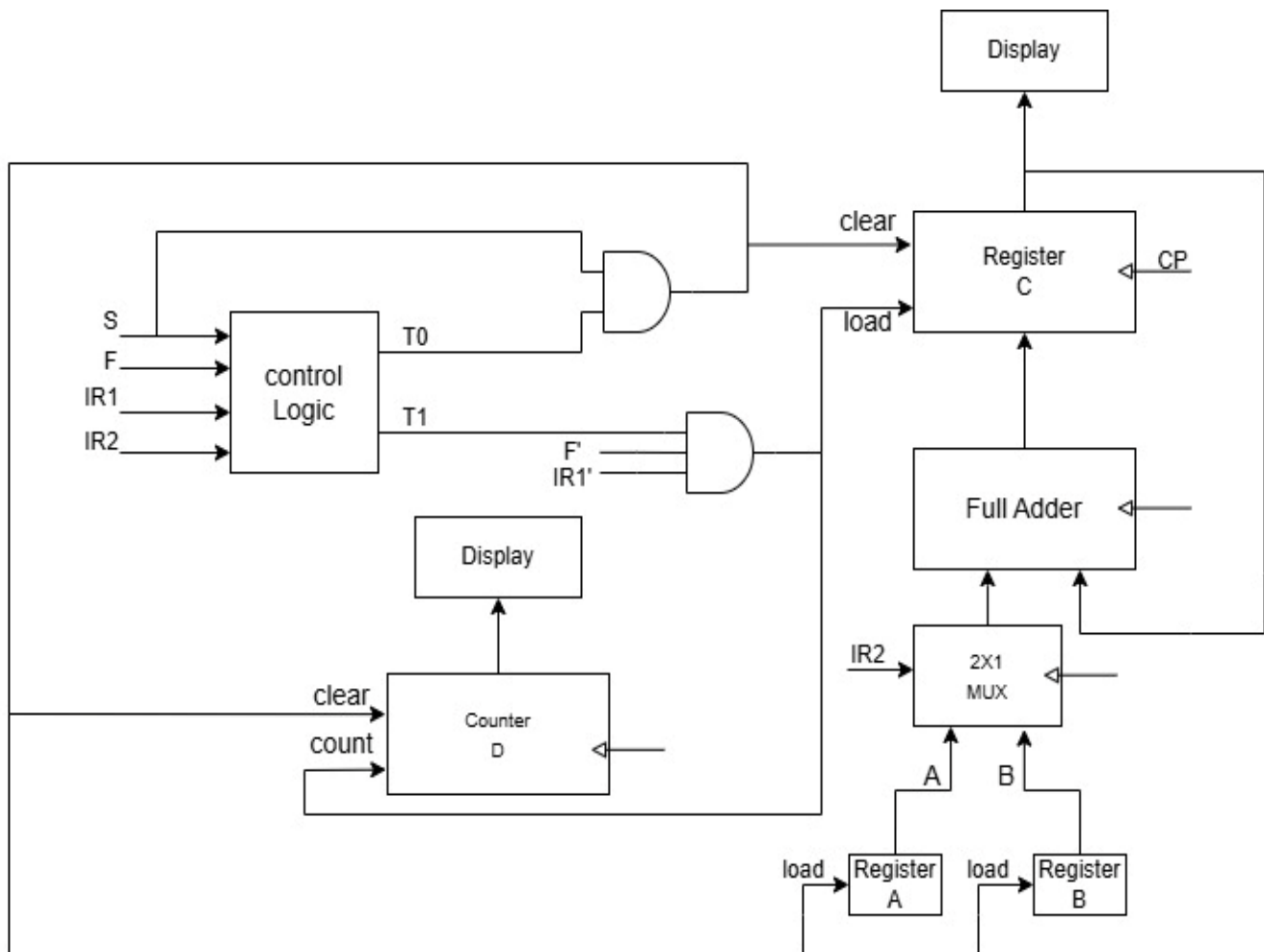
### Where:

- $S$  is the starting signal.
- $F$  is the finish signal.
- $A$  is the price for the first product.
- $B$  is the price for the second product.
- $C$  is the total price of the sold products.
- $D$  is counter for all products.
- $iR\ 1$  &  $iR\ 2$  are system inputs.
- $T_0$  &  $T_1$  are the system states

## 2. Data processor:

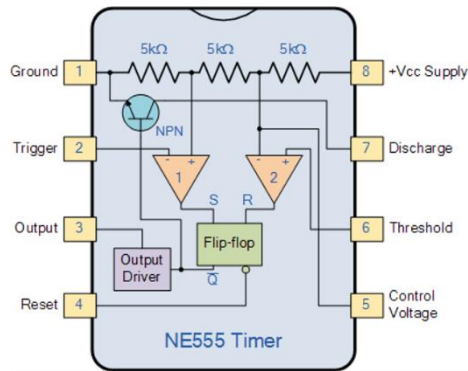
We need:

- 555 timer IC
- Register (IC 74175)
- 4X1 Multiplexer (IC 74153)
- Full adder (IC 7483)
- 7-segment & Decoder
- Synchronous up counter (IC 7490)
- Two IR sensors.

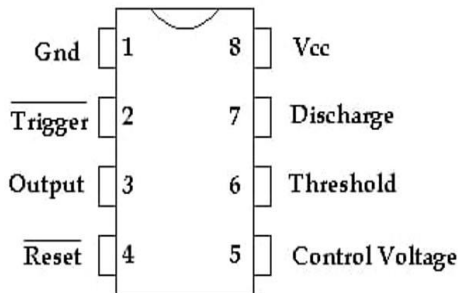


# Components & Datasheets:

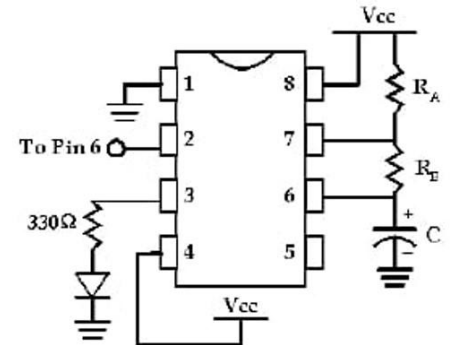
## 1- 555 Timer



Internal structure



Pinout



connections

## 2- Register (IC 74175)

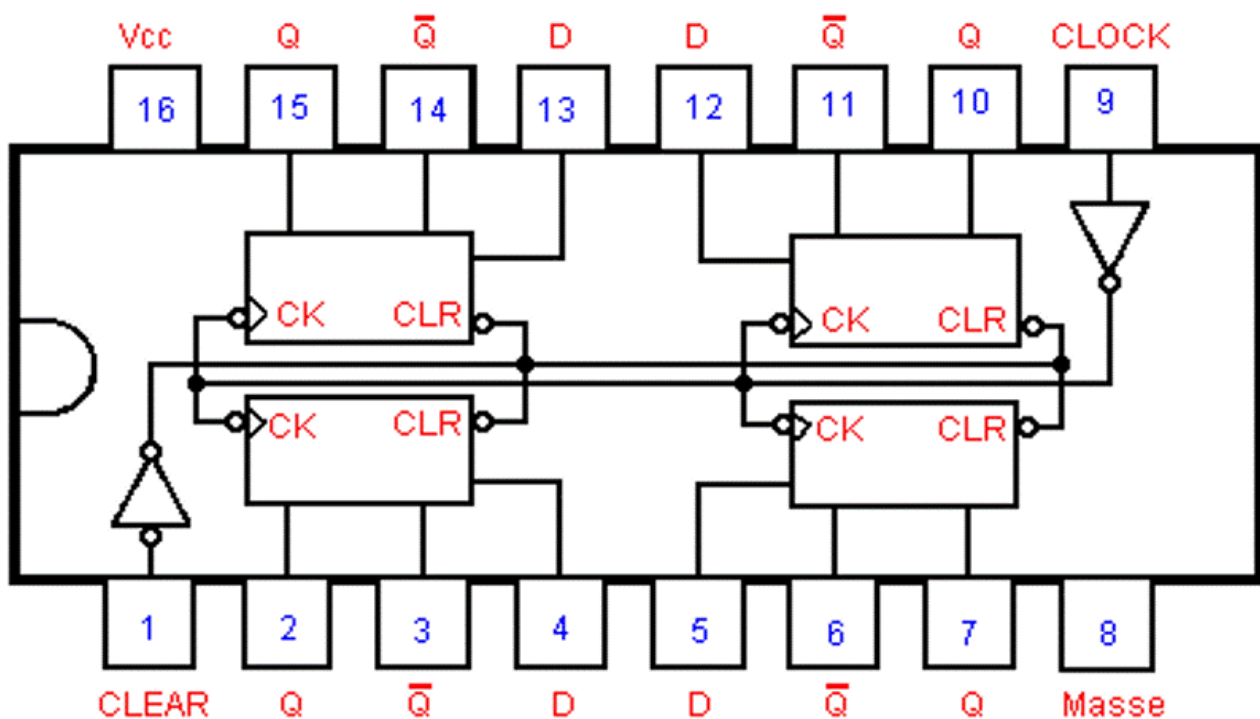
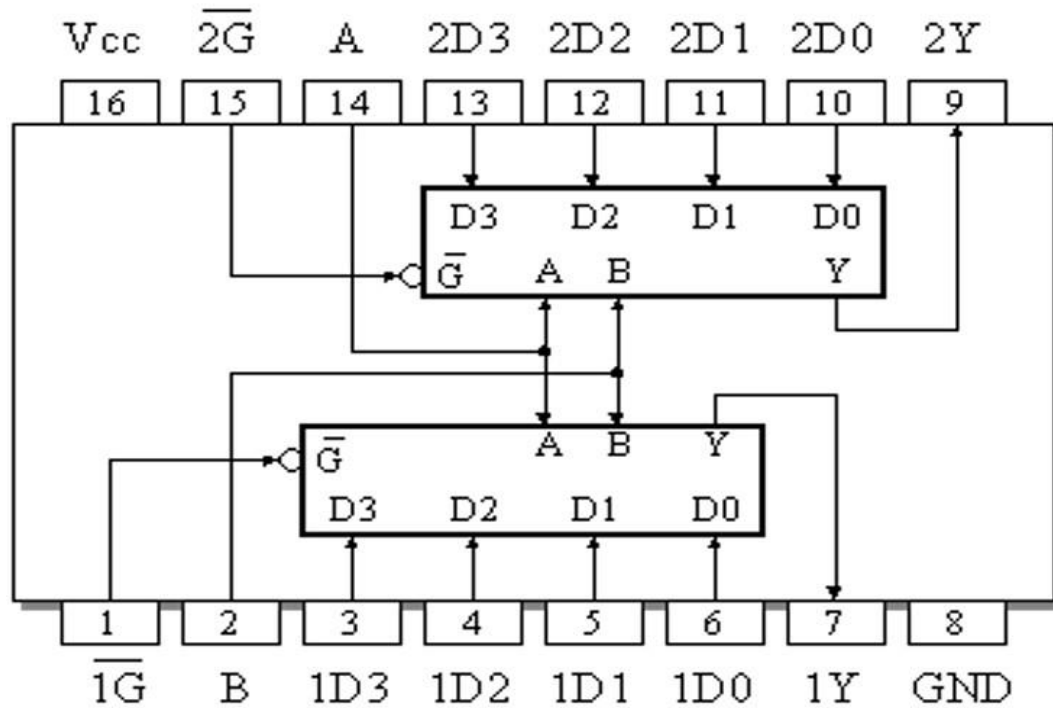
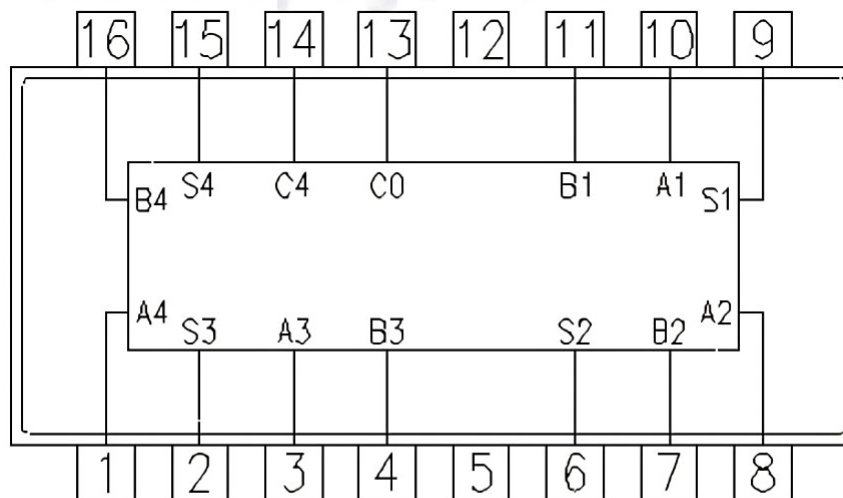


Fig. 51. - Brochage du circuit intégré 74175.

### 3- 4X1 Multiplexer (IC 74153)



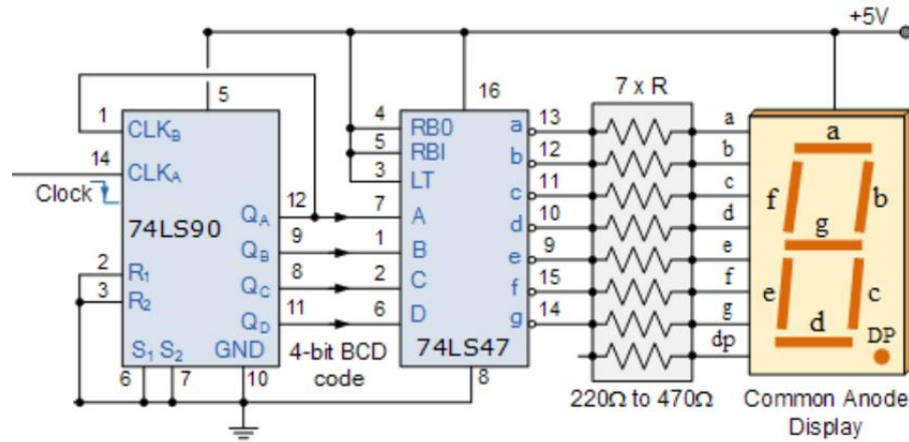
### 4- Full Adder (IC 7483)



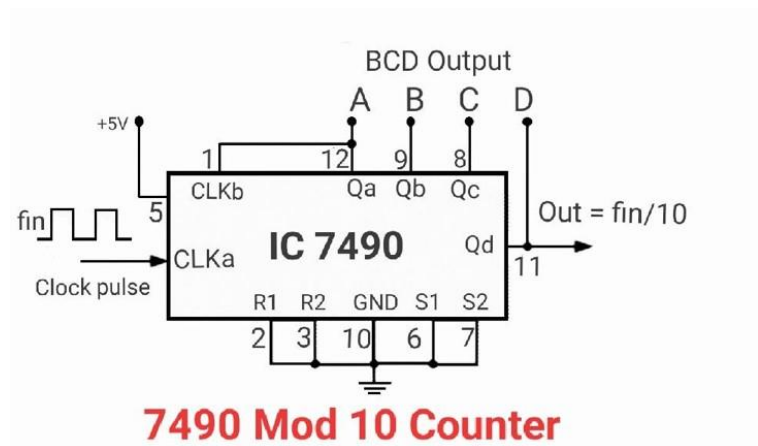
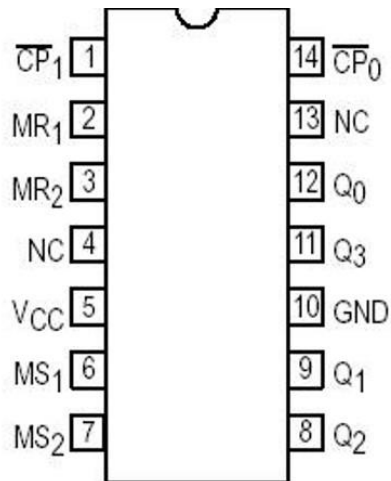
7483

4-Bit Full Adder

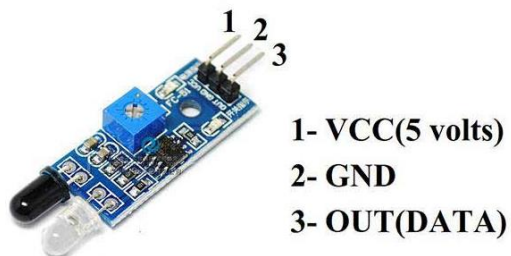
## 5- Counter using 7-segment display



## 6- Synchronous Counter (IC 7490)

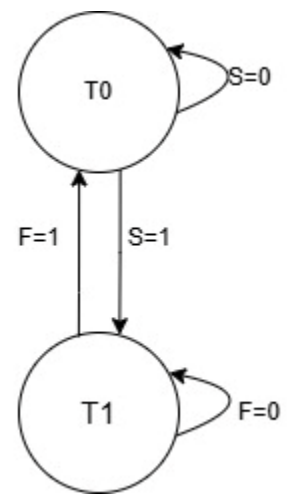


## 7- IR sensor



### 3. Control Logic

The control logic design is based on the "one flip-flop per state" method, which simplifies the process and provides a clear understanding of state transitions. This approach begins by converting the ASM chart into a state diagram. The state diagram provides a visual representation of the states ( $T_0$  and  $T_1$ ) and their transitions, which depend on specific input conditions. The figure illustrates the state diagram, and the following equations are used to define the transitions.



- $D_0 = T_0 S' + T_1 F$
- $D_1 = T_1 F' + T_0 S$

#### State Transitions:

##### - State $T_0$ :

If  $S = 0$  stays in  $T_0$

If  $S = 1$  transition to  $T_1$

##### - State $T_1$ :

If  $F = 0$  stay in  $T_1$

If  $F = 1$  transition to  $T_0$



## Complete circuit in Action:

