Sneak peek behind TensorFlow Python API

Accelerator integrator perspective

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Who am I

AI Software Engineering Manager

Yes, I still write code ;)

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All views expressed herein are those of my own and do not represent the opinions of any entity whatsoever with which I have been, am now, or will be affiliated.

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- Supports multiple devices like:
  - CPU
  - GPU
  - Habana Gaudi (a.k.a. HPU, using Habana TF plugin)

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Implemented in C++

TensorFlow development resources

`https://github.com/tensorflow/tensorflow`

`https://www.tensorflow.org/api_docs/`

`https://www.tensorflow.org/guide`

Sample model

```python
num_classes = 5

model = Sequential([
  layers.experimental.preprocessing.Rescaling(1./255, input_shape=(img_height, img_width, 3)),
  layers.Conv2D(16, 3, padding='same', activation='relu')
])

model.compile(optimizer='adam',
              loss=tf.keras.losses.SparseCategoricalCrossentropy(from_logits=True),
              metrics=['accuracy'])
```

Modes of execution

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Pure eager

tf.function graph eager

Legacy graph mode (TF1.x)

Eager tf.function graph mode

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Achieved by marking function with tf.function annotation

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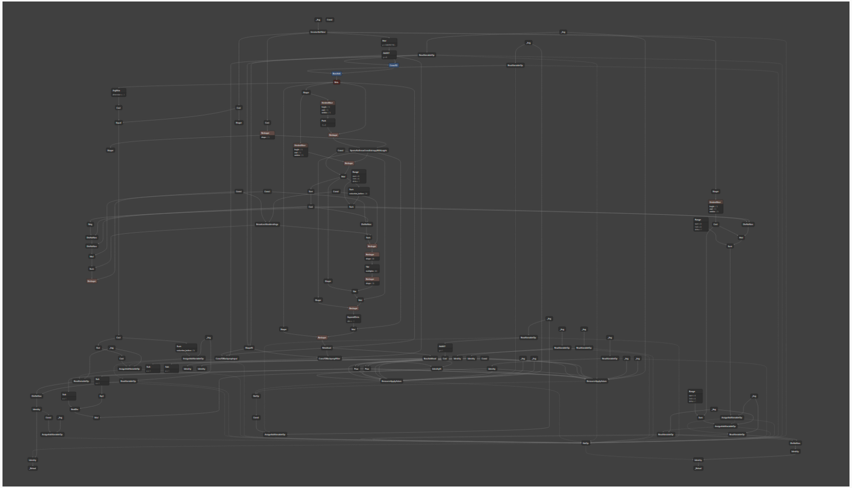
Before execution optimization passes are run on the graph

Pure eager mode

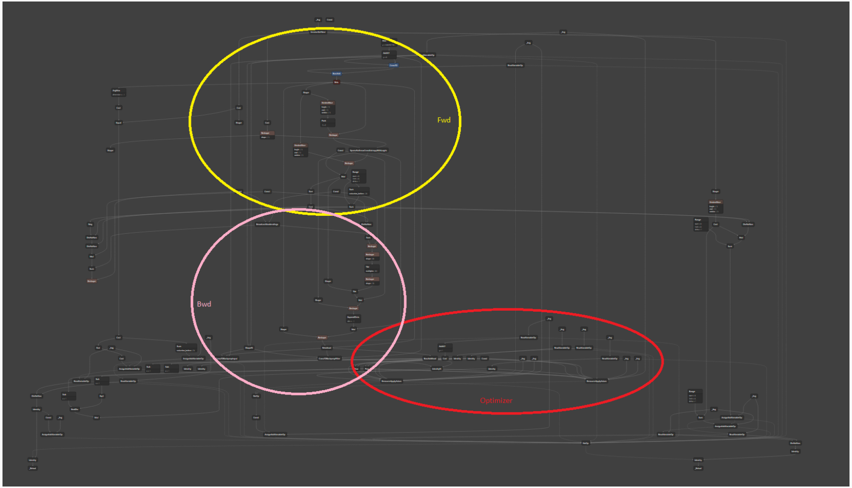
- Operators are executed one by one
- Up to TF2.9: No optimization passes performed
- Post TF2.9 or TF2.9 with TF_RUN_EAGER_OP_AS_FUNCTION flag set
  - Each operator is encapsulated in tf.function
  - All optimization passess are being run on such operator
  - TensorFlow developers effort to unify execution

TensorFlow model graph

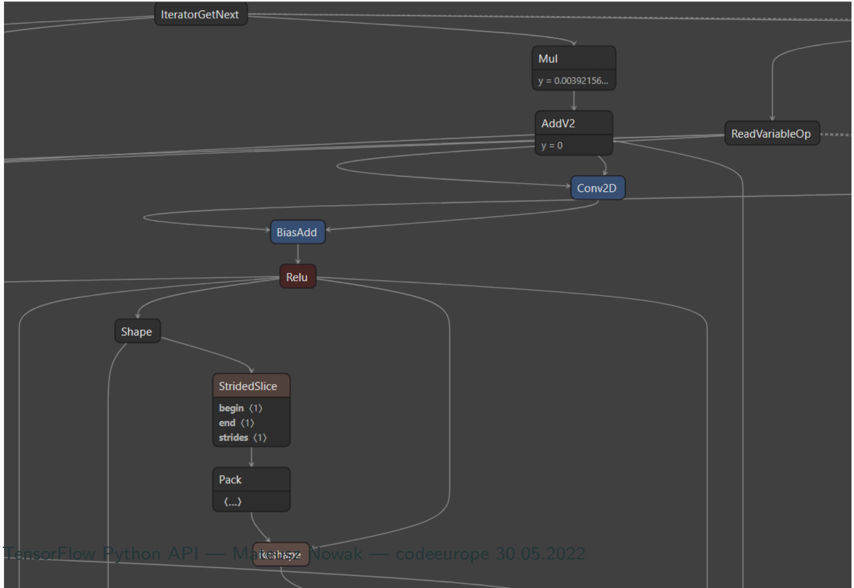
Sample model graph



Sample model graph - phases



Sample model graph - zoom in



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- Each device supply its own kernels
  - Exception: DEFAULT_DEVICE kernels

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Using REGISTER_OP macro

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Note: This is low level operator, high level operators calling low level ones can be separately defined on python level

Operator registration example

```
REGISTER_OP("MaxPoolGradV2")
    .Attr(GetPaddingAttrString())
    .Attr(GetConvnetDataFormatAttrString())
    .Input("orig_input: T")
    .Input("orig_output: T")
    .Input("grad: T")
    .Input("ksize: int32")
    .Input("strides: int32")
    .Output("output: T")
    .Attr("T: realnumbertype = DT_FLOAT")
    .SetShapeFn(shape_inference::MaxPoolGradShape);
```

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Kernel registration example

```
template <class Device, class T>
class MaxPoolingGradOp : public OpKernel

REGISTER_KERNEL_BUILDER(Name("MaxPoolGradV2")
                            .Device(DEVICE_CPU)
                            .HostMemory("ksize")
                            .HostMemory("strides")
                            .TypeConstraint<float>("T"),
                        MaxPoolingGradOp<DCPU, float>);
```

Tensors and Variables

Tensor

Tensor

Represents a multidimensional array of elements

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Data structure consisting of:

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- Data structure consisting of:
  - Metadata (data type, shape), stored on host
  - Reference counted data buffer, stored on host or device
  - Reference count
- Underlaying data buffer can be shared between tensors
  - Different tensors can use different slices of buffer

Variables

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Resource variables

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TF2 implementation of Variables

Has strict guarantees on R/W order and value changes visibility

In practice, following is happening:

- More control edges are added to graph to ensure ordering
- Additional tensor copies are being done, to ensure changes won't leak
- Resource Manager locks concurrent accesses to variable tensor

Optimization passes

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Transformations of graph

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Various targets

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- Various targets
  - Pattern matching and fusing operators
  - Optimizing graph - removing dead nodes, reducing control flows, etc.
  - Reassigning betweeen devices
  - Device specific optimizations, e.g. MKL

Optimization pass phases

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Grappler

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PRE_PLACEMENT - after cost model assignment, before placement

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POST_PLACEMENT - after placement

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PRE_PLACEMENT - after cost model assignment, before placement

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POST_REWRITE_FOR_EXEC - after re-write using feed/fetch endpoints

POST_PARTITIONING - after partitioning

Each pass has priority in group

Registering custom optimization pass

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Runtime registry of optimization passess

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```
class LowerFunctionalOpsPass : public GraphOptimizationPass
```

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Status Run(**const** GraphOptimizationPassOptions& options) override

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REGISTER_OPTIMIZATION(OptimizationPassRegistry::PRE_PLACEMENT, 10, LowerFunctionalOpsPass)

TensorFlow devices

Device abstraction

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Has unique name

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Serves related host and device memory allocators

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Manager tensor creation and moving data between host and inside the device

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Manager tensor creation and moving data between host and inside the device

Executes kernel and ensures execution queues synchronization

Device types

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ThreadPoolDevice

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GpuDevice

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GpuDevice

PluggableDevice

Registering new device

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Implement device using one of 3 base interfaces

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Implement DeviceFactory for device discovery and instantiation

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Register factory in runtime registry

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Implement device using one of 3 base interfaces

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REGISTER_LOCAL_DEVICE_FACTORY("CPU", ThreadPoolDeviceFactory, 60)

TensorFlow allocators

Types of memory

Types of memory

Device memory

Types of memory

Device memory

Host memory

Types of memory

Device memory

Host memory

Caveat: CPU has both device and host memory

Selecting memory type

Selecting memory type

Using AllocatorAttributes structure on tensor allocation

Selecting memory type

Using AllocatorAttributes structure on tensor allocation

Set set_on_host(true) to select host memory

Selecting memory type

Using AllocatorAttributes structure on tensor allocation

Set set_on_host(true) to select host memory

Set set_gpu_compatible(true) to make host memory be pinned, for fast GPU DMAs

Allocator interface

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High level allocator

Allocator interface

High level allocator

Important methods:

```
void* AllocateRaw( size_t alignment, size_t num_bytes)
void* AllocateRaw( size_t alignment, size_t num_bytes, const
 AllocationAttributes & allocation_attr )
void DeallocateRaw(void* ptr)
```

BFC Allocator

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Implementing best-fit with coalescing algorithm

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Sensitive to small allocations - smallest bucket is quite large

SubAllocator interface

SubAllocator interface

Low level allocator

SubAllocator interface

Low level allocator

De-facto allocates buffers, e.g., calls malloc & free

Adding device allocator

Adding device allocator

By simply implementing dedicated Allocator and SubAllocator

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Simply served by GetAllocator method of device

Adding custom CPU allocator

Adding custom CPU allocator

Implementing dedicated Allocator and SubAllocator

Adding custom CPU allocator

Implementing dedicated Allocator and SubAllocator

Implementing AllocatorFactory

Adding custom CPU allocator

Implementing dedicated Allocator and SubAllocator

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Registering to runtime registry

REGISTER_MEM_ALLOCATOR("MklCPUAllocator", 200, MklCPUAllocatorFactory)

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Caveat: Custom CPU allocator has to be registered before any call to TF APIs that may allocate

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Registering to runtime registry

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Need to be aware of static initialization fiasco to correctly handle this

Caveat: Unexpected alloaction sources

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Example: Anytime user provides tensor created in numpy

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Usually memory buffers are from TF allocators defined for device

But! user can provide manually allocated buffers

Example: Anytime user provides tensor created in numpy

Cannot assume, that all buffers will come from given host allocator

Thanks for your attention!

Mateusz Nowak

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Feedback is appreciated ☺