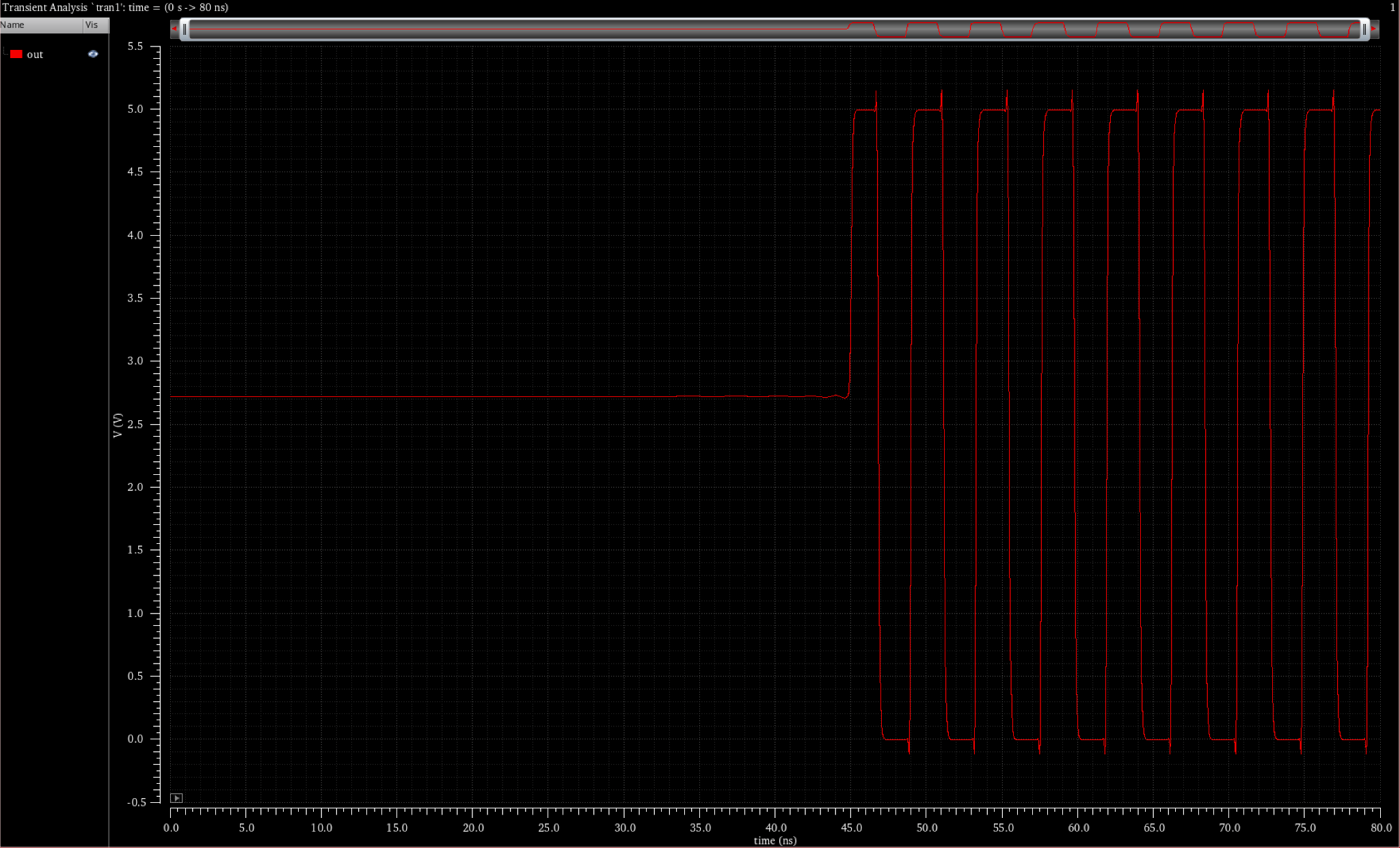
**CSE 30342 Lab 4 Group Submission**

Group Members: **Daniel Noronha, Ricky Ortiz, Nguyen Nguyen**

CRC Machine (Github Repo) Lab Folder: **dropbox/VLSI/boyz/lab4\_boyz**

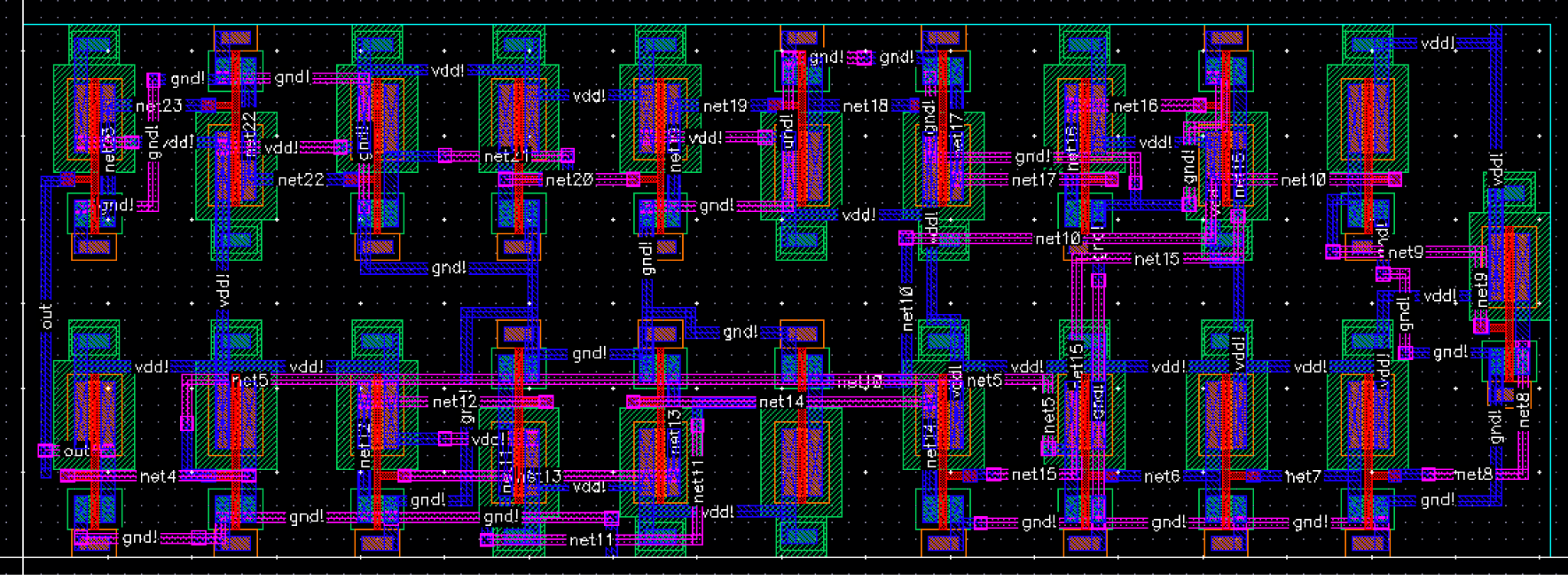
Date: 10/29/2024

**Part 1&2, Problem 1 - Ring Oscillator Waveform**

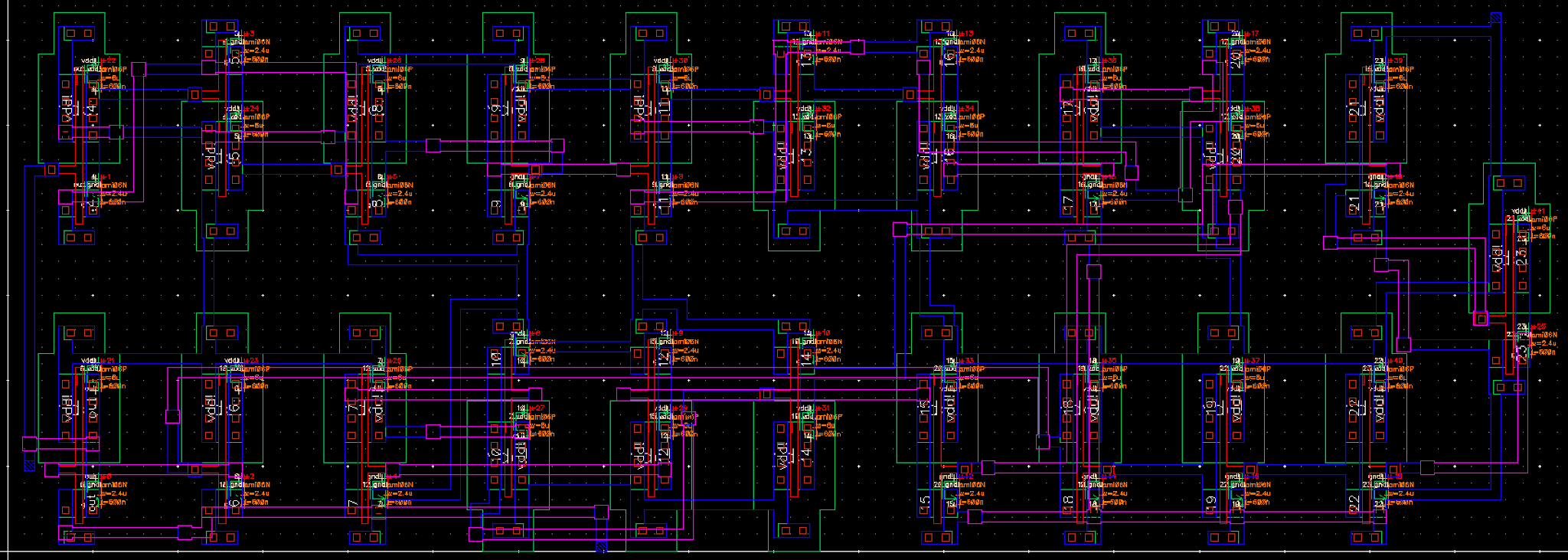


The initial delay is because it takes time for the ring oscillator to get an initial value at the output due to the propagation delay associated with each inverter. When the circuit is powered up initially, it takes some time for the signal to propagate through all 21 inverters and establish a stable oscillation with a fixed frequency and amplitude.

**Part 1&2, Problem 2 - Ring Oscillator Layout**

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**Part 1&2, Problem 2 - Ring Oscillator Extracted View**

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**Part 1&2, Problem 2 - Ring Oscillator Spectre si.inp Netlist File**

// Default Spectre Simulation run title card.

// Generated for: spectre

// Generated on: Oct 29 19:47:42 2024

// Design library name: lab4\_boyz\_dnoronha

// Design cell name: ring\_osc

// Design view name: schematic

simulator lang=spectre

global 0 vdd!

// Included Model Files

include "$CDK\_DIR/models/spectre/standalone/ami06P.m"

include "$CDK\_DIR/models/spectre/standalone/ami06N.m"

// Library name: lab4\_boyz\_dnoronha

// Cell name: NMOS\_IV\_3

// View name: schematic

subckt NMOS\_IV\_3 D G S

N0 (D G S 0) ami06N w=2.4u l=600n as=3.6e-12 ad=3.6e-12 ps=7.8u \

pd=7.8u m=1 region=sat

ends NMOS\_IV\_3

// End of subcircuit definition.

// Library name: lab4\_boyz\_dnoronha

// Cell name: PMOS\_IV\_3

// View name: schematic

subckt PMOS\_IV\_3 D G S

P0 (D G S vdd!) ami06P w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u pd=15.0u \

m=1 region=sat

ends PMOS\_IV\_3

// End of subcircuit definition.

// Library name: lab4\_boyz\_dnoronha

// Cell name: inv

// View name: schematic

subckt inv in out

I1 (out in 0) NMOS\_IV\_3

I0 (out in vdd!) PMOS\_IV\_3

ends inv

// End of subcircuit definition.

// Library name: lab4\_boyz\_dnoronha

// Cell name: ring\_osc

// View name: schematic

I23 (out net23) inv

I24 (net23 net22) inv

I25 (net22 net21) inv

I26 (net21 net20) inv

I27 (net20 net19) inv

I28 (net19 net18) inv

I29 (net18 net17) inv

I30 (net17 net16) inv

I31 (net16 net15) inv

I32 (net15 net14) inv

I33 (net14 net13) inv

I34 (net13 net12) inv

I35 (net12 net11) inv

I36 (net11 net10) inv

I37 (net10 net9) inv

I38 (net9 net8) inv

I39 (net8 net7) inv

I40 (net7 net6) inv

I41 (net6 net5) inv

I42 (net5 net4) inv

I43 (net4 out) inv

V0 (vdd! 0) vsource type=dc dc=5

// Spectre Source Statements

// Spectre Analyses and Output Options Statements

// Output Options

simOptions options

//+ reltol = 1.00000000E-03

//+ vabstol = 1.00000000E-06

//+ iabstol = 1.00000000E-12

//+ temp = 27

//+ save = allpub

//+ currents = selected

// Analyses

// dc1 dc oppoint=logfile homotopy=all

tran1 tran start=0 stop=80n step=0.1n errpreset=moderate

// End of Netlist

**Part 1&2, Problem 2 - Ring Oscillator LVS Netlist File\***

t 18 out output

n 1 vdd!

n 0 gnd!

n 2 /net20

n 3 /net10

n 4 /net7

n 5 /net11

n 6 /net13

n 7 /net5

n 8 /net14

n 9 /net19

n 10 /net17

n 11 /net18

n 12 /net8

n 13 /net6

n 14 /net22

n 15 /net4

n 16 /net15

n 18 /out

n 19 /net16

n 20 /net9

n 21 /net12

n 22 /net21

n 24 /net23

; nmos4 Instance /I23/I1/N0 = auLvs device Q0

d nmos D G S B (p D S)

i 0 nmos 24 18 0 0 " m 1 l 600e-9 w 2.4e-6 "

; pmos4 Instance /I23/I0/P0 = auLvs device Q1

d pmos D G S B (p D S)

i 1 pmos 24 18 1 1 " m 1 l 600e-9 w 6e-6 "

; nmos4 Instance /I24/I1/N0 = auLvs device Q2

i 2 nmos 14 24 0 0 " m 1 l 600e-9 w 2.4e-6 "

; pmos4 Instance /I24/I0/P0 = auLvs device Q3

i 3 pmos 14 24 1 1 " m 1 l 600e-9 w 6e-6 "

; nmos4 Instance /I25/I1/N0 = auLvs device Q4

i 4 nmos 22 14 0 0 " m 1 l 600e-9 w 2.4e-6 "

; pmos4 Instance /I25/I0/P0 = auLvs device Q5

i 5 pmos 22 14 1 1 " m 1 l 600e-9 w 6e-6 "

; nmos4 Instance /I26/I1/N0 = auLvs device Q6

i 6 nmos 2 22 0 0 " m 1 l 600e-9 w 2.4e-6 "

; pmos4 Instance /I26/I0/P0 = auLvs device Q7

i 7 pmos 2 22 1 1 " m 1 l 600e-9 w 6e-6 "

; nmos4 Instance /I27/I1/N0 = auLvs device Q8

i 8 nmos 9 2 0 0 " m 1 l 600e-9 w 2.4e-6 "

; pmos4 Instance /I27/I0/P0 = auLvs device Q9

i 9 pmos 9 2 1 1 " m 1 l 600e-9 w 6e-6 "

; nmos4 Instance /I28/I1/N0 = auLvs device Q10

i 10 nmos 11 9 0 0 " m 1 l 600e-9 w 2.4e-6 "

; pmos4 Instance /I28/I0/P0 = auLvs device Q11

i 11 pmos 11 9 1 1 " m 1 l 600e-9 w 6e-6 "

; nmos4 Instance /I29/I1/N0 = auLvs device Q12

i 12 nmos 10 11 0 0 " m 1 l 600e-9 w 2.4e-6 "

; pmos4 Instance /I29/I0/P0 = auLvs device Q13

i 13 pmos 10 11 1 1 " m 1 l 600e-9 w 6e-6 "

; nmos4 Instance /I30/I1/N0 = auLvs device Q14

i 14 nmos 19 10 0 0 " m 1 l 600e-9 w 2.4e-6 "

; pmos4 Instance /I30/I0/P0 = auLvs device Q15

i 15 pmos 19 10 1 1 " m 1 l 600e-9 w 6e-6 "

; nmos4 Instance /I31/I1/N0 = auLvs device Q16

i 16 nmos 16 19 0 0 " m 1 l 600e-9 w 2.4e-6 "

; pmos4 Instance /I31/I0/P0 = auLvs device Q17

i 17 pmos 16 19 1 1 " m 1 l 600e-9 w 6e-6 "

; nmos4 Instance /I32/I1/N0 = auLvs device Q18

i 18 nmos 8 16 0 0 " m 1 l 600e-9 w 2.4e-6 "

; pmos4 Instance /I32/I0/P0 = auLvs device Q19

i 19 pmos 8 16 1 1 " m 1 l 600e-9 w 6e-6 "

; nmos4 Instance /I33/I1/N0 = auLvs device Q20

i 20 nmos 6 8 0 0 " m 1 l 600e-9 w 2.4e-6 "

; pmos4 Instance /I33/I0/P0 = auLvs device Q21

i 21 pmos 6 8 1 1 " m 1 l 600e-9 w 6e-6 "

; nmos4 Instance /I34/I1/N0 = auLvs device Q22

i 22 nmos 21 6 0 0 " m 1 l 600e-9 w 2.4e-6 "

; pmos4 Instance /I34/I0/P0 = auLvs device Q23

i 23 pmos 21 6 1 1 " m 1 l 600e-9 w 6e-6 "

; nmos4 Instance /I35/I1/N0 = auLvs device Q24

i 24 nmos 5 21 0 0 " m 1 l 600e-9 w 2.4e-6 "

; pmos4 Instance /I35/I0/P0 = auLvs device Q25

i 25 pmos 5 21 1 1 " m 1 l 600e-9 w 6e-6 "

; nmos4 Instance /I36/I1/N0 = auLvs device Q26

i 26 nmos 3 5 0 0 " m 1 l 600e-9 w 2.4e-6 "

; pmos4 Instance /I36/I0/P0 = auLvs device Q27

i 27 pmos 3 5 1 1 " m 1 l 600e-9 w 6e-6 "

; nmos4 Instance /I37/I1/N0 = auLvs device Q28

i 28 nmos 20 3 0 0 " m 1 l 600e-9 w 2.4e-6 "

; pmos4 Instance /I37/I0/P0 = auLvs device Q29

i 29 pmos 20 3 1 1 " m 1 l 600e-9 w 6e-6 "

; nmos4 Instance /I38/I1/N0 = auLvs device Q30

i 30 nmos 12 20 0 0 " m 1 l 600e-9 w 2.4e-6 "

; pmos4 Instance /I38/I0/P0 = auLvs device Q31

i 31 pmos 12 20 1 1 " m 1 l 600e-9 w 6e-6 "

; nmos4 Instance /I39/I1/N0 = auLvs device Q32

i 32 nmos 4 12 0 0 " m 1 l 600e-9 w 2.4e-6 "

; pmos4 Instance /I39/I0/P0 = auLvs device Q33

i 33 pmos 4 12 1 1 " m 1 l 600e-9 w 6e-6 "

; nmos4 Instance /I40/I1/N0 = auLvs device Q34

i 34 nmos 13 4 0 0 " m 1 l 600e-9 w 2.4e-6 "

; pmos4 Instance /I40/I0/P0 = auLvs device Q35

i 35 pmos 13 4 1 1 " m 1 l 600e-9 w 6e-6 "

; nmos4 Instance /I41/I1/N0 = auLvs device Q36

i 36 nmos 7 13 0 0 " m 1 l 600e-9 w 2.4e-6 "

; pmos4 Instance /I41/I0/P0 = auLvs device Q37

i 37 pmos 7 13 1 1 " m 1 l 600e-9 w 6e-6 "

; nmos4 Instance /I42/I1/N0 = auLvs device Q38

i 38 nmos 15 7 0 0 " m 1 l 600e-9 w 2.4e-6 "

; pmos4 Instance /I42/I0/P0 = auLvs device Q39

i 39 pmos 15 7 1 1 " m 1 l 600e-9 w 6e-6 "

; nmos4 Instance /I43/I1/N0 = auLvs device Q40

i 40 nmos 18 15 0 0 " m 1 l 600e-9 w 2.4e-6 "

; pmos4 Instance /I43/I0/P0 = auLvs device Q41

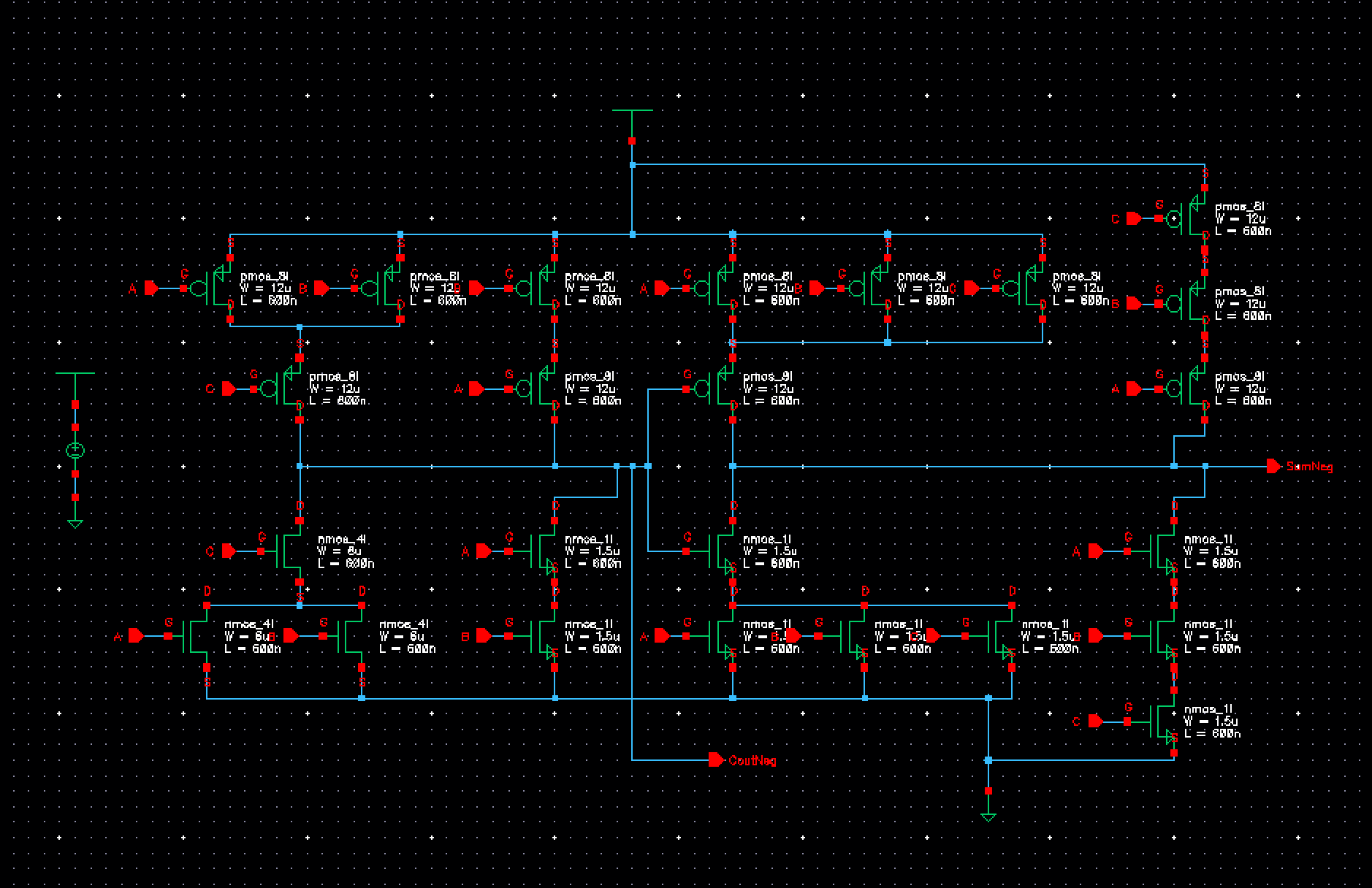
i 41 pmos 18 15 1 1 " m 1 l 600e-9 w 6e-6 "

t 0 gnd! global

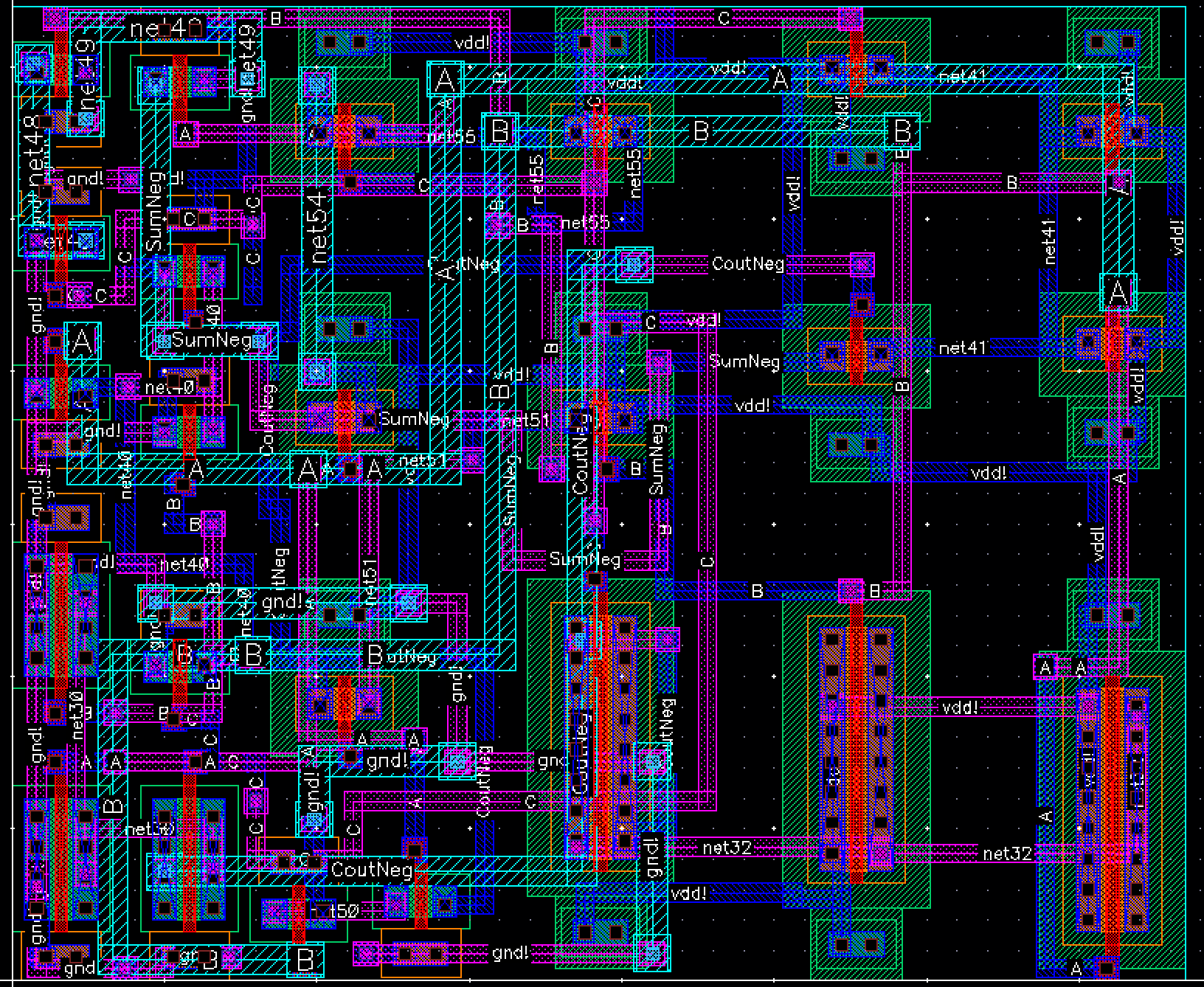
t 1 vdd! global

**\*Both LVS and Spectre (si.inp) netlist files were included because directions were not specific (asked for si.inp from LVS.ring\_osc folder but si.inp only exists in Spectre run directory).**

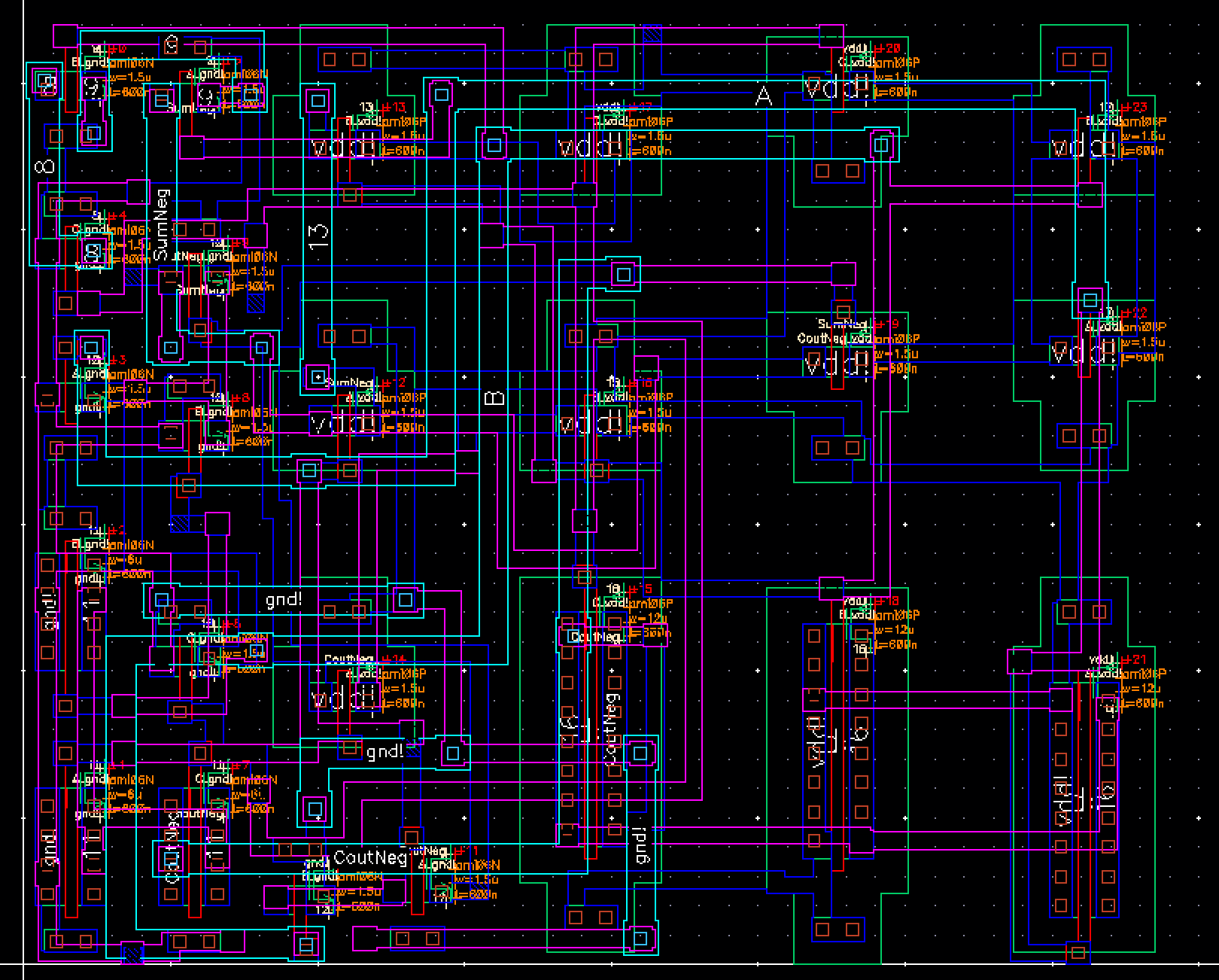
**Part 3, Problem 3 - Schematic**

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**Part 3, Problem 3 - Layout**

****

**Part 3, Problem 3 - Extracted View**

****

**Part 3, Problem 3 - Mirror Full Adder LVS Netlist File**

i 13 nmos 11 18 6 0 " m 1 l 600e-9 w 1.5e-6 "

; nmos4 Instance /I18/N0 = auLvs device Q14

i 14 nmos 4 2 11 0 " m 1 l 600e-9 w 1.5e-6 "

; nmos4 Instance /I17/N0 = auLvs device Q15

i 15 nmos 15 3 0 0 " m 1 l 600e-9 w 1.5e-6 "

; nmos4 Instance /I16/N0 = auLvs device Q16

i 16 nmos 15 18 0 0 " m 1 l 600e-9 w 1.5e-6 "

; nmos4 Instance /I15/N0 = auLvs device Q17

i 17 nmos 15 2 0 0 " m 1 l 600e-9 w 1.5e-6 "

; nmos4 Instance /I14/N0 = auLvs device Q18

i 18 nmos 14 18 0 0 " m 1 l 600e-9 w 1.5e-6 "

; nmos4 Instance /I13/N0 = auLvs device Q19

i 19 nmos 4 5 15 0 " m 1 l 600e-9 w 1.5e-6 "

; nmos4 Instance /I12/N0 = auLvs device Q20

i 20 nmos 5 2 14 0 " m 1 l 600e-9 w 1.5e-6 "

; nmos4 Instance /I23/N0 = auLvs device Q21

i 21 nmos 9 2 0 0 " m 1 l 600e-9 w 6e-6 "

; nmos4 Instance /I22/N0 = auLvs device Q22

i 22 nmos 9 18 0 0 " m 1 l 600e-9 w 6e-6 "

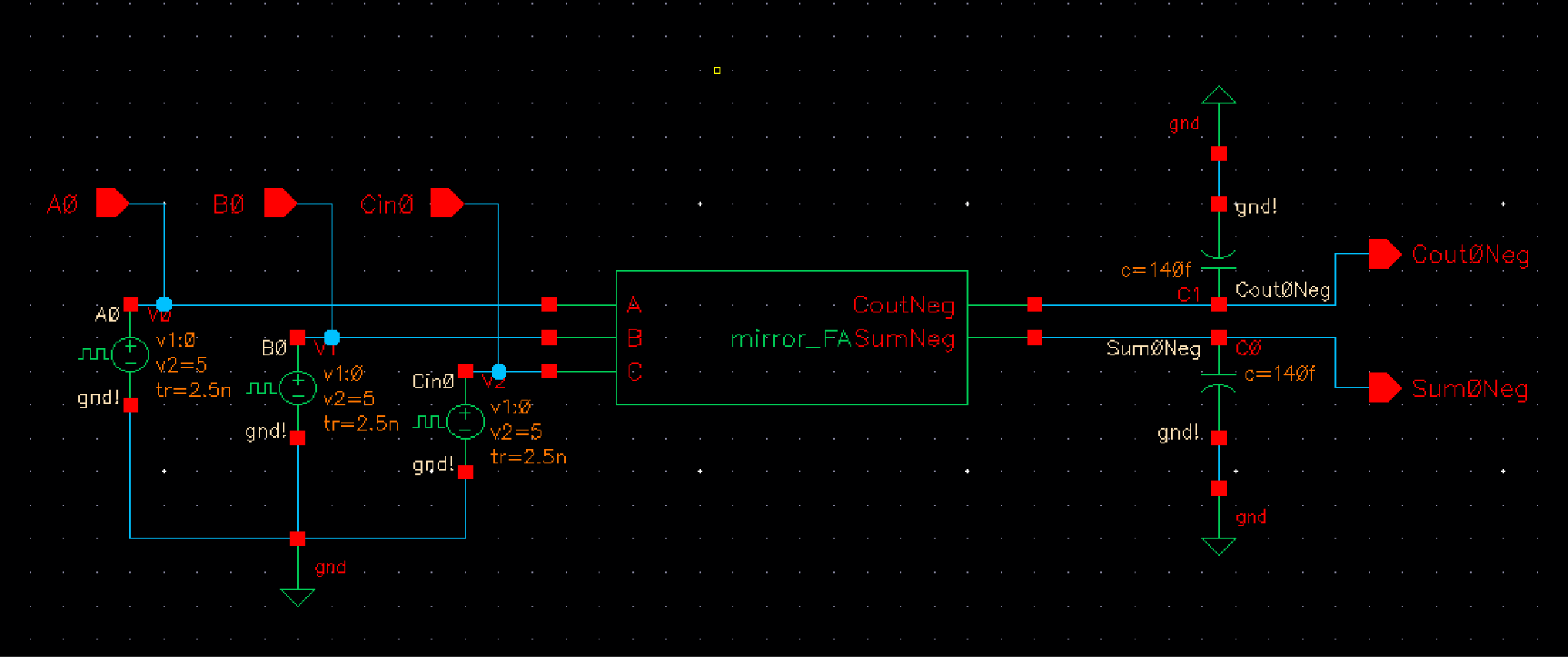
; nmos4 Instance /I21/N0 = auLvs device Q23

i 23 nmos 5 3 9 0 " m 1 l 600e-9 w 6e-6 "

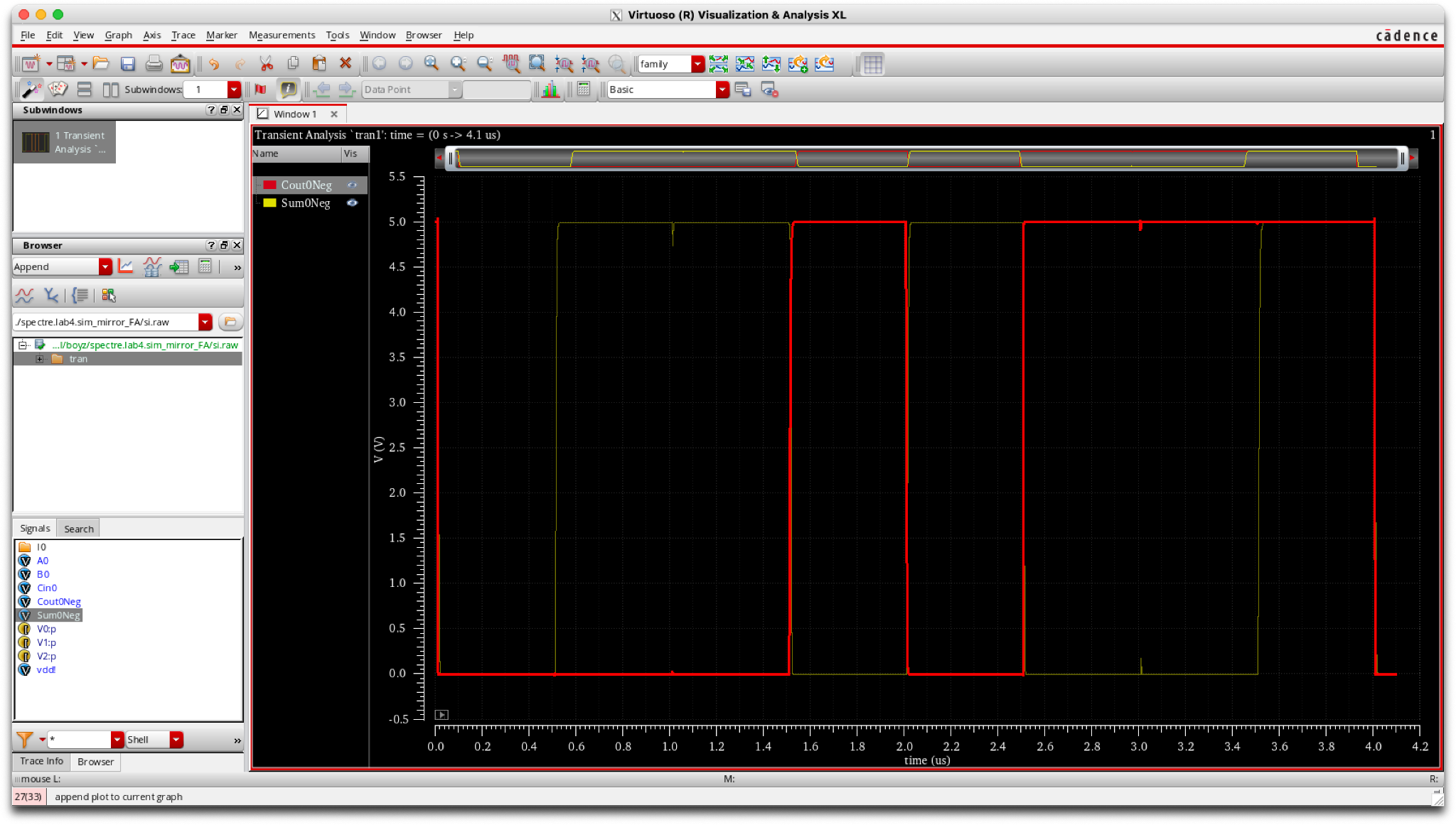
t 0 gnd! global

t 1 vdd! global

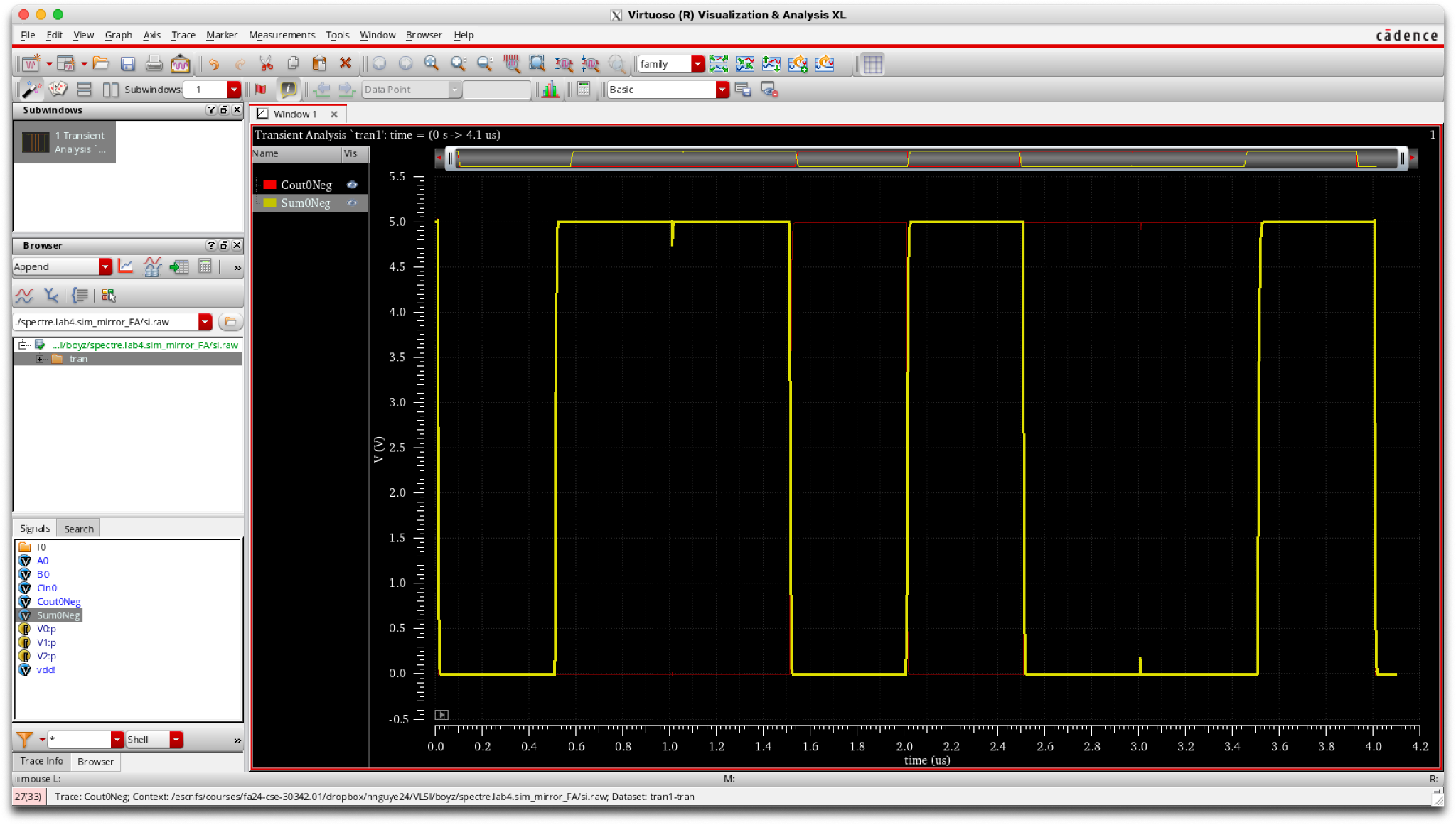
**Part 3, Problem 4 - Mirror Full Adder Spectre Schematic**

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**Part 3, Problem 4 - Mirror Full Adder Spectre Waveform (Cout0Neg)**

****

**Part 3, Problem 4 - Mirror Full Adder Spectre Waveform (Sum0Neg)**

****

**Part 3, Problem 4 - Mirror Full Adder Spectre si.inp Netlist File**

// Default Spectre Simulation run title card.

// Generated for: spectre

// Generated on: Oct 29 23:46:35 2024

// Design library name: lab4\_boyz\_nnguye24

// Design cell name: sim\_mirror\_FA

// Design view name: schematic

simulator lang=spectre

global 0 vdd!

// Included Model Files

include "$CDK\_DIR/models/spectre/standalone/ami06P.m"

include "$CDK\_DIR/models/spectre/standalone/ami06N.m"

// Library name: lab4\_boyz\_nnguye24

// Cell name: pmos\_8l

// View name: schematic

subckt pmos\_8l D G S

P0 (D G S vdd!) ami06P w=12.0u l=600n as=1.8e-11 ad=1.8e-11 ps=27.0u \

pd=27.0u m=1 region=sat

ends pmos\_8l

// End of subcircuit definition.

// Library name: lab4\_boyz\_nnguye24

// Cell name: pmos\_1l

// View name: schematic

subckt pmos\_1l D G S

P0 (D G S vdd!) ami06P w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u \

pd=6u m=1 region=sat

ends pmos\_1l

// End of subcircuit definition.

// Library name: lab4\_boyz\_nnguye24

// Cell name: nmos\_1l

// View name: schematic

subckt nmos\_1l D G S

N0 (D G S 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u pd=6u \

m=1 region=sat

ends nmos\_1l

// End of subcircuit definition.

// Library name: lab4\_boyz\_nnguye24

// Cell name: nmos\_4l

// View name: schematic

subckt nmos\_4l D G S

N0 (D G S 0) ami06N w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u pd=15.0u \

m=1 region=sat

ends nmos\_4l

// End of subcircuit definition.

// Library name: lab4\_boyz\_nnguye24

// Cell name: mirror\_FA

// View name: schematic

subckt mirror\_FA A B C CoutNeg SumNeg

I2 (CoutNeg C net32) pmos\_8l

I1 (net32 B vdd!) pmos\_8l

I0 (net32 A vdd!) pmos\_8l

I11 (SumNeg A net54) pmos\_1l

I10 (net54 B net55) pmos\_1l

I9 (net55 C vdd!) pmos\_1l

I8 (net41 C vdd!) pmos\_1l

I7 (net41 B vdd!) pmos\_1l

I6 (SumNeg CoutNeg net41) pmos\_1l

I5 (net41 A vdd!) pmos\_1l

I4 (CoutNeg A net51) pmos\_1l

I3 (net51 B vdd!) pmos\_1l

I20 (net48 C 0) nmos\_1l

I19 (net49 B net48) nmos\_1l

I18 (SumNeg A net49) nmos\_1l

I17 (net40 C 0) nmos\_1l

I16 (net40 B 0) nmos\_1l

I15 (net40 A 0) nmos\_1l

I14 (net50 B 0) nmos\_1l

I13 (SumNeg CoutNeg net40) nmos\_1l

I12 (CoutNeg A net50) nmos\_1l

I23 (net30 A 0) nmos\_4l

I22 (net30 B 0) nmos\_4l

I21 (CoutNeg C net30) nmos\_4l

V0 (vdd! 0) vsource type=dc dc=5

ends mirror\_FA

// End of subcircuit definition.

// Library name: lab4\_boyz\_nnguye24

// Cell name: sim\_mirror\_FA

// View name: schematic

I0 (A0 B0 Cin0 Cout0Neg Sum0Neg) mirror\_FA

V2 (Cin0 0) vsource type=pulse val0=0 val1=5 period=4u delay=10n rise=2.5n \

fall=2.5n width=1.9975u

V1 (B0 0) vsource type=pulse val0=0 val1=5 period=2u delay=10n rise=2.5n \

fall=2.5n width=997.5n

V0 (A0 0) vsource type=pulse val0=0 val1=5 period=1u delay=10n rise=2.5n \

fall=2.5n width=497.5n

C1 (Cout0Neg 0) capacitor c=140f m=1

C0 (Sum0Neg 0) capacitor c=140f m=1

// Spectre Source Statements

// Spectre Analyses and Output Options Statements

// Output Options

simOptions options

//+ reltol = 1.00000000E-03

//+ vabstol = 1.00000000E-06

//+ iabstol = 1.00000000E-12

//+ temp = 27

//+ save = allpub

//+ currents = selected

// Analyses

// dc1 dc oppoint=logfile homotopy=all

tran1 tran start=0 stop=4.1u step=0.1n errpreset=moderate

// End of Netlist