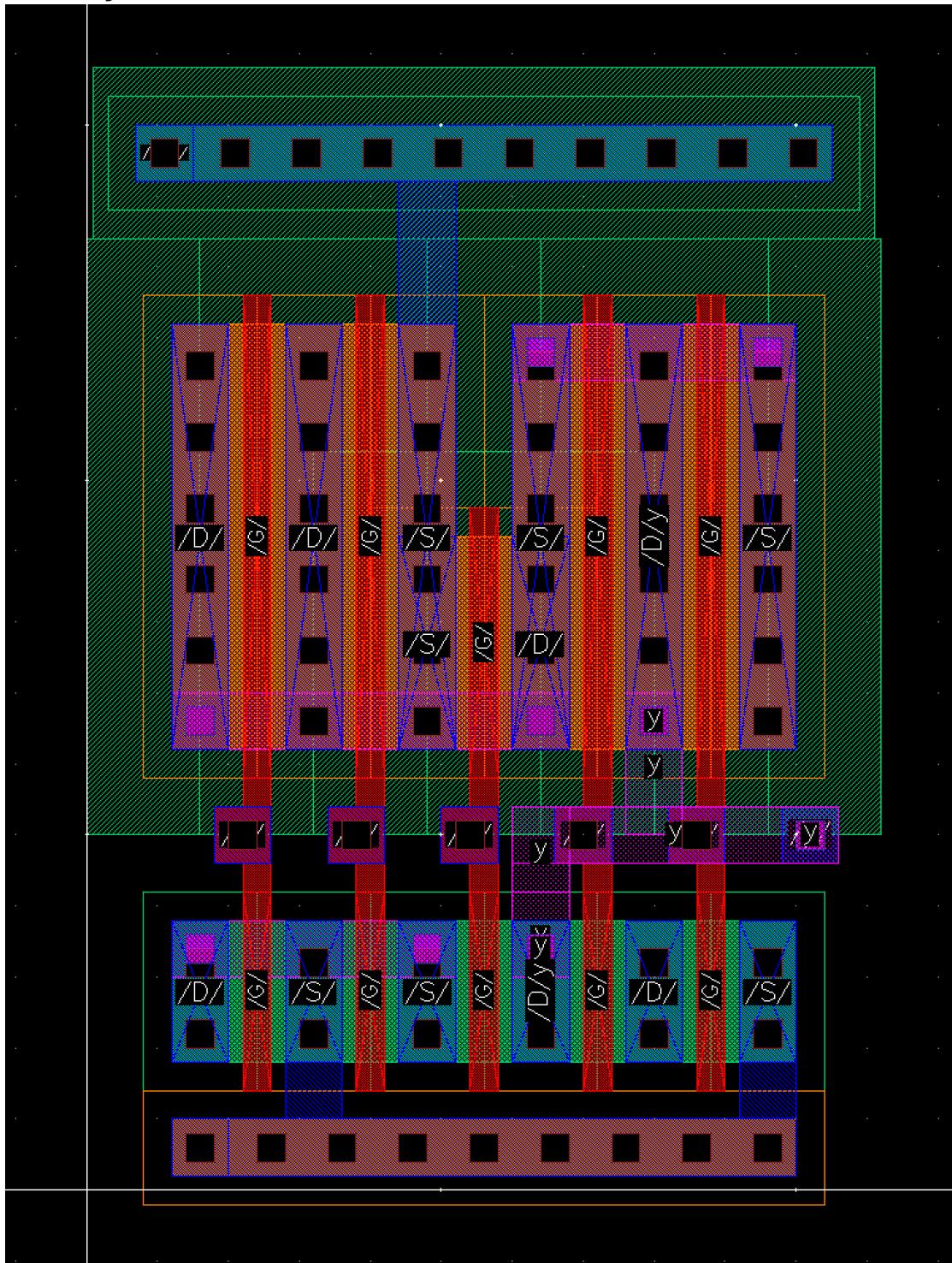


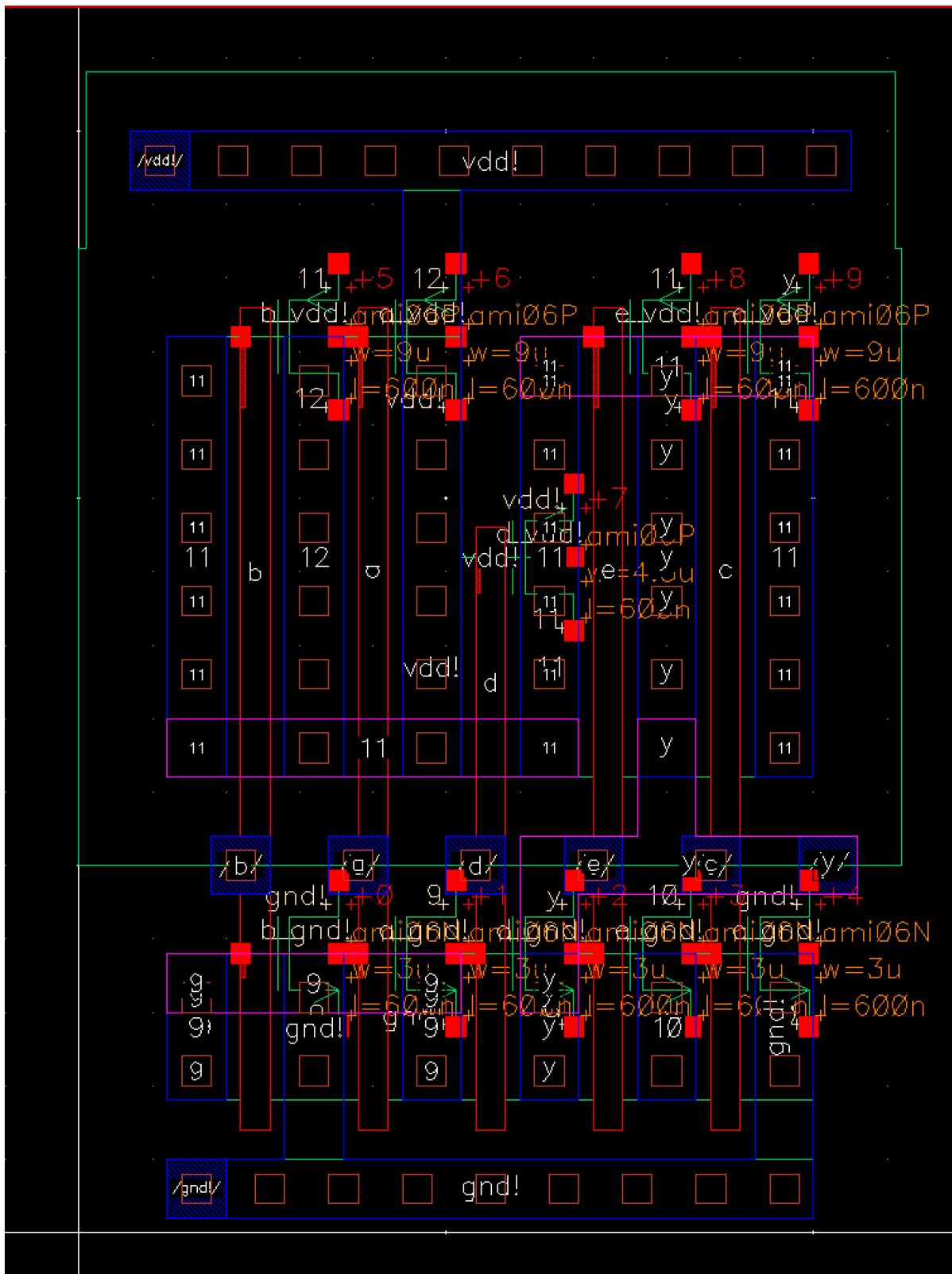
CSE 30342 Lab 3 Group Submission

Group Members: **Daniel Noronha, Ricky Ortiz, Nguyen Nguyen**
CRC Machine (Github Repo) Lab Folder: **dropbox/VLSI/boyz/lab3_boyz**
Date: Thursday, 17 October 2024

Part 1c - Layout



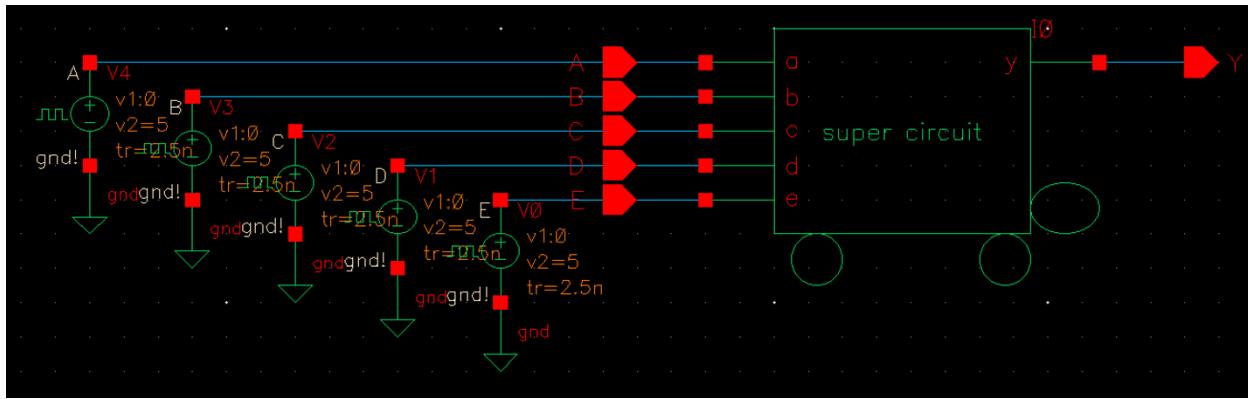
Part 1d – Extracted View



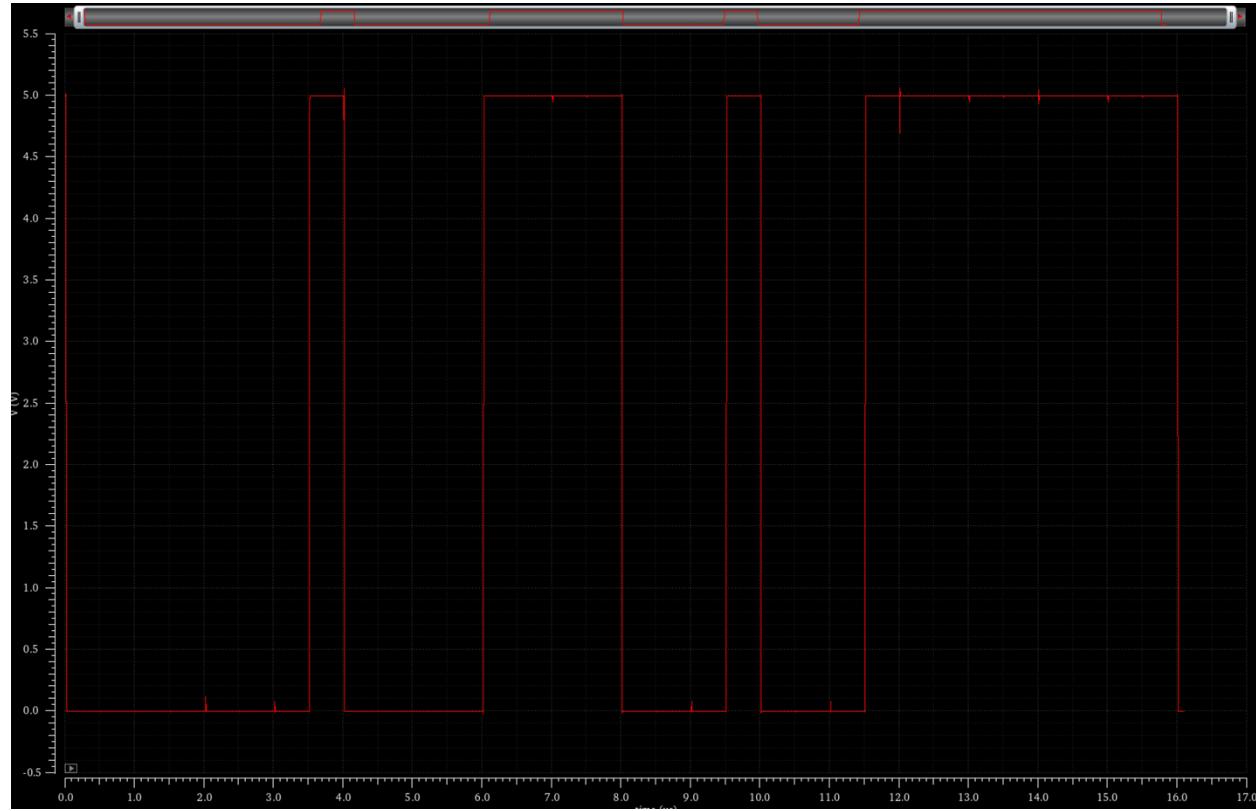
Part 1d – Netlist

```
t9 a input
t8 b input
t7 c input
t6 d input
t4 e input
t5 gnd! inputOutput
t10 vdd! inputOutput
t11 y output
n0/12
n1/11
n2/10
n3/9
n4/e
n5/gnd!
n6/d
n7/c
n8/b
n9/a
n10/vdd!
n11/y
; pmos4 Instance /+9 = auLvs device Q0
d pmos D G S B (p D S)
i0 pmos 1 7 11 10 " m 1 l 600e-9 w 9e-6 "
; pmos4 Instance /+8 = auLvs device Q1
i1 pmos 11 4 1 10 " m 1 l 600e-9 w 9e-6 "
; pmos4 Instance /+6 = auLvs device Q2
i2 pmos 10 9 0 10 " m 1 l 600e-9 w 9e-6 "
; pmos4 Instance /+5 = auLvs device Q3
i3 pmos 0 8 1 10 " m 1 l 600e-9 w 9e-6 "
; nmos4 Instance /+4 = auLvs device Q4
d nmos D G S B (p D S)
i4 nmos 5 7 2 5 " m 1 l 600e-9 w 3e-6 "
; nmos4 Instance /+3 = auLvs device Q5
i5 nmos 2 4 11 5 " m 1 l 600e-9 w 3e-6 "
; nmos4 Instance /+2 = auLvs device Q6
i6 nmos 11 6 3 5 " m 1 l 600e-9 w 3e-6 "
; nmos4 Instance /+1 = auLvs device Q7
i7 nmos 3 9 5 5 " m 1 l 600e-9 w 3e-6 "
; nmos4 Instance /+0 = auLvs device Q8
i8 nmos 5 8 3 5 " m 1 l 600e-9 w 3e-6 "
; pmos4 Instance /+7 = auLvs device Q9
i9 pmos 1 6 10 10 " m 1 l 600e-9 w 4.5e-6 "
```

Part 1e – Schematic



Part 1e – Waveform



Part 1e - Power Spike Mitigation Explanation

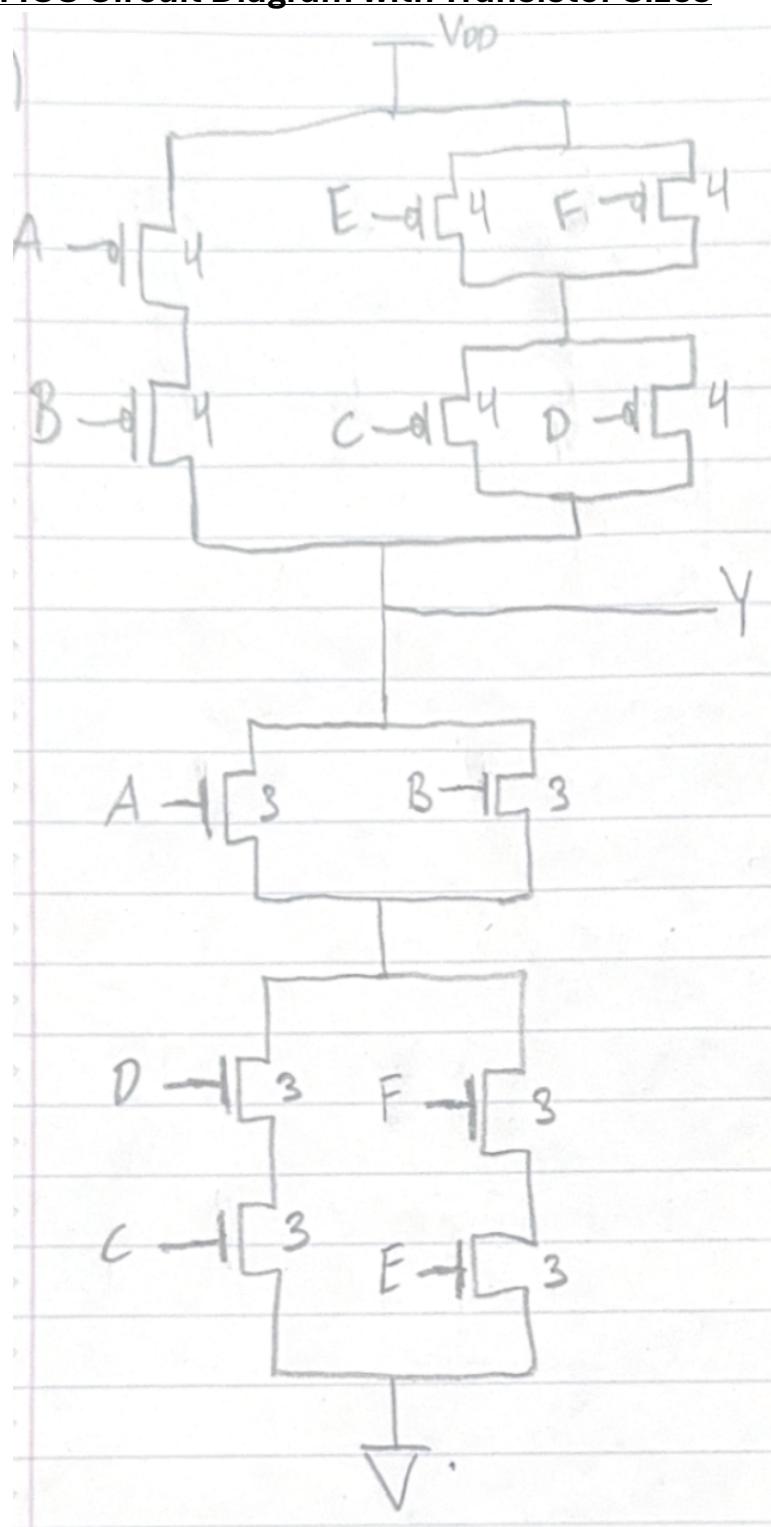
The updated delays reduced the spikes significantly. The new delay values were chosen to ensure that the pull-up network switches off in order. For example, the B pulse delay is 2.5n greater than that of A (in series) to allow the transistor with input A to switch off first. The spikes generally result when multiple transistors switch at (what should be) a fixed logic level, so using delays helps reduce the overlap in waveforms, mitigating the spikes.

Part 1e – Netlist

```
// Library name: lab3_boyz_dnoronha
// Cell name: adv_logic
// View name: schematic
subckt adv_logic a b c d e y
    P4 (y e net21 vdd!) ami06P w=9u l=600n as=1.35e-11 ad=1.35e-11 \
        ps=21.0u pd=21.0u m=1 region=sat
    P3 (net21 d vdd! vdd!) ami06P w=4.5u l=600n as=6.75e-12 ad=6.75e-12 \
        ps=12.0u pd=12.0u m=1 region=sat
    P2 (y c net21 vdd!) ami06P w=9u l=600n as=1.35e-11 ad=1.35e-11 \
        ps=21.0u pd=21.0u m=1 region=sat
    P1 (net21 b net32 vdd!) ami06P w=9u l=600n as=1.35e-11 ad=1.35e-11 \
        ps=21.0u pd=21.0u m=1 region=sat
    P0 (net32 a vdd! vdd!) ami06P w=9u l=600n as=1.35e-11 ad=1.35e-11 \
        ps=21.0u pd=21.0u m=1 region=sat
    V1 (0 0) vsource type=dc dc=0
    V0 (vdd! 0) vsource type=dc dc=5
    N4 (net30 c 0 0) ami06N w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u pd=9u \
        m=1 region=sat
    N3 (y e net30 0) ami06N w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u pd=9u \
        m=1 region=sat
    N2 (net19 b 0 0) ami06N w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u pd=9u \
        m=1 region=sat
    N1 (net19 a 0 0) ami06N w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u pd=9u \
        m=1 region=sat
    N0 (y d net19 0) ami06N w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u pd=9u \
        m=1 region=sat
ends adv_logic
// End of subcircuit definition.
```

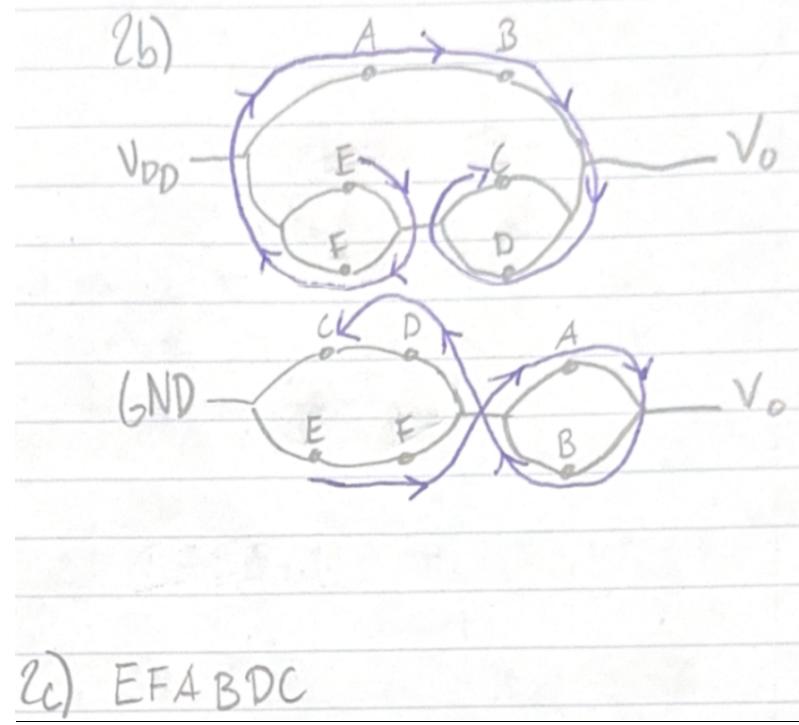
```
// Library name: lab3_boyz_dnoronha
// Cell name: sim_adv_circuit
// View name: schematic
I0 (A B C D E Y) adv_logic
V4 (A 0) vsource type=pulse val0=0 val1=5 period=1u delay=10n rise=2.5n \
    fall=2.5n width=497.5n
V3 (B 0) vsource type=pulse val0=0 val1=5 period=2u delay=12.5n rise=2.5n \
    fall=2.5n width=997.5n
V2 (C 0) vsource type=pulse val0=0 val1=5 period=4u delay=15n rise=2.5n \
    fall=2.5n width=1.9975u
V1 (D 0) vsource type=pulse val0=0 val1=5 period=8u delay=10n rise=2.5n \
    fall=2.5n width=3.9975u
V0 (E 0) vsource type=pulse val0=0 val1=5 period=16u delay=15n rise=2.5n \
    fall=2.5n width=7.9975u
```

Part 2a/2e - CMOS Circuit Diagram with Transistor Sizes

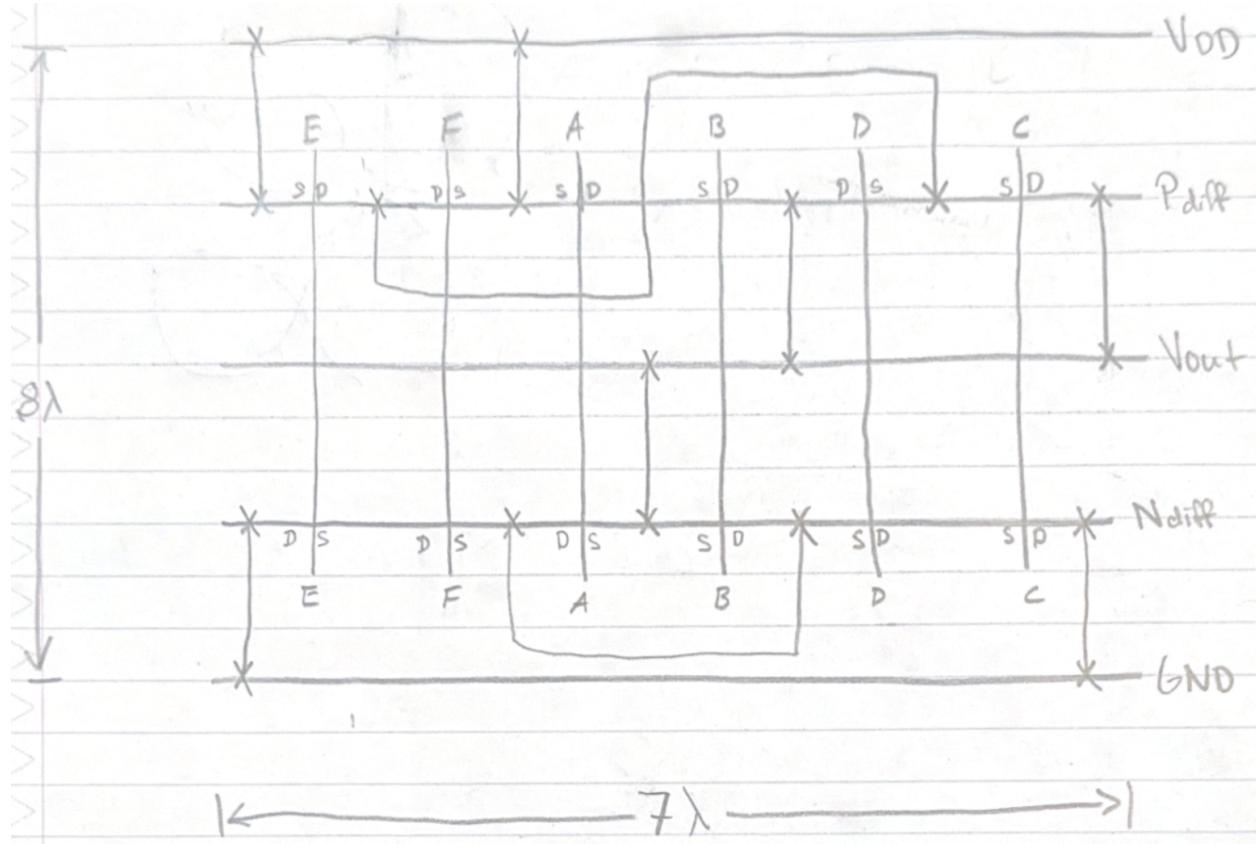


Note: Transistor size number written beside transistor. It was multiplied by $1.5\mu\text{m}$ to get physical transistor width (W) in the layout.

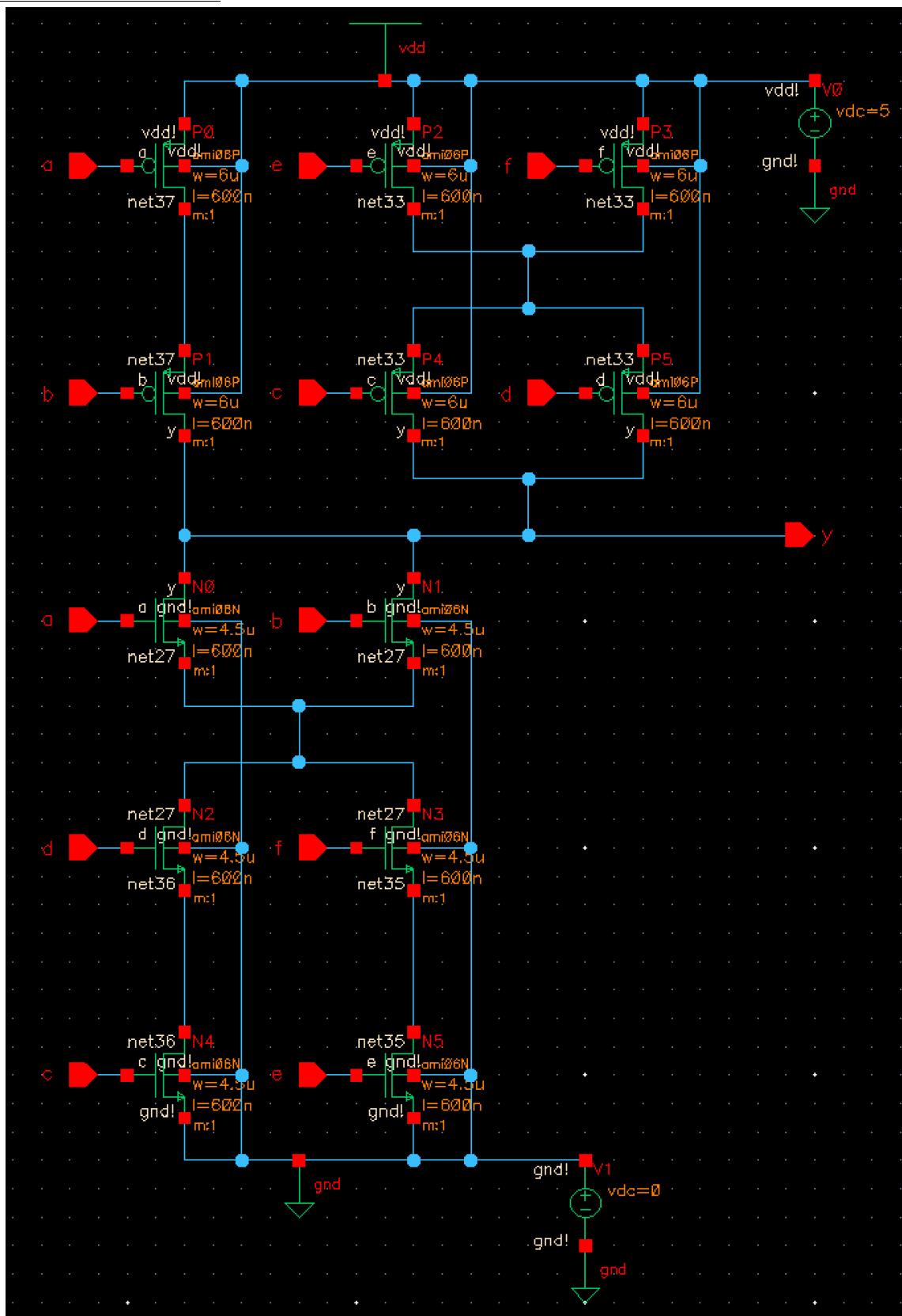
Part 2b/2c - Path Diagrams & Euler Path



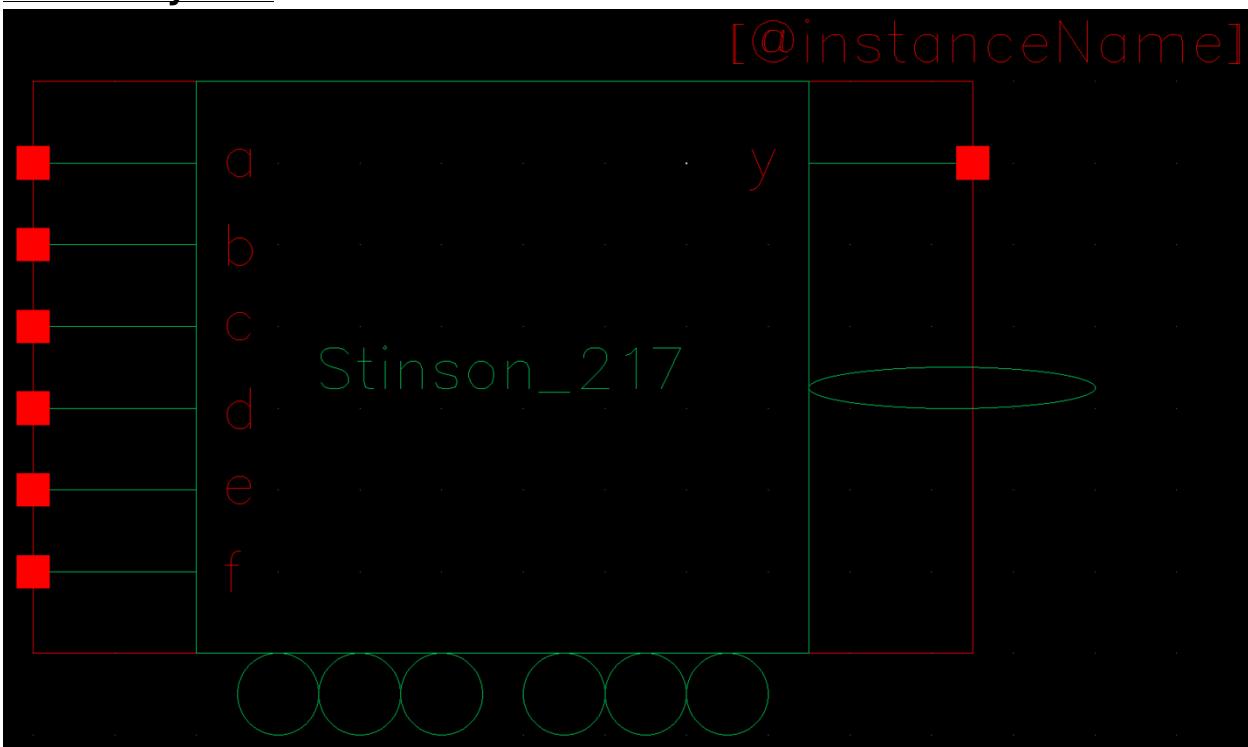
Part 2d - CMOS Layout Stick Diagram



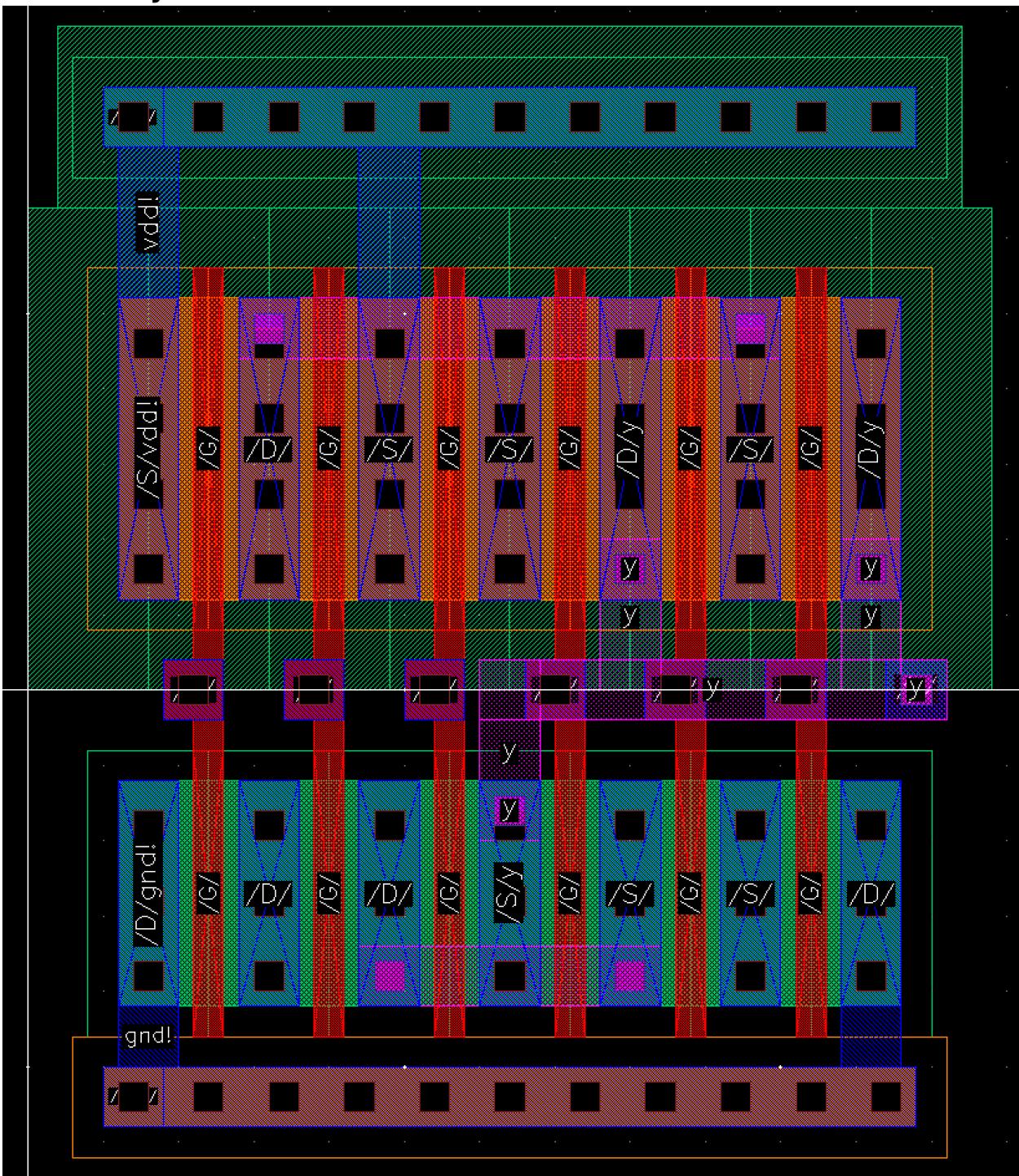
Part 2f – Schematic



Part 2f – Symbol



Part 2f – Layout

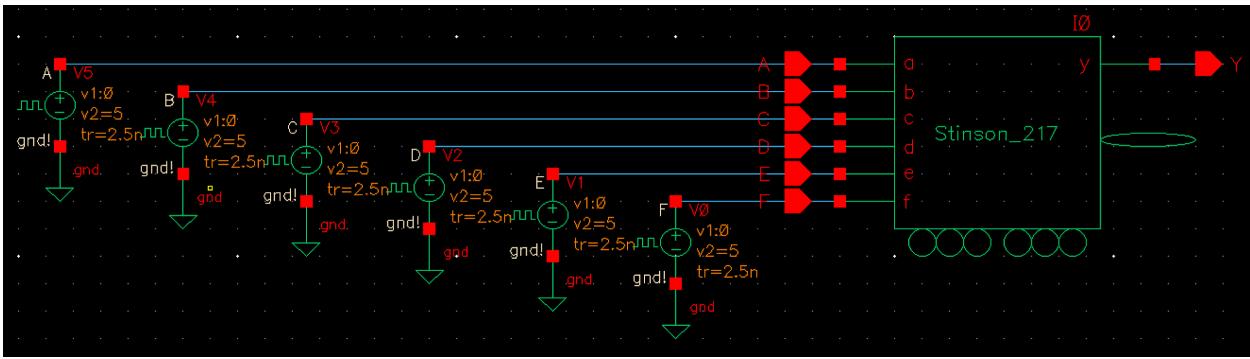


Part 2f – LVS Netlist

```
t 11 a input
t 10 b input
t 9 c input
t 8 d input
t 6 e input
t 5 f input
t 7 gnd! inputOutput
t 12 vdd! inputOutput
t 13 y output
n 0/14
n 1/13
n 2/12
n 3/11
n 4/10
n 5/f
n 6/e
n 7/gnd!
n 8/d
n 9/c
n 10/b
n 11/a
n 12/vdd!
n 13/y
; pmos4 Instance /+11 = auLvs device Q0
d pmos D G S B (p D S)
i 0 pmos 13 9 1 12 " m 1 l 600e-9 w 6e-6 "
; pmos4 Instance /+10 = auLvs device Q1
i 1 pmos 1 8 13 12 " m 1 l 600e-9 w 6e-6 "
; pmos4 Instance /+9 = auLvs device Q2
i 2 pmos 13 10 0 12 " m 1 l 600e-9 w 6e-6 "
; pmos4 Instance /+8 = auLvs device Q3
i 3 pmos 0 11 12 12 " m 1 l 600e-9 w 6e-6 "
; pmos4 Instance /+7 = auLvs device Q4
i 4 pmos 12 5 1 12 " m 1 l 600e-9 w 6e-6 "
; pmos4 Instance /+6 = auLvs device Q5
i 5 pmos 1 6 12 12 " m 1 l 600e-9 w 6e-6 "
; nmos4 Instance /+5 = auLvs device Q6
d nmos D G S B (p D S)
i 6 nmos 7 9 2 7 " m 1 l 600e-9 w 4.5e-6 "
; nmos4 Instance /+4 = auLvs device Q7
i 7 nmos 2 8 3 7 " m 1 l 600e-9 w 4.5e-6 "
; nmos4 Instance /+3 = auLvs device Q8
i 8 nmos 3 10 13 7 " m 1 l 600e-9 w 4.5e-6 "
```

```
; nmos4 Instance /+2 = auLvs device Q9
i9 nmos 13 11 3 7 " m 1 l 600e-9 w 4.5e-6 "
; nmos4 Instance /+1 = auLvs device Q10
i10 nmos 3 5 4 7 " m 1 l 600e-9 w 4.5e-6 "
; nmos4 Instance /+0 = auLvs device Q11
i11 nmos 4 6 7 7 " m 1 l 600e-9 w 4.5e-6 "
```

Part 2i – Simulation Schematic



Part 2i – Waveform (**before** power spike mitigation using delays)



Part 2i – Waveform (**after** power spike mitigation using delays)



Part 2i – Spectre Simulation Netlist

```
// Library name: lab3_boyz_dnoronha
// Cell name: part2_circuit
// View name: schematic
subckt part2_circuit a b c d e f y
    P5 (y d net33 vdd!) ami06P w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u \
        pd=15.0u m=1 region=sat
    P4 (y c net33 vdd!) ami06P w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u \
        pd=15.0u m=1 region=sat
    P3 (net33 f vdd! vdd!) ami06P w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u \
        pd=15.0u m=1 region=sat
    P2 (net33 e vdd! vdd!) ami06P w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u \
        pd=15.0u m=1 region=sat
    P1 (y b net37 vdd!) ami06P w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u \
        pd=15.0u m=1 region=sat
    P0 (net37 a vdd! vdd!) ami06P w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u \
        pd=15.0u m=1 region=sat
    N5 (net35 e 0 0) ami06N w=4.5u l=600n as=6.75e-12 ad=6.75e-12 ps=12.0u \
        pd=12.0u m=1 region=sat
    N4 (net36 c 0 0) ami06N w=4.5u l=600n as=6.75e-12 ad=6.75e-12 ps=12.0u \
        pd=12.0u m=1 region=sat
    N3 (net27 f net35 0) ami06N w=4.5u l=600n as=6.75e-12 ad=6.75e-12 \
        ps=12.0u pd=12.0u m=1 region=sat
    N2 (net27 d net36 0) ami06N w=4.5u l=600n as=6.75e-12 ad=6.75e-12 \
        ps=12.0u pd=12.0u m=1 region=sat
    N1 (y b net27 0) ami06N w=4.5u l=600n as=6.75e-12 ad=6.75e-12 ps=12.0u \
        pd=12.0u m=1 region=sat
    N0 (y a net27 0) ami06N w=4.5u l=600n as=6.75e-12 ad=6.75e-12 ps=12.0u \
        pd=12.0u m=1 region=sat
    V1 (0 0) vsource type=dc dc=0
    V0 (vdd! 0) vsource type=dc dc=5
ends part2_circuit
// End of subcircuit definition.
```

```
// Library name: lab3_boyz_dnoronha
// Cell name: sim_part2_circuit
// View name: schematic
I0 (A B C D E F Y) part2_circuit
V5 (A 0) vsource type=pulse val0=0 val1=5 period=1u delay=10n rise=2.5n \
    fall=2.5n width=497.5n
V4 (B 0) vsource type=pulse val0=0 val1=5 period=2u delay=12.5n rise=2.5n \
    fall=2.5n width=997.5n
V3 (C 0) vsource type=pulse val0=0 val1=5 period=4u delay=12.5n rise=2.5n \
    fall=2.5n width=1.9975u
```

```
V2 (D 0) vsource type=pulse val0=0 val1=5 period=8u delay=12.5n rise=2.5n \
    fall=2.5n width=3.9975u
V1 (E 0) vsource type=pulse val0=0 val1=5 period=16u delay=10n rise=2.5n \
    fall=2.5n width=7.9975u
V0 (F 0) vsource type=pulse val0=0 val1=5 period=32u delay=10n rise=2.5n \
    fall=2.5n width=15.9975u
```

Part 2i - Power Spike Mitigation Explanation

The updated delays reduced the spikes significantly. The new delay values were chosen to ensure that the pull-up network switches off in order.

Transistors with inputs B, C, and D have a delay 2.5ns greater than the others because they are the first in the series of 2 transistors that VDD must get through to propagate to the output. Only one of the two series transistors on each branch will switch off at a given time, reducing the power spikes. The spikes generally result when multiple transistors switch at (what should be) a fixed logic level, so using delays helps reduce the overlap in waveforms from transistors in series while holding a given logic level, mitigating the spikes. The only drawback is that the one worst-case pull-down network spike gets much worse, even exceeding noise margins.