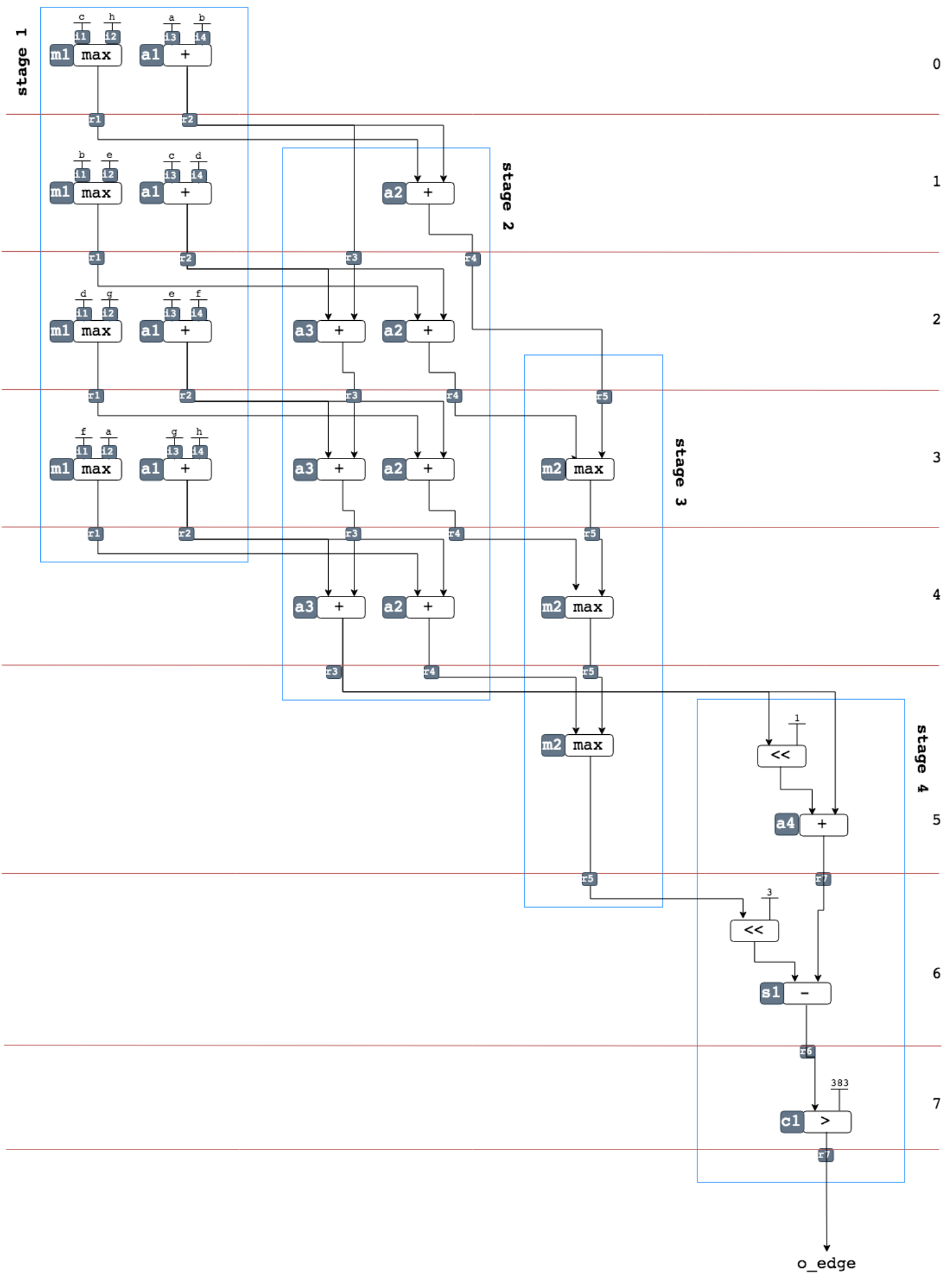
stage 1
stage 2
stage 3
stage 4
0
1
2
3
4
5
6
7
c
h
i1
i2
m1
max
a
b
i3
i4
a1
+
r1
r2
b
e
c
d
a2
r3
r4
d
g
e
f
a3
r5
f
a
g
h
m2
1
<<
a4
r7
3
s1
-
r6
383
c1
>
o_edge

System Measurements:

Latency = 8

Throughput = 1/4

Resources:

- 4 8-bit Adders with no mux
  - 4*8 LUTs
  - 1.77 delay
- 2 8-bit Max with no mux = 2 8-bit Comparators with no mux + 2 2:1 muxes
  - 2*(4 +1) LUTs
  - 1.50 delay
- 8-bit Subtractor with no mux
  - 11 LUTs
  - 2.86 delay
- 8-bit Comparator with no mux
  - 4 LUTs
  - 1.50 delay
- 3 8-bit Registers with 2:1 mux
  - 3*1 LUTs
  - 0.76 delay
- 4 8-bit Registers with no mux
  - 0 LUTs
  - 0.31 delay

Total LUTs = 60 LUTs

Total Flops = 56 Flops

DFD Area = 60 Cells

Total Area = DFD Area + Circuitry for control and to update memory + convolution table = 60 cells + 160 cells + 72 cells = 292 cells

Max Clock Speed = Subtractor + Flop with no mux = 1/((2.86 + 0.31)*10^(-9)) = 315 MHz

Optimality = Functionality Score * (Max Clock Speed / Total Area) = 1000 * (315 MHz / 292 cells) = 1079

Calculations:

o_edge = max_edge > 383

max_edge =

max(

5(a+b+c)-3(d+e+f+g+h),

5(b+c+d)-3(e+f+g+h+a),

5(c+d+e)-3(f+g+h+a+b),

5(d+e+f)-3(g+h+a+b+c),

5(e+f+g)-3(h+a+b+c+d),

5(f+g+h)-3(a+b+c+d+e),

5(g+h+a)-3(b+c+d+e+f),

5(h+a+b)-3(c+d+e+f+g)

)

Optimization 1: 5a - 3 = 8a - 3(a+b)

max_edge =

max(

8(a+b+c)-3(a+b+c+d+e+f+g+h),

8(b+c+d)-3(a+b+c+d+e+f+g+h),

8(c+d+e)-3(a+b+c+d+e+f+g+h),

8(d+e+f)-3(a+b+c+d+e+f+g+h),

8(e+f+g)-3(a+b+c+d+e+f+g+h),

8(f+g+h)-3(a+b+c+d+e+f+g+h),

8(g+h+a)-3(a+b+c+d+e+f+g+h),

8(h+a+b)-3(a+b+c+d+e+f+g+h)

)

Optimization 2: max(a-c, b-c) = max(a, b)-c

max_edge =

8*max(

(a+b+c), (h+a+b)),

(b+c+d), (c+d+e),

(d+e+f), (e+f+g),

(f+g+h), (g+h+a)

)

-3(a+b+c+d+e+f+g+h)

Optimization 3: max(a+b, b+c) = b+max(a,c)

8*max(

a+b+max(c, h),

c+d+max(b, e),

e+f+max(d, g),

g+h+max(f, a)

)

-3(a+b+c+d+e+f+g+h)