Laboratory Report #___

Name: Josh Ratificar **Date Completed:** 09/01/2023

Laboratory Exercise Title: Design Flow of Digital Systems

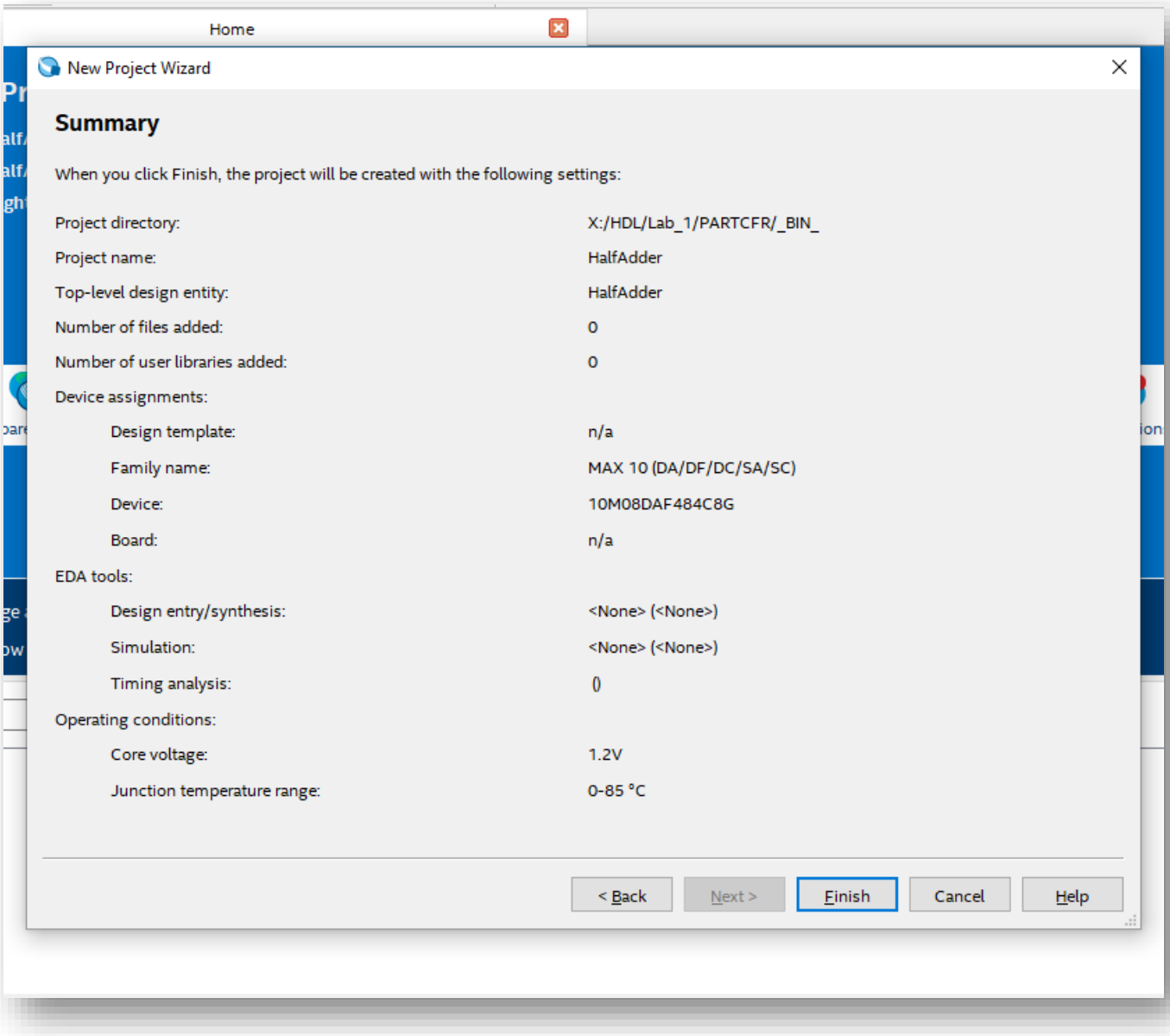

Figure 1.0 – *Project Summary*

```
1
2   /// Verilog HDL code for Half Adder
3   /// -------------------------------
4   ///
5   /// Name:       Josh Ratificar
6   /// Schedule:   Group 3 CpE 3101L - Introduction to HDL | 7:30 AM to 10:30 AM, Thursday
7   ///
8   ///
9
10  module HalfAdder (x, y, C, S);
11     input x, y;
12     output   C, S;
13     xor    X1 (S, x, y);
14     and    A1 (C, x, y);
15  endmodule
16
```

Figure 2.0 – *Verilog HDL Code for Half Adder Circuit*

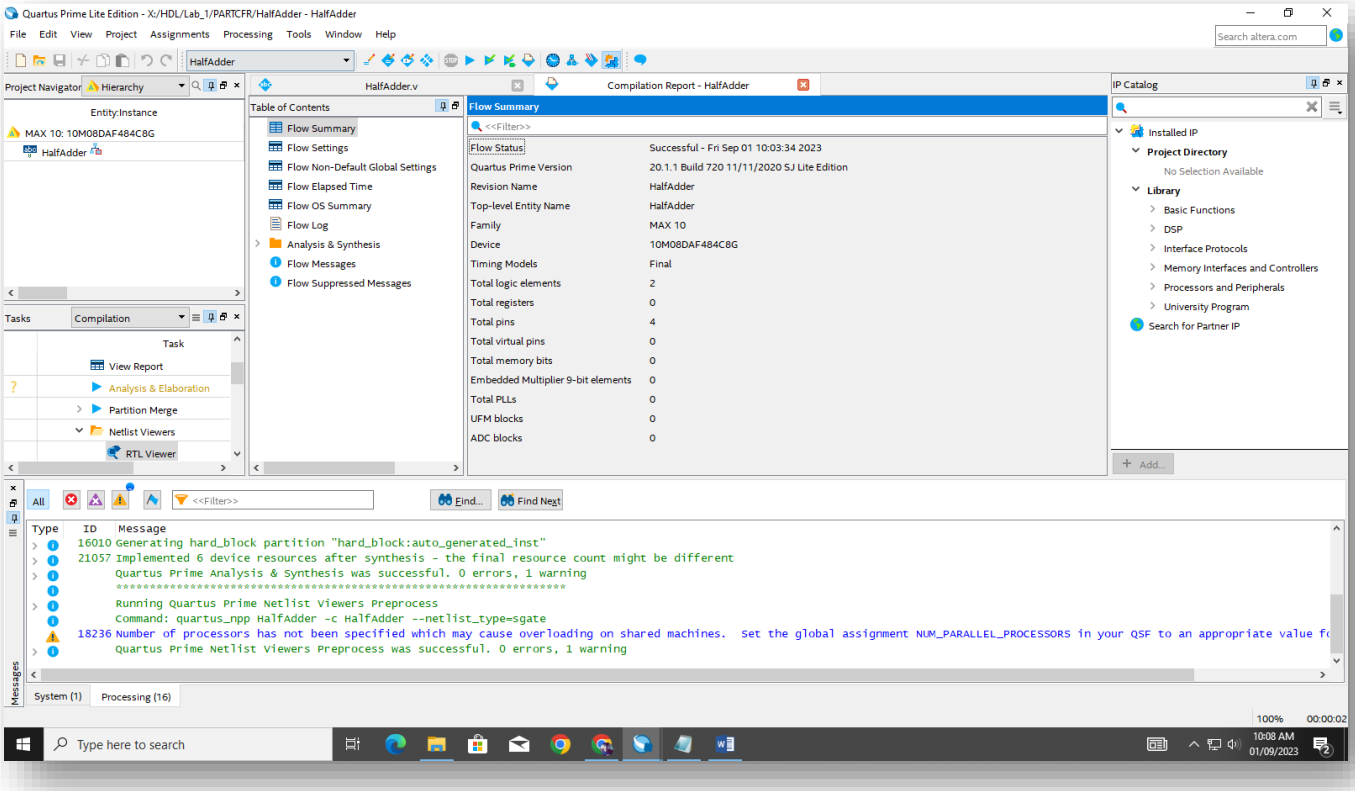

Figure 3.0 – *Verilog HDL Code Compilation Report*

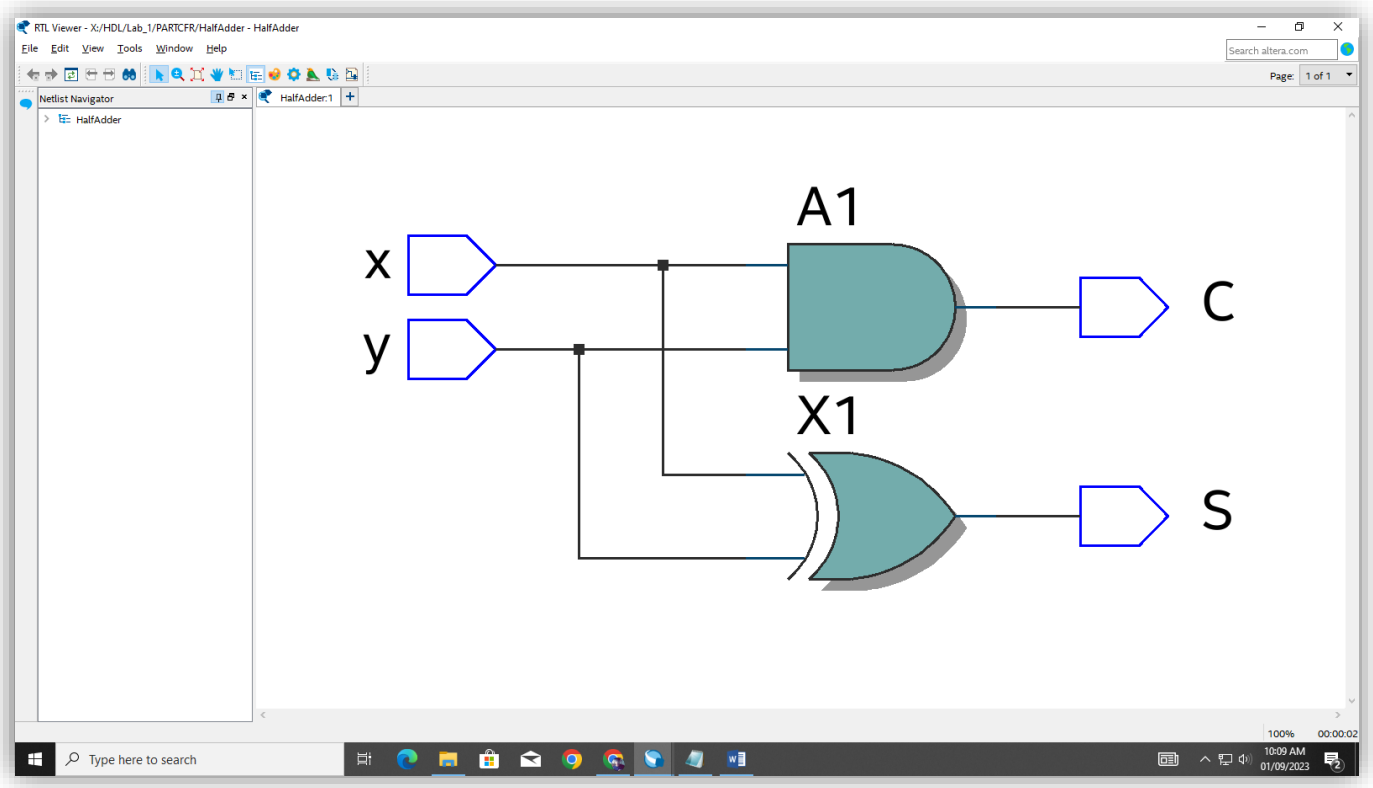

Figure 4.0 – *RCL Generated Schematic*

Exercise C Summary and Learnings:

The objective of this exercise was to familiarize myself with the user interface of the Quartus application. Within performing this exercise, I learned how to appropriately create a project, populate my project with new files, and as well compile and analyze my outputs. I as well studied the meaning of the syntax used in the description of the hardware which explains how the inputs and outputs correlate with each logic component.