Laboratory Exercise #6

Behavioral Modeling of Sequential Circuits

Name: _____ **Group:** _____

Target Course Outcomes:

CO1: Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

CO2: Verify the functionality of HDL-based components through design verification tools.

Intended Learning Outcomes:

- Create design entry of a sequential circuit using behavioral modeling in Verilog HDL code
- Synthesize the Verilog HDL design entry
- Simulate the designed circuit using a testbench file
- Fit a synthesized circuit into an Intel FPGA
- Programming and configuring the FPGA chip on Intel DE-series board (DE10-Lite)

Supplement:

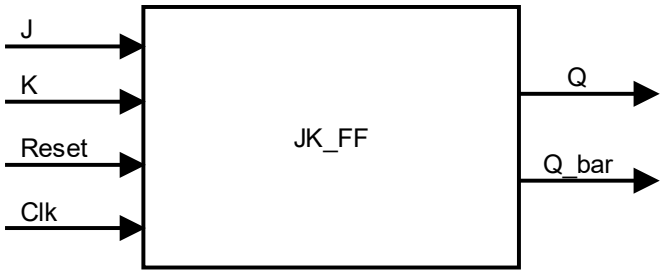
This exercise requires a basic understanding of the Intel Quartus Prime design flow with ModelSim functional verification, as detailed in Units 1-2 and Laboratory Exercises #1-2. It is also expected that Laboratory Exercise #5 has already been completed before performing this exercise.

Instructions:

Perform this hands-on laboratory exercise after attending/watching the onsite/online lecture for Unit 6. This activity is intended to be done individually.

Exercise 6A: JK Flip-flop

Create a **behavioral description** of a ***JK flip-flop*** using **either if-else statements or a case statement**. Refer to the entity diagram below for reference. Synthesize and simulate the design. Show both a simulation log (standard output) and simulation waveform (timing diagram) in the laboratory report.



**Clk: negative-edged (falling-edge) triggered*
Reset: asynchronous reset (active high)

Figure 1. Entity Diagram of Negative-edged Triggered JK Flip-flop

Test Cases: Assert reset (**Reset**) at the start of the simulation for a couple of **Clk** edges, while varying the **JK** input values. Then, de-assert **Reset** and continue to vary **JK** inputs. Prioritize the simulation waveforms (timing diagram) in the laboratory report.

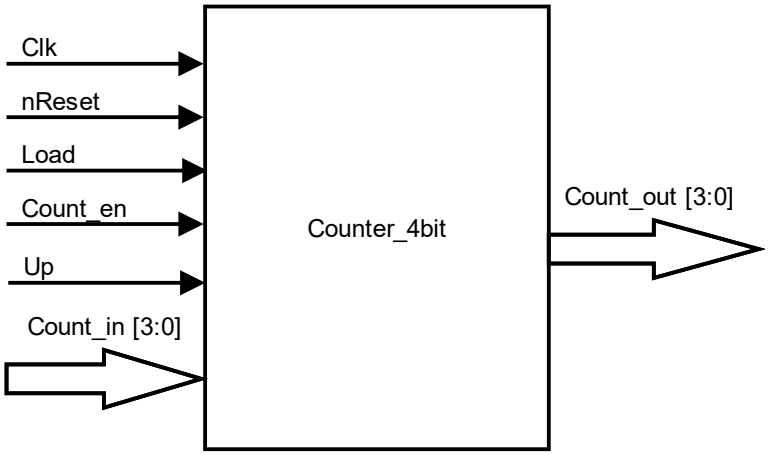
FPGA Implementation: After simulation, load the appropriate design file into the FPGA to test the functionality of the design. Refer to the onsite orientation and other attachments for this section.

Evaluation:

Level / Criteria	1.0 Outstanding	2.0 Competent	3.0 Marginal	5.0 Not Acceptable	Rating
CO1: Verilog Design Entry	Verilog HDL description is correct and follows specified instructions.	--	Verilog HDL description is correct but DID NOT follow the specified instructions.	NO Verilog HDL description is presented or the design entry is INCORRECT.	
CO1: Design Synthesis	Verilog HDL description is synthesized and compiled with NO issues (with 0-1 warning). There is clear evidence in the lab report that supports this result.	Verilog HDL description is synthesized and compiled with MINOR issues on constructs (with 2-3 warnings). There is clear evidence in the lab report that supports this result.	Verilog HDL description is synthesized and compiled with MAJOR issues on constructs (with 4 or more warnings). There is evidence in the lab report that supports this result.	Simulation has FAILED or there is NO evidence showing a successful simulation.	
CO2: Verilog Testbench Entry	Verilog HDL testbench is correct and follows specified instructions. ALL possible input combinations or AMPLE test stimuli are included to generate sufficient and verifiable output results.	--	Verilog HDL testbench is correct but DID NOT follow specified instructions. Possible input combinations may be INCOMPLETE or test stimuli are NOT SUFFICIENT included to generate verifiable output results.	NO Verilog testbench is presented or INCOMPLETE.	
CO2: Functional Verification	Simulation of the synthesized design is functional with NO issues and shows ALL correct and expected results. An analysis is made by providing image annotations and/or discussions of the results. There is clear evidence in the lab report that supports this.	Simulation of the synthesized design is functional. Expected results may be INCOMPLETE but are ALL correct. An analysis is made by providing image annotations and/or discussions of the results. There is clear evidence in the lab report that supports this.	Simulation of the synthesized design is functional. Expected results may be INCOMPLETE or there may be INCORRECT results. NO analysis is made with NO image annotations and/or discussions of the results. There is clear evidence in the lab report that supports this.	Simulation has FAILED or there is NO evidence showing a successful simulation.	
CO3: Design Flow	Synthesized HDL-based design file was properly loaded into the FPGA with NO problems.	--	Synthesized HDL-based design file was loaded into the FPGA with A FEW technical issues.	Synthesized HDL-based design file WAS NOT PROPERLY loaded into the FPGA.	
CO3: Accuracy of Results on FPGA	Results are ALL ACCURATE as expected and recorded data is validated upon checking.	--	Results are MOSTLY ACCURATE and recorded data is validated upon checking.	Results are ERRONEOUS or recorded data CANNOT be validated upon checking.	

Exercise 6B: 4-Bit Binary Up/Down Counter

Design a **4-bit binary up/down counter** using **behavioral description** with a function table and entity diagram shown below.



**Clk: negative-edged (falling-edge) triggered*
nReset: asynchronous reset (active low)

Figure 2. Entity Diagram of 4-bit Counter

Function Table:

nReset	Clk	Load	Count_en	Up	Counter Operation
0	X	X	X	X	Reset to 0
1	↓	1	X	X	Load inputs (parallel load)
1	↓	0	0	X	No change
1	↓	0	1	0	Count down
1	↓	0	1	1	Count up

Test Cases: Design the testbench to show ALL counter operations shown in the function table. Prioritize the simulation waveforms (timing diagram) in the laboratory report.

FPGA Implementation: After simulation, load the appropriate design file into the FPGA to test the functionality of the design. Refer to the onsite orientation and other attachments for this section. **Additional module needed: Clock divider**

Evaluation:

Level / Criteria	1.0 Outstanding	2.0 Competent	3.0 Marginal	5.0 Not Acceptable	Rating
CO1: Verilog Design Entry	Verilog HDL description is correct and follows specified instructions.	--	Verilog HDL description is correct but DID NOT follow the specified instructions.	NO Verilog HDL description is presented or the design entry is INCORRECT.	

CO1: Design Synthesis	Verilog HDL description is synthesized and compiled with NO issues (with 0-1 warning). There is clear evidence in the lab report that supports this result.	Verilog HDL description is synthesized and compiled with MINOR issues on constructs (with 2-3 warnings). There is clear evidence in the lab report that supports this result.	Verilog HDL description is synthesized and compiled with MAJOR issues on constructs (with 4 or more warnings). There is evidence in the lab report that supports this result.	Simulation has FAILED or there is NO evidence showing a successful simulation.	
CO2: Verilog Testbench Entry	Verilog HDL testbench is correct and follows specified instructions. ALL possible input combinations or AMPLE test stimuli are included to generate sufficient and verifiable output results.	--	Verilog HDL testbench is correct but DID NOT follow specified instructions. Possible input combinations may be INCOMPLETE or test stimuli are NOT SUFFICIENT included to generate verifiable output results.	NO Verilog testbench is presented or INCOMPLETE.	
CO2: Functional Verification	Simulation of the synthesized design is functional with NO issues and shows ALL correct and expected results. An analysis is made by providing image annotations and/or discussions of the results. There is clear evidence in the lab report that supports this.	Simulation of the synthesized design is functional. Expected results may be INCOMPLETE but are ALL correct. An analysis is made by providing image annotations and/or discussions of the results. There is clear evidence in the lab report that supports this.	Simulation of the synthesized design is functional. Expected results may be INCOMPLETE or there may be INCORRECT results. NO analysis is made with NO image annotations and/or discussions of the results. There is clear evidence in the lab report that supports this.	Simulation has FAILED or there is NO evidence showing a successful simulation.	
CO3: Design Flow	Synthesized HDL-based design file was properly loaded into the FPGA with NO problems.	--	Synthesized HDL-based design file was loaded into the FPGA with A FEW technical issues.	Synthesized HDL-based design file WAS NOT PROPERLY loaded into the FPGA.	
CO3: Accuracy of Results on FPGA	Results are ALL ACCURATE as expected and recorded data is validated upon checking.	--	Results are MOSTLY ACCURATE and recorded data is validated upon checking.	Results are ERRONEOUS or recorded data CANNOT be validated upon checking.	

For the laboratory report (LR #6), include the following items:

- **For both Exercises 6A and 6B:**
  - Proof of successful design synthesis *(screenshot showing 0 errors)*
  - Proof of successful simulation results with required number of test cases *(screenshots of simulation results with annotations or discussion of results)*
  - Proof of successful FPGA implementation *(1 sample photo of the board with sample result)*
- All Verilog files (.v) must be submitted along with LR #6