



Laboratory Report #____

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Date Completed: 09/01/2023

Laboratory Exercise Title: Design Flow of Digital Systems

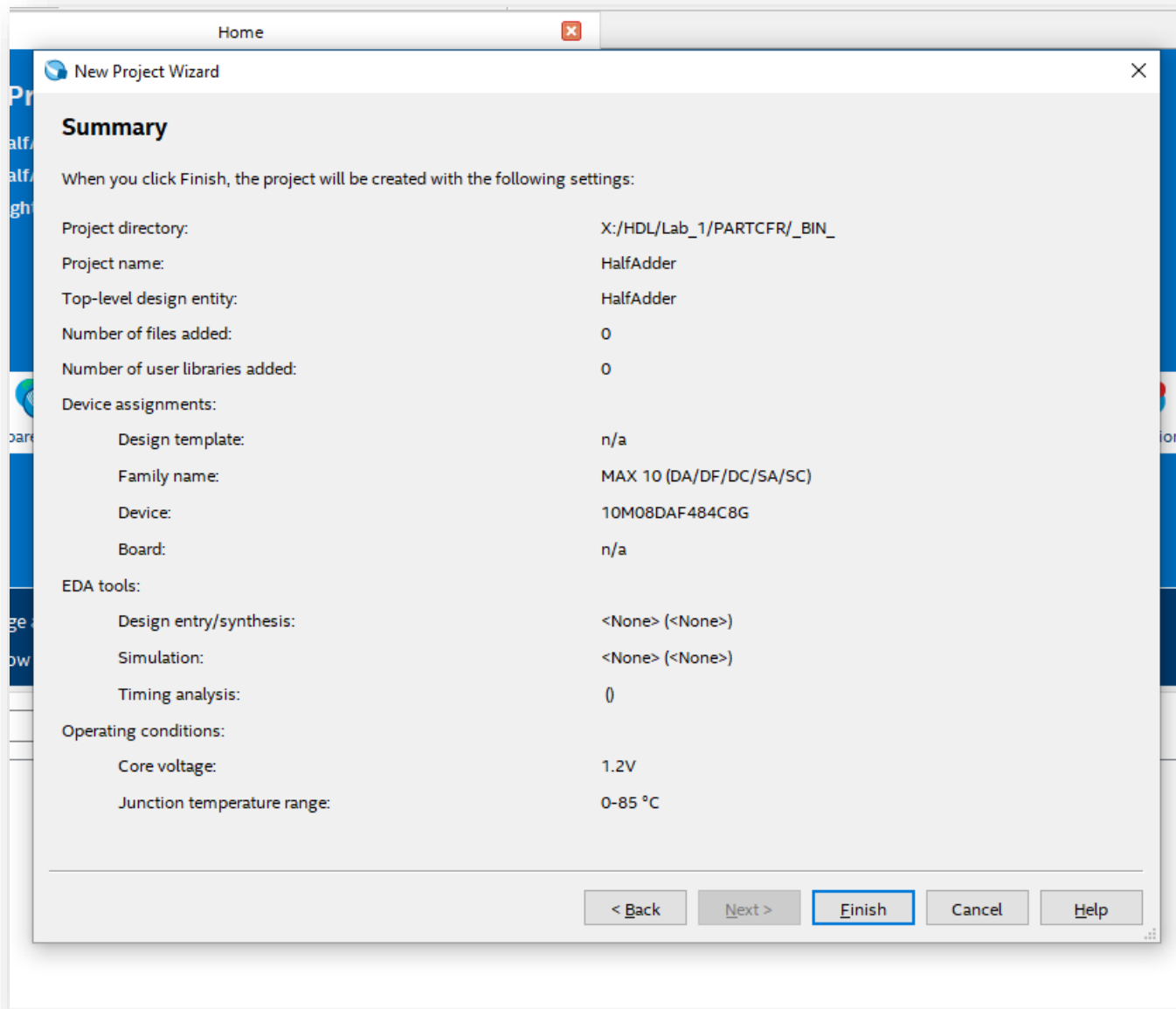


Figure 1.0 – Project Summary



```
1 // Verilog HDL code for Half Adder
2 -----
3
4 //
5 Name:      Josh Ratificar
6 Schedule:  Group 3 CpE 3101L - Introduction to HDL | 7:30 AM to 10:30 AM, Thursday
7 //
8
9
10 module HalfAdder (x, y, c, s);
11     input  x, y;
12     output c, s;
13     xor    x1 (s, x, y);
14     and    A1 (c, x, y);
15 endmodule
16 |
```

Figure 2.0 – Verilog HDL Code for Half Adder Circuit

The screenshot displays the Quartus Prime Lite Edition interface. The main window shows the 'Flow Summary' report for the 'HalfAdder.v' file. The report indicates a successful compilation on Friday, September 1, 2023, at 10:03:34. The device used is '10M08DAF484C8G' (MAX 10). The report lists various statistics: 2 total logic elements, 0 total registers, 4 total pins, 0 total virtual pins, 0 total memory bits, 0 embedded multiplier 9-bit elements, 0 total PLLs, 0 UFM blocks, and 0 ADC blocks. The 'Messages' window at the bottom shows several messages, including a warning about the number of processors (16) and a message about the final resource count.

Flow Status	Flow Summary
Successful - Fri Sep 01 10:03:34 2023	Quartus Prime Version: 20.1.1 Build 720 11/11/2020 SJ Lite Edition
	Revision Name: HalfAdder
	Top-level Entity Name: HalfAdder
	Family: MAX 10
	Device: 10M08DAF484C8G
	Timing Models: Final
	Total logic elements: 2
	Total registers: 0
	Total pins: 4
	Total virtual pins: 0
	Total memory bits: 0
	Embedded Multiplier 9-bit elements: 0
	Total PLLs: 0
	UFM blocks: 0
	ADC blocks: 0

Figure 3.0 – Verilog HDL Code Compilation Report

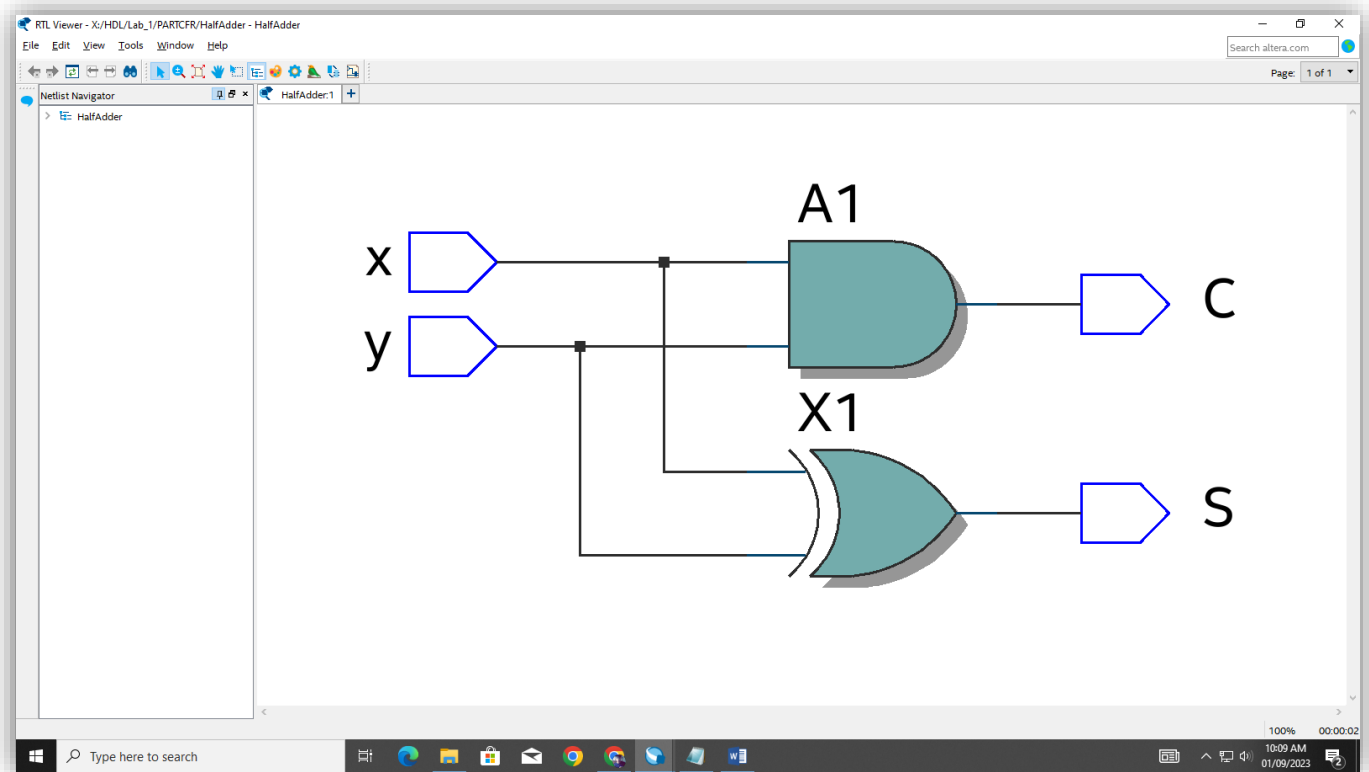


Figure 4.0 – RCL Generated Schematic

Exercise C Summary and Learnings:

The objective of this exercise was to familiarize myself with the user interface of the Quartus application. Within performing this exercise, I learned how to appropriately create a project, populate my project with new files, and as well compile and analyze my outputs. I as well studied the meaning of the syntax used in the description of the hardware which explains how the inputs and outputs correlate with each logic component.