Laboratory Exercise #4

Dataflow Modeling of Combinational Circuits

Name: _____ **Group:** _____

Target Course Outcomes:

CO1: Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

CO2: Verify the functionality of HDL-based components through design verification tools.

Intended Learning Outcomes:

- Create design entry of a combinational circuit using dataflow modeling in Verilog HDL code
- Synthesize the Verilog HDL design entry
- Simulate the designed circuit using a testbench file

Supplement:

This exercise requires a basic understanding of the Intel Quartus Prime design flow with ModelSim functional verification, as detailed in Units 1-2 and Laboratory Exercises #1-2. It is also expected that Laboratory Exercise #3 has already been completed before performing this exercise.

Instructions:

Perform this hands-on laboratory exercise after attending/watching the onsite/online lecture for Unit 4. This activity is intended to be done individually.

Exercise 4A: 4-Bit Comparator

Under a new project, create a Verilog HDL description of a ***4-bit comparator*** using **dataflow modeling**. Refer to the entity diagram and output details below for reference. Synthesize the design and simulate to verify the results. Show both a simulation log (standard output) and simulation waveform (timing diagram) in the laboratory report.

Output Details:

R [2] = G (1 if **A** > **B**, else 0)
R [1] = E (1 if **A** = **B**, else 0)
R [0] = L (1 if **A** < **B**, else 0)

Note: *G* (*"greater than"* is TRUE)
E (*"equal to"* is TRUE)
L (*"less than"* is TRUE)

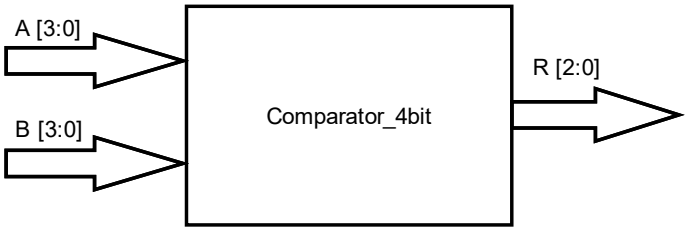

Figure 1. Entity Diagram of 4-bit Comparator

Test Cases: Give at least 10 cases of varying test values with varying output results.

Evaluation:

Level / Criteria	1.0 Outstanding	2.0 Competent	3.0 Marginal	5.0 Not Acceptable	Rating
CO1: Verilog Design Entry	Verilog HDL description is correct and follows specified instructions.	--	Verilog HDL description is correct but DID NOT follow the specified instructions.	NO Verilog HDL description is presented or the design entry is INCORRECT.	
CO1: Design Synthesis	Verilog HDL description is synthesized and compiled with NO issues (with 0-1 warning). There is clear evidence in the lab report that supports this result.	Verilog HDL description is synthesized and compiled with MINOR issues on constructs (with 2-3 warnings). There is clear evidence in the lab report that supports this result.	Verilog HDL description is synthesized and compiled with MAJOR issues on constructs (with 4 or more warnings). There is evidence in the lab report that supports this result.	Simulation has FAILED or there is NO evidence showing a successful simulation.	
CO2: Verilog Testbench Entry	Verilog HDL testbench is correct and follows specified instructions. ALL possible input combinations or AMPLE test stimuli are included to generate sufficient and verifiable output results.	--	Verilog HDL testbench is correct but DID NOT follow specified instructions. Possible input combinations may be INCOMPLETE or test stimuli are NOT SUFFICIENT included to generate verifiable output results.	NO Verilog testbench is presented or INCOMPLETE.	
CO2: Functional Verification	Simulation of the synthesized design is functional with NO issues and shows ALL correct and expected results. An analysis is made by providing image annotations and/or discussions of the results. There is clear evidence in the lab report that supports this.	Simulation of the synthesized design is functional. Expected results may be INCOMPLETE but are ALL correct. An analysis is made by providing image annotations and/or discussions of the results. There is clear evidence in the lab report that supports this.	Simulation of the synthesized design is functional. Expected results may be INCOMPLETE or there may be INCORRECT results. NO analysis is made with NO image annotations and/or discussions of the results. There is clear evidence in the lab report that supports this.	Simulation has FAILED or there is NO evidence showing a successful simulation.	

Exercise 4B: *n*-Bit 4-to-1 Line Multiplexer

Design a **dataflow description** of an ***n-bit 4x1 multiplexer***. Use a **parameter** to change the value of ***n*** (use ***n*** = 4 as the default value). Refer to the entity diagram and truth table below for reference. Synthesize the design.

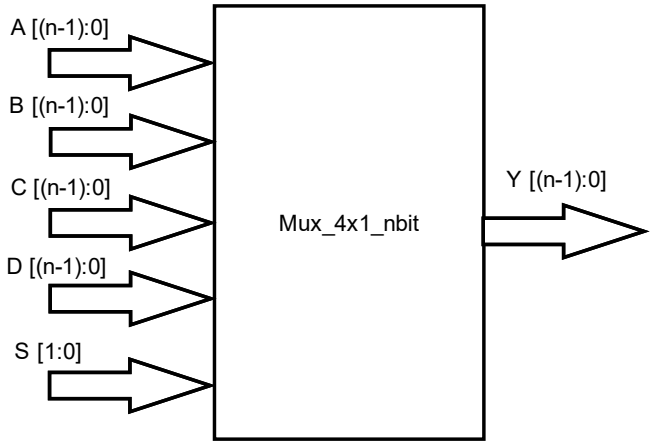

Figure 2. Entity Diagram of n-Bit 4x1 Multiplexer

Truth Table:

Selector S	Output Y
00	A
01	B
10	C
11	D

Part 1: 4-bit 4x1 Multiplexer

Create a testbench and instantiate the UUT as an *n*-bit 4x1 mux to this configuration: ***n = 4*** (for 4-bit inputs). Simulate and verify the results. Show both a simulation log (standard output) and simulation waveform (timing diagram) in the laboratory report.

Test Cases: Include ALL possible input combinations for **S** and vary the **4-bit input (A, B, C, D)** values.

Part 2: 8-bit 4x1 Multiplexer

Create a separate testbench and instantiate the UUT as an *n*-bit 4x1 mux to this configuration: ***n = 8*** (for 8-bit inputs). Simulate and verify the results. Show both a simulation log (standard output) and simulation waveform (timing diagram) in the laboratory report.

Test Cases: Include ALL possible input combinations for **S** and vary the **8-bit input (A, B, C, D)** values.

Evaluation:

Level / Criteria	1.0 Outstanding	2.0 Competent	3.0 Marginal	5.0 Not Acceptable	Rating
CO1: Verilog Design Entry	Verilog HDL description is correct and follows specified instructions.	--	Verilog HDL description is correct but DID NOT follow the specified instructions.	NO Verilog HDL description is presented or the design entry is INCORRECT.	
CO1: Design Synthesis	Verilog HDL description is synthesized and compiled with NO issues (with 0-1 warning). There is clear evidence in the lab report that supports this result.	Verilog HDL description is synthesized and compiled with MINOR issues on constructs (with 2-3 warnings). There is clear evidence in the lab report that supports this result.	Verilog HDL description is synthesized and compiled with MAJOR issues on constructs (with 4 or more warnings). There is evidence in the lab report that supports this result.	Simulation has FAILED or there is NO evidence showing a successful simulation.	
CO2: Verilog Testbench Entry	Verilog HDL testbench is correct and follows specified instructions. ALL possible input combinations or AMPLE test stimuli are included to generate sufficient and verifiable output results.	--	Verilog HDL testbench is correct but DID NOT follow specified instructions. Possible input combinations may be INCOMPLETE or test stimuli are NOT SUFFICIENT included to generate verifiable output results.	NO Verilog testbench is presented or INCOMPLETE.	
CO2: Functional Verification	Simulation of the synthesized design is functional with NO issues and shows ALL correct and expected results. An analysis is made by providing image annotations and/or discussions of the results. There is clear evidence in the lab report that supports this.	Simulation of the synthesized design is functional. Expected results may be INCOMPLETE but are ALL correct. An analysis is made by providing image annotations and/or discussions of the results. There is clear evidence in the lab report that supports this.	Simulation of the synthesized design is functional. Expected results may be INCOMPLETE or there may be INCORRECT results. NO analysis is made with NO image annotations and/or discussions of the results. There is clear evidence in the lab report that supports this.	Simulation has FAILED or there is NO evidence showing a successful simulation.	

For the laboratory report (LR #4), include the following items:

- **Exercise 4A: 4-Bit Comparator**
  - Proof of successful design synthesis *(screenshot showing 0 errors)*
  - Proof of successful simulation results with required number of test cases *(screenshots of simulation results with annotations or discussion of results)*
- **Exercise 4B: n-Bit 4-to-1 Line Multiplexer (Part 1 and Part 2)**
  - Proof of successful design synthesis *(screenshot showing 0 errors)*
  - Proof of successful simulation results with required number of test cases *(screenshots of simulation results with annotations or discussion of results)*
- All Verilog files (.v) must be submitted along with LR #4