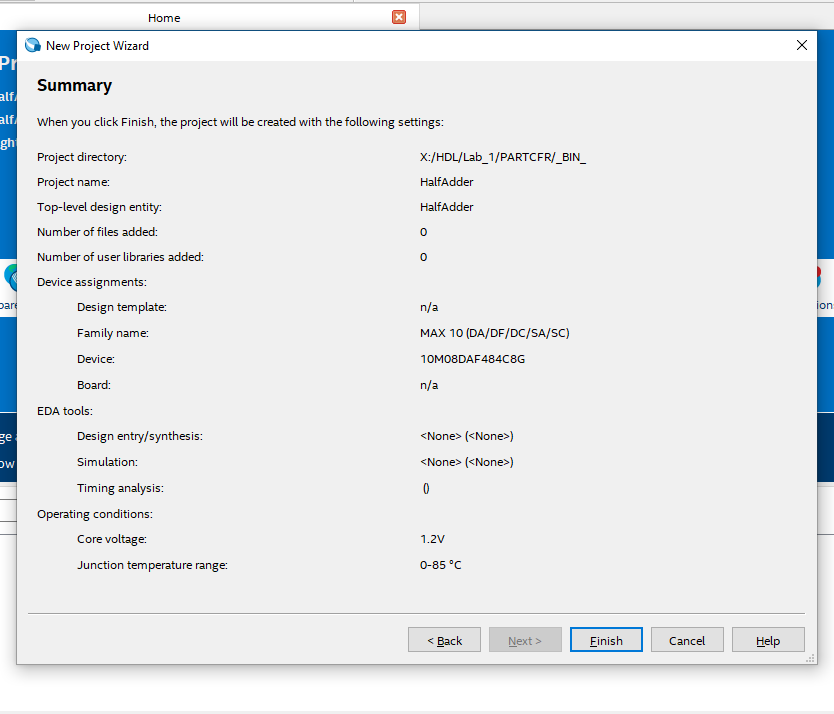
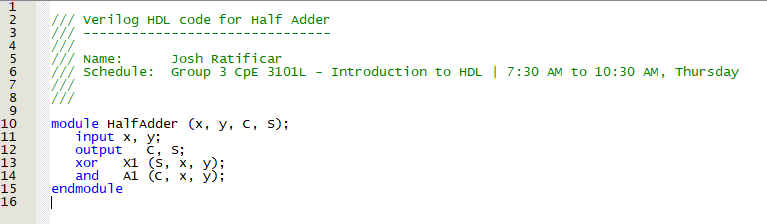
# Laboratory Report #\_\_\_

**Name:** Josh Ratificar **Date Completed:** 09/01/2023

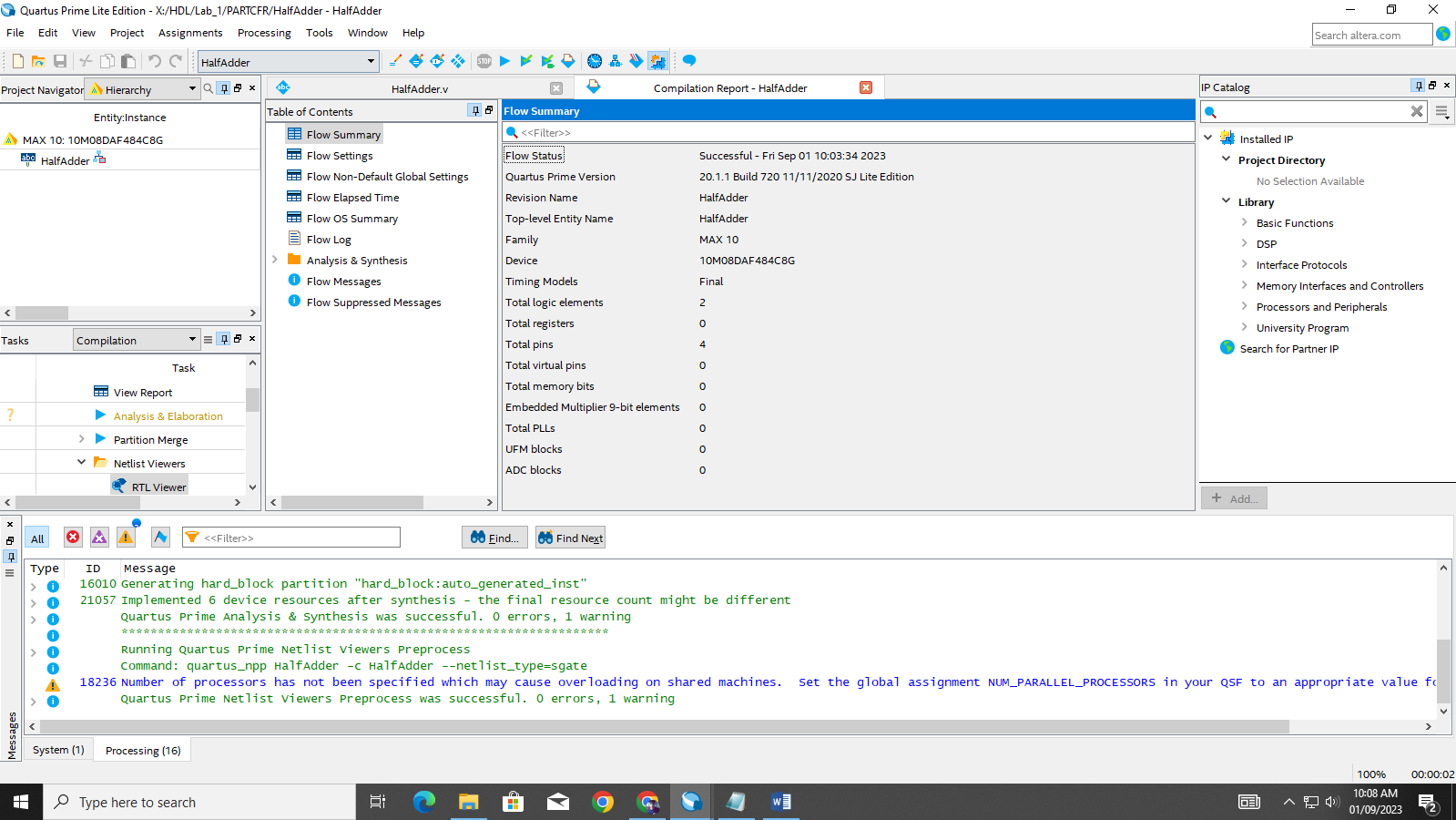
**Laboratory Exercise Title:** Design Flow of Digital Systems



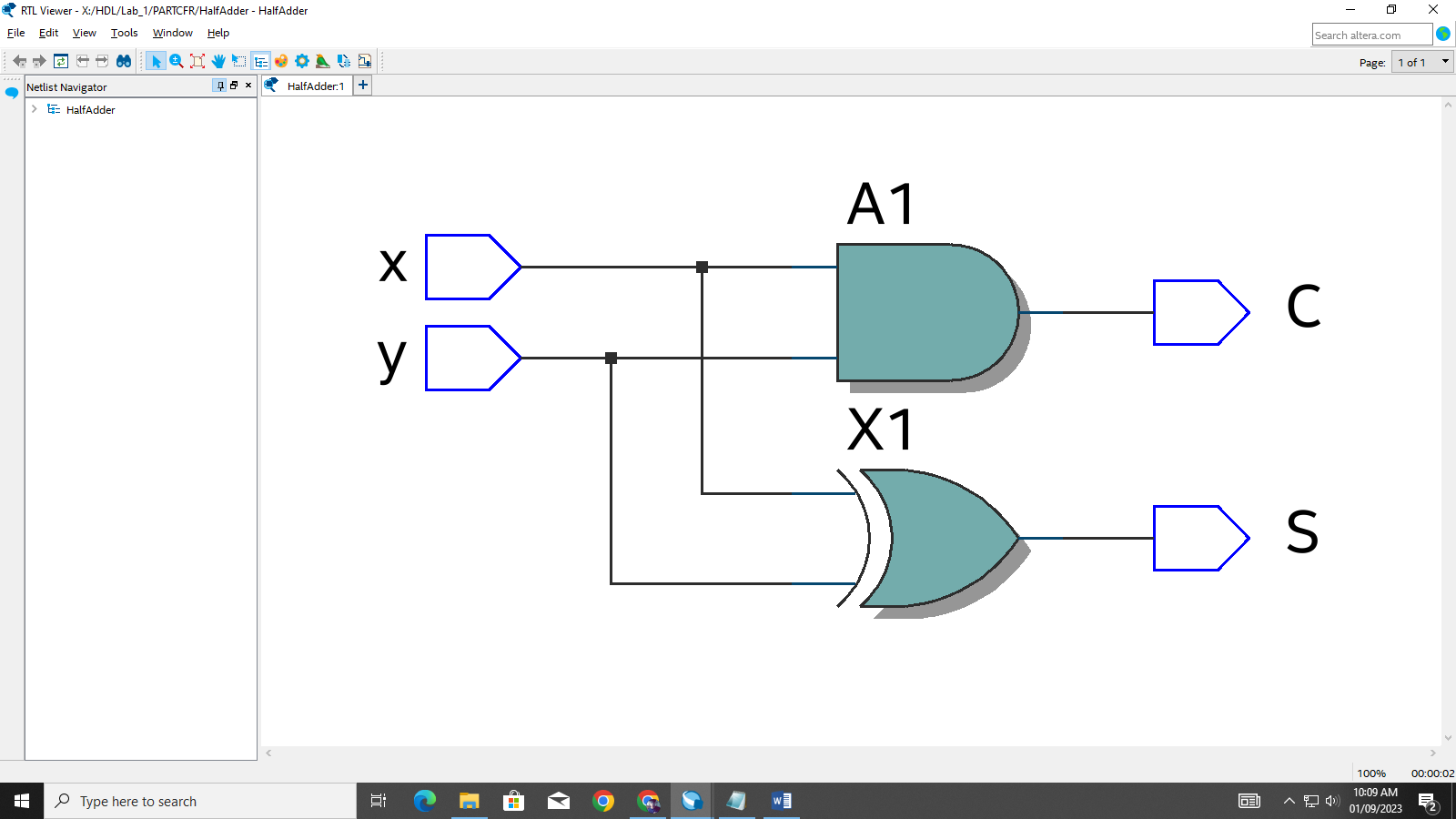
**Figure 1.0 –** *Project Summary*

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**Figure 2.0 –** *Verilog HDL Code for Half Adder Circuit*

**

**Figure 3.0 –** *Verilog HDL Code Compilation Report*

**

**Figure 4.0 –** *RCL Generated Schematic*

**Exercise C Summary and Learnings:**

The objective of this exercise was to familiarize myself with the user interface of the Quartus application. Within performing this exercise, I learned how to appropriately create a project, populate my project with new files, and as well compile and analyze my outputs. I as well studied the meaning of the syntax used in the description of the hardware which explains how the inputs and outputs correlate with each logic component.