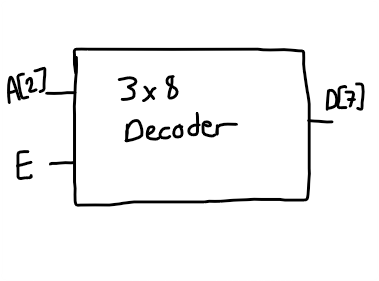
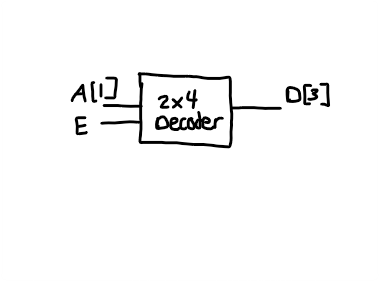
# Laboratory Report #3

**Name:** Josh Ratificar **Date Completed:** 09-23-2023

**Laboratory Exercise Title:** Structural Modeling of Combinational Circuits

**Block Diagrams:**



*Above includes the block diagrams for this Laboratory Exercise. Based on the diagrams, the following can be concluded:*

**2x4 Decoder**

**3-Input Ports:**

* **A[0], A[1], E**

**4-Output Ports:**

* **D[0], D[1], D[2], D[3]**

**3x8 Decoder**

**4-Input Ports:**

* **A[0], A[1], A[2], E**

**8-Output Ports:**

* **D[0], D[1], D[2], D[3], D[4], D[5], D[6], D[7]**

**Exercise 3A:**

**Table 1.0 –** *Truth Table for a 2x4 Decoder*

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| INPUTS | | | OUTPUTS | | | |
| E | A0 | A1 | D0 | D1 | D2 | D3 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 |

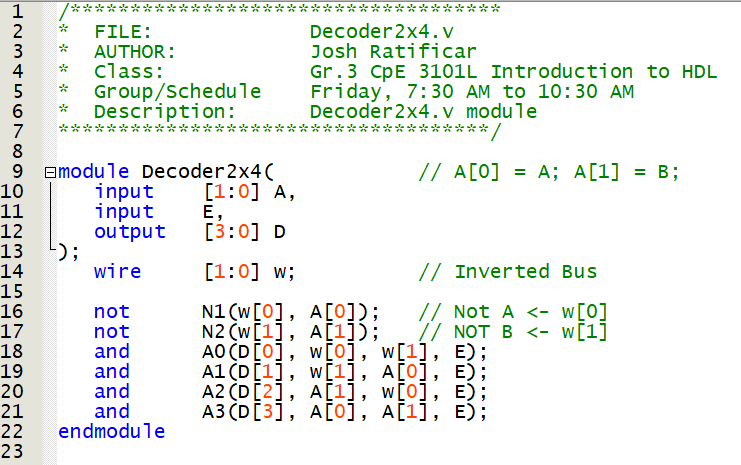
**Boolean Expressions:**

D3 = A0’A1’E

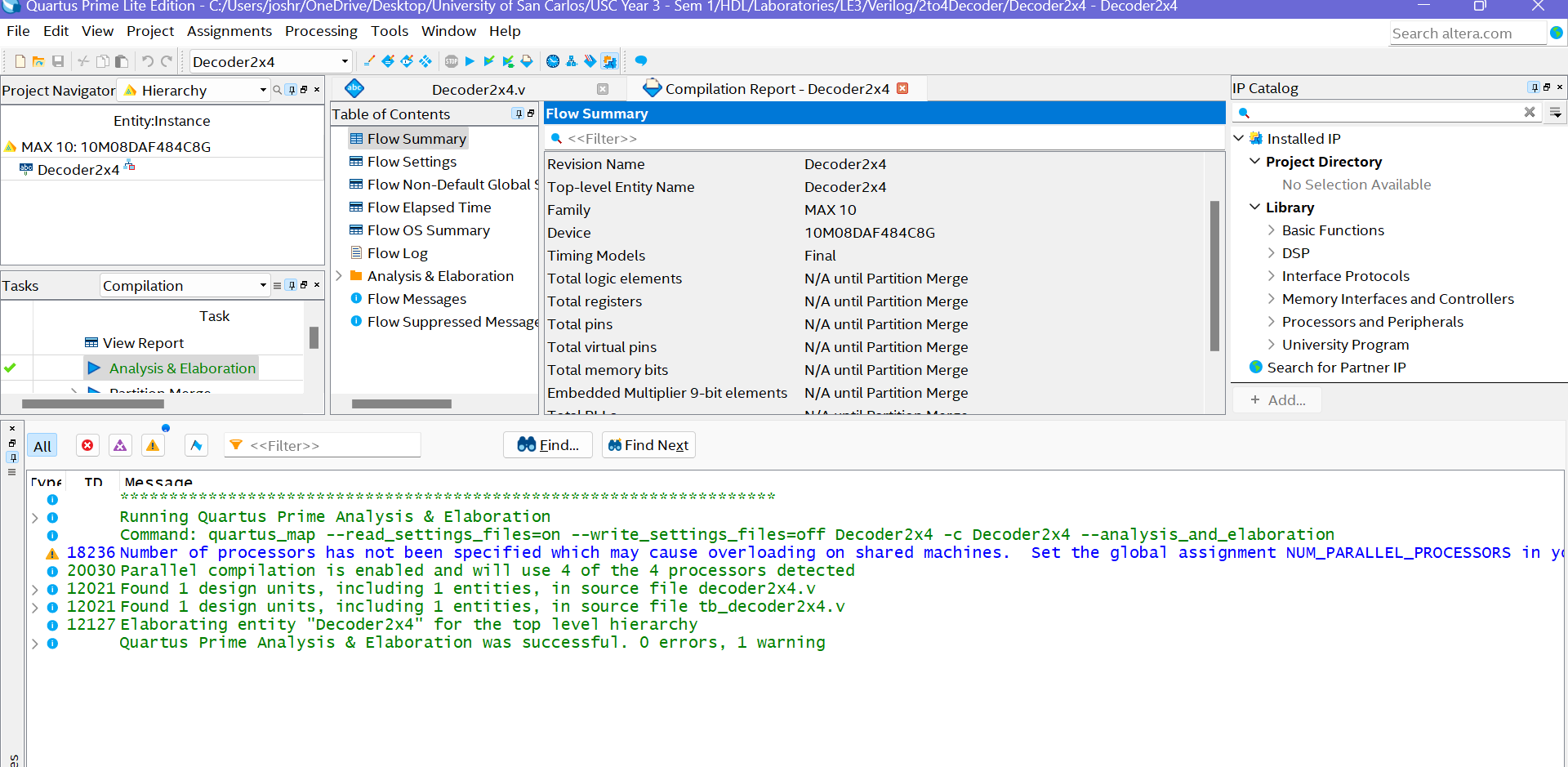
D2 = A0’A1E

D1 = A0A1’E

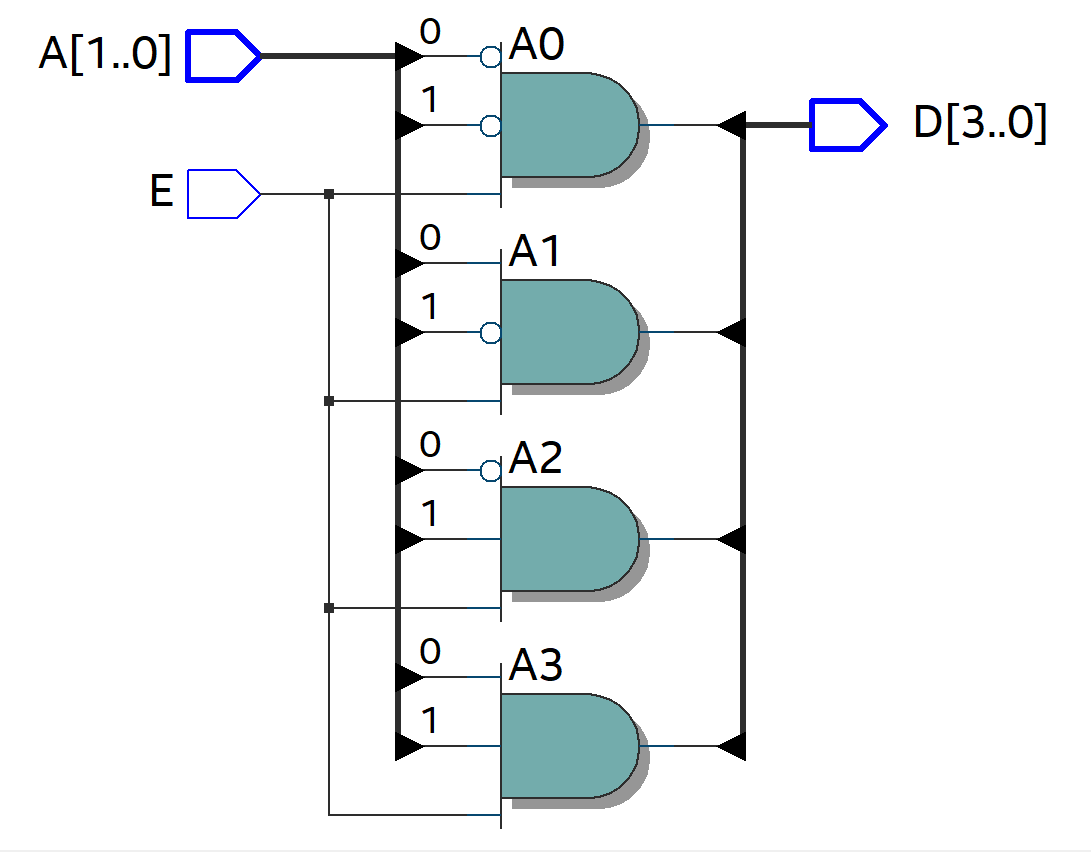
D0 = A0A1E



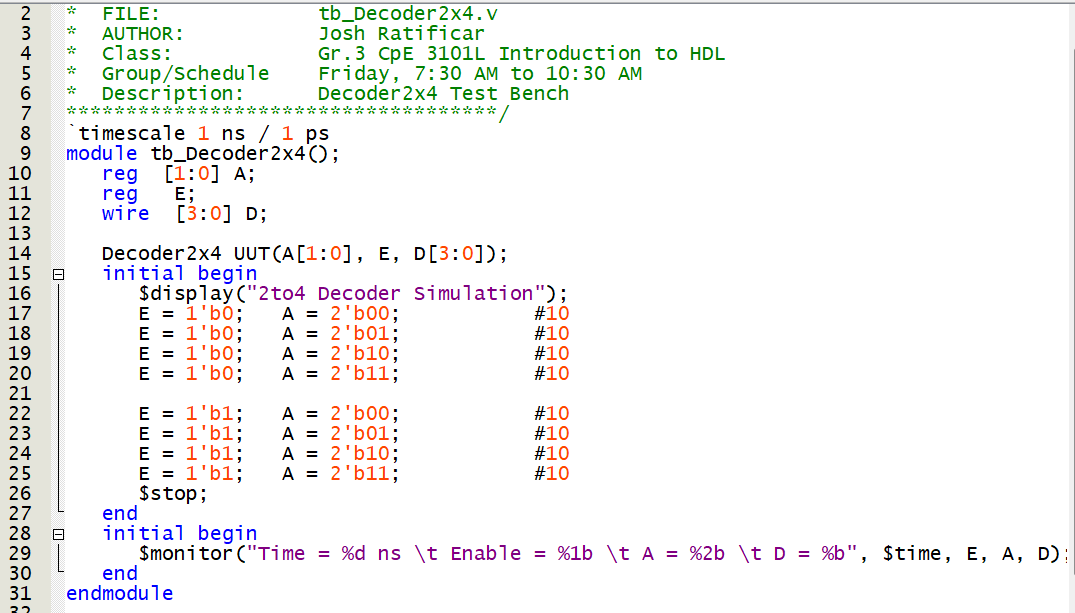
**Figure 1.0** – *Decoder2x4.v Script*

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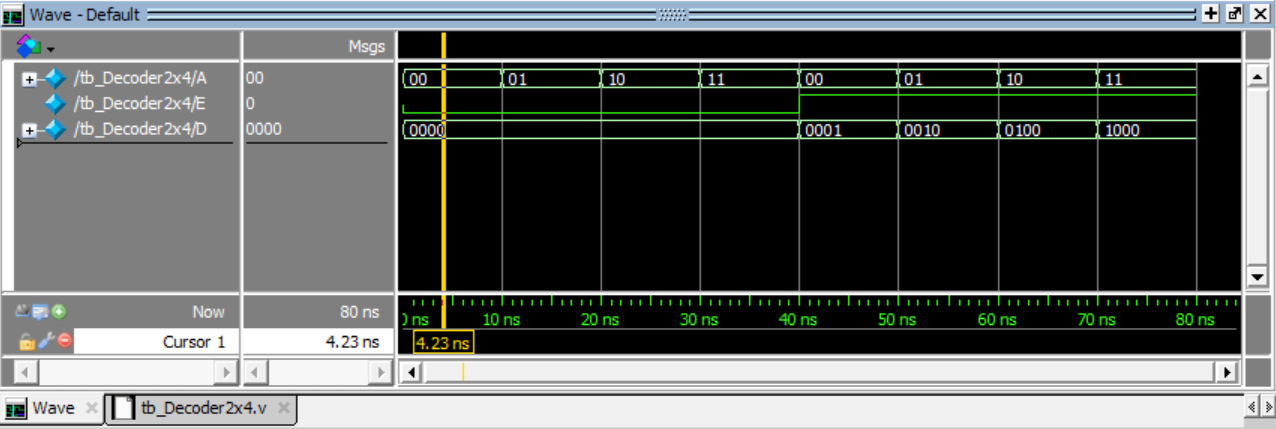
**Figure 1.1** – *Decoder2x4.v Analysis and Elaboration Test Results*



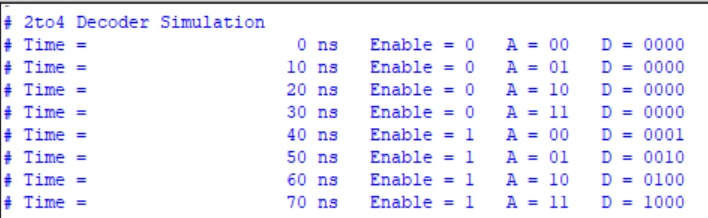
**Figure 1.2** – *2x4-Decoder RTL View Output*

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**Figure 1.3** – tb\_*Decoder2x4.v Script for Testing Module*

**

**Figure 1.4** – *2x4-Decoder RTL Simulation Output*

**

**Figure 1.5** – *2x4-Decoder Test Bench Monitor Output (Annotations to* ***Figure 1.4****)*

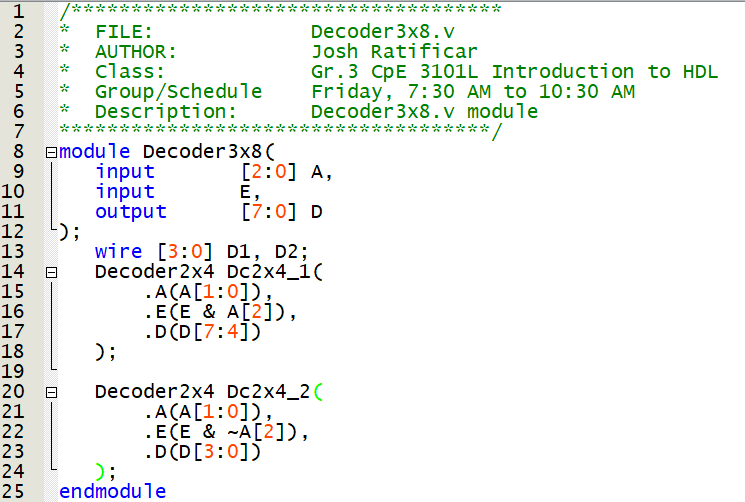
**Discussion of Results (Exercise 3A)**

From what we can observe, the circuit is operating how it is expected. This is apparent by observing **Figure 1.5’s** results in comparison to **Table 1.0’s** truth table. The “*$monitor*” command reflects the observable values in **Figure 1.4** and thus confirms that the test bench is appropriately designed. The output of this circuitry is dependent on the enabler. When the enabler is off, the output is 0.

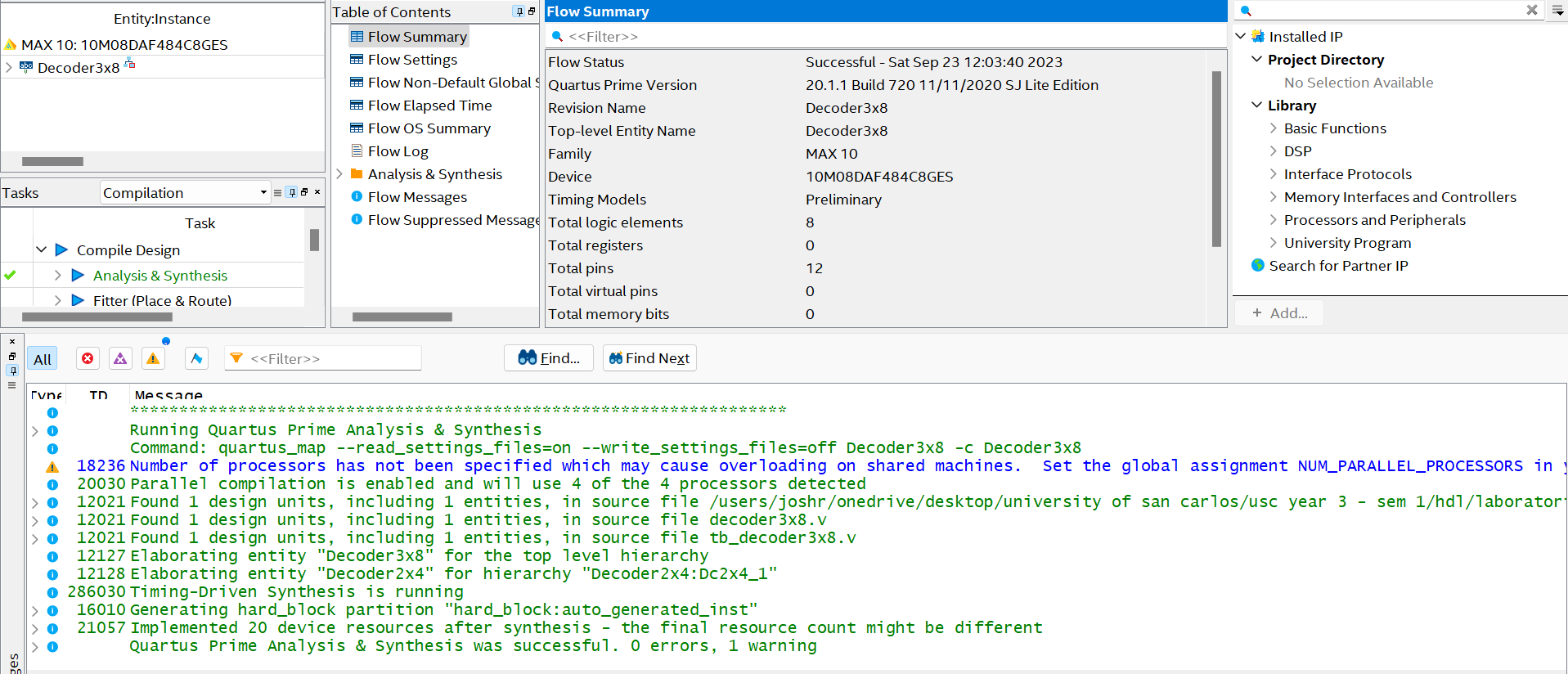
**Exercise 3B:**

**Table 2.0 –** *Truth Table for a 3x8 Decoder*

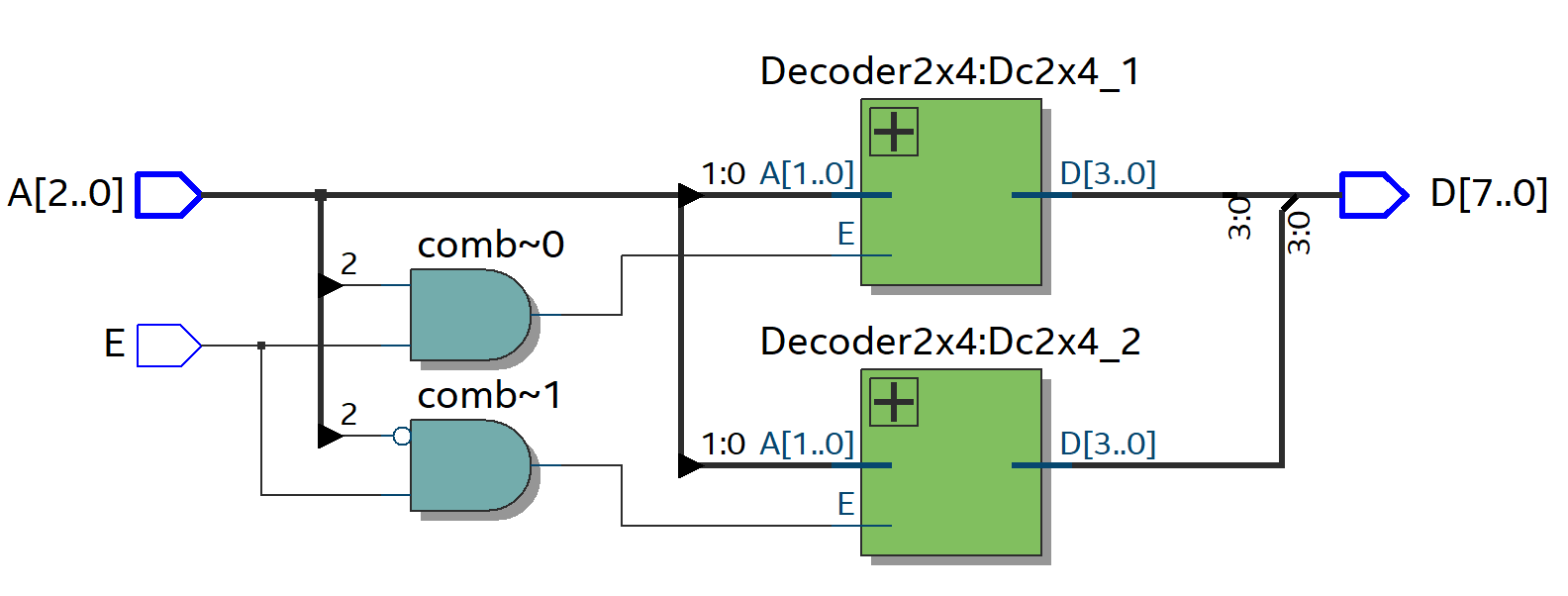
|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| INPUTS | | |  | OUTPUTS | | | |  |  |  |  |
| E | A0 | A1 | A2 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

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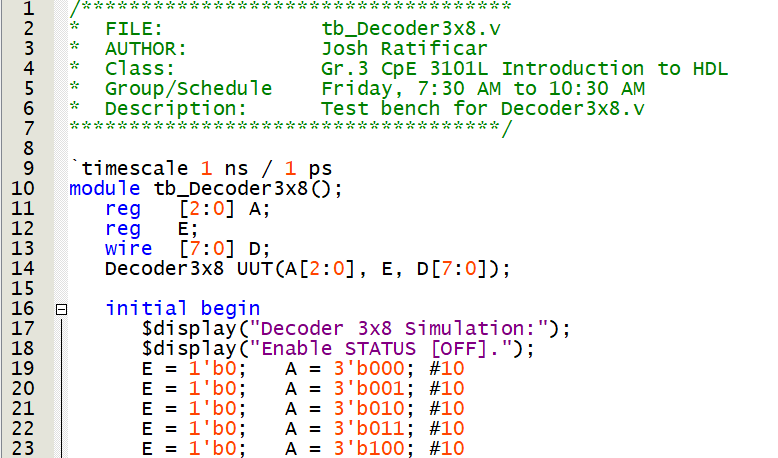
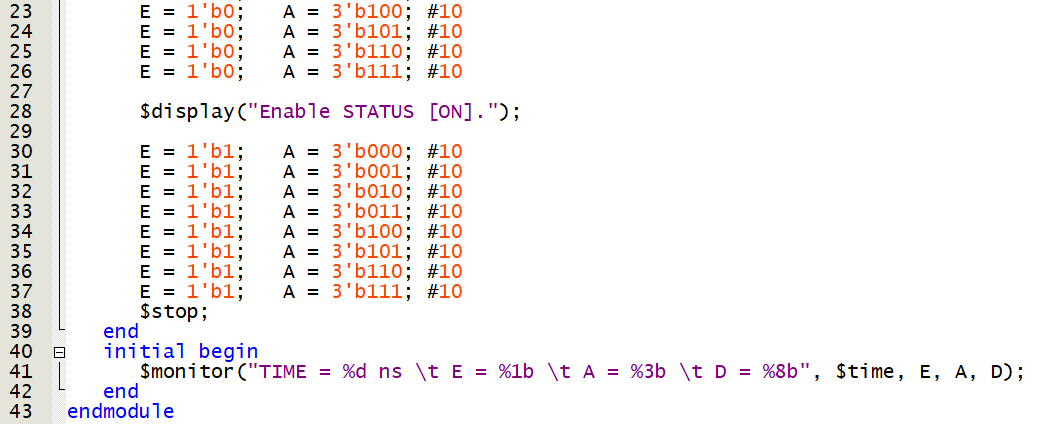
**Figure 2.0** – *Decoder3x8.v Script*

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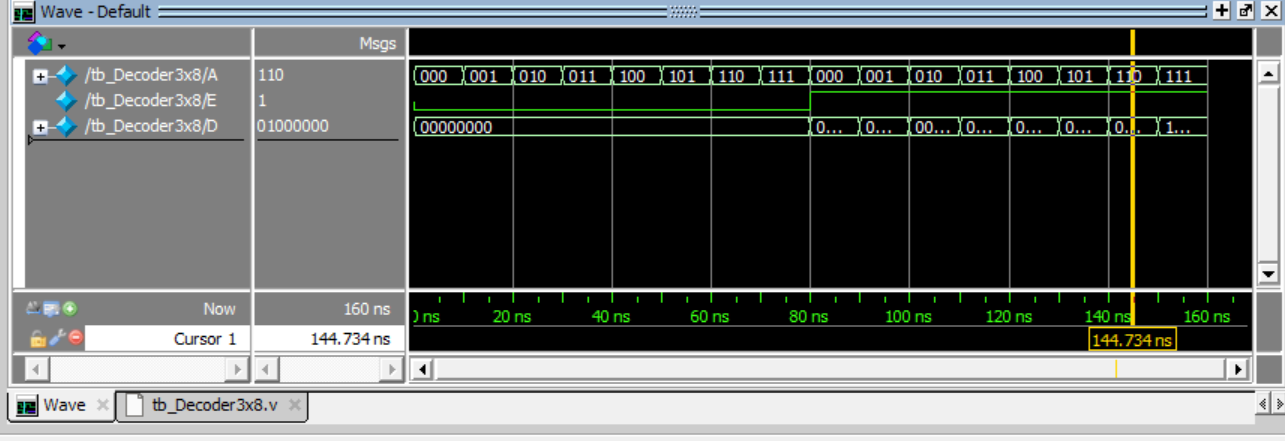
**Figure 2.1** – *Decoder3x8.v Analysis and Elaboration Test Results*

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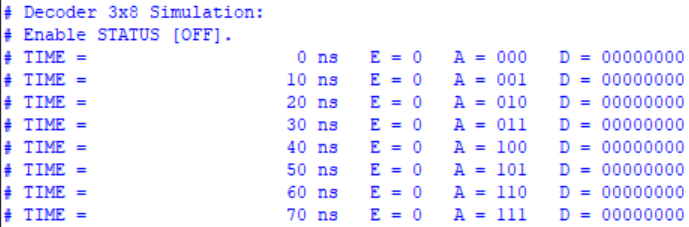
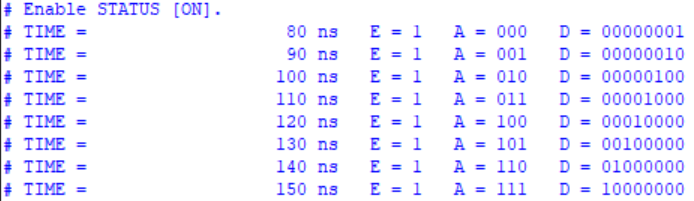
**Figure 2.2** – *3x8-Decoder RTL View Output*

**

**Figure 2.3** – tb\_*Decoder3x8.v Script for Testing Module*



**Figure 2.4** – *3x8-Decoder RTL Simulation Output*

**

**Figure 2.5** – *3x8-Decoder Test Bench Monitor Output (Annotations to* ***Figure 2.4****)*

**Discussion of Results (Exercise 3B)**

By modularizing, a 3x8 was created with the use of two 2x4-decoders. By creating a test bench (**Figure 2.3**), it was straight-forward verifying the results of the RTL simulation (**Figure 2.4**). As shown by the “*$monitor*” command, the results of **Figure 2.5** reflect the behaviour observed in the truth table (**Figure 1.0**). As observed, the output is dependent on the enabler being on, which is the desired outcome of the enabler.