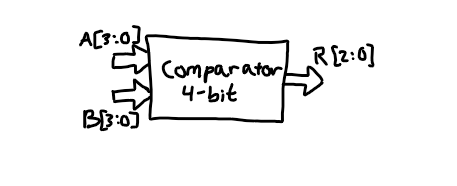
# Laboratory Report #4

**Name:** Josh Ratificar **Date Completed:** 10-02-2023

**Laboratory Exercise Title:** Dataflow Modeling of Combinational Circuits

**Block Diagrams:**



*Above includes the block diagrams for this Laboratory Exercise. Based on the diagrams, the following can be concluded:*

**4-Bit Comparator**

**8-Input Ports:**

* **A[0], A[1], A[2], A[3], B[0], B[1], B[2], B[3]**

**3-Output Ports:**

* **R[2], R[1], R[0]**

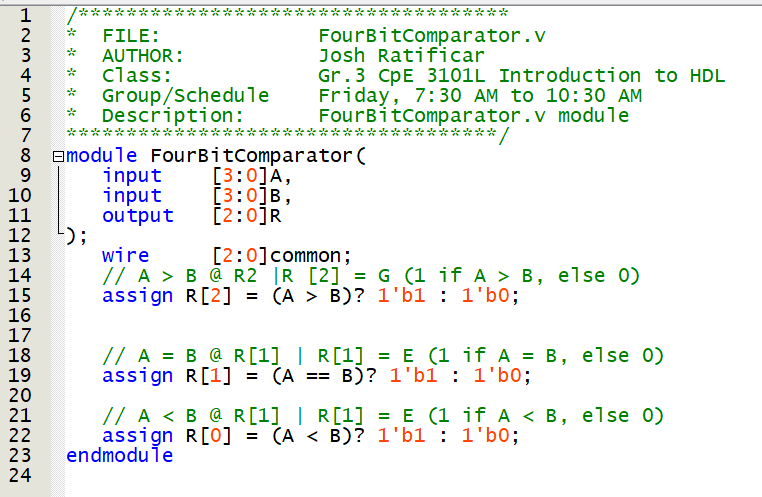
***NOTE***

**G (“greater than” is TRUE) |** R [2] = G (1 if A > B, else 0)

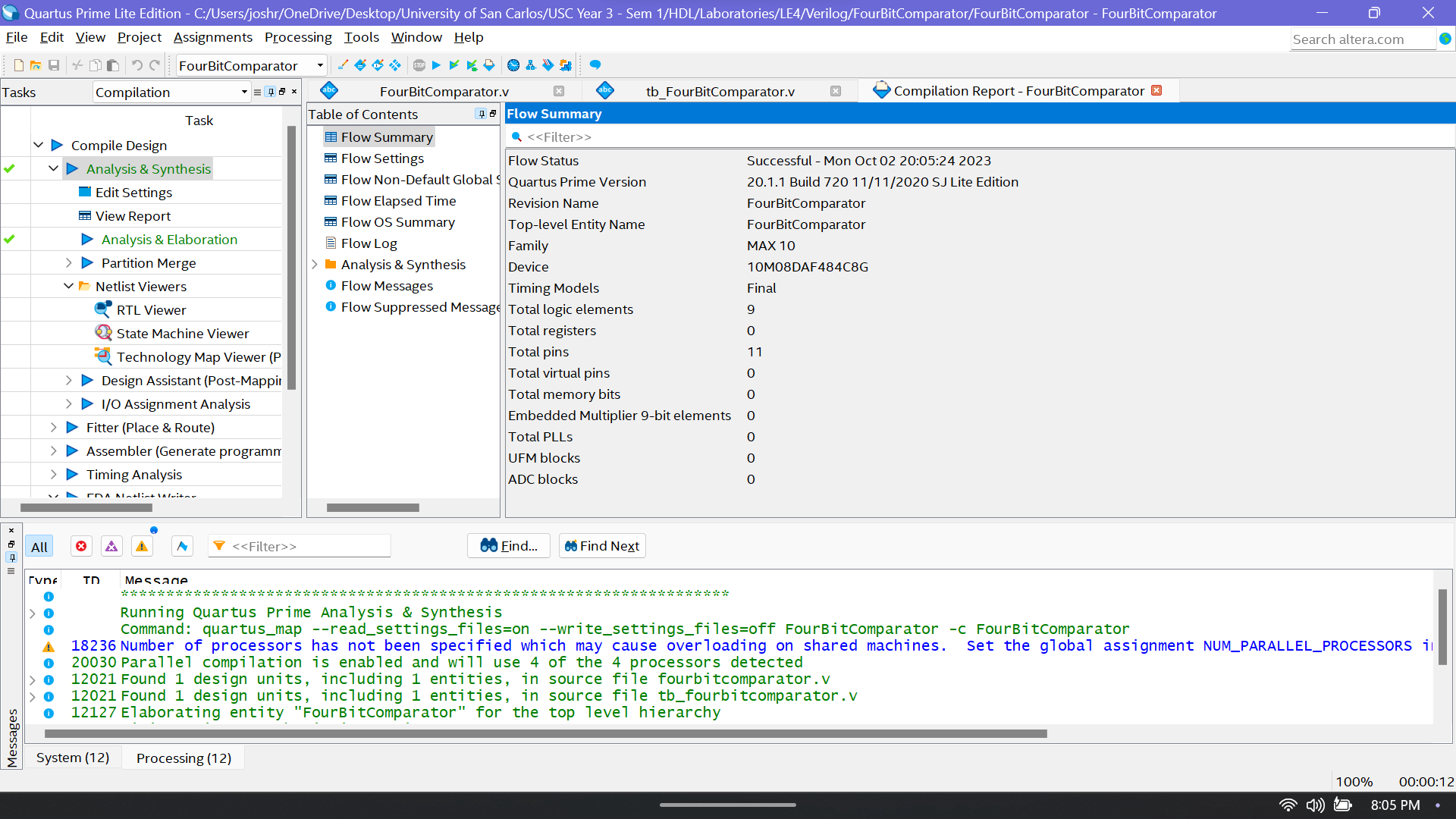
**E (“equal to” is TRUE) |** R [1] = E (1 if A = B, else 0)

**L (“less than” is TRUE) |** R [0] = L (1 if A < B, else 0)

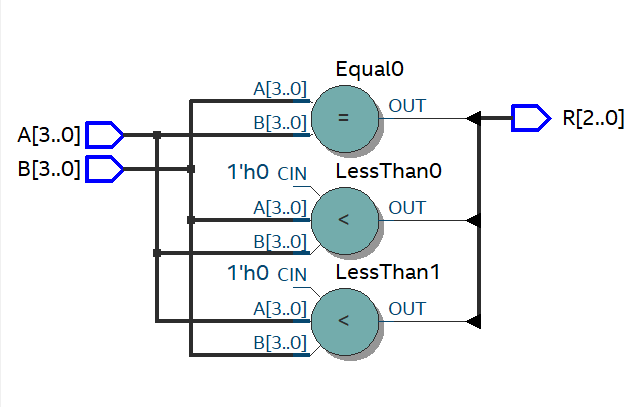
**Exercise 4A:**



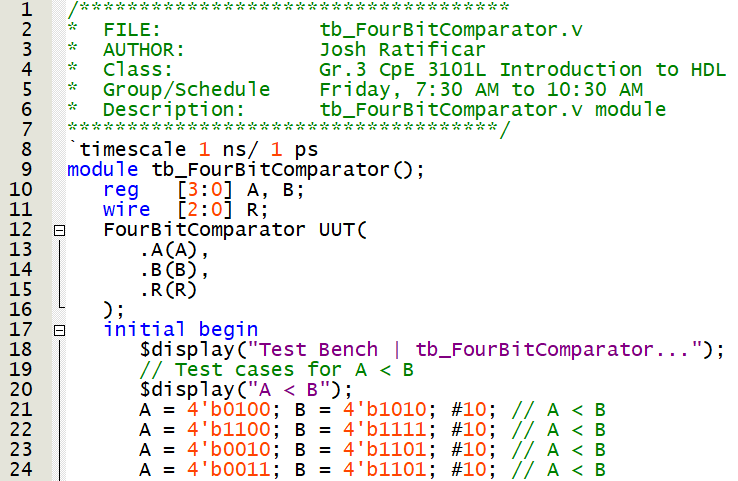
**Figure 1.0** – *FourBitComparator.v Script*

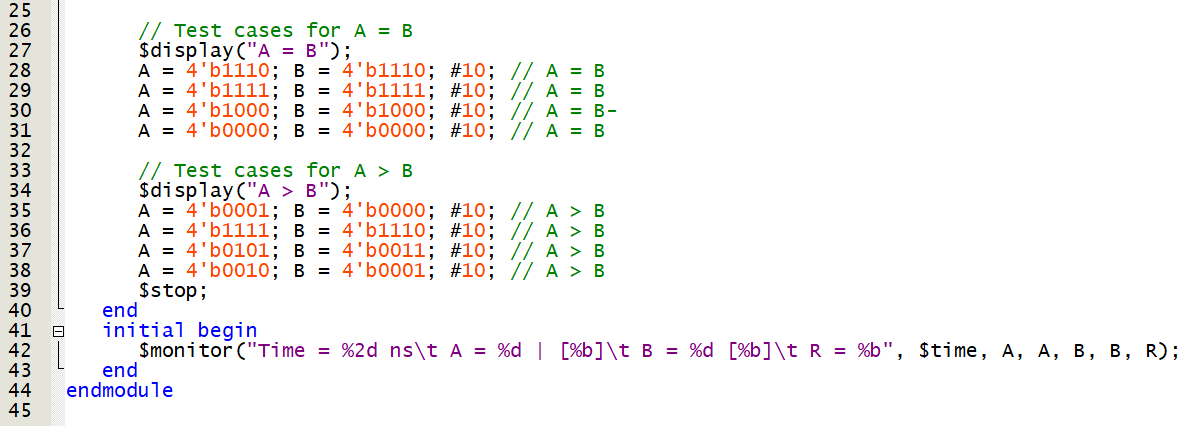
**

**Figure 1.1** – *FourBitComparator.v Analysis and Elaboration Test Results*

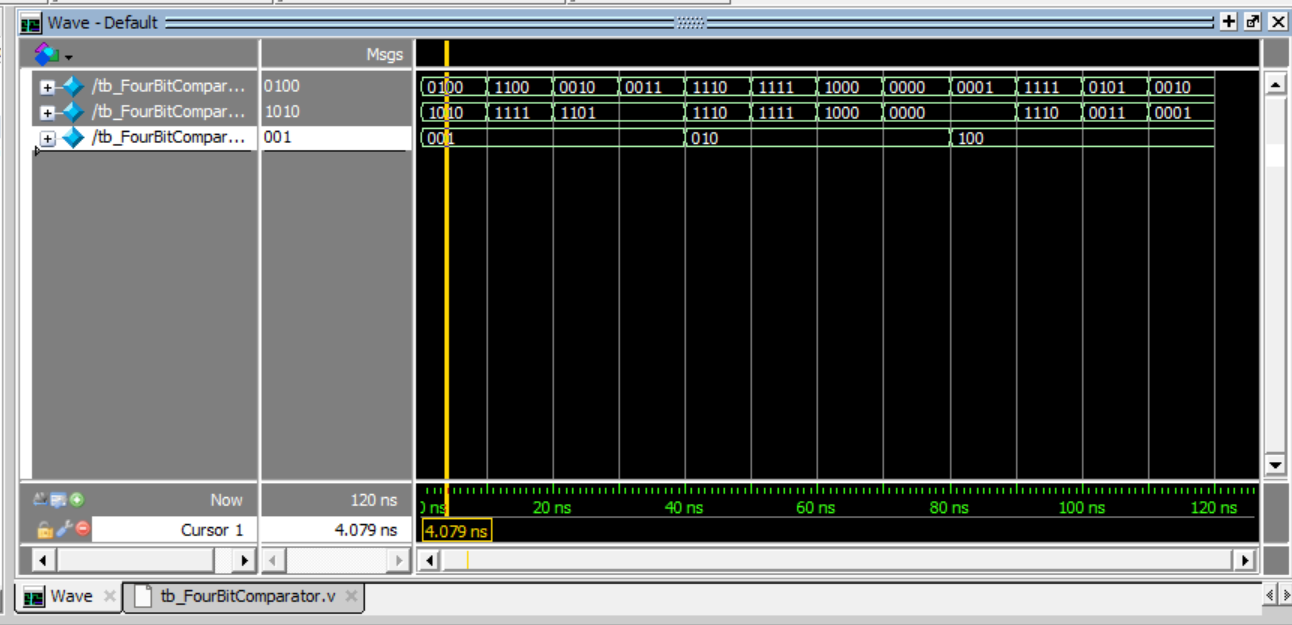


**Figure 1.2** – *FourBitComparator RTL View Output*

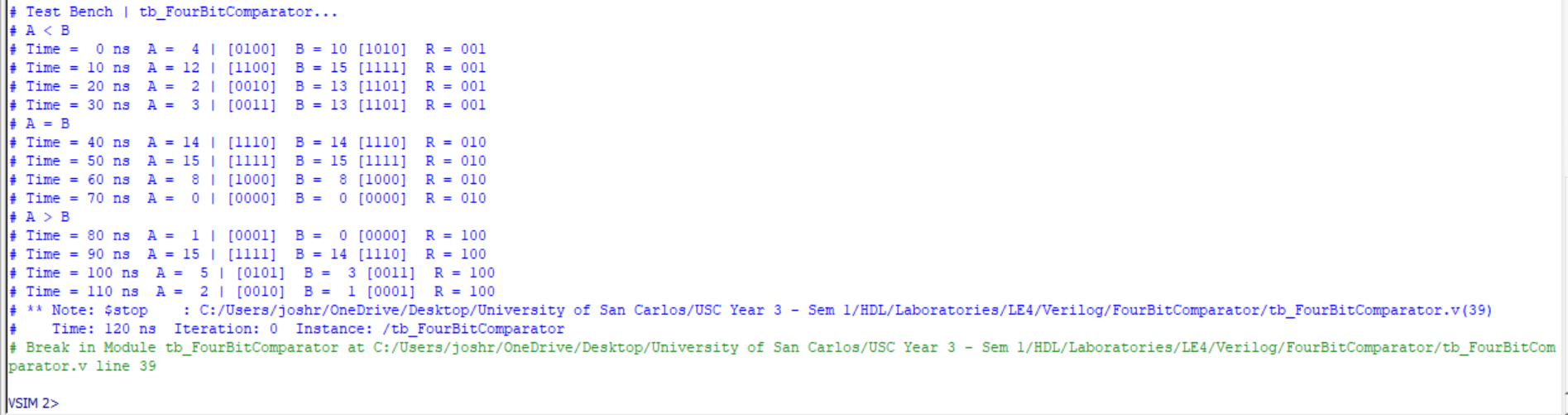




**Figure 1.3** – *tb\_* *FourBitComparator.v Script for Testing Module*

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**Figure 1.4** – *Four Bit Comparator RTL Simulation Output*

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**Figure 1.5** – *Four Bit Comparator Test Bench Monitor Output (Annotations to* ***Figure 1.4****)*

**Discussion of Results (Exercise 3A)**

By observing the Test bench script (**Figure 1.3**), we expect that the respective R bit reflect the comparison between two four-bit inputs. This is the best-case desired behaviour expected which after simulating through RTL simulation (**Figure 1.4**)**,** R appropriately and respectively changes every 40 ns. This is how the test bench was setup, and we can furthermore observe this behaviour in **Figure 1.5**. In conclusion, our design for our comparator works even when we applied Data Flow design in HDL Verilog.