

Course Name: Computer Organization and Architecture

Subject Code: TMC 102

Program Name: Master of Computer Applications (MCA)

1 Contact Hours: 45

L 3 T 0 P 0

2 Examination Duration (Hrs): **Theory** 0 3 **Practical** 0 0

3 Relative Weightage: **CWE:** 25 **MTE:** 25 **ETE:** 50

4 Credits: 0 3

5 Semester: ☐ * ☐ ☐
Autumn Spring Both

6 Pre-Requisite: Basic understanding of computers.

7 Subject Area: Computer Science

8 Objective: To familiarize students with the organization and architecture of a basic computer.

9 Course Outcome: After completion of course a student must be able to

CO 1 Understand the fundamental concepts of digital electronics, analyze and design the basic combinational and sequential circuits in lab using bread board.

CO 2 Exhibit a good understanding of the organization and architecture of a computer system. Cognize the working of central processing unit.

CO 3 Evaluate and describe the input output organization, various addressing modes and the concept of DMA.

CO 4 Appraise the various types of memories used in a computer system. Analyze the importance and functionality of cache and virtual memory organization.

CO 5 Describe and discuss the parallel processing concepts, benefits and structure of a multiprocessor system.

CO 6 Review the various aspects of computer organization and summarize the working principles of computer system

10 Details of the Course:

Unit No.	CONTENT	CONTACT HOURS
1	Introduction: Representation of Information and Basic Building Blocks: Introduction to Computer, Computer hardware generation, Number Systems, Character Codes (BCD, ASCII, EBCDIC), Logic gates, Boolean Algebra, K-map simplification, Combination circuits, Adders, Decoder, Encoders, Multiplexer, De-multiplexer, Sequential circuits,	7

	Flip-Flops, Registers, Counters (synchronous & asynchronous), IEEE standard for Floating point numbers. Division algorithm and Booth's multiplication algorithm.	
2	Basic Organization: Processor and its Components, ALU,CU and Special Purpose Registers, Von Neumann Machine (IAS Computer), Register Transfer Language, Bus and Memory Transfers, Common Bus System, Instruction Cycle Operational flow chart (Fetch, Decode), Organization of Central Processing Unit, Hardwired & micro programmed control unit, Single Organization, General Register Organization, Stack Organization, Addressing modes, Instruction formats, I/O Organization, Bus Architecture, Programming Registers	10
3	I/O Organization: Peripheral devices, I/O interface, Modes of Transfer, Priority Interrupt, Direct Memory Access (DMA), Input-Output Processor, Serial Communication. I/O Controllers, Asynchronous data transfer, Strobe Control, Handshaking.	10
4	Memory Organization: Memory Hierarchy, Main Memory (RAM/ROM chips), Auxiliary Memory, Magnetic Disk and its Performance, Magnetic Tape etc, Associative Memory, Cache Memory, Hit/Miss Ratio, Virtual Memory, Memory Management Hardware.	8
5	Parallel Processing Concepts: Introduction and Advantages, Pipeline & Vector Processing, Arithmetic Pipeline, Instruction Pipeline, RISC pipeline, Vector Processors. Multiprocessors: Characteristics, Interconnection Structures, Interprocessor Arbitration, Interprocessor communication and Synchronization, Cache Coherence.	10
	TOTAL	45

11 Suggested Books:

Sl. NO.	NAME OF AUTHERS/BOOKS/PUBLISHERS	YEAR OF PUBLICATION
1	Mano,M.M,"ComputerSyatem Architecture",3rd Ed., Pearson Education.	2017
2	Jain R. P. "Digital Electronics"4th Ed. Tata McGraw-Hill.	2009
3	Stallings W."Computer organization",10 th Ed. Prentice-Hall.	2016
4	John P.Hayes. "Computer organization",3 rd Tata McGraw-Hill.	2017
5	Vravice, Zaky & Hamacher, Computer Organization", 5 th Ed. McGraw-Hill.	2011