MODULE 2

Module – 2 FET and SCR

SYLLABUS

1. Introduction, JFET:
i.Construction and operation,
ii.JFET Drain Characteristics and Parameters,
iii.JFET Transfer Characteristic,
iv.Square law expression - I_D,
v.Input resistance, (7.1, 7.2, 7.4, 7.5 of Text 2),

2. MOSFET:
i.Depletion & Enhancement - MOSFET-Construction,
ii.Operation,
iii.Characteristics and Symbols, CMOS (4.5 of Text l)

3. Silicon Controlled Rectifier (SCR):
i.Two-transistor model, Switching action,
ii.Characteristics,
iii. Phase control application (3.4 - 3 .4.5 of Text 1).

TEXTBOOKS

1. *"Basic Electronics", D.P. Kothari, I. J. Nagrath, MHE (India) Private Limited, 2014.*
2. *"Electronic Devices", Thomas L Floyd, Pearson Education, 9th edition 2012*

NOTES

A transistor is a semiconductor device that controls an electrical parameter - current or voltage by application of a small electrical signal. Transistors may be: bipolar or field-effect. FETs are unipolar devices - the main current through them is comprised either of electrons through an N-type semiconductor (N-channel FET) or holes through a P-type semiconductor (P-channel FET).

JFET (Junction Field-Effect Transistor)

JFET(junction field-effect transistor) is a type of FET that operates with a reverse-biased ***pn*** junction to control current in a channel.

It is a voltage controlled three terminal uni-polar semiconductor device with terminals - Source (S), Gate (G) and Drain (D).

The voltage applied to the Gate with respect to the Source (V_{GS}), controls the current flowing between the Drain and the Source terminals

Depending on their structure, JFETs can be classified into N-Channel and P-Channel JFET

Structure and operation of N-Channel JFET

1. Wire leads are connected to each end of the n-channel forms the drain and source terminals; the **drain** is at the upper end, and the **source** is at the lower end.
2. Two p-type regions are diffused in the n-type material to form a **channel,** and both p-type regions are connected to form the **gate** terminal.
3. The source and the drain terminals are of n-type while the gate is of p-type. Due to this, two pn junctions will be formed within the device.

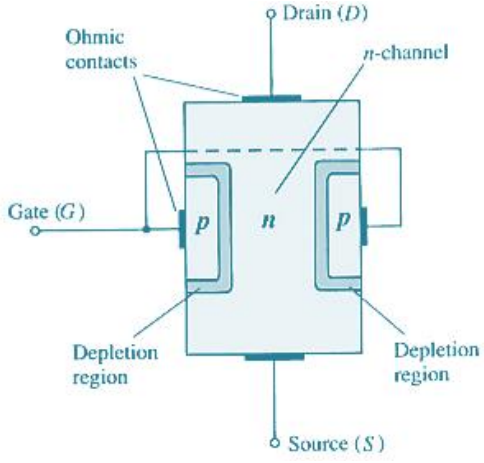


Fig.2.1: N-channel JFET

Operation of n-channel JFET

In n-channel JFET, the **majority charge carriers are electrons** as the channel formed in-between the source and the drain is of n-type.

The JFET is always operated with the gate-source pn junction reverse-biased.

To understand it better consider 3 cases.

Case I: V_{GS} = 0 and V_{DS} = 0

1. No voltage applied to the device i.e. $V_{GS} = 0$ | $V_{DS} = 0$, the device DOES NOT CONDUCT hence. **$I_{DS} = 0$.**

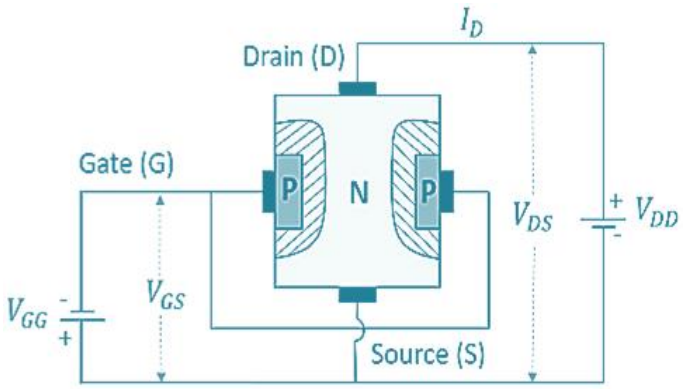


Fig.2.2: n-channel JFET with V_{GS} = 0 and V_{DS} = 0

Case II: V_{GS} = 0 and V_{DS} = +ve

1. Electrons within ***n*** region start moving towards the drain as electrons are attracted by the positive V_{DS}, this results in a current flow from drain to source whose value is restricted by the resistance offered to it by the channel.
2. The voltage drop gets progressively higher through the length of the channel. The reverse biasing effect is stronger at drain terminal than at the source terminal. Therefore the depletion layer tends to be wider at point A than at point B as shown in figure. The size of the depletion layers determines the width of the channel and hence, conduction of I_{DS}.

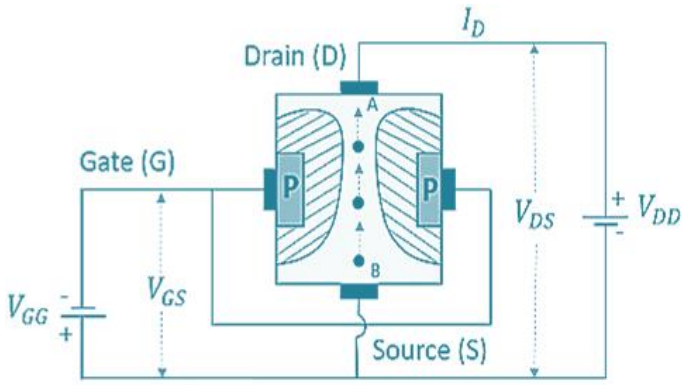
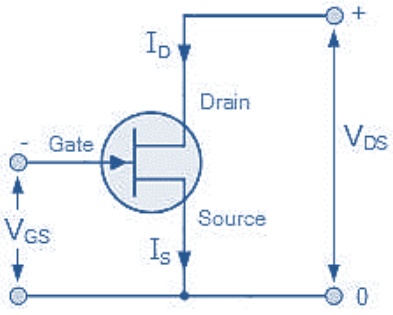
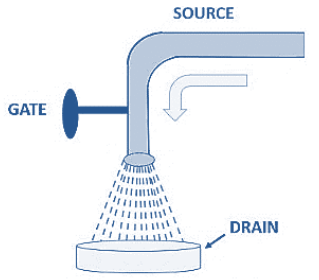


Fig.2.3: n-channel JFET when V_{GS} = 0V and V_{DS} = +ve





Water Analogy for Understanding FET

3. When V_{DS} is further increased, a stage occurs where both the depletion layers touch each other, and prevent the current I_D flow as shown in Fig.2.4
4. The $\mathbf{V_{DS}}$ voltage at which both these depletion layers literally "touch" is called as "**Pinch off voltage**". It is indicated as $\boldsymbol{V_P}$.
5. The drain current I_D is observed to be a function of reverse bias voltage at gate.

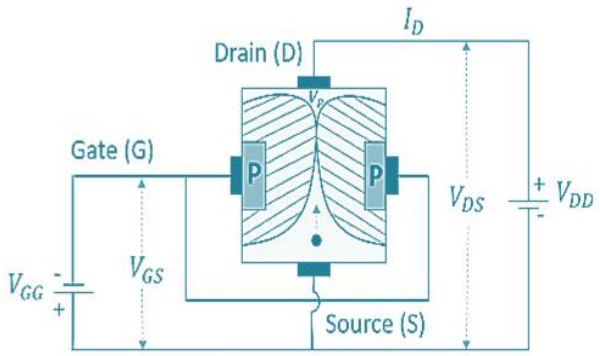


Fig.2.4: n-channel JFET when V_{GS} = 0V and V_{DS} = VP

Case III: V_{GS} = -ve and V_{DS} = +ve

1. Behaviour is similar to Case II, but for a lower value of V_{DS} . Hence the pinch-off and the saturation occur earlier

Drain characteristics

1. As V_{DS} is increased, current flow I_D increases linearly up to a certain point A, known as Knee Voltage.
2. The gate terminals are in reverse biased condition and as I_D increases, the depletion regions tend to constrict. The pinch off voltage is defined as the **minimum drain to source voltage where the drain current approaches a constant value saturation value.** The point at which this pinch off voltage occurs is called as Pinch off point, denoted as B.
3. In the Ohmic region with V_{GS}=0 the JFET acts like a voltage controlled resistor.
4. As V_{DS} is further increased, the channel resistance also increases in such a way that I_D practically remains constant. The region BC is known as saturation region or amplifier region. All these along with the points A, B and C are plotted in the graph below.

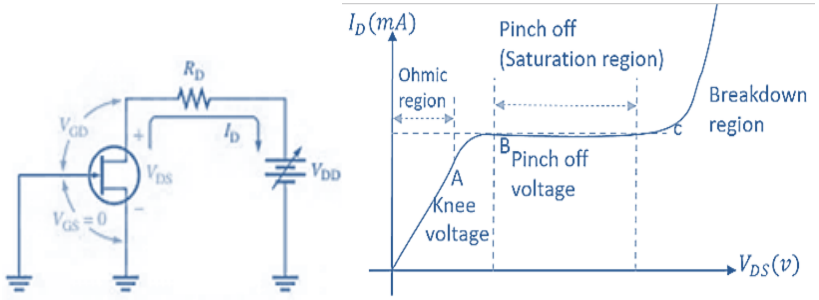


Fig.2.5 a: Drain characteristics of n-channel JFET

The drain characteristics - **I_D** against **V_{DS}** for different values of gate source voltage V_{GS}.

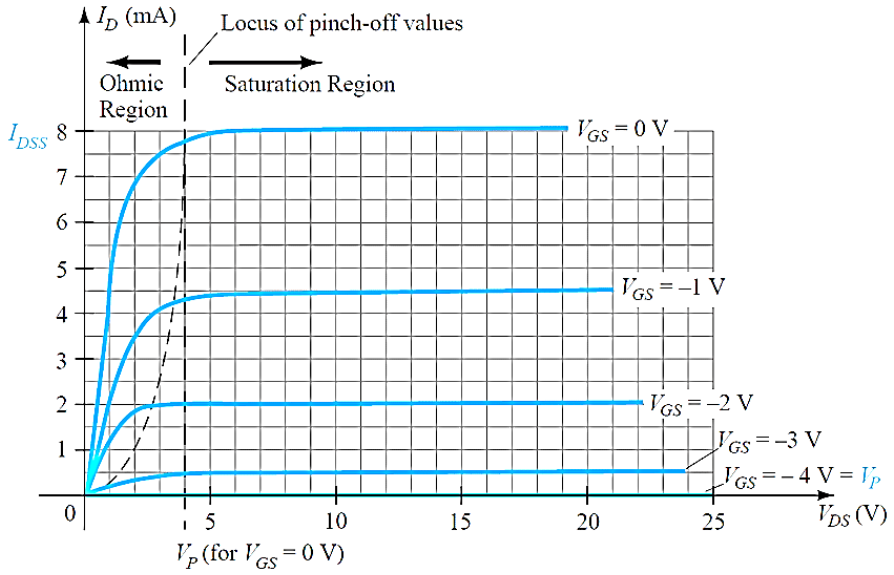


Fig.2.5: Drain characteristics of n-channel JFET

Transfer Characteristics

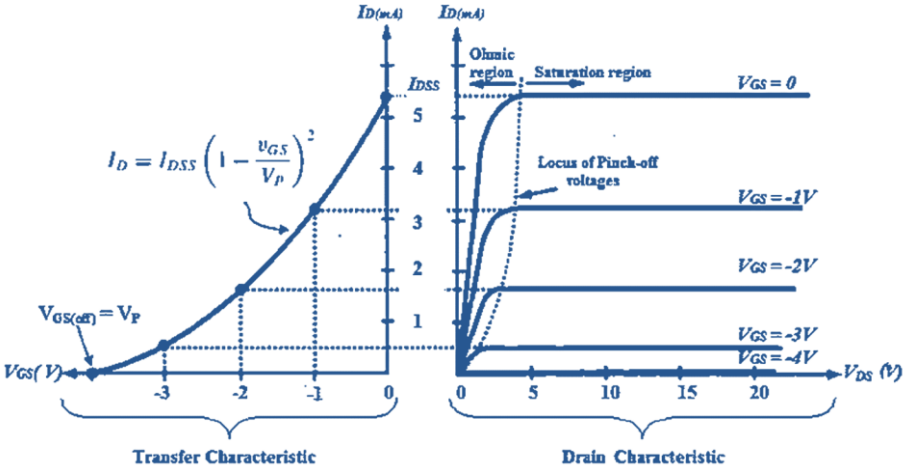


Fig.2.6: Transfer characteristics of n-channel JFET

Observations

I_{DS} is zero when $V_{GS} = V_P$. For normal operation, V_{GS} is biased to be somewhere between V_P and 0. We can calculate the Drain current, I_D for any given bias point in the saturation or active region as follows: I_D lies between (pinch-off) zero to I_{DSS}. From the Transfer Characteristics We have the square law or Shockley's equation: :

$$I_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2$$

Similarly, if we know V_{DS} and I_D we can calculate the Drain-Source channel resistance.

$$R_{DS} = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1}{g_m} \qquad \mu = \frac{\text{change in } V_{DS}}{\text{change in } V_{GS}} \text{ at } I_D \text{ constant}$$

gm is transconductance and Amplification factor Mu is simplified by substitution

$$\mu = \left(\frac{\Delta V_{DS}}{\Delta I_D}\right) * \left(\frac{\Delta I_D}{\Delta V_{GS}}\right) = \frac{\Delta V_{DS}}{\Delta V_{GS}} = R_{DS} * g_m$$

$$\mu = R_{DS} * g_m$$

1. An n-channel JFET has an I_{DSS} = 8mA, V_P = -4V. Determine I_D for V_{GS} = -1V and V_{GS} = -2V

The current in JFET is given by $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

On substituting the values At V_{GS} = -1V $I_D = 8\left(1 - \frac{-1}{-4}\right)^2 = 4.5\text{mA}$

At V_{GS} = -2V $I_D = 8\left(1 - \frac{-2}{-4}\right)^2 = 2\text{mA}$

2 The device parameters for an n-Channel JFET are: Maximum current I_{DSS} = 10mA, Pinch off voltage, V_p = - 4V. Calculate the drain current for (a) V_{GS} = 0, (b) V_{GS} = - 1.0V and (c) V_{GS} = - 4V

Solution: The expression for drain current I_D,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

(a) When VGS = 0, from Eq(1), $I_D = I_{DSS} = 10\text{mA}$

(b) When V_{GS} = -1.0V, the drain current from Eq is,

$$= 10x10^{-3}\left(1 - \frac{(-1)}{(-4)}\right)^2$$

(c) When V_{GS} = -4V = V_p, then from Eq $I_D = 0$

3 A JFET produces gate current of 2nA when gate is reverse biased with 8V. Determine the resistance between gate and source.

Solution: Since reverse gate-source voltage, V_{GS}, of 8v produces gate current, I_G of 2nA,
Therefore, gate-to-source resistance, R_{GS}, is

$$R_{GS} = \frac{V_{GS}}{I_D} = \frac{8}{2x10^{-9}} = \mathbf{4000M\Omega}$$

4 The reverse gate voltage of JFET when changes from 4.4V to 4.2V, the drain current changes from 2.2 mA to 2.6 mA. Find out the value of transconductance of the transistor.

Solution: The transconductance, g_m is defined as

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

In the given problem,

$\Delta_{ID} = (2.6 - 2.2)\text{ mA} = 0.4\text{ mA}$

$\Delta V_{GS} = (4.4 - 4.2)\text{ V} = 0.2\text{ V}$

$$\therefore g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{0.4x10^{-3}}{0.2} = \mathbf{2m\ mho}$$

5 Find out the operating point current and voltage values (I_{DQ} and V_{DSQ}) for a self biased JFET having the supply voltage V_{DD} = 20V and maximum value of drain current as 12 mA.

Solution: Value of drain current at Q-point may be taken as half of the maximum current, that is
In the same way, the value of drain-source voltage at Q-point may be taken as half of

$$I_{DQ} = \frac{I_{DSS}}{} = \frac{12x10^{-3}}{} = 6\ mA$$

$$V_{DSQ} = \frac{V_{DD}}{2} = \frac{20}{2} = 10V$$

supply voltage V_{DD}. That is,
Therefore, I_{DQ} = 6 mA and V_{DSQ} = 10V.

6 Calculate the value of source resistance RS required to self bias a n-JFET such that V_{GSQ} = - 3V. The n-JFET has maximum drain-source current I_{DSS} = 12 mA, and pinch-off voltage, Vp = - 6V.

Solution: Given, I_{DSS} = 12 mA, VGS = -3V and Vp = -6V, The drain current, ID, in a JFET, in the saturation region is,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = 12mA\left[1 - \left(\frac{-3}{-6}\right)\right]^2$$

$$R_S = \left|\frac{V_{GS}}{I_D}\right| = \frac{3V}{9mA} \simeq 333\Omega$$

Summary :

1. A JFET is a three-terminal voltage-controlled semiconductor device.
2. It is operated with gate-source PN junction reverse biased.
3. JFET must be operated between V_{GS} and $V_{GS\ (off)}$. For this range of Gate-to-Source voltages, I_D will vary from a maximum of I_{DSS} to a minimum of almost zero.
4. The drain current I_D is controlled by changing the channel width.
5. Applications of JFET constant current source, buffer amplifier, electronic switch, phase shift oscillator, voltage variable resistor (VVR) and chopper.

MOSFET

The MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is a semiconductor transistor widely used for switching and amplifying electronic signals in the electronic devices.

1. The MOSFET is a four terminal device with source (S), gate (G), drain (D) and body (B) terminals. The body of the MOSFET is frequently connected to the source terminal so making it a three terminal device like field effect transistor.
2. The MOSFET is very far the most common transistor and can be used in both analog and digital circuits.
3. The MOSFET can function in two ways

i. Depletion Mode: When there is no voltage on the gate, the channel shows its maximum conductance.

ii. Enhancement Mode: When there is no voltage on the gate the device does not conduct

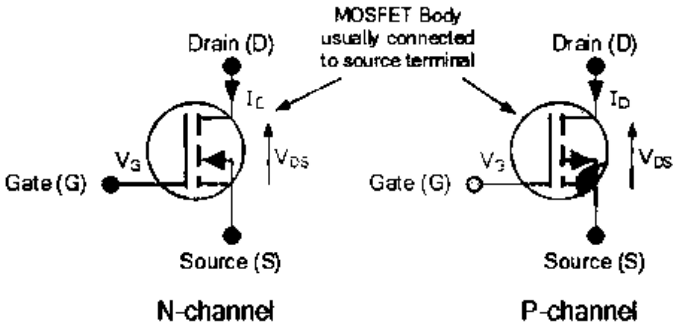


Fig. 2.7 MOSFET Symbol

Depletion-mode MOSFET

The **Depletion-mode MOSFET**, (less common than the enhancement mode types) is normally **switched "ON"** (conducting) with V_{GS}=0**.** That is the channel conducts without the application of V_{GS} making it a "normally-closed" device.

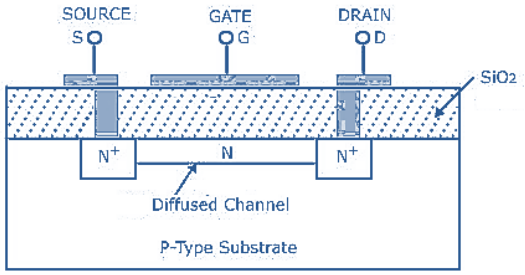


Fig.2.8 (a) Structure of depletion nMOS

Depletion nMOS transistor

Case 1 V_{GS}=0

When there is no Gate voltage V_{GS}=0 Max current I_D=I_{DSS} flows

Case 2 V_{GS}-ve

1. -V_{GS} will deplete the conductive channel of its free electrons switching the transistor "OFF".
2. This creates a depletion region in the channel, as illustrated in 2.9 (b) The more negative the gate, the less the Drain current.
3. When a -ve voltage is applied to the gate terminal the electrons gets repelled towards the substrate there will be a reduction in the drain current.
4. At a particular negative voltage the drain current becomes zero. This voltage is called as **pinch off voltage.**

Case 3 V_{GS} +ve

1. For an n-channel depletion mode MOSFET: +V_{GS} means more electrons and more current. While a -V_{GS} means less electrons and less current.
2. When a positive voltage is applied to the gate more electrons is attracted into the channel. On

applying more positive V_{DS} more current to flows from the drain to source.

3. The more positive the Gate is made, the more Drain current flows. In this mode of operation the device is referred to as a enhancement-mode MOSFET.

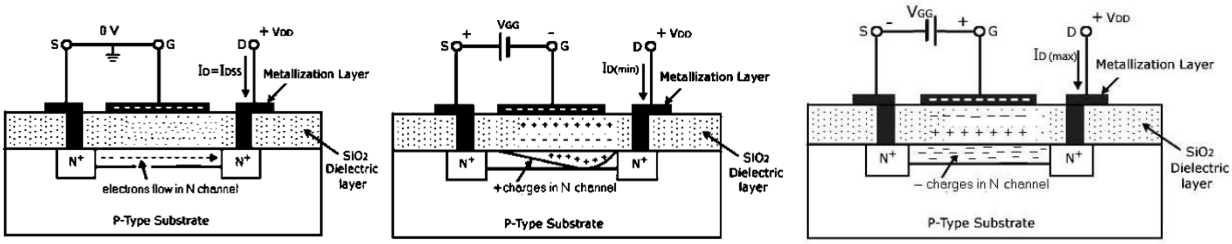


Fig.2.9(a) MOSFET in depletion mode with gate voltage =0; (b) -ve (c) +ve

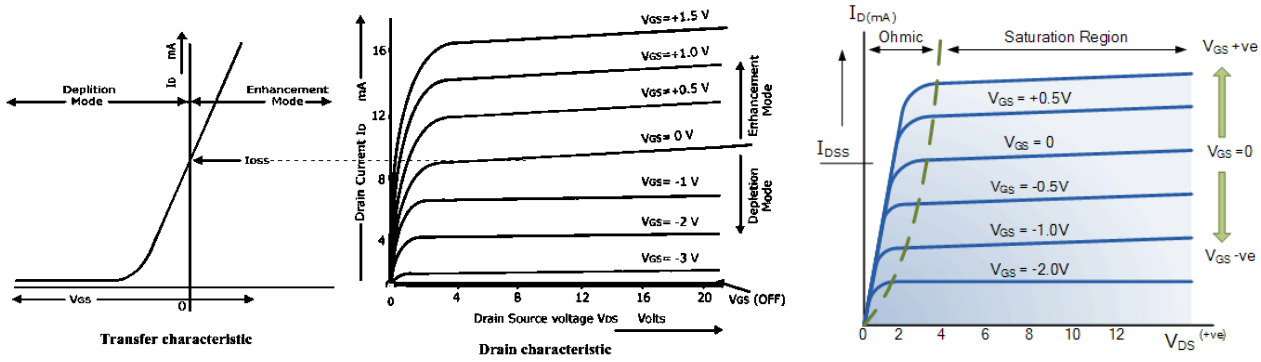


Fig.2.10 $I_d - V_{ds}$ characteristics of depletion nMOS with regions of operations

For Depletion type MOSFET, I_D = 10mA at V_{GS} = -1V. Determine V_P if I_{DSS} = 15mA

The current in DMOSFET is given by $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

On substituting the values $10m = 15m\left(1 + \frac{1}{V_P}\right)^2$

$$\mathbf{V_P = -5.5V}$$

Structure and operation of NMOS enhancement transistor

1. nMOS enhancement transistor in the fig.2.11 consists of lightly doped p-substrate. Two highly doped n-type regions are formed in the p-substrate by diffusing n-impurities. These regions forms the source and drain terminal of the transistor.

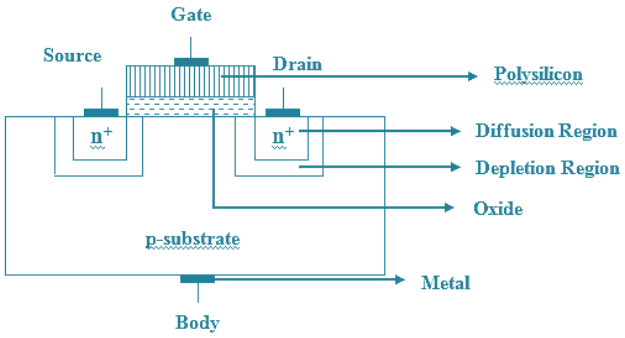


Fig.2.11 (a): Structure of nMOS enhancement transistor

2. A thin layer of silicon dioxide (SiO_2) is grown on the surface of the substrate which acts as an excellent insulator.
3. A polysilicon gate deposited above the substrate is separated from the substrate by an oxide layer.
4. Metal contacts are made for gate (G), source (S), drain (D) and substrate (B) regions.
5. Substrate (also known as body) region forms pn junctions with source and drain region and these pn junctions are reverse biased.

Operation of NMOS enhancement transistor

The construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of an N-channel between the drain and source terminals.

Minimum value of V_{GS} needed to form the induced N-channel, that turns the E-MOSFET ON is called threshold voltage $V_{GS\ (th)}$. For V_{GS} below $V_{GS\ (th)}$, the drain current $I_D = 0$.

Case (i) When $V_{GS} = 0$ V, V_{DS} = +ve :

There is no channel induced between Source and Drain. The p- substrate has minority carriers hence the drain current is almost zero.

Case (ii) When $V_{GS} = V_{GS(th)}$ = + ve, and V_{DS} = + ve:

1. Free electrons developed next to the SiO_2 layer and induced an N channel.
2. A Drain current I_D starts flowing. E-MOSFET is turned ON.
3. Beyond $V_{GS\ (th)}$, if V_{GS} is increased, the induced N channel becomes wider, resulting large I_D.
4. If the value of V_{GS} decreases not less than $V_{GS\ (th)}$, the channel becomes narrower and I_D will decrease.

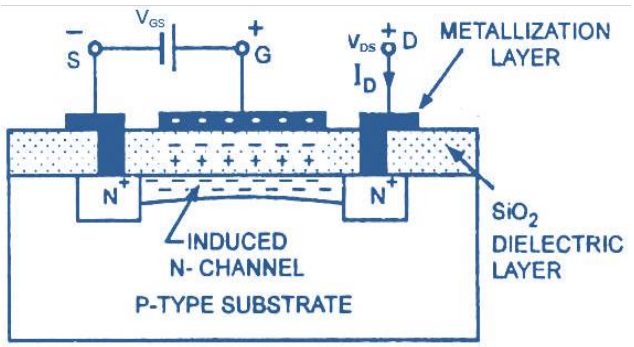


Fig. 2.11 (b)MOSFET in enhancement mode with gate voltage positive

Since the conductivity of the channel is enhanced by the positive bias on the Gate, so this device is also called the enhancement MOSFET or E- MOSFET.

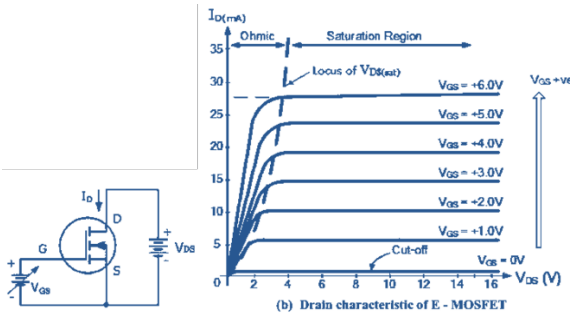
Drain Characteristic Curves

The vertical components of the curves correspond to the ohmic region, and horizontal components - to the saturation region (constant current).

Note the following worthy points:

I_D depends on different values of V_{GS} (from 0V to + $V_{GS\,(max)}$).

When V_{GS} = 0, even for large increase in $V_{DS,}$ I_D = 0. This is said to be cut-off region. (MOSFET off state).



(b) Drain characteristic of E - MOSFET

Transfer Characteristics

Case 1 When $V_{GS} < V_{GS(th)}$, then I_D =0. ;

This is because under this state, the channel will not be connecting between the drain and the source terminals. This is called as cut-off region. (MOSFET off state). The tranfer curves of MOSFET is shown in the fig.2.13.

Case ii) When $V_{GS} > V_{GS(th)}$,. then I_D flows through the device, initially (Ohmic region) and then saturates to a value (saturation region). That means, I_D is controlled by the Gate voltage, $V_{GS.}$

Case iii) I_D can be obtained by analytical expression:

$$I_D = k\,(V_{GS} \quad V_{GS(th)})^2 \quad \text{where} \quad k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2} \qquad A/V^2$$

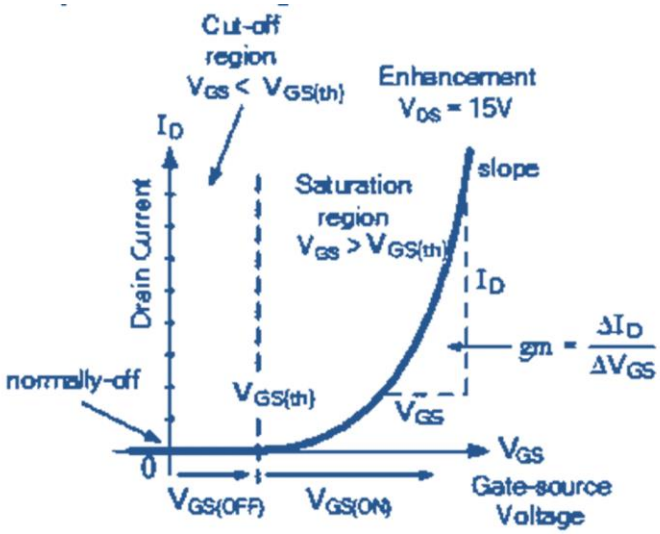


Fig.2.13 Transfer characteristic of E - MOSFET

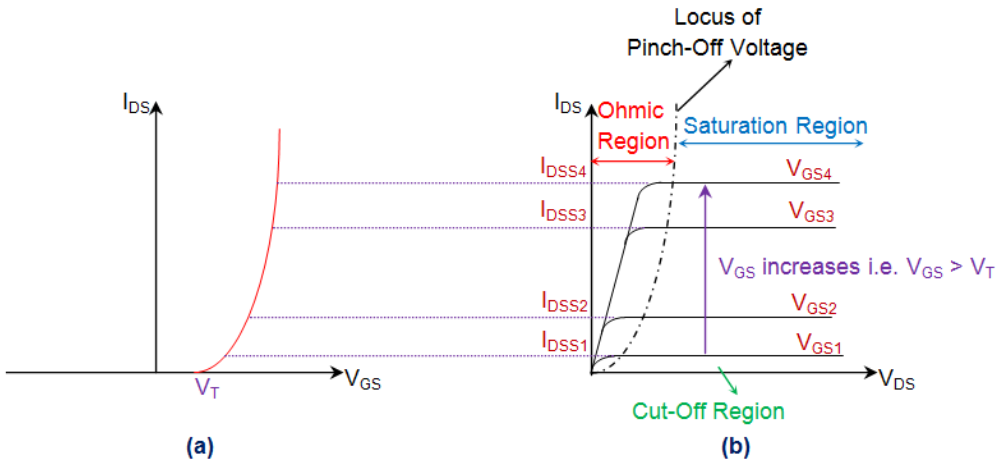


Fig.2.14: I_d - V_{ds} characteristics of nMOS with regions of operations

Symbol of enhancement nMOS transistor

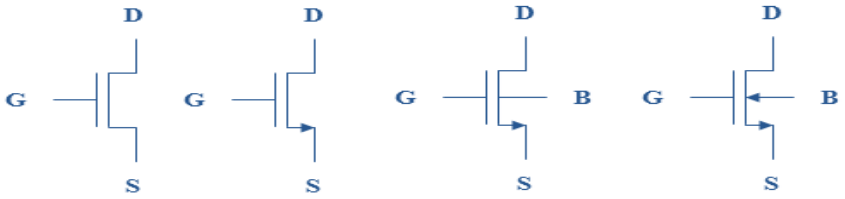


Fig.2.15: Symbol of nMOS transistor

Symbol of enhancement pMOS transistor

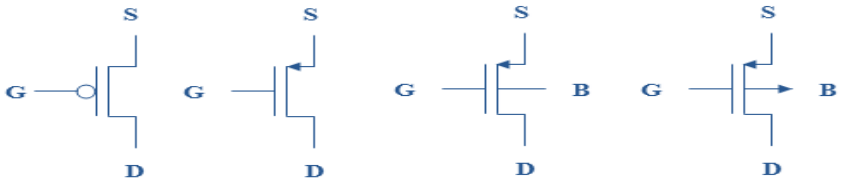


Fig.2.16: Symbol of pMOS transistor

1. For Enhancement type MOSFET (E-MOSFET), determine value of I_D, if $I_{D(ON)}$ = 4mA, $V_{GS(ON)}$ = 6V, V_T = 4V and V_{GS} = 8V.

The current in EMOSFET is given by $\mathbf{I_D = k(V_{GS} - V_T)^2}$

where constant k is given by $k = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2} = \frac{4*10^{-3}}{(6-4)^2} = 1 * 10^{-3} A/V^2$

$\therefore \quad I_D = 1 * 10^{-3}(8-4)^2$

$\mathbf{I_D = 16mA}$

CMOS circuits

1. A CMOS (Complementary MOSFET) inverter (NOT gate) contains a PMOS and a NMOS transistor.
2. In NMOS, majority carriers are electrons. When a high voltage is applied to the gate, the NMOS will conduct. When a low voltage is applied to the gate, NMOS will not conduct.
3. In PMOS the majority carriers are holes. When a high voltage is applied to the gate, the PMOS will not conduct. When a low voltage is applied to the gate, the PMOS conducts.

4. Fig.2.17(a) and (b) illustrate the basic operation of CMOS inverter and it can be studied by using simple switch models. NMOS source (S) is grounded. PMOS source (S) is connected to V (= +5V)

   PMOS and NMOS gates (G) are shorted and taken as input (V).

   PMOS and NMOS drain (D) are shorted and taken as output (V

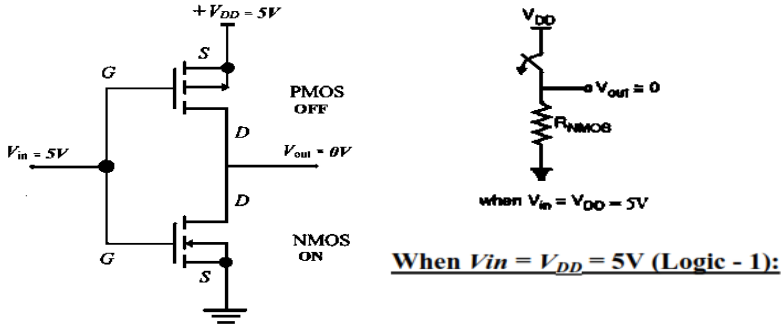


Fig.2.17(a) Circuit for input logic 1

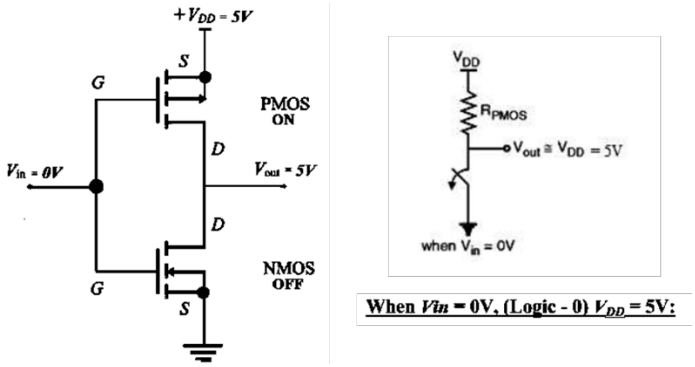


Fig.2.17 (b) Circuit for input logic 0

5. As the voltage at the input of the CMOS device varies between 0 and 5 volts, the state of the NMOS and PMOS varies accordingly.

When V_{IN} = 0 (low or 0V)	**When V_{IN} = 1 (high or 5V)**
for nMOS, V_{GS}=0V, hence nMOS is in off state.	for nMOS, V_{GS} = 5V, hence nMOS is in on state.
for pMOS, V_{GS} = -5V, hence pMOS is in on state.	for pMOS, V_{GS} = 0V, hence pMOS is in off state.
Therefore V_o = 5V (since V_{DD} is connected to Vo)	Therefore V_o = 0V (since V_o is connected to GND)

V_{in}	PMOS	NMOS	V_{out}
V_{DD} = 5V (logic 1)	OFF	NO	0V (logic 0)
0V (logic 0)	ON	OFF	V_{DD} = 5V (logic 1)

CMOS Advantages	CMOS Applications
High switching speed (50ns), Low power dissipation (2.5nW), Occupies lower packing density in IC fabrication,	Computer memories, CPUs Microprocessor designs Flash memory chip designing To design application specific integrated circuits (ASICs). Ex: ALU circuits, Microcontrollers, etc.

Silicon Controlled Rectifier (SCR)

An **SCR** (silicon-controlled rectifier) is a 4-layer, three terminal device. The four layers made of P and N layers, are arranged alternately such that they form three junctions J1, J2 and J3 and the three terminals are anode (A), cathode (K), and gate (G) as shown in fig.2.28.

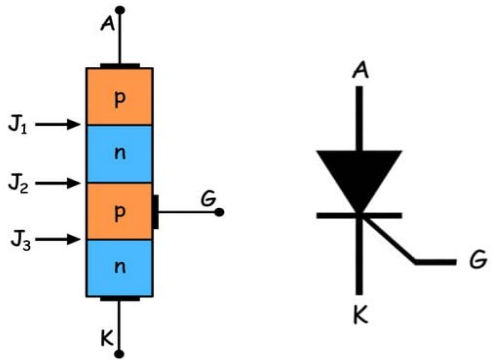


Fig.2.18: SCR and its symbol

1. The outer layers (P and N-layers) are heavily doped whereas middle P and N-layers are lightly doped. The gate terminal is taken at the middle P-layer, anode is from outer P-layer and cathode is from outer N- layer.
2. The SCR is made of silicon because leakage current in silicon is very small.
3. An SCR can be considered as two inter-connected transistors

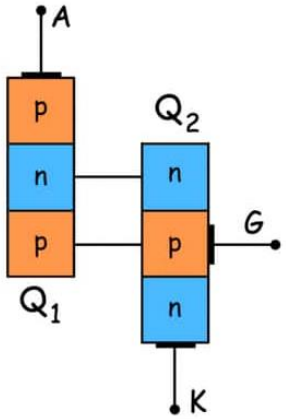


Fig.2.19: SCR as inter-connected transistors

4. It is seen that a single **SCR** is the combination of one pnp transistor (Q_1) and one npn transistor (Q_2).
5. The gate terminal of the SCR is connected to the base of Q_2, too.

Working or Modes of Operation of SCR

1. Depending on the biasing given to the SCR, the operation of SCR is divided into three modes. They are
    1. Forward blocking Mode
    2. Forward Conduction Mode and
    3. Reverse Blocking Mode

Forward Blocking Mode

1. Here the anode terminal is made positive while the gate terminal kept open

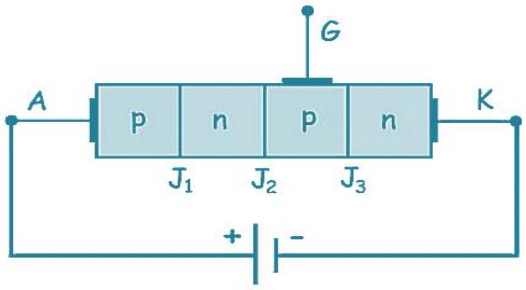


Fig.2.20: SCR under forward blocking Mode

2. Junctions J1 and J3 are forward biased and the junction J2 reverse biased.
3. A small leakage current flows through the SCR. Until the voltage applied across the SCR is more than the break over voltage of it, SCR offers a very high resistance to the current flow. SCR acts as an open switch in this mode by blocking forward current flowing through the SCR as shown in the VI characteristics curve of the SCR.

Forward Conduction Mode

1. In this mode, SCR comes into the conduction mode from blocking mode.
2. The SCR can be made to conduct either
    i. By increasing the +ve voltage applied at anode (A) beyond the Break Over Voltage, V_B
    ii. By applying +ve voltage at the Gate (G) as shown in the fig.2.32.

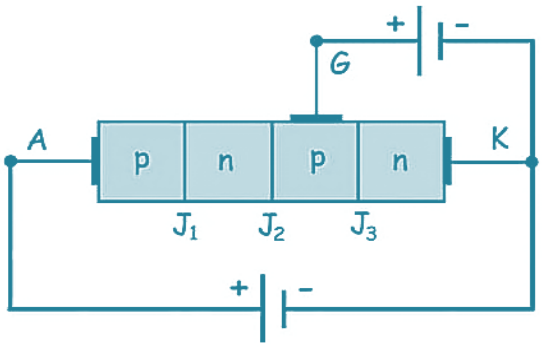


Fig.2.21: SCR under forward conduction Mode

3. Once any one of these is done, the **avalanche breakdown** occurs at J2 and SCR turns ON into conduction mode with current flowing through it.

4. Higher the value of gate current lesser the time to come in conduction mode. Ig3 > Ig2 > Ig1. In this mode, maximum current flows through the SCR depending on the load resistance or impedance.
5. The current at which the SCR turns into conduction mode from blocking mode is called as latching current (I_L).
6. When the forward current at which the SCR returns to blocking state is called as holding current (I_H). At this holding current level, depletion region starts to develop around junction J2. Holding current is slightly less than the latching current.

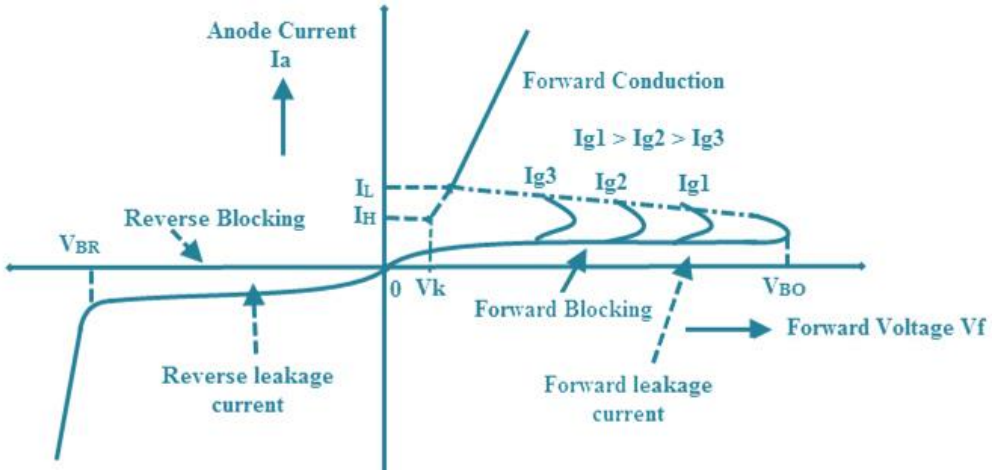


Fig.2.22: VI characteristics of SCR

Reverse Blocking Mode

1. Here, the SCR is reverse biased by connecting its anode (A) to negative end and the cathode terminal (K) to the positive end of the battery as shown in the fig.2.33.

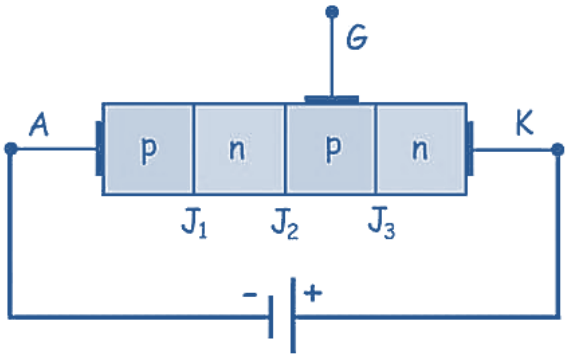


Fig.2.23: SCR under reverse blocking Mode

2. The junctions J_1 and J_3 are reverse biased, which in turn prohibits the flow of current through the device, in spite of the fact that the junction J_2 remains in forward biased condition.
3. This reverse voltage drives the SCR into reverse blocking region results to flow a small leakage current through it and acts as an open switch as shown in figure.
4. If reverse voltage is increased beyond the V_{BR}, avalanche breakdown occurs at junctions

J1 and J3 which results to increase reverse current flow through the SCR.

5. This reverse current causes more losses in the SCR and heats it up damaging SCR considerably if the reverse voltage applied more than VBR.

Two Transistor Model of SCR

Two transistor model of SCR is a method of representing SCR in the form of two transistor model. This represents SCR is the combination of PNP and NPN transistor as shown in the fig.2.34.

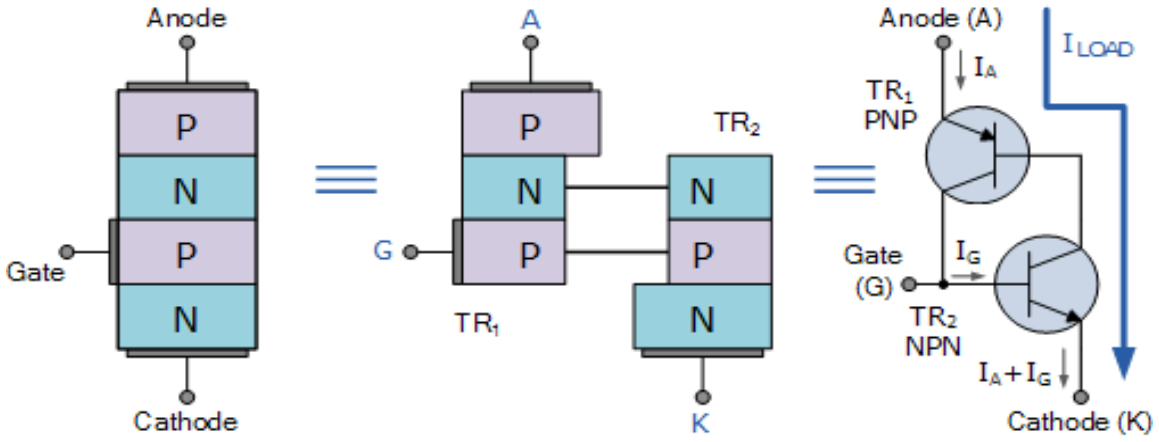


Fig. 2.24 Two transistor model to analuyse SCR working

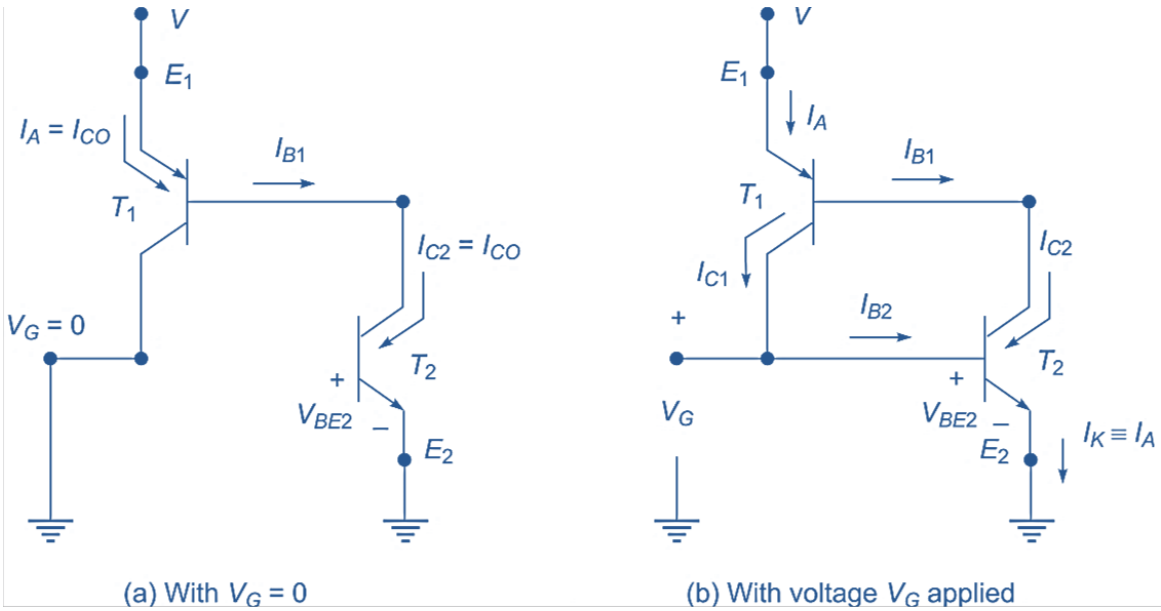


Fig.2.25: Two transistor model of SCR

1. The two transistor equivalent circuit shows that the collector current of the NPN transistor Q_2 feeds directly into the base of the PNP transistor Q_1, while the collector current of Q_1 feeds into the base of Q_2.
2. So until one of the transistors is given some base current SCR cannot turn ON
3. If a positive current is injected into the base of the NPN transistor q_2, the resulting collector current flows in the base of transistor Q_1. This in turn causes a collector current to flow in the PNP transistor, Q_1 which increases the base current of Q_2 and so on.

Commutation

The turn OFF process of an SCR is called commutation - it means the transfer of currents from one path to another. It is done by reducing the forward current to zero so as to turn OFF the SCR. To turn OFF the conducting SCR the below conditions must be satisfied.

The anode or forward current of SCR must be reduced to zero or below the level of holding current,

1) Natural commutation and 2) Forced commutation

Natural Commutation

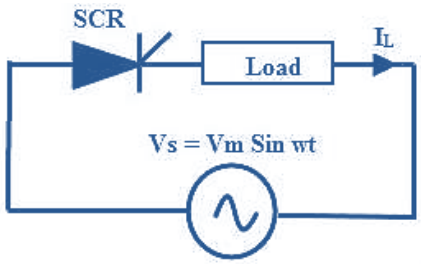
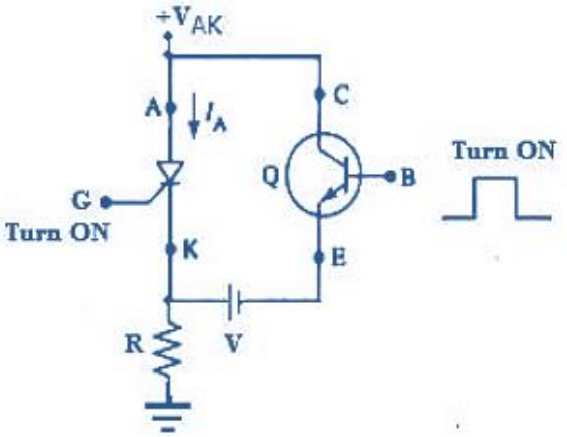


Fig. Inline or Natural Commutation

In AC circuit, the current always passes through zero for every half cycle. (Analyze one AC cycle).If the SCR is connected to an AC supply Vs, as shown in the fig. SCR turns off when negative voltage appears across it. This process is called as natural commutation, since no external circuit is required for this purpose.

2. Forced Commutation

In case of DC circuits, forward current must be forced to zero to turn OFF the SCR, with an external circuit. Hence, named as forced commutation.



This commutation circuit consists of a transistor and a DC supply connected in series to the SCR When SCR is ON, transistor is made OFF.

To turn OFF the SCR, a + ve pulse is applied to the Base of transistor to drive it into saturation. Now, transistor acts like a closed switch.

When $I_A < I_H$, SCR turns OFF. Transistor is held ON just long enough to turn OFF the SCR. Turn-off time of an SCR is typically 5 - 30µs.

QUESTION BANK

1. Explain the characteristics of N-channel JFET.
2. Explain the construction and operation of P-channel JFET with necessary diagram.
3. With neat diagram, explain the characteristics of a enhancement type MOSFET.
4. Explain the construction and working of P-channel enhancement type MOSFET.
5. What is MOSFET? Explain D- MOSFET and E- MOSFET transfer characteristics.
6. With neat circuit diagram, explain the working of CMOS inverter.
7. Draw and explain the operations of SCR using 2-transistor equivalent circuit.
8. Draw and explain the V-I characteristics of SCR.