MODULE 1

CHAPTER -POWER SUPPLIES

Power Supplies

The block diagram of a d.c. power supply is shown in Fig. 6.1. Since the mains input is at a relatively high voltage, a step-down transformer of appropriate turns ratio is used to convert this to a low voltage. The a.c. output from the transformer secondary is then rectified using conventional silicon rectifier diodes (see Chapter 5) to produce an unsmoothed (sometimes referred to as **pulsating d.c.**) output. This is then smoothed and filtered before being applied to a circuit which will **regulate** (or **stabilize**) the output voltage so that it remains relatively constant in spite of variations in both load current and incoming mains voltage. Fig. 6.2 shows how some of the electronic components that we have already met can be used in the realization of the block diagram in Fig. 6.1. The iron-cored step-down transformer feeds a rectifier arrangement (often based on a bridge circuit). The output of the rectifier is then applied to a high-value **reservoir** capacitor. This capacitor stores a considerable amount of charge and is being constantly topped-up by the rectifier arrangement. The capacitor also helps to smooth out the voltage pulses produced by the rectifier. Finally, a stabilizing circuit (often based on a **series transistor regulator** and a Zener diode **voltage reference**) provides a constant output voltage. We shall now examine each stageof this arrangement in turn, building up to some complete power supply circuits at the end of the chapter.

Rectifiers

Semiconductor diodes (see Chapter 5) are commonly used to convert alternating current (a.c.) to direct current (d.c), in which case they are referred to as **rectifiers**. The simplest form of rectifier circuit makes use of a single diode and, since it operates on only either positive or negative half-cycles of the supply, it is known as a **half-wave** rectifier. Fig. 6.4 shows a simple wave half-rectifier circuit. Main's voltage (220 to 240 V) is applied to the primary of a step-down transformer (T1). The secondary of T1 steps down the 240 V r.m.s. to 12 V r.m.s. (the turns ratio of T1 will thus be 240/12 or 20:1). Diode D1 will only allow the current to flow in the direction shown (i.e., from cathode to anode). D1 will be forward biased during each positive half-cycle (relative to common) and will effectively behave like a closed switch. When the circuit current tries to flow in the opposite direction, the voltage bias across the diode will be reversed, causing the diode to act like an open switch (see Figs 6.5(a) and 6.5(b), respectively).

The switching action of D1 results in a pulsating output voltage which is developed across the load resistor (RL). Since the mains supply is at 50 Hz, the pulses of voltage developed across RL will also be at 50 Hz even if only half the a.c. cycle is present. During the positive half-cycle, the diode will drop the 0.6 V to 0.7 V forward threshold voltage normally associated with silicon diodes. However, during the negative half-cycle the peak a.c. voltage will be dropped across D1 when it is reverse biased. This is an important consideration when selecting a diode for a particular application. Assuming that the secondary of T1 provides 12 V r.m.s., the peak voltage output from the transformer's secondary winding will be given by: The peak voltage applied to D1 will thus be approximately 17 V. The negative half-cycles are blocked by D1 and thus only the positive half- cycles appear across RL. Note, however, that the actual peak voltage across RL will be the 17 V positive peak being supplied from the secondary on T1, minus the 0.7 V forward threshold voltage dropped by D1. In other words, positive half-cycle pulses having a peak amplitude of 16.3 V will appear across R_L.

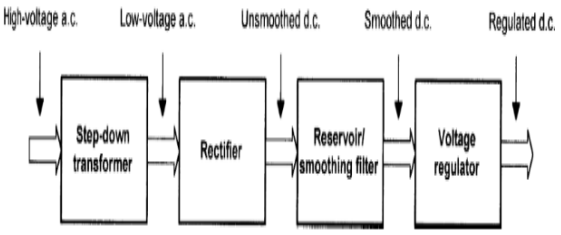


Figure 6.1 Block diagram of a d.c. power supply

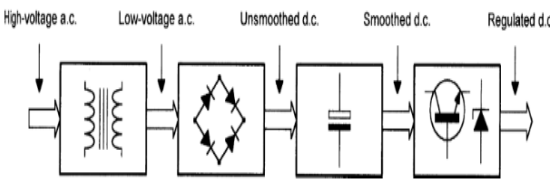


Figure 6.2 Block diagram of a d.c. power supply showing principal components

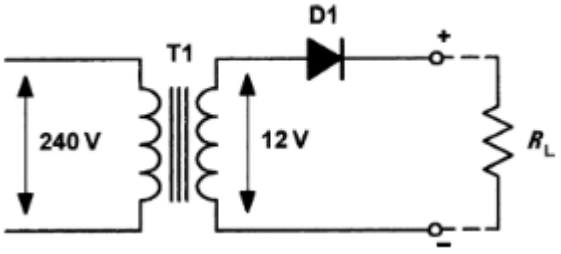


Figure 6.4 A simple half-wave rectifier circuit

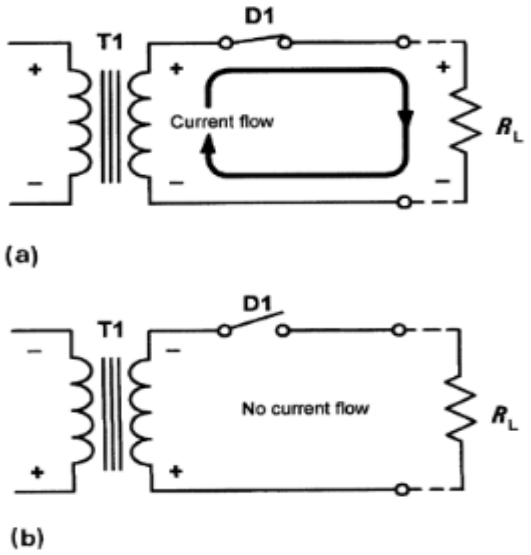


Figure 6.5 (a) Half-wave rectifier circuit with D1 conducting (positive-going half-cycles of secondary voltage); (b) half-wave rectifier with D1 not conducting (negative-going half-cycles ofsecondary voltage)

Reservoir and smoothing circuits

Fig. 6.6 shows a considerable improvement to the circuit of Fig. 6.4. The capacitor, C 1, has been added to ensure that the output voltage remains at, or near, the peak voltage even when the diode is not conducting. When the primary voltage is first applied to T1, the first positive half-cycle output from the secondary will charge C1 to the peak value seen across RL. Hence C1 charges to 16.3 V at the peak of the positive half-cycle. Because C1 and RL are in parallel, the voltage across RL will be the same as that across C1. The time required for C1 to charge to the maximum (peak) level is determined by the charging circuit time constant (the series resistance multiplied by the capacitance value). In this circuit, the series resistance comprises the secondary winding resistance together with the forward resistance of the diode and the (minimal) resistance of the wiring and connections. Hence C1 charges very rapidly as soon as D1 starts to conduct. The time required for C1 to discharge is, in contrast, very much greater. The discharge time constant is determined by the capacitance value and the load resistance, RL. In practice, RL is very much larger than the resistance of the secondary circuit and hence C1 takes an appreciable time to discharge. During this time, D1 will be reverse biased and will thus be held in its non-conducting state. As a consequence, the only discharge path for C1 is through RL. C1 is referred to as a reservoir capacitor. It stores charge during the positive half cycles of secondary voltage and releases it during the negative half-cycles. The circuit of Fig. 6.6 is thus able to maintain a reasonably constant output voltage across RL. Even so, C1 will discharge by a small amount during the negative half-cycle periods from the transformer secondary.

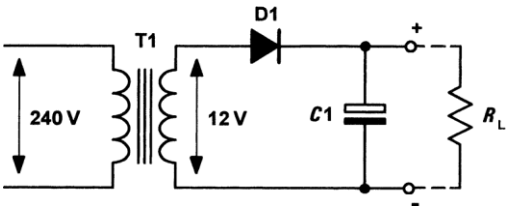


Figure 6.6 A simple half-wave rectifier circuitwith reservoir capacitor

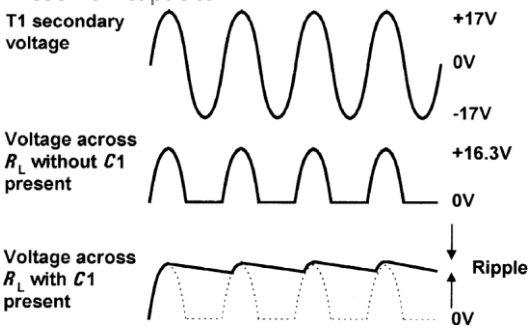


Figure 6.7 A simple half-wave rectifier circuitwith reservoir capacitor

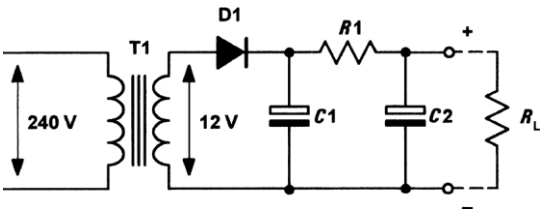


Figure 6.8 Half-wave rectifier circuit with *R-C* smoothing filter

Fig. 6.7 shows the secondary voltage waveform together with the voltage developed across R_L with and without *C*1 present. This gives rise to a small

variation in the d.c. output voltage (known as **ripple**). Since ripple is undesirable, we must take additional precautions to reduce it. One obvious method of reducing the amplitude of the ripple is that of simply increasing the discharge time constant. This can be achieved either by increasing the value of $C1$ or by increasing the resistance value of R_L. In practice, however, the latter is not really an option because R_L is the effective resistance of the circuit being supplied and we don't usually have the ability to change it! Increasing the value of $C1$ is a more practical alternative and very large capacitor values (often in excess of 4,700 μF) are typical. Fig. 6.8 shows a further refinement of the simple power supply circuit. This circuit employs two additional components, $R1$ and $C1$, which act as a filter to remove the ripple. The value of $C1$ is chosen so that the component exhibits a negligible reactance at the ripple frequency (50 Hz for a half-wave rectifier or 100 Hz for a full-wave rectifier – see later). In effect, $R1$ and $C1$ act like a potential divider. The amount of ripple is reduced by an approximate factor equal to:

$$\frac{X_C}{\sqrt{R^2 + X_C^2}}$$

Example 6.2

The R–C smoothing filter in 50 Hz mains operated half-wave rectifier circuit consists of $R1 = 100\ \Omega$ and $C2 = 1{,}000\ \mu F$. If 1 V of ripple appears at the input of the circuit, determine the amount of ripple appearing at the output.

Solution

First, we must determine the reactance of the capacitor, $C1$, at the ripple frequency (50 Hz):

$$X_C = \frac{1}{2\pi fC} = \frac{1}{6.28 \times 50 \times 1{,}000 \times 10^{-6}}$$
$$= \frac{1{,}000}{314} = 3.18\ \Omega$$

The amount of ripple at the output of the circuit (i.e., appearing across $C1$) will be given by:

$$V_{ripple} = 1 \times \frac{X_C}{\sqrt{R^2 + X_C^2}} = 1 \times \frac{3.18}{\sqrt{100^2 + 3.18^2}}$$

From which:

$$V = 0.032\ \text{V} = 32\ \text{mV}$$

Improved ripple filters

A further improvement can be achieved by using an inductor, $L1$, instead of a resistor in the smoothing circuit. This circuit also offers the advantage that the minimum d.c. voltage is dropped across the inductor (in the circuit of Fig. 6.7, the d.c. output voltage is *reduced* by an amount equal to the voltage drop across $R1$).

Fig. 6.9 shows the circuit of a half-wave power supply with an L–C smoothing circuit. At the ripple frequency, $L1$ exhibits a high value of inductive reactance while $C1$ exhibits a low value of capacitive reactance. The combined effect is that of an attenuator which greatly reduces the amplitude of the ripple while having a negligible effect on the direct voltage

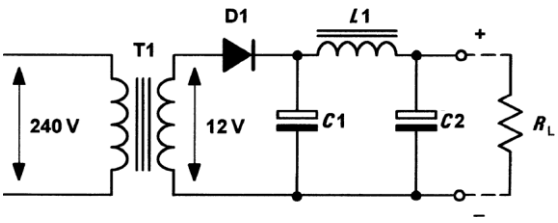


Figure 6.9 Half-wave rectifier circuit with L-C smoothing filter

Example 6.3

The L–C smoothing filter in 50 Hz mains operated half-wave rectifier circuit consists of $L1 = 10$ H and $C2 = 1{,}000\ \mu F$. If 1 V of ripple appears at the input of the circuit, determine the amount of ripple appearing at the output.

Solution

Once again, the reactance of the capacitor, $C1$, is 3.18 Ω (see Example 6.2). The reactance of $L1$ at 50 Hz can be calculated from:

$$X_L = 2\pi fL = 2 \times 3.14 \times 50 \times 10 = 3{,}140\ \Omega$$

The amount of ripple at the output of the circuit (i.e., appearing across $C1$) will be approximately given by:

$$V = 1 \times \frac{X_C}{X_C + X_L} = 1 \times \frac{3.18}{3140 + 3.18} \approx 0.001\ \text{V}$$

Hence the ripple produced by this arrangement (with 1 V of 50 Hz a.c. superimposed on the rectified input) will be a mere 1 mV. It is worth comparing this value with that obtained from the previous example!

Finally, it is important to note that the amount of ripple present at the output of a power supply will increase when the supply is loaded.

Unfortunately, the half-wave rectifier circuit is

relatively inefficient as conduction takes place only on alternate half-cycles. A better rectifier arrangement would make use of both positive *and* negative half-cycles. These **full-wave rectifier** circuits offer a considerable improvement over their half-wave counterparts. They are not only more efficient but are significantly less demandingin terms of the reservoir and smoothing components. There are two basic forms of full-wave rectifier; the bi-phase type and the bridgerectifier type.

Bi-phase rectifier circuits

Fig. 6.10 shows a simple bi-phase rectifier circuit. Main's voltage (240 V) is applied to the primary of the step-down transformer (T1) which has two identical secondary windings, each providing 12 V r.m.s. (the turns ratio of T1 will thus be 240/12 or 20:1 for *each* secondary winding).

On positive half-cycles, point A will be positive with respect to point B. Similarly, point B will be positive with respect to point C. In this condition D1 will allow conduction (its anode will be positive with respect to its cathode) while D2 will not allow conduction (its anode will be negative with respect to its cathode). Thus, D1 alone conducts on positive half-cycles.

On negative half-cycles, point C will be positive with respect to point B. Similarly, point B will be positive with respect to point A. In this condition D2 will allow conduction (its anode will be positive with respect to its cathode) while D1 will not allow conduction (its anode will be negative with respect to its cathode). Thus, D2 alone conducts on negative half-cycles.

Fig. 6.11 shows the bi-phase rectifier circuit with the diodes replaced by switches. In Fig. 6.11(a) D1 is shown conducting on a positive half-cycle while in Fig. 6.11(b) D2 is shown conducting. Theresult is that current is routed through the load *in the same direction* on successive half-cycles.

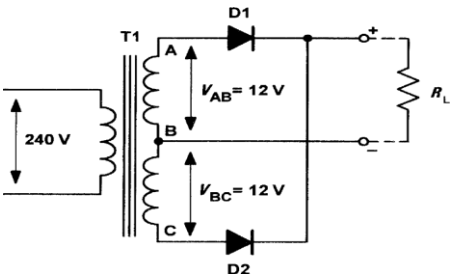


Figure 6.10 Bi-phase rectifier circuit

Furthermore, this current is derived alternately from the two secondary windings. As with the half-wave rectifier, the switching action of the two diodes results in a pulsating output voltage being developed across the load resistor (R_L). However, unlike the half-wave circuitthe pulses of voltage developed across R_L will occur at a frequency of 100 Hz (*not* 50 Hz). This doubling of the ripple frequency allows us to use smaller values of reservoir and smoothing capacitor to obtain the same degree of ripple reduction (recall that the reactance of a capacitoris reduced as frequency increases).

As before, the peak voltage produced by each of the secondary windings will be approximately 17 V and the peak voltage across R_L will be 16.3 V (i.e., 17 V less the 0.7 V forward threshold voltage dropped by the diodes).

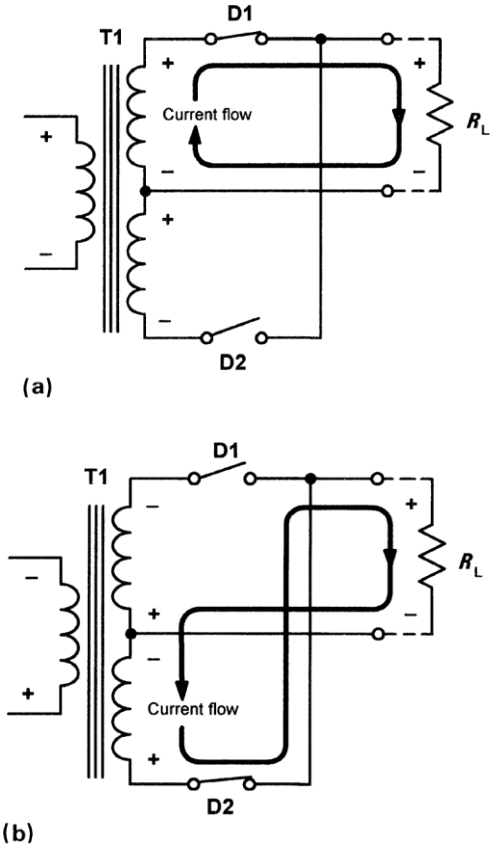


Figure 6.11 (a) Bi-phase rectifier with D1 conducting and D2 non-conducting
(b) bi-phase rectifier with D2 conducting and D1 non-conducting

Fig. 6.12 shows how a reservoir capacitor (*C*1) can be added to ensure that the output voltage remains at, or near, the peak voltage even whenthe diodes are not conducting. This component operates in exactly the same way as for the half-wave circuit, i.e., it charges to approximately 16.3 V at the peak of the positive half-cycle and holds the voltage at this level when the diodes are in their non-

conducting states. The time required for C1 to charge to the maximum (peak) level is determined by the charging circuit time constant (the series resistance multiplied by the capacitance value). In this circuit, the series resistance comprises the secondary winding resistance together with the forward resistance of the diode and the (minimal) resistance of the wiring and connections. Hence *C*1 charges very rapidly as soon as either D1 or D2 starts to conduct. The time required for *C*1 to discharge is, in contrast, very much greater. The discharge time contrast is determined by the capacitance value and the load resistance, *R*. In practice, *R* is very much larger than the resistance of the secondary circuit and hence *C*1 takes an appreciable time to discharge. During this time, D1 and D2 will be reverse biased and held in a non-conducting state. As a consequence, the only discharge path for *C*1 is through R_L. Fig. 6.13 shows voltage waveforms for the bi-phase rectifier, with and without *C*1 present. Note that the ripple frequency (100 Hz) is twice that of the half-wave circuit shown previously in Fig. 6.7.

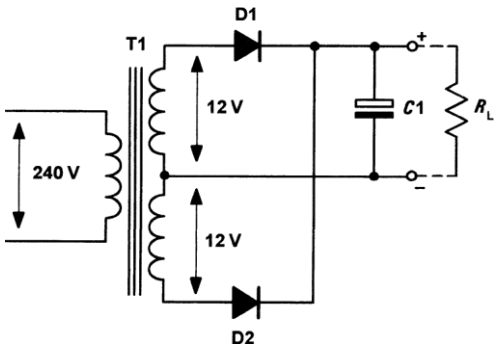


Figure 6.12 Bi-phase rectifier with reservoir capacitor

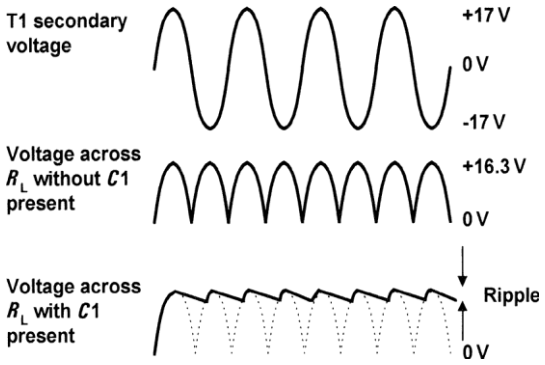


Figure 6.13 Waveforms for the bi-phase rectifier

Bridge rectifier circuits

An alternative to the use of the bi-phase circuitis that of using a four-diode bridge rectifier (seeFig. 6.14) in which opposite pairs of diodes conduct on alternate half-cycles. This arrangement avoids the need to have two separate secondary windings.

A full-wave bridge rectifier arrangement is shown in Fig. 6.15. Main's voltage (240 V) is applied to the primary of a step-down transformer (T1). The secondary winding provides 12V r.m.s. (Approximately 17 V peak) and has a turns ratio of 20:1, as before. On positive half-cycles, point A will be positive with respect to point B. In this condition D1 and D2 will allow conduction while D3 and D4 will not allow conduction. Conversely, on negative half-cycles, point B will be positive with respect to point A. In this condition D3 and D4 will allow conduction while D1 and D2 will not allow conduction.

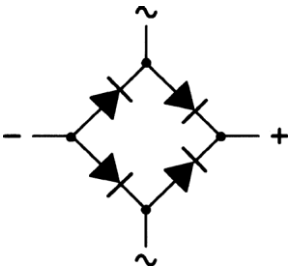


Figure 6.14 Four diodes connected as a bridge

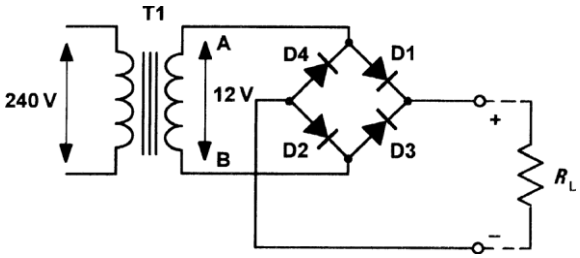


Figure 6.15 Full-wave bridge rectifier circuit

D4 are conducting. Once again, the result is that current is routed through the load *in the same direction* on successive half-cycles. As with the bi-phase rectifier, the switching action of the twodiodes results in a pulsating output voltage beingdeveloped across the load resistor (R_L). Once again, the peak output voltage is approximately 16.3 V (i.e., 17 V less the 0.7 V forward thresholdvoltage).

Fig. 6.17 shows how a reservoir capacitor (*C*1) can be

added to maintain the output voltage when the diodes are not conducting. This component operates in exactly the same way as for the bi-phase circuit, i.e., it charges to approximately 16.3 V at the peak of the positive half-cycle and holds the voltage at this level when the diodes are in their non-conducting states. This component operates in exactly the same way as for the bi-phase circuit and the secondary and rectified output waveforms are shown in Fig. 6.18. Once again note that the ripple frequency is twice thatof the incoming a.c. supply. Finally, *R–C* and *L–C* ripple filters can be added to bi-phase and bridge rectifier circuits in exactlythe same way as those shown for the half-waverectifier arrangement (see Figs 6.8 and 6.9).

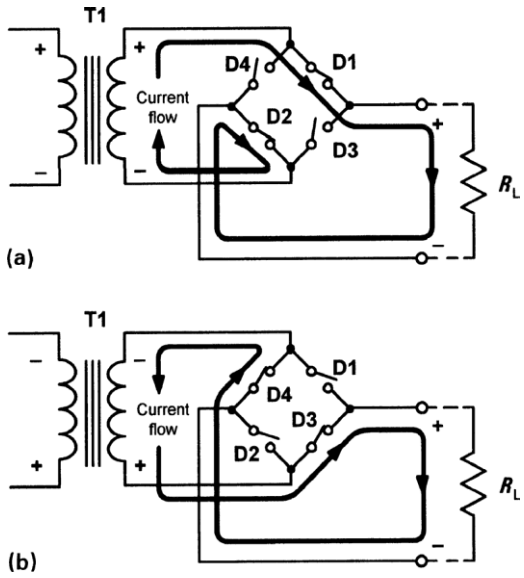


Figure 6.16 (a) Bridge rectifier with D1 and D2 conducting, D3 and D4 non-conducting (b) bridge rectifier with D1 and D2 non-conducting, D3 and D4 conducting

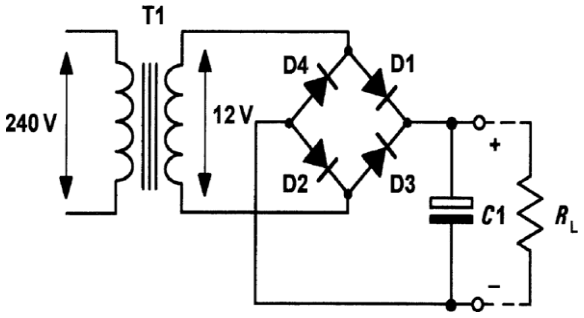


Figure 6.17 Bridge rectifier with reservoircapacitor

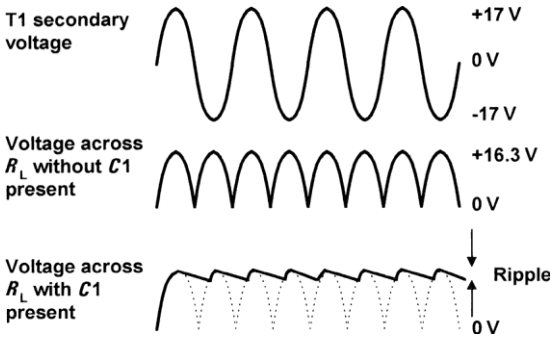


Figure 6.18 Waveforms for the bridge rectifier

Voltage regulators

A simple voltage regulator is shown in Fig. 6.19 R_S is included to limit the Zener current to a safe value when the load is disconnected. When a load (R_L) is connected, the Zener current (I_Z) will fall as current is diverted into the load resistance (it is usual to allow a minimum current of 2 mA to5 mA in order to ensure that the diode regulates).The output voltage (V_Z) will remain at the Zener voltage until regulation fails at the point at which the potential divider formed by R_S and R_L produces a lower output voltage that is less than V_z.

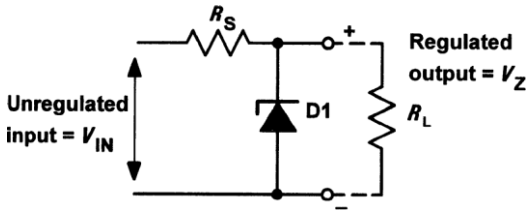


Figure 6.19 A simple shunt Zener voltage regulator

The ratio of *Rs* to R_L is thus important. At the point at which the circuit just begins to fail to regulate:

$$V_Z = V_{IN} \times \frac{R_L}{R_L + R_S}$$

Where V_{IN} is the unregulated input voltage. Thus, the *maximum* value for R_S can be calculated from:

$$R_S \text{ max.} = R_L \times \left(\frac{V_{IN}}{V_{IN}} - 1 \right)$$

The power dissipated in the Zener diode will be given by $P_Z = I_Z \times V_Z$, hence the minimum value forR_S can be determined from the off-load condition when:

$$R_S \text{ min.} = \frac{V_{IN} - V_Z}{I_Z} = \frac{V_{IN} - V_Z}{\left(\frac{P_Z \text{ max.}}{V_Z}\right)} = \frac{(V_{IN} - V_Z) \times V_Z}{P_Z \text{ max.}}$$

Thus:

$$R_S \text{ min.} = \frac{V_{IN}V_Z - V_Z^2}{P_Z \text{ max.}}$$

where *Pz* max. is the maximum rated power dissipation for the Zener diode.

Example 6.4

A 5 V Zener diode has a maximum rated power dissipation of 500 mW. If the diode is to be usedin a simple regulator circuit to supply a regulated5 V to a load having a resistance of 400 Ω,, determine a suitable value of series resistor for operation in conjunction with a supply of 9 V.

Solution

We shall use an arrangement similar to that shown in Fig. 6.19. First, we should determine the maximum value for the series resistor, R_S:

$$R_S \text{ max.} = R_L \times \left(\frac{V_{IN}}{V_{IN}} - 1\right)$$

thus:

$$R_S \text{ max.} = 400 \times \left(\frac{9}{5} - 1\right) = 400 \times (1.8 - 1) = 320\ \Omega$$

Now we need to determine the minimum value for the series resistor, R_S:

$$R_S \text{ min.} = \frac{V_{IN}V_Z - V_Z^2}{P_Z \text{ max.}}$$

thus:

$$R_S \text{ min.} = \frac{(9 \times 5) - 5^2}{0.5} = \frac{45 - 25}{0.5} = 40\ \Omega$$

Hence a suitable value for R_S would be 150 Ω (roughly mid-way between the two extremes).

Output resistance and voltage Regulation

In a perfect power supply, the output voltage would remain constant regardless of the current taken by the load. In practice, however, the output voltage falls as the load current increases. To account for this fact, we say that the power. supply has **internal resistance** (ideally this should be zero). This internal resistance appears at the output of the supply and is defined as the change in output voltage divided by the corresponding change in output current. Hence:

$$R_{out} = \frac{\text{change in output voltage}}{\text{change in output current}} = \frac{\Delta V_{out}}{\Delta I_{out}}$$

where ΔI_{out} represents a small change in output (load) current and ΔV_{out} represents a corresponding small change in output voltage. The **regulation** of a power supply is given by the relationship:

$$\text{Regulation} = \frac{\text{change in output voltage}}{\text{change in line (input) voltage}} \times 100\%$$

Ideally, the value of regulation should be verysmall. Simple shunt Zener diode regulators of the type shown in Fig. 6.19 are capable of producing values of regulation of 5% to 10%. More sophisticated circuits based on discrete components produce values of between 1% and 5% and integrated circuit regulators often providevalues of 1% or less

Example 6.5

The following data were obtained during a test carried out on a d.c. power supply:

***(i)** Load test*

Output voltage (no-load) = 12 V
Output voltage (2 A load current) = 11.5 V

***(ii)** Regulation test*

Output voltage (mains input, 220 V) = 12 V Output voltage (mains input, 200 V) = 11.9 V

Determine (a) the equivalent output resistance of the power supply and (b) the regulation of the power supply.

Solution

The output resistance can be determined fromthe load test data:

$$R_{out} = \frac{\text{change in output voltage}}{\text{change in output current}} = \frac{12 - 11.5}{2 - 0} = 0.25\ \Omega$$

The regulation can be determined from the regulation test data:

$$\text{Regulation} = \frac{\text{change in output voltage}}{\text{change in line (input) voltage}} \times 100\%$$

thus

$$\text{Regulation} = \frac{12 - 1.9}{220 - 200} \times 100\% = \frac{0.1}{20} \times 100\% = 0.5\%$$

Voltage multipliers

By adding a second diode and capacitor, we can increase the output of the simple half-wave rectifier that we met earlier. A voltage doubler using this technique is shown in Fig. 6.25. In this arrangement C1 will charge to the positive peak secondary voltage while C2 will charge to the negative peak secondary voltage. Since the output is taken from C1 and C2 connected in series the resulting output voltage is twice that produced by one diode alone. The voltage doubler can be extended to produce higher voltages using the cascade

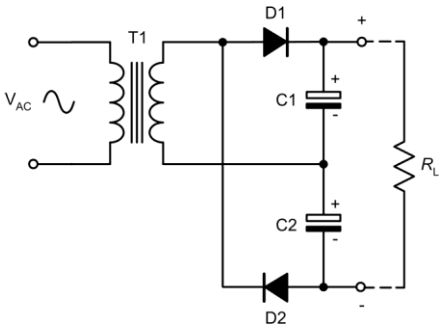


Figure 6.25 A voltage doubler

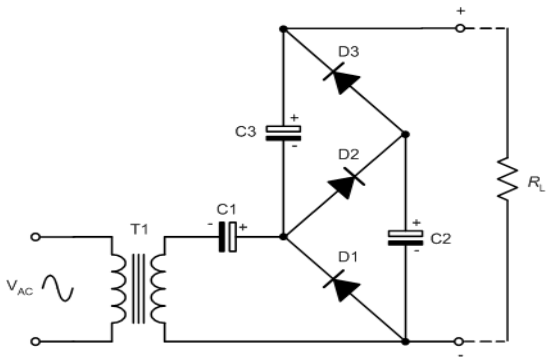


Figure 6.26 A voltage Tripler

arrangement shown in Fig. 6.26. Here C1 chargesto the positive peak secondary voltage, while C2 and C3 charge to twice the positive peak secondary voltage. The result is that the output voltage is the sum of the voltages across C1 and C3 which is three times the voltage that would be produced by a single diode. The ladderarrangement shown in Fig. 6.25 can be easily extended to provide even higher voltages but the efficiency of the circuit becomes increasingly impaired and high-order voltage multipliers of this type are only suitable for providing relativelysmall currents.

PROBLEMS:

6.1 A half-wave rectifier is fitted with an *R-C* smoothing filter comprising $R = 200\ \Omega$ and $C = 50\ \mu F$. If 2 V of 400 Hz ripple appearat the input of the circuit, determine the amount of ripple appearing at the output. The *L-C* smoothing filter fitted to a 50 Hz

6.2 *The L-C smoothing filter to a 50 Hz* mains operated full-wave rectifier circuit consists of $L = 4$ H and $C = 500\ \mu F$. If 4 V of ripple appear at the input of the circuit, determine the amount of ripple appearing at the output.

6.3 If a 9 V Zener diode is to be used in a simple shunt regulator circuit to supply a load having a nominal resistance of 300 Ω,determine the maximum value of series resistor for operation in conjunction with asupply of 15 V.

6.4 The circuit of a d.c. power supply is shown in Fig. 6.37. Determine the voltages that will appear at test points A,B and C.

6.5 In Fig. 6.37, determine the current flowing in *R*1 and the power dissipated in D5 when the circuit is operated without any load connected

6.6 In Fig. 6.37, determine the effect of each

Of the following fault conditions:

(a) *R*1 open-circuit;
(b) D5 open-circuit;
(c) D5 short-circuit.

6.7 A 220 V a.c supply feeds a 20:1 step- down transformer, the secondary of which is connected to a bridge rectifier and reservoir capacitor. Determine the approximate d.c. voltage that will appear across the reservoir capacitor under 'no- load' conditions.

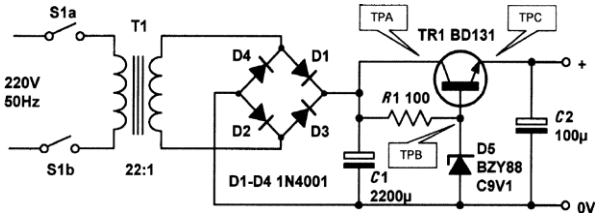


Figure 6.37 See Questions 6.4, 6.5 and 6.6

6.8 The following data were obtained during a load test carried out on a d.c. power supply:

Output voltage (no-load) = 8.5 V

Output voltage (800 mA load) = 8.1 V

Determine the output resistance of the

power supply and estimate the output

voltage at a load current of 400 mA.

6.9 The following data were obtained during a regulation test on a d.c. power supply:

Output voltage (a.c. input: 230 V) = 15 V Output voltage (a.c. input: 190 V) = 14.6 V

Determine the regulation of the power supply and estimate the output voltagewhen the input voltage is 245 V.

6.10 Fig. 6.38 shows a switching regulator circuit that produces an output of 9 V foran input of 4.5 V. What type of regulatoris this? Between which pins of IC1 is the switching transistor connected? Which pin on IC1 is used to feed back a proportion of the output voltage to the internal comparator stage?

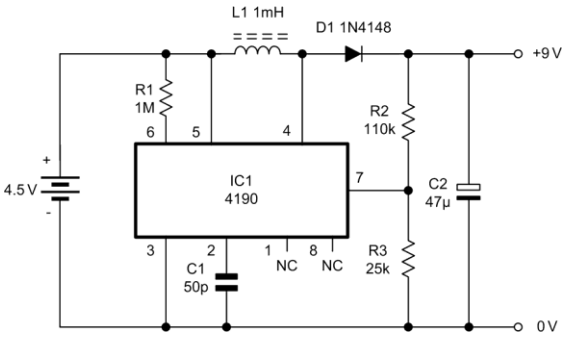


Figure 6.38 See Question 6.10

CHAPTER-AMPLIFIERS

Types of amplifiers

Many different types of amplifiers are found in electronic circuits. Before we explain the operation of transistor amplifiers in detail, we shallbriefly describe the main types of amplifiers.

a.c. coupled amplifiers

In a.c. coupled amplifiers, stages are coupled together in such a way that d.c. levels are isolated and only the a.c. components of a signal are transferred from stage to stage.

d.c. coupled amplifiers

In d.c. (or direct) coupled amplifiers, stages are coupled together in such a way that stages are not isolated to d.c. potentials. Both a.c. and d.c. signal components are transferred from stage to stage.

Large-signal amplifiers

Large-signal amplifiers are designed to cater for appreciable voltage and/or current levels (typically from 1 V to 100 V or more).

Small-signal amplifiers

Small-signal amplifiers are designed to cater for low-level signals (normally less than 1 V and often much smaller). Small-signal amplifiers have to be specially designed to combat the effects of noise.

Audio frequency amplifiers

Audio frequency amplifiers operate in the band of frequencies that is normally associated with audio signals (e.g., 20 Hz to 20 kHz).

Wideband amplifiers

Wideband amplifiers are capable of amplifying a very wide range of frequencies, typically from a few tens of hertz to several megahertz.

Radio frequency amplifiers

Radio frequency amplifiers operate in the band of frequencies that is normally associated with radio signals (e.g., from 100 kHz to over 1 GHz). Note that it is desirable for amplifiers of this type to be frequency selective and thus their frequency response may be restricted to a relatively narrow band of frequencies (see Fig. 7.9 on page 139).

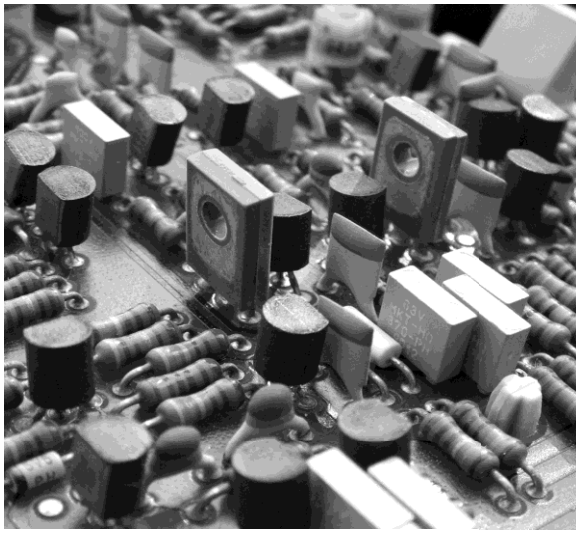


Figure 7.1 Part of a high-gain, wideband d.c. coupled amplifier using discrete components

Low-noise amplifiers

Low-noise amplifiers are designed so that they contribute negligible noise (signal disturbance) to the signal being amplified. These amplifiers are usually designed for use with very small signal levels (usually less than 10 mV or so).

Gain

One of the most important parameters of an amplifier is the amount of amplification or gain that it provides. Gain is simply the ratio of outputvoltage to input voltage, output current to input current, or output power to input power (see Fig. 7.2). These three ratios give, respectively, the voltage gain, current gain and power gain.
Thus:

$$\text{Voltage gain, } A_v = \frac{V_{out}}{V_{in}}$$

$$\text{Current gain, } A_i = \frac{I_{out}}{I_{in}}$$

$$\text{Power gain, } A_p = \frac{P_{out}}{P_{in}}$$

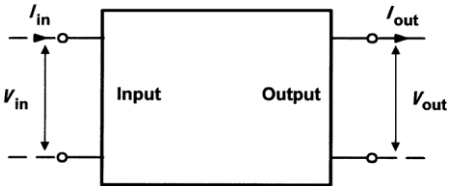


Figure 7.2 Block diagram for an amplifier showing input and output voltages and currents

Note that, since power is the product of currentand voltage ($P = I\ V$), we can infer that:

$$A_p = \frac{P_{out}}{P_{in}} = \frac{I_{out} \times V_{out}}{I_{in} \times V_{in}} = \frac{I_{out}}{I_{in}} \times \frac{V_{out}}{V_{in}} = A_i \times A_v$$

Example 7.1

An amplifier produces an output voltage of 2 V foran input of 50 mV. If the input and output currentsin this condition are, respectively, 4 mA and 200 mA, determine:

(a) the voltage gain;
(b) the current gain;
(c) the power gain.

Solution

(a) The voltage gain is calculated from:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{2\ \text{V}}{50\ \text{mV}} = 40$$

(b) The current gain is calculated from:

$$A_i = \frac{I_{out}}{I_{in}} = \frac{200\ \text{mA}}{4\ \text{mA}} = 50$$

(c) The power gain is calculated from:

$$A_p = \frac{I_{out} \times V_{out}}{I_{in} \times V_{in}} = \frac{200\ \text{mA} \times 2\ \text{V}}{4\ \text{mA} \times 50\ \text{mV}} = \frac{0.4\ \text{W}}{200\ \mu\text{W}} = 2{,}000$$

Note that the same result is obtained from:

$$A_p = A_i \times A_v = 50 \times 40 = 2{,}000$$

Class of operation

An important requirement of most amplifiers isthat the output signal should be a faithful copyof the input signal, albeit somewhat larger in amplitude. Other types of amplifier are non-linear,in which case their input and output waveforms will not necessarily be similar. In practice, the degree of **linearity** provided by an amplifier can be affected by a number of factors including the amount of bias applied (see later) and theamplitude of the input signal. It is also worth noting that a linear amplifier will become non-linear when the applied input signalexceeds a threshold value. Beyond this value theamplifier is said to be **overdriven** and the outputwill become increasingly distorted if the input signal is further increased.

Amplifiers are usually designed to be operated with a particular value of bias supplied to the active devices (i.e., transistors). For linear operation, the active device(s) must be operated in the linear part of their **transfer characteristic** (V_{out} plotted against V_{in}). In Fig. 7.3 the input andoutput signals for an amplifier are operating in linear mode. This form of operation is known as **Class A** and the **bias point** is adjusted to the mid-point of the linear part of the transfer characteristic. Furthermore, current will flow in the active devices used in a Class A amplifier during a complete cycle of the signal waveform.At no time does the current fall to zero. Fig. 7.4 shows the effect of moving the bias pointdown the transfer characteristic and, at the same time, increasing the amplitude of the input signal.From this, you should notice that the extreme negative portion of the output signal has become distorted. This effect arises from the non-linearity of the transfer characteristic that occurs near theorigin (i.e., the zero point). Despite the obvious

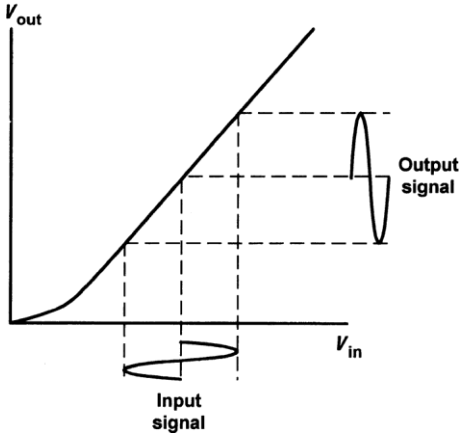


Figure 7.3 Class A (linear) operation

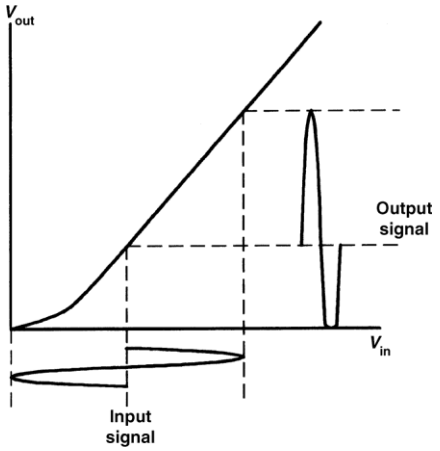


Figure 7.4 Effect of reducing bias and increasing input signal amplitude (the output waveform is no longer a faithful reproduction of the input)

non-linearity in the output waveform, the activedevice(s) will conduct current during a complete cycle of the signal waveform. Now consider the case of reducing the bias even further while further increasing the amplitude of the input signal (see Fig. 7.5). Herethe bias point has been set at the projected cut-off point. The negative-going portion of the output signal becomes cut-off (or **clipped**) and theactive device(s) will cease to conduct for this part of the cycle. This mode of operation is known as **Class AB**. Now let's consider what will happen if no biasat all is applied to the amplifier (see Fig. 7.6).

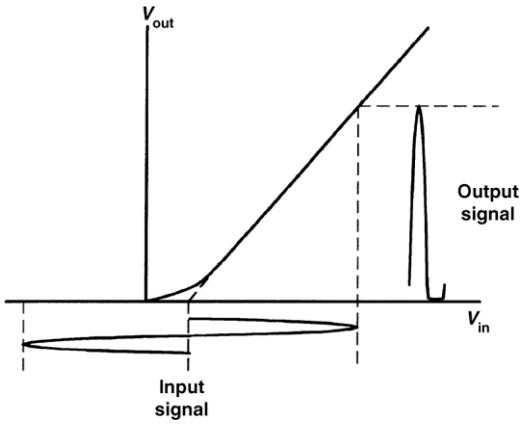


Figure 7.5 Class AB operation (bias set atprojected cut-off)

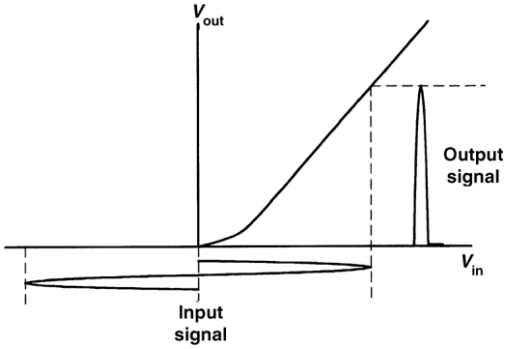


Figure 7.6 Class B operation (no bias applied)

The output signal will only comprise a series of positive-going half-cycles and the active device(s) will only be conducting during half-cycles of the waveform (i.e., they will only be operating 50% ofthe time). This mode of operation is known as **Class B** and is commonly used in high-efficiency push–pull power amplifiers where the two active devices inthe output stage operate on alternate half-cycles of the waveform. Finally, there is one more class of operation to consider. The input and output waveforms for **Class C** operation are shown in Fig. 7.7. Here, the bias point is set at beyond the cut-off (zero) point and a very large input signal is applied. Theoutput waveform will then comprise a series of quite sharp positive-going pulses. These pulses of current or voltage can be applied to a tuned circuit load in order to recreate a sinusoidal signal.In effect, the pulses will excite the tuned circuit.

and its inherent flywheel action will produce a sinusoidal output waveform. This mode of operation is only used in RF power amplifiers that must operate at very high levels of efficiency

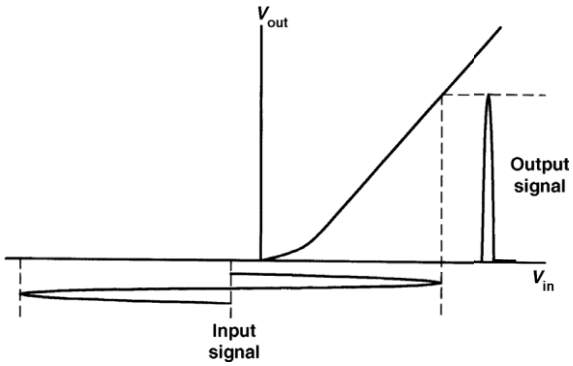


Figure 7.7 Class C operation (bias is set beyondcut-off)

Input and output resistance

Input resistance is the ratio of input voltage to input current and it is expressed in ohms. The input of an amplifier is normally purely resistive (i.e., any reactive component is negligible) in the middle of its working frequency range (i.e., the **mid-band**). In some cases, the reactance of the input may become appreciable (e.g., if a large value of stray capacitance appears in parallel withthe input resistance). In such cases we would refer to **input impedance** rather than input resistance. Output resistance is the ratio of open-circuit output voltage to short-circuit output current andis measured in ohms. Note that this resistance is internal to the amplifier and should not be confused with the resistance of a load connectedexternally. As with input resistance, the output of an amplifier is normally purely resistive and we can safely ignore any reactive component. If thisis not the case, we would once again need to refer to **output impedance** rather than output resistance. Fig. 7.8 shows how the input and output resistances are 'seen' looking into the input and output terminals, respectively. We shall bereturning to this equivalent circuit a little later in

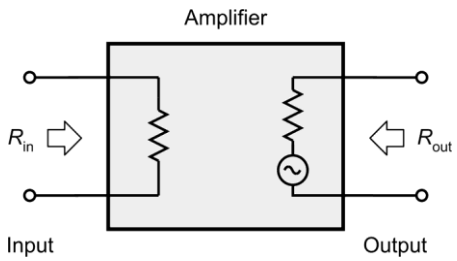


Figure 7.8 Input and output resistances 'seen'looking into the input and output terminals, respectively

this chapter. Finally, it's important to note that, although these resistances are meaningful in terms of the signals present, they cannot be measured using a conventional meter!

Frequency response

The frequency response characteristics for various types of amplifiers are shown in Fig. 7.9.Note that, for response curves of this type, frequency is almost invariably plotted on a **logarithmic scale**. The frequency response of an amplifier is usually specified in terms of the upper and lower **cut-off frequencies** of the amplifier. These frequencies are those at which the output power has droppedto 50% (otherwise known as the **–3 dB points**) or where the voltage gain has dropped to 70.7% of its mid-band value. Figs 7.10 and 7.11, respectively, show how the bandwidth can be expressed in terms of either power or voltage (the cut-off frequencies, f_1 andf_2, and bandwidth are identical).

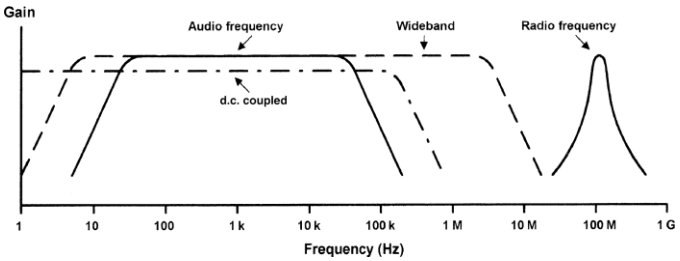


Figure 7.9 Frequency response and bandwidth (output power plotted against frequency)

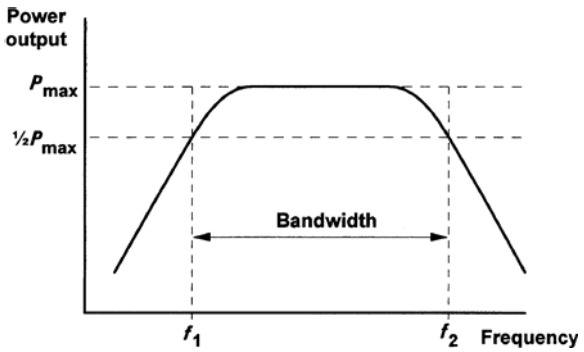


Figure 7.10 Frequency response and bandwidth(output power plotted against frequency)

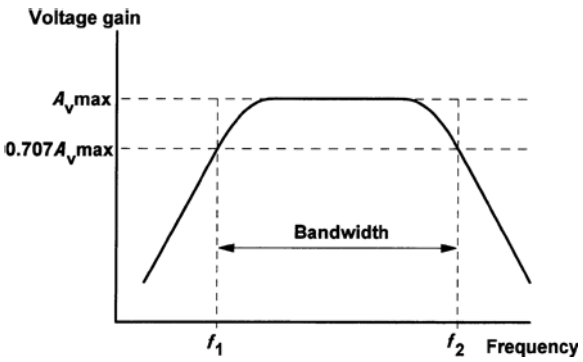


Figure 7.11 Frequency response and bandwidth(output voltage plotted against frequency)

Example 7.2

Determine the mid-band voltage gain and upper and lower cut-off frequencies for the amplifier whose frequency response is shown in Fig. 7.12.

Solution

The mid-band voltage gain corresponds with the flat part of the frequency response characteristic. At that point the voltage gain reaches a maximumof 35 (see Fig. 7.12).

The voltage gain at the two cut-off frequenciescan be calculated from:

A_v cut-off $= 0.707 \times A_v$ max $= 0.707 \times 35 = 24.7$This value of gain intercepts the frequency response graph at $f_1 = 57$ Hz and $f_2 = 590$ kHz (seeFig. 7.12).

Bandwidth

The bandwidth of an amplifier is usually taken as the difference between the upper and lower cut-off frequencies (i.e., $f_2 - f_1$ in Figs 7.10 and 7.11). The bandwidth of an amplifier must be sufficient to accommodate the rangeof frequencies present within the signals that it is to be presented with. Many signals contain **harmonic** components (i.e., signals at $2f$, $3f$, $4f$, etc. where f is the frequency of the **fundamental** signal). To reproduce a square wave, for example, requires an amplifier with avery wide bandwidth (note that a square wave comprises an infinite series of harmonics). Clearlyit is not possible to *perfectly* reproduce such a wave, but it does explain why it can be desirable for an amplifier's bandwidth to greatly exceed the highest signal frequency that it is requiredto handle!

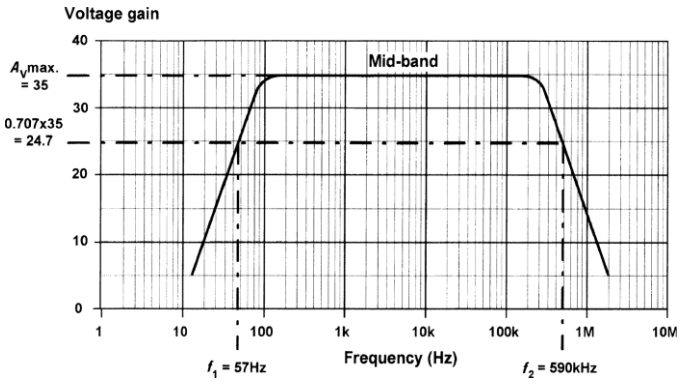


Figure 7.12 See Example 7.2

Phase shift

Phase shift is the phase angle between the inputand output signal voltages measured in degrees.The measurement is usually carried out in the mid-band where, for most amplifiers, the phase shift remains relatively constant. Note also that conventional single-stage transistor amplifiers

provide phase shifts of either 180° or 360°.

Negative feedback

Many practical amplifiers use negative feedbackin order to precisely control the gain, reduce distortion and improve bandwidth. The gain can be reduced to a manageable value by feeding back a small proportion of the output. The amount of feedback determines the overall (or **closed-loop**) gain. Because this form of feedback has the effectof reducing the overall gain of the circuit, this form of feedback is known as **negative feedback**. An alternative form of feedback, where the output is fed back in such a way as to reinforce the input (rather than to subtract from it) is known as **positive feedback**. This form of feedback is used in oscillator circuits (see Chapter 9). Fig. 7.13 shows the block diagram of an amplifier stage with negative feedback applied. In this circuit, the proportion of the output voltage fed back to the input is given by β and the overall voltage gain will be given by:

$$\text{Overall gain, } G = \frac{V_{out}}{V_{in}}$$

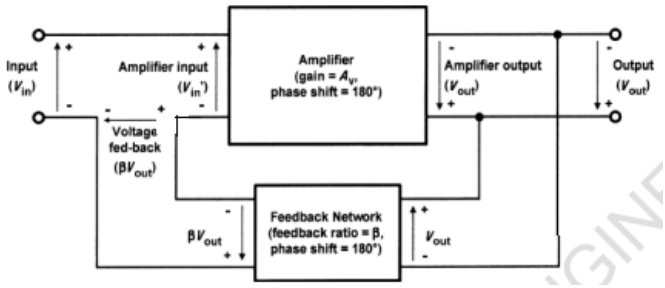


Figure 7.13 Amplifier with negative feedback applied

Now $V_{in}' = V_{in} - \beta V_{out}$ (by applying Kirchhoff's Voltage Law) (note that the amplifier's input voltage has been *reduced* by applying negativefeedback) thus:

$$V_{in} = V_{in}' + \beta V_{out}$$

and

$V_{out} = A_v \times V_{in}$ (note that A_v is the **internal gain** of the amplifier)

Hence:

$$\text{Overall gain, } G = \frac{A_v \times V_{in}'}{V_{in}' + \beta V_{out}} = \frac{A_v \times V_{in}'}{V_{in}' + \beta(A_v \times V_{in}')}$$

Thus:

$$G = \frac{A_v}{1 + \beta A_v}$$

Hence, the overall gain with negative feedback applied will be less than the gain without feedback.

Furthermore, if A_V is very large (as is the case with an operational amplifier – see Chapter 8) the overall gain with negative feedback applied will be given by:

$G = 1/\beta$ (when A_v is very large)

Note, also, that the **loop gain** of feedback amplifier is defined as the product of β and A_v.

Example 7.3

An amplifier with negative feedback applied has an open-loop voltage gain of 50, and one-tenth of its output is fed back to the input (i.e., $\beta = 0.1$).Determine the overall voltage gain with negativefeedback applied.

Solution

With negative feedback applied the overall voltagegain will be given by:

$$G = \frac{A_v}{1 + \beta A_v} = \frac{50}{1 + (0.1 \times 50)} = \frac{50}{6} = 8.33$$

Example 7.4

If, in Example 7.3, the amplifier's open-loop voltage gain increases by 20%, determine thepercentage increase in overall voltage gain.

Solution

The new value of voltage gain will be given by:

$$A_v = A_v + 0.2A_v = 1.2 \times 50 = 60$$

The overall voltage gain with negative feedbackwill then be:

$$G = \frac{A_v}{1 + \beta A_v} = \frac{60}{1 + (0.1 \times 60)} = \frac{60}{7} = 7.14$$

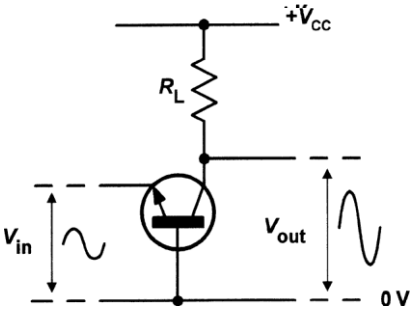
The increase in overall voltage gain, expressed asa percentage, will thus be:

$$\frac{8.57 - 8.33}{8.33} \times 100\% = 2.88\%$$

Note that this example illustrates one of the important benefits of negative feedback in stabilizing the overall gain of an amplifier stage.

Example 7.5

An integrated circuit that produces an open- loop gain of 100 is to be used as the basis of an amplifier stage having a precise voltage gain of 20. Determine the amount of feedback required.



Solution

Re-arranging the formula, $G = \frac{A_v}{1+\beta A_v}$ to make β the subject gives:

$$\beta = \frac{1}{G} - \frac{1}{A_v}$$

Thus:

$$\beta = \frac{1}{20} - \frac{1}{100} = 0.05 - 0.01 = 0.04$$

Transistor amplifiers

Regardless of what type of transistor is employed,three basic circuit configurations are used. These three circuit configurations depend upon which one of the three transistor connections is made common to both the input and the output. In the case of bipolar transistors, the configurations are known as **common emitter**, **common collector** (or **emitter follower**) and **common base**. Where field effect transistors are used, the corresponding configurations are **common source**, **common drain** (or **source follower**) and common gate The three basic circuit configurations (Figs 7.14 to 7.19) exhibit quite different performance characteristics, as shown in Tables 7.2 and 7.3 (typical values are given in brackets).

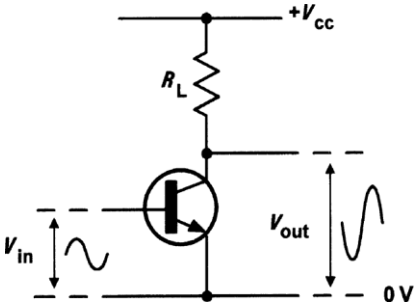


Figure 7.14 Common-emitter configuration

Figure 7.15 Common-collector (emitter follower) configuration

Figure 7.16 Common-base configuration

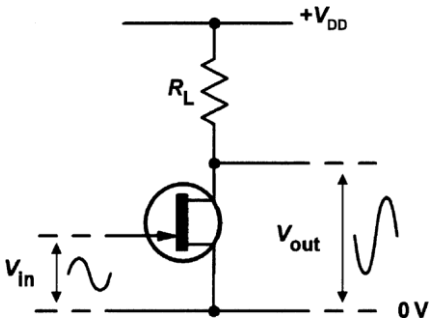


Figure 7.17 Common-source configuration

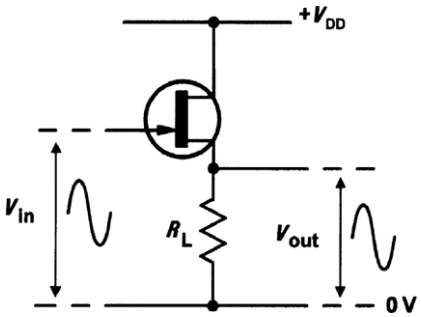


Figure 7.18 Common-drain (source follower) configuration

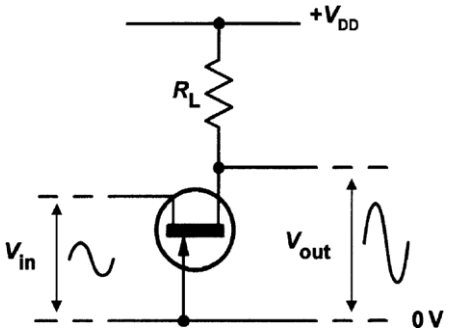


Figure 7.19 Common-gate configuration

Multi-stage amplifiers

In order to provide sufficiently large values of gain, it is frequently necessary to use a number of interconnected stages within an amplifier. The overall gain of an amplifier with several stages (i.e., a multi-stage amplifier) is simply the productof the individual voltage gains. Hence:

$$A_v = A_{v1} \times A_{v2} \times A_{v3}, \text{ etc.}$$

Note, however, that the bandwidth of a multi- stage amplifier will be less than the bandwidth ofeach individual stage. In other words, an increasein gain can only be achieved at the expense of a reduction in bandwidth. Signals can be coupled between the individual stages of a multi-stage amplifier using one of a number of different methods shown in Fig.

7.43.

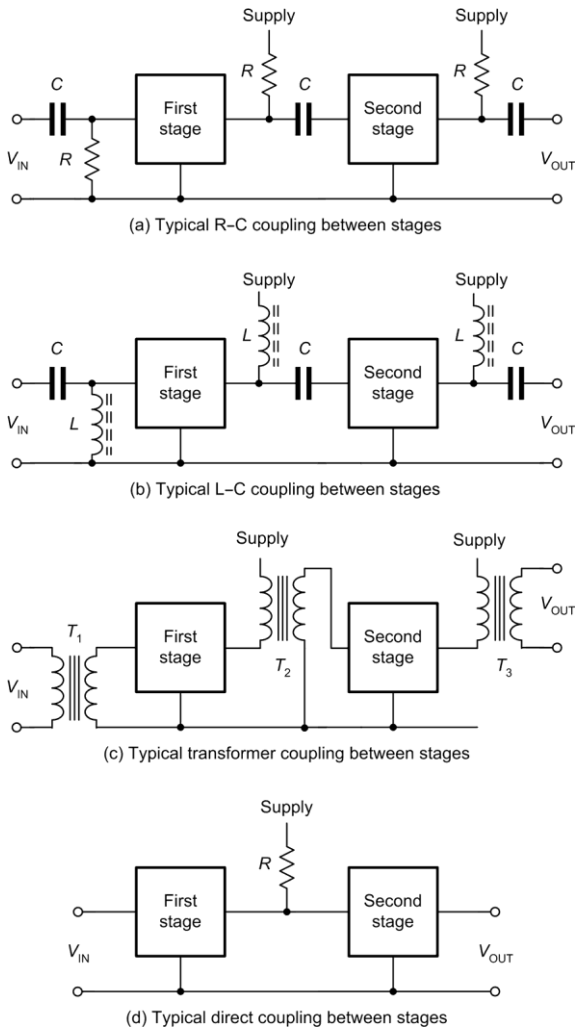


Figure 7.43 Different methods used forinterstage coupling

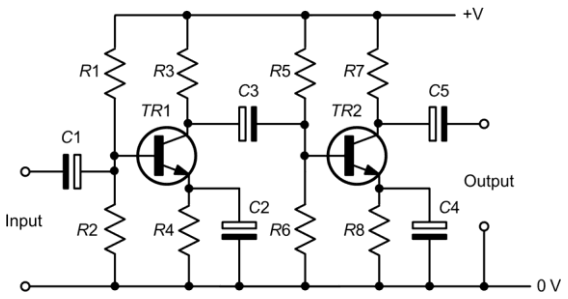


Figure 7.44 A typical two-stage high-gain *R-C* coupled common-emitter amplifier

The most commonly used method is that of ***R–C* coupling** as shown in In Fig. 7.43(a). In this coupling method, the stages are coupled togetherusing capacitors having a low reactance at the signal frequency and resistors (which also providea means of connecting the supply). Fig. 7.44 shows a practical example of this coupling method. A similar coupling method, known as ***L–C* coupling**, is shown in Fig. 7.43(b). In this method,the inductors have a high reactance at the signal frequency. This type of coupling is generally only used in RF and high-frequency amplifiers. Two further methods, **transformer coupling** and**direct coupling,** are shown in Figs 7.43(c) and 7.43(d), respectively. The latter method is used where d.c. levels present on signals must be preserved.

PROBLEMS:

7.1 The following measurements were madeduring a test on an amplifier:

V_{in} = 250 mV, I_{in} = 2.5 mA,

V_{out} = 10 V, I_{out} = 400 mA

Determine:

(a) the voltage gain;
(b) the current gain;
(c) the power gain;
(d) the input resistance.

7.2 An amplifier has a power gain of 25 andidentical input and output resistances of600 Ω. Determine the input voltage required to produce an output of 10 V.

7.3 Determine the mid-band voltage gain and upper and lower cut-off frequencies for the amplifier whose frequency response curve is shown in Fig. 7.53. Also determine the voltage gain at frequencies of:

(a) 10 Hz
(b) 1 MHz

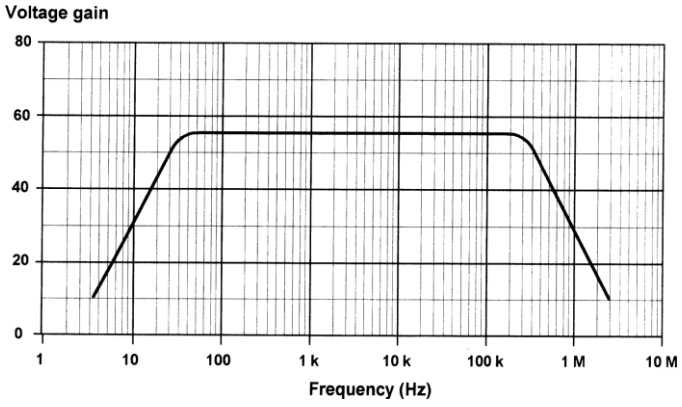


Figure 7.53 See Question 7.3

7.4 An amplifier with negative feedback applied has an open-loop voltage gain of 250, and 5% of its output is fed-back to the input. Determine the overall voltagegain with negative feedback applied. If the open-loop voltage gain increases by20% determine the new value of overallvoltage gain.

7.5 An amplifier produces an open-loop gain of 180.

Determine the amount of feedback required if it is to be operatedwith a precise voltage gain of 50.

7.6 A transistor has the following parameters:

$h_{ie} = 800\ \Omega$
h_{re} = negligible
$h_{fe} = 120$
$h_{oe} = 50\ \mu S$.

If the transistor is to be used as the basisof a common-emitter amplifier stage with $R_L = 12\ k\Omega$, determine the output voltage when an input signal of 2 mV is applied.

7.7 Determine the unknown current andvoltages in Fig. 7.54.

7.8 The output characteristics of a bipolar transistor are shown in Fig. 7.55. If this transistor is used in an amplifier circuit operating from a 12 V supply with a basebias current of 60 μA and a load resistor of 1 kΩ, determine the quiescent values

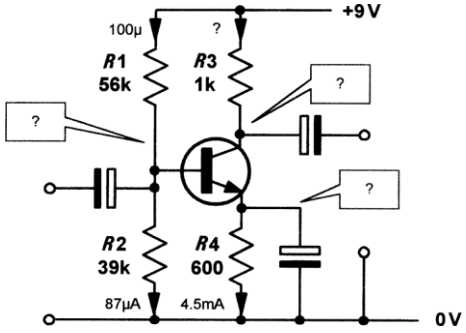


Figure 7.54 See Question 7.7

of collector-emitter voltage and collector current. Also determine the peak–peak output voltage produced when an 80 μA peak–peak signal current is applied to thebase of the transistor.

7.9 Fig. 7.56 shows a simple audio power amplifier in which all of the semiconductordevices are silicon and all three transistors have an h_{FE} of 100. If *RV*1 is adjusted to produce 4.5 V at Test Point D, determinethe base, emitter and collector currents and voltages for each transistor and thevoltages that will appear at Test Points A to C.

7.10 The output characteristics of a junctiongate field effect transistor are shown in Fig. 7.57. If this JFET is used in an amplifier circuit operating from an 18 V supply with a gate–source bias voltage of −3 V and a load resistor of 900 Ω, determine the quiescent values of drain–source voltage and drain current. Also determine the peak–peak output voltage when an input voltage of 2 V peak–peak is applied to the gate. Also determine thevoltage gain of the stage.

7.11 A multi-stage amplifier consists of two *R-C* coupled common emitter stages. If each stage has a voltage gain of 50, determine the overall voltage gain. Draw a circuit diagram of the amplifier and label your drawing clearly.

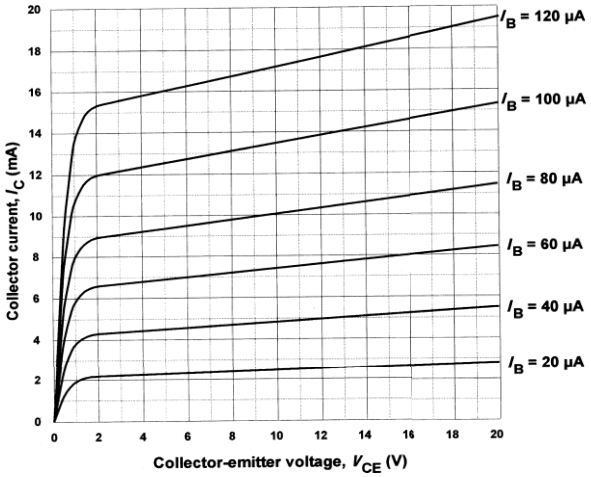


Figure 7.55 See Question 7.8

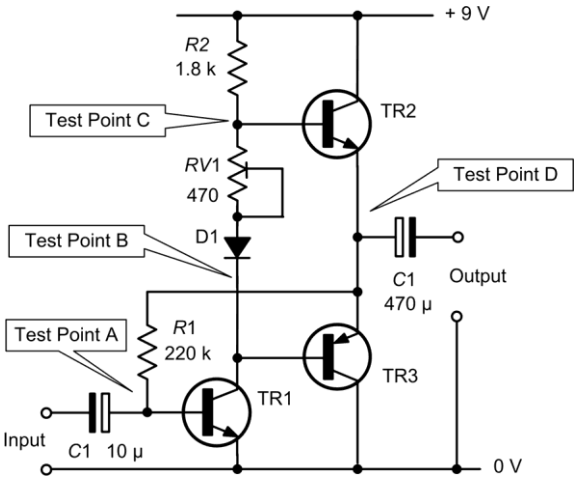


Figure 7.56 See Questions 7.9, 7.12 and 7.13

7.12 The following r.m.s. voltage measurements were made during a signaltest on the simple power amplifier shownin Fig. 7.56 when connected to a 15 Ω load:

$V_{in} = 50$ mV

$V_{out} = 2$ V

Determine:

(a) the voltage gain
(b) the output power
(c) the output current.

7.13 If the power amplifier shown in Fig. 7.56 produces a maximum r.m.s. output power of 0.25 W, determine its overall efficiencyif the supply current

is 75 mA. Also determine the power dissipated in each ofthe output transistors in this condition. Answers to these problems appear on page 417.

CHAPTER-OPERATIONAL AMPLIFIERS

Operational amplifier parameters

Before we take a look at some of the characteristics of 'ideal' and 'real' operational amplifiers it is important to define some of theterms and parameters that we apply to these devices.

Open-loop voltage gain

The open-loop voltage gain of an operational amplifier is defined as the ratio of output voltage to input voltage measured with no feedback applied. In practice, this value is exceptionally high (typically greater than 100,000) but is liable toconsiderable variation from one device to another.

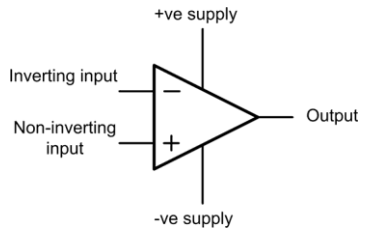


Figure 8.2 Symbol for an operational amplifier

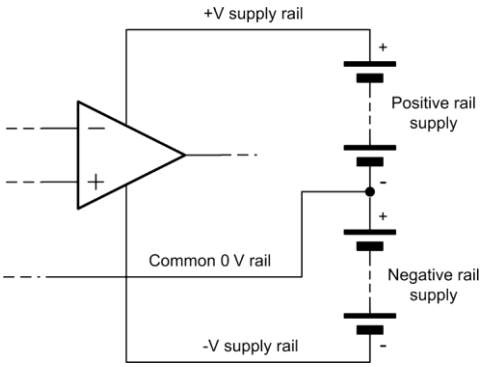


Figure 8.3 Supply connections for an operational amplifier

Open-loop voltage gain may thus be thought of as the 'internal' voltage gain of the device, thus:

$$A_{V(OL)} = \frac{V_{OUT}}{V_{IN}}$$

where $A_{V(OL)}$ is the open-loop voltage gain, V_{OUT} and V_{IN} are the output and input voltages,respectively, under open-loop conditions. In linear voltage amplifying applications, a large amount of negative feedback will normally be applied and the open-loop voltage gain can be thought of as the internal voltage gain provided by the device. The open-loop voltage gain is often expressed in **decibels** (**dB**) rather than as a ratio. In this case:

$$A_{V(OL)} = 20\log_{10}\frac{V_{OUT}}{V_{IN}}$$

Most operational amplifiers have open-loopvoltage gains of 90 dB or more.

Closed-loop voltage gain

The closed-loop voltage gain of an operationalamplifier is defined as the ratio of output voltage to input voltage measured with a smallproportion of the output fed-back to the input (i.e., with feedback applied). The effect of providing negative feedback is to reduce the loopvoltage gain to a value that is both predictable and manageable. Practical closed-loop voltage gains range from one to several thousand but note that high values of voltage gain may make unacceptable restrictions on bandwidth (see later). Closed-loop voltage gain is once again the ratio of output voltage to input voltage but with negative feedback applied, hence:

$$A_{V(CL)} = \frac{V_{OUT}}{V_{IN}}$$

where $A_{V(CL)}$ is the open-loop voltage gain, V_{OUT} and V_{IN} are the output and input voltages, respectively, under closed-loop conditions. The closed-loop voltage gain is normally very much less than theopen-loop voltage gain.

Example 8.1

An operational amplifier operating with negative feedback produces an output voltage of 2 V whensupplied with an input of 400 μV. Determine the value of closed-loop voltage gain.

Solution

Now:

$$A = \frac{V_{OUT}}{V_{IN}} V(CL)$$

Thus:

$$A_{V(CL)} = \frac{2}{400 \times 10^{-6}} = \frac{2 \times 10^{6}}{400} = 5{,}000$$

Expressed in decibels (rather than as a ratio) this is:

$$A_{V(CL)} = 20 \log_{10}(5{,}000) = 20 \times 3.7 = 74 \text{ dB}$$

Input resistance

The input resistance of an operational amplifier is defined as the ratio of input voltage to input current expressed in ohms. It is often expedientto assume that the input of an operational amplifier is purely resistive, though this is not the case at high frequencies where shunt capacitive reactance may become significant. The input resistance of operational amplifiers is very much dependent on the semiconductor technology employed. In practice values range from about 1 MΩ for common bipolar types to over 10^{12} Ω forFET and CMOS devices.

Input resistance is the ratio of input voltage to input current:

$$R_{IN} = \frac{V_{IN}}{I_{IN}}$$

where R_{IN} is the input resistance (in ohms), V_{IN} is the input voltage (in volts) and I_{IN} is the inputcurrent (in amps). Note that we usually assume that the input of an operational amplifier is purely resistive though this may not be the case at high frequencies where shunt capacitive reactance may become significant.

The input resistance of operational amplifiers is very much dependent on the semiconductortechnology employed. In practice, values range from about 2 MΩ for bipolar operational amplifiersto over 10^{12} Ω for CMOS devices.

Example 8.2

An operational amplifier has an input resistance of2 MΩ. Determine the input current when an input voltage of 5 mV is present.

Solution

Now:

$$R_{IN} = \frac{V_{IN}}{I_{IN}}$$

thus

$$I_{IN} = \frac{V_{IN}}{R_{IN}} = \frac{5 \times 10^{-3}}{2 \times 10^{6}} = 2.5 \times 10^{-9} \text{A} = 2.5 \text{ nA}$$

Output resistance

The output resistance of an operational amplifier is defined as the ratio of open-circuit output voltage to short-circuit output current expressed in ohms. Typical values of output resistance rangefrom less than 10 Ω to around 100 Ω, depending upon the configuration and amount of feedback employed. Output resistance is the ratio of open-circuit output voltage to short-circuit output current,hence:

$$R_{OUT} = \frac{V_{OUT(OC)}}{I_{OUT(SC)}}$$

where R_{OUT} is the output resistance (in ohms), $V_{OUT(OC)}$ is the open-circuit output voltage (in volts)and $I_{OUT(SC)}$ is the short-circuit output current (in amps).

Input offset voltage

An ideal operational amplifier would provide zero output voltage when 0 V difference is applied to its inputs. In practice, due to imperfect internal balance, there may be some small voltage presentat the output. The voltage that must be applied differentially to the operational amplifier input in order to make the output voltage exactly zero is known as the input offset voltage. Input offset voltage may be minimized by applyingrelatively large amounts of negative feedback or by using the offset null facility provided by a number of operational amplifier devices. Typicalvalues of input offset voltage range from 1 mV to 15 mV. Where a.c. rather than d.c. coupling is employed, offset voltage is not normally a problem and can be happily ignored.

Full-power bandwidth

The full-power bandwidth for an operational amplifier is equivalent to the frequency at which the maximum undistorted peak output voltage swing falls to 0.707 of its low-frequency (d.c.) value (the sinusoidal input voltage remaining constant). Typical full-power bandwidths range from 10 kHz to over 1 MHz for some high-speeddevices.

Slew rate

Slew rate is the rate of change of output voltagewith time, when a rectangular step input voltageis applied (as shown in Fig. 8.4). The slew rate ofan operational amplifier is the rate of change of output voltage with time in response to a perfectstep-function input. Hence:

$$\text{Slew rate} = \frac{\Delta V_{OUT}}{\Delta t}$$

where Δ V_{OUT} is the change in output voltage (in volts) and Δ t is the corresponding interval of time (in seconds). Slew rate is measured in V/s (or V/μs) and typical values range from 0.2 V/μs to over 20 V/μs. Slew rate imposes a limitation on circuits in which large amplitude pulses rather than small amplitude sinusoidal signals are likely to be encountered.

Operational amplifier characteristics

Having defined the parameters that, we use to describe operational amplifiers we shall now consider the desirable characteristics for an 'ideal'operational amplifier. These

are:

(a) The open-loop voltage gain should be very high(ideally infinite).
(b) The input resistance should be very high(ideally infinite).
(c) The output resistance should be very low(ideally zero).
(d) Full-power bandwidth should be as wide as possible.
(e) Slew rate should be as large as possible.
(f) Input offset should be as small as possible.

The characteristics of most modern integrated circuit operational amplifiers (i.e., 'real' operational amplifiers) come very close to those of an 'ideal' operational amplifier, as witnessed by the data shown in Table 8.1.

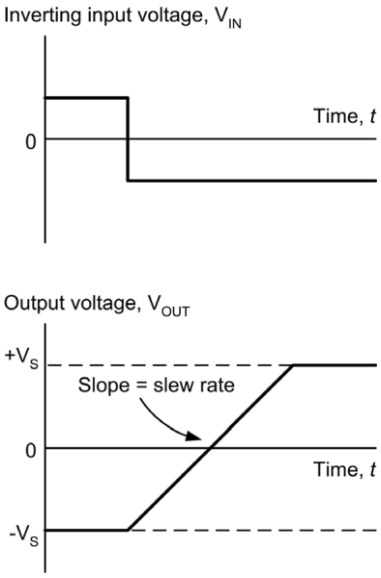


Figure 8.4 Slew rate for an operational amplifier

Table 8.1 Comparison of operational amplifierparameters for 'ideal' and 'real' devices

Parameter	Ideal	Real
Voltage gain	Infinite	100,000
Input resistance	Infinite	100 MΩ
Output resistance	Zero	20 Ω
Bandwidth	Infinite	2 MHz
Slew rate	Infinite	10 V/μs
Input offset	Zero	Less than 5 mV

Example 8.3

A perfect rectangular pulse is applied to the inputof an operational amplifier. If it takes 4 μs for the output voltage to change from –5 V to +5 V,determine the slew rate of the device.

Solution

The slew rate can be determined from:

$$\text{Slew rate} = \frac{\Delta V_{OUT}}{\Delta t} = \frac{10\text{ V}}{4\,\mu\text{s}} = 2.5\text{ V}/\mu\text{s}$$

Example 8.4

A wideband operational amplifier has a slew rate of 15 V/μs. If the amplifier is used in a circuit witha voltage gain of 20 and a perfect step input of 100 mV is applied to its input, determine the timetaken for the output to change level.

Solution

The output voltage change will be $20 \times 100 = 2{,}000$ mV (or 2 V). Re-arranging the formula forslew rate gives:

$$\Delta t = \frac{\Delta V_{OUT}}{\text{Slew rate}} = \frac{2\text{ V}}{15\text{ V}/\mu\text{s}} = 0.133\ \mu\text{s}$$

Operational amplifier configurations

The three basic configurations for operational voltage amplifiers, together with the expressions for their voltage gain, are shown in Fig. 8.7. Supply rails have been omitted from these diagrams for clarity but are assumed to be symmetrical about 0 V. All of the amplifier circuits described previously have used direct coupling and thus have frequency response characteristics that extend to d.c. This, of course, is undesirable for many applications, particularly where a wanted a.c. signal may be superimposed on an unwanted d.c. voltage level or when the bandwidth of the amplifier greatly exceeds that of the signal that it is required to amplify. In such cases, capacitors of appropriate value may be inserted in series with the input resistor, R_{IN}, and in parallel with the feedback resistor, R_F, as shown in Fig. 8.8. The value of the input and feedback capacitors, C_{IN} and C_F respectively, are chosen so as to roll off the frequency response of the amplifier at the desired lower and upper cut-off frequencies, respectively. The effect of these two capacitors on an operational amplifier's frequency response is shown in Fig. 8.9. By selecting appropriate values of capacitor, the frequency response of an inverting operational voltage amplifier may be very easily tailored to suit a particular set of requirements. The lower cut-off frequency is determined by the value of the input capacitance, C_{IN}, and input resistance, R_{IN}. The lower cut-off frequency is given by:

$$f_1 = \frac{1}{2\pi C_{IN} R_{IN}} = \frac{0.159}{C_{IN} R_{IN}}$$

where f_1 is the lower cut-off frequency in hertz, C_{IN} is in farads and R_{IN} is in ohms. Provided the upper frequency

response it notlimited by the gain × bandwidth product, the upper cut-off frequency will be determined by the feedback capacitance, C_F, and feedback resistance, R_F, such that:

$$f_2 = \frac{1}{2\pi C_F R_F} = \frac{0.159}{C_F R_F}$$

where f_2 is the upper cut-off frequency in hertz, C_F is in farads and R_2 is in ohms.

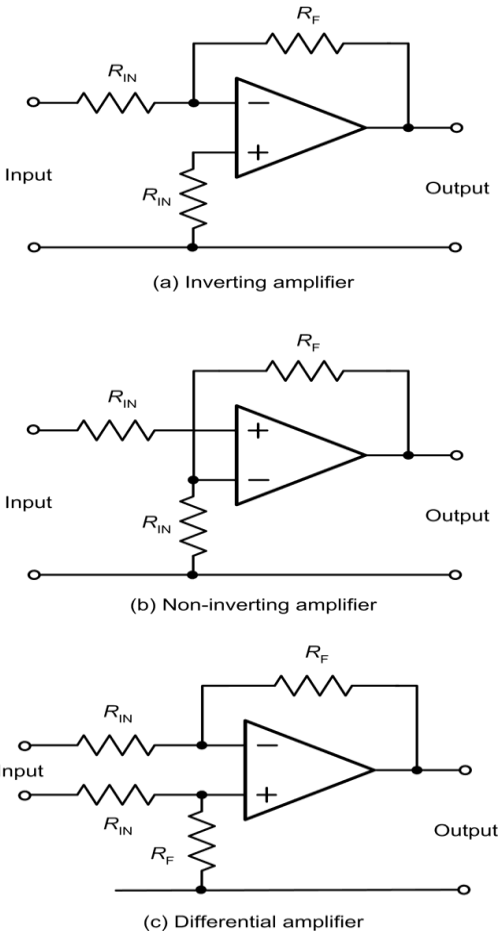


Figure 8.7 The three basic configurations foroperational voltage amplifiers

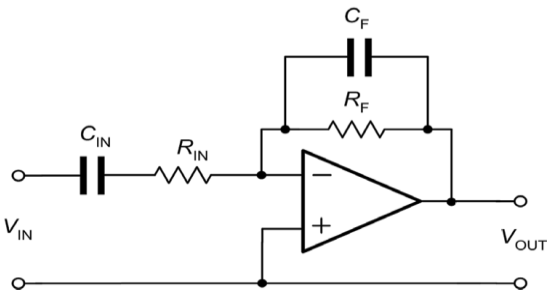


Figure 8.8 Adding capacitors to modify the frequency response of an inverting operationalamplifier

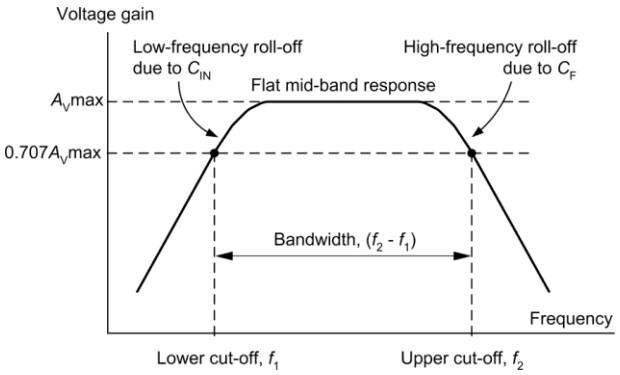


Figure 8.9 Effect of adding capacitors, C_{IN} andC_F, to modify the frequency response of an operational amplifier

Example 8.6

An inverting operational amplifier is to operateaccording to the following specification:

Voltage gain = 100
Input resistance (at mid-band) = 10 kΩLower cut-off frequency = 250 Hz Upper cut-off frequency = 15 kHz

Devise a circuit to satisfy the above specificationusing an operational amplifier.

Solution

To make things a little easier, we can break the problem down into manageable parts. Weshall base our circuit on a single operational amplifier configured as an inverting amplifier withcapacitors to define the upper and lower cut-off frequencies, as shown in Fig. 8.9.

The nominal input resistance is the same as thevalue for R_{IN}. Thus:

$R_{IN} = 10\ k\Omega$

To determine the value of R_F we can make use ofthe formula for mid-band voltage gain:

$$A_v = \frac{R2}{R1}$$

thus R2 = Av× R1 = 100 × 10 kΩ = 100 kΩ

To determine the value of C_{IN} we will use the formula for the low-frequency cut-off:

$$f_1 = \frac{0.159}{C_{IN} R_{IN}}$$

hence:

$$C_{IN} = \frac{0.159}{2.5 \times 10^6} = 63 \times 10^{-9} F = 63\ nF$$

Finally, to determine the value of C_F we will use the

formula for high-frequency cut-off:

$$f_2 = \frac{0.159}{C_F R_F}$$

from which:

$$C_F = \frac{0.159}{f_2 R_{IN}} = \frac{0.159}{15 \times 10^3 \times 100 \times 10^3}$$

hence:

$$C_F = \frac{0.159}{1.5 \times 10^9} = 0.106 \times 10^{-9} \text{F} = 106 \text{ pF}$$

For most applications the nearest preferred values (68 nF for C_{IN} and 100 pF for C_F) would be perfectly adequate. The complete circuit of the operational amplifier stage is shown in Fig. 8.10.

Operational amplifier circuits

As well as their application as a general-purpose amplifying device, operational amplifiers have a number of other uses, including voltage followers, differentiators, integrators, comparators and summing amplifiers. We shall conclude this section by taking a brief look at each of these applications.

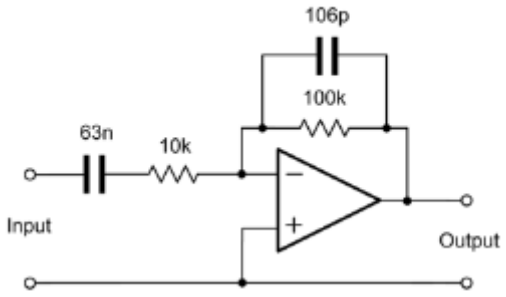


Figure 8.10 See Example 8.6. This operationalamplifier has a mid-band voltage gain of 10 overthe frequency range 250 Hz to 15 kHz

Voltage followers

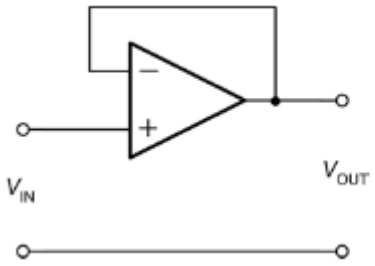


Figure 8.11 A voltage follower

A voltage follower using an operational amplifier is shown in Fig. 8.11. This circuit is essentially an inverting amplifier in which 100% of the output is fed back to the input. The result is an amplifier that has a voltage gain of 1 (i.e., unity), a very high input resistance and a very high output resistance. This stage is often referred to as a buffer and is used for matching a high-impedance circuit to a low-impedance circuit. Typical input and output waveforms for a voltage follower are shown in Fig. 8.12. Notice how the input and output waveforms are both in-phase (they rise and fall together) and that they are identical in amplitude.

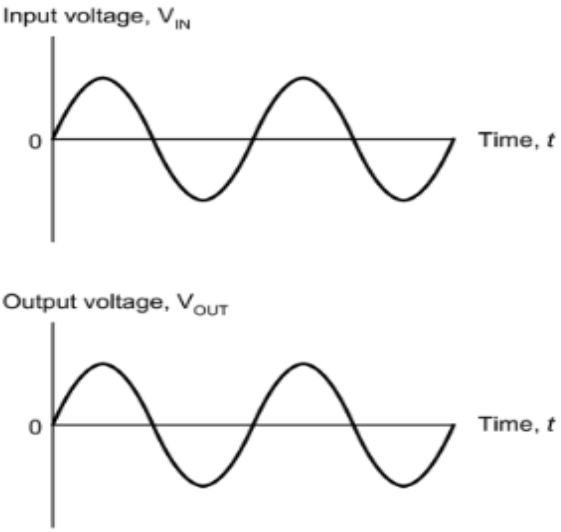


Figure 8.12 Typical input and output waveformsfor a voltage follower

Differentiators

A differentiator using an operational amplifier is shown in Fig. 8.13. A differentiator produces an output voltage that is equivalent to the rate of change of its input. This may sound a little complex but it simply means that if the input voltage remains constant (i.e., if it isn't changing) the output also remains constant. The faster the input voltage changes the greater will the output be. In mathematics this is equivalent to the differential function. Typical input and output waveforms for a differentiator is shown in Fig. 8.14. Notice how the square wave input is converted to a train of short duration pulses at the output. Note also that the output waveform is inverted because the signal has been applied to the inverting input of the operational amplifier.

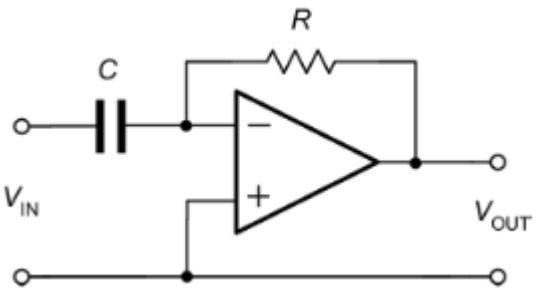


Figure 8.13 A differentiator

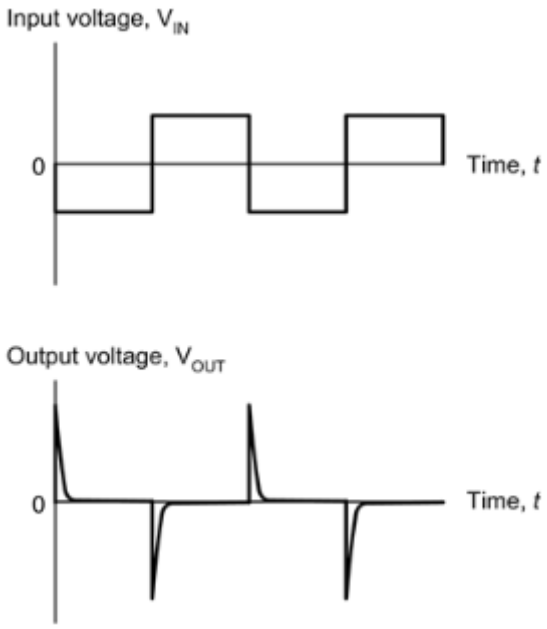


Figure 8.14 Typical input and output waveformsfor a differentiator

Integrators

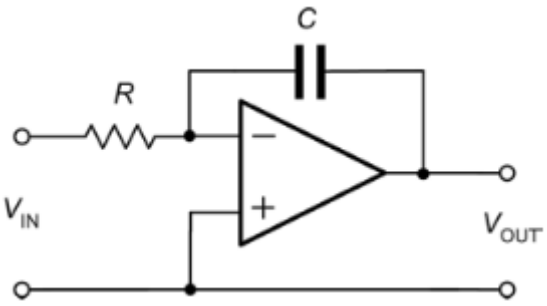


Figure 8.15 An integrator

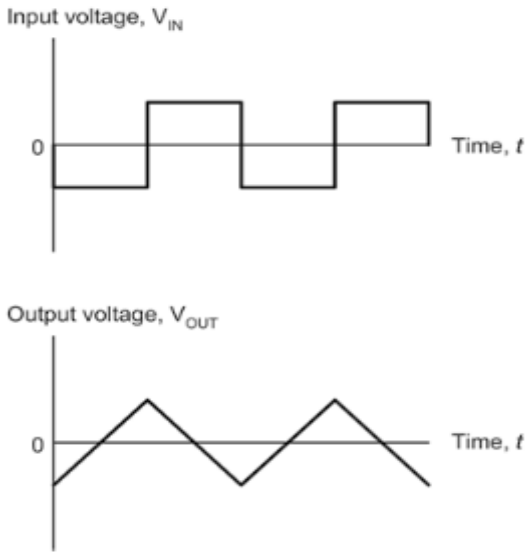


Figure 8.16 Typical input and output waveformsfor an integrator

An integrator using an operational amplifier is shown in Fig. 8.15. This circuit provides the opposite function to that of a differentiator (see earlier) in that its output is equivalent to the are under the graph of the input function rather than its rate of change. If the input voltage remains constant (and is other than 0 V) the output voltage will ramp up or down according to the polarity of the input. The longer the input voltage remains at a particular value the larger the value of output voltage (of either polarity) will be produced.

Typical input and output waveforms for an integrator are shown in Fig. 8.16. Notice how the square wave input is converted to a wave that has a triangular shape. Once again, note that the output waveform is inverted.

Comparators

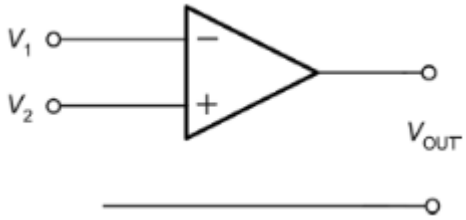


Figure 8.17 A comparator

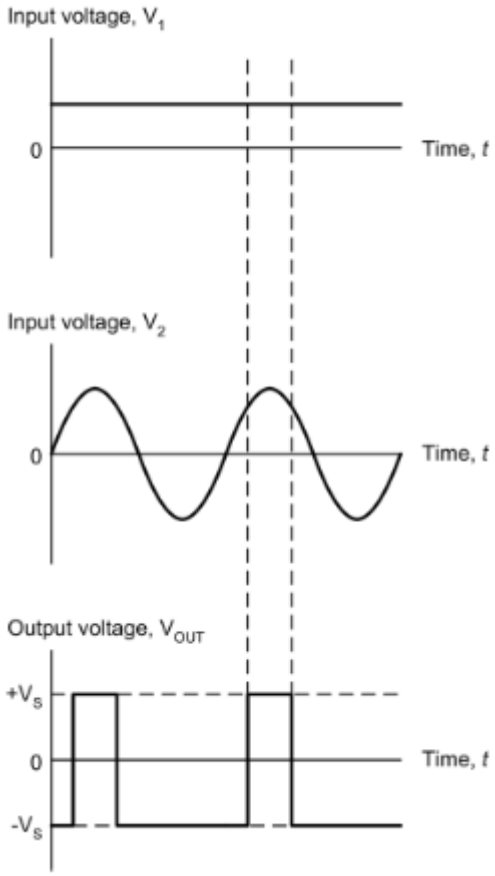


Figure 8.18 Typical input and output waveformsfor a comparator

A comparator using an operational amplifier is shown in Fig. 8.17. Since no negative feedback has been applied, this circuit uses the maximum gain of the operational amplifier.

The output voltage produced by the operational amplifier will thus rise to the maximum possible value (equal to the positive supply rail voltage) whenever the voltage present at the non-inverting input exceeds that present at the inverting input. Conversely, the output voltage produced by the operational amplifier will fall to the minimum possible value (equal to the negative supply rail voltage) whenever the voltage present at the inverting input exceeds that present at the non-inverting input. Typical input and output waveforms for a comparator are shown in Fig. 8.18. Notice how the output is either +15 V or –15 V depending on the relative polarity of the two inputs. A typical application for a comparator is that of comparing a signal voltage with a reference voltage. The output will go high (or low) in order to signal the result of the comparison.

Summing amplifiers

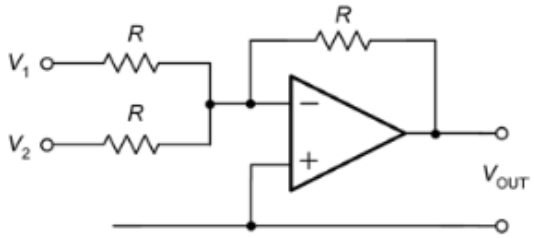


Figure 8.19 A summing amplifier

A summing amplifier using an operational amplifier is shown in Fig. 8.19. This circuit produces an output that is the sum of its two input voltages. However, since the operational amplifier is connected in inverting mode, the output voltage is given by:

$$V_{OUT} = -(V_1 + V_2)$$

where V1 and V2 are the input voltages (note that all of the resistors used in the circuit have the same value). Typical input and output waveforms for a summing amplifier are shown in Fig. 8.20. A typical application is that of 'mixing' two input signals to produce an output voltage that is the sum of the two.

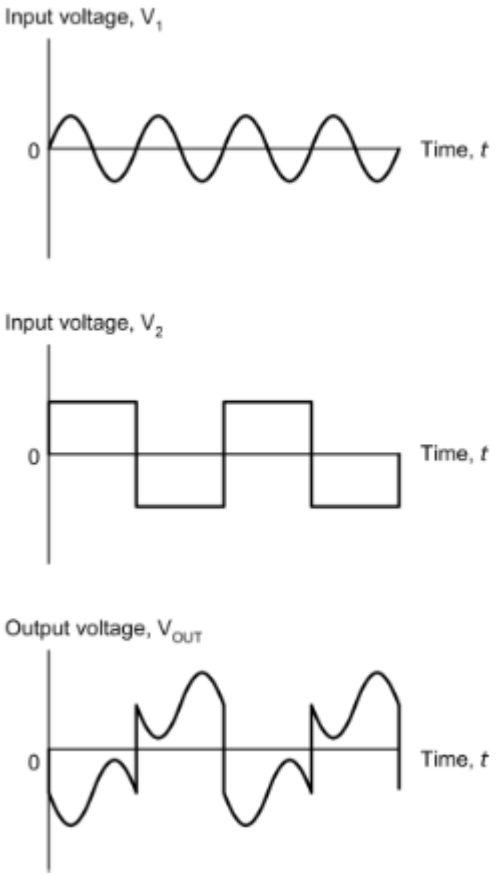


Figure 8.20 Typical input and output waveformsfor a summing amplifier

Multi-stage amplifiers

Multi-stage amplifiers can easily be produced using operational amplifiers. Coupling methods can be broadly similar to those described earlier in Chapter 7 (see page 152). As an example, Fig. 8.21 shows a two-stage amplifier in which each stage has a tailored frequency response. Note how C1 and C3 provide d.c. isolation between the stages as well as helping to determine the low-frequency roll-off.

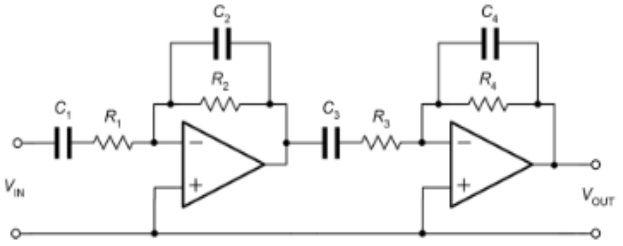


Figure 8.21 A multi-stage amplifier (both stageshave tailored frequency responses)

PROBLEMS:

8.1 Sketch the circuit symbol for an operational amplifier. Label each of theconnections.

8.2 List four characteristics associated withan 'ideal' operational amplifier.

8.3 An operational amplifier with negative feedback applied produces an output of 1.5 V when an input of 7.5 mV is present. Determine the close loop open gain

8.4 Sketch the circuit of an inverting amplifierbased on an operational amplifier. Label your circuit and identify the components that determine the close-loop voltage gain.

8.5 Sketch the circuit of each of the following based on the use of operational amplifiers:

a) a comparator

b) a differentiator

c) an integrator

8.6 An inverting amplifier is to be constructedhaving a mid-band voltage gain of 40, an input resistance of 5 kΩ and a frequency response extending from 20 Hz to 20 kHz.Devise a circuit and specify all componentvalues required.

8.7 A summing amplifier with two inputs has $R_F = 10$ kΩ, and R_{IN} (for both inputs)of 2 kΩ. Determine the output voltage when one input is at -2 V and the other is $+0.5$ V.

8.8 During measurements on an operationalamplifier under open-loop conditions, anoutput voltage of 12 V is produced by an input voltage of 1 mV. Determine theopen-loop voltage gain expressed in dB.

8.9 With the aid of a sketch, explain what is meant by the term 'slew rate'. Why is thisimportant?

CHAPTER- OSCILLATORS

Positive feedback

In Chapter 7 we showed how negative feedback can be applied to an amplifier to form the basis ofa stage which has a precisely controlled gain. An alternative form of feedback, where the output isfed back in such a way as to reinforce the input (rather than to subtract from it), is known as positive feedback. Fig. 9.1 shows the block diagram of an amplifier stage with positive feedback applied. Note that the amplifier provides a phase shift of 180° andthe feedback network provides a further 180°. Thus, the overall phase shift is 0°. The overall voltage gain, *G*, is given by:

$$\text{Overall gain, } G = \frac{V_{out}}{V_{in}}$$

By applying Kirchhoff's Voltage Law

$$V_{in}' = V_{in} + \beta V_{out}$$

thus

$$V_{in} = V_{in}' - \beta V_{out}$$

and

$$V_{out} = A_v \times V_{in}$$

where *A*v is the internal gain of the amplifier.Hence:

$$\text{Overall gain, } G = \frac{A_v \times V_{in}'}{V_{in}' - \beta V_{out}} = \frac{A_v \times V_{in}'}{V_{in}' - \beta(A_v \times V_{in}')}$$

$$\text{Thus, } G = \frac{A_v}{1 - \beta A_v}$$

Now consider what will happen when the loop gain, βA_v, approaches unity (i.e., when the loop gain is just less than 1). The denominator $(1 - \beta A_v)$will become close to zero. This will have the effect of *increasing* the overall gain, i.e., the overall gain with positive feedback applied will be *greater* than the gain without feedback. It is worth illustrating this difficult concept using some practical figures. Assume that you have an amplifier with a gain of 9 and one-tenth of the output is fed back to the input (i.e., $\beta = 0.1$). In thiscase the loop gain ($\beta \times A_v$) is 0.9. With negative feedback applied (see Chapter 7)the overall voltage gain will be:

$$G = \frac{A_v}{1+\beta A_v} = \frac{9}{1+(0.1\times 9)} = \frac{9}{1+0.9} = \frac{9}{1.9} = 4.7$$

With positive feedback applied the overall voltage gain will be:

$$G = \frac{A_v}{1-\beta A_v} = \frac{10}{1-(0.1\times 9)} = \frac{10}{1-0.9} = \frac{10}{0.1} = 90$$

Now assume that you have an amplifier with a gain of 10 and, once again, one-tenth of the output is fed back to the input (i.e., $\beta = 0.1$). In thisexample the loop gain ($\beta \times A_V$) is exactly 1. With negative feedback applied (see Chapter 7) the overall voltage gain will be:

$$G = \frac{A_v}{1+\beta A_v} = \frac{10}{1+(0.1\times 10)} = \frac{10}{1+1} = \frac{10}{2} = 5$$

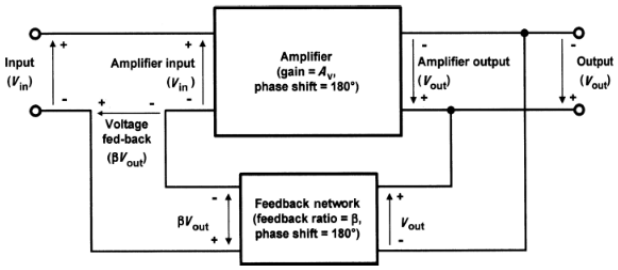


Figure 9.1 Amplifier with positive feedback applied With positive feedback applied the overall voltagegain will be:

$$G = \frac{A_v}{1-\beta A_v} = \frac{10}{1-(0.1\times 10)} = \frac{10}{1-1} = \frac{10}{0} = \infty$$

This simple example shows that a loop gain of unity (or larger) will result in infinite gain and an amplifier which is unstable. In fact, the amplifier will oscillate since any disturbance will be amplified and result in an output. Clearly, as far as an amplifier is concerned, positive feedback may have an undesirable effect – instead of reducing the overall gain the effect is that of reinforcing any signal present and the output can build up into continuous oscillation if the loop gain is 1 or greater. To put this anotherway, oscillator circuits can simply be thought of as amplifiers that generate an output signal without the need for an input!

Conditions for oscillation

From the foregoing we can deduce that theconditions for oscillation are:

(a) the feedback must be positive (i.e., the signal fed back must arrive back in-phase with the signal at the input);

(b) the overall loop voltage gain must be greaterthan 1 (i.e., the amplifier's gain must be sufficient to overcome the losses associatedwith any frequency selective feedback network).

Hence, to create an oscillator we simply need an amplifier with sufficient gain to overcome the losses of the network that provide positive feedback. Assuming that the amplifier provides 180° phase shift, the frequency of oscillation will be that at which there is 180° phase shift in the feedback

network.

A number of circuits can be used to provide 180°phase shift, one of the simplest being a three- stage *C–R* ladder network that we shall meet next. Alternatively, if the amplifier produces 0° phase shift, the circuit will oscillate at the frequency at which the feedback network produces 0° phase shift. In both cases, the essential point is that the feedback should be

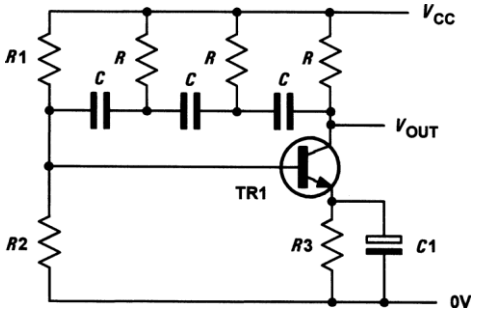


Figure 9.2 Sine wave oscillator based on a three-stage *C–R* ladder network

positive so that the output signal arrives back at the input in such a sense as to reinforce theoriginal signal.

Ladder network oscillator

A simple phase-shift oscillator based on a three- stage *C–R* ladder network is shown in Fig. 9.2. TR1 operates as a conventional common-emitteramplifier stage with *R*1 and *R*2 providing base bias potential and *R*3 and *C*1 providing emitter stabilization.

The total phase shift provided by the *C–R* laddernetwork (connected between collector and base) is 180° at the frequency of oscillation. Thetransistor provides the other 180° phase shift in order to realize an overall phase shift of 360° or 0°(note that these are the same). The frequency of oscillation of the circuit shownin Fig. 9.2 is given by:

$$f = \frac{1}{2\pi \times \sqrt{6}CR}$$

The loss associated with the ladder network is 29,thus the amplifier must provide a gain of *at least* 29 in order for the circuit to oscillate. In practice this is easily achieved with a single transistor.

Example 9.1

Determine the frequency of oscillation of a three-stage ladder network oscillator in which $C = 10$ nF and $R = 10$ kΩ.

Solution

Using

$$f = \frac{1}{2\pi \times \sqrt{6}CR}$$

gives

$$f = \frac{1}{6.28 \times 2.45 \times 10 \times 10^{-9} \times 10 \times 10^{3}}$$

from which

$$f = \frac{1}{6.28 \times 2.45 \times 10^{-4}} = \frac{10^{4}}{15.386} = 647 \text{ Hz}$$

Wien bridge oscillator

An alternative approach to providing the phase shift required is the use of a Wien bridge network (Fig. 9.3). Like the *C-R* ladder, this network provides a phase shift which varies withfrequency. The input signal is applied to A and B while the output is taken from C and D. At one particular frequency, the phase shift produced by the network will be exactly zero (i.e., the input andoutput signals will be in-phase). If we connect thenetwork to an amplifier producing 0° phase shift which has sufficient gain to overcome the losses of the Wien bridge, oscillation will result. The minimum amplifier gain required to sustain oscillation is given by:

$$A_v = 1 + \frac{C1}{C2} + \frac{R2}{R1}$$

In most cases, $C1 = C2$ and $R1 = R2$, hence theminimum amplifier gain will be 3.

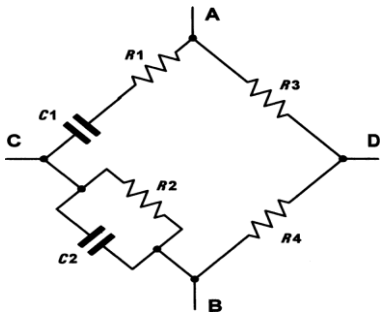


Figure 9.3 A Wien bridge network

The frequency at which the phase shift will bezero is given by:

$$f = \frac{1}{2\pi \times \sqrt{C1\,C2\,R1\,R2}}$$

When $R1 = R2$ and $C1 = C2$ the frequency at which the phase shift will be zero will be given by:

$$f = \frac{1}{2\pi \times \sqrt{C^2R^2}} = \frac{1}{2\pi CR}$$

where $R = R1 = R2$ and $C = C1 = C2$.

Example 9.2

Fig. 9.4 shows the circuit of a Wien bridge oscillator based on an operational amplifier. If $C1 = C2 = 100$ nF, determine the output frequencies produced by this arrangement (a) when $R1 = R2 = 1$ kΩ and (b) when $R1 = R2 = 6$ kΩ.

Solution

(a) When $R1 = R2 = 1$ kΩ

$$f = \frac{1}{2\pi CR}$$

where $R = R1 = R1$ and $C = C1 = C2$.

Thus

$$f = \frac{1}{6.28 \times 100 \times 10^{-9} \times 1 \times 10^{3}}$$

$$f = \frac{10^{4}}{6.28} = 1.59 \text{ kHz}$$

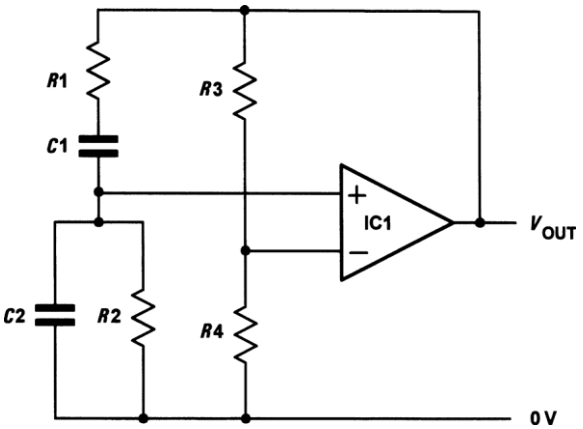


Figure 9.4 Sine wave oscillator based on a Wienbridge network (see Example 9.2)

(b) when $R1 = R1 = 6$ kΩ

$$f = \frac{1}{2\pi CR}$$

where $R = R1 = R1$ and $C = C1 = C2$.

Thus

$$f = \frac{1}{6.28 \times 100 \times 10^{-9} \times 6 \times 10^{3}}$$

$$f = \frac{10^{4}}{37.68} = 265 \text{ Hz}$$

Multivibrators

There are many occasions when we require a square wave output from an oscillator rather than a sine wave output.

Multivibrators are a family of oscillator circuits that produce output waveforms consisting of one or more rectangular pulses. The term 'multivibrator' simply originates from the factthat this type of waveform is rich in harmonics (i.e., 'multiple vibrations').

Multivibrators use regenerative (i.e., positive) feedback; the active devices present within the oscillator circuit being operated as switches, beingalternately cut-off and driven into saturation.

The principal types of multivibrators are:

(a) astable multivibrators that provide a continuous train of pulses (these are sometimes also referred to as free-runningmultivibrators);

(b) monostable multivibrators that produce a single output pulse (they have one stable stateand are thus sometimes also referred to as 'one-shot');

(c) bistable multivibrators that have two stablestates and require a trigger pulse or control signal to change from one state to another.

The astable multivibrator

Fig. 9.6 shows a classic form of astable multivibrator based on two transistors. Fig. 9.7 shows how this circuit can be redrawn in an arrangement that more closely resembles a two- stage common-emitter amplifier with its output connected back to its input. In Fig. 9.6, the valuesof the base resistors, $R3$ and $R4$, are such that the sufficient base

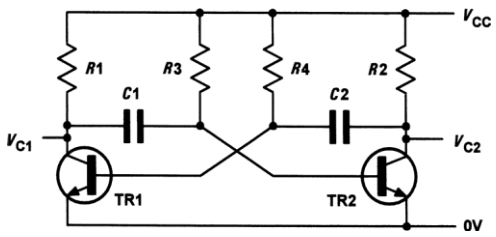


Figure 9.6 Astable multivibrator using BJTs

current will be available to completely saturate the respective transistor. The values of the collector load resistors, $R1$ and $R2$, are very much smaller than $R3$ and $R4$. When power is first applied to the circuit, assume that TR2 saturates before TR1 when the power is firstapplied (in practice one transistor would always saturate before the other due to variations in component tolerances and transistor parameters).

As TR2 saturates, its collector voltage will fall rapidly from $+V_{CC}$ to 0 V. This drop in voltage willbe transferred to the base of TR1 via $C1$. This negative-going voltage will ensure that TR1 is initially placed in the non-conducting state. As long as TR1 remains cut-off, TR2 will continue to be saturated. During this time, $C1$ will charge via$R4$ and TR1's base voltage will rise exponentially from $-V_{CC}$ towards $+V_{CC}$. However, TR1's base voltage will not rise much above

0 V because, as soon as it reaches +0.7 V (sufficient to cause

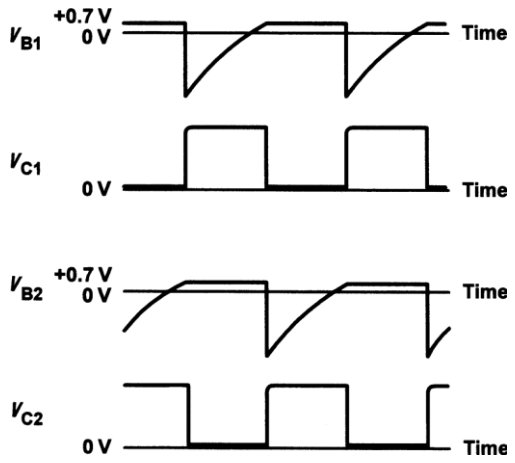


Figure 9.7 Circuit of Fig. 9.6 redrawn to showtwo common-emitter amplifier stages with positive feedback

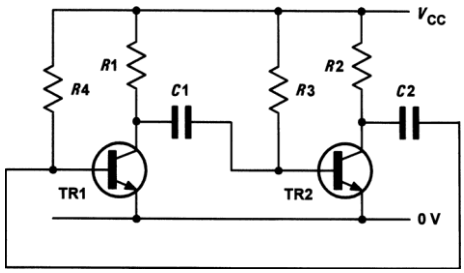


Figure 9.8 Waveforms for the BJT multivibratorshown in Fig. 9.6

base current to flow), TR1 will begin to conduct. As TR1 begins to turn on, its collector voltage will rapidly fall from $+V_{CC}$ to 0 V. This fall in voltage is transferred to the base of TR2 via $C1$ and, as a consequence, TR2 will turn off. $C1$ will then charge via $R3$ and TR2's base voltage will rise exponentially from $-V_{CC}$ towards $+V_{CC}$. As before,TR2's base voltage will not rise much above 0 V because, as soon as it reaches +0.7 V (sufficient to cause base current to flow), TR2 will start to conduct. The cycle is then repeated indefinitely.

The time for which the collector voltage of TR2 is low and TR1 is high ($T1$) will be determined bythe time constant, $R4 \times C1$. Similarly, the time for which the collector voltage of TR1 is low and TR2 is high ($T2$) will be determined by the timeconstant, $R3 \times C1$.

The following approximate relationships apply:

$$T1 = 0.7\,C2\,R4 \quad \text{and} \quad T2 = 0.7\,C1\,R3$$

Since one complete cycle of the output occurs in a time, $T = T1 + T2$, the periodic time of theoutput is given by:

$$T = 0.7\,(C2\,R4 + C1\,R3)$$

Finally, we often require a symmetrical **square wave** output where $T1 = T2$. To obtain such an output, we should make $R3 = R4$ and $C1 = C2$, inwhich case the periodic time of the output will begiven by:

$$T = 1.4\,C\,R$$

where $C = C1 = C2$ and $R = R3 = R4$. Waveformsfor the astable oscillator are shown in Fig. 9.8.

Example 9.3

The astable multivibrator in Fig. 9.6 is requiredto produce a square wave output at 1 kHz.
Determine suitable values for $R3$ and $R4$ if $C1$and $C2$ are both 10 nF.

Solution

Since a square wave is required and $C1$ and $C2$have identical values, $R3$ must be made equal to $R4$. Now:

$$T = \frac{1}{f} = \frac{1}{1\times10^{3}} = 1\times10^{-3}\ \text{s}$$

Re-arranging $T = 1.4CR$ to make R the subject gives:

$$R = \frac{T}{1.4C} = \frac{1\times10^{-3}}{1.4\times10\times10^{-9}} = \frac{1\times10^{6}}{14} = 0.071\times10^{6}$$

hence

$$R = 71\times10^{3} = 71\ \text{k}\Omega$$

Single-stage astable oscillator

A simple form of astable oscillator that produces a square wave output can be built using just one operational amplifier, as shown in Fig. 9.10. The circuit employs positive feedback with the output fed back to the non-inverting input via the potential

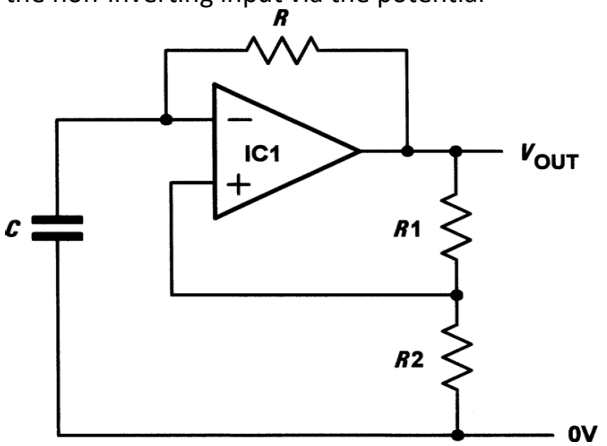


Figure 9.10 Single-stage astable oscillator usingan operational amplifier

divider formed by *R*1 and *R*2. This circuit canmake a very simple square wave source witha frequency that can be made adjustable by replacing *R* with a variable or preset resistor. Assume that *C* is initially uncharged and the voltage at the inverting input is slightly less than the voltage at the non-inverting input. The output voltage will rise rapidly to $+V_{CC}$ and the voltage atthe inverting input will begin to rise exponentiallyas capacitor *C* charges through *R*.

Eventually the voltage at the inverting input will have reached a value that causes the voltage at the inverting input to exceed that present at the non-inverting input. At this point, the output voltage will rapidly fall to −VCC. Capacitor C will then start to charge in the other direction and the voltage at the inverting input will begin to fall exponentially.

Eventually, the voltage at the inverting input will have reached a value that causes the voltage at the inverting input to be less than that present at the non-inverting input. At this point, the output voltage will rise rapidly to +VCC once again and the cycle will continue indefinitely. The upper threshold voltage (i.e., the maximum positive value for the voltage at the inverting input) will be given by:

$$V_{UT} = V_{CC} \times \left(\frac{R2}{R1+R2} \right)$$

The lower threshold voltage (i.e., the maximumnegative value for the voltage at the inverting input) will be given by:

$$V_{LT} = -V_{CC} \times \left(\frac{R2}{R1+R2} \right)$$

Finally, the time for one complete cycle of the output waveform produced by the astable oscillator is given by:

$$T = 2CR \ln\left(1+2\left(\frac{R2}{R1}\right)\right)$$

Crystal controlled oscillators

A requirement of some oscillators is that they accurately maintain an exact frequency of oscillation. In such cases, a quartz crystal can be used as the frequency determining element. The quartz crystal (a thin slice of quartz in a hermetically sealed enclosure, see Fig. 9.11)
vibrates whenever a potential difference is appliedacross its faces (this phenomenon is known as the piezoelectric effect). The frequency of oscillation is determined by the crystal's 'cut' andphysical size.
Most quartz crystals can be expected to stabilize the frequency of oscillation of a circuitto within a few parts in a million. Crystals can be manufactured for operation in **fundamentalmode** over a frequency range extending from 100 kHz to around 20 MHz and for **overtone** operation from 20 MHz to well over 100 MHz Fig. 9.12 shows a simple crystal oscillator circuit in which the crystal provides feedback from the drain to the source of a junction gate FET.

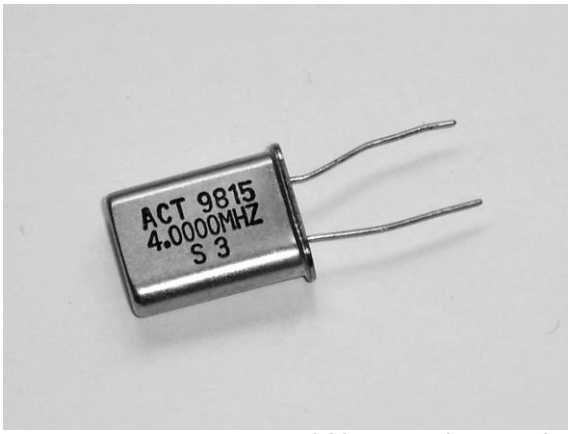


Figure 9.11 A quartz crystal (this crystal is cut tobe resonant at 4 MHz and is supplied in an HC18wire-ended package)

PROBLEMS:

9.1 An amplifier with a gain of 8 has 10% of its output fed back to the input. Determine the gain of the stage (a) withnegative feedback, (b) with positive feedback.

9.2 A phase-shift oscillator is to operate with an output at 1 kHz. If the oscillator is based on a three-stage ladder network, determine the required values of resistance if three capacitors of 10 nF areto be used.

9.3 A Wien bridge oscillator is based on the circuit shown in Fig. 9.4 but *R*1 and *R*2 arereplaced by a dual-gang potentiometer. If *C*1 = *C*2 = 22 nF, determine the values of *R*1 and *R*2 required to produce an output at exactly 400 Hz.

9.4 Determine the peak–peak voltage developed across *C*1 in the oscillatorcircuit shown in Fig. 9.22.

9.5 Determine the periodic time and frequency of the output signal produced by the oscillator circuit shown in Fig. 9.22.

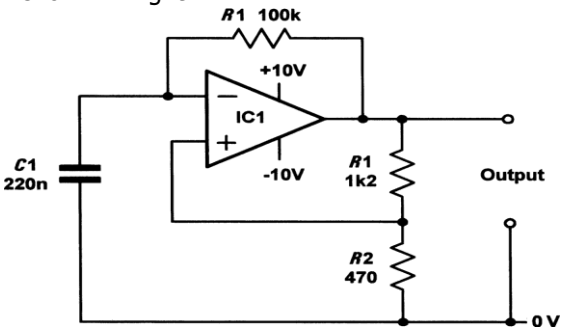


Figure 9.22 See Questions 9.4 and 9.5.

9.6 An astable multivibrator circuit is required to produce an asymmetrical rectangular output which has a period of 4 ms and is to be 'high' for 1 ms and 'low' for 3 ms. If the timing capacitors are both to be 100 nF, determine the values of the two-timing resistors required.

9.7 Explain, briefly, how the astable multivibrator shown in Fig. 9.23 operates. Illustrate your answer using a waveform sketch.

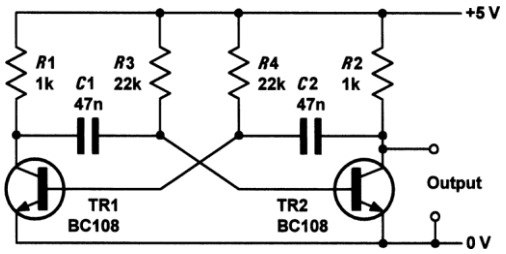


Figure 9.23 See Questions 9.7 and 9.8.

9.8 Determine the output frequency of the signal produced by the circuit shown in Fig. 9.23.

9.9. Explain, briefly, how the Wien bridge oscillator shown in Fig. 9.24 operates. What factors affect the choice of values for $R3$ and $R4$?

9.10 Determine the output frequency of the signal produced by the circuit shown in Fig. 9.24.

9.11 Sketch the circuit of an oscillator that will produce a triangular waveform output. Explain briefly how the circuit operates and suggest a means of varying the output frequency over a limited range.

9.12 Distinguish between the following types of mulitivibrator circuit:

(a) astable multivibrators, (b) monostable multivibrators, (c) bistable multivibrators.

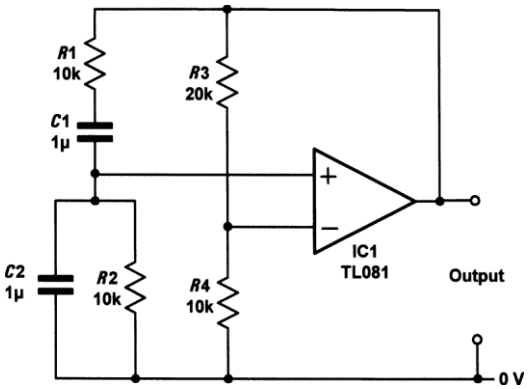


Figure 9.24 See Questions 9.9 and 9.10.

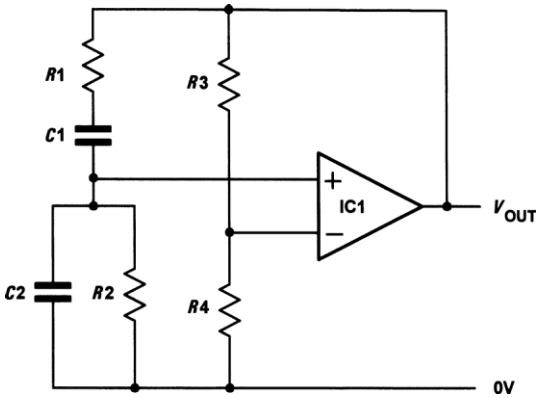


Figure 9.25 See Question 9.13

9.13 Derive an expression (in terms of $R3$ and $R4$) for the minimum value of voltage gain required to produce oscillation in the circuit shown in Fig. 9.25

9.14 Design an oscillator circuit that will generate the output waveform shown in Fig. 9.26. Sketch a circuit diagram for the oscillator and specify all component values (including supply voltage). Give reasons for your choice of oscillator circuit.

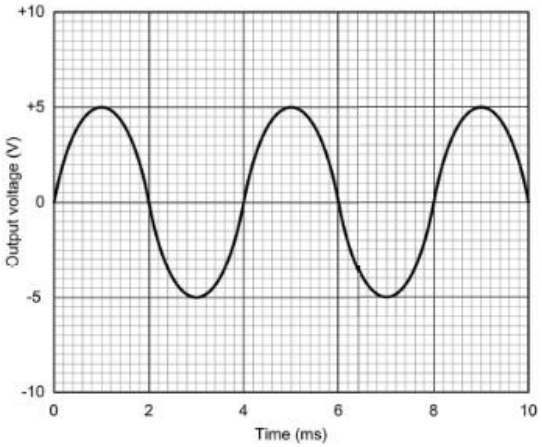


Figure 9.26 See Question 9.14

9.15 Design an oscillator circuit that will generate the output waveform shown in Fig. 9.27. Sketch a circuit diagram for the oscillator and specify all component values (including supply voltage). Give reasons for your choice of oscillator circuit.

9.16 Design an oscillator circuit that will generate the output waveform shown in Fig. 9.28. Sketch a circuit diagram for the oscillator and specify all component values (including supply voltage). Give reasons for your choice of oscillator circuit.

9.17 Briefly explain the term 'piezoelectric effect'.

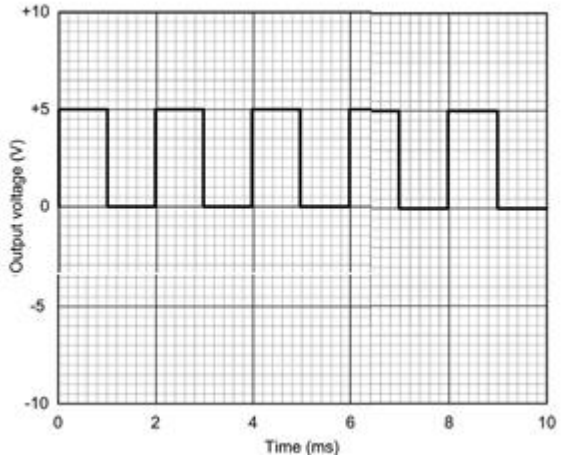


Figure 9.27 See Question 9.15

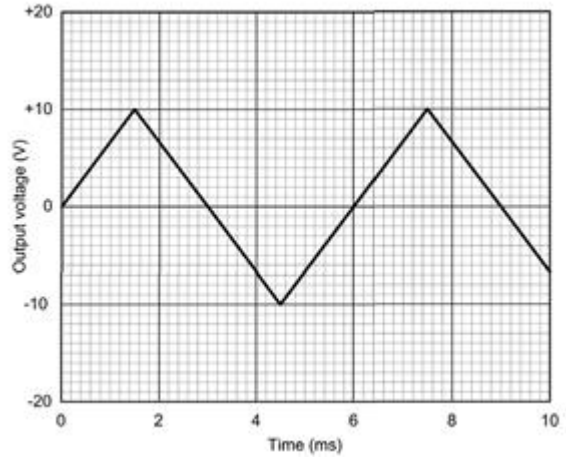


Figure 9.28 See Question 9.16

9.18 Sketch the circuit diagram of a simple single-stage crystal oscillator and explain the advantages of using a quartz crystal as the frequency determining element.