BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI –K. K. BIRLA GOA CAMPUS

INSTRUCTION DIVISION

FIRST SEMESTER 2021-2022

Course Handout (Part II)

August 20, 2021

In addition to part-I (General Handout for all courses appended to the time-table), this portion gives further specific details regarding the course.

Course No.	: CS F215/ECE F215/EEE F215/INSTR F215
Course Title	: Digital Design
Instructor-in-charge	: PRAVIN MANE *(pravinmane@goa.bits-pilani.ac.in)*
Team of Instructors	: Ravi Kadlimatti, Manish Bhatt, Hrishikesh Sonalikar, Manish Varun Yadav, Joshi Viraj Vilas, Swati Varun Yadav, Afroz Fatima,Jerry Anto K, Purab Nandi

1 Scope and Objective:

This is a foundation course that provides students with a fundamental knowledge of digital systems and their various components. Topics covered include Boolean algebra, digital gates, analysis of basic digital circuits, Combinatorial and Sequential digital circuits, digital ICs, arithmetic operations and algorithms, memories and basic computer organization.

2 Text Books:

1. M.Moris Mano, "Digital Design", Pearson, 5^{th} Edition, 2009.
2. Brian Holdsworth, Clive Woods, "Digital Logic Design", Elsevier, 4^{th} Edition, 2008

3 Reference Book:

1. John.M.Yarbrough, "Digital Logic Design", Cengage Learning, 2009.
2. Ronald.J.Tocci, Neal.S.Widmer, Gregory.L.Moss, "Digital Systems", 2007.
3. Stephen Brown, Zvonko Vranesic, "Digital Logic with VHDL Design", McGraw Hill,2013

4 Course Plan:

Lec. No.	Topic to be covered	Reading list
1	Number systems, radix and diminished radix complements	1.2-1.5
2	Signed numbers, arithmetic operations, codes	1.6-1.7
3	Boolean Algebra - basic theorems and properties	2.1-2.4
4	Algebraic manipulation, canonical forms	2.5-2.6
5	Logic gate basics, types of logic, IC families	2.7-2.9
6	Gate minimization - K-maps, SOP form	3.1-3.4
7	POS form, Don't care conditions,	3.5
8	AND-OR, NAND, NOR Implementations, Ex-OR	3.6-3.8
9	Quinn-McCluskey Method, Prime implicants	3.10
10	Combinatorial circuits - gate level design	4.1-4.4
11	Binary adders and subtractors	4.5
12	Comparators and Decoders	4.8-4.9
13	Encoders and Multiplexers	4.10-4.11
14	Three state gates, Design using MSI components	4.11
15	Introduction to Sequential circuits, Latches	5.1-5.3
16	Latches and flip-flops	5.4
17	Characteristic equations and transition tables	5.4
18	Analysis of sequential circuits	5.5
19	Finite state machines - design	5.7
20	FSM design continued	5.8
21	Registers	6.1-6.2
22	Counters - ripple	6.3
23	Synchronous counters	6.4
24	Other counters	6.5
25	Introduction to memories - RAM read and write	7.1-7.2
26	Memory decoding and ROM	7.3-7.5
27	Programmable logic, Introduction to sequential programmable logic	7.6-7.8
28	RTL design	8.1-8.3
29	ASM	8.4
30	Datapath design examples	8.5-8.6
31	Introduction to Asynchronous Sequential Logic	9.1-9.2
32	Race conditions, Latch based design	9.3-9.4
33	Design procedure with example	9.4
34	Reduction of states and flow tables, Hazards	9.5-9.6
35	Hazards in sequential design with examples	9.6-9.8
36	Introduction to Computer Architecture	Class notes
37	Conclusion	

5 Evaluation:

Component	Duration	Maximum marks	Date Time	Remarks
Theory				
Mid-Term Test	90 Minutes	60	18.10.2021 9.00 am-10.30 am	OB
Class participation surprise Quizzes	-	15	Throughout Semester	OB
Announced Quizzes (Best 3 out of 4)	30 Minutes each	45	TBA	CB
Comprehensive Examination	120 Minutes	80	13.12.2021 FN	CB
Lab				
Regular Lab (Best 5 out of 6)	As per timetable	50	As per timetable	OB
Verilog Evaluations (2)	60 Minutes	20	TBA	
Lab Comprehensive Examination	90 Minutes	30	TBA	

6 Make-up Policy:

Application for Make-up will be considered only for Mid-Sem and Comprehensive Examination. An application in writing with relevant certificates attached (medical from Campus Medical center or SWD) needs to be submitted to the IC of the course at least a day before the scheduled exam. No make-up will be given for labs, lab evaluations, surprise tests, tutorials and quizzes.

7 Lab Policy:

All students are required to be present for all scheduled lab sessions which will have an evaluation component. No make-up for lab sessions will be provided. An evaluation component will be conducted in all labs and will be considered towards the final grade.

8 Attendance Policy:

Since BITS, Pilani is a residential campus; all students are expected to engage in all regular and special lectures/tutorials as announced by the instructors. Attendance and class participation of the student will be considered during final grading and will be based on the sole discretion of the instructors.

9 Grading notice

All students registered in the course are expected to appear for all evaluation components. Per section 4.19 of the BITS, Pilani Academic regulations, NC may be given to students if they fail to provide a chance for the instructor to evaluate their progress in the class. Absence in any evaluation components without prior consent of the instructor or submitting blank or incomplete/incoherent answer books may present grounds for awarding NC in the course.

10 Honor code and disciplinary action

All submissions by students in this class towards quizzes, tests and tutorials will be considered their own original and individual work. It will be assumed that the students have not resorted to any unfair means during the evaluation. If malpractice is discovered, strictest action will be initiated against the student.

11 FAQs

(i). *Is lecture/tutorial attendance compulsory?* – Attendance will be taken per instructor discretion. 100% attendance for lectures and tutorials is expected.

(ii). *Can I get a makeup for tutorials/quizzes?* – No makeup will be provided for these. They are intended to serve as techniques to assess course speed and relevance.

(iii). *Is lab attendance compulsory?* – Attendance for all lab components is compulsory. Absence from lab sessions may provide grounds for awarding NC.

(iv). *If I make >10% in the course, will I be safe from an NC?* – All grading decisions will be taken by the team of instructors after the comprehensive examinations are over. There is no stipulated cut-off for NC. Students are expected to perform to the best of their abilities.

(v). *I thought I understood all the tutorials; however, I did not do well in the examination. Why?* - Tutorial sessions are used as an aid to help understand concepts that have been taught in lecture and provide an opportunity for students to revisit topics with the instructor. They should not be viewed as templates for the mid-sem or comprehensive examination.

(vi). *I find the course difficult. How do I improve my performance?* – Students are encouraged to meet with instructors during their office hours for additional help. A team of TA's will be available to also help students with classwork, labwork and tutorials.

12 Announcements

Course management and announcements will be handled through the BITS moodle webpage. However, since 100% class attendance is expected, there might be a delay between class announcements to the information appearing on the moodle webpage.

13 Chamber Consultation Hour:

To be announced in class by individual instructors.

Instruction Incharge

CS F215/EEE F215/INSTR F215