Birla Institute of Technology & Science, Pilani
Work-Integrated Learning Programmes Division

Second Semester 2013-2014

Course Handout

Course No. **: ES ZC261**

Course Title **: Digital Electronics & Microprocessors**

Instructor **: Rekha K**

Course Description

Binary logic gates; logic circuits; Boolean algebra and K-map simplification; number systems and code; arithmetic logic units; flipflops; registers and counters; introduction to microprocessors; architecture; instruction set and programming; memory and I/O interfacing; examples of system design.

Scope and Objectives

The course aims at teaching students the fundamentals of Digital electronics & Digital Systems Design. It also covers 8-bit microprocessor architecture, Programming and interfacing of memory and I/O. Using these concepts the students will be able to design microprocessor based systems for different applications.

Prescribed Text Books

T1. Mano, M. Morris, Michael D. Ciletti, Digital Design, Pearson Education, 4th Ed., 2008.

T2. Barry B. Brey, The Intel Microprocessors, Architecture, Programming and Interfacing, Pearson Education, 8th Ed., 2009

Reference Books

R1. David Money Harris and Sarah L. Harris, Digital Design and Computer Architecture (Books24X7)

R2. Saha and N. Manna, Digital Principles and Logic Design (Books24X7)

R3. Douglas V Hall, Microprocessors and Interfacing, McGraw-Hill, revised second edition.2006

Legend
M = Module, VL = Video Lecture, CS = Contact Session, LE = Lab Exercises, SS = Self Study, HW = Home Work Problems

Modular Structure

Module Summary

No	Title of the Module	No of Video Lectures	No of Contact Sessions	Contact sessions
M0	Introduction	0	1	CS1 Week1
M1	Boolean algebra, logic gates , canonical representations, Boolean function minimization	2	1	CS2: Week 2&3
M2	**Combinational Logic** (Arithmetic circuits (binary adder-subtractor), BCD adder, Decoders, Encoders, Multiplexers, De-Multiplexers)	5	2	CS 3&4 Week 4&5
M3	**Sequential Logic building blocks** (latches and flip-flops, characteristic and excitation tables, state equations, analysis of sequential circuits)	2	1	CS 5 Week 6
M4	**Registers & Counters** (parallel and serial data transfer, universal shift register, ripple and synchronous counter)	2	2	CS 6&7 Week 7
M5	**Microprocessor Architecture** (Programmers Register Set of Intel x86 Processor, address/data buses and memory segmentation)	2	1	CS 8 Week 8
	Review session		1	CS 9 Week 9
M6	**Addressing Modes & Data Movement Instructions** (data and program memory addressing modes, instructions involved in movement of data)	2	1	CS 10 Week 10&11
M7	**Assembly language Programming** (Data movement instructions, Arithmetic and Logic instructions, instructions for data strings, introduction to the assembler and assembly language programming)	3	3	CS 11,12& 13 Week 12 &13
M8	**Interrupts & Programme Control Instructions** (Interrupt instructions, vectors and control, conditional and unconditional program control instructions, subroutines)	2	2	CS 14&15 Week 14&15
M9	**Memory Design** (Memory devices, interface of RAM and ROM to 8086, decoding logic, odd and even addressing)	2	1	CS 16 Week 16
M10	**I/O Interfacing & System Design** (isolated vs memory-mapped I/O, port decoding, building a complete microprocessor based system)	2	1	CS 17 Week 17
	Review session		1	CS 18 Week 18
	Total:	24	18	

Detailed Structure

M0: Introduction

Introduction, Digital systems and binary numbers, evolution of microprocessors

Week 1

Type	Description/Plan/Reference
CS1	Introduction, Digital systems and binary numbers, evolution of microprocessors
SS1.1	Chapter 1 T1.
HW1.1	Assign problems as Home Work : Ex: 1.3; 1.16; 1.26

M1: Boolean algebra, logic gates and canonical representations.

Introduction to digital systems; logic gates; Binary code;, Boolean functions and canonical forms of representation; minimization using k- Maps.

Week 2.

Type	Description/Plan/Reference
VL1.1	Introduction to Digital systems, Canonical forms: Sum Of Products & Product Of Sums representations, Maxterms & Minterms. (30 Minutes)
VL1.2	Minimization using k-MAP : Minimal Sum of Products expression, Three variable & Four variable functions, (20 minutes)
CS2	Quick recap of the topics of the Recorded video lecture by the Instructor (20 Minutes). **(While some Problem numbers are given these are broad guidelines and the Faculty could pick some other similar examples)** • Examples (From T1): Ex: 2.18; 2.19 & 2.20 introduce the concept of Compliments and compare between two forms of representations. • Examples (From T1): Ex: 3.5; 3.11; 3.17: Introduce POS Implementation and use of don't cares. Also introduce use of NAND gates and NAND-NAND Implementation.
SS1.1	Chapter 1 T1.
HW1.1	Assign problems as Home Work : Ex: 3.16; 3.23; 3.24;

M2: Combinational Logic: (Arithmetic circuits (binary adder-subtractor), BCD adder, Decoders, Encoders, Multiplexers, De-Multiplexers)

Week 3 &4

VL 2.1	Arithmetic circuits (Half adder/Half Subtractor, Binary adder, Multiplier)
VL 2.2	Decoders: What is a Decoder, Decoder using gates, Modular design, Decoder Applications.
VL 2.3	Encoders: What is an Encoder, Priority Encoder, Application of Encoder
VL 2.4	Multiplexer: 2:1 Multiplexer, Building Larger Multiplexers, Multiplexer Applications
VL 2.5	DeMultiplexer: Building a Demultiplexer, Applications of Demultiplexers
CS 3	**Arithmetic Circuits:** Quick recap of the topics of the Recorded video lecture VL2.1 by the Instructor (15 Minutes). • Exercise Problem 4.12 .Design of Half subtractor & Full subtractor; • Topic 4.6: BCD adder design,

	• Topic 4.8 Magnitude Comparator. • Design of a 4 bit binary Multiplier.
CS 4	Combinational MSI Blocks: Recap of what is given in Recorded video lecture VL2.2, VL2.3, VL2.4 & VL2.5 (20 Minutes), • Topic 4.6 :Design of a code converter • Exercise 4.30: Combinational circuit design using Decoder: • Exercise 4.33: Multiplexer Modular design Exercise 4.33: • Exercise 4.34 Combinational circuit design using Multiplexer • One example of Multiplexer One example on Encoder (40 Minutes).
SS2.1	Ripple carry adder and what are its speed limitations and how look ahead carry adder improves the speed.
HW2.1	Assign problems as Home Work :ex: 4.7; 4.10; 4.27; 4.37

M3: Sequential Logic Building blocks: (Latches and flip-flops, characteristic and excitation tables, state equations, analysis of sequential circuits)

Week 5

VL 3.1 VL 3.2	Latches & Flip flops: SR Latch, D latches: D, JK and T Flip-flops. Design of a sequential circuit using D FF: Sequence Detector example.
CS5	**Latches & Flip flops.** Quick recap of the topics of the recorded video lecture VL2.1 by the Instructor (15 Minutes). • Characteristic tables of flip flops • Flip flop characteristic equation. • Section 5.5: Analysis of clocked sequential circuits. • Exercise Problems: 5.2; 5.7; 5.10
SS2.1	State reduction : Section 5.7
HW2.1	Assign problems as Home Work :ex: 5.16; 4.10; 4.27; 4.37

M4: Registers & Counters: (parallel and serial data transfer, universal shift register, ripple and synchronous counter)

Week 6&7

VL 4.1 VL4.2	Registers: Design of N-bit register using D FFs, Design of Shit Register; universal Shift Register Counters: Ripple counters; Synchronous counters
CS6	**Registers & Counters:** Quick recap of the topics of the recorded lecture VL4.1 & 4.2 by the Instructor (20 Minutes). • Section 6.2 (T1) Design of serial adder using a Shift Register; Serial to Parallel and Parallel to serial conversion • Design of a BCD ripple counter; block diagram of decade counters.
CS 7	Quick recap of the topics of the recorded video lecture by the Instructor (20 Minutes). • Section 6.5: Design of a counter with unused states, Ring counter; twisted ring counter • Exercise Problems: 6.6; 6.7; 6.12; 6.24
SS5.1	Design of counters with asynchronous inputs like clear & set
HW2.1	Assign problems as Home Work :ex:6.11; 6.14; 6.27;

M5: Microprocessor Architecture: (Programmers Register Set of Intel x86 Processor, address/data buses and memory segmentation)

Week 8

VL 5.1 VL5.2	Architecture of x86 CPU: Internal functional blocks of x86 CPU; Programmers Register set; Flag Registers. Address Data bus Multiplexing: Odd and Even Memory banks. Address data Demultiplexing using Latch.
CS8	**Architecture of x86 CPU** Quick recap of the topics of the recorded lecture VL4.1 & 4.2 by the Instructor (20 Minutes). • Section 2.1 (T2) Programmers model of x86 CPU • Section 2.2 (T2) Memory segmentation: Different segments of Memory and their functions. • Exercise Problems: Chapter 2 (14; 20)
SS5.1	Architecture of high end processors of x86 series.

Week 9

CS9	• Review session

M6: Addressing Modes & Data Movement Instructions (data and program memory addressing modes, instructions involved in movement of data, MOV instruction)

Week 10

Type	Description/Plan/Reference
VL6.1	Introduction to data addressing modes, (30 Minutes)
VL6.2	Introduction to memory addressing modes, form assembly language statements using data movement instructions (30 minutes)
CS10	Quick recap of the topics of the recorded video lecture by the Instructor (20 Minutes). **(While some Problem numbers are given these are broad guidelines and the Faculty could pick some other similar examples)** • Examples (From T2): Ex: 3.6, 3.8, 3.9, 3.10. Introduction to data addressing modes using assembly language statements • Examples (From T2): Ex: 3.14, 3.15: Introduction to program memory addressing modes using JMP, CALL instructions and stack memory..
SS6.1	Self Study of Scaled Index Addressing and RIP relative addressing, pages 98-99 of T2.
HW6.1	Assign problems as Home Work : Chapter 3 (22, 29, 33, 39);

M7: Assembly language Programming (Data movement instructions, Arithmetic and Logic instructions, instructions for data strings, introduction to the assembler and assembly language programming)

Week 11,12 & 13

Type	Description/Plan/Reference
VL7.1	Introduction to data movement instructions involving data strings. (30 Minutes)
VL 7.2	Introduction to arithmetic instructions using assembler (30 minutes)
VL 7.3	Introduction to Logical Instructions (30 minutes)
CS11	Quick recap of the topics of the recorded lecture by the Instructor (20 Minutes). **(While some Problem numbers are given these are broad guidelines and the Faculty could pick some other similar examples)** • Examples (From T2): Ex: 4.3, 4.4, 4.11. Introduction to data movement instructions along with data strings transfer. • Examples (From T2): Ex: 5.4, 5.6, 5.7, 5.11. Introduction to arithmetic instructions involving signed and unsigned data.

CS12	Quick recap of the topics of the recorded video lecture by the Instructor (20 Minutes). • Examples (From T2): Ex: 5.13, 5.17, 5.21. Introduction to arithmetic instructions (contd..).
CS13	Quick recap of the topics of the recorded lecture by the Instructor (20 Minutes). • Examples (From T2): Ex: 5.27, 5.31, 5.33. Introduction to logical instructions.
SS7.1	Self Study of BCD and ASCII arithmetic instructions, Sec 5-3, pages 172-175 of T2.
HW7.1	Assign problems as Home Work : Chapter 4 (25, 27, 43); Chapter 5 (26, 32, 44, 48)

M8: Interrupts & Programme Control Instructions (Interrupt instructions, vectors and control, conditional and unconditional program control instructions, subroutines)
Week 14&15

Type	Description/Plan/Reference
VL8.1	Introduction to program control instructions (un-conditional/conditional jump instructions). (40 Minutes)
VL 8.2	Introduction to program control instructions (procedures/macro) and interrupt instruction (50 minutes).
CS14	Quick recap of the topics of the recorded video lecture by the Instructor (20 Minutes). **(While some Problem numbers are given these are broad guidelines and the Faculty could pick some other similar examples)** • Examples (From T2): Ex: 6.1, 6.2, Introduction to jump instructions. • Examples (From T2): Ex: 6.14, 6.15.
CS15	Quick recap of the topics of the recorded lecture by the Instructor (20 Minutes). • Examples (From T2): Ex: 6.16, 6.17 Introduction to procedures. • Examples (From T2): Ex: 6.18. Introduction to Interrupts.
SS8.1	Self Study of Loop instructions, pages 201-202 of T2.
HW8.1	Assign problems as Home Work : Chapter 6 (24, 33, 38, 42)

M9: Memory Interfacing (Memory devices, interface of RAM and ROM to 8086, address decoding logic, odd and even addressing)
Week 16

Type	Description/Plan/Reference
VL9.1	Memory Address Space, Interfacing memory with odd and even banks, Memory internal blocks
VL 9.2	Address decoding logic; Memory fold back, variable size memory interfacing, ROM and RAM address space.
CS16	Quick recap of the topics of the recorded video lecture by the Instructor (20 Minutes). **(While some Problem numbers are given these are broad guidelines and the Faculty could pick some other similar examples)** • Memory read write Machine cycles; • Section 10.2: Memory Address decoding • Section 10.4: 8086 Memory interfacing
SS9.1	Timing diagrams of memory read & memory write cycles.
HW9.1	Memory interfacing design examples.

M10: I/O Interfacing (isolated vs memory-mapped I/O, port decoding, building a complete

microprocessor based system)

Week 17

Type	Description/Plan/Reference
VL10.1	Interfacing input devices: Introduction I/O mapped I/O; key pad interfacing
VL 10.2	Interfacing Output devices: LED interfacing; seven segment display interfacing
VL 10.3	System Design example
CS17	Quick recap of the topics of the recorded video lecture by the Instructor (20 Minutes). • Section 10.2: I/O Port address decoding • Interfacing A/D converter with 8086. • Stepper Motor controller Interface
SS10.1	System Design example
HW7.1	Design examples:

Week 18

CS18	• Review session

Evaluation Scheme:

EC No.	**Evaluation Component & Type of Examination**	**Duration**	**Weigh-tage**	***Day, Date, Session,Time***
EC-1	Assignment/Quiz	*** Details to be announced on LMS Taxila website by Instructor*	15%	*** Details to be announced on LMS Taxila website by Instructor*
EC-2	Mid-Semester Test **(Closed Book)***	2 Hours	35%	Sunday, 16/02/2014 (AN)* 2 PM – 4 PM
EC-3	Comprehensive Exam **(Open Book)***	3 Hours	50%	Sunday, 06/04/2014 (AN)* 2 PM – 5 PM

***** Please check the details by January 10, 2014 on LMS Taxila web site.***

AN: AfterNoon Session**;** **FN:** ForeNoon Session

Closed Book Test: No reference material of any kind will be permitted inside the exam hall.
Open Book Exam: Use of any printed / written reference material (books and notebooks) will be permitted inside the exam hall. Loose sheets of paper will not be permitted. Computers of any kind will not be allowed inside the exam hall. Use of calculators will be allowed in all exams. No exchange of any material will be allowed.

Note:
It shall be the responsibility of the individual student to be regular in maintaining the self study schedule as given in the course handout, attend the online/on demand lectures as per details that would be put up in the **BITS LMS Taxila** website **www.taxila.bits-pilani.ac.in** and take all the prescribed components of the evaluation such as Assignment **(Course Page on LMS Taxila),** Mid Semester Test and Comprehensive Examination according to the Evaluation Scheme given in the respective Course Handout. If the student is unable to appear for the Regular Test/Examination due to genuine exigencies, the student must refer to the procedure for applying for Make-up Test/Examination, which will be available through the Important Information link on the **BITS LMS Taxila** website **www.taxila.bits-pilani.ac.in** on the date of the Regular Test/Examination. The Make-up Tests/Exams will be conducted only at selected exam centres on the dates to be announced later.

Instructor-in-Charge