BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI –

K. K. BIRLA GOA CAMPUS

II Semester 2022-2023

Course Handout – II

In addition to Part-I (General Handout for all courses appended to the timetable), this portion gives specific details regarding the course.

Course Number: ECE/EEE/INSTR F244

Course Name: Microelectronic Circuits

Instructor-in-charge: Abhijit Pethe *(abhijitp@goa.bits-pilani.ac.in)*

Team of Instructors: Pravin Mane, Abhijit Pethe

1. **Scope and Objective:**

Basic microelectronic circuit analysis and design, biasing in discrete and integrated circuit amplifiers, an overview of modeling of microelectronic devices single and two transistor amplifier configurations with passive and active loads; current mirrors & current sources; single-ended and differential linear amplifiers, differential and multistage amplifiers; 2 stages CMOS OPAMP, the frequency response of amplifiers; negative feedback in amplifiers, R-C frequency compensation. This course will also introduce students to design in Cadence Design studio in an unstructured lab component

2. **Textbook**

i. A.S. Sedra and K.C. Smith, "Microelectronic Circuits – Theory and Applications", Oxford University Press, 7th ed., 2017

3. **Reference Book**

i. B. Razavi, "Design of Analog Integrated Circuits", Tata McGraw Hill, 2001

4. **Course Plan**

Lect. No.	Topic	Learning objectives	Book reference
1	Introduction	Course contents, circuit design uses, amplification etc.	
2-4	Circuits Review	Circuit abstraction, network theorems, analysis of non-linear circuits, 2-port networks	Class notes
5-8	MOS Transistor Physics	Review MOSFET models, generalized biasing, small signal analysis	Ch. 5

9-16	IC Amplifier Design	Design and analysis of basic MOS amplifier stages, Cascading stages	Ch. 6, 7.1-7.4
17-20	IC biasing, Basic current mirrors	Overview of passive and active current mirrors, current biasing techniques	7.5-7.7
20-27	Differential Amplifiers	Design and analysis of MOS-based differential amplifiers.	Ch. 8
28-33	Frequency response	Analysis of frequency response of amplifier circuits, stability, and design	Ch. 9
34-37	Feedback	Types of feedback	Ch. 10
38-40	Operation Amplifier abstraction	Block diagram of OPAMP, simple applications	Class notes

5. Evaluation Scheme

No.	Component	Duration	CB/OB	Marks (%)	Date
1	Continuous evaluation – announced quizzes	----	OB	24%	Tentative dates: 15/02, 29/03, 19/04 (subject to change)
2	Labs – continuous evaluation	----	OB	11%	Weekly labs with evaluation
3	Mid-semester Exam	1.5 hours	CB	25%	13/03/22 11:00am-12:30pm
4	Comprehensive Exam	3 hours	CB	40%	15/05/22 AN

6. Make-up Policy

Application for Make-up will be considered only for Mid-Sem and Comprehensive Examination. An application in writing with relevant certificates attached (medical from Campus Medical center or SWD) needs to be submitted to the IC of the course at least a day before the scheduled exam. No make-up will be given for surprise tests, tutorials, labs and quizzes. (no exceptions)

7. Attendance Policy

Since BITS, Pilani is a residential campus; students are expected to engage in all regular and special lectures/tutorials as announced by the instructors. Attendance and class participation of the student will be considered during final grading and will be based on sole discretion of the instructors.

8. Grading notice

All students registered in the course are expected to appear for all evaluation components. Per section 4.19 of the BITS, Pilani Academic regulations, NC may be given to students if they fail to provide a chance for the instructor to evaluate their progress in the class. Absence in any evaluation components without the prior consent of the instructor or submitting blank or incomplete/incoherent answer books may present grounds for awarding NC in the course.

9. Honor code and disciplinary action

All submissions by students in this class towards quizzes, tests, and tutorials will be considered their original and individual work. It will be assumed that the students have not resorted to unfair means during the evaluation. If malpractice is discovered, the strictest action will be initiated against the student.

10. FAQs

(i) *Is attendance compulsory?* – Attendance will be taken at the instructor's discretion. 100% attendance for lectures and tutorials is expected.

(ii) *Can I get a makeup for tutorials/quizzes?* – No makeup will be provided for these.

(iii) *If I make >10% in the course, will I be safe from an NC?* – All grading decisions will be taken by the team of instructors after the comprehensive examinations are over. There is no stipulated cut-off for NC. Students are expected to perform to the best of their abilities.

(iv) *Why should I take this class?* – This class is a pre-requisite for Analog and Digital VLSI Design and other VLSI electives. It is an introductory class for anyone planning a career in VLSI, Analog design, technology, optoelectronics, etc.

(v) *I find the course mathematical and difficult. How do I improve my performance?* – Students are encouraged to meet with instructors during office hours for additional help. A team of TAs will be available also to help students with classwork and tutorials.

(vi) *I thought I understood all the tutorials but did not do well in the examination. Why?* - Tutorial sessions help students understand concepts taught in lectures and provide an opportunity for students to revisit topics with the instructor. They should not be viewed as templates for the mid-sem or comprehensive examination.

11. Announcements

Course management and announcements will be handled through the BITS moodle webpage. However, since 100% class attendance is expected, there might be a delay between class announcements to the information appearing on the moodle webpage.

12. Chamber consultation hours

To be announced in class by individual instructors.

Instructor-in-Charge

ECE/EEE/INSTR F244