Birla Institute of Technology & Science, Pilani, K.K Birla Goa Campus Second Semester 2023-2024

Course Handout Part II

Date:09/01/2024

In addition to Part-I (General Handout) for all courses appended to the time table), this portion gives further specific details regarding the course.

Course No : ECE F341 / EEE F341 / INSTR F341

Course Title : Analog Electronics Instructor-in-charge: RAMESHA C K

Instructors: Apurba Chakraborty, Anurag Nishad, and Ashish Chittora

Scope and Objective of the course

The aim of the course is to deal with various electronic techniques and building blocks used in analog signal processing. Discrete and Integrated electronic circuits will be studied. Experiments using discrete IC modules will be carried out in the laboratory. In addition SPICE (Simulation Program with Integrated Circuit Emphasis) is used as a simulation tool for circuit analysis.

1. Text Book

TB1 L.K. Maheshwari, Analog Electronics, PHI, 2008

TB2 L.K. Maheshwari and M.M.S. Anand, Laboratory Experiments & PSPICE Simulation in Analog Electronics Experiments, PHI, 2008.

2. Reference Book(Relevant Portion)

R1 Sergio Franco, Design with Operational Amplifiers and Analog Integrated Circuits, Third Edition, Tata McGraw-Hill Edition

R2 Ramakant A. Gayakwad Op-Amps and Linear Integrated Circuits, PHI 2009

R3 Adel S Sedra and Kenneth C Smith Microelectronic Circuits Theory and Applications

3. Course Plan

S.No	Topic	No. of	Reference to Text
		Lectures	
1	Introduction & Review of Concepts:	2	TB1 Ch 1
	Basic understanding of analog and digital		
	signals, Discrete and Integrated Circuits,		
	Differential circuits		
2	Op-amp basics:	3	TB1 Ch 2 (2.1-2.6)
	Introduction of op-amp, Block diagram of typical		, ,
	op-amp, op-amp symbol, equivalent circuit,		
	transfer characteristics, ideal op-amp, basic		
	circuit configuration of op-amp, practical op-		
	amp, PSPICE model of op-amp		
3	Special purpose opamp circuits:	3	TB1 Ch 3 (3.1-3.6)
	Instrumentation amplifier, Isolation amplifier,		
	Programmable gain amplifier, negative feedback		
	amplifier and controlled sources, Inductance		
	simulation		
4	Filters: Basics of filter circuits, realization of active	4	TB1 Ch 4 (4.1-4.4)
	filters, IC filters		, ,

5	Non-linear Op-amp circuits: Logarithmic amplifiers, Analog multipliers, applications of analog multipliers, Precision	5	TB1 Ch 5 (5.1-5.6)
	circuits, Comparator and Schmitt triggers, Analog switch, Sample and hold circuits, Analog multiplexers		
6	Signal Sources & Phase lock loop: Sinusoidal Oscillators, Non-Sinusoidal Oscillators, IC Timers, Function generator, Phase lock loop	6	TB1 Ch 6 (6.1-6.6)
7	Voltage Regulators: Performance measures of voltage regulators, Voltage regulator ICs	5	TB1 Ch 7 (7.1-7.4)
8	IC Power Amplifiers: Power amplifier, CMOS Power amplifiers, IC Power amplifiers	2	TB1 Ch 8 (8.1-8.4)
9	Tuned Amplifiers	2	TB1Ch 9-9.4
10	Data Converters : D/A, A/D Converters	4	TB1Ch10 (10.1-10.3)
11	IC sensors and Analog Systems	4	TB1Ch 11 (11.1-11.6)
	Total lectures	40	

4. Evaluation Scheme

Component	Duration	Marks	Date and Time	Remarks
Mid Sem Exam	90 min	80	14/3/2024	Closed Book
			(9 - 10:30 am)	
Two Online Quiz	30 min	15+15=30	TBA	Open Book
	each			
Online Test (PSPICE		20		Open Book
Computer Simulation)				_
Laboratory	2 hours	30	Regularly	Open Book
Experiments/Viva				
Laboratory Compre		30		Closed Book
Examination/Viva				
Comprehensive	3 hours	110	06/5/2024 (FN)	Closed Book
TOTAL		300		

5. Chamber Consultation Hour: To be announced in Class

6. Make-up Policy: Make-up shall be granted only on extremely genuine grounds only. Application for Make-up will be considered only for mid-sem and Comprehensive Examination. An application in writing with relevant certificates attached needs to be submitted to the IC of the course at least a day before the scheduled exam. No make-up will be given for labs, lab evaluations, tests, tutorials and quizzes..

7. Lab Policy:

All students are required to be present for all scheduled lab sessions which will have an evaluation component. No make-up for lab sessions will be provided. An evaluation component will be conducted in all labs and will be considered towards the final grade.

8. Attendance Policy:

All students are expected to engage in all regular and special lectures/tutorials as announced by the instructors. Attendance and class participation of the student will be considered during final grading and will be based on the sole discretion of the instructors.

9. Grading Notice:

All students registered in the course are expected to appear for all evaluation components. Per section 4.19 of the BITS, Pilani Academic regulations, NC may be given to students if they fail to provide a chance for the instructor to evaluate their progress in the class. Absence in any evaluation components without prior consent of the instructor or submitting blank or incomplete/incoherent answer books may present grounds for awarding NC in the course.

10. Honor code and Disciplinary Action:

All submissions by students in this class towards quizzes, tests and tutorials will be considered their own original and individual work. It will be assumed that the students have not resorted to any unfair means during the evaluation. If malpractice is discovered, strictest action will be initiated against the student.

11. Notices: Notices, if any, concerning the course will be put up on the Quanta server.

Instructor In Charge ECE F341 / EEE F341 / INSTR F341

BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI, GOA CAMPUS SECOND SEMESTER 2023-2024

ECE F341/ EEE F341 / INSTR F341 Analog Electronics

S.No. Experiment and Reference to Manual

1.	Characterization of Op-amp
	Exp.6

- 2. Basic Configuration of Op-amp Exp.5
- 3. Precision Circuit Exp. 12
- 4. Instrumentation and Programmable Amplifier Exp.7
- 5. Comparators and Schmitt Trigger Circuits Exp. 13
- 6. Sinusoidal and non-sinusoidal Oscillators Exp. 15
- 7. Integrated Circuit Timer Exp. 16
- 8. Study of Active filters Using Op-amps- low pass, high pass and band pass Exp. 9
- 9. IC Fixed and adjustable Voltage Regulators Exp. 19
- 10. D to A and A to D Converters Exp.24 and 25