BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI, K. K. BIRLA GOA CAMPUS
FIRST SEMESTER 2018-2019
COURSE HANDOUT (PART II)

Date: 02/08/2018

In addition to Part I (General Handout for all courses appended to the timetable) this portion gives further specific details regarding the course.

Course No. : **CS F342**
Course Title : **Computer Architecture**
Instructor-in-charge : **GEETA PATIL (geetapatil@goa.bits-pilani.ac.in)**
Guest Instructor : **Dr. BIJU RAVEENDRAN (biju@goa.bits-pilani.ac.in)**
Instructor : **Mrs. Gargi Kabirdas (p20160008@goa.bits-pilani.ac.in)**

1.1 Objective

Introduce the students to various components of computing system. Educate them to architect and organize the computing system, measure performance of the system and optimize the system for the specific requirements. Expose them to languages used for designing such systems. Also expose them to the latest advancements in this area.

1.2 Scope

The course will review basics of Digital electronics and Microprocessors. The primary focus of this course is to understand various components of a computing system, underlying architectures of the components and the organization of them to make a computing system functional. It also looks at methods and problems of designing architectures like single cycle, multi-cycle, pipelining and superscalar. The course will also evaluate the performance of the computing systems and will try to optimize the system for the specific requirements like area, power and performance. The course will address the processor design considering ISAs of MIPS and ARM. It will also address the system resources like Memory and I/O subsystem. The course will also address the design aspects of the computing system with the help of Verilog HDL as hands on experiments in lab.

1.3 Course description

Introduction to Computer Organization – MIPS ISA and data path design for Single Cycle architecture - Programming with MIPS, MIPS Address modes: R – type, I – type and J – type, Single Cycle Data path design for a sub set of MIPS ISA; MIPS ISA and data path design for Multi-Cycle and pipelined architectures; ARM ISA and Addressing modes; DRAM - Memory hierarchy, Memory interleaving, Evolution; Cache Memory – Mapping functions: Direct mapped, Set Associative and Fully Associative; Cache Misses – Compulsory, Conflict and Capacity misses, Replacement Algorithms; Optimization of Cache performance and Inter connection structures; Advance concepts in Computer Organization – Instruction-level parallelism and Superscalar Processors, Parallel Processing, Multi Core Architectures and Multi-processor architectures.

2.1 Text Books:

(T1) David A. Patterson and John L. Hennessy, “Computer Organisation and Design: The Hardware/Software Interface”, Elsevier, 5th Edition - MIPS Edition, 2016.

(T2) William Stallings, “Computer Organisation & Architecture: Designing for performance”, Pearson Education, 10th Edition, 2015.

2.2 Reference Books:

(R1) Samir Palnitkar, “Verilog HDL: A Guide to Digital Design and Synthesis”, Pearson Education, 2003.

(R2) Barry B. Brey, “The Intel Microprocessors: Architecture, Programming and Interfacing”, PHI, 8th Edition, 2009.

(R3) John L. Hennessy and David A. Patterson, “Computer Architecture: A Quantitative Approach”, Elsevier, 4th Edition, 2007.

3.1 Lecture Modules & Learning Objectives

Module	Title	Learning Objectives
1	Introduction to Computer Organization	Review of basics of Digital Electronics and Microprocessors. Introduce to the world of computer organization & Architecture
3	MIPS ISA and data path design for Single Cycle architecture	MIPS instruction set architecture and data path design for each instruction in Single Cycle architecture.
4	MIPS ISA and data path design for Multi-Cycle and pipelined architectures	MIPS instruction set architecture and data path design for each instruction in Multi-Cycle and pipelined architectures.
5	ARM ISA	ARM Instruction set architecture and modes of operations
6	RAM, Cache Memory and Inter connection structures	DRAM design, Cache memory design and Inter connection structures
7	Advance concepts in Computer Organization	Instruction-level parallelism and Superscalar Processors, Parallel Processing, Multi Core Architectures, Intel Core 2 Duo Processor

3.2 Lecture Schedule

Mod #	Lect #	Topics	References
1	1 – 3	**Introduction to Computer Organization**	
	1 – 1	Introduction to Computer Organization	Class Notes
	2 – 3	Instruction Set Architecture, RISC and CISC Design	Class Notes

2	**4 – 9**	**Hardware design for Basic Arithmetic Circuits**	
	4 – 4	Floating point representation and basic operations	Class Notes
	5 - 6	Floating point operations in hardware	T2 Ch. 9.3 – 9.5
	7 – 9	Basics of Instruction Processing and introduction of various parameters for Performance evaluation	T1 Ch. 4, Class Notes
3	**10 – 18**	**MIPS ISA and data path design for Single Cycle Architecture**	
	10 – 11	Programming with MIPS	T1 Ch. 5.1 – 5.4
	12 – 14	MIPS Address modes: R – type, I – type and J - type	
	15 – 18	Single Cycle Data path design for a sub set of MIPS ISA	
4	**19 - 28**	**MIPS / ARM ISA and data path design for Multi-Cycle and Pipelined Architectures**	
	19 – 20	MIPS ISA and data path design for Multi-cycle architecture	T1 Ch. 5.5 – 5.9
	21 – 22	FSM based control circuit design and Micro-programming for Multi-cycle architecture	T1 Ch. 5.5 – 5.9
	23 – 23	Exception in Multi-cycle architecture	T1 Ch. 5.5 – 5.9
	24 – 28	MIPS ISA and data path design for Pipelined architecture. Pipeline hazards, Branch prediction & Exceptions	T1 Ch. 6.1 – 6.6
5	**29 – 38**	**DRAM, SRAM (Cache Memory) and Inter connection structures**	
	31	Memory hierarchy, DRAM Organization – Memory interleaving, Evolution	T1 Ch. 7.4 – 7.9
	32	SRAM – Cache memory structure	T1 Ch. 7.1 – 7.3 R3 Ch. 5.1 – 5.5
	33	Cache design: Mapping functions – Direct mapped, Set Associative and Fully Associative	
	34 – 35	Cache Misses – compulsory, conflict and capacity misses, Replacement Algorithms	
	36 – 38	Optimizations of Cache performance	
6	**39 - 42**	**Advance Concepts in Computer Organization**	
	39 – 40	Parallel Processing, MIPS / ARM ISA and data path for Super scalar	T1 Ch. 9
	41 – 42	Multi Core Architectures, Intel Core 2 Duo Processor	Class Notes

4.1 Evaluation Scheme:

S. No	Evaluation Component	Duration (Mints)	Weightage (%)	Date & Time	Nature of Component
1.	Mid- Semester	90	25%	10–10–2018, 16:00–17:30	Closed Book
2.	Lab	--	10%	Lab 1 : **16/08/2018** Lab 2 : **30/08/2018** Lab 3 : **06/09/2018** Lab 4 : **04/10/2018** Lab 5 : **18/10/2018** Lab 6 : **08/11/2018** Best 5 of 6	Open Book
3.	Online(s) and Quizes	--	30%	Online 1: 27/09/2018 (7%) Online 2: 15/11/2018 (8%) Quiz : 22/11/2018 (5%) Surprise Quizzes: During Class [Best N-1 of N where N is unknown] (10%)	Open Book
4.	Comprehensive	180	35%	04 – 12 – 2018, AN	Closed Book

4.2 Malpractice Regulations:

1. Any student or team of students found involved in mal practices in working out lab problems and online will be awarded negative marks equal to the weightage of that component and will be blacklisted.
2. Any student or team of students found repeatedly – more than once across all courses – involved in mal-practices will be reported to the Disciplinary Committee for further action. This will be in addition to the sanction mentioned above.
3. A mal-practice - in this context - will include but not be limited to:
   - Submitting some other student's / team's solution(s) as one's own;
   - Copying some other student's / team's data or code or other forms of a solution;
   - Seeing some other student's / team's data or code or other forms of a solution;
   - Permitting some other student / team to see or to copy or to submit one's own solution;
   - OR other equivalent forms of plagiarism wherein the student or team does not work out the solution and/or uses some other solution or part thereof (such as downloading it from the web).
4. The degree of mal-practice (the size of the solution involved or the number of students involved) will not be considered as mitigating evidence. Failure on the part of instructor(s) to detect mal-practice at or before the time of evaluation may not prevent sanctions later on.

5. **Chamber Consultation Hour**: To be announced in the class.
6. **Notice**: Notice concerning this course will be displayed on **http://10.1.1.242/lms**
7. **Makeup Policy**:

- Permission of the Instructor-in-Charge is required to take a make-up
  - Make-up applications must be given to the Instructor-in-charge personally.
  - A make-up test shall be granted only in genuine cases where - in the Instructor's judgment - the student would be physically unable to appear for the test.
  - In case of an unanticipated illness preventing a student from appearing for a test, the student must present a Medical Certificate from BITS medical centre.
  - Requests for make-up for the comprehensive examination – under any circumstances – can only be made to Associate Dean, Instruction Division.

Instructor-in-charge, CS F342