BIRLA INSTITUTE OF TECHNOLOY & SCIENCE PIANI
INSTRCTION DIVISION
FIRST SEMESTER 2017-18
(Course Handout (Part II)

20 August 2021

In addition to Part I (General Handout for all courses appended to the time table, this portion gives further specific details of the course

Course No.: **EEE/ INSTR F-313**

Course Title: **Analog & Digital VLSI Design**

Instructor-in-Charge: **Dipankar Pal**
Team of Instructor: **Dipankar Pal and Apurba Chakraborty**

1. Course Description

The course presents a broad base of circuit-techniques used in designing analog and digital VLSI. Current mirror and temperature invariant source for biasing, op-amp topologies, feedback, noise models, MOS inverter, switching circuits, combinational and sequential circuits, memory design shall be discussed. Additionally, an overview of IC-fabrication process, design rules and scaling shall be introduced in the beginning.

2. Scope and Objective

To understand the circuit approach to VLSI design. After doing this course, the students ideally should be able to design both analog and digital full-custom circuits that are implementable in integrated form.

3. Book

Text Book

i. Rabay, J. M., Chandrakashan, A. and Borivoje, N., "Digital Integrated Circuit Design: A Design Perspective", PHI Leaning Pvt. Ltd.
ii. Behzard Razavi, "Design of Analog Integrated Circuit", Tata McGraw Hill, 2001

Reference Books

i. Kang, S. M. and Leblebici, Y., "CMOS Digital Integrated Circuits", McGraw Hill International Edition, 3rd Edition 2003
ii. John, David & Martin, K., "Analog Integrated Circuit Design", John Wiley & Sons Inc. 2002

4. **Course Plan**

Lecture No.	Learning Objective	Topics to be Covered	Reference
1-2	To be introduced to the subject	Introduction to VLSI Design Technology	Lecture Notes/ Slides
3-6	Understanding of technology generation	Scaling	Lecture Notes/ Slides, Chapter 3.5 of RB 1
7-10	To understand layout rules for VLSI Design	CMOS Technology, Design Rule Check, Capacitors	Chapter 1 & 2 of TB 1, Chapter-2.4 of RB 1,
11-18	To learn analog circuit elements	Advanced current mirrors, voltage reference, op-amp topologies	Chapters 5, 11, 9, 8 of TB 2
19-24	To understand the concept of noise	Noise: Time domain and frequency domain analysis, noise models of circuit elements	Chapter 4 of RB 2
25-30	To learn combinational digital circuit elements	CMOS inverter, performance, delay, robustness, noise margin; static CMOS design, ratioed logic, dynamic CMOS design	Lecture Notes/ Slides, Chapter 5 & 6 of TB 1
31-36	To learn sequential digital circuit elements	CMOS sequential circuits, latches, registers, flip-flops, timing issues, hold time, set-up time, delays	Lecture Notes/ Slides, Chapter 7 of TB 1
37-40	To learn memory-design techniques	Static & Dynamic RAM, non-volatile memory	Lecture Notes/ Slides, Chapter 10 of RB 1

5. **Evaluation Scheme:**

Component	Duration	Weightage	Date, Time and Venue of Examination	Remarks
Quiz (30%) including Unstructured Lab	3 X Online-Quizzes (15 mts.) = 30%	*30%	*IC to announce	Open book
Mid Sem Examination	90 minutes	30%	AUGSD to announce	Closed book
Comprehensive Examination	120 minutes	40%	AUGSD to announce	Closed book

6. **Chamber Consultation Hour:** To be announced in class.
7. **Notices:** Moodle/ G-Classroom/ email (only in selected cases)
8. **Make-up Policy:** As per the Institute-norms, only in genuine cases.

Instructor-in-Charge
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